Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



THIS SPEC IS OBSOLETE

Spec No: 002-04942

Spec Title: AN204942 - F2MC - 8L FAMILY, EMC DESIGN GUIDE

Replaced By: NONE

AN204942

F²MC - 8L Family, EMC Design Guide

In the following description, the EMC design guide of 8-bit Cypress microcontroller will be discussed. It describes how external power supply should be connected to the Vcc and Vss pins and offers some suggestions. An overview of internal supply of MCU is made as well to have a better understanding of the design. The EMI measurements in the following described tests are just example measurements. The measured emissions are no data, which are specified in the DS of the microcontroller series.

OBSOLETE

Contents

1 Introduction....1
2 Rules to create a good Layout....2
3 Crystal Oscillator Circuit....3
4 Power supply routing....4
5 Noise reduction for general IO pins....8
6 Function of certain MCU pins....9
7 EMI Measurement for F²MC-8L family....10
7.1 Measurement setup....10
7.2 Measurement procedure....10
7.3 Measurements....10
7.4 Blank check....11
7.5 Noise measurements on VCC....12
Document History....14

1 Introduction

In the following description, the EMC design guide of 8-bit Cypress microcontroller will be discussed. It describes how external power supply should be connected to the Vcc and Vss pins and offers some suggestions. An overview of internal supply of MCU is made as well to have a better understanding of the design. The EMI measurements in the following described tests are just example measurements. The measured emissions are no data, which are specified in the DS of the microcontroller series.

During the last designs the EMI of the Cypress F²MC-8L microcontroller series could be reduced step by step. The PLL multiplier circuit allows the usage of low crystal frequency to reduce high-frequency noise from the oscillator circuit.

The clock tree is mostly the cause of the noise. Therefore the driver capability of clock buffers is optimized and for one big buffer are used several small clock buffers.

The integration of On-chip bypass capacitors reduces the noise ripple on the internal power supply net so that the broadband noise on the IO pins is improved.

The following description is based on the MB89530 series, but the same situation exists for all current devices of the F²MC-8L family, with or without an external bus interface.

2 Rules to create a good Layout

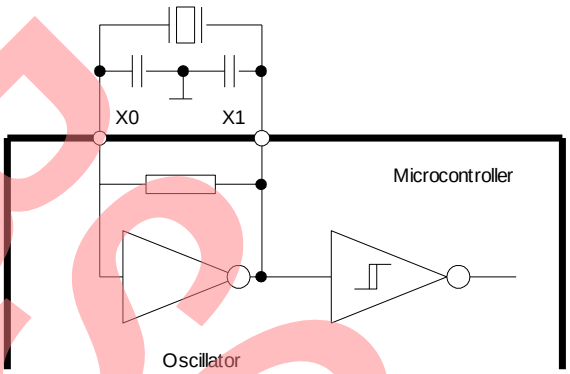
1. Use max. trace-width and min. length to connect VSS and VDD µC-pins to decoupling capacitors (DeCap)
2. Don’t use stub line to connect the DeCap to µC-pins, let flows the noise current direct through pads of DeCap
3. Use close ground plane direct below MCU package as shield
4. Use different ground systems for analogue, digital, power-driver and connector ground
5. Avoid loop current in the ground system, check for ground loops.
6. Use a star point ground below MCU for analogue and digital ground, use a second star point ground below 5V regulator for MCU, power-driver and connector ground
7. Don't create signal loop on the PCB, minimize trace length
8. Partitioned system into analogue, digital and power-driver section
9. Place series resistor or RC-block for the IO-circuit nearby MCU-pin to reduce the noise on the signal line.
10. Use a capacitor for each connector pin to reduce the noise of external lines, place this capacitor close to connector pin

OBSOLETE

3 Crystal Oscillator Circuit

Error! Reference source not found. shows the oscillator for the 8-bit family. For best performance, the PCB layout of this circuit should cover only a very small area. For the layout is recommended a PCB with two or more layers. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator, and ground lines. The lines of the oscillation circuit should not cross lines of other circuits.

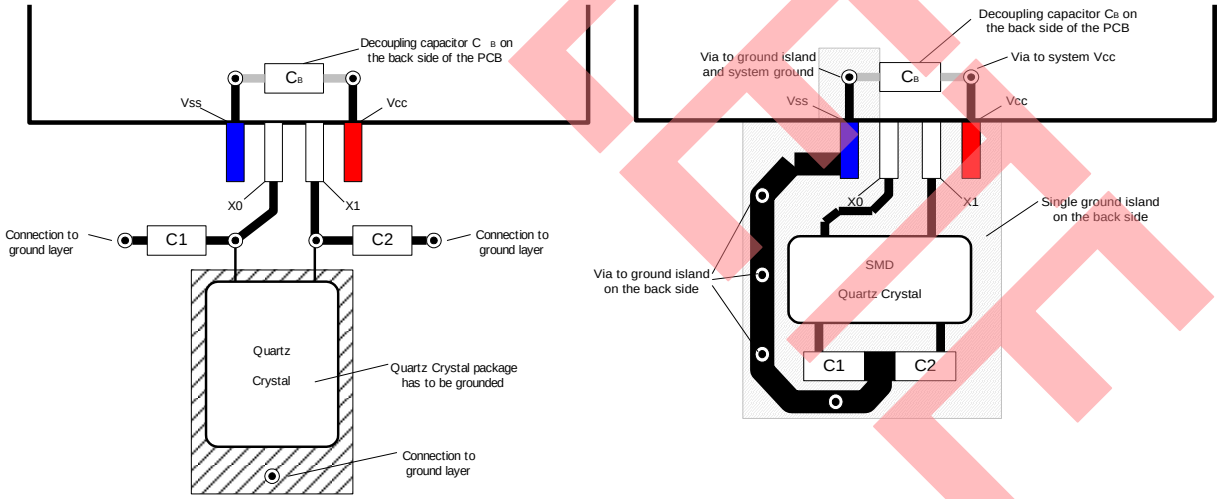
Figure 1. Principle of the Oscillator circuit



It is necessary to avoid coupling noise into the power supply (pin 81/84) of the clock circuit.

The crystal oscillator has to be connected with short lines to X0/X1 and Vss. Note that pin X1 is the output of inverter. Particularly this track should have a short length.

Figure 2. Layout example for oscillator circuit



a) Layout example for a leaded quartz crystal worse layout design, because C1 and C2 are wrong connected to VSS

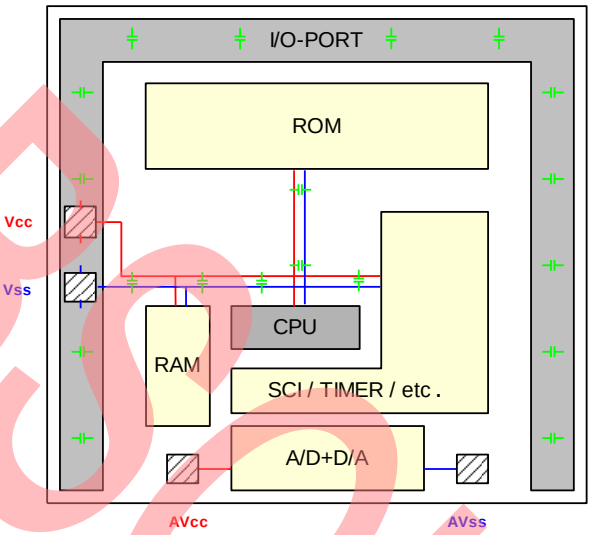
b) Layout example for a SMD quartz crystal better layout design, because C1 and C2 are connected to Vss and than after with the system ground

OBSOLETE

4 Power supply routing

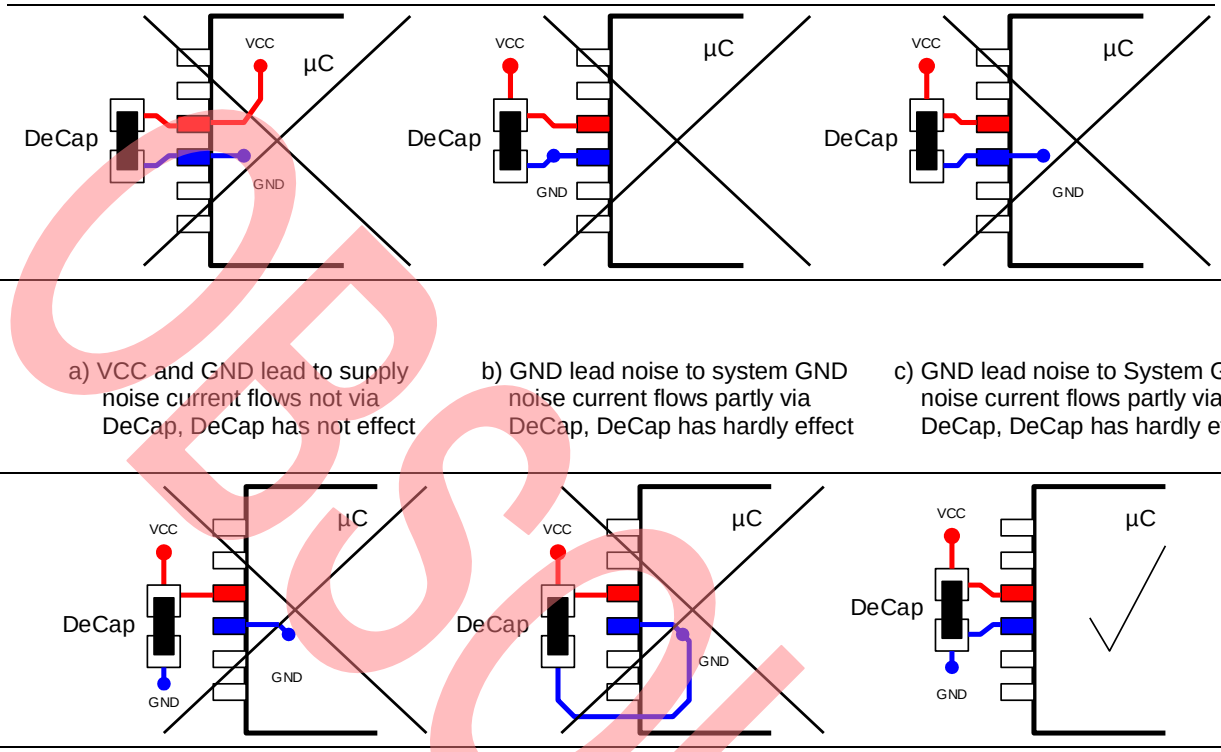
One topic our noise reduction technology is the bypass capacitors. By placing of modules inside the chip, it is possible to connect a bypass capacitor with low impedance where power supply lines are short, effectively reducing the noise to very low flow levels. These bypass capacitors are place into power supply of IO and logic.

Figure 3. Structure of power supply for MCU core and IO-Port



OBSOLETE

Figure 4.The exactly use of the DeCap (decoupling capacitor)



a) VCC and GND lead to supply noise current flows not via DeCap, DeCap has not effect

b) GND lead noise to system GND noise current flows partly via DeCap, DeCap has hardly effect

c) GND lead noise to System GND noise current flows partly via DeCap, DeCap has hardly effect

d) VCC and GND lead to supply noise current flows not via DeCap, DeCap has not effect

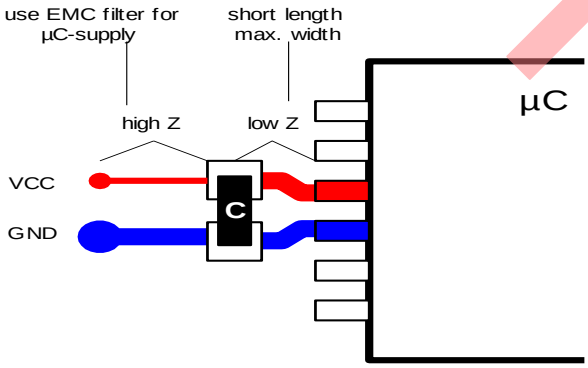
e) GND is not short connected to DeCap. between GND and DeCap flows a loop current DeCap has hardly effect

f) DeCap correct connected to µC and power supply. high speed current will be supported from DeCap

The high-speed current (di/dt) will be supported from the decoupling capacitor only.

Therefore use traces with max. width and min. length between Vss/Vcc pin and DeCap. After DeCap use thin traces to route the trace to the power supply system.

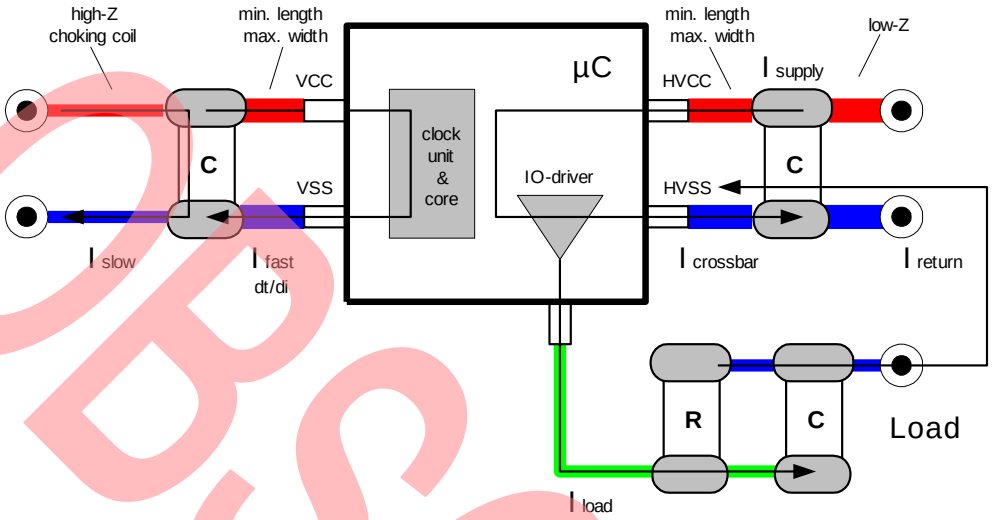
Figure 5. The noise current flows return over the ground line



The exactly use of decoupling capacitors for the Vcc and Vss pins is the basis to reduce the noise, but also the return way between load and MCU ground is not neglect.

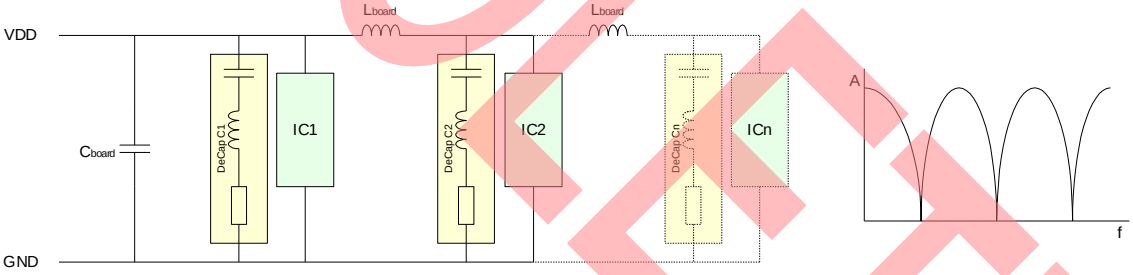
OBSOLETE

Figure 6. The noise current flows return over the ground line



To ensure an efficient decoupling of the power supply, two capacitors should be placed close on each Vcc pin. The values of both capacitors should have a relationship of about 1:100. Typical values are e.g. 100nF (XR7) and 1nF (COG). The accurate value is depended on the application board, e.g. impedance of PCB or the length of supply lines. However, all of the DeCaps on the PCB should have the same value.

Figure 7. The use of several values of DeCaps lead to undefined resonance frequencies, that's why all DeCaps should have the same value.



For 2-layer boards should be used a closed ground plane (located directly below the MCU). The Vcc supplies should be taken from the bottom layer.

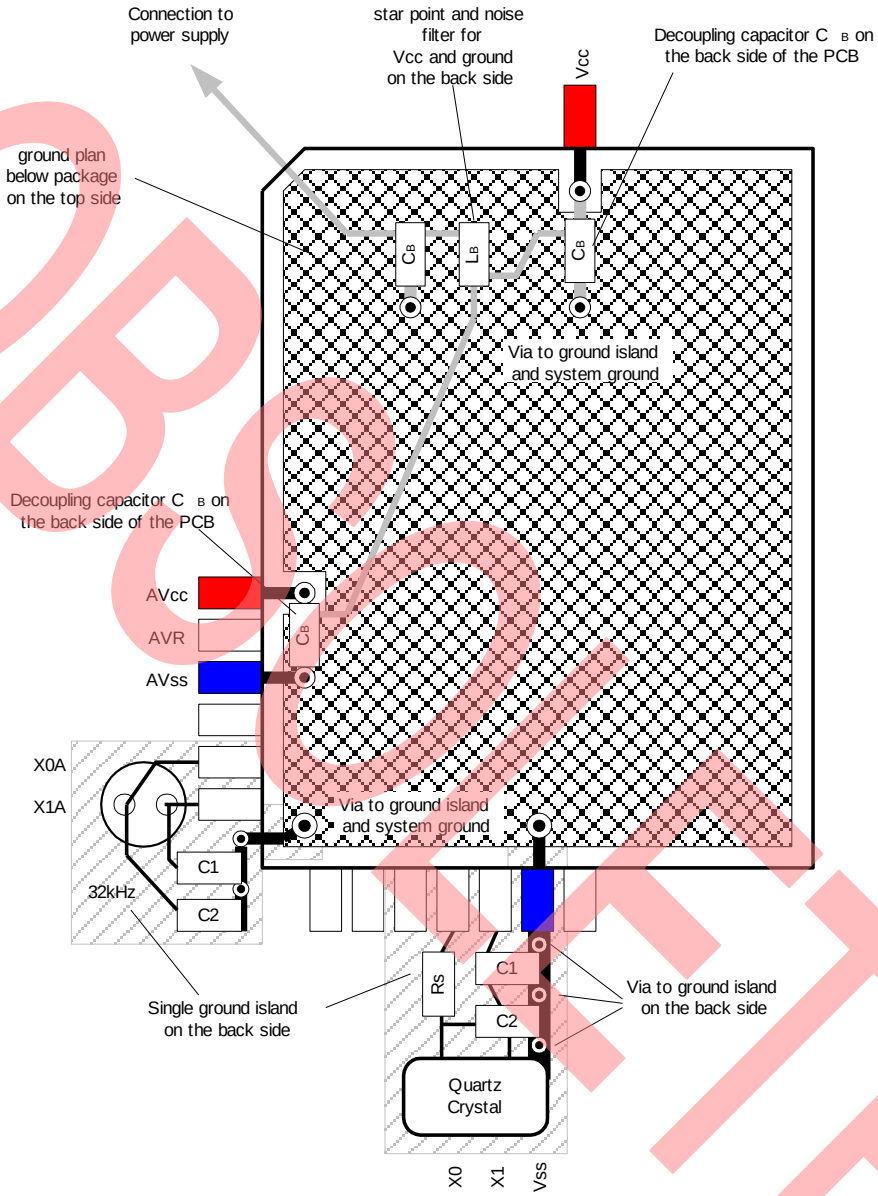
For 4-layer boards should be used the inside layers for GND and Vcc supplies. In this case, both layers form additional capacitor (broadband behaviour) for the power supply.

Figure 8 shows a layout example for the connection of powers supply on the MCU.

This method of Vcc connection reduces the loop of the Vcc lines around the MCU, thus reducing noise emission. A variation of this circuit may be needed, if separate filtered supply voltages are routed to the A/D supplies (pin AVCC/AVSS).

OBSOLETE

Figure 8. F²MC-8L family with main- and subclock, recommended layout for multiple layers PCB



OBSOLETE

Note:

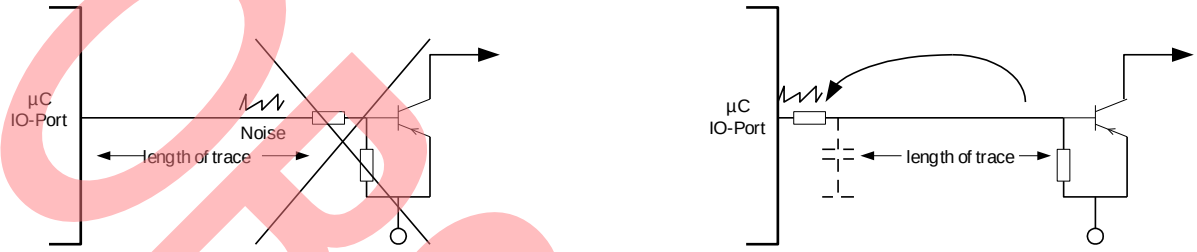
All decoupling capacitors on the Vcc pins should have the same value.

These capacitors should be placed close to the Vcc pin. The Vcc/Vss current should flows through the pad of the capacitor.

5 Noise reduction for general IO pins

To reduce noise, make sure to connect the Vss or Vcc with smoothed power supply, because the noise on the power supply will also distributed via IO-pin, which is configured as static low or high output. **Error! Reference source not found.** shows an example to reduce the noise on output lines.

Figure 9. Place the series resistor close to IO pin because so will be reduced the noise of output



Note: To reduce noise, make sure to connect unused input pins to Vss or Vcc (Use pull-down or pull-up resistor, please check the DS of the microcontroller series).

Also, especially if CMOS Logic is used, floating gates could generate problems regarding high input currents and latch up.

OBSOLETE

6 Function of certain MCU pins

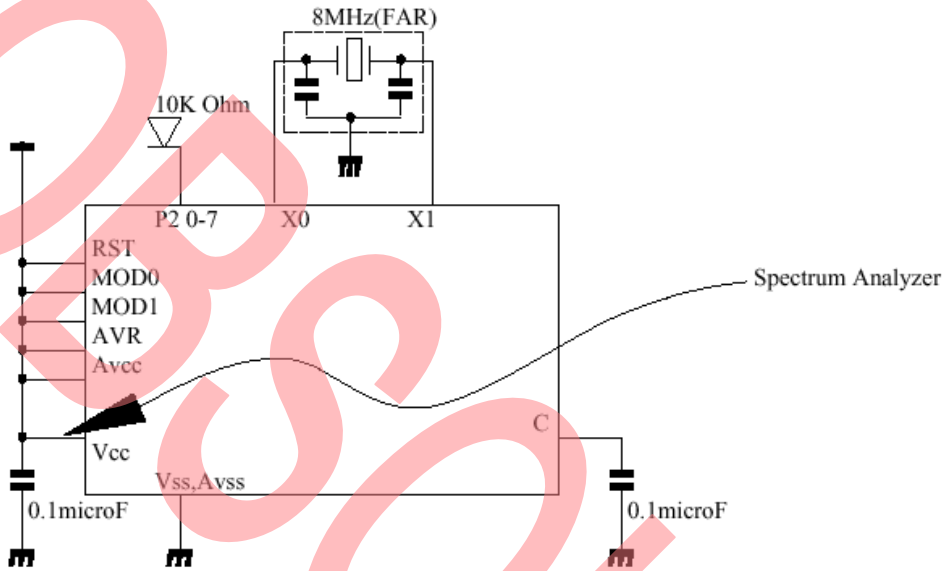
Pin name	Function
VDD	Main supply for IO buffer and MCU core
VSS	Main supply for IO buffer and MCU core close to crystal oscillator
AVCC	Power supply for the A/D converter
AVR	Reference voltage input for the A/D converter
AVSS	Power supply for the A/D converter
X0 X0A	Oscillator input, if not used so shall be connected with pull-up or pull-down resistor (see please DS)
X1 X1A	Oscillator output, the crystal and bypass capacitor must be connected via shortest distance with X1 pin, if not used so shall be open

OBSOLETE

7 EMI Measurement for F²MC-8L family

7.1 Measurement setup

Figure 10. Set-up for noise measurement on power supply



7.2 Measurement procedure

- RF- voltage, measured on VCC power supply by BI mode RUN
- RF- voltage, measured on VCC power supply by BI mode RESET

7.3 Measurements

Sample: MB89538A, MB89538AL, MB89535A

Measurement condition: Ta = 25 deg.C

Power supply: Vcc = 5.0V / 3.0V

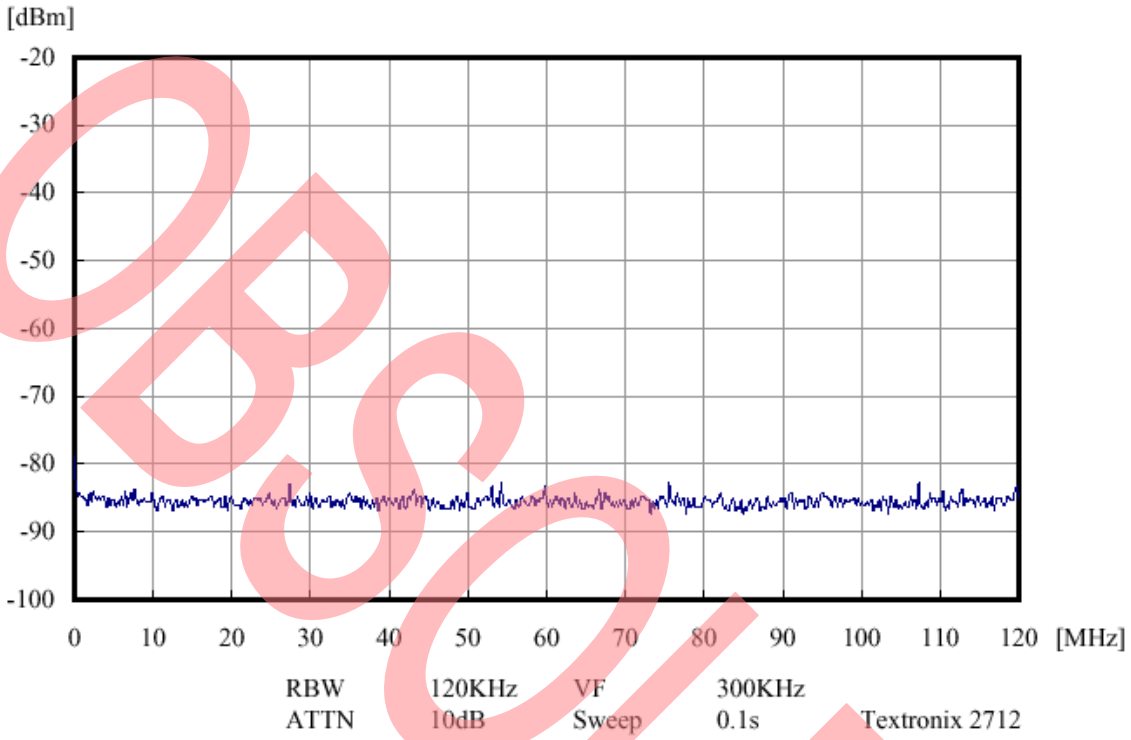
Crystal: 8MHz (FAR)

Frequency range: 0MHz to 120MHz, BW: 120kHz

OBSOLETE

7.4 Blank check

Figure 11. Noise measured on VCC power supply, blank check



OBSOLETE

7.5 Noise measurements on VCC

Figure 12. MB89538A - Noise measured on VCC power supply, BI-mode RUN

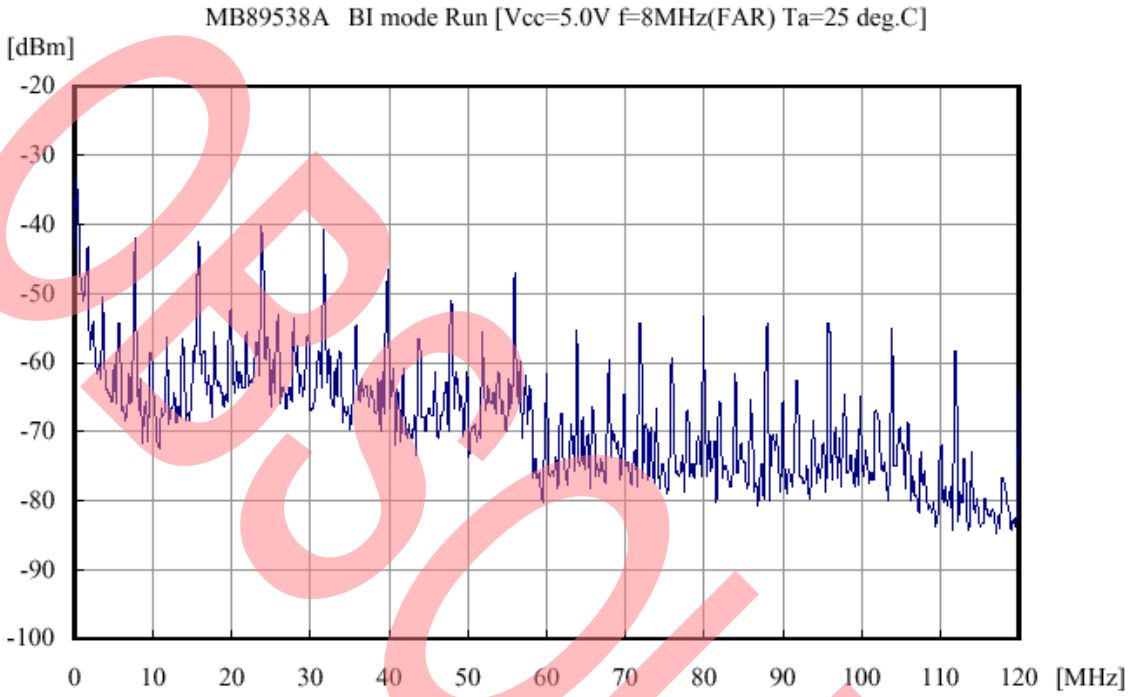
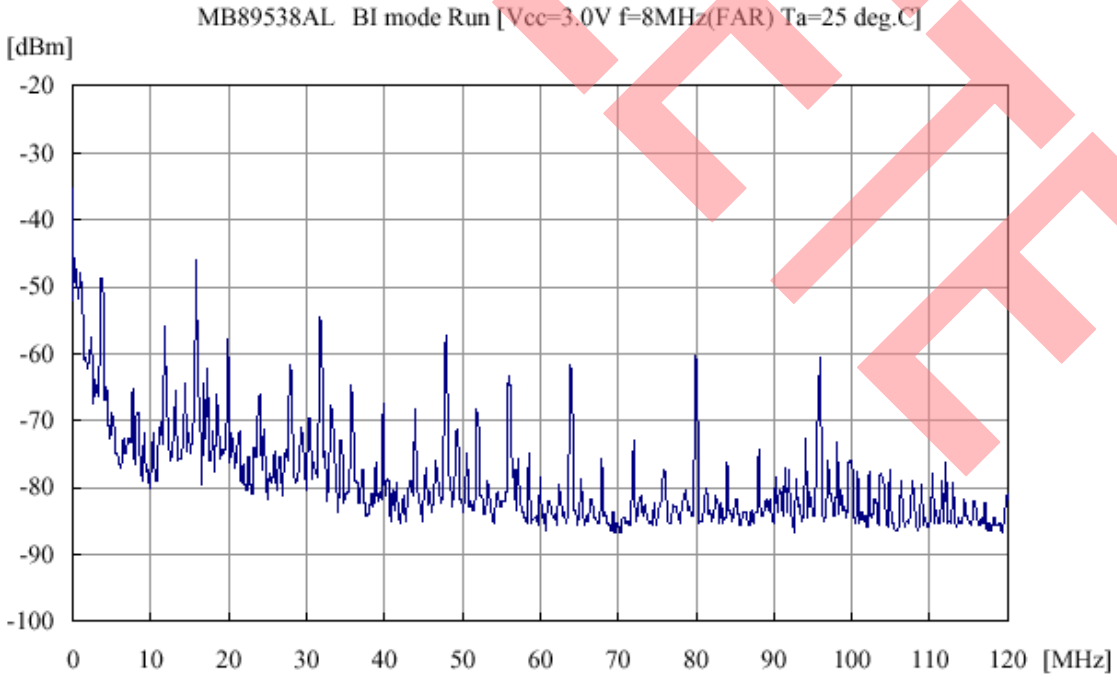
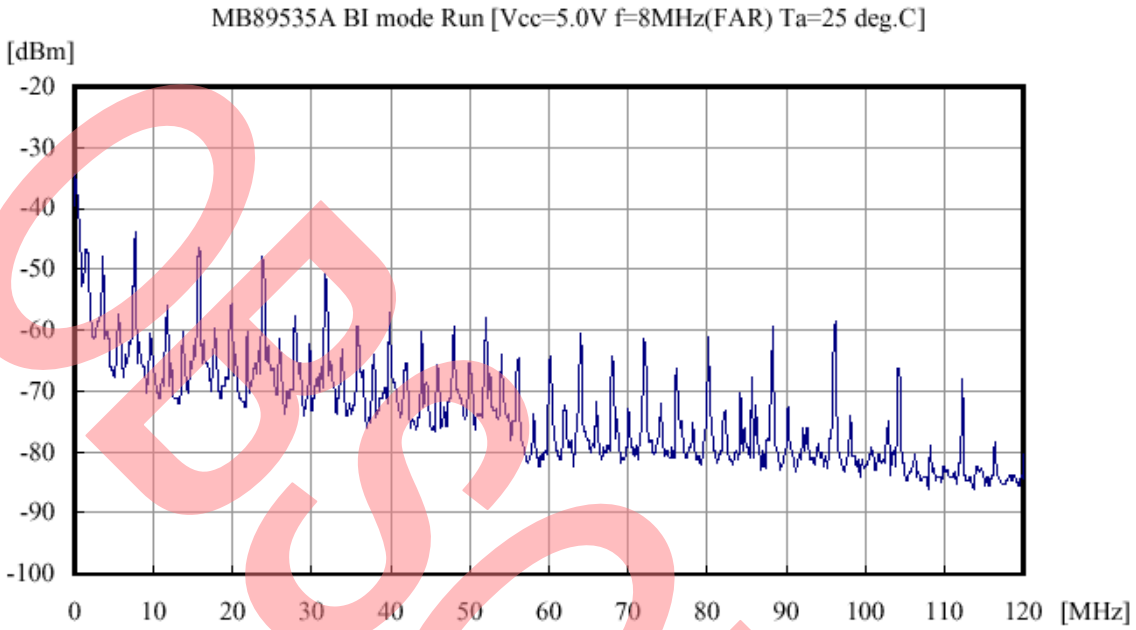


Figure 13: . MB89538AL - Noise measured on VCC power supply, BI-mode RUN



OBSOLETE

Figure 14. MB89535A - Noise measured on VCC power supply, BI-mode RUN



OBSOLETE

Document History

Document Title: AN204942 – F²MC - 8L Family, EMC Design Guide

Document Number: 002-04942

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NFL.	07/04/2002	V1.0, Initial draft
		NFL	07/18/2002	V1.1, Description DeCap added
*A	5278888	WOFR	05/20/2016	Migrated Spansion Application Note “MCU-AN-389024-E-V11” to Cypress format.
*B	5612332	WOFR	01/31/2017	Spec obsoleted, no further updates planned.

OBSOLETE

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

OBSOLETE

PSoC is a registered trademark and PSoC Creator is a trademark of Cypress Semiconductor Corporation. All other trademarks or registered trademarks referenced herein are the property of their respective owners.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

Phone : 408-943-2600
Fax : 408-943-4730
Website : www.cypress.com

© Cypress Semiconductor Corporation,2002-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.