Voltage Sequencer Example Project

1.1

Features

- Controlled power-up and power-down sequencing of 4 DC-DC power converters
- Automatic power converter fault response handling
- Automatic re-sequencing in response to fault conditions
- Demonstrates how general purpose control inputs can influence sequencing
- Demonstrates how to generate user-defined general purpose status outputs
- Configured to run on the PSoC Power Management Expansion Board Kit (CY8CKIT-035) plugged into the PSoC Development Kit (CY8CKIT-001)

General Description

This example project demonstrates the basic operation of the Voltage Sequencer component.

Development Kit Configuration

1. The PSoC 3 or PSoC 5LP Processor Module must be installed on the PSoC Development Kit (DVK)
2. The PSoC DVK must be configured for 5V operation using SW3
3. All VDDIO banks must be set to VDD using J2 through J5 on the PSoC DVK
4. *Do not connect the PSoC Power Management EBK yet*
5. Build the project and program the CY8C3866AXI-040 using a MiniProg3 programmer
6. Remove power from the PSoC DVK and attach the PSoC Power Management EBK to Port A of the PSoC DVK
7. The PSoC Power Management Expansion Board Kit (EBK) must be configured to draw power from the PSoC DVK (J5 jumper shorting positions 2 and 3)
8. Apply power to the PSoC DVK

Project Configuration

The example project consists of the Voltage Sequencer, Power Monitor, Status Register and Character LCD components. The design schematic is shown in Figure 1. The blue annotation

components used in the middle of the schematic show the relevant components that are installed on the PSoC Power Management EBK, most notably the power converters and the components used for voltage sensing. The Voltage Sequencer component is responsible for controlling the power-up and power-down sequence of the power converters. The Power Monitor component is used to monitor the power converter output voltages to generate the power good (PGOOD) signals for the Voltage Sequencer. The Status Register is used to monitor the state of the Voltage Sequencer and the power system.

The four power converter enables are mapped to PSoC GPIO pins P3[4], P3[5], P3[6] and P3[7] respectively. The four power converter output voltages are mapped to PSoC GPIO pins P4[0], P4[2], P4[4] and P4[6] respectively. The 2 switches and the 4 LED's on the development kit should be wired up as shown in Figure 1.

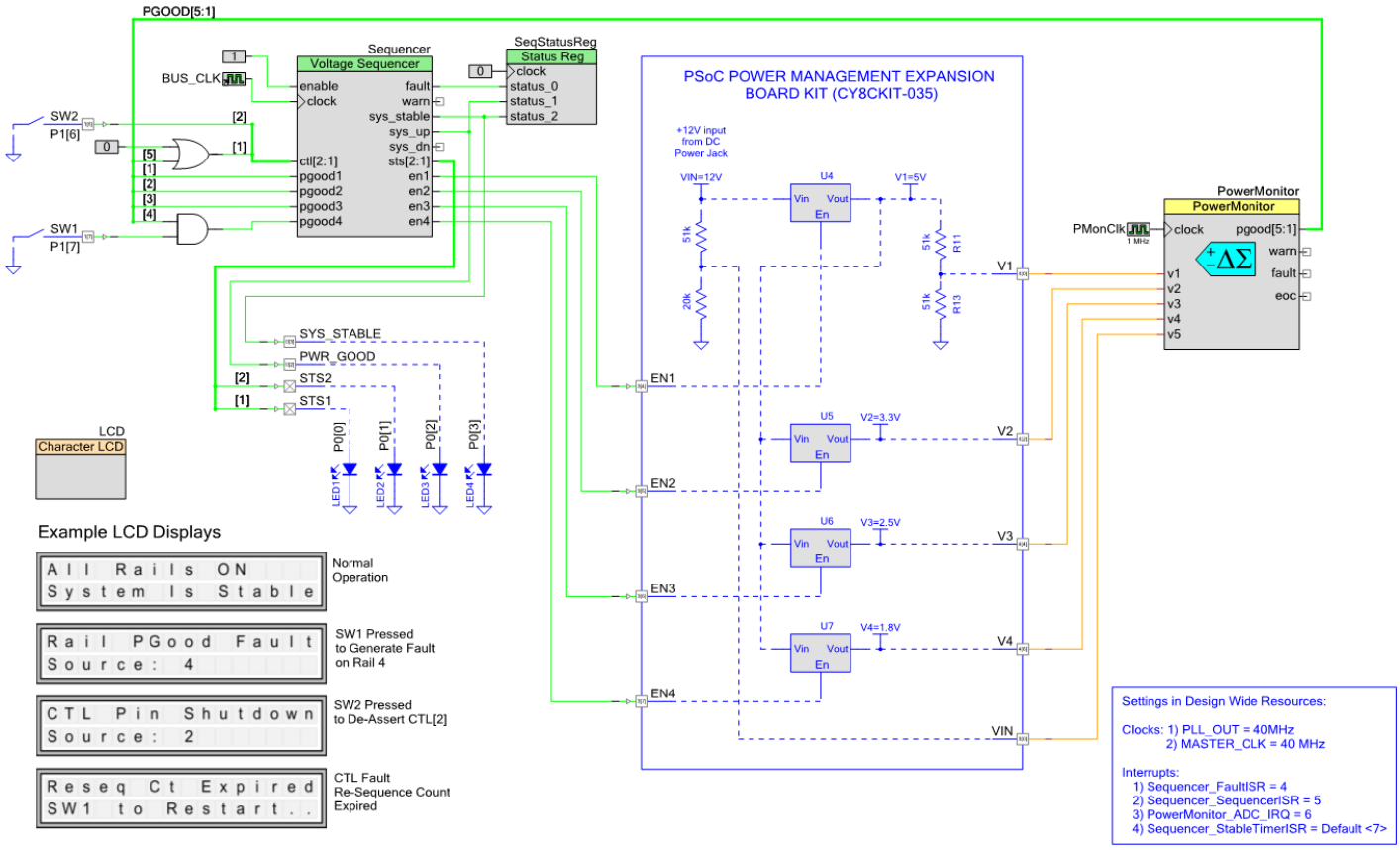


Figure 1. Example project design schematic

The Voltage Sequencer and the Power Monitor components are both configured to support the 4 power converters installed on the PSoC Power Management EBK. The component configuration windows are shown below.

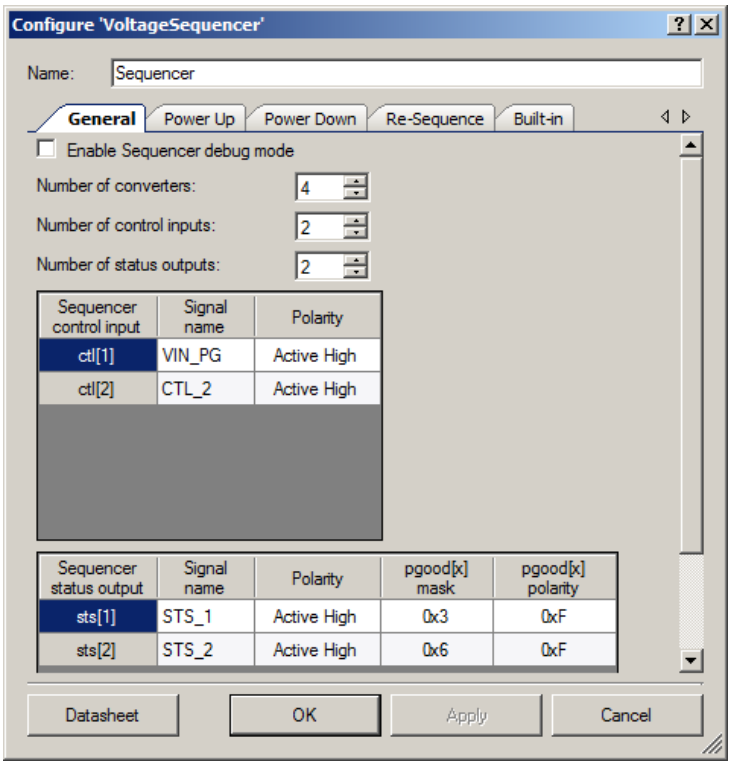


Figure 2. Voltage Sequencer component configuration - General tab

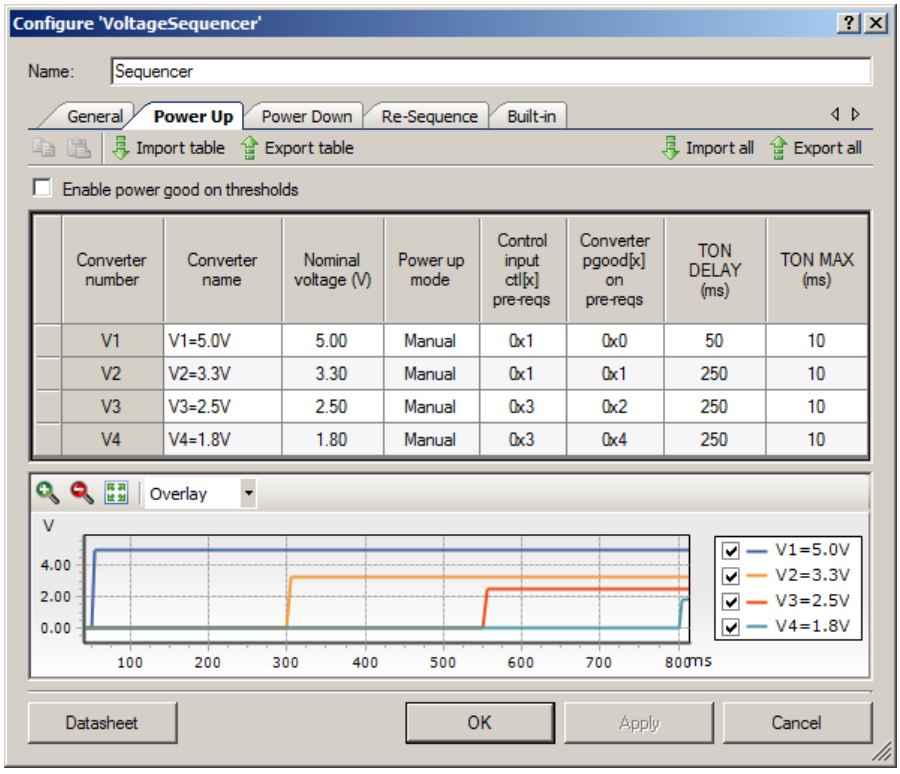


Figure 3. Voltage Sequencer component configuration – Power Up tab

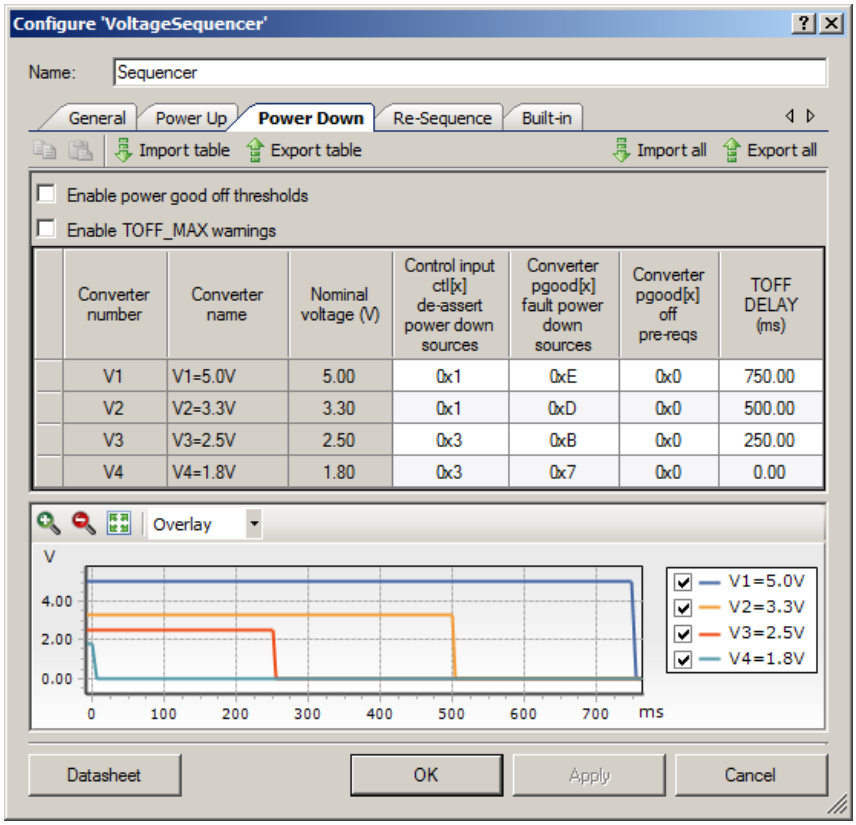


Figure 4. Voltage Sequencer component configuration – Power Down tab

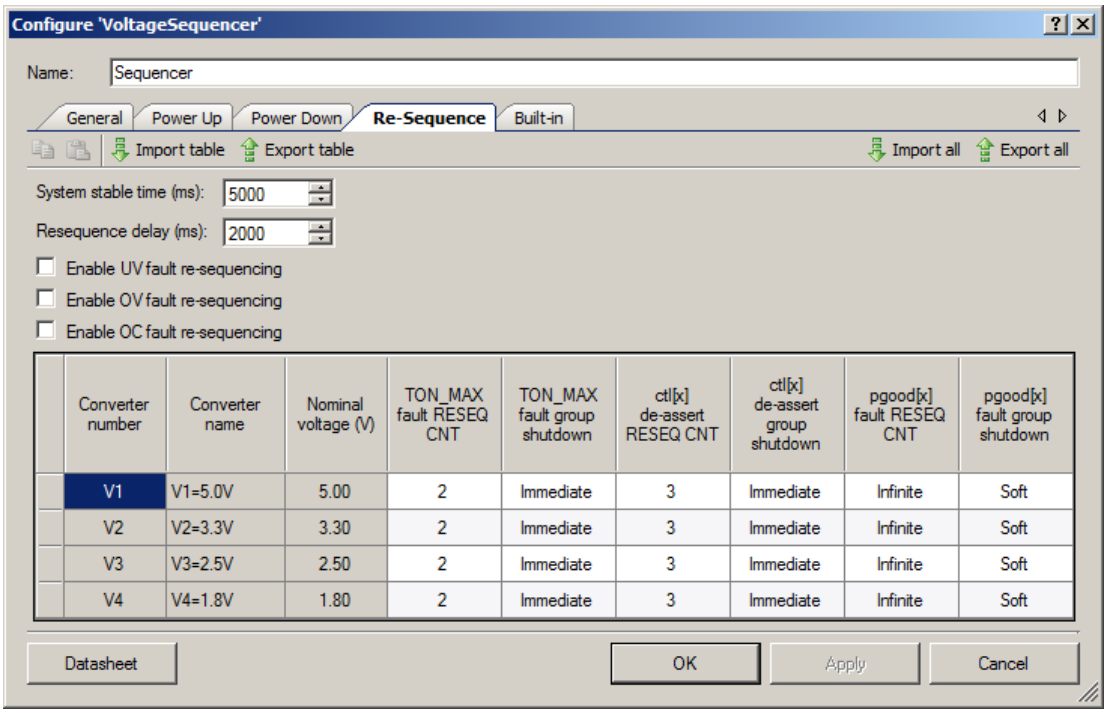


Figure 5. Voltage Sequencer component configuration – Re-Sequence tab

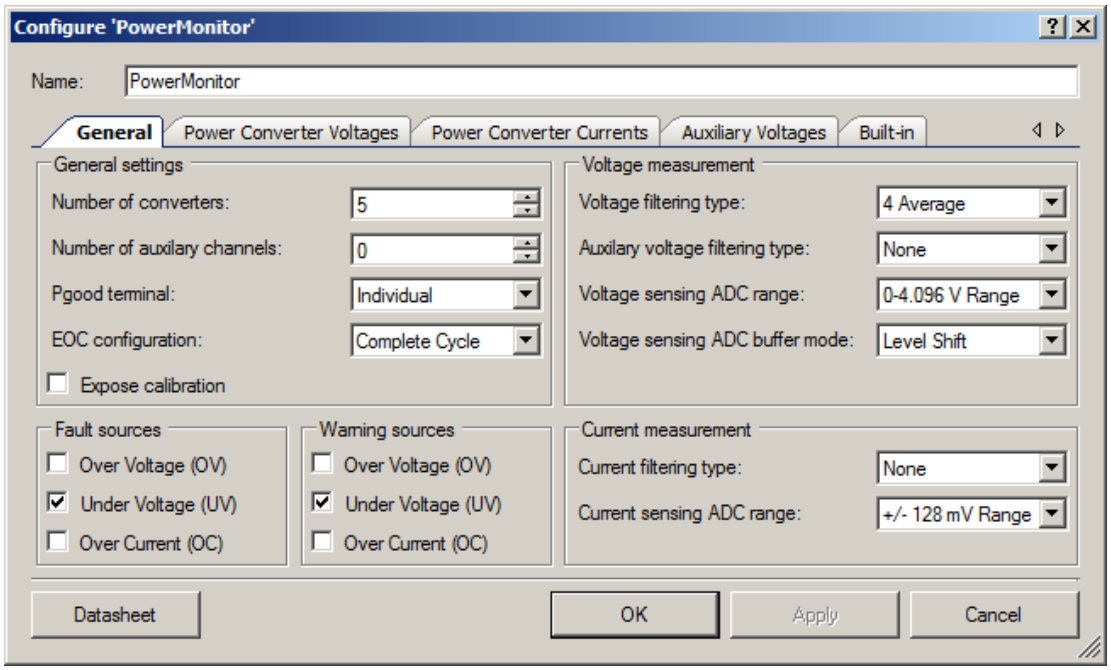


Figure 6. Power Monitor component configuration – General tab

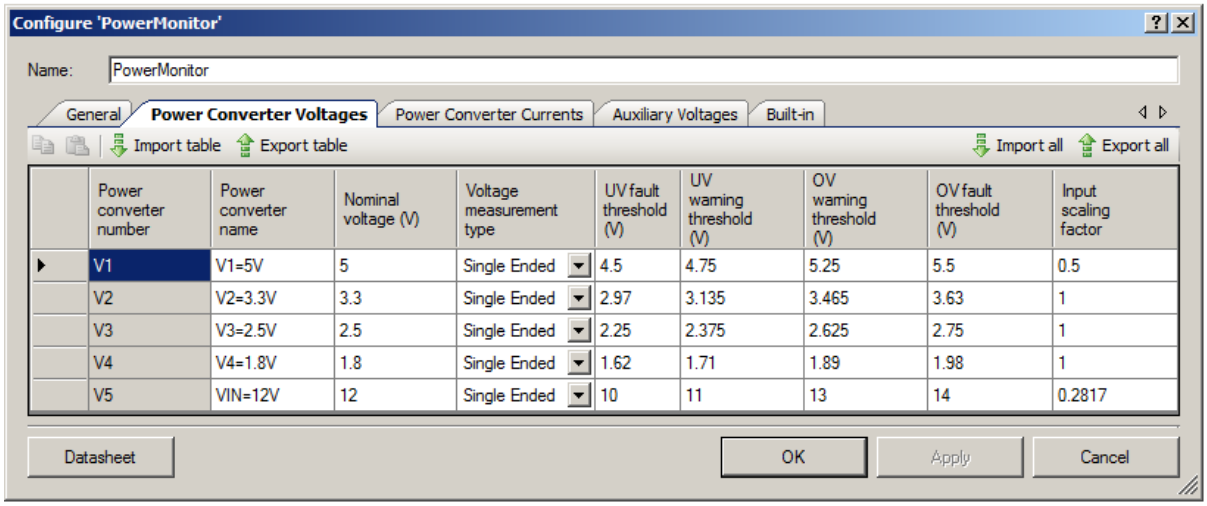


Figure 7. Power Monitor component configuration – Power Converter Voltages tab

The Character LCD is used in its default configuration. For more information on the usage of the Character LCD and Status Register components, please refer to the corresponding component datasheets.

Project Description

In the main firmware routine, all components are started and interrupts are enabled to the 8051 CPU core as required for both the Voltage Sequencer and the Power Monitor components.

The Power Monitor component is configured to monitor the output voltages of the 4 power converters installed on the PSoC Power Management EBK and generate power good (PGOOD) signals for the Voltage Sequencer component. The Voltage Sequencer is responsible for sequencing the power converters up and down based on the user-defined sequencing parameters entered into the configuration GUI.

Pressing SW1 on the development kit simulates a power converter fail by de-asserting the PGOOD signal from the Power Monitor component. The Voltage Sequencer will then shutdown all other power converters as described in the configuration GUI. Pressing SW2 on the development kit simulates de-assertion of a general purpose control input signal. The Voltage Sequencer will then shutdown 2 of the power converters as described in the configuration GUI. Automatic re-sequencing has been configured for both of these simulated conditions.

The LCD displays the status of the system in response to the various simulated conditions. The 4 LEDs on the development kit are used to display sequencer output signals as follows:

LED1: User configurable STS[1] output = pgood[2] & pgood[1]
LED2: User configurable STS[2] output = pgood[3] & pgood[2]
LED3: Power system up = all power converters are on and good
LED4: Power system stable = system has been up for user-defined period of time

Expected Results

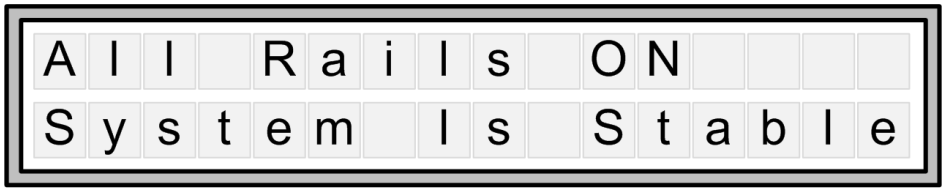
On power up, the Voltage Sequencer will bring up all the power converters in sequence with a 250 ms delay between them. This can be observed by viewing the green colored LEDs on the Power Management EBK.

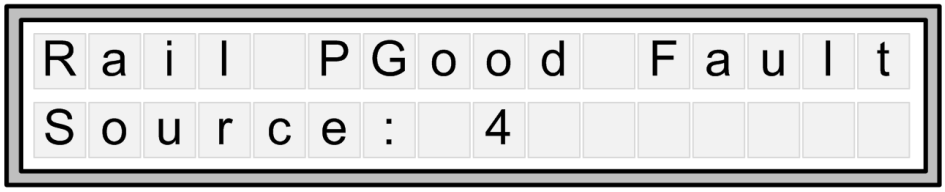
Pressing SW1 simulates a fault condition on power converter rail 4, causing all converters to shut down and attempt to re-sequence. Holding down SW1 will prevent the system coming back up. Releasing SW1 will enable the sequencer to complete the power-up re-sequence.

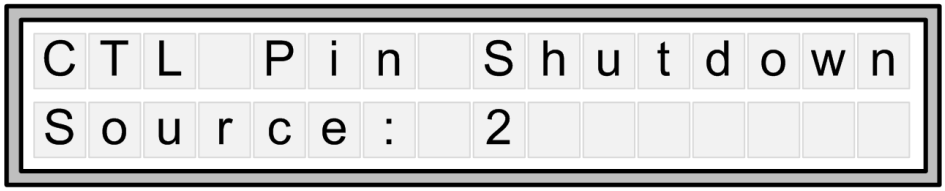
Pressing SW2 simulates the de-assertion of one of the general purpose control inputs causing converter rails 3 and 4 to shut down and attempt to re-sequence. Holding down SW2 will prevent rail 3 turning on, since the Voltage Sequencer has been instructed to wait for that control input to be high. Releasing SW2 will enable the sequencer to complete the power-up re-sequence.

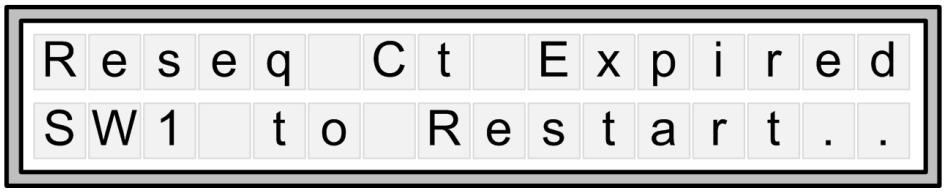
The Voltage Sequencer has been configured to automatically attempt re-sequencing only 3 times in response to pressing SW2. After the 3rd failed re-sequence attempt, rails 3 and 4 will remain off until the Voltage Sequencer is instructed to try again through a command. Pressing SW1 in this condition will send the command to re-try.

Examples of what you should see on the LCD in various situations are shown below:









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