MDIO Basic Example

1.0

Features

- Demonstrates how to connect the MDIO Interface component to an MDIO host device
- Demonstrates the Basic mode of the MDIO Interface component
- Shows how to manually examine the received frame and retrieve the relevant information
- Configured to run on the PSoC Development Kit (CY8CKIT-001)

General Description

This example project demonstrates the basic operation of the MDIO Interface component. The basic mode allows the user to process the MDIO frame using firmware and gives full control over the implementation of the data transfers and memory accesses. The frame information is received from the MDIO host, and the extracted information is displayed on the character LCD on the CY8CKIT-001 Development Kit.

Development Kit Configuration

1. The PSoC 3 or PSoC 5LP Processor Module must be installed on the PSoC Development Kit (DVK)
2. Configure the pin connections as shown on the project schematic
3. Apply power to the PSoC DVK
4. Build the project and program the CY8C3866AXI-040 using a MiniProg3 programmer
5. Observe the frame information on the LCD

Project Configuration

The example project consists of the MDIO Interface and the Character LCD components. The project assumes that an MDIO host device is available and that necessary pin connections can be made to the Development Kit. The design schematic is shown in Figure 1. The blue annotation components in the schematic show the external connections required for correct component operation. This requires a (recommended) 330 Ohm pull-up resistor on the MDIO data line to a 1.2V supply, and a common ground connection between the host and the interface.

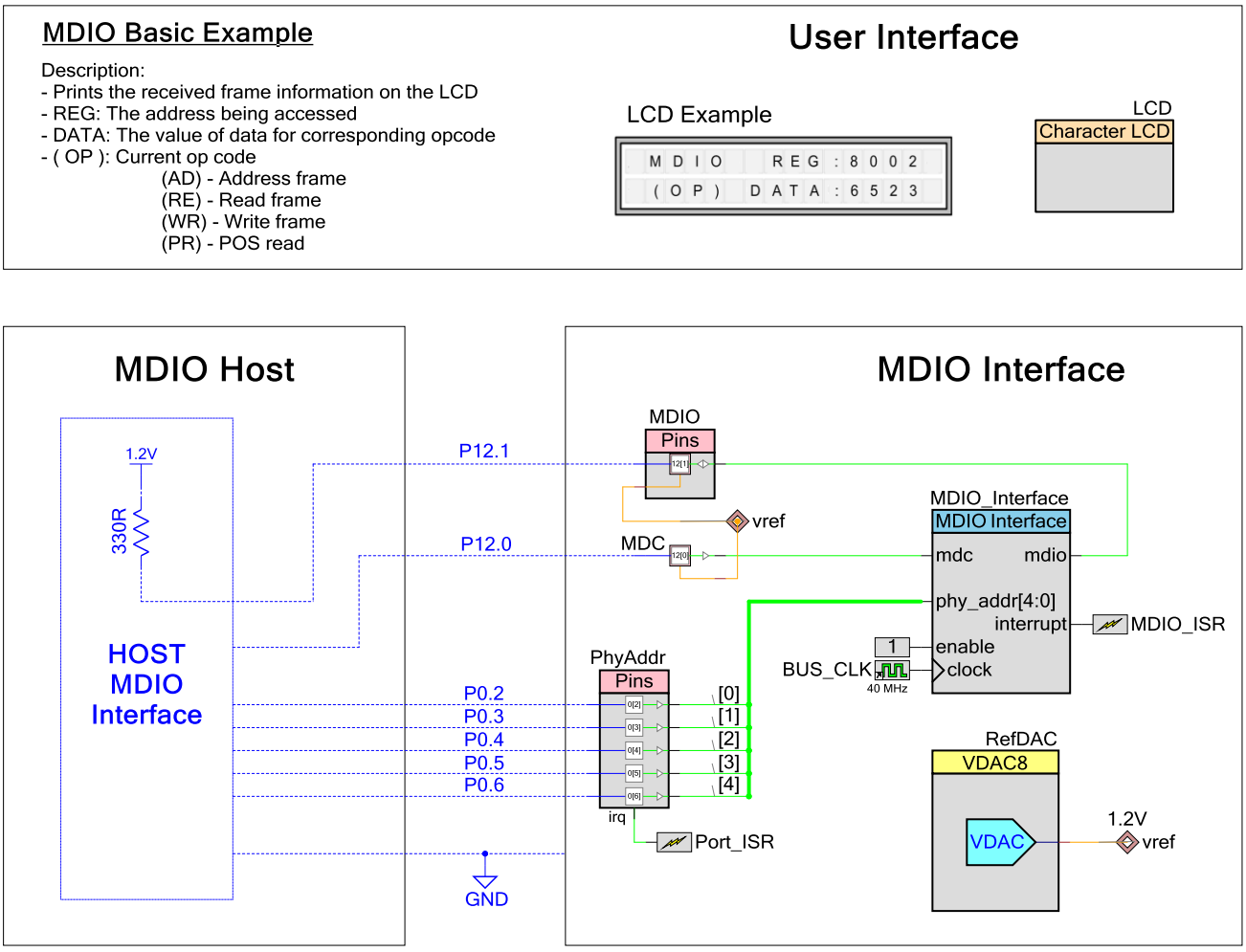

Figure 1. Example project design schematic

Pin configuration

The pins are configured as shown in the table below. Aside from these, the MDIO line needs to be connected to a 1.2V supply through an external 330 Ohm resistor, and the ground connection of the Development Kit must be tied to the MDIO Host.

Pin Name	Port	Description
MDC	P12[0]	The MDC clock signal connected to the MDIO host's MDC terminal
MDIO	P12[1]	Terminal for the MDIO data signal
PhyAddr[4:0]	P0[6:2]	Configures the Physical address through hardware
LCD:LCDPort[6:0]	P2[6:0]	Connection to the Character LCD on the Dev. Kit

LCD Display

The Character LCD displays the address (REG), op code (OP), and data (DATA) information of the received MDIO frame. The op codes can be (AD) address frame, (RE) read frame, (WR) write frame, and (PR) pos read.



Customizer settings information

The customizer for the MDIO Interface component in Basic mode requires only configuration in the General tab.

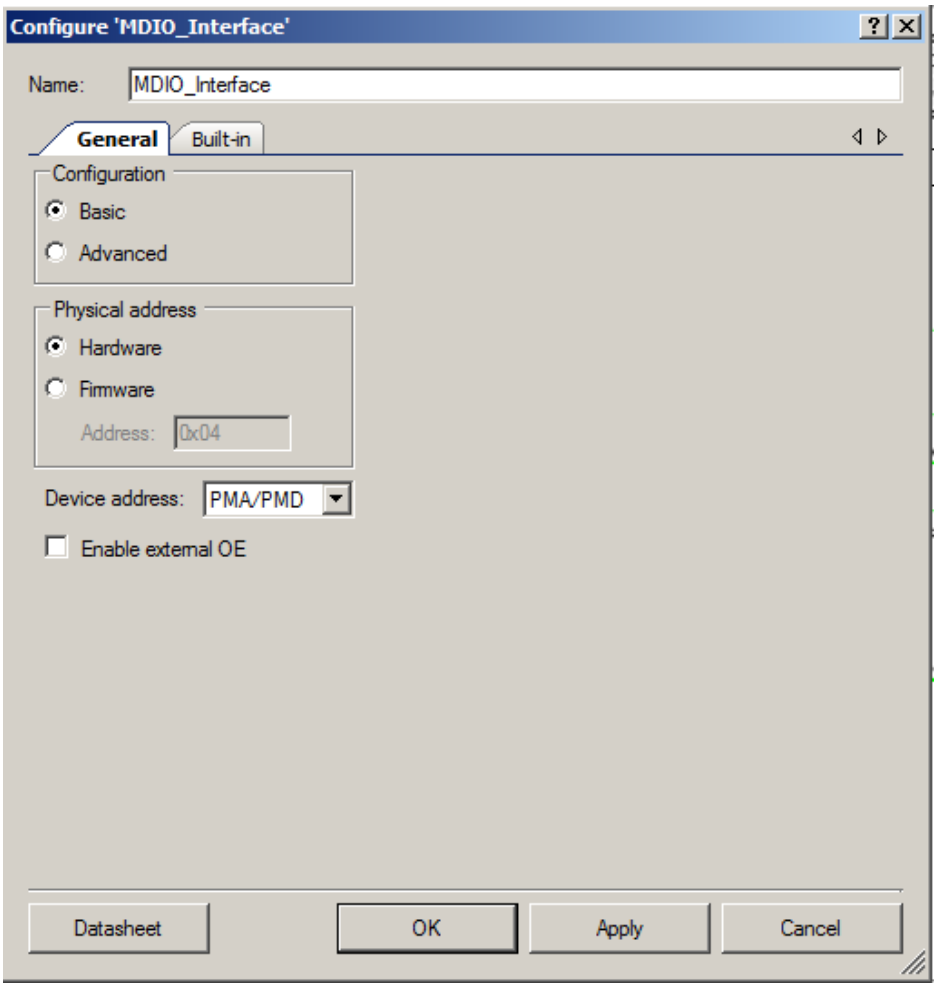

Figure 2. MDIO Interface component configuration - General tab

The component is set to Basic mode, the physical address is configured to Hardware, and the device address is set to PMA/PMD. The Enable external OE checkbox is unchecked.

Project Description

In the main firmware routine, the MDIO Interface component is configured to have a valid address space of 512 words starting from a base address of 0x8000. Upon receiving a frame from the host, the extracted information is displayed on the character LCD. If the accessed address during a read operation is not within the valid address space, then the device returns 0xFFFF (accessed address < valid address) and returns 0x0000 (accessed address > valid address) to the host.

Expected Results

The user should observe the address, data, and the op code information sent by the MDIO host on the character LCD. If the address is outside the range of the valid address space, then the data value received by the MDIO host should be 0xFFFF for an accessed address that is less than the valid address, and should be 0x0000 for an accessed address that is greater than the valid address.

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