DelSig_SPIM Example Project
1.00

Features

- 8-channel sequenced Delta Sigma ADC
- SPI Master
- Easy debugging using Character LCD

General Description

This example project is also a PSoC Creator starter design. This design shows a 16-bit differential ADC, hardware multiplexed into 8 channels, and transported over SPI. To test this design, a test project (DelSig_SPIM_Test) is available as a separate example project.

This starter design also includes advanced debugging techniques to detect and handle system level faults and conditions, such as a missing wire or missing device on the bus. The PSoC 0.1% internal voltage reference shows the additional BOM integration.

This design makes it easy to get started and utilize precision analog capability of PSoC.

Development Kit Configuration

The following configuration instructions provide a guideline to test this design with the DelSig_SPIM_Test Example Project. For simplicity, the instructions describe the stepwise process to follow when testing this design with two PSoC Development Kits (CY8CKIT-001) boards, but can be generalized for the PSoC 3 Development Kits (CY8CKIT-030) and PSoC 5 Development Kits (CY8CKIT-050) as well.

1. Set LCD power jumper J12 to ON position and position jumpers for Vdd, Vdda and Vddd to be at 5V for both the main and test board.
2. In order to generate different voltages to test the Example Project, set up a resistor ladder on the breadboard available on the PSoC DVK (See Figure 1). Use 7 resistors of 10k ohm in series, followed by a 0 ohm resistor or jumper wire to ground. Starting from the top of the first 10k resistor tap each point of the resistive ladder to P0[0] to P0[6]. The zero-ohm resistor tap is sent to P1[4], and P2[7] is also connected to ground. Finally, connect the current output of the IDAC – from P0[7] to the top of the resistor ladder – P0[0]. Ensure that the LCD is connected to the LCD header P18 on the development kit.
3. The SPI pin connections are as follows: P5[0] is SCLK, P5[1] – MOSI, P5[2] – SS, P5[3] – MISO. Connect these pins to corresponding (same) pins on the Slave board.
4. Connect a character LCD to P2[6:0] on both boards.

5. Ensure that the grounds of the two boards are tied together using a short wire.
6. Build the DelSig_SPIM project and then program the hex file onto the master board, and repeat this for the DelSig_SPIM_Test project with its corresponding board. After programming is complete, disconnect the MiniProg3.
7. Reset both the master and the slave devices.

Project Configuration

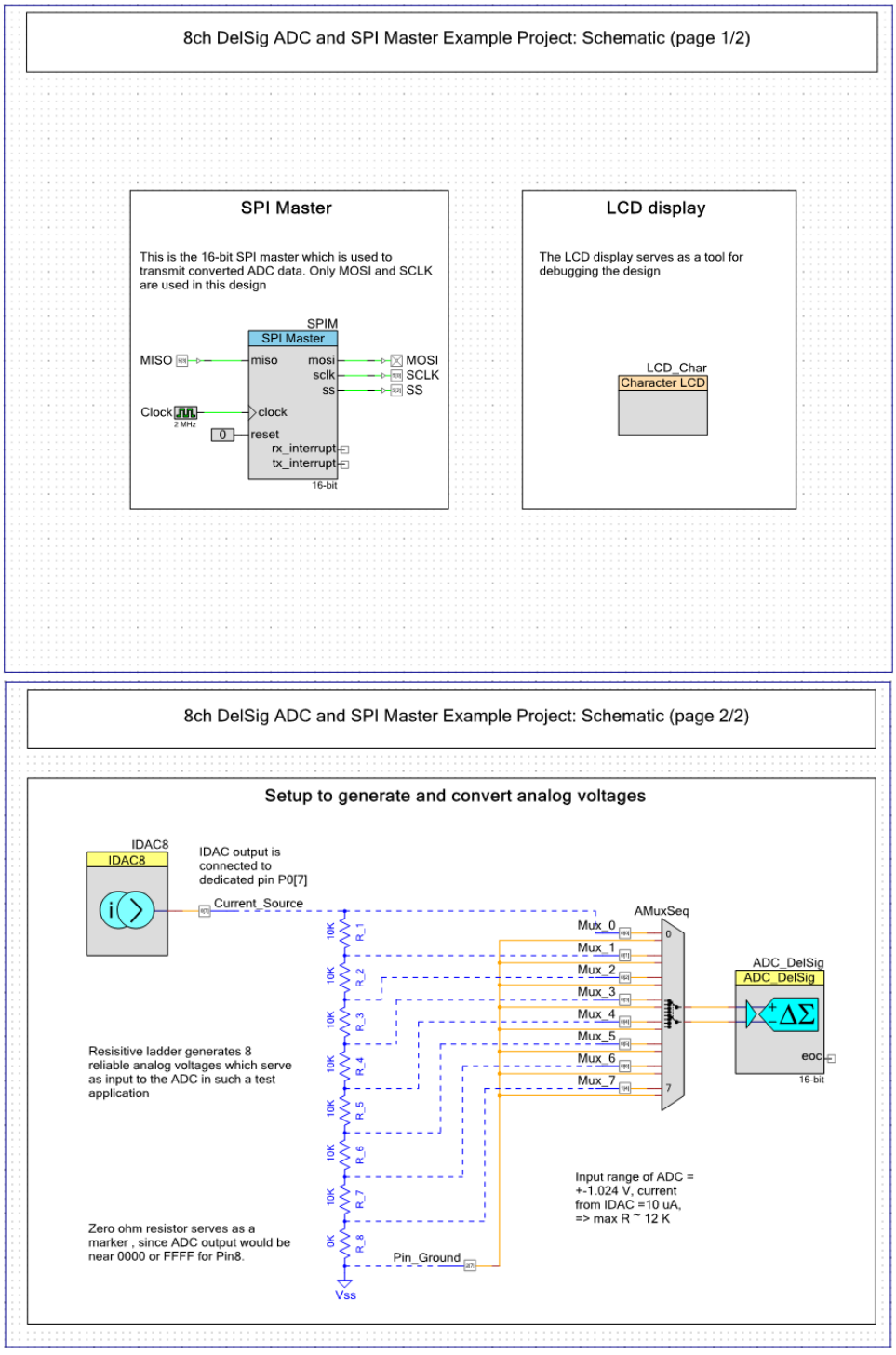

Figure 1. Top design schematic

The top design schematic is shown in Figure 1 above.

The SPI Master Full Duplex Mode macro is used for the SPI Master; the default settings are retained, except that the data bits parameter is set to 16, and an external 2 MHz clock is used. See Figure 2 below.

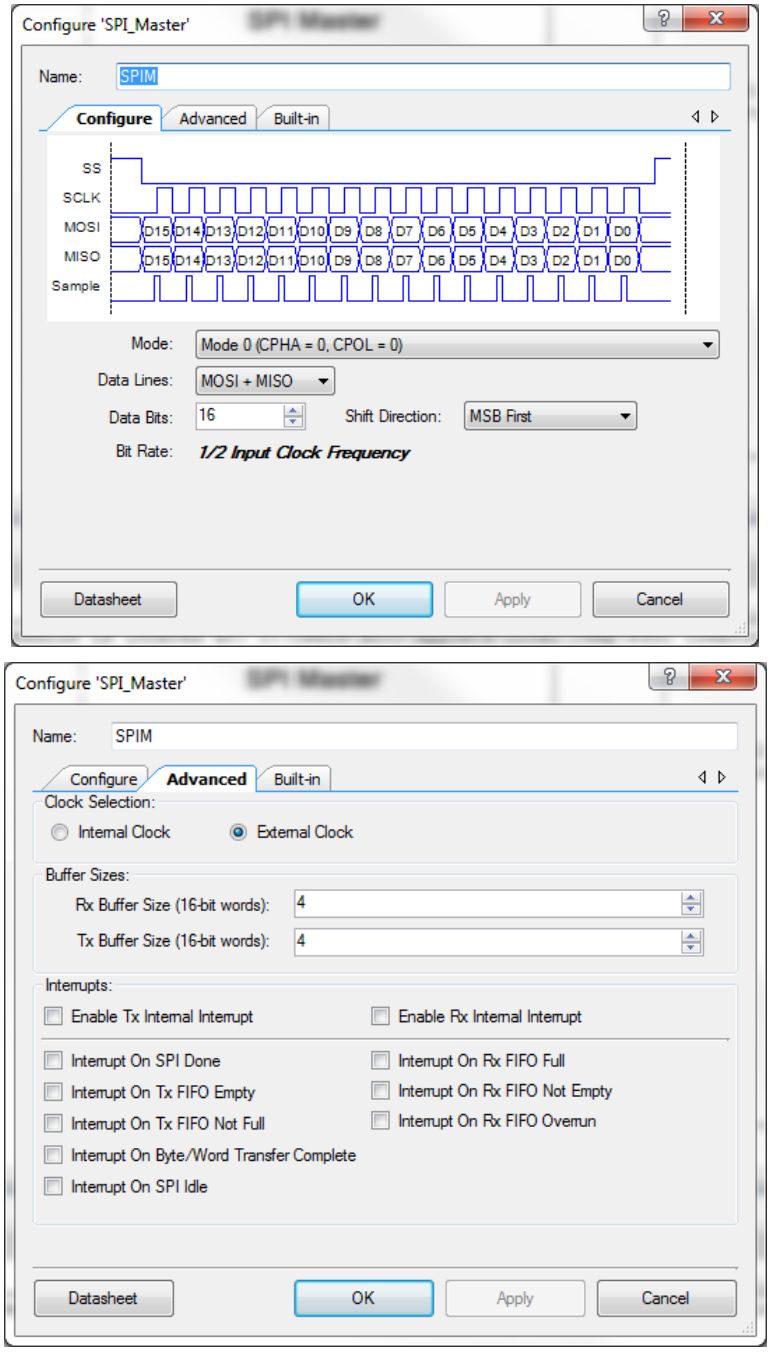

Figure 2. SPI Master configuration

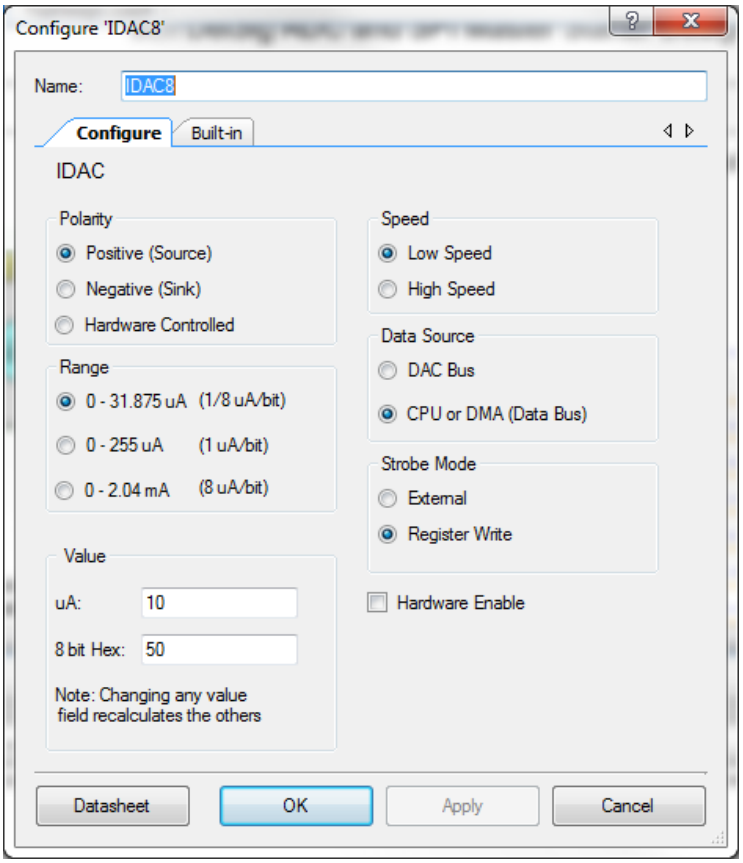

Figure 3. IDAC configuration

The analog and digital pins are retained with their default settings. The analog sequencing mux is chosen to multiplex the 8 differential inputs to the ADC on account of its fast response. The IDAC is set to source current in the 0-31.875 µA range and an initial value of 10µA. This value can be adjusted according to the input range of the ADC and the value of the resistors in the resistor ladder.

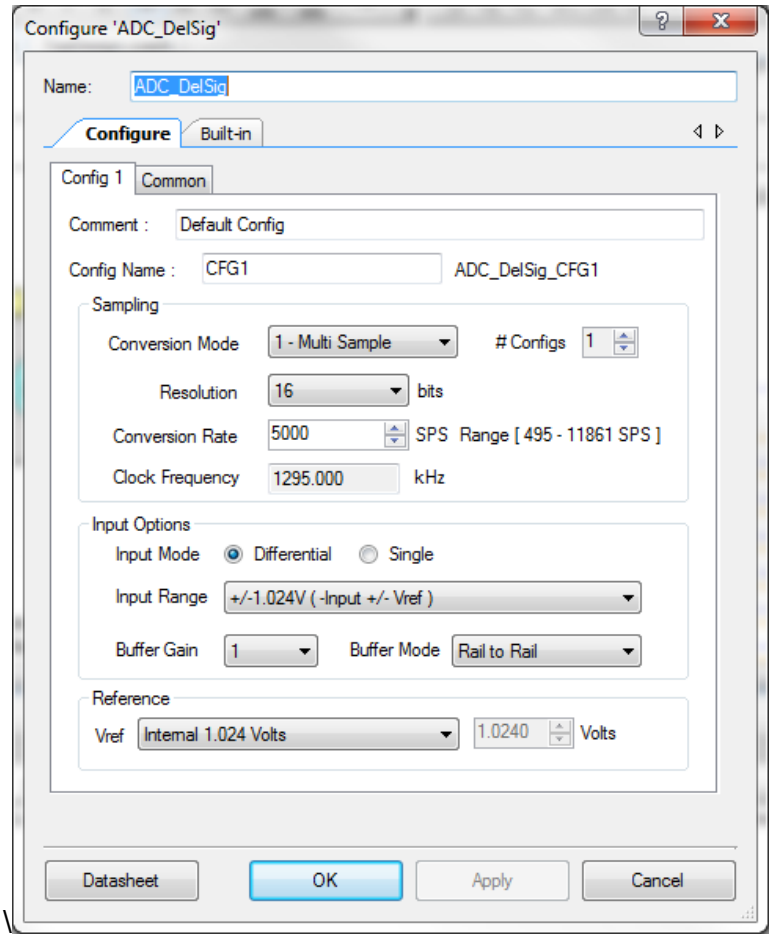

Figure 4. Delta Sigma ADC configuration

Figure 4 shows the configuration for the Delta Sigma ADC. The test project settings are simple as shown in Figure 5 and Figure 6.

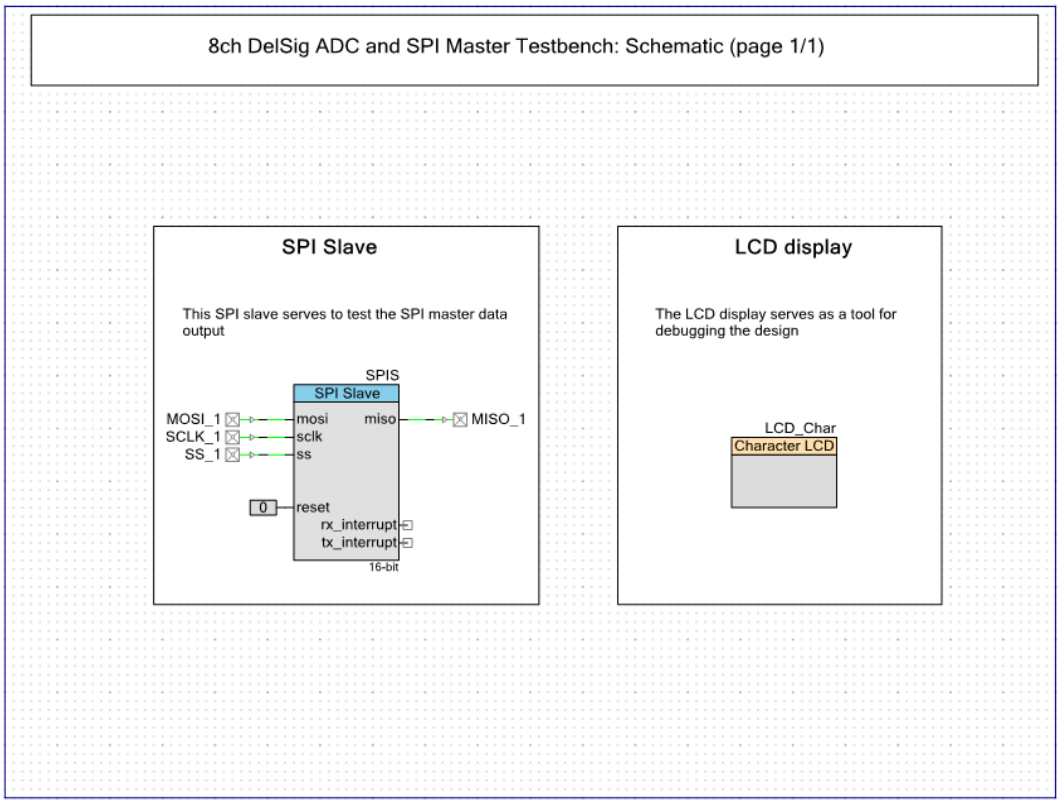

Figure 5. SPI Slave top design schematic

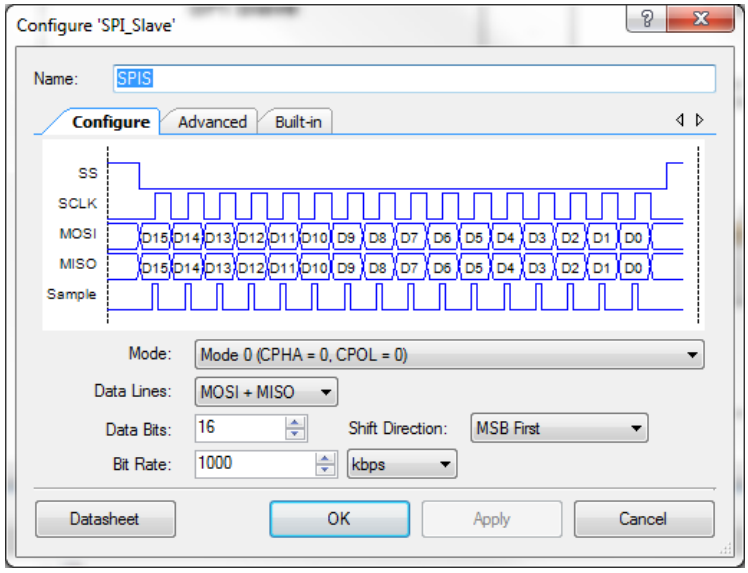

Figure 6. SPI Slave configuration

Project Description

The analog voltages input to the analog sequencing mux, are selected in succession, one every 2 seconds (to facilitate reading of the LCD). Each selected analog voltage is converted by the ADC, and transmitted over SPI using the SPI Master component. This digital value is also displayed in hexadecimal format on the Character LCD on the development kit.

The receiver (test) board has a pre-configured SPI slave which waits for data from the SPI master. When data arrives, this is displayed in hex using the Character LCD. The functionality is verified by checking the data displayed on the main and test board LCDs (at the same time).

Expected Results

The Character LCD on the master board as well as the slave board should display the same hexadecimal representation of the analog inputs fed from the resistor ladder. The subsequent analog voltage value should appear every 2 seconds, while cycling through all 8 voltages continuously.

Related Material

Example Projects

- ADC_16Channel
- DelSig_I2CM
- DelSig_I2CS
- SAR_SPIM_USB
- ADC_DMA_VDAC

Component Datasheets

- Serial Peripheral Interface (SPI) Master 2.21
- Serial Peripheral Interface (SPI) Slave 2.20
- Delta Sigma Analog to Digital Converter (ADC_DelSig) 2.20

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