DelSig_I2CS Example Project
1.00

Features

- 8-channel sequenced Delta Sigma ADC
- I2C Slave
- Easy debugging using Character LCD
- Exception Handling

General Description

This example project is also a PSoC Creator starter design. This design shows a 16-bit differential ADC, hardware multiplexed into 8 channels, and transported over I2C. To test this design, an I2C Slave project (DelSig_I2CS_Test) is available as a separate example project.

This starter design also includes advanced debugging techniques to detect and handle system level faults and conditions, such as a missing wire or missing device on the bus. The PSoC 0.1% internal voltage reference shows the additional BOM integration.

This design makes it easy to get started and utilize precision analog capability of PSoC.

Development kit configuration

The following configuration instructions provide a guideline to test this design with the DelSig_I2CM_Test Example Project. For simplicity, the instructions describe the stepwise process to be followed when testing this design with 2 PSoC Development Kits (CY8CKIT-001), but can be generalized for the PSoC 3 Development Kit (CY8CKIT-030) and PSoC 5 Development Kit (CY8CKIT-050) as well.

1. Set LCD power jumper J12 to ON position and position jumpers for Vdd, Vdda and Vddd to be at 5V for both the main and test board.
2. In order to generate different voltages to test the Example Project, set up a resistor ladder on the breadboard available on the CY8CKIT-001 (See Figure 2). Use 7 resistors of 10k ohm in series, followed by a 0 ohm resistor or jumper wire to ground. Starting from the top of the first 10k resistor tap each point of the resistor ladder to P0[0] to P0[6]. The zero-ohm resistor tap is sent to P1[4], and P2[7] is also connected to ground. Finally, connect the current output of the IDAC – from P0[7] to the top of the resistor ladder – P0[0].
3. For the I2C communication, connect P12[0] to SCL, P12[1] to SDA. Use 2 external 2.67k resistors to pull-up SCL and SDA to 5V (Figure 1). Note that Figure 1 is a depiction for the

purpose of understanding the external connections and not the actual PSoC Creator schematic (Figure 2).

4. Externally connect the corresponding pins (SCL and SDA) on I2C Slave board to the master test board as depicted in Figure 1.

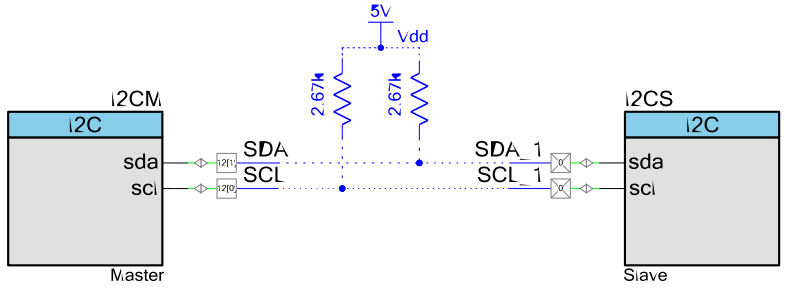
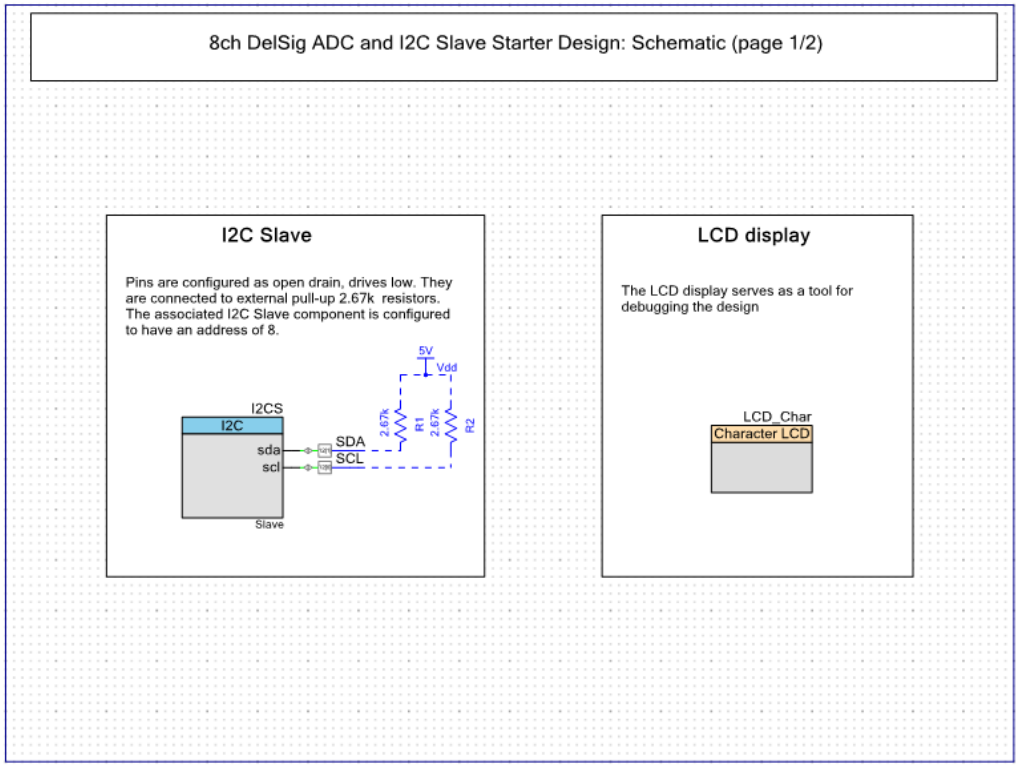
5. 

Figure 1. Connection of SDA and SCL to pull-up resistors

6. Connect the Character LCD to P2[6:0] on both boards.
7. Ensure that the grounds of the two boards are tied together.
8. Build the DelSig_I2CS project and then program the hex file onto the main board, and repeat this for the DelSig_I2CS_Test project and its corresponding board. After programming is complete, disconnect the MiniProg3.
9. Power cycle the master device and reset the slave device.

Project configuration



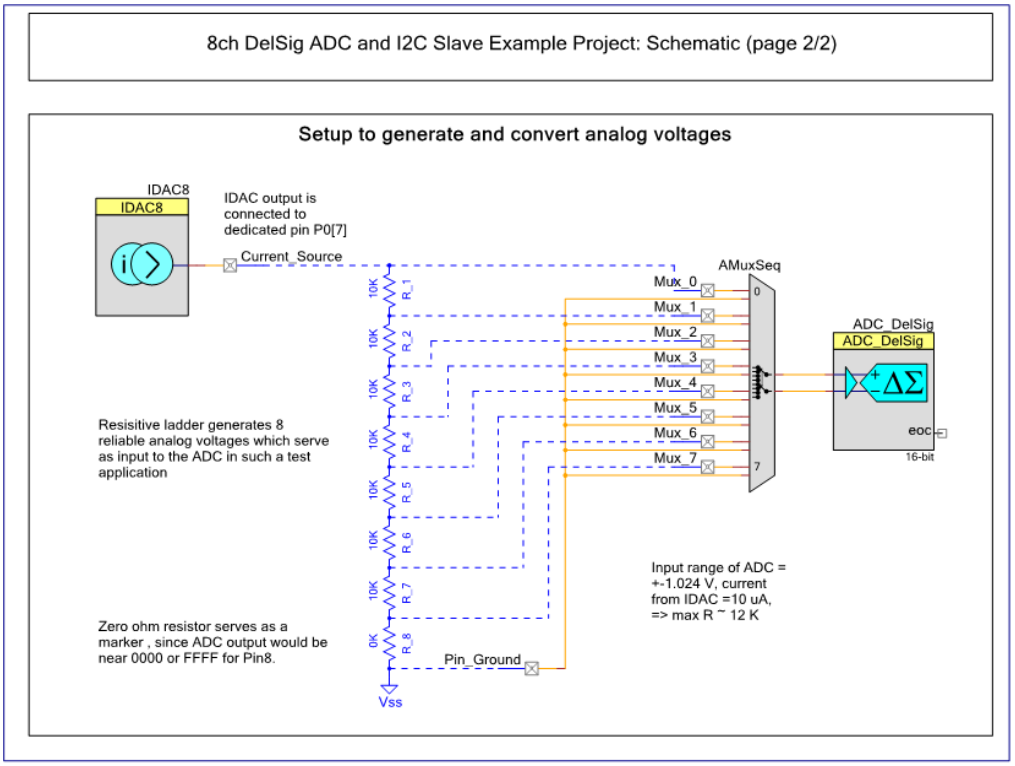


Figure 2. I2C Slave Top design schematic

The top design schematic is shown in Figure 2 above. As shown in Figure 3, a Fixed Function I2C block is used, with a data rate of 100 kbps and an address of 8.

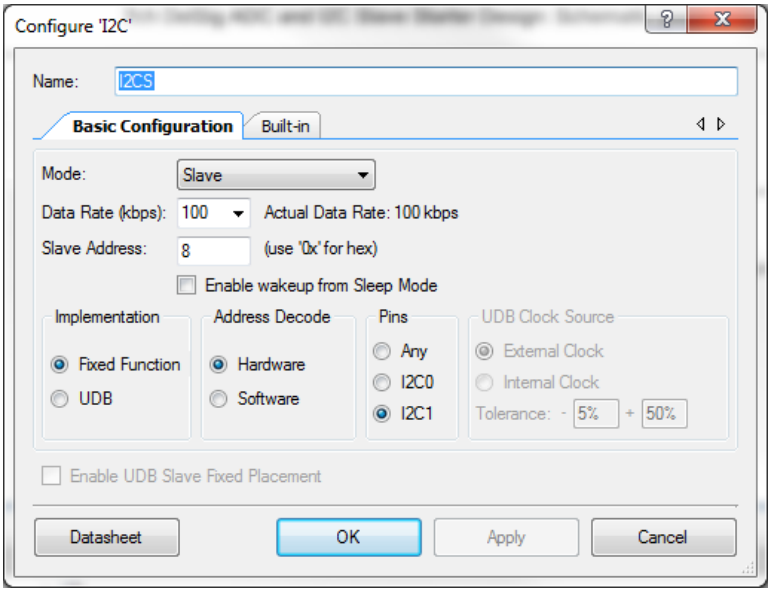


Figure 3. I2C Slave Configuration

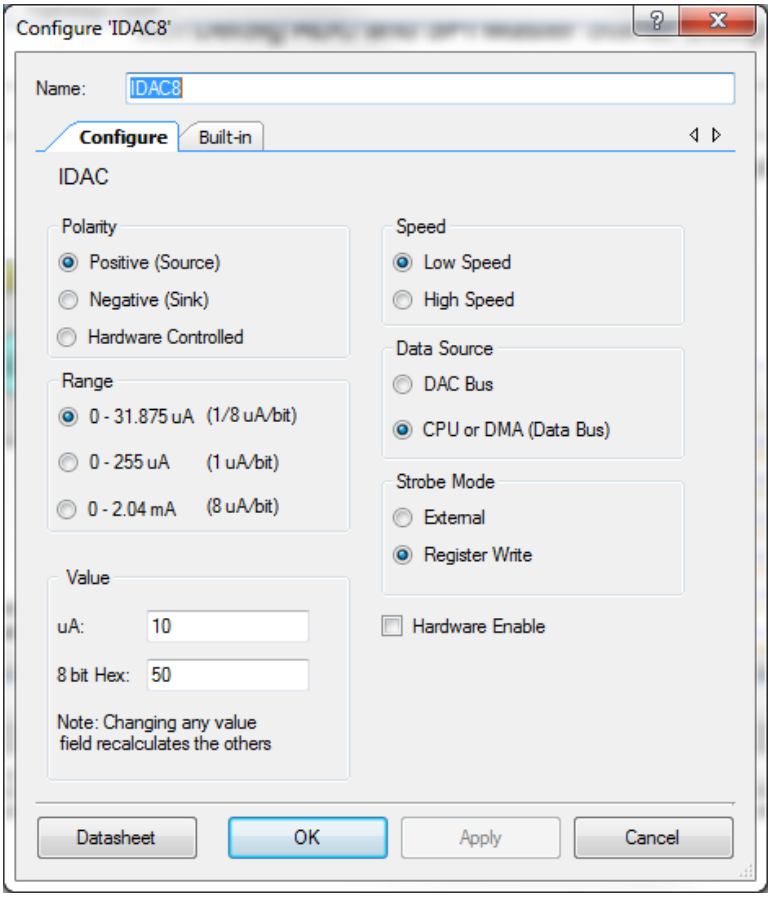


Figure 4. IDAC configuration

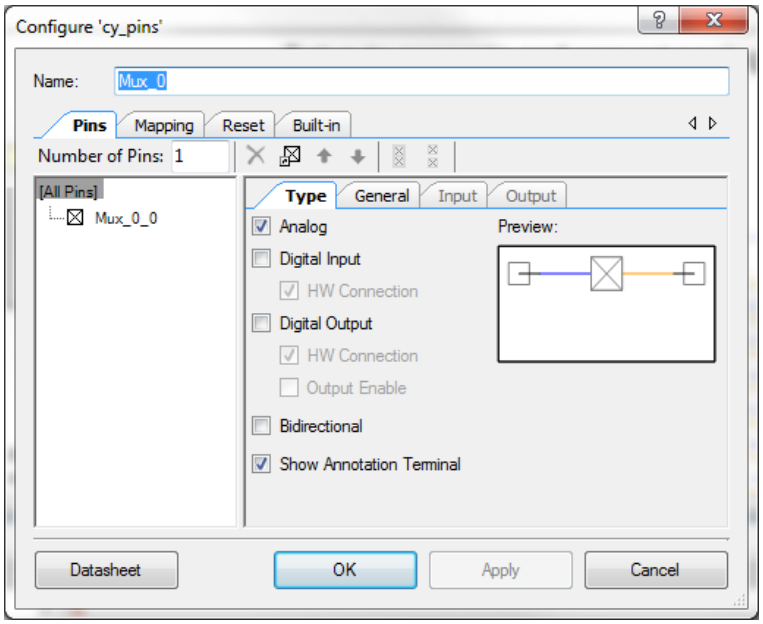


Figure 5. Configuration for the pins

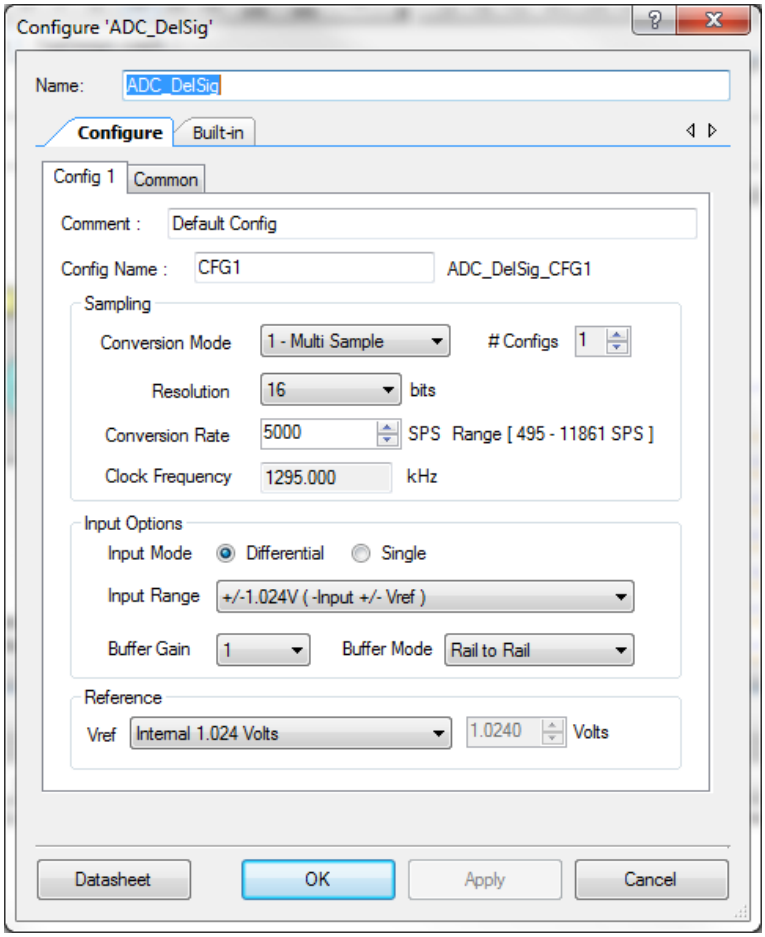


Figure 6. Delta Sigma ADC configuration

The character LCD is left at default settings. The IDAC is set to source current in the 0-31.875 µA range and an initial value of 10µA. This value can be adjusted according to the input range of the ADC and the value of the resistors in the resistor ladder.

The analog sequencing mux is configured for 8 differential inputs, and all the analog pins are used with their default settings (Figure 5). Figure 6 shows the configuration for the Delta Sigma ADC. The test project has a very simple setup as shown in Figure 7 and Figure 8.

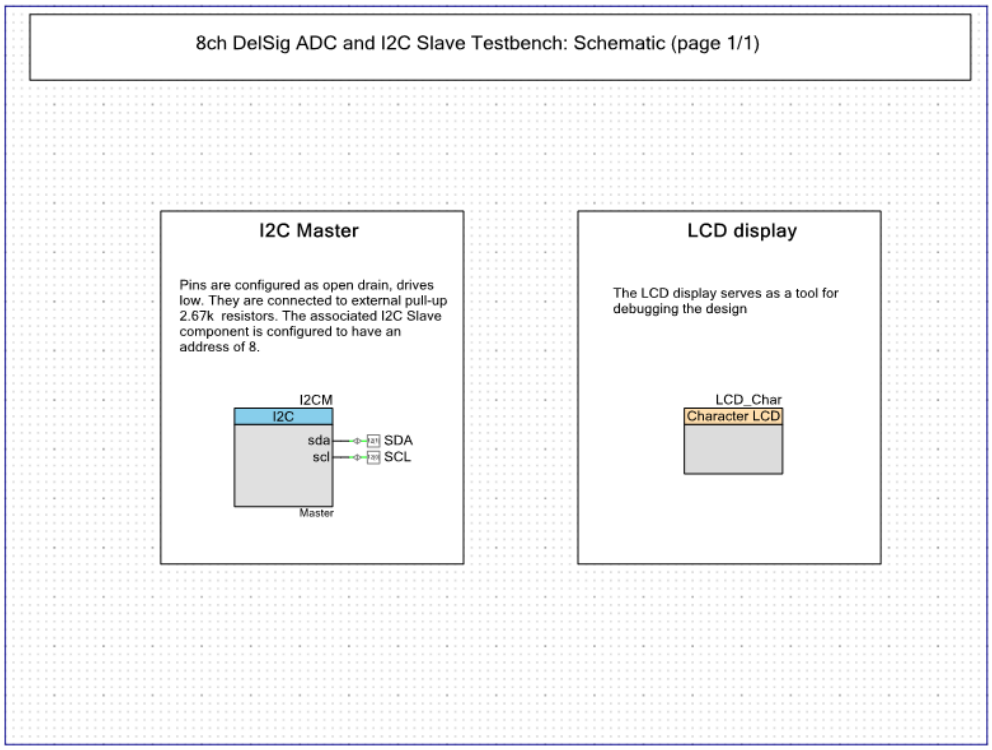


Figure 7. I2C Master Top design schematic

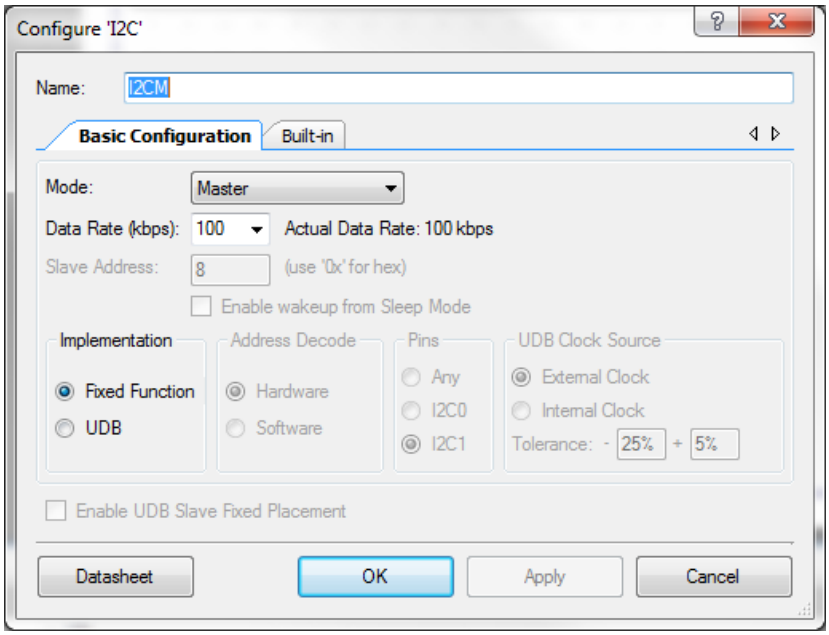


Figure 8. I2C Master configuration

Project description

The analog voltages input to the analog sequencing mux, are selected in succession. Each selected analog voltage is converted by the ADC, and stored in a read buffer. This read buffer is read by the Master in the test project every 2 seconds (to facilitate reading of the LCD). Subsequent channels are selected and read every time the I2C master reads the I2C slave data buffer. The digital value out of the ADC is also displayed on the Character LCD on the development kit.

The receiver board has a pre-configured I2C master which reads new data from the I2C slave. When new data is read, this is displayed using the Character LCD. After a delay of 2 seconds the I2C master again starts checking for new data from the I2C slave. The functionality is verified by checking the data displayed on the main and test board LCDs (at the same time).

Expected Results

The Character LCD on the master board as well as the slave board should display the same hexadecimal representation of the analog inputs fed from the resistor ladder. The subsequent analog voltage values should appear every 2 seconds, while cycling through all 8 voltages continuously.

Related Material

Example Projects

- ADC_16Channel
- DelSig_I2CM
- DelSig_SPIM
- SAR_SPIM_USB
- ADC_DMA_VDAC

Component Datasheets

- Delta Sigma Analog to Digital Converter (ADC_DelSig) 2.20

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

Phone : 408-943-2600
Fax : 408-943-4730
Website : www.cypress.com

© Cypress Semiconductor Corporation, 2012. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges. PSoC® is a registered trademark, and PSoC Creator™ and Programmable System-on-Chip™ are trademarks of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein are property of the respective corporations.

This Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.