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CE219881 - PSoC 6 MCU Switching Between Power Modes

Objective

This example demonstrates how to transition PSoC® 6 MCU among the following power modes – Low Power Active, Low Power Sleep, Ultra-Low Power Active, Ultra-Low Power Sleep, and Deep Sleep.

Requirements

Tool: PSoC® Creator™ 4.2 and Peripheral Driver Library (PDL) 3.1.0

Programming Language: C (ARM® GCC 5.4-2016-q2-update)

Associated Parts: All PSoC 6 MCU parts

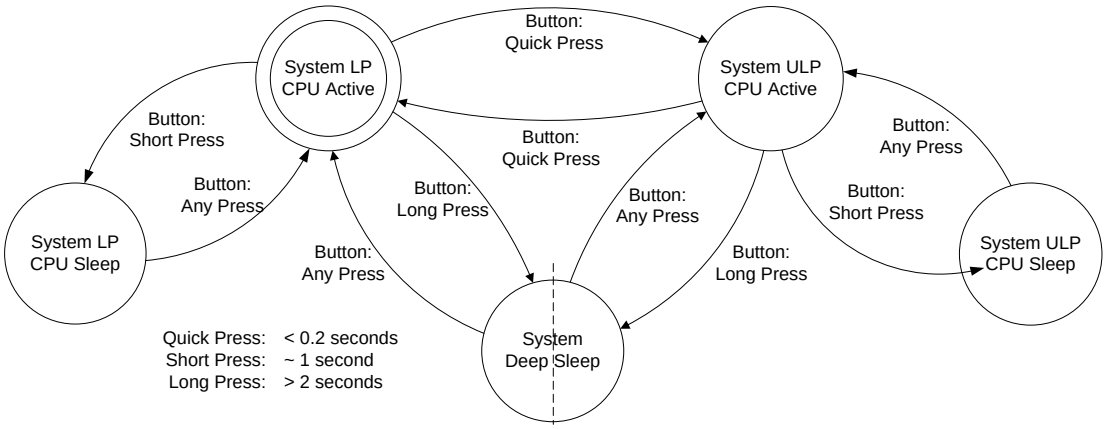
Related Hardware: PSoC 6 BLE Pioneer Kit, PSoC 6 Wi-Fi-BT Pioneer Kit

Overview

This code example shows how to enter system Low Power (LP) and Ultra Low Power (ULP) modes, and transition to CPU Sleep or Deep Sleep mode. After transitioning to Deep Sleep or Sleep mode, the example also shows how to wake up and return to LP or ULP mode. This example does not cover Hibernate mode. Refer to the PSoC 6 documentation for more information about this mode. AN219528 - PSoC 6 MCU Low-Power Modes and Power Reduction Techniques provides additional detail on the PSoC 6 MCU power modes, use of the SysPM driver, and other recommendations for reducing power consumption.

The project uses a kit button to change power mode. Figure 1 shows the state machine implemented in the firmware to execute the transitions.

Figure 1. Power Mode State Machine



The project also uses one LED to indicate the power mode selected. Table 1 shows the state of the LED for each mode.

Table 1. Power Mode Versus LED State

System /Power Mode	LED State
System LP / CPU Active	Blinks quickly
System LP / CPU Sleep	Turned ON and bright
System ULP / CPU Active	Blinks slowly
System ULP / CPU Sleep	Turned ON and dimmed
System / Deep Sleep	Turned OFF

Hardware Setup

This example does not require any additional hardware to run. However, you can connect an ammeter to measure the current consumed by the CM0+ and CM4. Simply remove the jumper PWR_MON from the PSoC 6 kit and connect the ammeter on the header pins. This jumper is located in the backside of the PSoC 6 kit. Refer to the kit guide for the exact location.

Operation

Follow the instructions that came with your kit to make sure that it is connected to your PC.

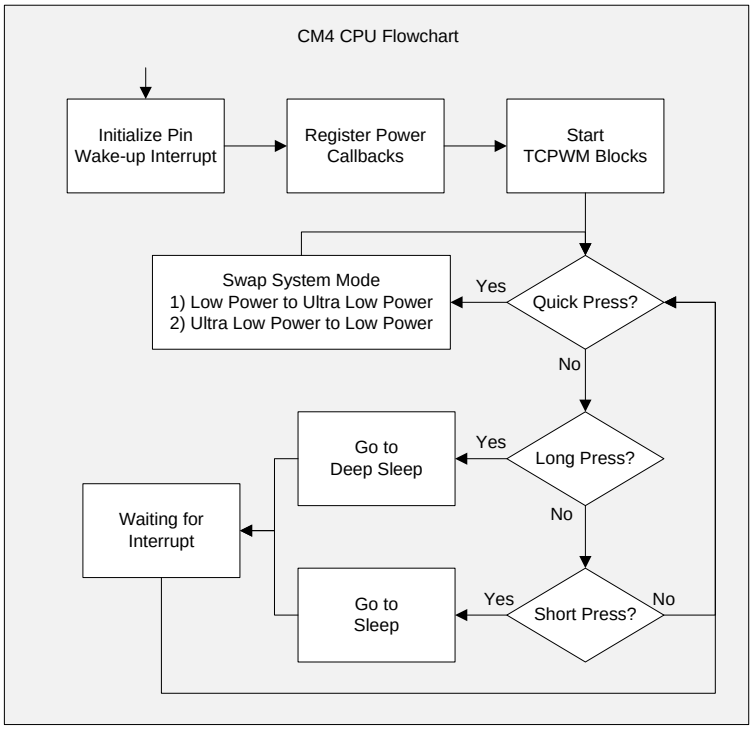
1. If observation of the current is desired, remove the PWR_MON jumper on CY8CKIT-062 and connect an ammeter to the header pins.
2. Build the “CE219881_PowerModes” project and program CY8CKIT-062. For more information on building projects and device programming, see PSoC Creator Help.
3. Confirm that the kit LED is blinking quickly and take note of the current consumption. The device is in System LP and CPU Active modes at this moment.
4. Press the kit button for approximately one second and release it. Observe that the LED is ON and fully bright. Confirm that the current consumption drops by a few hundreds of microamperes. The device is in System LP and CPU Sleep mode at this moment.
5. Quickly press the kit button to return to System LP and CPU Active modes. Observe that the LED is blinking quickly again.
6. Press the kit button for at least two seconds and release it. Observe that the LED is OFF and that the current consumption has dropped to a few microamperes. The device is in System Deep Sleep mode at this moment.
7. Quickly press the kit button to return to System LP mode. Observe that the LED is blinking quickly and that the current consumption has increased to the same level measured before.
8. Quickly press the kit button again to enter System ULP mode. Observe that the LED is blinking slowly and that the current consumption has dropped significantly when comparing to System LP mode. You can quickly press the kit button to switch between the two modes.
9. Keep the device in System ULP mode and press the kit button for approximately one second and release it. Observe that the LED dims and that the current consumption has dropped a few hundred microamperes. The device is in the System ULP and CPU Sleep modes at this moment.
10. Quickly press the kit button to return to the System ULP and CPU Active modes. Observe that the is blinking slowly again.
11. Press the kit button for at least two seconds and release it. Observe that the LED is OFF and that the current consumption has dropped to a few microamperes. The device is in System Deep Sleep mode at this moment.
12. Quickly press the user button and return to the System ULP and CPU Active modes. Observe that the LED is blinking slowly again and that the current consumption has increased to the same level measured before.

Design and Implementation

PSoC 6 MCU is a dual-CPU architecture MCU with Arm® Cortex® M0+ (CM0+) and Arm Cortex M4 (CM4) CPUs. The CM0+ CPU enables the CM4 CPU on device reset. This example configures a TCPWM resource in PWM mode to blink and turn ON/OFF the LED. Another TCPWM resource is configured in Timer-Counter mode to measure the amount of time the user button is pressed.

This example uses only the CM4 CPUs of PSoC 6 MCU. The CM4 CPU handles the state machine shown in Figure 1 and controls the duty cycle of the PWM block. The device wakes up when a switch press is detected. Figure 2 shows the firmware flow of CM4 CPU.

Figure 2. Firmware Flowchart



Six power callback functions are registered. Table 2 shows the actions of each callback function. For more information on power callbacks, refer to the PDL Driver – System Power Management (SysPm).

Table 2. Power Callback Actions

Power Callback Functions	State Modes (CY_SYSPM_*)			
	CHECK_READY	CHECK_FAIL	BEFORE_TRANSITION	AFTER_TRANSITION
TCPWM Sleep Callback	Nothing	Nothing	If in System ULP Mode, dim the LED. If in System LP Mode, turn ON the LED. Disable the Counter block.	If in System ULP Mode, blink the LED slowly. If in System LP blink the LED fast.
TCPWM Deep Sleep Callback	Nothing	Nothing	Disable all TCPWM blocks.	Re-enable the PWM block. If in System ULP mode, blink the LED slowly. If in System LP Mode, blink the LED fast.
TCPWM Enter ULP Callback	Nothing	Nothing	Nothing	Blink the LED slowly.
TCPWM Enter LP Callback	Nothing	Nothing	Nothing	Blink the LED fast.
Clock Enter System ULP Callback	Nothing	Nothing	Reconfigure the FLL frequency to 50 MHz.	Nothing
Clock Exit Ultra-Low Power Callback	Nothing	Nothing	Nothing	Reconfigure the FLL frequency to 100 MHz.

Components and Settings

Table 3 lists the PSoC Creator Components used in this example, how they are used in the design, and the non-default settings required so they function as intended.

Table 3. List of PSoC Creator Components

Component	Instance Name	Purpose	Non-default Settings
PWM (TCPWM)	KIT_LED1_PWM	Drives the user LED.	Period: 50000 Compare: 25000
Timer Counter (TCPWM)	APP_COUNTER	Counts how long the user button is pressed.	Resolution: 32-bits Period: 100000000
Digital Output Pin	KIT_LED1	Controls the user LED.	All defaults
Digital Input Pin	KIT_BTN1	Changes the power mode.	Drive Mode: Resistive Pull Up Interrupt: Falling edge
Clock	CLOCK_PWM	Clock the PWM	Frequency: 500 kHz

Reusing This Example

This code example runs on PSoC 6 BLE Pioneer Kit and PSoC 6 Wi-Fi-BT Pioneer Kit, which have a PSoC 6 device. To port the design to other PSoC 6 devices and kits, change the target device using PSoC Creator **Project** > **Device Selector**, and pin assignments in the Design Wide Resources window.

Related Documents

Table 4 lists all relevant application notes, code examples, knowledge base articles, device datasheets, and Component / user module datasheets.

Table 4. Related Documents

Application Notes	
AN210781 Getting Started with PSoC 6 MCU with BLE Connectivity	Describes the PSoC 6 BLE, and how to build this code example
AN215656 PSoC 6 MCU Dual-CPU System Design	Describes the dual-CPU architecture in the PSoC 6 MCU
AN219528 PSoC 6 MCU Low-Power Modes and Power Reduction Techniques	Describes the PSoC 6 power modes to optimize power consumption.
PSoC Creator Component Datasheets	
Clock (SYSCLK) Component	Provides an interface to the programmable peripheral clock dividers
General Purpose Input / Output (GPIO) Component	Allows hardware resources to connect to a physical port-pin
Pulse Width Modulator (TCPWM_PWM)	Configures the TCPWM hardware for PWM functionality
Timer / Counter (TCPWM_COUNTER)	Configures the TCPWM hardware for Timer/Counter functionality
Device Documentation	
PSoC 6 MCU Datasheets	PSoC 6 MCU Technical Reference Manuals
Development Kit (DVK) Documentation	
CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit	
CY8CKIT-062-WiFi-BT PSoC 6 WiFi-BT Pioneer Kit	

Document History

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Document Number: 002-19881

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5777742	RLOS	06/19/2017	New Code Example
*A	5848138	RLOS	08/08/2017	Updated Project to PSoC Creator 4.2
*B	6002595	RLOS	12/22/2017	Removed figure of the CY8CKIT-062 BLE kit and added description of the location of the PWR_MON jumper.
*C	6415634	RLOS	12/18/2018	Changed the documentation to align with the new terms of power modes from PDL 3.1.0
*D	6470364	RLOS	01/31/2019	Updated code only. Fixed bug related to exiting the ULP mode.

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