CE216796 - FM0+ MFS CSIO (SPI) Master & Slave

This application demonstrates master and slave CSIO (SPI) communication using a single device.

Overview

A pair of CSIO channels are implemented in two MFS Components. First, the master sends a string to the slave, then the roles reverse and the slave sends a different string to the master. The returned strings are compared against the originals and the green LED used to indicate that the transfers were successful (strings match).

Requirements

Tool: PSoC Creator 4.0

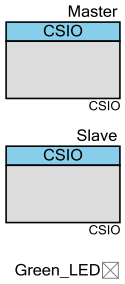
Programming Language: C (GCC 4.9.3)

Associated Parts: All S6E1 parts

Related Hardware: FM0-V48-S6E1A1 and FM0-64L-S6E1C3

Design

The schematic includes the two MFS Components in CSIO mode and a GPIO for the LED.



The firmware performs following functions:

1. Initialize the LED (off)
2. Initialize the master (Tx enabled) and slave (Rx enabled) Components
3. Send a message from master to slave
4. Verify sent data == received data
5. Switch Tx and Rx functions
6. Send a message from slave to master
7. Verify sent data == received data
8. Indicate success with green LED
9. De-initialize the MFS Components

Design Considerations

Pin Selection

The project includes control files to automatically place the SCK, MISO, MOSI and LED IO onto the appropriate pins for the supported kit hardware. To change the pin selection, delete the control file or over-ride the control file selections in the Design Wide Resources Pin Editor.

PDL Installation

The project assumes that you have installed the PDL in the location specified in the **Project Management** panel of the **Tools** > **Options** dialog. If that location is incorrect you will see the build error "The given PDL path is invalid. Unable to find required PDSC file." To correct this problem in a newly-created project open the **Project** > **Properties** dialog and enter the correct path to the PDL. To avoid the problem in projects you create in the future, make sure you put the correct path in the **Tools** > **Options** dialog.

Hardware Setup

The GPIO is connected to the green LED.

The MFS signals are connected to headers on the kits. Follow the wiring instructions, below, for each kit.

Table 1 lists the pin connections required to use this code example on FM0+ kits.

Table 1. List of Pins

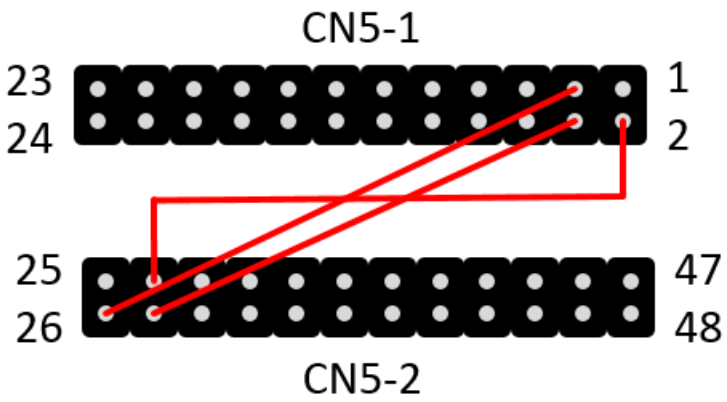
Pin	FM0-V48-S6E1A1	FM0-64L-S6E1C3
Green_LED:GPIO	P61	P3E
Master:SCK	P52	P4C
Master:SIN	P50	P4E
Master:SOT	P51	P4D
Slave:SCK	P13	P13
Slave:SIN	P11	P11
Slave:SOT	P12	P12

FM0-V48-S6E1A1 Wiring

Make the following jumper wire connections to run this application on the FM0-V48-S6E1A1 kit.

CN5.4 – CN5.28	Master SCK to Slave SCK
CN5.2 – CN5.27	Master SIN to Slave SOT
CN5.3 – CN5.26	Master SOT to Slave SIN

Figure 1. FM0-V48-S6E1A1 Jumper Wires



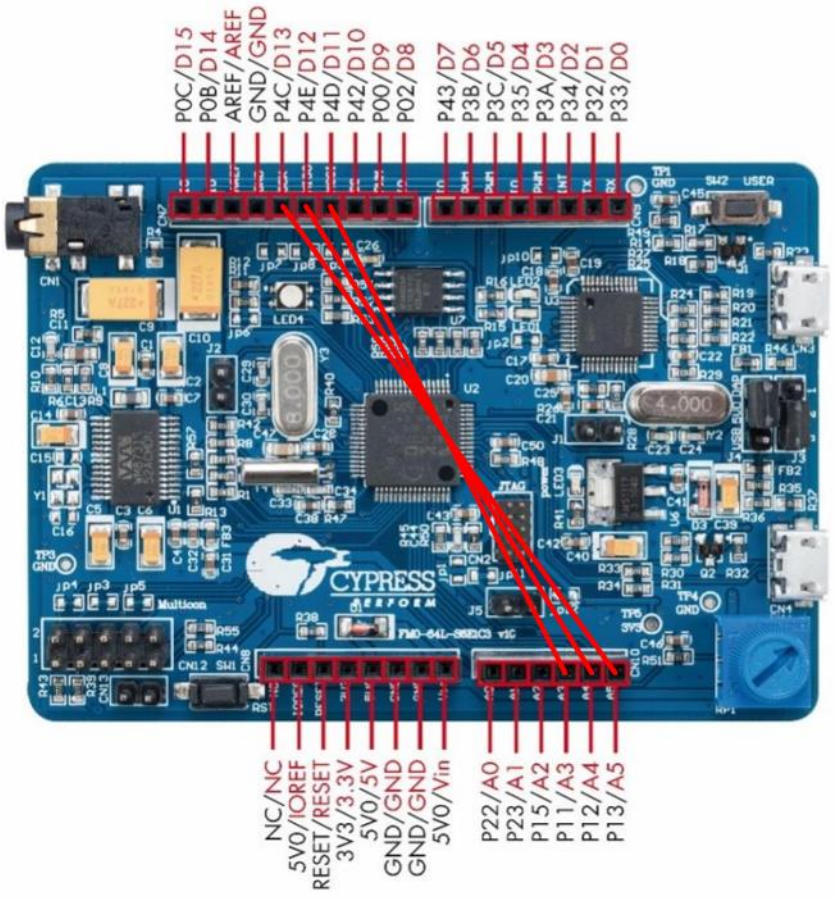
FM0-64L-S6E1C3 Wiring

Make the following jumper wire connections to run this application on the FM0-64L-S6E1C3 kit.

CN7.6 (D13) – CN10.6 (A5)	Master SCK to Slave SCK
CN7.5 (D12) – CN10.5 (A4)	Master SIN to Slave SOT
CN7.4 (D11) – CN10.4 (A3)	Master SOT to Slave SIN

Note: On this kit the D11, D12, and D13 pins are connected to the FM0+ device across header-less jumpers JP9, JP8 and JP7 respectively. These jumpers are open by default but can be closed by soldering a 0 Ω wire across each jumper.

Figure 2. FM0-64L-S6E1C3 Jumper Wiring



Components

Table 2 lists the PSoC Creator Components used in this example, as well as the hardware resources used by each.

Table 2. List of PSoC Creator Components

Component	Version	Hardware Resources
PDL_MFS	1.0	MFS block plus SCK, SIN and SOT pins
PDL_GPIO	1.0	GPIO pin

Parameter Settings

The Master MFS Component uses default parameter settings, with these exceptions.

Table 3: Component Settings

Tab	Setting	Value
None	Name	Master
Basic	MFSConfig	CSIO (SPI)
CSIO	enCsioMsMode	Master
	enCsioDataLength	8 bits
	enCsioBitDirection	MSB First
FIFO	u8ByteCount1	0
	u8ByteCount2	0

The Slave MFS Component uses default parameter settings, with these exceptions.

Table 4: Component Settings

Tab	Setting	Value
None	Name	Slave
Basic	MFSConfig	CSIO (SPI)
CSIO	enCsioMsMode	Slave
	enCsioDataLength	8 bits
	enCsioBitDirection	MSB First
FIFO	u8ByteCount1	0
	u8ByteCount2	0

Operation

Wire up the kit using jumper wires as described in Hardware setup, above.

After programming, the application runs and the green LED lights to indicate that two transfers have been completed successfully. To follow the transactions more closely, use the debugger to step through the program and monitor the contents of the two receive buffers; master_recbuf and slave_recbuf.

Related Documents

Table 5 lists relevant application notes, code examples, knowledge base articles, device datasheets, and Component datasheets.

Table 5. Related Documents

PSoC Creator Component Datasheets	
PDL_MFS	Supports UART, I2C, LIN and CSIO (SPI) serial communication. Right-click the Component to access.
Device Documentation	
S6E1A	FM0+ S6E1A-Series 5V Robust ARM® Cortex®-M0+ Microcontroller (MCU) Family
S6E1C	FM0+ S6E1C-Series Ultra Low Power ARM® Cortex®-M0+ Microcontroller (MCU) Family
Development Kit (DVK) Documentation	
FM0-V48-S6E1A1	ARM® Cortex®-M0+ FM0+ MCU Evaluation Board
FM0-64L-S6E1C3	ARM® Cortex®-M0+ MCU Starter Kit with USB and Digital Audio Interface

Document History

Document Title: CE216796 - FM0+ MFS CSIO (SPI) Master & Slave

Document Number: 002-16796

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5448648	YFS	09/27/16	New Code Example.
*A	5776655	YFS	6/16/17	Added search keyword so that user can quickly find Code Examples from the component instance popup menu. Updated logo and copyright date.
*B	5988608	YFS	12/8/17	Removing S6E1B support.

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