CE216669 – FM0+ CLK Driving Dual Timer

This application toggles an LED with a Dual Timer and periodically switches the system source clock between Main and PLL to vary the toggling speed.

Overview

The firmware toggles the system source clock between the Main clock (CLKMO) and PLL. A Dual timer is used to fire a periodic interrupt, which toggles the state of an LED. Every 5 seconds the source clock changes and the LED blink rate changes markedly.

Requirements

Tool: PSoC Creator 4.0

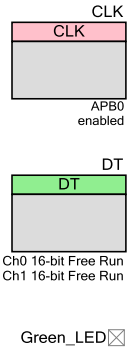
Programming Language: C (GCC 4.9.3)

Associated Parts: All S6E1 parts

Related Hardware: FM0-V48-S6E1A1 and FM0-64L-S6E1C3

Design

The schematic file includes CLK, DT and GPIO Components, renamed as shown below.



The firmware performs following functions:

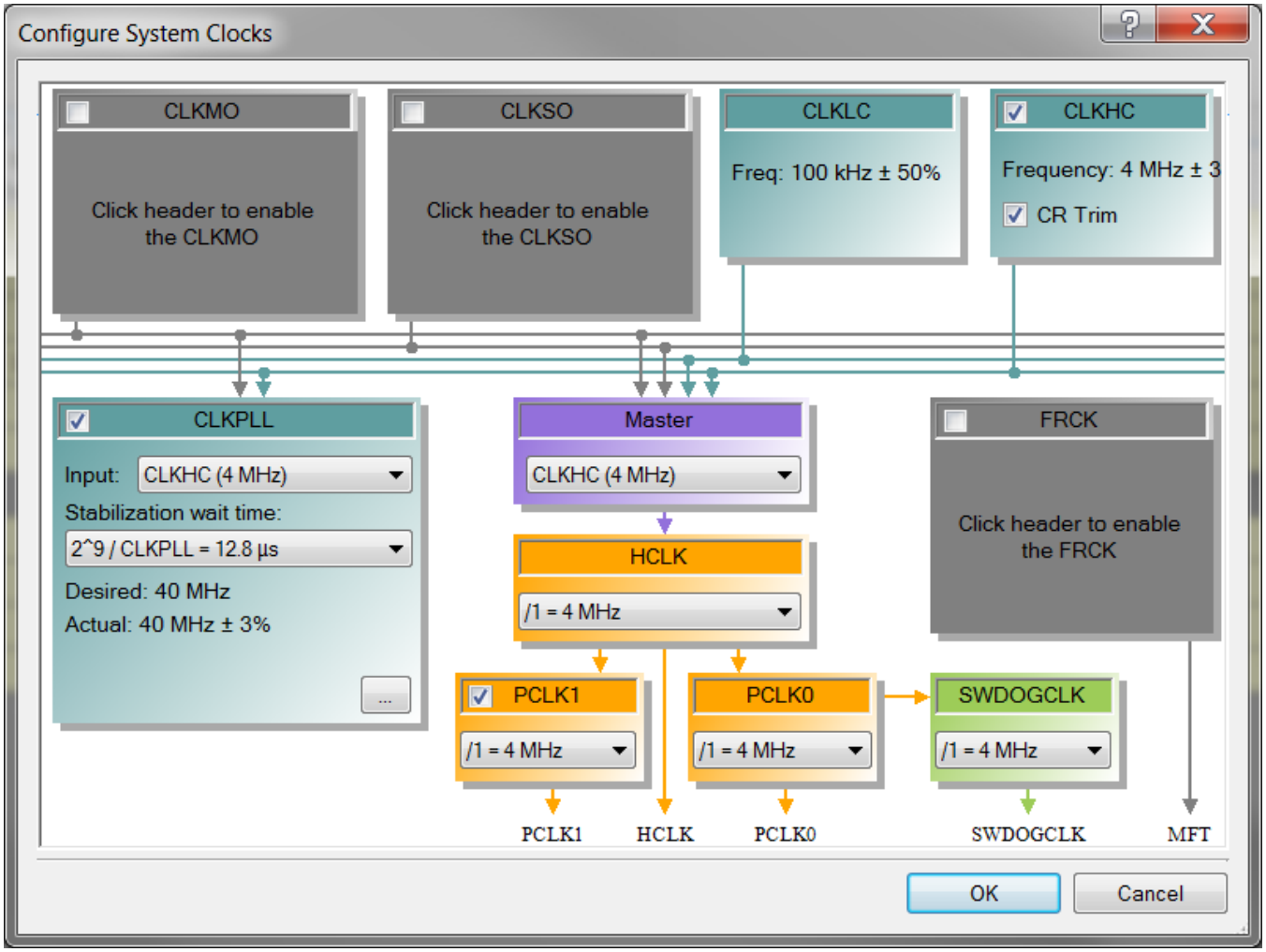
1. Initialize the LED GPIO (off) and enable read
2. Initialize and start the dual timer which toggles the LED in an interrupt
3. Enable the main and PLL clocks
4. Clear the count of toggles, switch to main clock, and wait 5 seconds
5. Clear the count of toggles, switch to PLL clock, and wait 5 seconds
6. Repeat from step #4

Design Considerations

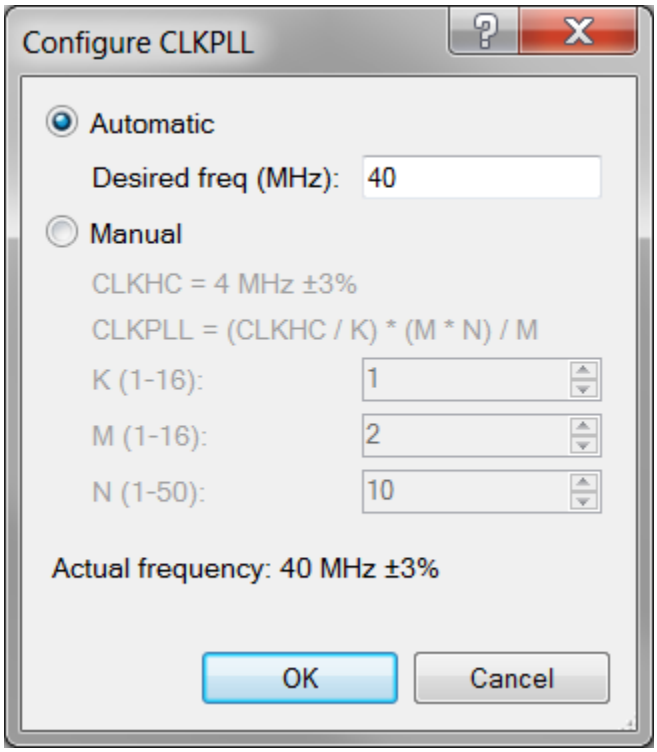
PLL Configuration

The PLL is set up in the System Clocks editor. It is configured to run at 40 MHz, which is noticeably faster than CLKMO (4 MHz on S6E1A devices, 8 MHz on S6E1C) so that the LED blinks sat a very different speed when the source is changed.

The System Clocks editor, shown below, is launched by double-clicking on any system clock in the DWR editor.


Configure System Clocks
CLKMO
Click header to enable the CLKMO
CLKSO
Click header to enable the CLKSO
CLKLC
Freq: 100 kHz ± 50%
CLKHC
Frequency: 4 MHz ± 3
CR Trim
CLKPLL
Input: CLKHC (4 MHz)
Stabilization wait time:
2^9 / CLKPLL = 12.8 µs
Desired: 40 MHz
Actual: 40 MHz ± 3%
...
Master
CLKHC (4 MHz)
HCLK
/1 = 4 MHz
FRCK
Click header to enable the FRCK
PCLK1
/1 = 4 MHz
PCLK0
/1 = 4 MHz
SWDOGCLK
/1 = 4 MHz
PCLK1
HCLK
PCLK0
SWDOGCLK
MFT
OK
Cancel

The desired frequency is set by pressing the configure button in the CLKPLL block to present the Configure PLL dialog.



PDL Installation

The project assumes that you have installed the PDL in the location specified in the Project Management panel of the Tools > Options dialog. If that location is incorrect you will see the build error “The given PDL path is invalid. Unable to find required PDSC file.” To correct this problem in a newly-created project open the Project > Properties dialog and enter the correct path to the PDL. To avoid the problem in projects you create in the future, make sure you put the correct path in the Tools > Options dialog.

Pin Selection

The project includes control files to automatically place the GPIO onto the appropriate pin for the supported kit hardware. To change the pin selection, delete the control file or over-ride the control file selections in the Design Wide Resources Pin Editor.

Hardware Setup

The GPIO is connected to the green LED.

Table 1 lists the pin connections required to use this code example on FM0+ kits.

Table 1. List of Pins

Pin	FM0-V48-S6E1A1	FM0-64L-S6E1C3
Green_LED:GPIO	P61	P3E

Components

Table 2 lists the PSoC Creator Components used in this example, as well as the hardware resources used by each.

Table 2. List of PSoC Creator Components

Component	Version	Hardware Resources
PDL_CLK	1.0	None
PDL_DT	1.0	DT block (one channel)
PDL_GPIO	1.0	GPIO pin

Parameter Settings

The CLK and GPIO Components use their default parameter settings. Only the Component instance names have been changed for readability.

The CLK Component is present in the design to cause the CLK module functions to be included from the PDL.

The DT Component uses mostly default parameter settings, with the following modifications.

Table 3: Component Settings

Tab	Setting	Value
None	Name	DT
Timer	U8Ch0PrescalerDiv	16
Interrupts	bCh0IrqEnable	true
	bCh0TouchNvic	true

Operation

Program the kit and observe the rate of the blinking green LED. It repeatedly blinks slowly for 5 seconds and then much faster for 5 seconds.

Related Documents

Table 4 lists all relevant application notes, code examples, knowledge base articles, device datasheets, and Component datasheets.

Table 4. Related Documents

PSoC Creator Component Datasheets	
PDL_CLK	Includes the CLM module API from the PDL (right-click on the component to access)
PDL_DT	Supports Periodic, Free-Run and One-Shot operation of the Dual Timer (right-click on the component to access)
PDL_GPIO	Supports firmware access to physical pins (right-click on the component to access)
Device Documentation	
S6E1A	FM0+ S6E1A-Series 5V Robust ARM® Cortex®-M0+ Microcontroller (MCU) Family
S6E1C	FM0+ S6E1C-Series Ultra Low Power ARM® Cortex®-M0+ Microcontroller (MCU) Family
Development Kit (DVK) Documentation	
FM0-V48-S6E1A1	ARM® Cortex®-M0+ FM0+ MCU Evaluation Board
FM0-64L-S6E1C3	ARM® Cortex®-M0+ MCU Starter Kit with USB and Digital Audio Interface

Document History

Document Title: CE216669 - FM0+ CLK Driving Dual Timer

Document Number: 002-16669

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5439701	YFS	09/16/16	New Code Example.
*A	5776623	YFS	6/16/17	Added search keyword so that user can quickly find Code Examples from the component instance popup menu. Updated logo and copyright date.
*B	5988572	YFS	12/8/17	Removing S6E1B support.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

Phone : 408-943-2600
Fax : 408-943-4730
Website : www.cypress.com

© Cypress Semiconductor Corporation, 2016-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.