CE215883 - FM0+ MFT Two PWMs

Two PWMs with constantly varying duty cycle are implemented in the Multi-Function Timer to drive the color of an RGB LED from blue to green.

Overview

The application uses a Free-Running Timer (FRT) to drive a pair of Output Compare Units (OCU) with an interrupt slowly modifying the OCU compare value. The OCU outputs are passed through the Waveform Generator (WFG) to pins connected to the green and blue LEDs.

The Multi-Function Timer (MFT) is configured in the "MFTs" tab of the Design-Wide Resources editor.

Requirements

Tool: PSoC Creator 4.0

Programming Language: C (GCC 4.9.3)

Associated Parts: All S6E1B parts

Related Hardware: FM0-100L-S6E1B8

Design

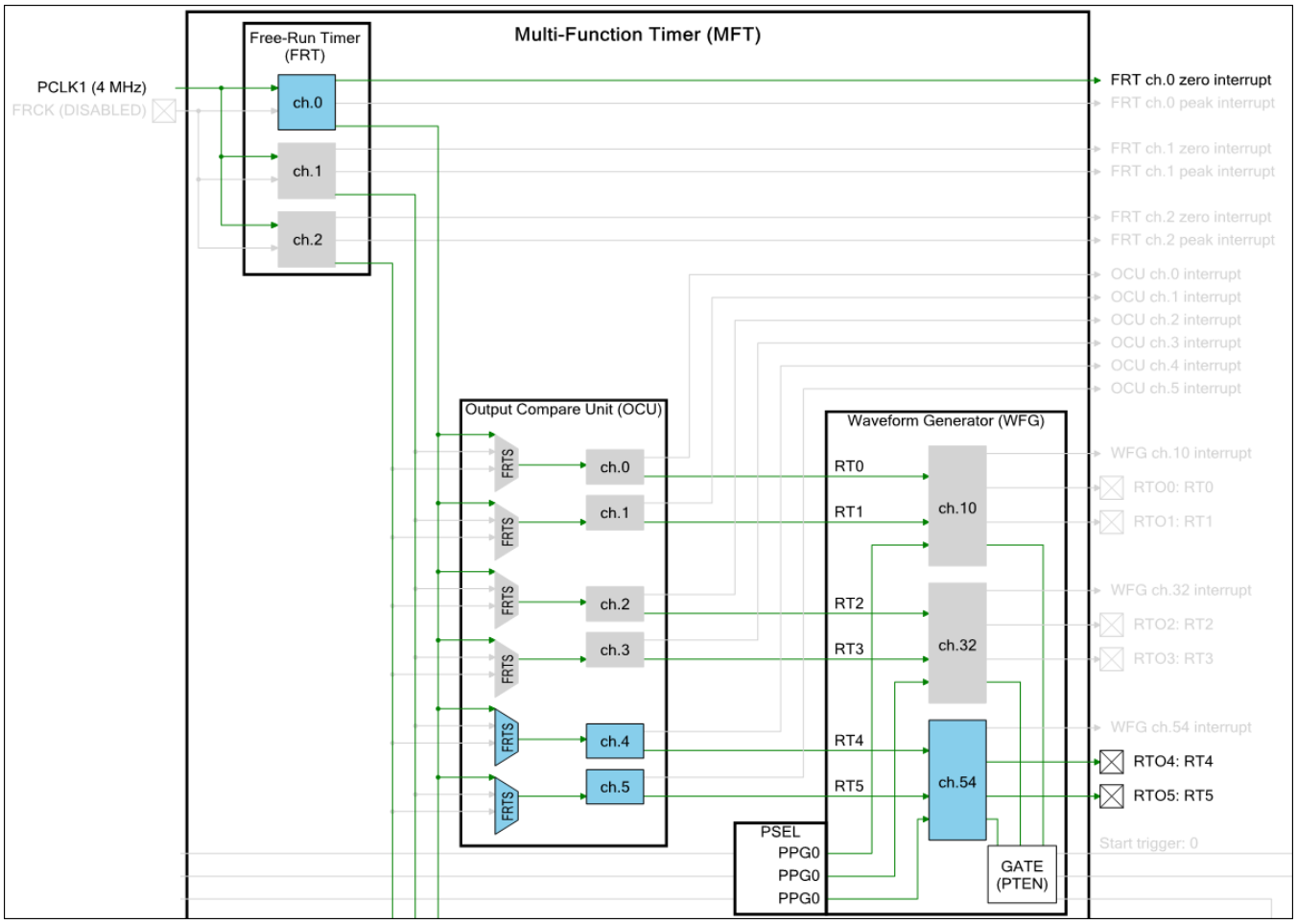
The MFT schematic in Figure 1 shows the overall MFT configuration. To see this in PSoC Creator, click **MFTs** in the Design Wide Resources file.

The FRT is configured to operate as an up/down counter (triangle wave) with an interrupt generated when the counter returns to zero. The interrupt handler increments the compare value in both OCUs (they always have the same value), resetting to the minimum value when the maximum is reached. The peak count set in firmware and does not change.

Both OCUs use this FRT as the source. As the FRT runs, the OCUs toggle the output on a compare match with the FRT counter. The OCUs are configured with different initial output values so that as one toggles high, the other toggles low. As a result the LEDs, to which these signals are connected, glow bright and dim in opposition, creating a gradual color transition from blue to green.

The WFG is configured as a pass through, and does not modify the signals from the OCU.

Figure 1: MFT Editor



The firmware performs following functions:

1. Initialize the WFG and set up the output pins
2. Initialize and enable the OCU channels (one starts high, the other low)
3. Initialize, set peak count, and start the FRT
4. Set the compare values to determine the duty cycle (must be in this order)
5. The FRT interrupt modifies the OCU compare value

Design Considerations

This Code Example does not change the FRT peak value. It does modify the OCU compare value, but only when the FRT is at zero. In a typical application, you would likely change one or the other (or both) dynamically. Changing either value at a random moment in the FRT cycle will result in an equally random PWM duty cycle until a cycle completes.

You can buffer either the FRT peak value or the OCU compare value to precisely control the moment when the new value takes effect.

Buffering the FRT Peak Value

To buffer this value, set *bEnBuffer* to True. When buffered, the peak value changes the next time the FRT reaches zero.

Buffering the OCU Compare Value (OCCP)

To buffer this value, set the value of *enOccpBufMode*. The options are to transfer the value at the FRT peak value, FRT zero value, or at both peak and zero.

Buffering the OCU Control Register (OCSE)

This code example uses default behavior for OCU operation and does not modify the OCU control register. The OCU control register defines what constitutes a match between the FRT timer and the OCU compare value. It also defines what happens to the output signal (held low, held high, inverted). You can change this value dynamically. The buffering options are identical to those for the OCU compare value.

Using Other MFT Blocks

Use the ICU Block to receive control signals from an external source. When the signal arrives, an interrupt occurs. You specify whether a rising edge, falling edge, or both edges qualify as a signal.

Use the ADCMP Component to control ADCs associated with the motor; for example, position sensors. The FRT provides the timing signal to control ADC conversions.

PDL Installation

The project assumes that you have installed the PDL in the location specified in the **Project Management** panel of the **Tools** > **Options** dialog. If that location is incorrect you will see the build error “The given PDL path is invalid. Unable to find required PDSC file.” To correct this problem in a newly-created project open the **Project** > **Properties** dialog and enter the correct path to the PDL. To avoid the problem in projects you create in the future, make sure you put the correct path in the **Tools** > **Options** dialog.

Hardware Setup

The RTO4 and RTO5 signals are connected to green and blue LEDs respectively.

Table 1 lists the pin connections required to use this code example on the FM0+ S6E1B8 kit.

Table 1. List of Pins

Pin	FM0-100L-S6E1B8
CyMft0_RTO4	P3E
CyMft0_RTO5	P3F

Peripheral clock 1 (PCLK1) is the clock source for the FRT. This example uses the default value of 4 MHz for PCLK1.

Components

Table 2 lists the PSoC Creator Components used in this example, as well as the hardware resources used by each.

Table 2. List of PSoC Creator Components

Component	Version	Hardware Resources
PDL_MFT (using FRT channel 0, OCU channels 4 and 5, WFG channel 54)	1.0	MFT block; two GPIO pins (RTO4 and RTO4)

Parameter Settings

The components in this code example use mostly default settings. Table 3 lists the modifications.

Table 3: Component Settings

Item	Name	Value
FRT channel 0	Configure	True
	enFrtMode	FrtUpDownCount
	bFrtZeroMatching	True
	pfnFrtZeroIrqCb	FrtZeroCallback
	bTouchNvic	True
OCU channel 4	Configure	True
	enPinState	RtLowLevel
OCU channel 5	Configure	True
	enPinState	RtHighLevel
WFG Channel 54	Configure	True

Operation

Program the kit and observe the RGB LED color change gradually from blue to green. The effect is repeated every few seconds.

Related Documents

Table 4 lists relevant application notes, code examples, knowledge base articles, device datasheets, and Component datasheets.

Table 4. Related Documents

Device Documentation	
S6E1B	FM0+ S6E1B-Series Ultra Low Power ARM® Cortex®-M0+ Microcontroller (MCU) Family
Development Kit (DVK) Documentation	
FM0-100L-S6E1B8	ARM® Cortex®-M0+ MCU Starter Kit with USB and SD Card Interface
Technical Reference Manual	
FM0+	FM0+ Peripheral Manual Timer Subsystem

Document History

Document Title: CE215883 - FM0+ MFT Two PWMs

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5440375	YFS	09/19/16	New Code Example.
*A	5823655	JETT	07/18/2017	Added search keyword so that user can quickly find Code Examples from the component instance popup menu. Updated logo and copyright date. Added FM0+ as prefix to title.

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