CE215703 - FM0+ UART Character Echo

A UART is implemented in a Multi-Function Serial (MFS) block. The firmware reads incoming characters and echoes them back over the serial line.

Overview

The application implements a UART in an MFS block. On the FM0+ kits the UART is connected to the CMSIS-DAP device, which acts as a bridge from the MCU to a PC-based terminal emulator. The firmware simply reads and echoes characters.

Requirements

Tool: PSoC Creator 4.0

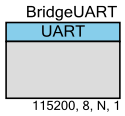
Programming Language: C (GCC 4.9.3)

Associated Parts: All S6E1A parts

Related Hardware: FM0-V48-S6E1A1

Design

The schematic file includes just the MFS component. It is configured to be a UART at 115200 baud and renamed “BridgeUART” as shown below.



The firmware performs following functions:

1. Initialize and start the UART
2. Read the UART input
3. Echo the data to UART output

Design Considerations

Pin Selection

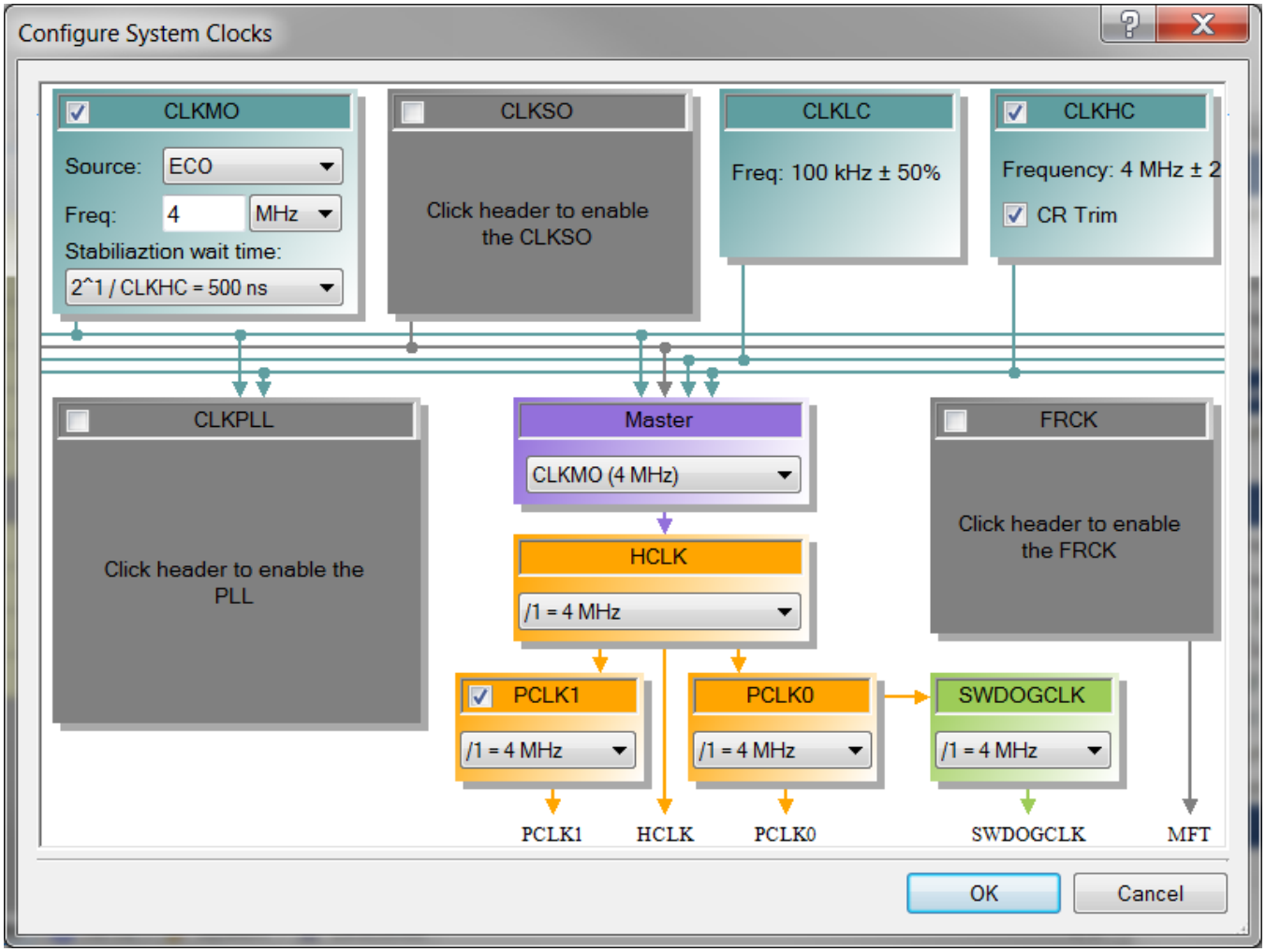
The project includes control files to automatically place the UART IO onto the appropriate pins for the supported kit hardware. To change the pin selections, delete the control file or over-ride the control file selections in the Design Wide Resources Pin Editor.

Baud Rate

Reliable UART communication depends largely on the accuracy of the baud rate. In FM0+ the UART baud rate is generated from the input clock to the MFS block. Because the MFS blocks are on APB1 the input clock is PCLK1. PCLK1 is sourced from the master clock. By default, the master clock is sourced from CLKHC, the device’s internal clock. CLKHC runs at 4MHz and has an accuracy of +/- 2%, which is not good enough for higher baud rates.

In order to improve the UART baud rate this project uses CLKMO as the source to the master clock. CLKMO is generated from an external oscillator on the kit and is accurate to 50ppm. In the Clocks Editor (Design-Wide Resources file) CLKMO is enabled and the frequency set to 4MHz. The Master clock is edited to use CLKMO instead of CLKHC. PCLK1 remains a 4MHz clock but with improved accuracy.

The System Clocks editor, shown below, is launched by double-clicking on any system clock in the DWR editor.



Hardware Setup

The UART is connected on the FM0+ kit hardware to an on-board CMSIS-DAP module. This enables serial communication to a PC (in addition to programming and debugging of the FM0+ MCU) through a USB cable. Refer to the kit User Guide for details on CMSIS-DAP operation.

Table 1 lists the pin connections required to use this code example on FM0+ kits.

Table 1. List of Pins

Pin	FM0-V48-S6E1A1
BridgeUART:SIN	P21
BridgeUART:SOT	P22

The CLKMO is connected to a 4MHz (50ppm) crystal oscillator.

Components

Table 2 lists the PSoC Creator Components used in this example, as well as the hardware resources used by each.

Table 2. List of PSoC Creator Components

Component	Version	Hardware Resources
PDL_MFS	1.0	MFS block and two pins

Parameter Settings

The “Multi-Function Serial UART” component macro uses mostly default parameter settings, with the following modifications.

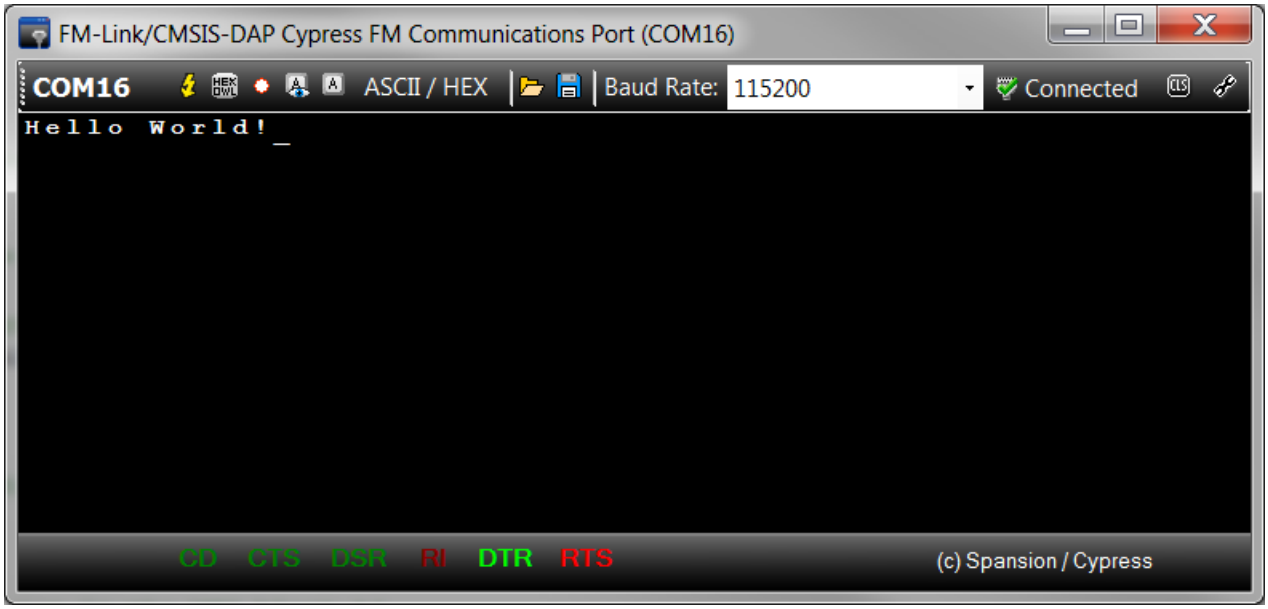
Table 3: Component Settings

Tab	Setting	Value
None	Name	BridgeUART
Basic	MFSConfig	UART
UART	u32UartBaudRate	115200
FIFO	u8ByteCount1	0
	u8ByteCount2	0

Operation

Use a terminal emulator, such as the Cypress Serial Port Viewer and Terminal, to connect to the kit. Be sure to set the baud rate to match the component and connect the program to the emulated serial port. Type characters into the emulator window and the kit echoes them back onto the screen.

Figure 1: Characters echoed to Cypress Serial Port Viewer and Terminal



Related Documents

Table 4 lists relevant application notes, code examples, knowledge base articles, device datasheets, and Component datasheets.

Table 4. Related Documents

PSoC Creator Component Datasheets	
PDL_MFS	Supports UART, I2C, CSIO (SPI) and LIN serial communications (right-click on the component to access)
Device Documentation	
S6E1A	FM0+ S6E1A-Series 5V Robust ARM® Cortex®-M0+ Microcontroller (MCU) Family
Development Kit (DVK) Documentation	
FM0-V48-S6E1A1	ARM® Cortex®-M0+ FM0+ MCU Evaluation Board

Document History

Document Title: CE215703 - FM0+ UART Character Echo

Document Number: 002-15703

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5375232	YFS	07/29/16	New Code Example.
*A	5435898	YFS	9/13/16	Removed support for S6E1C devices. Added table 4 for component parameters. New copyright.
*B	5447488	YFS	9/29/16	Added workspace file.
*C	5775153	YFS	6/15/17	Added search keyword so that user can quickly find Code Examples from the component instance popup menu. Updated logo and copyright date.
*D	5987551	YFS	12/7/17	Removing S6E1B support.
*E	6046933	JETT	2/1/18	Updating version numbers in code example

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