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# Analog Voltage Reference (Vref)

1.70

## Features




- Precision voltage reference for analog blocks
- Routable bandgap generated voltage references

## General Description

The Analog Voltage Reference (Vref) Component allows you to provide a stable precision reference voltage for the analog resources in your design. Each Component instance represents a physical analog reference source in the PSoC MCU. Depending on the allowed routing options available for your intended analog peripheral, you may choose from a list of supported reference voltages.

### Notes

- The on-chip voltage reference is not intended to source or sink current. If the intended usage is to drive a signal, then buffer the Vref signal with an Opamp Component.
- Every Vref is associated with an analog resource. To enable a Vref, the associated resource must be enabled. All Vrefs default their **AutoEnable** parameter to **true**. Since auto-enable Vrefs automatically enable the associated analog resource, all Vrefs are automatically enabled by default.

### When to Use a Vref

Use Vref Components for threshold detectors, reference inputs to analog-to-digital converters, comparators, and programmable gain amplifiers. They can also be used whenever you need a known voltage.

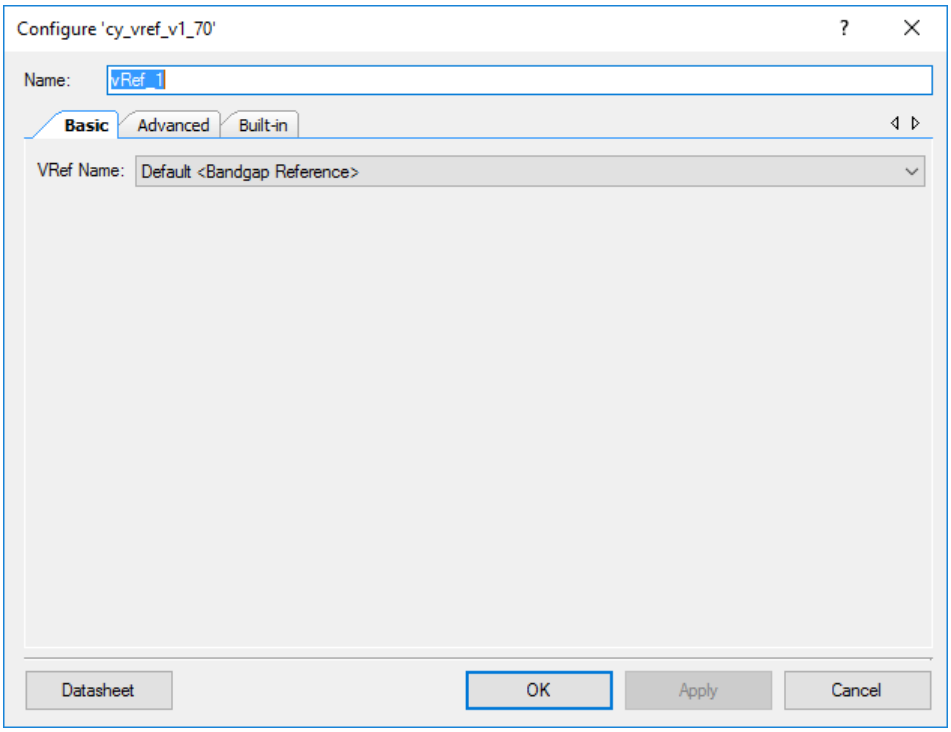
## Input/Output Connections

The Vref Component has a single output terminal that provides access to the selected voltage reference.

# Component Parameters

Drag a Vref onto your design and double click it to open the **Configure** dialog.

## Basic Tab



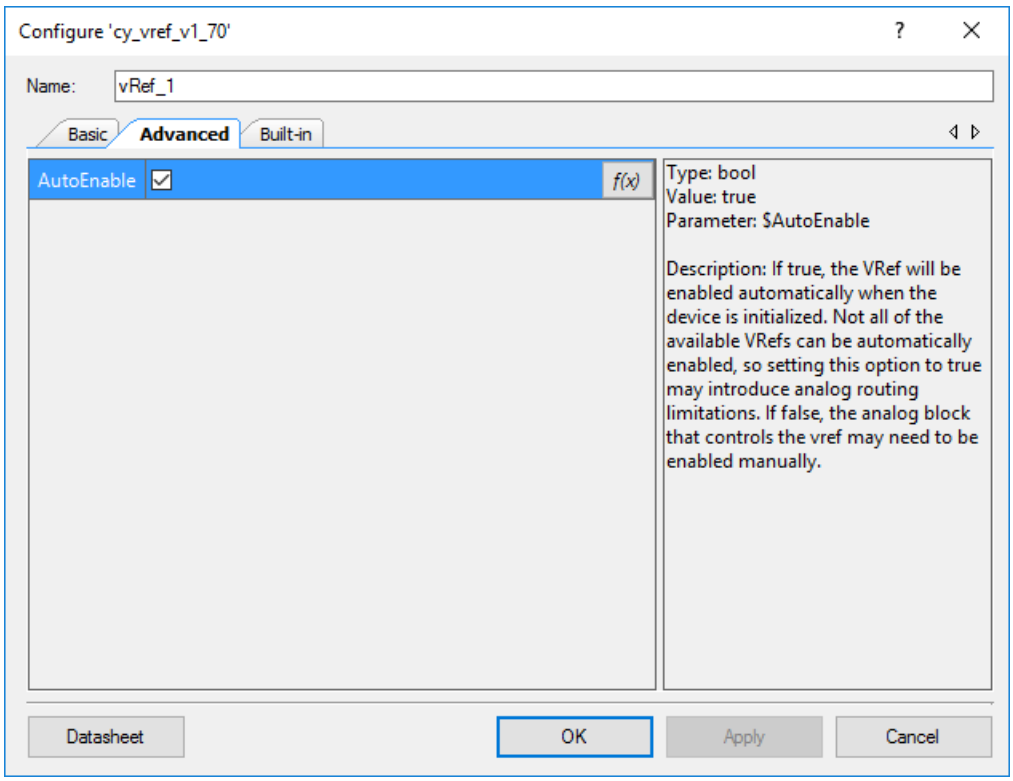

### Vref Name

Defines the Vref source:

- Bandgap Reference (**Default**) – Produced using the bandgap generator. Options for this reference are the following:
  - System (0.80 V) – routes the VREF from SRSS
  - Local (1.20 V) – routes the locally generated bandgap reference
  - External Pin (P9[7]) – routes the reference from the external VREF pin

**Note** The above options are available in drop-down list for the “Bandgap Value” option in the PSoC Creator System Editor.

## Advanced Tab




### AutoEnable

When **AutoEnable** is set to **true** (**Default**), Vref is enabled automatically when the device is initialized and the static analog routes are established.

If the intended use of the Vref Component is to connect to a non-dedicated block, then it is necessary for the dedicated block for that voltage reference to be consumed and powered in order to power the voltage reference.

### Notes

- Vref Components that require **AutoEnable** set to **true** have reduced routing capability because specific analog routing resources are required to supply the auto-enable Vref.
- If **AutoEnable** is set to **false**, then you will need to enable the associated analog peripheral (e.g., comparator, DAC, etc.) to be able to use that particular Vref source. Refer to the PSoC Creator Analog Editor to view the analog routing in your design.

# Functional Description

The Vref Component provides an analog voltage reference in your design by using one of the available voltage references. Connection to this particular voltage reference is through a single terminal. Depending on the source and available routing, the Vref Component may be shared among several Components.

## Placement

For a design project, the list of available voltage references is determined by what is available from the selected family or device. Refer to the PSoC Creator Analog Editor to see the resource usage and analog routing in your design.

**Note** If using the Vref Component in a library project, make the implementation device specific to be able to see the available reference sources.

**Note** If your design requires routing the voltage reference to destinations that are not meant for the dedicated analog block terminal, then additional resources may be used / needed.

# Component Changes

This section lists the major changes in the Component from the previous version.

| Version | Description of Changes | Reason for Changes / Impact |
|---|---|---|
| 1.70 | Added support for PSoC 6 devices. | Previous versions of the Component were not applicable to PSoC 6. |

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