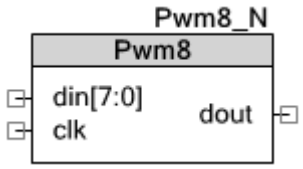
Byte Wide PWM with HW Control

JLS1_Pwm8 v1.0 **JLS1**

Features



- Hardware control of frequency
- 8-bit wide internal counter
- Output frequency can be adjusted on every input clock

General Description

This component divides the incoming clock based on the value of the byte wide input control signal. The output signal frequency is equal to:

$$dout_{freq} = clk_{freq} * din / 512$$

If the din input is changed over time, then the output frequency will average the din value over each clock cycle.

Pin Description

Pin	Type	Function
din[7:0]	Input	8-bit Divider
clk	Input	Clock
dout	Output	PWM Output

Support

PSoC Creator Community Components are developed and supported by the Cypress Developer Community. Go to www.cypress.com/CommunityComponents to discuss this and other Community Components.