# Voltage Reference (Vref)

1.70




## Features

- Precision voltage reference for analog blocks
- Routable bandgap generated voltage references: 0.256 V, 1.024 V
- Routable voltage supplies: Vdda, Vssa, Vccd, Vddd, Vbat, System-Wide Reference

## General Description

The Voltage Reference (Vref) component allows you to provide a stable precision reference voltage for the analog resources in your design. Each component instance represents a physical analog reference source in the PSoC device. Depending on the allowed routing options available for your intended analog peripheral, you may choose from a list of supported reference voltages.

The on-chip voltage reference uses a curvature compensated voltage bandgap with a resistor divider to generate reference voltages of 1.024 V and 0.256 V. The method achieves a fixed DC voltage reference that remains stable and agnostic to temperature and supply voltage variations. You may also use the Vref component to route a voltage supply to your design, as long as the path is valid.

**Notes**

- The on-chip voltage reference is not intended to source or sink current. If the intended usage is to drive a signal, then buffer the Vref signal with an Opamp component.
- Every Vref is associated with an analog resource. To enable a Vref, the associated resource must be enabled. All Vrefs default their **AutoEnable** parameter to **true**. Since auto-enable Vrefs automatically enable the associated analog resource, all Vrefs are automatically enabled by default.

### When to Use a Vref

Use Vref components for threshold detectors, reference inputs to analog-to-digital converters, comparators, and programmable gain amplifiers. They can also be used whenever you need a known voltage.

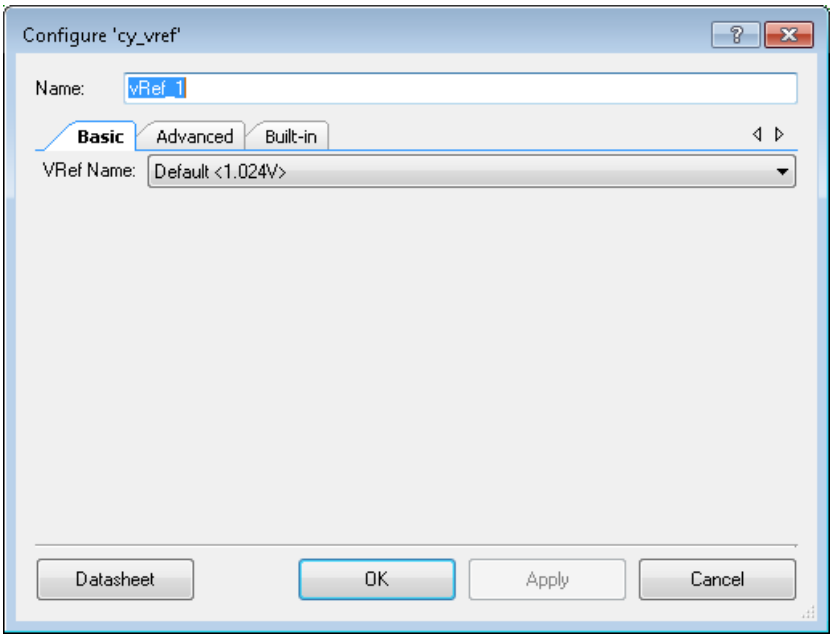
# Input/Output Connections

The Vref component has a single output terminal that provides access to the selected voltage reference.

# Component Parameters

Drag a Vref onto your design and double click it to open the **Configure** dialog.

## Basic Tab



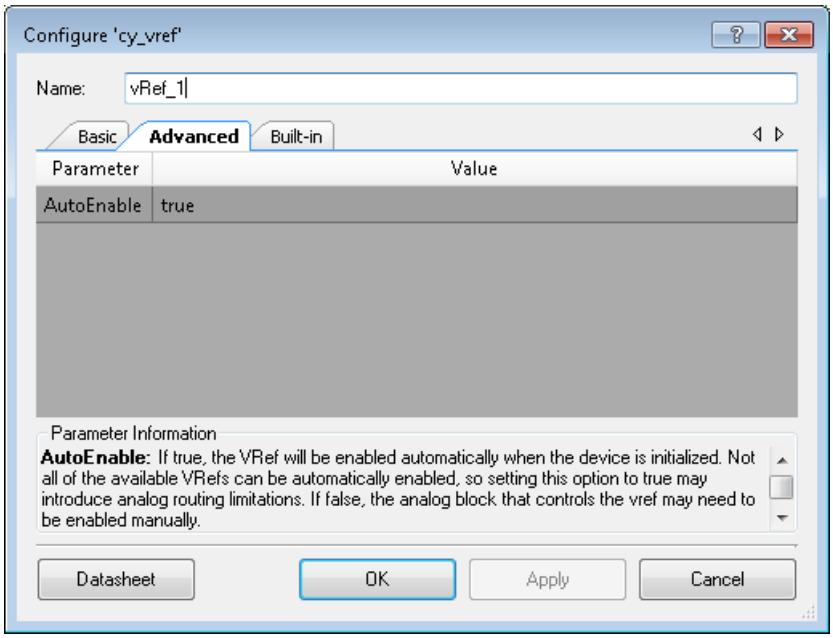

### VRef Name

Defines the Vref source:

- 1.024 V (**Default**) – Produced using bandgap generator. Most widely supported voltage reference for analog peripherals.
- Vssa (GND) – Internal Vssa voltage.
- 0.256 V – Produced using bandgap generator. Supported in select analog peripherals.
- Vdda/2 – Derived from Vdda (HiZ) using a resistive divider. (Cannot be used in the design if a Vref component instance with Vdda (HiZ) exists, since they share the same source).
- Vdda (HiZ) – The Vdda voltage reference is provided with a resistive divider and so has high impedance. (Cannot be used in the design if a Vref component instance with Vdda/2 exists since they share the same source.)

- Vccd – Special 1.8-V reference that is only available as a source for SIO pins.
- Vddd – Internal Vddd voltage. Cannot be used in design if Vbat or Vdda are used.
- Vbat – Internal Vbat voltage. Cannot be used in design if Vddd or Vdda are used.
- Vdda – Internal Vdda voltage. Cannot be used in design if Vddd or Vbat are used.
- System-Wide Reference – Design-wide voltage reference derived from the programmable reference block. Not available for PSoC 3 or PSoC 5LP devices.

## Advanced Tab




### AutoEnable

When **AutoEnable** is set to **true** (**Default**), Vref is enabled automatically when the device is initialized and the static analog routes are established. This parameter applies to the 1.024 V and 0.256 V options for connections that are not dedicated to analog peripherals.

When a 1.024 V or 0.256 V Vref is connected to intended analog block connections such as the comparator, the device automatically enables the Vref when the connected components are enabled. AutoEnable is not necessary in these cases.

If the intended use of the Vref component is to connect to a non-dedicated block, then it is necessary for the dedicated block for that voltage reference to be consumed and powered in order to power the voltage reference.

### Notes

- Vref components that require **AutoEnable** set to **true** have reduced routing capability because specific analog routing resources are required to supply the auto-enable Vref.
- If **AutoEnable** is set to **false**, then you will need to enable the associated analog peripheral (e.g. comparator, DAC) to be able to use that particular Vref source. Refer to the Analog tab of the Design Wide Resources file to view the analog routing in your design.

# Functional Description

The Vref component provides an analog voltage reference in your design by using one of the available voltage references. Connection to this particular voltage reference is through a single terminal. Depending on the source and available routing, the Vref component may be shared among several components.

## Placement

For a design project, the list of available voltage references is determined by what is available from the selected family or device.

**Note** If using the Vref component in a library project, make the implementation device specific to be able to see the available reference sources.

The table below shows the list of supported voltage references for the dedicated analog blocks. All analog block reference sources are buffered by a low-power 5uA high accuracy buffer. You may use the table as a guide to determine the relationship between the voltage reference and the associated analog block.

**Note** If your design requires routing the voltage reference to destinations that are not meant for the dedicated analog block terminal, then additional resources may be used / needed.

**Note** Refer to the Analog tab of the Design Wide Resources editor to see the resource usage and analog routing in your design.

| Analog block | Reference | Description |
|---|---|---|
| Comparator | 1.024 V | To Comparator negative inputs. |
| | 0.256 V | To Comparator negative inputs. |
| Opamp | 1.024 V | To Opamp positive inputs. |
| SC/CT | 1.024 V | To SC/CT block positive and negative inputs. For example, PGA and TIA components. |

| Analog block | Reference | Description |
|---|---|---|
| DAC | 0.256 V | Reference voltage for DAC during VDAC mode operation. |
| DeltaSig ADC | 1.024 V | Reference voltage to Delta Sigma Modulator. This voltage is additionally buffered in the DSM block by a 10 uA buffer. |

The following table is a summary of routing resource used to connect voltage supplies in your design as voltage references.

| Route source | Reference | Description |
|---|---|---|
| ABUSL0 | Vdda (HiZ) | All analog blocks connected to the analog local bus ABUSL0 can get this voltage. Cannot be used if Vdda/2 is also used in the design via ABUSL0. |
| | Vdda/2 | All analog blocks connected to the analog local bus ABUSL0 can get this voltage. Cannot be used if Vdda (HiZ) is also used in the design via ABUSL0. |
| Internal | Vccd | Uses the device Vccd source as voltage reference for the SIO pin. |
| | Vssa | Uses the internal device ground as reference. |
| Pin | Vddd | Connects to the Vddd pin |
| | Vbat | Connects to the Vbat pin (Passes through internal LPF). |
| | Vdda | Connects to the Vdda pin. |

## System-Wide Reference

The System-Wide Reference is based on the dedicated programmable reference hardware block in the silicon (not available for PSoC 3 or PSoC 5LP devices).

The System-Wide Reference provides an adjustable, stable reference voltage for the analog resources in your design. It could be based on either Vdda or the Bandgap voltage in 1/16 increments. This reference may be connected to any high impedance input, such as the input to an opamp or comparator. It cannot be routed to a GPIO unless it is buffered with an opamp.

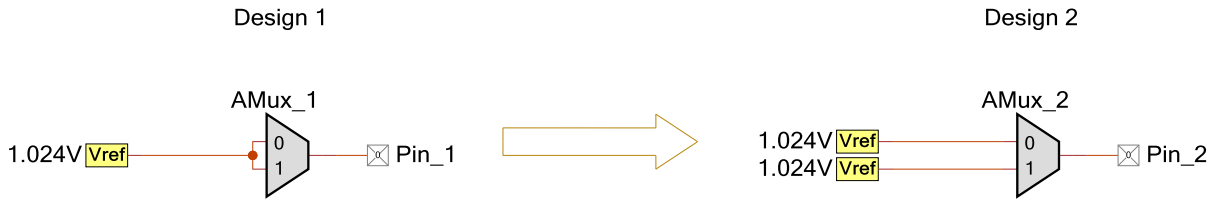
Refer to the System Editor of the Design-Wide Resources (*<project>.cydwr*) file to see/adjust the configuration of the System-Wide Reference in your design.

You can also tune the Design-Wide Resources settings using System APIs. For more details, refer to device *System Reference Guide*.

### AutoEnable Vref Connecting to an Amux Switchable Connection

An auto-enable 1.024 V or a 0.256 V Vref component must be by itself when connected to an Amux switchable connection. This restriction is introduced so the analog routine can handle the auto-enable Vref feature without ambiguities.

For example, in order for Design 1 to work it must be converted as shown in Design2.




**Note** If you choose to set the **AutoEnable** parameter of the Vref component to **false**, this restriction does not apply. However it is likely that you will need to manually enable the associated analog block to supply power to the voltage reference.

### Low Power Mode

In low power mode, Vssa (GND) and Vdda (HiZ) are the only two Vref options available.

## Resources

When **AutoEnable** is enabled for a non-dedicated analog signal, the bandgap generated Vref (1.024 V and 0.256 V) consumes the associated analog block (e.g. a comparator). This is a necessary step in order to control the power setting of the voltage reference. Hence the analog block will no longer be available as a resource to be used in your design.

# DC and AC Electrical Characteristics

The following values indicate expected performance based on initial characterization data. Note that the 1.024 V voltage reference calibrations were performed for the buffered ADC_DelSig reference.

## Voltage Reference Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{ref}$ | 1.024V Vref = 1.024 [1] | Initial trimming, 25 °C | | 1.024 (+/- 0.5%) | | V |
| | Temperature drift [2] | Box method | – | – | 30 | ppm/°C |
| | Long term drift | | – | 100 | – | ppm/Khr |
| | Thermal cycling drift (stability) [2] | | – | 100 | – | Ppm |
| $R_{vdda}$ | Vdda/2 resistor division ratio accuracy | | -1% | – | +1% | % |
| | DC Offset (process variation) | | – | 0 | 3.5 | mV |

1 Although the +/-0.1% error is true for the output of the buffered Delsig reference, it is not true for any of the 1.024 V Vref components that a user places. These voltages can easily be off by +/-0.5% or more.

2 Based on device characterization (Not production tested).

# Component Changes

This section lists the major changes in the component from the previous version.

| Version | Description of Changes | Reason for Changes / Impact |
|---|---|---|
| 1.70.a | Minor datasheet edits. | |
| 1.70 | Added System-Wide Reference to the Vref sources.<br>Edited datasheet to add note about the 1.024 V reference error. | PSoC Analog Coprocessor device support. |
| 1.60.a | Expanded Functional Description section | Added placement details and analog block relationship |
| | Updated DC and AC electrical characteristics | Added $R_{vdda}$ |
| | Miscellaneous datasheet updates | General cleanup and added clarifying information |
| 1.60 | Removed IgnoreSleep parameter from the customizer. | The Vref component can't remain powered in low power mode. The IgnoreSleep parameter has no effect. |
| 1.50.c | Minor datasheet edits and updates | |
| 1.50.b | Updated description of Vdda(HiZ) | Description was unclear. |
| | Updated AutoEnable section to include quarter volt Vref | 0.256-V Vref has the same AutoEnable properties as the 1.024-V Vref. |
| 1.50.a | Added characterization data to datasheet | |
| | Datasheet edits | |
| 1.50 | Added AutoEnable and IgnoreSleep parameters to the customizer. | The AutoEnable and IgnoreSleep parameters provide additional functionality and a more intuitive user experience. |
| | Added the special purpose Vccd Vref for use with SIO pins. | The Vccd reference is used with SIO pins. |
| | Added Vbat, Vddd, and Vdda references. | The Vbat, Vddd, and Vdda references were added to provide additional functionality. |

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