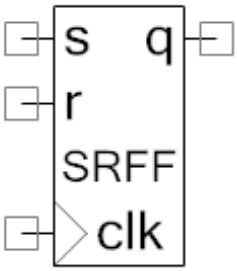
SR Flip Flop
1.0



Features

- Clocked for safe use in synchronous circuits.
- Configurable width for array of SR Flip Flops.

General Description

The SR Flip Flop stores a digital value that can be set or reset.

When to Use an SR Flip Flop

Use the SR Flip Flop to implement sequential logic.

Input/Output Connections

This section describes the various input and output connections for the SR Flip Flop.

s – Input

This input sets the output (to logic high ‘1’). The output does not change until the next rising edge of the clock.

r – Input

This input resets the output (to logic low ‘0’). The output does not change until the next rising edge of the clock.

clock – Input

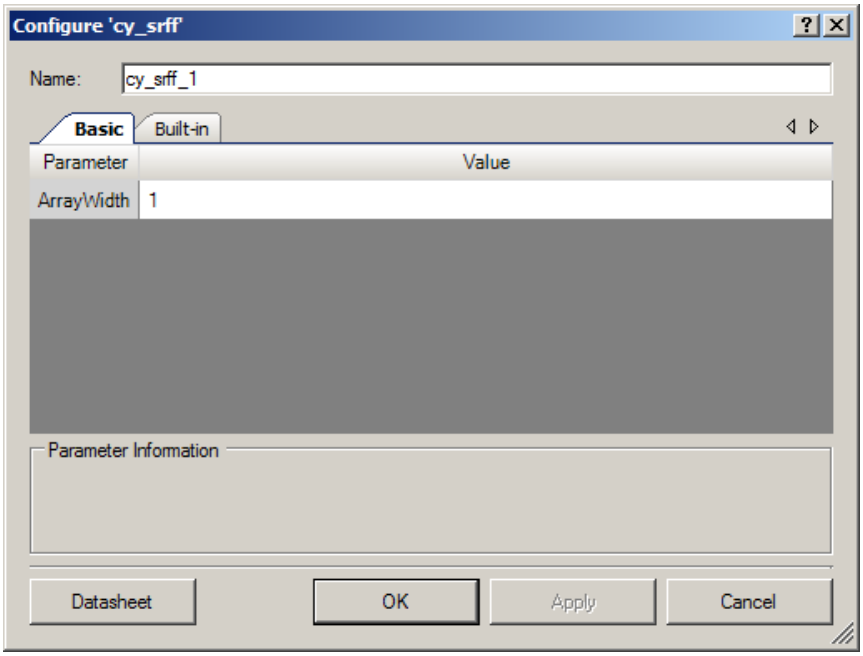
The clock signal determines when the output will change. The output changes when a rising edge of the clock is detected.

q – Output

The stored value.

Component Parameters

Drag a Toggle Flip Flop onto your design and double-click it to open the **Configure** dialog.



The SR Flip Flop provides the following parameters.

ArrayWidth

You can create an array of SR Flip Flops, which is useful if the input or output is a bus. This parameter defines the bus width of the t and q terminals. The value must be between 1 and 32. The default is **1**.

Functional Description

The SR Flip Flop is implemented in macrocell product terms using the following logical equation:

$Q = (Q_{PREV} \mid S) \& \sim R$

Note that Reset dominates Set.

Table 1. 1-ArrayWidth SR Flip Flop Truth Table

Q_{PREV}	S	R	Q
0	0	0	0
1	0	0	1
X	1	0	1
X	X	1	0

Resources

The SR Flip Flop uses one macrocell. If the ArrayWidth parameter is greater than 1, the SR Flip Flop uses a number of macrocells equal to ArrayWidth. All SR Flip Flop components in the same PLD must have the same clock signal for clocking.

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined: project deviations – deviations that are applicable for all PSoC Creator components and specific deviations – deviations that are applicable only for this component. This section provides information on component specific deviations. Non PSoC 6 project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment. For PSoC 6, refer to PSoC Creator Help > Building a PSoC Creator Project > Generated Files (PSoC 6) for information on MISRA compliance and deviations for files generated by PSoC Creator.

The SR Flip Flop component does not have any C source code APIs.

DC and AC Electrical Characteristics

The SR Flip Flop component supports the maximum device frequency.

Component Changes

This section lists the changes in the Component from the previous version.

Version	Description of Changes
1.0.b	Updated MISRA section. Added PSoC 6 support.
1.0.a	Minor datasheet update.
1.0	Initial release of the SR Flip Flop Component.

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