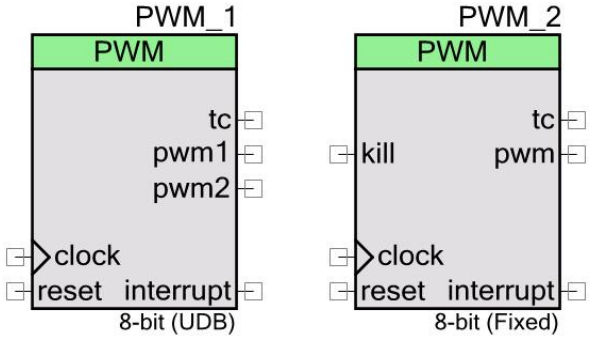
Pulse Width Modulator (PWM)

3.30

Features



- 8- or 16-bit resolution
- Multiple pulse width output modes
- Configurable trigger
- Configurable capture
- Configurable hardware/software enable
- Configurable dead band
- Multiple configurable kill modes
- Customized configuration tool
- Fixed-function (FF) implementation for PSoC 3 and PSoC 5LP devices

General Description

The PWM component provides compare outputs to generate single or continuous timing and control signals in hardware. The PWM provides an easy method of generating complex real-time events accurately with minimal CPU intervention. PWM features may be combined with other analog and digital components to create custom peripherals.

For PSoC 3 and PSoC 5LP devices, the component can be implemented using FF blocks or universal digital blocks (UDBs). PSoC 4 devices support only UDB implementation. A UDB implementation typically has more features than an FF implementation. If the design is simple enough, consider using FF and save UDB resources for other purposes. The PWM generates up to two left- or right-aligned PWM outputs or one center-aligned or dual-edged PWM output. The PWM outputs are double buffered to avoid glitches caused by duty cycle changes while running. Left-aligned PWMs are used for most general-purpose PWM uses. Right-aligned PWMs are typically only used in special cases that require alignment opposite of left-aligned PWMs. Center-aligned PWMs are most often used in AC motor control to maintain phase alignment. Dual-edged PWMs are optimized for power conversion where phase alignment must be adjusted.

The optional dead band provides complementary outputs with adjustable dead time where both outputs are low between each transition. The complementary outputs and dead time are most often used to drive power devices in half-bridge configurations to avoid shoot-through currents

and resulting damage. A kill input is also available that immediately disables the dead band outputs when enabled. Four kill modes are available to support multiple use scenarios.

Two hardware dither modes are provided to increase PWM flexibility. The first dither mode increases effective resolution by two bits when resources or clock frequency preclude a standard implementation in the PWM counter. The second dither mode uses a digital input to select one of the two PWM outputs on a cycle-by-cycle basis; this mode is typically used to provide fast transient response in power converts.

The trigger and reset inputs allow the PWM to be synchronized with other internal or external hardware. The optional trigger input is configurable with the **Trigger Mode** parameter. Only hardware trigger is available in the component for starts the PWM. The PWM cannot be triggered with an API call. A rising edge on the reset input causes the PWM counter to reset its count as if the terminal count was reached. The enable input provides hardware enable to gate PWM operation based on a hardware signal.

An interrupt can be programmed to be generated under any combination of the following conditions: when the PWM reaches the terminal count or when a compare output goes high.

When to Use a PWM

The most common use of the PWM is to generate periodic waveforms with adjustable duty cycles. The PWM also provides optimized features for power control, motor control, switching regulators, and lighting control. You can also use the PWM as a clock divider by driving a clock into the clock input and using the terminal count or a PWM output as the divided clock output.

PWMs, timers, and counters share many capabilities, but each provides specific capabilities. A Counter component is better used in situations that require the counting of a number of events but also provides rising edge capture input as well as a compare output. A Timer component is better used in situations focused on timing the length of events, measuring the interval of multiple rising and/or falling edges, or for multiple capture events.

Input/Output Connections

This section describes the various input and output connections for the PWM. Some I/Os may be hidden on the symbol under the conditions listed in the description of that I/O.

Note All signals are active high unless otherwise specified.

Input	May Be Hidden	Description
clock	N	The “clock” input defines the signal to count. The counter is incremented or decremented on each rising edge of the clock.
reset	N	This input resets the period counter to **Period** and continues normal operation. **Note** For UDB implementation in Reset, the “pwm”, “pwm1”, and “pwm2” outputs are driven to ‘0’. The “reset” signal is synchronous for the component. The outputs will reflect component reset state up to two clock cycles. For FF implementation, see Reset Signal in Fixed Function Implementation section. In fixed-function implementation, if dead band is enabled then both outputs (“ph1” and “ph2”) will be driven to ‘0’. If dead band is disabled, then ”pwm” output will be driven to ‘0’.
enable	Y	The “enable” input works in conjunction with software enable and “trigger” input (if the “trigger” input is enabled) to enable the period counter and apply it to the “pwm” outputs. The “enable” input is not visible if the **Enable Mode** parameter is set to **Software Only**. This input is not available when the fixed-function PWM implementation is chosen. **Note** The “enable” signal is synchronous for the component. The outputs and component behavior will reflect component enable state up to two clock cycles.
kill	Y	If “kill” signal is active, the PWM block behaves differently for different configurations. In fixed-function implementation, if dead band is enabled then both outputs (“ph1” and “ph2”) will be driven to ‘0’. If dead band is disabled, then ”pwm” output will be driven to ‘0’. Kill signal has no impact on period counter operation. The “tc” signal will be triggered every period independently from the logic level on the “kill” input. In UDB implementation for both devices, if dead band is enabled then the “pwm”, “pwm1” and “pwm2” outputs will be driven to ‘0’, “ph1” output to ‘0’ and “ph2” output to ‘0’. If dead band is disabled, then “pwm”, “pwm1” and “pwm2” will be driven to ‘0’. The “kill” signal has no impact on period counter operation. The “tc” signal will be triggered every period independently from the logic level on the “kill” input.
cmp_sel	Y	The “cmp_sel” input selects either the “pwm1” or “pwm2” output as the final output to the “pwm” terminal. When the input is ‘0’ (low), the “pwm” output is “pwm1” and when the input is ‘1’ (high), the “pwm” output is “pwm2”, as shown in the configuration tool waveform viewer. The “cmp_sel” input is visible when the **PWM Mode** parameter is set to **Hardware Select**.
capture	Y	The “capture” input forces the period counter value into the read FIFO. There are several modes defined for this input in the **Capture Mode** parameter. The “capture” input is not visible if the **Capture Mode** parameter is set to **None**.

Input	May Be Hidden	Description
trigger	Y	The “trigger” input enables the operation of the PWM. The functionality of this input is defined by the **Trigger Mode** and **Run Mode** parameters. After the PWM_Start() API command, the PWM is enabled. However, the counter does not decrement, and outputs do not changes until the trigger condition has occurred. For the UDB implementation of the PWM, the “trigger” input is registered with the input clock and so the counter starts and outputs change one clock after the “trigger” input is asserted. The trigger condition is set with the **Trigger Mode** parameter. The “trigger” input is not visible if the parameter is set to **None**. The PWM cannot be triggered with an API call.

Output	May Be Hidden	Description
tc	N	The terminal count (“tc”) output is ‘1’ when the period counter is equal to zero. In normal operation this output is ‘1’ for a single cycle where the counter is reloaded with period. This output is registered and synchronized to the block clock input of the component. **Note** For FF implementation, the “tc” output is “ph2” output, if dead band is enabled. If the PWM is stopped with the period counter equal to zero, then this signal remains high until the period counter is no longer zero.
interrupt	Y	The “interrupt” output is registered logical OR of the group of possible interrupt sources. This signal goes high while any of the enabled interrupt sources are true. The “interrupt” output remains asserted until the software reads out the status register. In order to receive subsequent interrupts, the interrupt is cleared by reading the status register using the PWM_ReadStatusRegister() API. The “interrupt” output is only visible if the **Use Interrupt** parameter is set. This allows the status register to be removed for resource optimization as necessary.
pwm/pwm1	Y	The “pwm” or “pwm1” output is the first or only pulse-width modulated output. This signal is defined by **PWM Mode**, compare modes, and compare values, as indicated in waveforms in the **Configure** dialog. When the instance is configured in **One Output**, **Dual Edge**, **Hardware Select**, **Center Align**, or **Dither** PWM modes, then the output “pwm” is visible. Otherwise, the output “pwm1” is visible with “pwm2” the other pulse-width signal. This output is registered and synchronized to the block clock input of the component. **Note** For FF implementation, the “pwm” output is “ph1” output, if dead band is enabled.
pwm2	Y	The “pwm2” output is the second pulse width modulated output. The “pwm2” output is only visible when **PWM Mode** is set to **Two Outputs**. This output is registered and synchronized to the block “clock” input of the component.
ph1/ph2	Y	The “ph1” and “ph2” outputs are the dead band phase outputs of the PWM. In all modes where only the “pwm” output is visible, these are the phased outputs of the “pwm” signal, which is also visible. When **PWM Mode** is set to **Two Outputs**, these signals are the phased outputs of the “pwm1” signal only. Both of these outputs are visible if dead band is enabled in 2 to 4 or 2 to 256 modes and are not visible if dead band is disabled. These outputs are registered and synchronized to the block clock input of the component. **Note** These ouput signals are available for UDB implementation only. For FF implementation, see the pwm and tc output descriptions, as well as the Fixed-Function Block Limitations section for details.

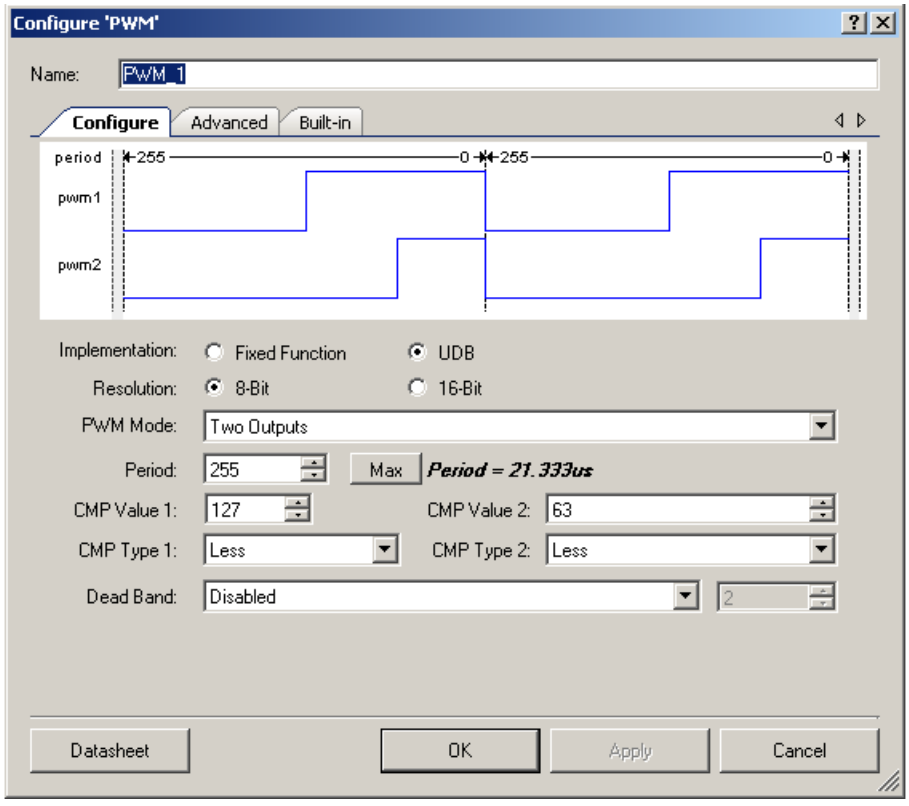
Component Parameters

Drag a PWM component onto your design and double click it to open the **Configure** dialog. The dialog contains two main tabs: **Configure** and **Advanced**.

Hardware versus Software Configuration Options

Hardware configuration options change the way the project is synthesized and placed in the hardware. You must rebuild the hardware if you make changes to any of these options. Software configuration options do not affect synthesis or placement. When setting these parameters before build time you are setting their initial value, which may be modified at any time with the APIs provided. Most parameters described in the next sections are hardware options. The software options are noted as such.

Configure Tab (Default Configuration)



Implementation

This parameter allows you to choose between a **Fixed Function** and a **UDB** implementation of the PWM. If this parameter is set to **Fixed Function**, the PWM is implemented in a fixed function block with the associated limitations (see Fixed-Function Block Limitations section) of that block.

Resolution

The **Resolution** parameter defines the bit-width resolution of the period counter.

Resolution	Maximum Period Count Values
8 (default)	255
16	65,535

Note If **PWM Mode** is set to **Center Align**, the component requires counting up to the incremented period value and then back down to zero, doubling the incremented period of the PWM. In this mode, configured period is limited to 254 for an 8-bit PWM and to 65534 for 16-bit PWM. The real PWM period will be equal to (configured in customizer period + 1) x 2. See Center Aligned section for details.

PWM Mode

The **PWM Mode** parameter defines the overall functionality of the PWM. It is disabled if **Implementation** is set to **Fixed Function**.

This parameter has a tremendous influence on the visible pins of the symbol as well as the functionality of the pwm, pwm1, and pwm2 outputs as depicted in the waveforms shown in the configuration tool. Options include:

- **One Output** – Only a single PWM output. In this mode the pwm output is visible
- **Two Output** – Two individually configurable PWM outputs. In this mode the pwm1 and pwm2 outputs are visible
- **Dual Edge** – A single dual-edged output created by ANDing together the pwm1 and pwm2 signals. In this mode the pwm output is visible.
- **Center Align** – A single center-aligned output created by having the counter count up to the incremented period value and back down to zero, while creating one center-aligned pulse width based on the compare value. In this mode the pwm output is visible.
- **Dither** – A single output selected from the two internal pwm signals (pwm1 and pwm2) by a hardware state machine included in the pwm hardware implementation. You select between a 0.00, 0.25, 0.50 or 0.75 bit increase in the output pulse width and the hardware controls the selection between the two pwm signals to make this happen. In this case the compare values are set to compare and compare+1. In this mode the pwm output is visible.

- **Hardware Select** – A single output selected from the two internal pwm signals by a hardware input pin cmp_sel. When cmp_sel is low the pwm1 signal is output on the pwm output pin, when cmp_sel is high the pwm2 signal is output on the pwm output pin. In this mode the pwm output is visible.

Period (Software)

The **Period** parameter defines the initial starting value of the counter and the value any time the terminal count is reached and the PWM mode allows reloading of the period counter.

The PWM is implemented as a down counter counting from the **Period** value to zero. The period is limited on the high side by the resolution of the PWM. For an 8-bit PWM the period value has a maximum of 255. Otherwise the period value has a maximum of 65535. When the PWM mode is configured in Center Aligned mode the PWM counts up from zero to the period value and then back down to zero. The period value in Center Aligned mode is twice as long as all other modes because of this special functionality. The period value may be changed at any time by the PWM_WritePeriod() API Call. The parameter holds only the initial value written during configuration.

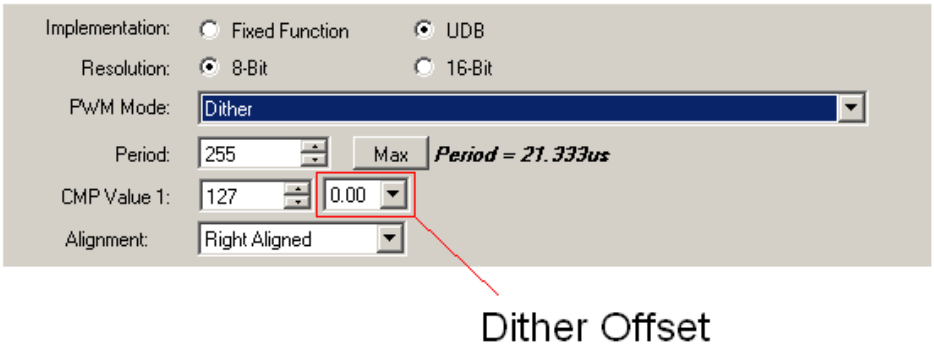
CMP Value 1 / CMP Value2 (Software)

The compare values define the compare output functionality in conjunction with the hardware **Compare Type** options.

The compare values are limited on the high side by the resolution of the PWM. For an 8-bit PWM the compare value has a maximum of 255. Otherwise the compare value has a maximum of 65535. The compare values may be changed at any time by the PWM_WriteCompare1() and PWM_WriteCompare2() API calls. These parameters hold only the initial value written during configuration.

Dither Offset

The **Dither Offset** parameter configures the functionality of the pwm output when **PWM Mode** is set to **Dither**.



A dither-mode PWM is implemented as a hardware-select-mode PWM with the caveat that the first and compare values have a difference of 1 and both compare modes are identical. There is also a built-in state machine controlling the hardware select. In this mode, the cmp_sel input is not available. You can set the offset as 0.00, 0.25, 0.50, and 0.75, with the parameter field visible in this mode. If the offset is configured as 0.00, then the output is always the compare1 output. When set to 0.25 the output is compare1 for three cycles and compare1 + 1 for a single cycle.

Dither Mode	Cycle 0	Cycle 1	Cycle 2	Cycle 3
0.00	Compare1	Compare1	Compare1	Compare1
0.25	Compare1 + 1	Compare1	Compare1	Compare1
0.50	Compare1	Compare1 + 1	Compare1	Compare1 + 1
0.75	Compare1 + 1	Compare1 + 1	Compare1 + 1	Compare 1

Alignment

The **Alignment** parameter is available when **PWM Mode** is set to **Dither**. Options include:

- **Right Aligned**
- **Left Aligned**

CMP Type 1 / CMP Type 2 (Software)

The compare value parameters define the two period counter comparisons that make up the PWM outputs. These are implemented differently for each of the **PWM Modes**, so they are typically controlled with the configuration tool. Each of the two compare mode parameters can be set independently to one of the following enumerated types. Options include:

- **Less** – Compare output is true if period counter is less than the corresponding compare value.
- **Less or Equal** – Compare output is true if period counter is less than or equal to the corresponding compare value.
- **Greater** – Compare output is true if period counter is greater than the corresponding compare value.
- **Greater or Equal** – Compare output is true if period counter is greater than or equal to the corresponding compare value.
- **Equal** – Compare output is true if period counter is equal to the corresponding compare value.
- **Firmware Control** – The **Firmware Control** option provides for a more flexible resource usage model in which the compare mode can be set during run time. The compare modes

may be changed at any time by the PWM_SetCompareMode1 and PWM_SetCompareMode2 API calls. Default value is Greater_Or_Equal. These parameters hold only the initial mode written during configuration. If any option other than **Firmware Control** is chosen, the hardware is preconfigured and fixed at that configuration at build time. In this case, the SetCompareMode APIs are removed from the compilation and therefore are not available.

Dead Band

The **Dead Band** parameter enables or disables the dead band functionality of the PWM. Dead band modes are slightly different in the fixed-function implementation. If dead band mode is one of the two enabled options then the ph1 and ph2 outputs are visible. Options include:

- **Disabled** – No dead band
- **0-3 Counts** – Dead band is implemented on the pwm or the pwm1 output with a maximum of three counts. This mode is applicable for FF implementation only.
- **2-4 Clock Cycles** – Dead band is implemented on the pwm or the pwm1 output with a maximum of four clock cycles. This mode is applicable for UDB implementation only.
- **2-256 Clock Cycles** – Dead band is implemented on the pwm or the pwm1 output with a maximum of 256 clock cycles. This is implemented in a datapath for the counter. This mode is applicable for UDB implementation only.

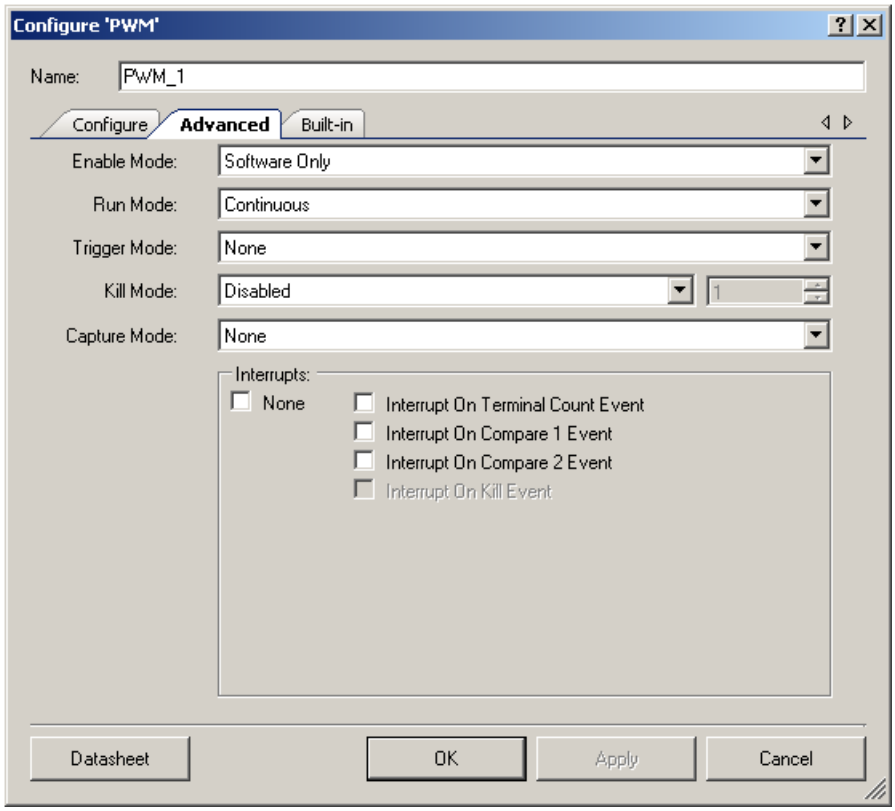
Dead Time (Software)

The dead time value defines the amount of dead time implemented in the dead band output signals ph1 and ph2. This parameter is only valid when **Dead Band** is enabled and is limited based on the hardware configuration option defined in the **Dead Band** parameter.



Dead time is only software configurable when the dead band is enabled with a 2-256 range. This data is controlled with the PWM_WriteDeadTime(n) and the n = PWM_ReadDeadTime() API calls. These APIs correspond with the Dead Band setting (in the customizer) of "n-1". When dead band is enabled with the 2-4 range, the value set in the configuration is built into the hardware and cannot be set using an API.

Advanced Tab (Default Configuration)



Enable Mode

The **Enable Mode** parameter defines what hardware and software combination is required to enable the overall functionality of the PWM. Options include:

- **Software Only** – The PWM is only enabled when the enable bit in the control register is set by software. The enable input is not visible when the enable mode is set to **Software Only**.
- **Hardware Only** – The PWM is only enabled while the hardware enable input is active (high). In this mode, the PWM_Start() API must be called for proper initialization of the component, to avoid unexpected behavior.
- **Hardware And Software –** The PWM is enabled while both the bit in the control register and the hardware input are active (high).

Run Mode

The **Run Mode** parameter defines how the PWM is triggered to start and continue running. The PWM runs depending on the enable inputs, as described by the following enumerated values.

- **Continuous** – The PWM runs forever on a trigger event.

- **One Shot with Single Trigger** – The PWM runs once on a trigger event
- **One Shot with Multi Trigger** – The PWM runs once on a trigger event. Upon completion of each period the PWM halts until the next trigger event occurs. The PWM cannot be triggered with an API call.

Trigger Mode

The **Trigger Mode** parameter defines what hardware event constitutes a valid trigger event. The PWM cannot be triggered with an API call. The trigger input is not visible when **Trigger Mode** is set to **None**. Options include:

- **None** – No trigger is enabled (trigger is treated as always true)
- **Rising Edge** – A trigger event is signaled on a rising edge of the trigger input.
- **Falling Edge** – A trigger event is signaled on the falling edge of the trigger input.
- **Either Edge** – A trigger event is signal on either a rising edge or a falling edge of the trigger input.

Kill Mode

The **Kill Mode** parameter defines how the hardware handles the pwm outputs when the hardware kill input is active. The kill input is not visible when the kill mode is set to **Disabled**. Options include:

- **Disabled** – No kill is enabled
- **Asynchronous** – The pwm outputs are disabled while kill is active. The pwm outputs are synchronous, so outputs will be disabled when a raising edge of clock has occurred.
- **Single Cycle** – The pwm outputs are disabled while kill is active and are not re-enabled until the end of the period has been reached (that is, tc).
- **Latched** – The pwm outputs are disabled on kill and remain disabled until the PWM is reset.
- **Minimum Time** – The pwm outputs are disabled while kill is active and are not re-enabled until the minimum time has elapsed. The pulse width of kill signal should be less than minimum Kill time.

Minimum Kill Time (Software)

The minimum kill time parameter defines the minimum length of the kill signal to be applied to the pwm outputs (minimum of the necessary kill signal duration in clock cycles) when the **Kill Mode** parameter is set to **Minimum Time**.



The minimum kill time value is defined in the number of clock counts limited to 1 to 255 and it is controlled with the PWM_WriteKillTime() and PWM_ReadKillTime() API calls.

Capture Mode

The **Capture Mode** parameter defines what hardware event will cause a capture of the period counter value to the read FIFO. It is always possible to read the current counter value (that is, a software capture) by calling the PWM_ReadCounter() API. The capture input is not visible when the capture mode is set to **None**. Options include:

- **None** – No capture is enabled
- **Rising Edge** – A capture event is signaled on a rising edge of the capture input.
- **Falling Edge** – A capture event is signaled on the falling edge of the capture input.
- **Either Edge** – A capture event is signaled on either a rising edge or a falling edge of the capture input.

Interrupts

The **Interrupts** parameters allow you to configure the initial interrupt sources. These values are ORed with any of the other interrupt parameters to give a final group of events that can trigger an interrupt. The software can reconfigure this mode at any time, as long as **Interrupts** is not set to **None**. This parameter defines an initial configuration.

- **None** – No interrupts are set.
- **Interrupt On Terminal Count Event** – This option is always available; it is deselected by default.
- **Interrupt On Compare 1 Event** – This option is deselected by default. It is always shown. See the difference in Interrupt generation (one clock cycle) for a compare event between UDB and FF implementation in the Enable / Reset Signals in UDB Implementation and Reset Signal in Fixed Function Implementation sections.

- **Interrupt On Compare 2 Event** – This option is deselected by default. It is only available when **UDB** is selected for **Implementation** and **PWM Mode** is set appropriately.
- **Interrupt On Kill Event** – This option is deselected by default. It is only available when **UDB** is selected for **Implementation** and **PWM Mode** is set appropriately.

Local Parameters (For API usage)

These parameters are used in the APIs and not exposed in the GUI.

- **FixedFunctionUsed** – Defined as a '1' (true) if you have chosen to implement the PWM using the fixed-function block.
- **KillModeMinTime** – Defined as a '1' (true) if you have set the **Kill Mode** as **Minimum Time**. This allows PWM_WriteKillTIme() and PWM_ReadKillTime() functions to be included as necessary.
- **PWMModeCenterAligned** – Defined as '1' (true) if you have set the **PWM Mode** as **Center Aligned.** The PWM_ReadCompare() and PWM_WriteCompare() functions are defined differently for this mode than other modes. This parameter is used to add the correct functions and remove the unnecessary functions.
- **DeadBandUsed** – Defined as '1' (true) if you have chosen to implement dead band with the 2-256 enable mode. This is used to conditionally include PWM_WriteDeadTime() and PWM_ReadDeadTime() API functions.
- **DeadBand2_4** – Defined as '1' (true) if you have chosen to implement dead band with the 2-4 counts range. This is used inside of the PWM_WriteDeadTime() and PWM_ReadDeadTime() functions for the different operations that must happen to handle the DeadTime.
- **UseStatus –** Defined as '1' (true) when the configuration warrants the use of a status register. This allows the status register resource to be removed if it is not necessary in the design.
- **UseControl** – Defined as '1' (true) when the configuration warrants the use of a control register. This allows the control register resource to be removed if it is not necessary in the design.
- **UseOneCompareMode** – Defined as '1' (true) when the configuration requires only a single compare mode API to be available. This allows the API to be removed, as defined by the architecture chosen.

Clock Selection

There is no internal clock in this component. You must attach a clock source.

WARNING When configured to use the fixed-function block in the device, the PWM component has the following restrictions:

- The clock input must be from a local clock that is synchronized to the bus clock or directly sourced from the bus clock (configure the clock type as Existing and the source as BUS_CLK).
- If the frequency of the clock matches the bus clock, then the clock must be a direct connection to the bus clock (again configure the clock type as Existing and the source as BUS_CLK). A local clock with a frequency that matches the bus clock generates an error during the build process.

For UDB-Based Components

If the component allows asynchronous clocks, you may use any clock input frequency within the device's frequency range.

If the component requires synchronization to the bus clock, then when using a routed clock [1] to clock the component, the frequency of the routed clock cannot exceed one half the routed clock’s source clock frequency.

- If the routed clock is synchronous to the bus clock, then it is one half the bus clock.
- If the routed clock is synchronous to one of the clock dividers, its maximum is one half of that clock rate.

1 A routed clock is anything that is not a clock symbol directly attached to the clock input.

Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software. The following table lists and describes the interface to each function. The subsequent sections cover each function in more detail.

By default, PSoC Creator assigns the instance name “PWM_1” to the first instance of a component in a given design. You can the rename the instance to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is “PWM.”

Functions

Function	Description
PWM_Start()	Initializes the PWM with default customizer values.
PWM_Stop()	Disables the PWM operation. Clears the enable bit of the control register for either of the software controlled enable modes.
PWM_SetInterruptMode()	Configures the interrupts mask control of the interrupt source status register.
PWM_ReadStatusRegister()	Returns the current state of the status register.
PWM_ReadControlRegister()	Returns the current state of the control register.
PWM_WriteControlRegister()	Sets the bit field of the control register.
PWM_SetCompareMode()	Writes the compare mode for compare output when **PWM Mode** is set to Dither mode, Center Align mode or One Output mode.
PWM_SetCompareMode1()	Writes the compare mode for compare1 output into the control register.
PWM_SetCompareMode2()	Writes the compare mode for compare2 output into the control register.
PWM_ReadCounter()	Reads the current counter value (software capture).
PWM_ReadCapture()	Reads the capture value from the capture FIFO.
PWM_WriteCounter()	Writes a new counter value directly to the counter register. This will be implemented only for that currently running period.
PWM_WritePeriod()	Writes the period value used by the PWM hardware.
PWM_ReadPeriod()	Reads the period value used by the PWM hardware.
PWM_WriteCompare()	Writes the compare value when the instance is defined as Dither mode, Center Align mode or One Output mode.
PWM_ReadCompare()	Reads the compare value when the instance is defined as Dither mode, Center Align mode or One Output mode.
PWM_WriteCompare1()	Writes the compare value for the compare1 output.
PWM_ReadCompare1()	Reads the compare value for the compare1 output.
PWM_WriteCompare2()	Writes the compare value for the compare2 output

Function	Description
PWM_ReadCompare2()	Reads the compare value for the compare2 output.
PWM_WriteDeadTime()	Writes the dead time value used by the hardware in dead band implementation.
PWM_ReadDeadTime()	Reads the dead time value used by the hardware in dead band implementation.
PWM_WriteKillTime()	Writes the kill time value used by the hardware when the kill mode is set as Minimum Time.
PWM_ReadKillTime()	Reads the kill time value used by the hardware when the kill mode is set as Minimum Time.
PWM_ClearFIFO()	Clears all capture data from the capture FIFO.
PWM_Sleep()	Stops and saves the user configuration.
PWM_Wakeup()	Restores and enables the user configuration.
PWM_Init()	Initializes component's parameters to those set in the customizer placed on the schematic.
PWM_Enable()	Enables the PWM block operation.
PWM_SaveConfig()	Saves the current user configuration of the component.
PWM_RestoreConfig()	Restores the current user configuration of the component.

void PWM_Start(void)

Description: This function intended to start component operation. PWM_Start() sets the initVar variable, calls the PWM_Init function, and then calls the PWM_Enable function.

Parameters: None

Return Value: None

Side Effects: Sets the enable bit in the control registers of the PWM. If the **Enable Mode** is set to **Hardware Only**, this has no effect on the PWM. If the **Enable Mode** is set to **Hardware and Software**, then this will only enable the software portion of this mode and the hardware input must also be enabled to finally enable the PWM.

void PWM_Stop(void)

Description: Disables the PWM operation by resetting the seventh bit of the control register for either of the software-controlled enable modes. Disables the fixed-function block that has been chosen.

Parameters: None

Return Value: None

Side Effects: Clears the enable bit in the control register of the PWM. If the **Enable Mode** is set to **Hardware Only**, this function has no effect on the PWM. If the **Enable Mode** is set to **Hardware and Software**, this function will disable the software portion of this mode and the hardware input will have no further effect on the enable of the PWM.

For FF implementation, if the component is stopped, the “pwm” output retains the state of the previous value and the “ph1” output will be driven to 0.

For UDB implementation, if the component is stopped, the “pwm” output (“pwm1”, ”pwm2”) will be driven to 0.

void PWM_SetInterruptMode(uint8 interruptMode)

Description: Configures the interrupts mask control of the interrupt source status register.

Parameters: uint8 interruptMode: Bit mask containing the interrupt sources enabled

Available interrupt sources for the fixed-function implementation:

Bit	Define	Description
[3]	PWM_STATUS_TC_INT_EN_MASK	Enables interrupt that triggered on terminal count event.
[2]	PWM_STATUS_CMP1_INT_EN_MASK	Enables interrupt that triggered on compare event on PWM channel. Intended to use in dual-channel mode only.

Available interrupt sources for the UDB implementation:

Bit	Define	Description
[5]	PWM_STATUS_KILL_INT_EN_MASK	Enables interrupt that triggered on active kill signal.
[4]	PWM_STATUS_FIFONEMPTY_INT_EN_MASK	This bit is not used.
[3]	PWM_STATUS_FIFOFULL_INT_EN_MASK	Enables interrupt that triggered if FIFO is full.
[2]	PWM_STATUS_TC_INT_EN_MASK	Enables interrupt that triggered on terminal count event.
[1]	PWM_STATUS_CMP2_INT_EN_MASK	Enables interrupt that triggered on compare event on PWM2 channel. Intended to use in dual-channel mode only.
[0]	PWM_STATUS_CMP1_INT_EN_MASK	Enables interrupt that triggered on compare event on PWM1 channel. Intended to use in dual-channel mode only.

Return Value: None

Side Effects: None

uint8 PWM_ReadStatusRegister(void)

Description: Returns the current state of the status register.

Parameters: None

Return Value: uint8: Current status register value.

Available statuses for the fixed-function implementation.

Bit	Mask	Description
[7]	PWM_STATUS_TC	Set to 1 on terminal count event. This bit clears on read.
[6]	PWM_STATUS_CMP1	Set to 1 on compare event on PWM channel. This bit clears on read.

Available statuses for the UDB implementation.

Bit	Mask	Description
[5]	PWM_STATUS_KILL	Set to 1 when kill signal is active. This bit clears on read.
[4]	PWM_STATUS_FIFONEMPTY	This bit is not used.
[3]	PWM_STATUS_FIFOFULL	Set to 1 if capture FIFO is full.
[2]	PWM_STATUS_TC	Set to 1 on terminal count event. This bit clears on read.
[1]	PWM_STATUS_CMP2	Set to 1 on compare event on PWM2 channel. Intended to use in dual-channel mode only. This bit clears on read.
[0]	PWM_STATUS_CMP1	Set to 1 on compare event on PWM channel for one-channel mode and on PWM1 channel for dual-channel mode. This bit clears on read.

Side Effects: None

uint8 PWM_ReadControlRegister(void)

Description: Returns the current state of the control register. This API is available only if the enable mode is not “Hardware Only” or compare mode is software controlled at least for one channel. See Control (FF) section for fixed function implementation.

Parameters: None

Return Value: uint8: Current control register value

UDB implementation

Bit	Mask	Description
[7]	PWM_CTRL_ENABLE	Reads enable state of the PWM block.
[6]	PWM_CTRL_RESET	Reads reset state of the PWM block.
[5:3]	PWM_CTRL_CMPMODE2_MASK	Reads the compare mode configuration for compare2/compare1 modes from the control register. For compare mode defines, see the description for the PWM_SetCompareMode() function.
[2:0]	PWM_CTRL_CMPMODE1_MASK	

FF implementation

Bit	Mask	Description
[7:6]	PWM_DEADBAND_COUNT_MASK	Reads the Deadband Period of the PWM block.
[5]	PWM_CFG0_DB	Reads Deadband mode state of the PWM block.
[1]	PWM_CFG0_MODE	Reads enable state of the compare mode of the PWM block.
[0]	PWM_CTRL_ENABLE	Reads enable state of the PWM block.

Side Effects: None

void PWM_WriteControlRegister(uint8 control)

Description: Sets the bit field of the control register. This API is available only if the enable mode is not “Hardware Only” or compare mode is software controlled at least for one channel. See Control (FF) section for fixed function implementation.

Parameters: uint8 control: Control register bit mask.

UDB implementation

Bit	Mask	Description
[7]	PWM_CTRL_ENABLE	Setting this bit to 1 enables the PWM module.
[6]	PWM_CTRL_RESET	Setting this bit to 1 resets the PWM block.
[5:3]	PWM_CTRL_CMPMODE2_MASK	Writes the compare mode configuration for compare2/compare1 modes into the control register. For compare mode defines, see the description for the PWM_SetCompareMode() function.
[2:0]	PWM_CTRL_CMPMODE1_MASK	

FF implementation

Bit	Mask	Description
[7:6]	PWM_DEADBAND_COUNT_MASK	Writes Deadband Period from 0 to 3.
[5]	PWM_CFG0_DB	Setting this bit to 1 routes compare output to TC output port.
[1]	PWM_CFG0_MODE	Setting this bit to 1 enables compare mode of the PWM block.
[0]	PWM_CTRL_ENABLE	Setting this bit to 1 enables the PWM block.

Return Value: None

Side Effects: None

void PWM_SetCompareMode(enum comparemode)

Description: Writes the compare mode for compare output when **PWM Mode** is set to Dither mode, Center Align mode or One Output mode.

Parameters: enum comparemode: Compare mode enumerated type.

Mask	Description
PWM__B_PWM__LESS_THAN	Compare output is true if period counter is less than the corresponding compare value.
PWM__B_PWM__LESS_THAN_OR_EQUAL	Compare output is true if period counter is less than or equal to the corresponding compare value.
PWM__B_PWM__GREATER_THAN	Compare output is true if period counter is greater than the corresponding compare value.
PWM__B_PWM__GREATER_THAN_OR_EQUAL_TO	Compare output is true if period counter is greater than or equal to the corresponding compare value.
PWM__B_PWM__EQUAL	Compare output is true if period counter is equal to the corresponding compare value.

Return Value: None

Side Effects: None

void PWM_SetCompareMode1(enum comparemode)

Description: Writes the compare mode for compare1 output into the control register.

Parameters: enum comparemode: For compare mode defines, see the description for the PWM_SetCompareMode() function.

Return Value: None

Side Effects: None

void PWM_SetCompareMode2(enum comparemode)

Description: Writes the compare mode for compare2 output into the control register. This API is valid only for UDB implementation and not available for fixed function PWM implementation.

Parameters: enum comparemode: For compare mode defines, see the description for the PWM_SetCompareMode() function.

Return Value: None

Side Effects: None

uint8/16 PWM_ReadCounter(void)

Description: Reads the current counter value (software capture). This API is valid only for UDB implementation and not available for fixed function PWM implementation.

Parameters: None

Return Value: uint8/uint16: The current period counter value

Side Effects: None

uint8/16 PWM_ReadCapture(void)

Description: Reads the capture value from the capture FIFO. This API is valid only for UDB implementation and not available for fixed function PWM implementation.

Parameters: None

Return Value: uint8/uint16: The current capture value

Side Effects: None

Note FIFOs are cleared after going into low-power mode. You must read any data from the capture FIFO before going into low-power mode, if required.

void PWM_WriteCounter(uint8/16 counter)

Description: Writes a new counter value directly to the counter register. This will be implemented for that currently running period and only that period. This API is valid only for UDB implementation and not available for fixed function PWM implementation.

Parameters: uint8/uint16 counter: The new period counter value

Return Value: None

Side Effects: If API is called with counter parameter equal to zero, the PWM counter value will be reloaded with period value.

void PWM_WritePeriod(uint8/16 period)

Description: Writes the period value used by the PWM hardware.

Parameters: period: uint8 or 16 depending on resolution, the new period value

Return Value: None

Side Effects: None

uint8/16 PWM_ReadPeriod(void)

Description: Reads the period value used by the PWM hardware.

Parameters: None

Return Value: uint8/16: Period value

Side Effects: None

void PWM_WriteCompare(uint8/16 compare)

Description: Writes the compare values for the compare output when the **PWM Mode** parameter is set to **Dither** mode, **Center Aligned** mode, or **One Output** mode.

Parameters: uint8/16: Compare value

Return Value: None

Side Effects: Using the PWM_WriteCompare() API when the PWM is running will cause the comparison to use the new compare value immediately and that result will propagate to the output terminal on the next clock. A change in the PWM output also triggers deadband logic if Deadband Mode is enabled.

uint8/16 PWM_ReadCompare(void)

Description: Reads the compare value for the compare output when the **PWM Mode** parameter is set to **Dither** mode, **Center Aligned** mode, or **One Output** mode.

Parameters: None

Return Value: uint8/uint16: Current compare value

Side Effects: This function is only available if the **PWM Mode** parameter is set to one of the modes described above. Otherwise the ReadCompare1/2 functions must be called.

void PWM_WriteCompare1(uint8/16 compare)

Description: Writes the compare value for the compare1 output.

Parameters: uint8/uint16: New compare value for pwm1

Return Value: None

Side Effects: Using the PWM_WriteCompare1() API when the PWM is running will cause the comparison to use the new compare value immediately and that result will propagate to the output terminal on the next clock. A change in the PWM output also triggers deadband logic if Deadband Mode is enabled.

uint8/16 PWM_ReadCompare1(void)

Description: Reads the compare value for the compare1 output.

Parameters: None

Return Value: uint8/uint16: Current compare value 1

Side Effects: None

void PWM_WriteCompare2(uint8/16 compare)

Description: Writes the compare value for the compare2 output. This API is valid only for UDB implementation and not available for fixed function PWM implementation.

Parameters: uint8/uint16: New compare value for pwm2

Return Value: None

Side Effects: Using the PWM_WriteCompare2() API when the PWM is running will cause the comparison to use the new compare value immediately and that result will propagate to the output terminal on the next clock. A change in the PWM output also triggers deadband logic if Deadband Mode is enabled.

uint8/16 PWM_ReadCompare2(void)

Description: Reads the compare value for the compare2 output. This API is valid only for UDB implementation and not available for fixed function PWM implementation.

Parameters: None

Return Value: uint8/uint16: The current compare value

Side Effects: None

void PWM_WriteDeadTime(uint8 deadband)

Description: Writes the dead time value used by the hardware in dead band implementation.

Parameters: uint8: Dead Band counts - 1

Return Value: None

Side Effects: None

uint8 PWM_ReadDeadTime(void)

Description: Reads the dead time value used by the hardware in dead band implementation.

Parameters: None

Return Value: uint8: The current setting of Dead Band counts - 1

Side Effects: None

void PWM_WriteKillTime(uint8 killtime)

Description: Writes the kill time value used by the hardware when the **Kill Mode** is set to **Minimum Time**. This API is valid only for UDB implementation and not available for fixed function PWM implementation.

Parameters: uint8: Minimum Time kill counts

Return Value: None

Side Effects: None

uint8 PWM_ReadKillTime(void)

Description: Reads the kill time value used by the hardware when the **Kill Mode** is set to **Minimum Time**. This API is valid only for UDB implementation and not available for fixed function PWM implementation.

Parameters: None

Return Value: uint8: The current Minimum Time kill counts

Side Effects: None

void PWM_ClearFIFO(void)

Description: Clears the capture FIFO of any previously captured data. Here PWM_ReadCapture() is called until the FIFO is empty. This API is valid only for UDB implementation and not available for fixed function PWM implementation.

Parameters: None

Return Value: None

Side Effects: None

void PWM_Sleep(void)

Description: Stops and saves the user configuration.

Parameters: None

Return Value: None

Side Effects: None

void PWM_Wakeup(void)

Description: Restores and enables the user configuration.

Parameters: None

Return Value: None

Side Effects: None

void PWM_Init(void)

Description: Initializes component's parameters to those set in the customizer placed on the schematic. The compare modes are set by setting the respective bits of the control register. The interrupts are chosen as the output from the status register. If you are using fixed-function mode, the chosen fixed-function block is enabled. FIFO is cleared to enable FIFO full bit to be set in the status register. Usually called in PWM_Start().

Parameters: None

Return Value: None

Side Effects: All registers will be reset to their initial values. This reinitializes the component

void PWM_Enable(void)

Description: Enables the PWM block operation by setting the seventh bit of the control register. The outputs and component behavior will reflect component enable state after two clock cycles.

Parameters: None

Return Value: None

Side Effects: None

void PWM_SaveConfig(void)

Description: Saves the current user configuration of the component. The period, dead band, counter, and control register values are saved.

Parameters: None

Return Value: None

Side Effects: None

void PWM_RestoreConfig(void)

Description: Restores the current user configuration of the component.

Parameters: None

Return Value: None

Side Effects: None

Global Variables

Variable	Description
PWM_initVar	Indicates whether the PWM has been initialized. The variable is initialized to 0 and set to 1 the first time PWM_Start() is called. This allows the component to restart without reinitialization after the first call to the PWM_Start() routine. If reinitialization of the component is required, then the PWM_Init() function can be called before the PWM_Start() or PWM_Enable() function.

Sample Firmware Source Code

PSoC Creator provides many example projects that include schematics and example code in the Find Example Project dialog. For component-specific examples, open the dialog from the Component Catalog or an instance of the component in a schematic. For general examples, open the dialog from the Start Page or **File** menu. As needed, use the **Filter Options** in the dialog to narrow the list of projects available to select.

Refer to the “Find Example Project” topic in the PSoC Creator Help for more information.

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined:

- project deviations – deviations that are applicable for all PSoC Creator components
- specific deviations – deviations that are applicable only for this component

This section provides information on component-specific deviations. Project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment.

The PWM component does not have any specific deviations.

API Memory Usage

The component memory usage varies significantly, depending on the compiler, device, number of APIs used and component configuration. The following table provides the memory usage for all APIs available in the given component configuration.

The measurements have been done with the associated compiler configured in Release mode with optimization set for Size. For a specific design the map file generated by the compiler can be analyzed to determine the memory usage.

Configuration	PSoC 3 (Keil_PK51)		PSoC 4 (GCC)		PSoC 5LP (GCC)	
	Flash (Bytes)	RAM (Bytes)	Flash (Bytes)	RAM (Bytes)	Flash (Bytes)	RAM (Bytes)
8-bit One Output Mode[2]	279	6	456	9	464	9
8-bit Two Outputs Mode[2] (FW Control, Minimum Time for kill)	362	7	580	7	580	7
8-bit Dual Edged Mode[2]	284	6	452	6	448	6
8-bit Center Align Mode[2]	263	5	452	5	456	5
8-bit HW Select Mode[2]	284	6	484	9	492	9
8-bit Dither Mode[2]	284	6	488	6	476	6
16-bit One Output Mode[2]	342	8	480	9	480	9
8-bit with Dead Band 2-4[3]	325	7	520	7	536	7
16-bit with Dead Band 2-4[3]	388	9	536	11	552	11
8-bit with Dead Band 2-256[3]	312	7	508	7	512	7
16-bit with Dead Band 2-256[3]	375	9	524	11	528	11
8 Bits Fixed Function	243	2	-	-	356	2

2 Configuration 1: The PWM in the corresponding PWM mode and resolution is configured with Software Only Enable mode, Continuous Run Mode, Trigger mode set to None, Kill mode and Capture mode disabled with no dead band and Interrupt on TC.

3 Configuration 2: 2-4 Dead Band range and 2-256 Dead Band range are mutually exclusive. The PWM is configured for the corresponding resolution and One Output PWM mode with Software Only Enable mode, Trigger mode set to None, Kill mode and Capture mode disabled with Interrupt on TC.

Configuration	PSoC 3 (Keil_PK51)		PSoC 4 (GCC)		PSoC 5LP (GCC)	
	Flash (Bytes)	RAM (Bytes)	Flash (Bytes)	RAM (Bytes)	Flash (Bytes)	RAM (Bytes)
16 Bits Fixed Function	247	2	-	-	356	2

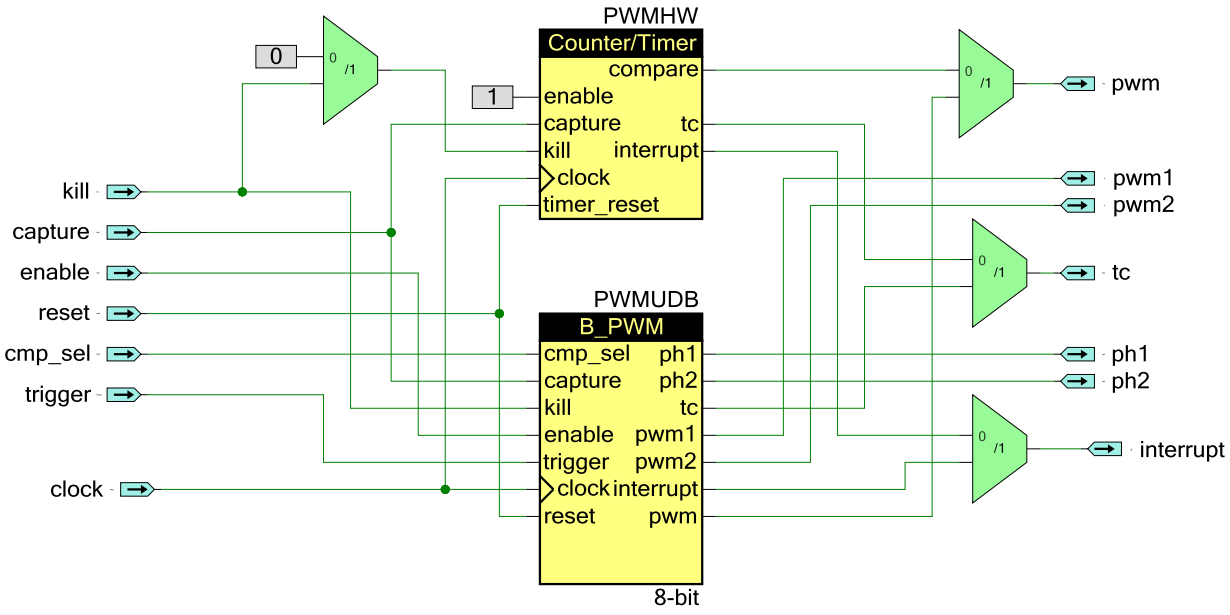
Functional Description

Block Diagram and Configuration

The PWM can be implemented using a fixed-function block or using UDB components. The **Implementation** parameter allows you to specify the block in which you expect to place this component. The fixed-function implementation consumes one of the Timer/Counter/PWM blocks. In both the fixed-function or UDB configurations, all of the registers and APIs are consolidated to give a single entity look and feel. The API is described earlier and the registers are described here to define the overall implementation of the PWM.

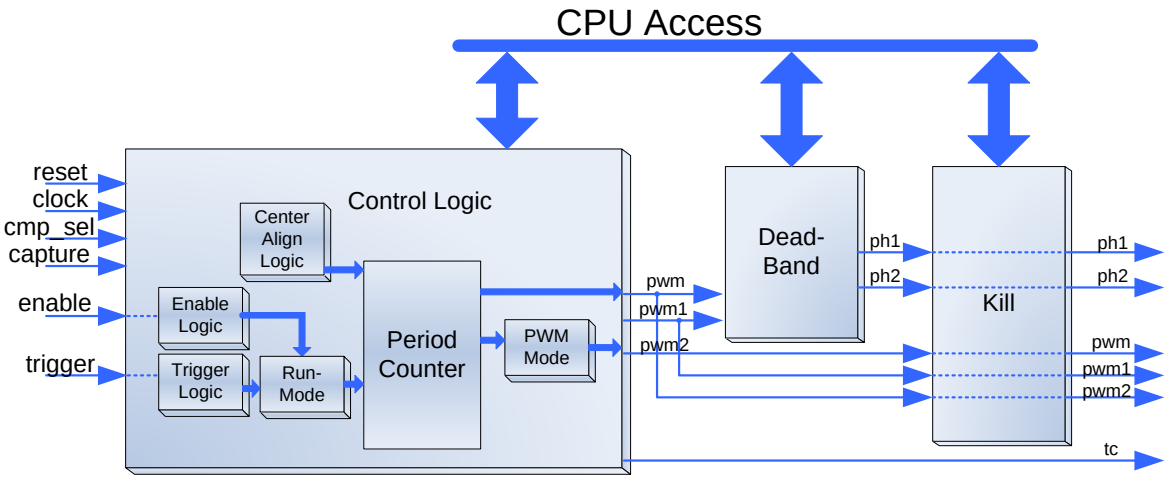
The two hardware implementations you chose are selected from a top-level schematic as shown in Figure 1.

Figure 1. Top-Level Schematic



This configuration allows you to select either the fixed-function block or the UDB implementation. The routing of the I/Os is handled in the background to give this single component look and feel. The UDB implementation is described in Figure 2.

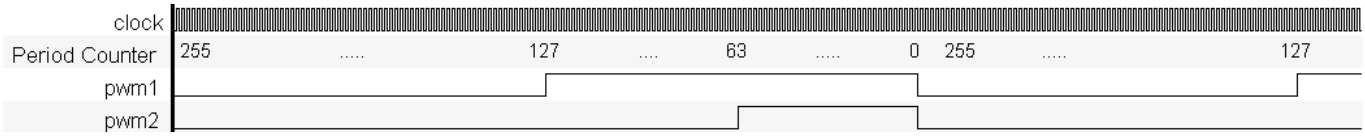
Figure 2. UDB Implementation



Default Configuration

The default configuration for the PWM is as a two-output 8-bit PWM that creates one output with a compare of less than 127 (with a period of 255) and a second output of less than 63. Figure 3 shows the inputs and outputs of the PWM when it is left in the default configuration.

Figure 3. PWM Inputs and Outputs



Fixed-Function Block Limitations

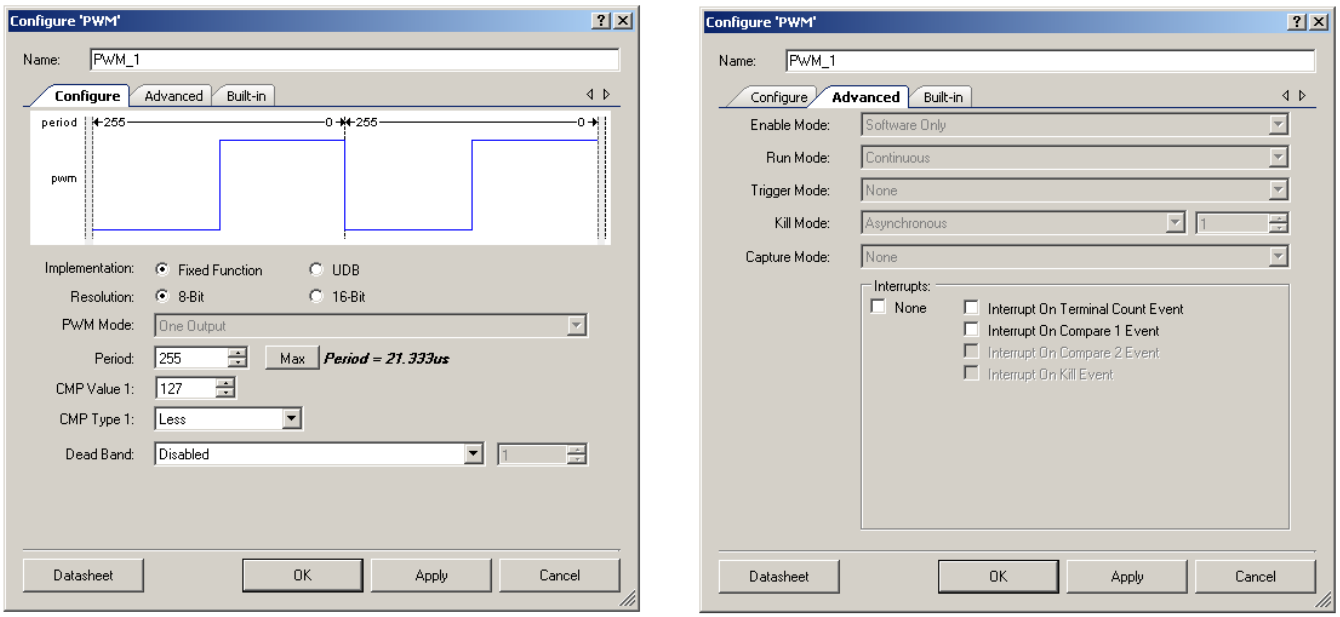
The fixed-function implementation of the PWM provides for less UDB resource use by implementing a PWM with reduced functionality in a configurable hardware block. The functionality of the PWM within one of these blocks has the following limitations:

- No counter value access – PWM_ReadCapture() and PWM_ReadCounter() are not available.
- One output mode only – No Center Align, Dual Edge, Dither, or Two Outputs modes
- Asynchronous kill mode only
- No trigger
- Continuous run mode only

- Software enable only – No Hardware enable mode
- Reduced dead band functionality – Limited to 0 to 3 counts of dead band
- Reduced I/O when dead band is enabled – TC and PWM become PH2 and PH1, respectively.

When you choose the **Fixed Function** implementation, the **Configure** tab and the **Advanced** tab indicate these limitations by setting the parameter fields and disabling the options, as shown in Figure 4.

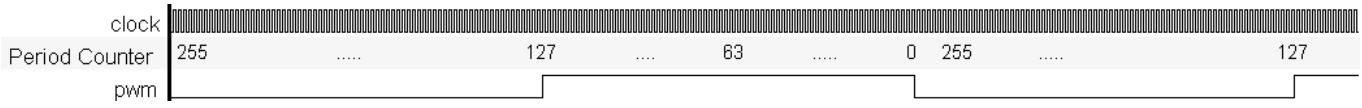
Figure 4. Fixed Function Settings



PWM Mode

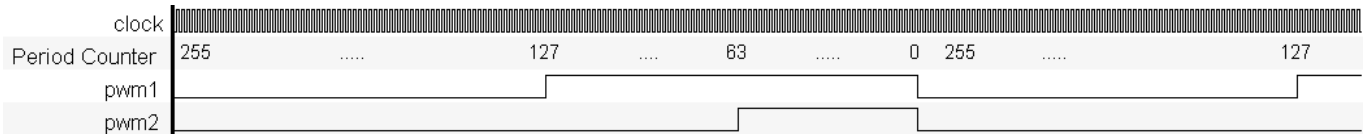
One Output

A one-output PWM has only one output that is controlled by a single compare value and a single compare mode. This waveform can be left-aligned with a compare mode of **Greater** or **Greater or Equal** or it can be right-aligned with a compare mode of **Less** or **Less or Equal**.



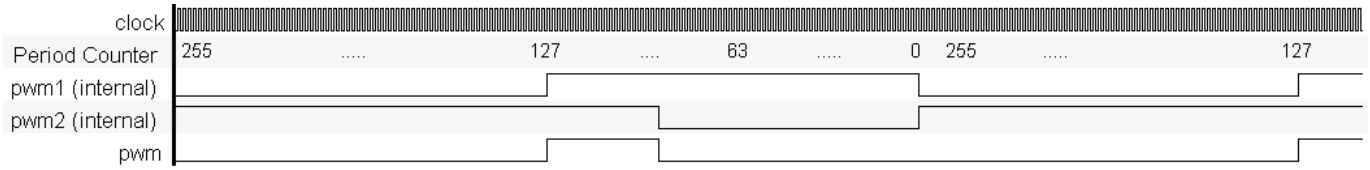
Two Outputs

The two-output PWM is the default configuration. The two PWM outputs are defined independently of each other using two compare values and two compare modes. Each of these two outputs can be left aligned or right aligned, as described previously in One Output mode.



Dual Edge

A dual-edge PWM uses the two compare outputs and two compare modes to generate a single PWM output. The final output is an ANDing of the two different signals defined by the two compare values and compare modes. This mode requires you to have some understanding of what the different modes will generate. The waveform examples in the parameter editing customizer provide help as to what the final waveform will look like. However, the compare values, compare modes, and period values can all be set at run time. Changing these values without understanding the final configuration can easily create a 0 value output.



Center Aligned

A center-aligned PWM implements the PWM differently from all of the other modes. The desired output requires that the period counter start at zero and count up to the period value, and when the period value is reached the counter starts counting back down to zero. In this mode, the period value is actually half of the period of the final output. A single compare value and compare mode are available for this functionality.

All other modes of the PWM start the period counter at the period setting counting down to 0 and reloading to the period value which makes them period+1 for the actual period time. This is represented in the calculated period displayed in the customizer. For center-aligned mode the calculated period is NOT period+1. This is because the period counter counts from 0 to period+1 and immediately starts counting back down. For example, with a period of 4 the counter will count, 0,1,2,3,4,5,4,3,2,1,0,1,2… making the period 10 clock cycles.

Hardware Select

A hardware-select PWM is implemented as a two-output PWM, where the implementation has two independent compare values and compare modes. A hardware input cmp_sel selects which of the two inputs is the final PWM output. This allows you to switch between two preconfigured values as necessary, without modifying the parameters.

Dither

A dither-mode PWM is implemented as a hardware-select-mode PWM with the caveat that the first and compare values have a difference of 1 and both compare modes are identical. There is also a built-in state machine controlling the hardware select. In this mode, the cmp_sel input is not available. You can set the offset as 0.00, 0.25, 0.50, and 0.75, with the parameter field visible in this mode. If the offset is configured as 0.00, then the output is always the compare1 output. When set to 0.25 the output is compare1 for three cycles and compare1 + 1 for a single cycle.

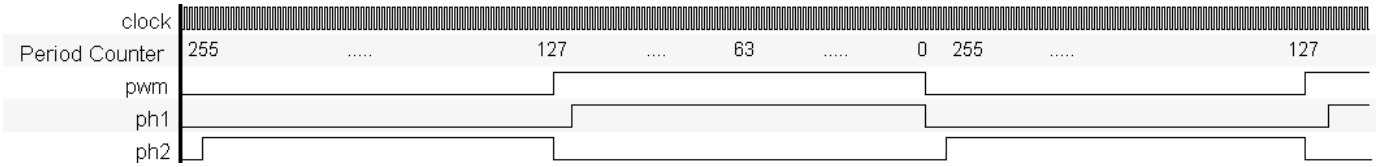
Dither Mode	Cycle 0	Cycle 1	Cycle 2	Cycle 3
0.00	Compare1	Compare1	Compare1	Compare1
0.25	Compare1 + 1	Compare1	Compare1	Compare1
0.50	Compare1	Compare1 + 1	Compare1	Compare1 + 1
0.75	Compare1 + 1	Compare1 + 1	Compare1 + 1	Compare 1

Dead Band

Dead band is an add-on option to any of the PWM modes just described. When dead band is enabled, two new outputs (UDB implementation), ph1 and ph2 (PWM and TC, respectively, for FF implementation), become visible on the symbol. The dead band outputs work on a single PWM output. In all modes except two-output mode, the dead band outputs are related to the single PWM output. In two-output mode, the dead band is only implemented on the pwm1 output. In all dead band modes, the original output is available, along with the ph1 and ph2 outputs.

FF implementation: Dead band can be configured as having a range of 0 to 3 clock cycles for dead band time.

UDB implementation: Dead band can be configured as having a range of 2 to 4 or 2 to 256 clock cycles for dead band time. The 2 to 4 cycle range is provided to reduce resource usage by implementing the counter in PLDs instead of using a full datapath. When the 2 to 256 range dead band is selected, a full datapath and the necessary logic are used from the UDB array.



Kill Mode

Like dead band, kill mode is an add-on function that does not interrupt the implementation of the PWM internally. This add-on is placed at the outputs of the PWM and manipulates only the final output signals. When dead band is not implemented, the kill operation disables the PWM outputs by pulling them low. If dead band is implemented, the kill operation disables the ph1 and ph2 outputs by pulling them low.

Asynchronous

In asynchronous kill mode, the outputs are disabled while the kill input is active (high) and the outputs are re-enabled as soon as the kill input goes inactive.

Single Cycle

In single cycle kill mode, the outputs are disabled while the kill input is active (high) and the outputs are re-enabled at the beginning of the next period.

Latched

In latched kill mode, the outputs are disabled when the kill input goes high. After the PWM has been reset, if the kill input is not still active, the PWM outputs are re-enabled; otherwise, they remain in the kill state until the next reset of the PWM with an inactive kill input.

Minimum Time

In minimum-time kill mode, the outputs are disabled while the kill input is active (high). The outputs are re-enabled after the minimum time has elapsed, if the kill input is no longer active. For this mode, you define the minimum kill time in the number of clock counts 1 to 255. The API necessary for controlling the minimum kill time counts is only available if this kill mode is selected.

Run Mode

Continuous

Continuous run mode is the default configuration of the PWM. This mode allows the PWM to run forever while enabled. As long as the PWM is enabled, the output cycles through period after period implementing the specified pulse width output.

One Shot Single

One Shot Single run mode runs the PWM for a single period on a valid trigger event. After the period has completed the PWM halts. The PWM halts after reloading the counter with the value from the period register. The “pwm”, “pwm1” and “pwm2” (if visible) will be driven to ‘0’. A hardware reset pulse will re-arm the PWM and allow the next trigger event to cause the PWM to run another period. See examples in the PWM Component as a Pulse Generator section.

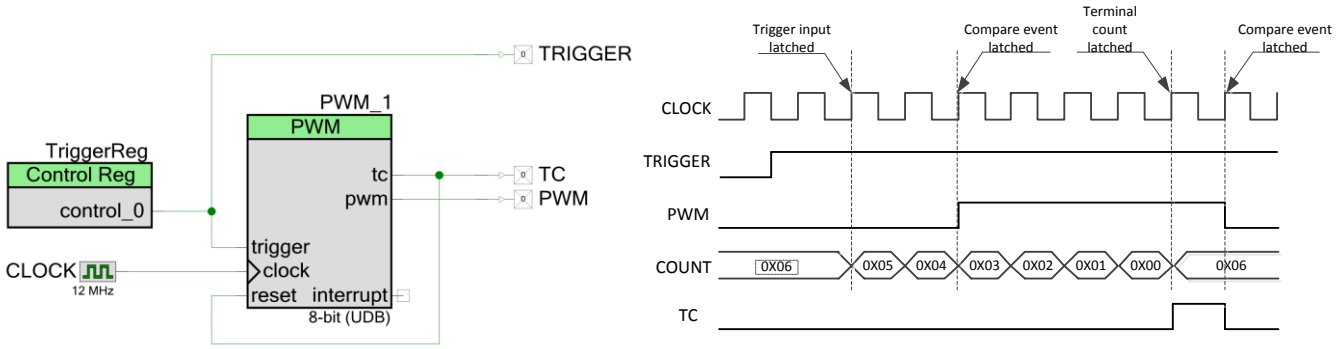
One Shot Multi

One Shot Multi run mode runs the PWM for a single period on a valid trigger event. After the period has completed the PWM halts and re-arms waiting for the next trigger event. The PWM halts after reloading the counter with the value from the period register. The “pwm”, “pwm1” and “pwm2” (if visible) will be driven to ‘0’. The difference between One Shot Single and One Shot Multi run modes is that One Shot Multi is re-armed without requiring a reset.

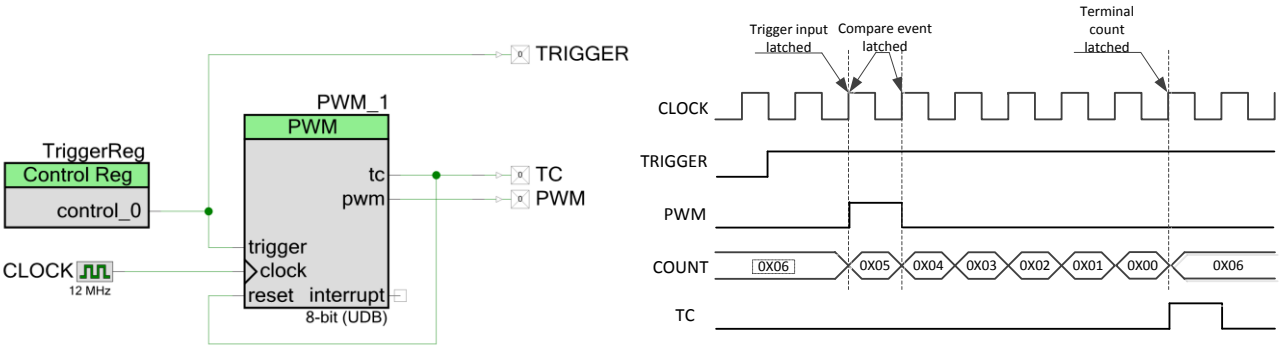
PWM Component as a Pulse Generator

A PWM component can be used to design a software-triggered pulse generator circuit to generate a timing pulse of a known period. The following timing diagrams describe examples of a pulse generation application that generates a timing pulse on a software trigger.

A PWM configured in One Shot Single mode can be used with a control register component to realize this design. In the One Shot Single mode, the PWM should be reset after it reaches the period value to make sure it functions correctly. You can do this by connecting the TC output to its reset input. The schematic features a UDB implementation of the PWM that creates such a circuit and timing diagram (Period = 6, CMP Value = 5, CMP Type = Less, Trigger mode = Rising Edge).

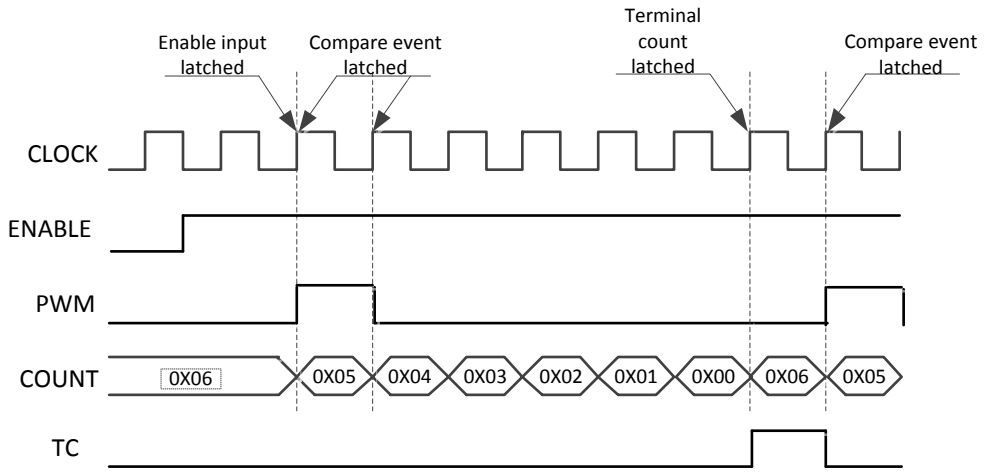


The schematic features a UDB implementation of the PWM that creates such a circuit and timing diagram (Period = 6, CMP Value = 5, CMP Type = Greater, Trigger mode = Rising Edge).

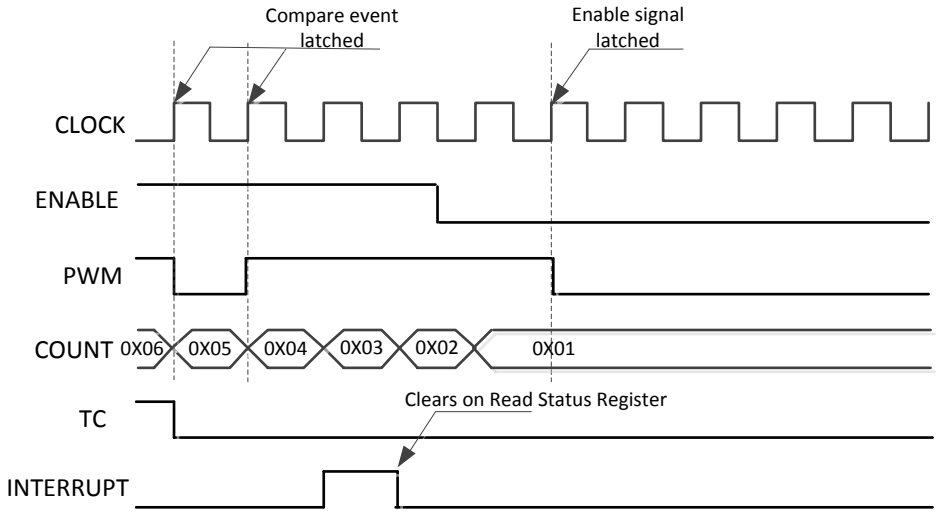


Enable / Reset Signals in UDB Implementation

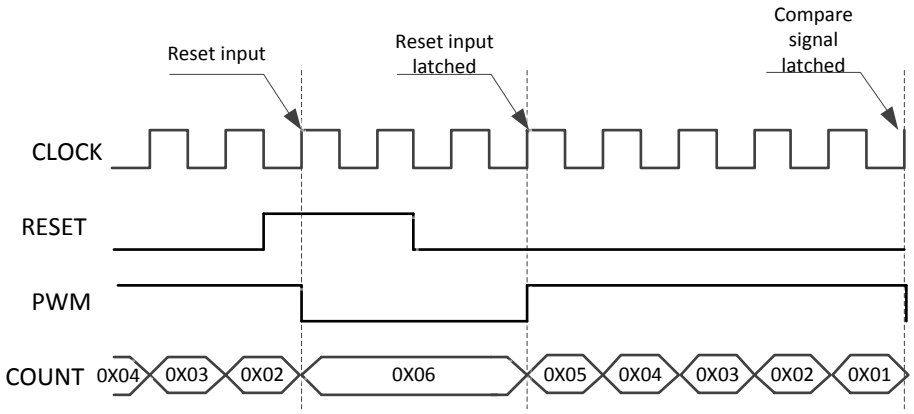
The following timing diagram shows the rising edge of the enable input signal using the PWM configuration: Period = 6, CMP Value = 5, CMP Type = Greater.



The following timing diagram shows the falling edge of the enable input signal using the PWM configuration: Period = 6, CMP Value = 5, CMP Type = Less or Equal, Interrupt On Compare 1 Event.

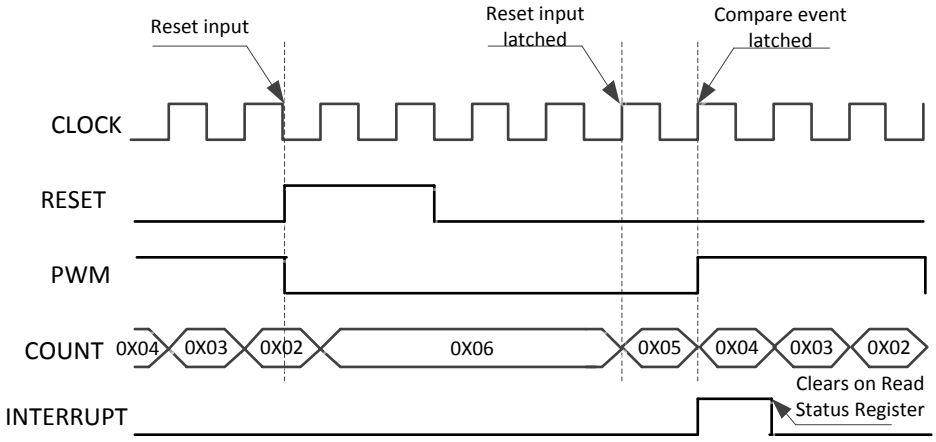


The following timing diagram shows the reset input signal using the PWM configuration: Period = 6, CMP Value = 2, CMP Type = Greater or Equal.



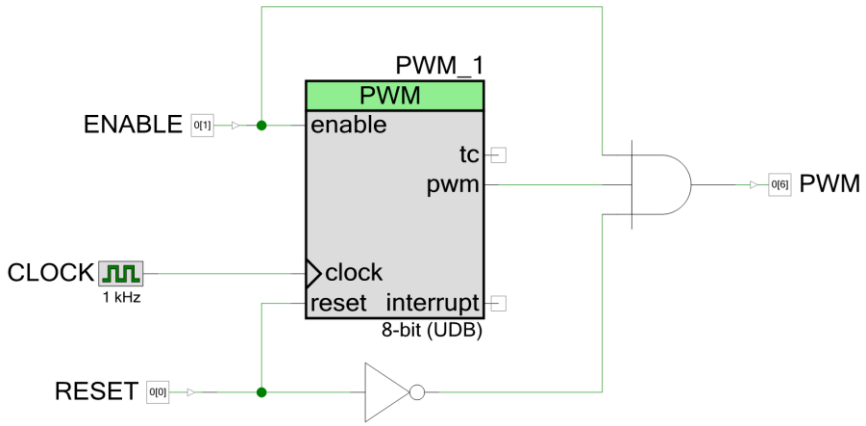
Reset Signal in Fixed Function Implementation

The following timing diagram shows the reset input signal using the PWM configuration: Period = 6, CMP Value = 5, CMP Type = Less or Equal,Interrupt On Compare 1 Event.



Immediate Reaction to Enable/Reset signals

If you need an immediate reaction to the Enable/Reset signals on the component outputs, use the following design as a reference:



It is recommended to use an additional trigger after the logic AND gate.

Registers

Status

The status register is a read-only register that contains the various status bits defined for the PWM. The PWM_ReadStatusRegister() function call gives you the value of this register. The interrupt output signal (interrupt) is generated from an ORing of the masked bit fields within this register. You can set the mask using the PWM_SetInterruptMode() function call and upon receiving an interrupt you can retrieve the interrupt source by reading the status register with the PWM_ReadStatusRegister() function call. The status register is a clear-on-read register so the interrupt source is held until the PWM_ReadStatusRegister() function is called. The PWM_ReadStatusRegister() API handles which interrupts are enabled to provide an accurate report of the actual source of the interrupt. All operations on the status register must use the following defines for the bit fields because these bit fields may be moved within the status register during place and route.

You may choose to remove the status register completely from the hardware by setting the **None** option in the **Interrupts** section of the configuration editor. If this option is set, the API does not support access to the status register. Building a design with API access to the status register will have errors stating that the PWM_1_PWMUDB_sSTSReg_stsreg__STATUS_REG is an undefined identifier. This can be corrected by removing the API and deselecting the **None** option for interrupts in the configuration editor.

The status data is registered at the input clock edge of the counter, giving all bits configured as Mode = 1 the timing resolution of the counter. These bits are sticky and are cleared on a read of the status register. All other bits configured as Mode = 0 are transparent and read directly from the inputs to the status register; they are not sticky and therefore not clear on read. All bits

configured as Mode = 1 are indicated with an asterisk (*) in the following defines. There are several bit-fields masks defined in the status register. Any of these bit fields may be included as an interrupt source. The #defines are available in the generated header file (.h) as follows:

PWM_STATUS_TC *

Status of the terminal count output. This bit goes high when the terminal count output is high.

PWM_STATUS_CMP1 *

Status of the pwm1 compare value as it relates to the period counter. For a fixed-function implementation, this bit goes high when the comparison output is high. For a UDB implementation, this bit is asserted with the registered version of the comparison output; so, the bit is asserted two clocks after the comparison output is high.

PWM_STATUS_CMP2 *

Status of the pwm2 compare value as it relates to the period counter. For a fixed-function implementation, this bit goes high when the comparison output is high. For a UDB implementation, this bit is asserted with the registered version of the comparison output; so, the bit is asserted two clocks after the comparison output is high.

PWM_STATUS_KILL

Status of the output kill. If it is currently active the output will be high.

PWM_STATUS_FIFOFULL

Status of the Capture FIFO level. This bit is a real-time status of the FIFO level indicating that the FIFO is currently Full. A “0” in this bit of the status register indicates that the FIFO is not full but does not indicate that there is not data in the FIFO.

Control (UDB)

The control register allows you to control the general operation of the PWM. This register is written with the PWM_WriteControlRegister() function call and read with PWM_ReadControlRegister(). When reading or writing the control register you must use the bit-field definitions as defined in the header (.h) file. The #defines for the control register are as follows:

PWM_CTRL_ENABLE

The enable bit controls software enabling of the PWM operation. The PWM has a configurable enable mode defined at build time. If the **Enable Mode** parameter is set to **Hardware Only**, this bit has no function. However, in either of the other modes the PWM does not decrement unless this bit is set high. Normal operation requires that this bit is set and held high during all operation of the PWM.

PWM_CTRL_CMPMODE1_MASK

The compare mode control is a three-bit field used to define the expected compare output operation for the pwm1 output. This bit field is three consecutive bits in the control register. All operations on this bit-field must use the #defines associated with the compare modes available. These are:

- PWM_1_B_PWM_CM_LESSTHAN
- PWM_1_B_PWM_CM_LESSTHANOREQUAL
- PWM_1_B_PWM_CM_EQUAL
- PWM_1_B_PWM_CM_GREATERTHAN
- PWM_1_B_PWM_CM_GREATERTHANOREQUAL

This bit field is configured at initialization with the compare mode defined in the CompareMode1 parameter and may be modified with the PWM_SetCompareMode() or PWM_SetCompareMode1() API call.

PWM_CTRL_CMPMODE2_MASK

The compare mode control is a three-bit field used to define the expected compare output operation for the pwm2 output. This bit field is three consecutive bits in the control register. All operations on this bit field must use the #defines associated with the compare modes available. These are:

- PWM_1_B_PWM_CM_LESSTHAN
- PWM_1_B_PWM_CM_LESSTHANOREQUAL
- PWM_1_B_PWM_CM_EQUAL
- PWM_1_B_PWM_CM_GREATERTHAN
- PWM_1_B_PWM_CM_GREATERTHANOREQUAL

This bit field is configured at initialization with the compare mode defined in the CompareMode2 parameter and may be modified with the PWM_SetCompareMode2() API call.

PWM_Control

Bits	7	6	5	4	3	2	1	0
Name	Enable	RSVD	PWM_CTRL_CMPMODE2_MASK [5:3]			PWM_CTRL_CMPMODE1_MASK [2:0]		

Control (FF)

The control register allows you to control the general operation of the PWM. This register is written with the PWM_WriteControlRegister() function call and read with PWM_ReadControlRegister().

Note When writing to the control register, you must not change any of the reserved bits. All operations must be read-modify-write with the reserved bits masked.

PWM_Control

Bits	7	6	5	4	3	2	1	0
Name	Dead Period [1:0]		Deadband mode	RSVD	RSVD	RSVD	Enable Compare Mode	Enable

Bit Name	#define in header file	Description / Enumerated Type
Dead Period	PWM_DEADBAND_COUNT_MASK	Deadband Period from 0 to 3
Deadband mode	PWM_CFG0_DB	Deadband mode - routes compare output to TC output port ▪ 1: compare output goes out on TC output port ▪ 0: terminal count goes out on TC output port
Enable Compare Mode	PWM_CFG0_MODE	This bit enables CNT/CMP register holds comparator threshold value.
Enable	PWM_CTRL_ENABLE	This bit enables counting under software control

Period (8 or 16-bit based on Resolution)

The period register contains the period value set by the user through the PWM_WritePeriod() function call and defined by the **Period** parameter at initialization. The PWM_ReadPeriod() function may be used to find the current value of this register. The period register has no effect on the PWM until a terminal count is reached, at which time the period counter is reloaded with this value.

Compare1/Compare2 (8 or 16-bit based on Resolution)

The compare registers contains the compare values used to determine the state of the pwm or pwm1 and pwm2 outputs (depending on the setting of the **PWM Mode** parameter). The pwm/pwm1 and pwm2 outputs are based on how these registers compare to the period counter value in relation to the compare modes defined in the control register.

Period Counter (8 or 16-bit based on Resolution)

The period counter register contains the counter value throughout the operation of the PWM. During basic operation, this register decrements by 1 while the PWM is enabled and on each rising edge of the clock input. You can read the contents of this register at any time with the PWM_ReadCounter() function call. When the terminal count is reached, this register is reloaded with the period value you define in the period register through the PWM_WritePeriod() function call or during initialization with the **Period** parameter.

The pwm, pwm1, and pwm2 outputs are based on the relationship between the value held in this register and the value defined in the compare registers through the PWM_WriteCompare() function calls or during initialization with the Compare1/Compare2 parameters.

Conditional Compilation Information

The PWM API requires several conditional compile definitions to handle the multiple configurations it must support. The API must conditionally compile on the resolution chosen, the implementation chosen between the fixed-function block or the UDB blocks, dead band modes, kill modes, and PWM modes. The conditions defined are based on the parameters **Implementation**, **Resolution**, **Dead Band**, **Kill Mode**, and **PWM Mode**. The API should never use these parameters directly but should use the following defines.

PWM_Resolution

The resolution define is assigned to the resolution value at build time. It is used throughout the API to compile in the correct data width types for the API functions relying on this information.

PWM_UsingFixedFunction

Using the fixed function define is used mostly in the header file to make the correct register assignments. This is necessary because the registers provided in the fixed-function block are different than those used when the PWM is implemented in UDBs.

PWM_DeadBandMode

The dead band mode define is used to conditionally compile in PWM_WriteDeadTime() and PWM_ReadDeadTime() APIs.

PWM_KillModeMinTime

The kill mode minimum time define is used to conditionally compile in PWM_WriteKillTime() and PWM_ReadKillTime() APIs.

PWM_KillMode

The kill mode define is used to define the register access point for the Kill Mode Min Time register if **Kill Mode** is set to **Minimum Time**.

PWM_PWMMode

The PWM mode define is used to include the correct PWM_WriteCompare() and PWM_ReadCompare() API functions as necessary for the mode in use.

PWM_PWMModeIsCenterAligned

The PWM mode is center aligned define is used to redefine the period register address. Center aligned is different from other modes in implementation and requires the use of different registers for operation that must be handled in the header file.

PWM_DeadBandUsed

The deadband used define controls conditionally compiling the PWM_WriteDeadTime() and PWM_ReadDeadTime() APIs.

PWM_DeadBand2_4

The deadband 2-4 define controls conditionally compiling the implementation within the PWM_WriteDeadTime() and PWM_ReadDeadTime() APIs.

PWM_UseStatus

The use status define is used to remove the status register, if the design requires it, in the Verilog code and to conditionally compile out the status register definitions and APIs in the header and C files.

PWM_UseControl

The use control define is used to remove the control register, if the design requires it, in the Verilog code and to conditionally compile out the control register definitions and APIs in the header and C files.

PWM_UseOneCompareMode

The use one compare mode is used to conditionally compile in and out the expected API calls necessary for 1 or 2 compare mode PWM mode functions.

PWM_MinimumKillTime

Provides the initial minimum kill time programmed into the min-time datapath when the **Kill Mode** is set to **Minimum Kill Time**.

PWM_EnableMode

Allows for condition compilation to remove the API provided for specific Enable modes.

Constants

There are several constants defined for the status and control registers, as well as some of the enumerated types. Most of the constants for the control and status registers have been described earlier in this datasheet. However, there are more constants needed in the header file to make all of this happen. Each of the register definitions requires either a pointer into the register data or a register address. Because of multiple Endianness of the compilers, the CY_GET_REGX and CY_SET_REGX macros must be used for register accesses greater than eight bits. These macros require the use of the _PTR definition for each of the registers.

It is also required that the control and status register bits be allowed to be placed and routed by the fitter engine, because the component must have constants that define the placement of the bits. For each of the status and control register bits there is an associated _SHIFT value that defines the bit's offset within the register. These are used in the header file to define the final bit mask as a _MASK definition. (The _MASK extension is only added to bit fields greater than a single bit, all single bit values drop the _MASK extension.)

The fixed-function block has some limitations compared to the UDB implementations because it is designed with limited configurability.

Resources

Depending on the **Implementation** parameter, the PWM component uses one FF block or is placed throughout the UDB array. The UDB Implementation utilizes the following resources.

Configuration	Resource Type					
	Datapath Cells	Macrocells	Status Cells	Control Cells	DMA Channels	Interrupts
8-bit One Output Mode[4]	1	6	1	1	–	–
8-bit Two Outputs Mode[4]	1	9	1	1	–	–
8-bit Dual Edged Mode[4]	1	8	1	1	–	–
8-bit Center Align Mode[4]	1	10	1	1	–	–
8-bit HW Select Mode[4]	1	8	1	1	–	–
8-bit Dither Mode[4]	1	7	1	1	–	–
16-bit One Output Mode[4]	2	6	1	1	–	–
8-bit with Dead Band 2-4[5]	1	12	1	2	–	–

[4] Configuration 1: The PWM in the corresponding PWM mode and resolution is configured with Software Only Enable mode, Continuous Run Mode, Trigger mode set to None, Kill mode and Capture mode disabled with no dead band and Interrupt on TC.

Configuration	Resource Type					
	Datapath Cells	Macrocells	Status Cells	Control Cells	DMA Channels	Interrupts
16-bit with Dead Band 2-4[5]	2	12	1	2	–	–
8-bit with Dead Band 2-256[5]	2	11	1	1	–	–
16-bit with Dead Band 2-256[5]	3	11	1	1	–	–

DC and AC Electrical Characteristics for PSoC 3 (FF Implementation)

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.
Specifications are valid for 1.71 V to 5.5 V, except where noted.

DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	16-bit PWM block current consumption	Input clock frequency - 3 MHz	–	15	–	µA
		Input clock frequency - 12 MHz	–	60	–	µA
		Input clock frequency - 48 MHz	–	260	–	µA
		Input clock frequency - 67 MHz	–	350	–	µA

AC Specifications

Parameter	Description	Conditions	Min [6]	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Pulse width		T	–	–	ns
	Pulse width (external)		T*2	–	–	ns
	Kill pulse width		T			ns
	Kill pulse width (external)		T*2	–	–	ns
	Enable pulse width		T	–	–	ns
	Enable pulse width (external)		T*2	–	–	ns

5 Configuration 2: 2-4 Dead Band range and 2-256 Dead Band range are mutually exclusive. The PWM is configured for the corresponding resolution and One Output PWM mode with Software Only Enable mode, Trigger mode set to None, Kill mode and Capture mode disabled with Interrupt on TC.

6 T(clock period) = 1/f (Operating frequency)

Parameter	Description	Conditions	Min [6]	Typ	Max	Units
	Reset pulse width		T	–	–	ns
	Reset pulse width (external)		T*2	–	–	ns

DC and AC Electrical Characteristics for PSoC 5LP (FF Implementation)

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.
Specifications are valid for 2.7 V to 5.5 V, except where noted.

DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	16-bit PWM block current consumption	Input clock frequency - 3 MHz	–	65	–	µA
		Input clock frequency - 12 MHz	–	170	–	µA
		Input clock frequency - 48 MHz	–	650	–	µA
		Input clock frequency - 67 MHz	–	900	–	µA

AC Specifications

Parameter	Description	Conditions	Min [6]	Typ	Max[7]	Units
	Operating frequency		DC	–	80.01	MHz
	Pulse width		T	–	–	ns
	Pulse width (external)		T*2	–	–	ns
	Kill pulse width		T	–	–	ns
	Kill pulse width (external)		T*2	–	–	ns
	Enable pulse width		T	–	–	ns
	Enable pulse width (external)		T*2	–	–	ns
	Reset pulse width		T	–	–	ns
	Reset pulse width (external)		T*2	–	–	ns

7 Review the device-specific datasheet to determine the maximum frequency for a particular device.

DC and AC Electrical Characteristics (UDB Implementation)

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.
Specifications are valid for 1.71 V to 5.5 V, except where noted.

DC Characteristics

Parameter	Description	Min	Typ [8]	Max	Units
I_{DD}	Component current consumption				
	8-bit One Output Mode in Continuous Run Mode	–	6	–	µA/MHz
	8-bit One output in Continuous Run Mode with Dither	–	7	–	µA/MHz
	8-bit Center Aligned Output	–	7	–	µA/MHz
	8-bits One output with Dead Band	–	8	–	µA/MHz
	8-bit Continuous Run mode with Kill Mode	–	8	–	µA/MHz
	16-bit One output in Continuous Run Mode	–	10	–	µA/MHz
	16-bit One output in Continuous Run Mode with Dither	–	11	–	µA/MHz
	16 bit Center Aligned Output	–	10	–	µA/MHz
	16-bit One output with Dead Band	–	12	–	µA/MHz
	16-bit Continuous Run mode with Kill Mode	–	11	–	µA/MHz

AC Characteristics

Parameter	Description	Min	Typ	Max [9]	Units
f_{CLOCK}	Component clock frequency				
	8-bit One Output Mode in Continuous Run Mode	–	–	50	MHz
	8-bit One output in Continuous Run Mode with Dither	–	–	51	MHz
	8-bit Center Aligned Output	–	–	43	MHz
	8-bits One output with Dead Band	–	–	38	MHz

8 Device IO and clock distribution current not included. The values are at 25 °C.

9 The values provide a maximum safe operating frequency of the component. The component may run at higher clock frequencies, at which point validation of the timing requirements with STA results is necessary.

Parameter	Description	Min	Typ	Max [9]	Units
	8-bit Continuous Run mode with Kill Mode	–	–	49	MHz
	16-bit One output in Continuous Run Mode	–	–	43	MHz
	16-bit One output in Continuous Run Mode with Dither	–	–	41	MHz
	16 bit Center Aligned Output	–	–	34	MHz
	16-bit One output with Dead Band	–	–	36	MHz
	16-bit Continuous Run mode with Kill Mode	–	–	40	MHz

Component Errata

This section lists known problems with the component.

Cypress ID	Component Version	Problem	Workaround
215899	All	The UDB version of the component has an incorrect define of the status register mask for KILL signal (PWM_STATUS_KILL, PWM_STATUS_KILL_INT_EN_MASK): (0x00u << PWM_STATUS_KILL_SHIFT) instead of (0x01u << PWM_STATUS_KILL_SHIFT). It could impact the following APIs: PWM_SetInterruptMode, PWM_ReadStatusRegister.	If you are using the interrupt for KILL signal, use the define (0x01u << PWM_STATUS_KILL_SHIFT) for the following APIs: PWM_SetInterruptMode(), PWM_ReadStatusRegister().

209259	All	An unintended interrupt pulse can appear on the interrupt output of the PWM component during Start() function execution.	If you are facing this problem, apply the following workaround:
			`CyGlobalIntDisable;`
			`PWM_Start();`
			`isr_ClearPending();`
			`CyGlobalIntEnable;`
			where “isr” is the name of an interrupt component connected to the interrupt output of the PWM component.

Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
3.30.c	Updated datasheet.	Updated Component Errata section to document an issue with an incorrect define of the status register mask for KILL signal.
3.30.b	Updated datasheet.	Updated Input/Output Connections section. Updated Functional Description (Run Mode, PWM Component as a Pulse Generator) section.
3.30.a	Updated datasheet.	Updated Input/Output Connections section. Updated Component Parameters section. Updated Application Programming Interface section. Updated Functional Description section. Updated Registers section.
3.30	Addressed an issue where version 3.20 of the PWM component consumes too many resources.	Reverted fix in the 3.20 version of the PWM component that addressed output signal behavior when the enable signal goes low. Projects that use the 3.20 version of the component contain additional restrictions for the UDB resources placement, potentially leading to a build failure.
	Updated datasheet.	Clarified in the Input/Output Connections section that “enable” and “reset” signals are synchronous. Clarified PWM_Enable() API description in the Application Programming Interface section. Updated Resources section. Updated Functional Description section with timing diagrams to show Enable/Reset signals for the FF and UDB implementations; removed obsolete information not related to the PWM component. Added Component Errata section to document a potential issue with an unintended interrupt pulse.
3.20	Updated PWM output signals behavior when enable input signal is low. Corrected first cycle of the PWM output signals when enable input signal value is changed to high.	Corrected PWM output signals behavior for "Greater", "Greater or Equal" compare modes with enable input signal dependency.
	Updated datasheet.	Updated Component Parameters section. Updated DC and AC Electrical Characteristics for PSoC 5LP section. Clarified Firmware Control value for CMP Type 1 / CMP Type 2 parameters.

Version	Description of Changes	Reason for Changes / Impact
3.10.a	Updated the datasheet.	Corrected the Fixed-Function Block Limitations subsection. Clarify the Input/Output Connections section. Clarify the side effects for the Start API.
3.10	Added support for Bluetooth Low Energy devices.	
	Updated the datasheet.	Clarify API usage (updated API descriptions).
3.0.b	Updated the datasheet.	Clarified PWM_WriteControlRegister API description. Clarified Reset signal behavior. Updated DC and AC Electrical Characteristics (FF Implementation) sections. Updated dead time parameter description.
3.0.a	Updated the datasheet.	Clarified the dither description and removed references to obsolete PSoC 5 device.
3.0	Changed ph2 output behavior when kill high in the UDB implementation from high to low	
2.40	Added PSoC 4 support.	
2.30	Added MISRA Compliance section.	The component does not have any specific deviations.
	Updated API description.	Not full descriptions in previous version.
	Updated incorrect figures.	
2.20	Removed WriteCounter() API support for Fixed Function PWM.	This function is not supported in Fixed function PWM.
	Updated the customizer to fix the issue with waveform display	The waveform is not displayed properly.
2.10	Customizer related updates	To fix minor GUI related issues.
	Updated PWM_RestoreConfig() API	To fix an issue with interrupt trigger after wakeup from low power mode.
	Updated PWM_Stop() and PWM_Enable() APIs	To enable the alternate active power mode for FF PWM.
	Updated PWM_SaveConfig() and PWM_RestoreConfig()updates	To restore PWM period register after wakeup.
	Added PSoC 5 FF DC and AC characteristics to datasheet	
2.0.a	Datasheet updates	
2.0	Synchronized inputs	All inputs are synchronized in the fixed function implementation, at the input of the block.

Version	Description of Changes	Reason for Changes / Impact
	PWM_GetInterruptSource() function was converted to a Macro	The PWM_GetInterruptSource() function is exactly the same implementation as the PWM_ReadStatusRegister() function. To save code space this was converted to a macro substitution of the PWM_ReadStatusRegister() function.
	Outputs are now Registered to the component clock	To avoid glitches on the outputs of the component it was required that all outputs are synchronized. This is done inside of the Datapath when possible, to avoid excess resource usage.
	Implemented critical regions when writing to Aux Control registers.	CyEnterCriticalSection and CyExitCriticalSections functions are used when writing to Aux Control registers so that it is not modified by any other process thread.
	Added characterization data to datasheet	
	Minor datasheet edits and updates	

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