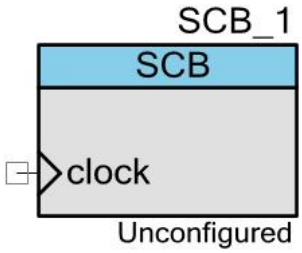
PSoC 4 Serial Communication Block (SCB)

3.20



Features

- Industry-standard NXP® I²C bus interface
- Standard SPI Master and Slave interfaces with Motorola, Texas Instruments, and the National Semiconductor's Microwire protocols
- Standard UART TX and RX interfaces with SmartCard reader and IrDA protocols
- EZ I²C mode which emulates a common I²C EEPROM interface
- Supports wakeup from Deep Sleep mode
- Run-time reconfigurable
- I²C Bootloader support

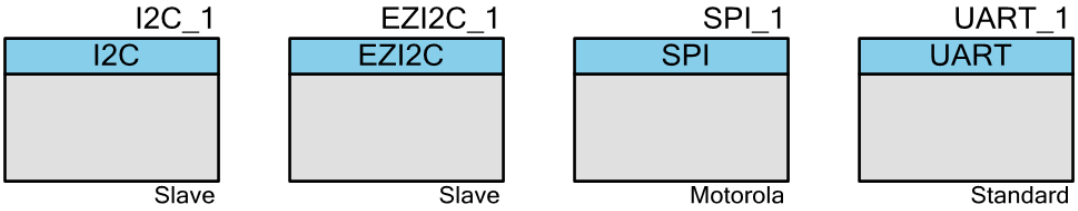
General Description

The PSoC 4 SCB Component is a multifunction hardware block that implements the following communication Components: I²C, SPI, UART, and EZI2C. Each is available as a pre-configured schematic macro in the PSoC Creator Component Catalog, labeled with “SCB Mode.”

Note PSoC 4000 devices support only I²C modes. The UART or SPI mode choice is not available.

Click on one of the links below to jump to the appropriate section:

I2C **EZI2C** **SPI** **UART**

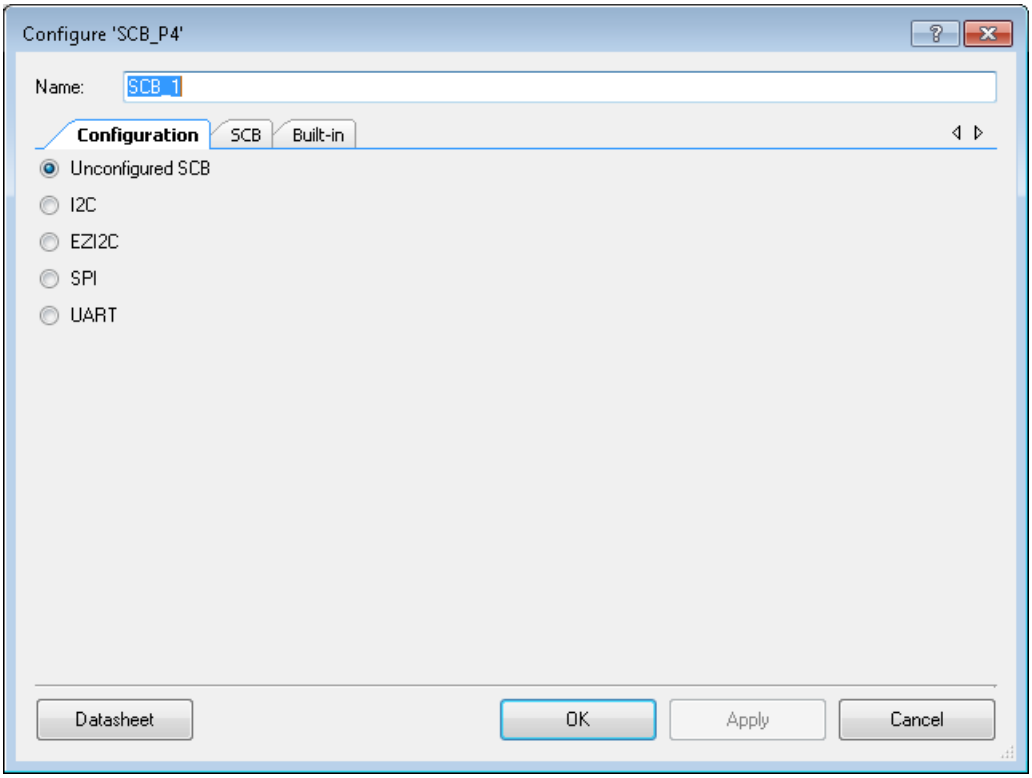


There is also an Unconfigured SCB Component entry in the Component Catalog.

When to Use an SCB Component

The SCB can be used in a pre-configured mode: I²C, EZI2C, SPI, and UART. Alternatively, the SCB can be left unconfigured at build time and then configured during run-time into any of the modes by calling the appropriate API functions. All configuration settings made at build time can also be made during run time.

The following figure shows the Component Configure dialog used to select the desired mode.

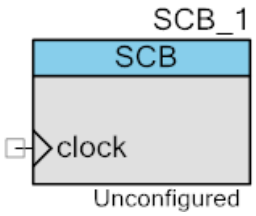


Note PSoC 4000 devices support only I²C modes. The UART or SPI mode choice is not available.

The pre-configured modes are the typical use case. They are the simplest method to configure the SCB into the mode of operation that is desired. The unconfigured method can be used to create designs for multiple applications and where the specific usage of the SCB in the design is not known when the PSoC Creator hardware design is created.

Unconfigured SCB

The SCB can be run-time configured for operation in any of the modes(I2C, SPI, UART, EZI2C) from the Unconfigured mode. It can also be re-configured from any of these modes to any of the other modes during run time. For example, you can reconfigured the SCB from SPI to UART during run time.



Input/Output Connections

This section describes the various input and output connections for the SCB Component. An asterisk (*) in the list of terminals indicates that the terminal may be hidden on the symbol under the conditions listed in the description of that terminal.

clock – Input

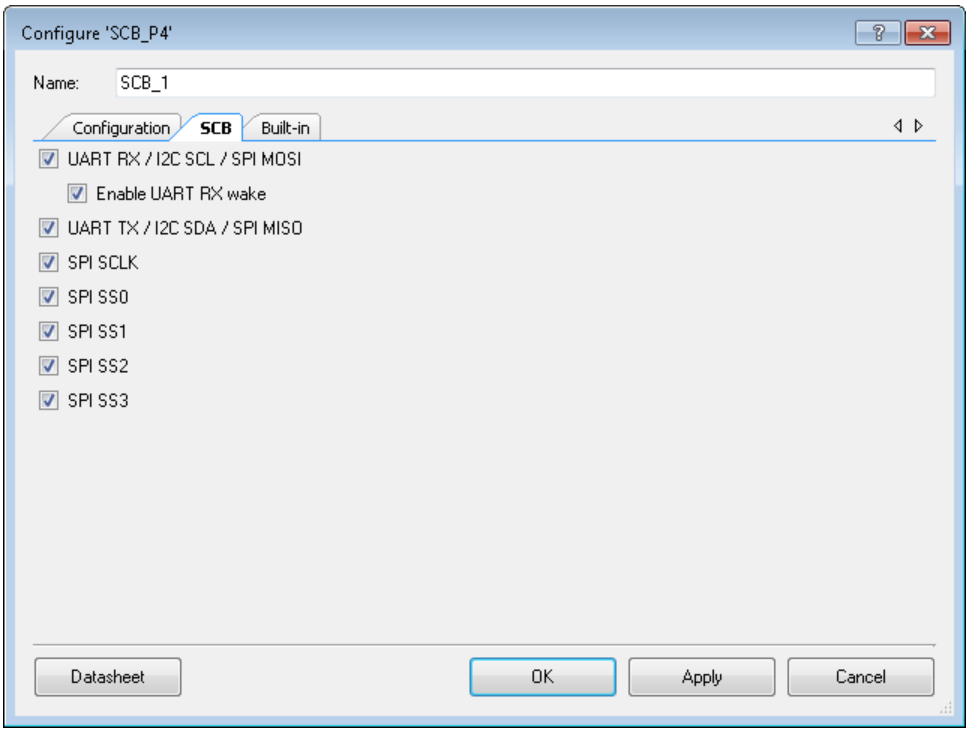
Clock that operates this block. This terminal is required in Unconfigured mode. For other modes the option is provided to use an internal clock or an external clock connected to this terminal.

The interface-specific pins are buried inside the Component because these pins use dedicated connections and are not routable as general purpose signals. See the *I/O System* section in the device *Technical Reference Manual (TRM)* for more information.

Note The input buffer of buried output pins is disabled so as not to cause current linkage in low power mode. Reading the status of these pins always returns zero. To get the current status, the input buffer must be enabled before status read.

SCB Tab

Use the **SCB** tab to select the pins that will be used by the SCB Component in Unconfigured mode. The communication type along with the pin name is listed with a check box to enable pin. When the pin is enabled it is reserved for the SCB, and cannot be used by other functions. To see what pins were reserved consult the pins tab in the .cydwr file



The **Enable UART RX wake** adds an interrupt to the RX pin to accomplish the UART wake-up capability. This option restricts the processing of any other pin interrupts from the port where this RX pin is placed.

Note PSoC 4000 devices only support I^2C modes. The following pin names are used for this device:

- UART RX / I2C SCL / SPI MOSI pin name is I2C SCL
- UART TX / I2C SDA / SPI MISO pin name is I2C SDA
- SPI SCLK, SPI SS0 – SS3 pins are not available, nor is the Enable UART RX wake option

Note PSoC 4100 / PSoC 4200 devices do not support UART hardware flow control. The following pin name changes are used for these devices:

- UART CTS / SPI SCLK pin name is SPI SCLK
- UART RTS / SPI SS0 pin name is SPI SS0

Note PSoC 4100 BLE / PSoC 4200 BLE devices have different locations for the SCL and SDA pins. The following pin name changes are used for these devices:

- UART RX / **I2C SCL** / SPI MOSI pin name is UART RX / **I2C SDA** / SPI MOSI
- UART TX / **I2C SDA** / SPI MISO pin name is UART TX / **I2C SCL** / SPI MISO

Unconfigured mode operation

Before starting operation in Unconfigured mode, determine which communication interfaces will be used (more than one communication interface can be used in one SCB). Next, use the **SCB** parameters tab to select pins required to implement the chosen communication interfaces.

The communication interface name is listed first, followed by the pin name related to the specific interface. For example, UART RX / I2C SCL / SPI MOSI means this pin functions as MOSI when the SCB is configured to utilize the SPI interface; it functions as SCL for the I^2C interface; and as RX for the UART interface.

Next, a clock Component must be connected to the SCB clock input. This clock frequency along with the SCB oversampling configuration (set in the interface-specific Init API function) determines the operation speed of the communications interface. The clock frequency will be configured later in the firmware by setting a clock divider, using the clock's API. The possible choice of clock configuration is: source HFCLK with divider 1.

To use the UART and I^2C interfaces, select the following pins on the **SCB** tab:

- UART RX / I2C SCL / SPI MOSI pin
- UART TX / I2C SDA / SPI MISO pin

To use the SPI interface, select the following pins on the **SCB** tab:

- UART RX / I2C SCL / SPI MOSI pin
- UART TX / I2C SDA / SPI MISO pin
- SPI SCLK
- Any combination of SPI SS0 – SPI SS3

Interface data rate configuration

The data rate is a function of the clock source frequency and the Component configuration of the oversampling parameter. The oversampling parameter is only important for master modes and has no effect for slave (UART mode has the same dependency on oversampling as master modes). For slave modes only, the connected clock source frequency is important.

For I^2C master modes, SPI master, and UART, the data rate is calculated using the formula below (where f_{SCBCLK} is the frequency of the clock Component connected to the SCB):

$$\text{Data rate} = (f_{SCBCLK} / \text{Oversampling value})$$

$$f_{SCBCLK} = \text{Data rate} * \text{Oversampling value}$$

Note For the I^2C interface in master modes, the oversampling value is a sum of Low and High oversampling factor values.

For I^2C and EZI^2C in slave modes, the f_{SCBCLK} must match the values provided in Table 2 on page 16.

For SPI slave mode, the clock source frequency impacts T_{DSO} parameter. Refer to SPI AC Specifications for the selected device and to the Slave data rate section.

Refer to the applicable I2C / EZI2C / SPI / UART Parameter section for more information about data rate and oversampling. To change f_{SCBCLK} clock frequency, the clock divider must be changed. The clock Component provides API to perform this task.

$$Div_{SCBCLK} = f_{HFCLK} / f_{SCBCLK}$$

Note The Div_{SCBCLK} must be an integer value.

Example of Div_{SCBCLK} calculation for I^2C and UART is as follows:

Design HFCLK configuration of f_{HFCLK} = 24 MHz

Required I2C slave data rate = 100 kbps and UART baud rate = 115200 bps

The f_{SCBCLK} = 1.6MHz is taken from Table 2 on page 16 for data rate 100 kbps:

$$Div_{SCBCLK} = f_{HFCLK} / f_{SCBCLK} = 24 \text{ MHz} / 1.6 \text{ MHz} = 15$$

The oversampling default value 16 is chosen to calculate Div_{SCBCLK} for the UART.

$$f_{SCBCLK} = \text{Data rate} * \text{Oversampling value} = 115200 * 16 = \sim 1{,}843 \text{ MHz}$$

$$Div_{SCBCLK} = f_{HFCLK} / f_{SCBCLK} = 24 \text{ MHz} / 1,\ 843 \text{ MHz} = \sim 13$$

For the UART, the f_{SCBCLK} accuracy is important for correct operation and the actual f_{SCBCLK} must be calculated to use f_{HFCLK} and Div_{SCBCLK}.

Actual $f_{SCBCLK} = f_{HFCLK} / Div_{SCBCLK}$ = 24 MHz / 13 = ~1,846 MHz

The deviation of actual f_{SCBCLK} from desired must be calculated:

(1,843MHz – 1,846 MHz) / 1,843 MHz = ~0.2%

Taking into account HFCLK accuracy ±2%, the total error is: 0.2 + 2= 2.2%. The total error value is less than 5% and it is enough for correct UART operation.

The following numbers are calculated:

- I^2C master data rate = 100 kbps: Div_{SCBCLK} = 15
- UART baud rate = 115200 bps: Oversampling = 16, Div_{SCBCLK} = 13

Run-time Configuration

Configuration structures are provided for each interface. These structures provide configuration fields that match the selections available in the Configure dialog for the specific interface. The description of each structure is provided in the APIs section of corresponding interface:

- void SCB_**I2CInit**(SCB_I2C_INIT_STRUCT *config)
- void SCB_**EzI2CInit**(SCB_EZI2C_INIT_STRUCT *config)
- void SCB_**SpiInit**(SCB_SPI_INIT_STRUCT *config)
- Void SCB_**UartInit**(SCB_UART_INIT_STRUCT *config)

Allocate structures for the selected interfaces and fill the structure with the required configuration information. A pointer to this structure is passed to the appropriate initialization function of the selected interface. The list of initialization functions for each interface is provided above.

The following example provides configuration structures for:

- I2C slave, data rate 100 kbps, slave address is 0x08
- UART RX+TX, sub-mode Standard, buffer size 16 for TX and RX (implies software buffer utilization)

The following code snippets are taken from the SCB Uncofigured example project SCB_UnconfiguredComm.

```
/*******************************************************************************
* Common Definitions
*******************************************************************************/
/* Constants */
#define ENABLED         (1u)
#define DISABLED        (0u)
#define NON_APPLICABLE  (DISABLED)
```

```
/* Common RX and TX buffers for I2C and UART operation */
#define COMMON_BUFFER_SIZE     (16u)
uint8 bufferTx[COMMON_BUFFER_SIZE];

/* UART RX buffer requires one extra element for proper operation. One element
* remains empty while operation. Keeping this element empty simplifies
* circular buffer operation.
*/
uint8 bufferRx[COMMON_BUFFER_SIZE + 1u];


/*******************************************************************************
* I2C Configuration
*******************************************************************************/
#define I2C_SLAVE_ADDRESS       (0x08u)
#define I2C_SLAVE_ADDRESS_MASK  (0xFEu)
#define I2C_STANDARD_MODE_MAX   (100u)

#define I2C_RX_BUFFER_SIZE      (PACKET_SIZE)
#define I2C_TX_BUFFER_SIZE      (PACKET_SIZE)
#define I2C_RX_BUFER_PTR        bufferRx
#define I2C_TX_BUFER_PTR        bufferTx

/* I2C slave desired data rate is 100 kbps. The datasheet Table 1 provides a
* range of possible clock values 1.55 - 12.8 MHz. The CommCLK = 1.6 MHz is
* selected from this range. The clock divider has to be calculated to control
* clock frequency as clock Component provides interface to it.
* Divider = (HFCLK / CommCLK) = (24MHz / 1.6 MHz) = 15. But the value written
* into the register has to decremented by 1. The end result is 14.
*/
#define I2C_CLK_DIVIDER         (14u)

/* Comm_I2C_INIT_STRUCT provides the fields which match the selections available
* in the customizer. Refer to the I2C customizer for detailed description of
* the settings.
*/
const Comm_I2C_INIT_STRUCT configI2C =
{
    Comm_I2C_MODE_SLAVE,    /* mode: slave */
    NON_APPLICABLE,         /* oversampleLow: N/A for slave */
    NON_APPLICABLE,         /* oversampleHigh: N/A for slave */
    NON_APPLICABLE,         /* enableMedianFilter: N/A */
    I2C_SLAVE_ADDRESS,      /* slaveAddr: slave address */
    I2C_SLAVE_ADDRESS_MASK, /* slaveAddrMask: single slave address */
    DISABLED,               /* acceptAddr: disabled */
    DISABLED,               /* enableWake: disabled */
    DISABLED,               /* enableByteMode: disabled */
    I2C_STANDARD_MODE_MAX,  /* dataRate: 100 kbps */
    DISABLED,               /* acceptGeneralAddr */
};
```

```
/*******************************************************************************
* UART Configuration
*******************************************************************************/
#define UART_OVERSAMPLING       (16u)
#define UART_DATA_WIDTH         (8u)
#define UART_RX_INTR_MASK       (Comm_INTR_RX_NOT_EMPTY)
#define UART_TX_INTR_MASK       (0u)

#define UART_RX_BUFFER_SIZE     (COMMON_BUFFER_SIZE)
#define UART_TX_BUFFER_SIZE     (COMMON_BUFFER_SIZE)
#define UART_RX_BUFER_PTR       bufferRx
#define UART_TX_BUFER_PTR       bufferTx

/* UART desired baud rate is 115200 bps. The selected Oversampling parameter is
* 16. The CommCLK = Baud rate * Oversampling = 115200 * 16 = 1.843 MHz.
* The clock divider has to be calculated to control clock frequency as clock
* Component provides interface to it.
* Divider = (HFCLK / CommCLK) = (24MHz / 1.8432 MHz) = 13. But the value
* written into the register has to decremented by 1. The end result is 12.
* The clock accuracy is important for UART operation. The actual CommCLK equal:
* CommCLK(actual) = (24MHz / 13MHz) = 1.846 MHz
* The deviation of actual CommCLK from desired must be calculated:
* Deviation = (1.843MHz - 1.846 MHz) / 1.843 MHz = ~0.2%
* Taking into account HFCLK accuracy ±2%, the total error is: 0.2 + 2= 2.2%.
* The total error value is less than 5% and it is enough for correct
* UART operation.
*/
#define UART_CLK_DIVIDER        (12u)

/* Comm_UART_INIT_STRUCT provides the fields which match the selections
* available in the customizer. Refer to the I2C customizer for detailed
* description of the settings.
*/
const Comm_UART_INIT_STRUCT configUart =
{
    Comm_UART_MODE_STD,     /* mode: Standard */
    Comm_UART_TX_RX,        /* direction: RX + TX */
    UART_DATA_WIDTH,        /* dataBits: 8 bits */
    Comm_UART_PARITY_NONE,  /* parity: None */
    Comm_UART_STOP_BITS_1,  /* stopBits: 1 bit */
    UART_OVERSAMPLING,      /* oversample: 16 */
    DISABLED,               /* enableIrdaLowPower: disabled */
    DISABLED,               /* enableMedianFilter: disabled */
    DISABLED,               /* enableRetryNack: disabled */
    DISABLED,               /* enableInvertedRx: disabled */
    DISABLED,               /* dropOnParityErr: disabled */
    DISABLED,               /* dropOnFrameErr: disabled */
    NON_APPLICABLE,         /* enableWake: disabled */
    UART_RX_BUFFER_SIZE,    /* rxBufferSize: TX software buffer size */
    UART_RX_BUFER_PTR,      /* rxBuffer: pointer to RX software buffer */
    UART_TX_BUFFER_SIZE,    /* txBufferSize: TX software buffer size */
    UART_TX_BUFER_PTR,      /* txBuffer: pointer to TX software buffer */
    DISABLED,               /* enableMultiproc: disabled */
    DISABLED,               /* multiprocAcceptAddr: disabled */
    NON_APPLICABLE,         /* multiprocAddr: N/A */
```

```
    NON_APPLICABLE,         /* multiprocAddrMask: N/A */
    ENABLED,                /* enableInterrupt: enable internal interrupt
                             * handler for the software buffer */
    UART_RX_INTR_MASK,      /* rxInterruptMask: enable INTR_RX.NOT_EMPTY to
                             * handle RX software buffer operations */
    NON_APPLICABLE,         /* rxTriggerLevel: N/A */
    UART_TX_INTR_MASK,      /* txInterruptMask: no TX interrupts on start up */
    NON_APPLICABLE,         /* txTriggerLevel: N/A */
    DISABLED,               /* enableByteMode: disabled */
    DISABLED,               /* enableCts: disabled */
    DISABLED,               /* ctsPolarity: disabled */
    DISABLED,               /* rtsRxFifoLevel: disabled */
    DISABLED,               /* rtsPolarity: disabled */
};
```

The following example implements a function that changes the SCB configuration according to the passed opMode, and returns the status of the configuration change. This function refers to configuration structures provided for the I^2C and UART previously.

The instance name of the SCB Component is “Comm” and the instance name of the clock Component is “CommCLK”.

```
/* Operation mode: I2C slave or UART */
#define OP_MODE_UART    (0u)
#define OP_MODE_I2C     (1u)

/* Global variables to manage current operation mode and initialization state */
uint32 mode = OP_MODE_UART;


/*******************************************************************************
* Function Name: ConfigurationChange
*******************************************************************************/
static cystatus ConfigurationChange(uint32 opMode)
{
    cystatus status = CYRET_SUCCESS;

    if (OP_MODE_I2C == opMode)
    {
        /***********************************************************************
        * Configure SCB in I2C mode and enable Component after completion.
        ***********************************************************************/

        /* Disable Component before re-configuration */
        Comm_Stop();

        /* Set clock divider to provide clock frequency to the SCB Component
        * to operated with desired data rate.
        */
        CommCLK_SetFractionalDividerRegister(I2C_CLK_DIVIDER, 0u);

        /* Configure SCB Component. The configuration is stored in the I2C
        * configuration structure.
        */
```

```
            Comm_I2CInit(&configI2C);

            /* Set read and write buffers for the I2C slave */
            Comm_I2CSlaveInitWriteBuf(I2C_RX_BUFER_PTR, I2C_RX_BUFFER_SIZE);
            Comm_I2CSlaveInitReadBuf (I2C_TX_BUFER_PTR, I2C_TX_BUFFER_SIZE);

            /* Start Component after re-configuration is complete */
            Comm_Start();
        }
        else if (OP_MODE_UART == opMode)
        {
            /*****************************************************************
            * Configure SCB in UART mode and enable Component after completion
            *****************************************************************/

            /* Disable Component before re-configuration */
            Comm_Stop();

            /* Set clock divider to provide clock frequency to the SCB Component
            * to operated with desired data rate.
            */
            CommCLK_SetFractionalDividerRegister(UART_CLK_DIVIDER, 0u);

            /* Configure SCB Component. The configuration is stored in the UART
            * configuration structure.
            */
            Comm_UartInit(&configUart);

            /* Start Component after re-configuration is complete */
            Comm_Start();
        }
        else
        {
            status = CYRET_BAD_PARAM; /* Unknown operation mode - no action */
        }

        return (status);
    }
```

Note The ConfigurationChange() is a custom function that is not part of the Component API.

Note Before changing the configuration, the SCB Component must be disabled.

Note The SCB_Init() function does not initialize the Component when the mode is Unconfigured. The SCB_**"Mode"**Init() specific APIs have to called.

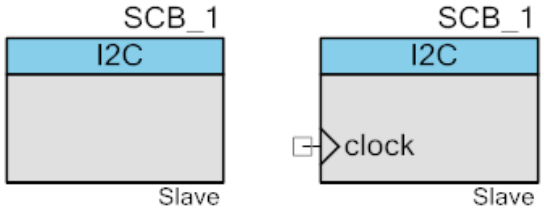
API Names

Some APIs contain specific interface prefixes as part of their name. These APIs operate correctly only when the Component is configured to utilize this interface. For example, the SCB_I2CSlaveStatus() function works with the I^2C interface.

Other APIs are shared between two interfaces. In these cases, the API name contains each interface. For example, the SCB_SpiUartWriteTxData() works with both the SPI or UART interfaces.

APIs that do not belong to specific interfaces do not contain interface prefixes. For example, SCB_Enable() or SCB_EnableInt().

I2C



The I²C bus is an industry-standard, two-wire hardware interface developed by Philips. The master initiates all communication on the I²C bus and supplies the clock for all slave devices. I²C is an ideal solution when networking multiple devices on a single board or small system.

The Component supports I²C Slave, Master, Multi-Master and Multi-Master-Slave configurations.

The Component supports standard clock speeds up to 1000 kbps. It is compatible [1] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification [2] on the NXP web site at www.nxp.com. The Component is compatible with other third-party slave and master devices.

Input/Output Connections

This section describes the various input and output connections for the SCB Component. An asterisk (*) in the list of terminals indicates that the terminal may be hidden on the symbol under the conditions listed in the description of that terminal.

clock – Input*

Clock that operates this block. The presence of this terminal varies depending on the Clock from terminal parameter.

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1 The PSoC 4 I²C peripherals are not completely compliant with the I²C specification except PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L which have GPIO_OVT pins. For detailed information refer to the *Device datasheet*.

2. Refer to the *I²C-Bus Specification* (Rev. 6 from October 2012) on the NXP web site at www.nxp.com.

Internal Pins Configuration

The I²C SCL and SDA pins are buried inside Component: SCB_scl and SCB_sda. These pins are buried because they use dedicated connections and are not routable as general purpose signals. Refer to the *I/O System* section in the device *Technical Reference Manual (TRM)* for more information.

Note The instance name is not included in the Pin Name provided in the following table.

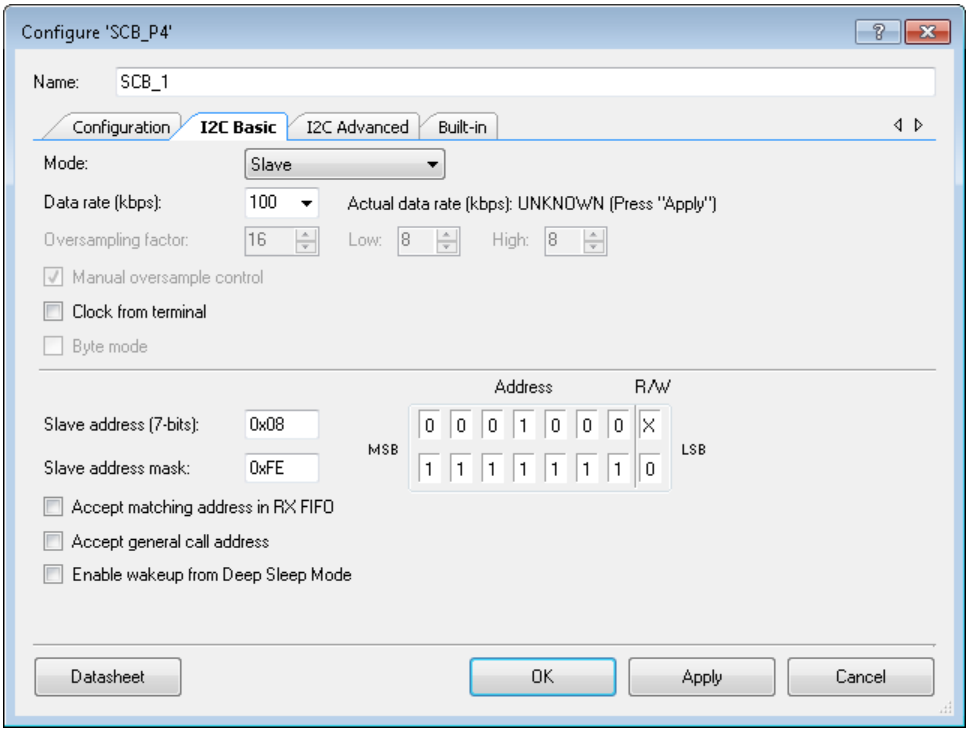
Table 1. I2C Pins Configuration

Pin Name	Direction	Drive Mode	Initial Drive State	Threshold	Slew Rate	Descriptiion
scl	Bidirectional	Open Drain Drives Low	High	CMOS	Fast	Serial clock (SCL) is the master-generated I²C clock. This pins configuration requires connection of external pulls on the I²C bus. The other option is applying internal pull-ups, described in the Internal Pull-Ups section. For PSoC 4100 / PSoC 4200 devices, I²C pins output enable is assigend to 0 to make High-Z state when I²C device does not drive the bus. This behavior supresses usage of internal pull-ups (changing Drive Mode to Resistive pull-up has no effect). For other devices, I²C pins output enable tied to 1 and pin state depends on drive mode and output signal. The internal pull-ups can be used.
sda	Bidirectional	Open Drain Drives Low	High	CMOS	Fast	Serial data (SDA) is the I2C data pin. This pins configuration requires connection of external pulls on the I2C bus. The other option is applying internal pull-ups which is described in the Internal Pull-Ups section. For PSoC 4100 / PSoC 4200 devices I²C pins output enable is assigend to 0 to make High-Z state when I²C device does not drive the bus. This behaviour supresses usage of internal pull-ups (changing Drive Mode to Resistive pull-up has no effect). For other devices: I²C pins output enable tied to 1 and pin state depends on pin's drive mode and output signal. The internal pull-ups can be used.

The Input threshold level CMOS should be used for the vast majority of application connections. The Output slew rate can be changed use Slew rate parameter. The other Input and Output pin's parameters are set to default. Refer to pin Component datasheet for more information about parameters values.

To change I²C pins configuration the pin's Component APIs should be used or direct pin registers configuration. For example refer to the Internal Pull-Ups section.

Basic I2C Parameters



The **I2C Basic** tab has the following parameters:

Mode

This option determines which mode will be supported: Slave, Master, Multi-Master or Multi-Master-Slave.

- **Slave** – Slave only operation (default)
- **Master** – Master only operation
- **Multi-Master** – Supports more than one master on the bus
- **Multi-Master-Slave** – Simultaneous slave and multi-master operation

Data rate

This parameter is used to set the I^2C data rate value up to 1000 kbps (400 kbps for PSoC 4000 family); the actual data rate may differ from the selected data rate due to available clock frequency and Component settings. The standard data rates are 100 (default), 400, and 1000 kbps. This parameter has no effect if the **Clock from terminal** option is enabled.

Refer to the Data rate configuration section for more information about provided options of the data rate selection.

Actual data rate

The actual data rate displays the data rate at which the Component will operate with current settings. The factors that affect the actual data rate calculation are: the accuracy of the Component clock (internal or external) and oversampling factor (only for the Master modes). If any of these parameters change the actual data rate is unknown. To calculate the new actual data rate press the Apply button.

Note For Slave mode the actual data rate always provides maximum value for the selected data rate mode (Standard-mode, Fast-mode, Fast-mode Plus).

Oversampling factor

This parameter defines the oversampling factor of the I^2C SCL clock; the number of Component clocks within one I^2C SCL clock period.

For Slave mode, the oversampling factor is not applicable. The Component configures the SCB clock to be within the valid range for the selected data rate. The valid clock frequency range is taken from the Table 2 on page 16.

For Master modes, the Oversampling factor is the sum of Low and High oversampling values. These values are used to generate the Low and High phases of the I^2C clock.

The valid range of the Oversampling factor values is 12–32. The default is 16.

Low

This parameter is only applicable for **Master** modes. It specifies the oversampling factor of the I^2C SCL clock low phase; the number of Component clocks within one low period of the I^2C SCL clock. The minimum oversampling factor value is 7. The default is 8.

High

This parameter is only applicable for **Master** modes. It specifies the oversampling factor of the I^2C SCL clock high phase; the number of Component clocks within one high period of the I^2C SCL clock. The minimum oversampling factor value is 5. The default is 8.

Manual oversample control

This option is only available for **Master** modes. It allows a choice between manual and automatic selection of I^2C Oversampling factor parameters.

In the case of manual oversample control all oversampling parameters are editable. The oversampling factor is used to calculate internal clock frequency to achieve this amount of oversampling for the defined Data rate: f_{SCBCLK} = Data rate * Oversampling factor. The oversampling Low and High values are editable but sum of them must be equal to Oversampling factor.

In the case of automatic oversample control all oversampling parameters are disabled and calculated by the GUI. The GUI requests an internal clock that is in range provided in the Table 3 on page 16 for the selected data rate. Creator creates a clock in this range and returns the clock frequency to the GUI. The GUI uses this clock frequency and the selected data rate to calculate the oversampling value. The oversampling values Low and High are adjusted to meet the request data rate.

Note Refer to the Clock from terminal section to get more information about possible deviation of requested clock frequency and actual value.

Clock from terminal

This check box allows choosing an internally configured clock (by the Component) or an externally configured clock (by the user) for Component operation. Refer to the Oversampling factor section to understand relationship between Component clock frequency and the Component parameters.

When this option is enabled, the Component does not control the data rate, but displays the actual data rate based on the user-connected clock source frequency and the Component oversampling factor (only for the Master modes). When this option is not enabled, the clock configuration is provided by the Component. The clock source frequency is calculated or selected by the Component based on the Data rate parameter and Oversampling factor (only for the Master mode).

The following tables show the valid ranges for the Component clock for each data rate. When using the Clock from terminal option, ensure that the external clock is within these ranges.

Table 2. I2C Slave clock frequency ranges

Parameter	Standard-mode (0-100 kbps)		Fast-mode (0-400 kbps)		Fast-mode Plus (0-1000 kbps)		Units
	Min	Max	Min	Max	Min	Max	
f_{SCB}	1.55	12.8	7.82	15.38	15.84	48.0	MHz

Note For Slave mode, if the clock frequency is less than lower limit of 1.55 MHz, an error is generated while building the project.

Table 3. I2C Master modes clock frequency ranges

Parameter	Standard-mode (0-100 kbps)		Fast-mode (0-400 kbps)		Fast-mode Plus (0-1000 kbps)		Units
	Min	Max	Min	Max	Min	Max	
f_{SCB}	1.55	3.2	7.82	10.00	14.32	25.8	MHz
Oversampling Low	8	16	13	16	9	16	–

Parameter	Standard-mode (0-100 kbps)		Fast-mode (0-400 kbps)		Fast-mode Plus (0-1000 kbps)		Units
	Min	Max	Min	Max	Min	Max	
Oversampling High	8	16	8	16	6	16	–

Taking into account the ranges provided in Table 3 on page 16 for clock frequency and oversampling the calculated data rate ranges are provided in Table 4 on page 17.

It is possible to create data rates that are outside of the ranges provided in Table 4 on page 17. However creating these data rates requires using clock frequencies or oversampling outside of the ranges provided in Table 3 on page 16. If a clock frequency or oversampling is used outside of the range provided in Table 3 on page 16 certain I^2C parameters in the I^2C specification may be violated. To determine which specifications are violated refer to the I2C spec parameters calculation section.

Table 4. I2C master modes data rates ranges

Parameter	Standard-mode (0-100 kbps)		Fast-mode (0-400 kbps)		Fast-mode Plus (0-1000 kbps)		Units
	Min	Max	Min	Max	Min	Max	
Data rate	48	100	244	400	447	1000	kbps

Note PSoC Creator is responsible for providing requested clock frequency (internal or external clock) based on current design clock configuration. When the requested clock frequency with requested tolerance cannot be created, a warning about the clock accuracy range is generated while building the project. This warning contains the actual clock frequency value created by PSoC Creator. To remove this warning you must either change the system clock, Component settings or external clock to fit the clocking system requirements.

Byte mode

This option is only applicable for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices. It allows doubling the TX and RX FIFO depth from 8 to 16 bytes. Increasing FIFO depth improves performance of I^2C operation, as more bytes can be transmitted or received without software interaction.

Slave address (7-bits)

This is the I^2C address that will be recognized by the slave. It is only applicable for slave modes. This address is the 7-bit right-justified slave address and does not include the R/W bit. A slave address between 0x08 and 0x7F may be selected; the default is 0x08.

The value may be entered as decimal or hexadecimal; for hexadecimal numbers type ‘0x’ before the address. The binary input format is supported as well.

Slave address mask

This parameter is used to mask bits of the slave address during the address match procedure. Bit 0 of the address mask corresponds to the read/write direction bit and is always a do not care in the address match.

- Bit value 0 – excludes bit from address comparison.
- Bit value 1 – the bit needs to match with the corresponding bit of the I^2C slave address.

The following example shows the 7-bit slave address is 0x1B and the 8-bit address Mask is 0xDE.

	7-bits Slave address							R/W
Address	0	0	1	1	0	1	1	x
Mask	1	1	0	1	1	1	1	0
Result	0	0	x	1	0	1	1	x

x = Do not care

Thus the matched 7-bit slave addresses are 0x1B and 0x0B.

The value may be entered as decimal or hexadecimal; for hexadecimal numbers type ‘0x’ before the address. The binary input format is supported as well.

Accept matching address in RX FIFO

This parameter determines whether to accept a matched I^2C slave address in the RX FIFO or not. This can be useful when more than one I^2C address is implemented in a single SCB. In order to access this address a callback function needs to be registered with the SCB_SetI2cAddressCustomInterruptHandler() function. Inside this call back function the address can be read out of the RX FIFO, and then appropriate action can be taken based on the address in the FIFO. This may include a status update or changing read or write buffer. The callback function must return the decision made to ACK or NACK the address. The NACK or ACK command is executed by the I^2C slave ISR. If the callback function is not registered the accepted addresses are ACKed and the address is read from the RX FIFO and discarded.

For more information, refer to the Accept matching address RX FIFO section under the I^2C chapter in this document.

Note If this option is checked and the address is not read in a callback function the address will appear in the write buffer. This may not be desirable behavior.

Accept general call address

This option enables the hardware to accept the I²C general call address (0x00). In order to access this general call address a callback function needs to be registered with the SCB_SetI2cAddressCustomInterruptHandler() function. Inside this callback function the general call address accept status can be checked, and then appropriate action can be taken based on the address in the FIFO. This may include status update, changing read or write buffer. The callback function must return the decision made to ACK or NACK the address. The NACK or ACK command is executed by the I²C slave ISR. If the callback function is not registered the general call address is ACKed.

For more information, refer to the Accept General Call section under the I²C chapter in this document.

Note The general call address accept does not cause wakeup event to occur.

Enable wakeup from Deep Sleep Mode

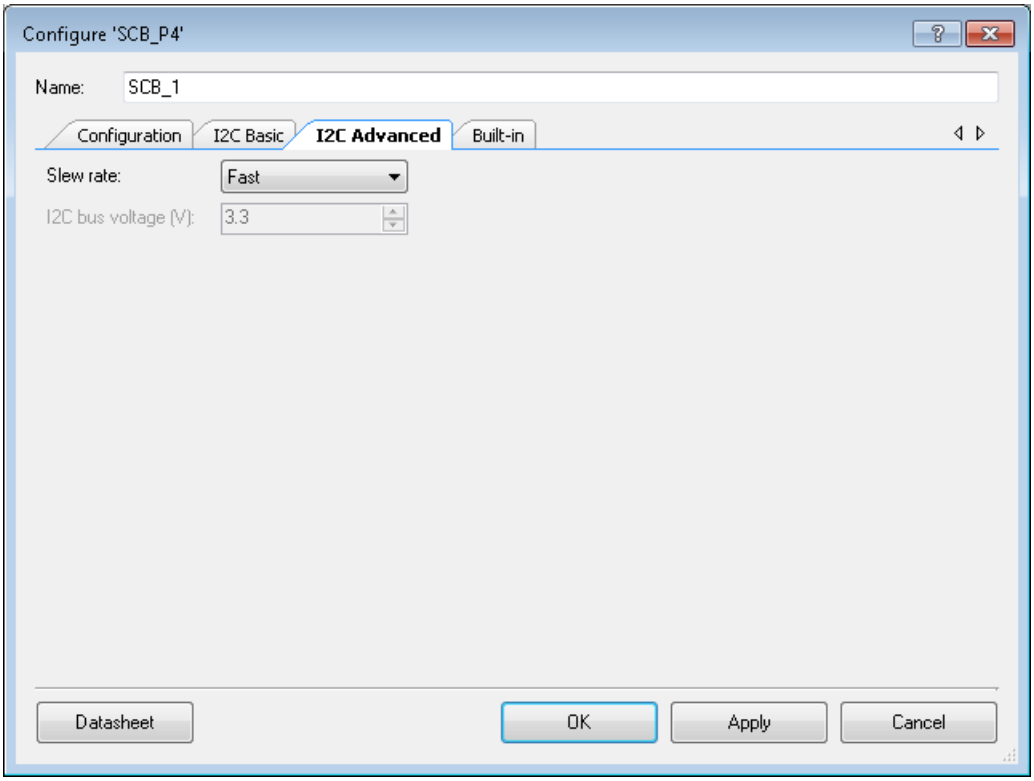
Use this option to enable the Component to wake the system from Deep Sleep when a slave address match occurs. It is only available for Slave or Multi-Master-Slave mode.

For PSoC 4100 / PSoC 4200 devices, the Slave address (7-bits) must be even (bit 0 equal zero) when this option is enabled.

For all supported devices, the data rate must be less than or equal to 400 kbps for Multi-Master-Slave mode when this option is enabled.

Refer to the Low power modes section under the I²C chapter in this document; refer also to the *Power Management APIs* section of the *System Reference Guide* for more information.

Advanced I2C Parameters



The **I2C Advanced** tab contains the following parameters:

Slew rate

This option allows to control slew rate setting of the SCL and SDA pins. The slow slew rate increases the fall time on the lines, reducing EMI and coupling with neighboring signals. For devices supporting GPIO Over-Voltage Tolerance (GPIO_OVT) pins, I2C FM+ options should be used when I²C data rate is greater than 400 kbps. This option also requires the I2C bus voltage to be defined. Refer to the *Device Datasheet* to determine which pins are GPIO_OVT capable. Default is fast.

Notes

- GPIO_OVT pins are fully compliant with the I²C specification (except for hot swap capability during I²C active communication), but the slew rate must be set appropriately:
  - **Slew rate** "Slow" for Standard mode (100 kbps) and Fast mode (400 kbps)
  - **Slew rate** "I2C FM+" for Fast mode plus (1 Mbps)

  Common GPIO pins are not completely compliant with the I²C specification. Refer to the *Device Datasheet* for the details.
- **Slew rate** settings are applied to all pins of the associated port.

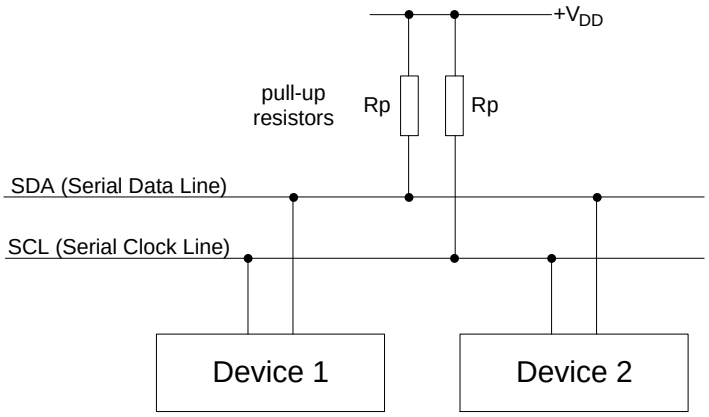
I2C bus voltage (V)

This option is only applicable for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L devices. It specifies the voltage applied to the I^2C pull up resistors when Slew rate is I2C FM+. The voltage no less than applied to I^2C pulls up resistors must be provided by the V_{DDD} supply input, otherwise the I^2C pins cannot be placed. Valid values of V_{DDD} are determined by the settings in the Design-Wide Resources System Editor (in the *<project>.cydwr* file). This range check is performed outside this dialog; the results appear in the Notice List window if the check fails. Default is 3.3 V.

External Electrical Connections

As shown in the following figure, the I^2C bus requires external pull-up resistors. The pull-up resistors (R_P) are primarily determined by the supply voltage, bus speed, and bus capacitance. For detailed information on how to calculate the optimum pull-up resistor value for your design we recommend using the UM10204 I^2C-bus specification and user manual Rev. 6, available from the NXP website at www.nxp.com.

Figure 1. Connection of Devices to the I^2C Bus



For most designs, the default values shown in the following table provide excellent performance without any calculations. The default values were chosen to use standard resistor values between the minimum and maximum limits.

Table 5. Recommended Default Pull-up Resistor Values

Standard Mode (0 – 100 kbps)	Fast Mode (0 – 400 kbps)	Fast Mode Plus (0 – 1000 kbps)	Units
4.7 k, 5%	1.74 k, 1%	620, 5%	Ω

These values work for designs with 1.8 V to 5.0V V_{DD}, less than 200 pF bus capacitance (C_B), up to 25 µA of total input leakage (I_{IL}), up to 0.4 V output voltage level (V_{OL}), and a max V_{IH} of 0.7 * V_{DD}.

Standard Mode and Fast Mode can use either GPIO [1] or GPIO_OVT PSoC pins. Fast Mode Plus requires use of GPIO_OVT pins to meet the V_{OL} spec at 20 mA. Calculation of custom pull-up resistor values is required if; your design does not meet the default assumptions, you use series resistors (R_S) to limit injected noise, or you want to maximize the resistor value for low power consumption.

Calculation of the ideal pull-up resistor value involves finding a value between the limits set by three equations detailed in the NXP I^2C specification. These equations are:

Equation 1: $R_{PMIN} = (V_{DD}(max) – V_{OL}(max)) / I_{OL}(min)$

Equation 2: $R_{PMAX} = T_R(max) / 0.8473 \times C_B(max)$

Equation 3: $R_{PMAX} = V_{DD}(min) – (V_{IH}(min) + V_{NH}(min)) / I_{IH}(max)$

Equation parameters:

- V_{DD} = Nominal supply voltage for I^2C bus
- V_{OL} = Maximum output low voltage of bus devices.
- I_{OL}= Low level output current from I^2C specification
- T_R = Rise Time of bus from I^2C specification
- C_B = Capacitance of each bus line including pins and PCB traces
- V_{IH} = Minimum high level input voltage of all bus devices
- V_{NH} = Minimum high level input noise margin from I^2C specification
- I_{IH} = Total input leakage current of all devices on the bus

The supply voltage (V_{DD}) limits the minimum pull-up resistor value due to bus devices maximum low output voltage (V_{OL}) specifications. Lower pull-up resistance increases current through the pins and can therefore exceed the spec conditions of V_{OH}. Equation 1 is derived using Ohm's law to determine the minimum resistance that will still meet the V_{OL} specification at 3 mA for standard and fast modes, and 20 mA for fast mode plus at the given V_{DD}.

Equation 2 determines the maximum pull-up resistance due to bus capacitance. Total bus capacitance is comprised of all pin, wire, and trace capacitance on the bus. The higher the bus capacitance the lower the pull-up resistance required to meet the specified bus speeds rise time due to RC delays. Choosing a pull-up resistance higher than allowed can result in failing timing requirements resulting in communication errors. Most designs with five of fewer I^2C devices and up to 20 centimeters of bus trace length have less than 100 pF of bus capacitance.

A secondary effect that limits the maximum pull-up resistor value is total bus leakage calculated in Equation 3. The primary source of leakage is I/O pins connected to the bus. If leakage is too high, the pull-ups will have difficulty maintaining an acceptable V_{IH} level causing communication errors. Most designs with five or fewer I^2C devices on the bus have less than 10 µA of total leakage current.

Internal Pull-Ups

PSoC also has an internal pull-up resistor for each pin that can be used instead of external pull-up resistors connected to the I²C bus. These resistors are weak (5.6k Ω); therefore, their usage is limited to Standard mode operation according to Table 5 on page 21. Refer to *Device Datasheet* parameter R_{PULLUP} for resistor value specification. It is **not recommended** to use internal I²C pull-up resistors because their value **cannot be changed** if needed later in the design.

The I²C pins SCL and SDA are buried inside the SCB Component. The drive mode for these pins is “Open Drain, Drives Low” for use with external pull-up resistors on the I²C bus. To enable use of the PSoC internal pull-up resistor, the drive mode of the pin must be changed to “Resistive Pull Up.” The SCB Component GUI does not provide this option; therefore, the drive mode must be changed by firmware. The pin names are generated from the Component name in the schematic and may require updating. The following code must be added before starting the Component:

```
/* Change SCL and SDA pins drive mode to Resistive Pull Up */
SCB_scl_SetDriveMode(SCB_scl_DM_RES_UP);
SCB_sda_SetDriveMode(SCB_sda_DM_RES_UP);
```

Note For PSoC 4100 / PSoC 4200 I2C pins output enable is assigned to 0 to make High-Z state when I²C device does not drive the bus. This behavior suppresses usage of internal pull-ups (changing Drive Mode to Resistive pull-up has no effect). The external pull-ups must be used.

I2C APIs

Application Programming Interface (API) functions allow you to configure the Component using software. The following table lists and describes the interface to each function. The subsequent section discusses each function in more detail.

By default, PSoC Creator assigns the instance name “SCB_1” to the first instance of a Component in a given design. You can rename the instance to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is “SCB”.

Function	Description
SCB_Start()	Starts the SCB Component.
SCB_Init()	Initialize the SCB Component according to defined parameters in the customizer.
SCB_Enable()	Enables the SCB Component operation.
SCB_Stop()	Disable the SCB Component.
SCB_Sleep()	Prepares the SCB Component to enter Deep Sleep.
SCB_Wakeup()	Prepares Component for Active mode operation after Deep Sleep.
SCB_I2CInit()	Configures the SCB Component for operation in I2C mode. Only applicable when Component is in unconfigured mode.

Function	Description
SCB_I2CSlaveStatus()	Returns slave status flags.
SCB_I2CSlaveClearReadStatus()	Returns the slave read status flags and clears slave read status flags.
SCB_I2CSlaveClearWriteStatus()	Returns the slave write status and clears the slave write status flags.
SCB_I2CSlaveSetAddress()	Sets slave address, a value between 0 and 127 (0x00 to 0x7F).
SCB_I2CSlaveSetAddressMask()	Sets slave address mask, a value between 0 and 254 (0x00 to 0xFE).
SCB_I2CSlaveInitReadBuf()	Sets up the slave receive data buffer (master <- slave).
SCB_I2CSlaveInitWriteBuf()	Sets up the slave write buffer (master -> slave).
SCB_I2CSlaveGetReadBufSize()	Returns the number of bytes read by the master since SCB_I2CSlaveClearReadBuf() was called.
SCB_I2CSlaveGetWriteBufSize()	Returns the number of bytes written by the master since SCB_I2CSlaveClearWriteBuf() was called.
SCB_I2CSlaveClearReadBuf()	Resets the read buffer counter to zero.
SCB_I2CSlaveClearWriteBuf()	Resets the write buffer counter to zero.
SCB_I2CMasterStatus()	Returns the master status.
SCB_I2CMasterClearStatus()	Returns the master status and clears the status flags.
SCB_I2CMasterWriteBuf()	Writes the referenced data buffer to a specified slave address.
SCB_I2CMasterReadBuf()	Reads data from the specified slave address and places the data in the referenced buffer.
SCB_I2CMasterSendStart()	Generates a start condition and sends specified slave address.
SCB_I2CMasterSendRestart()	Generates a restart condition and sends specified slave address.
SCB_I2CMasterSendStop()	Generates a stop condition.
SCB_I2CMasterWriteByte()	Writes a single byte. This is a manual command that should only be used with the SCB_I2CMasterSendStart() or SCB_I2CMasterSendRestart() functions.
SCB_I2CMasterReadByte()	Reads a single byte. This is a manual command that should only be used with the SCB_I2CMasterSendStart() or SCB_I2CMasterSendRestart() functions.
SCB_I2CMasterGetReadBufSize()	Returns the number of bytes that have been transferred with the SCB_I2CMasterReadBuf() function.
SCB_I2CMasterGetWriteBufSize()	Returns the number of bytes that have been transferred with the SCB_I2CMasterWriteBuf() function.
SCB_I2CMasterClearReadBuf()	Resets the read buffer pointer back to the beginning of the buffer.
SCB_I2CMasterClearWriteBuf()	Resets the write buffer pointer back to the beginning of the buffer.

void SCB_Start(void)

Description: Invokes SCB_Init() and SCB_Enable(). After this function call the Component is enabled and ready for operation. This is the preferred method to begin Component operation.

When configuration is set to “Unconfigured SCB”, the Component must first be initialized to operate in one of the following configurations: I²C, SPI, UART or EZ I²C. Otherwise this function does not enable the Component.

void SCB_Init(void)

Description: Initializes SCB Component to operate in one of selected configurations: I²C, SPI, UART or EZ I²C.

When the configuration is set to “Unconfigured SCB”, this function does not do any initialization. Use mode-specific initialization APIs instead: SCB_I2CInit, SCB_SpiInit, SCB_UartInit or SCB_EzI2CInit.

void SCB_Enable(void)

Description: Enables SCB Component operation; activates the hardware and internal interrupt. It also restores TX interrupt sources disabled after the SCB_Stop() function was called (note that level-triggered TX interrupt sources remain disabled to not cause code lock-up).

For I²C and EZ I²C modes the interrupt is internal and mandatory for operation. For SPI and UART modes the interrupt can be configured as none, internal or external.

The SCB configuration should be not changed when the Component is enabled. Any configuration changes should be made after disabling the Component.

When configuration is set to “Unconfigured SCB”, the Component must first be initialized to operate in one of the following configurations: I²C, SPI, UART or EZ I²C, using the mode-specific initialization API. Otherwise this function does not enable the Component.

void SCB_Stop(void)

Description: Disables the SCB Component: disable the hardware and internal interrupt. It also disables all TX interrupt sources so as not to cause an unexpected interrupt trigger because after the Component is enabled, the TX FIFO is empty.

Refer to the function SCB_Enable() for the interrupt configuration details.

This function disables the SCB Component without checking to see if communication is in progress. Before calling this function it may be necessary to check the status of communication to make sure communication is complete. If this is not done then communication could be stopped mid byte and corrupted data could result.

void SCB_Sleep(void)

Description: Prepares the SCB Component to enter Deep Sleep.

The “Enable wakeup from Deep Sleep Mode” selection has an influence on this function implementation:

- Checked: configures the Component to be wakeup source from Deep Sleep.
- Unchecked: stores the current Component state (enabled or disabled) and disables the Component. See SCB_Stop() function for details about Component disabling.

Call the SCB_Sleep() function before calling the CyPmSysDeepSleep() function. Refer to the PSoC Creator *System Reference Guide* for more information about power management functions and *Low power* section of this document for the selected mode.

This function should not be called before entering Sleep.

void SCB_Wakeup(void)

Description: Prepares the SCB Component for Active mode operation after Deep Sleep.

The “Enable wakeup from Deep Sleep Mode” selection has influence on this function implementation:

- Checked: restores the Component Active mode configuration.
- Unchecked: enables the Component if it was enabled before enter Deep Sleep.

This function should not be called after exiting Sleep.

Side Effects: Calling the SCB_Wakeup() function without first calling the SCB_Sleep() function may produce unexpected behavior.

void SCB_I2CInit(SCB_I2C_INIT_STRUCT *config)

Description: Configures the SCB for I^2C operation.

This function is **intended specifically** to be used when the SCB configuration is set to “Unconfigured SCB” in the customizer. After initializing the SCB in I2C mode using this function, the Component can be enabled using the SCB_Start() or SCB_Enable() function.

This function uses a pointer to a structure that provides the configuration settings. This structure contains the same information that would otherwise be provided by the customizer settings.

Parameters: config: pointer to a structure that contains the following list of fields. These fields match the selections available in the customizer. Refer to the customizer for further description of the settings.

Field	Description
uint32 mode	Mode of operation for I2C. The following defines are available choices: • SCB_I2C_MODE_SLAVE • SCB_I2C_MODE_MASTER • SCB_I2C_MODE_MULTI_MASTER • SCB_I2C_MODE_MULTI_MASTER_SLAVE

uint32 oversampleLow	Oversampling factor for the low phase of the I²C clock. Ignored for Slave mode operation. The oversampling factors need to be chosen in conjunction with the clock rate in order to generate the desired rate of I²C operation.
uint32 oversampleHigh	Oversampling factor for the high phase of the I²C clock. Ignored for Slave mode operation.
uint32 enableMedianFilter	This field is left for compatibility and its value is ignored. Median filter is enabled or disabled depends on the data rate and operation mode.
uint32 slaveAddr	7-bit slave address. Ignored for non-slave modes.
uint32 slaveAddrMask	8-bit slave address mask. Bit 0 must have a value of 0. Ignored for non-slave modes.

Parameters (cont.) config :

Field	Description
uint32 acceptAddr	0 – disable 1 – enable When enabled the matching address is received into the RX FIFO. The callback function has to be registered to handle the address accepted in the RX FIFO. Refer to section Accept matching address RX FIFO for more information.
uint32 enableWake	0 – disable 1 – enable Ignored for non-slave modes.
uint8 enableByteMode	Ignored for all devices other than PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor 0 – disable 1 – enable When enabled the TX and RX FIFO depth is 16 bytes.
uint16 dataRate	Data rate in kbps used while the of I²C is in operation. Valid values are between 1 and 1000. Note This filed must be initialized for correct operation if Unconfigured SCB was utilized with previous version of the Component.
uint8 acceptGeneralAddr	0 – disable 1 – enable When enabled the I²C general call address (0x00) will be accepted by the I²C hardware and trigger an interrupt The callback function has to be registered to handle a general call address. Refer to section Accept General Call for more information.

uint32 SCB_I2CSlaveStatus(void)

Description: Returns the slave's communication status.

Return Value: uint32: Current status of I²C slave.

This status incorporates read and write status constants. Each constant is a bit field value. The value returned may have multiple bits set to indicate the status of the read or write transfer.

Slave Status constants	Description
SCB_I2C_SSTAT_RD_CMPLT	Slave read transfer complete. Set when master indicates it is done reading by sending a NAK [3]. The read error condition status bit must be checked to ensure that the read transfer was completed successfully.
SCB_I2C_SSTAT_RD_BUSY	Slave read transfer is in progress. Set when master addresses slave with a read, cleared when RD_CMPLT is set.
SCB_I2C_SSTAT_RD_OVFL	Master attempted to read more bytes than are in buffer. Slave continually returns 0xFF byte in this case.
SCB_I2C_SSTAT_RD_ERR	Slave captured error on the bus during a read transfer. The sources of error are: misplaced Start or Stop condition or lost arbitration while slave drives SDA.
SCB_I2C_SSTAT_WR_CMPLT	Slave write transfer complete. Set at reception of a Stop or ReStart condition. The write error condition status bit must be checked to ensure that write transfer was completed successfully.
SCB_I2C_SSTAT_WR_BUSY	Slave write transfer is in progress. Set when the master addresses the slave with a write, cleared when WR_CMPLT is set.
SCB_I2C_SSTAT_WR_OVFL	Master attempted to write past end of buffer. Further bytes are ignored.
SCB_I2C_SSTAT_WR_ERR	Slave captured error on the bus during write transfer. The sources of error are: misplaced Start or Stop condition or lost arbitration while slave drives SDA. The write buffer may contain invalid bytes or part of the data transfer when SCB_I2C_SSTAT_WR_ERR is set. It is recommended to discard write buffer content in this case.

[3] NAK is an abbreviation for negative acknowledgment or not acknowledged. I²C documents commonly use NACK while the rest of the networking world uses NAK. They mean the same thing.

uint32 SCB_I2CSlaveClearReadStatus(void)

Description: Clears the read status flags and returns their values. No other status flags are affected.

Return Value: uint32: Current read status of slave. See the SCB_I2CSlaveStatus() function for constants.

Side Effects: This function does not clear SCB_I2C_SSTAT_RD_BUSY.

uint32 SCB_I2CSlaveClearWriteStatus(void)

Description: Clears the write status flags and returns their values. No other status flags are affected.

Return Value: uint32: Current write status of slave. See the SCB_I2CSlaveStatus() function for constants.

Side Effects: This function does not clear SCB_I2C_SSTAT_WR_BUSY.

void SCB_I2CSlaveSetAddress(uint32 address)

Description: Sets the I^2C slave address

Parameters: uint32 address: I^2C slave address. This address is the 7-bit right-justified slave address and does not include the R/W bit.

The address value is not checked to see if it violates the I^2C spec. The preferred addresses are between 8 and 120 (0x08 to 0x78).

void SCB_I2CSlaveSetAddressMask(uint32 addressMask)

Description: Sets the I^2C slave address

Parameters: uint32 addressMask: I^2C slave address mask.

Bit value 0 – excludes bit from address comparison.

Bit value 1 – the bit needs to match with the corresponding bit of the I^2C slave address.

The range of valid values is between 0 and 254 (0x00 to 0xFE). The LSB of the address mask must be 0 because it corresponds to R/W bit within I^2C slave address byte.

void SCB_I2CSlaveInitReadBuf(uint8 * rdBuf, uint32 bufSize)

Description: Sets the buffer pointer and size of the read buffer. This function also resets the transfer count returned with the SCB_I2CSlaveGetReadBufSize() function.

Parameters: uint8* rdBuf: Pointer to the data buffer to be read by the master.

uint32 bufSize: Size of the buffer exposed to the I^2C master.

Side Effects: If this function is called during a bus transaction, data from the previous buffer location and the beginning of the current buffer may be transmitted.

void SCB_I2CSlaveInitWriteBuf(uint8 * wrBuf, uint32 bufSize)

Description: Sets the buffer pointer and size of the write buffer. This function also resets the transfer count returned with the SCB_I2CSlaveGetWriteBufSize() function.

Parameters: uint8* wrBuf: Pointer to the data buffer to be written by the master.

uint32 bufSize: Size of the write buffer exposed to the I²C master.

Side Effects: If this function is called during a bus transaction, data may be received in the previous buffer and the current buffer location.

uint32 SCB_I2CSlaveGetReadBufSize(void)

Description: Returns the number of bytes read by the I²C master since the SCB_I2CSlaveInitReadBuf() or SCB_I2CSlaveClearReadBuf() function was called.

The maximum return value is the size of the read buffer.

Return Value: uint32: Bytes read by master. If the transfer is not yet complete, it returns zero until transfer completion.

Side Effects: The returned value is not valid if SCB_I2C_SSTAT_RD_ERR was captured by the slave.

uint32 SCB_I2CSlaveGetWriteBufSize(void)

Description: Returns the number of bytes written by the I²C master since the SCB_I2CSlaveInitWriteBuf() or SCB_I2CSlaveClearWriteBuf() function was called.

The maximum return value is the size of the write buffer.

Return Value: uint32: Bytes written by master. If the transfer is not yet complete, it returns the byte count transferred so far.

Side Effects: The returned value is not valid if SCB_I2C_SSTAT_WR_ERR was captured by the slave.

void SCB_I2CSlaveClearReadBuf(void)

Description: Resets the read pointer to the first byte in the read buffer. The next byte read by the master will be the first byte in the read buffer.

void SCB_I2CSlaveClearWriteBuf(void)

Description: Resets the write pointer to the first byte in the write buffer. The next byte written by the master will be the first byte in the write buffer.

uint32 SCB_I2CMasterStatus(void)

Description: Returns the master's communication status.

Return Value: uint32: Current status of I²C master. This status incorporates status constants. Each constant is a bit field value. The value returned may have multiple bits set to indicate the status of the read or write transfer.

Master Status constants	Description
SCB_I2C_MSTAT_RD_CMPLT	Read transfer complete. The error condition status bits must be checked to ensure that read transfer was completed successfully.
SCB_I2C_MSTAT_WR_CMPLT	Write transfer complete. The error condition status bits must be checked to ensure that write transfer was completed successfully.
SCB_I2C_MSTAT_XFER_INP	Transfer in progress.
SCB_I2C_MSTAT_XFER_HALT	Transfer has been halted. The I²C bus is waiting for ReStart or Stop condition generation.
SCB_I2C_MSTAT_ERR_SHORT_XFER	**Error condition**: Write transfer completed before all bytes were transferred. The slave NAKed the byte which was expected to be ACKed.
SCB_I2C_MSTAT_ERR_ADDR_NAK	**Error condition:** Slave did not acknowledge address.
SCB_I2C_MSTAT_ERR_ARB_LOST	**Error condition**: Master lost arbitration during communications with slave.
SCB_I2C_MSTAT_ERR_BUS_ERROR	**Error condition**: bus error occurred during master transfer due to misplaced Start or Stop condition on the bus.
SCB_I2C_MSTAT_ERR_ABORT_XFER	**Error condition**: Slave was addressed by another master while master performed the start condition generation. As a result, master has automatically switched to slave mode and is responding. The master transaction has not taken place This error condition only applicable for Multi-Master-Slave mode.
SCB_I2C_MSTAT_ERR_XFER	**Error condition**: This is the ORed value of all error conditions provided above.

uint32 SCB_I2CMasterClearStatus(void)

Description: Clears all status flags and returns the master status.

Return Value: uint32: Current status of master. See the SCB_I2CMasterStatus() function for constants.

uint32 SCB_I2CMasterWriteBuf(uint32 slaveAddress, uint8 * wrData, uint32 cnt, uint32 mode)

Description: Automatically writes an entire buffer of data to a slave device. Once the data transfer is initiated by this function, further data transfer is handled by the included ISR.

Enables the I²C interrupt and clears SCB_ I2C_MSTAT_WR_CMPLT status.

Parameters: uint32 slaveAddress: Right-justified 7-bit Slave address (valid range 8 to 120).

uint8 wrData: Pointer to buffer of data to be sent.

uint32 cnt: Number of bytes of buffer to send.

uint32 mode: Transfer mode defines:

(1) Whether a start or restart condition is generated at the beginning of the transfer, and

(2) Whether the transfer is completed or halted before the stop condition is generated on the bus.

Transfer mode, mode constants may be ORed together.

Transfer Mode constants	Description
SCB_I2C_MODE_COMPLETE_XFER	Perform complete transfer from Start to Stop.
SCB_I2C_MODE_REPEAT_START	Send Repeat Start instead of Start. A Stop is generated after transfer is completed unless NO_STOP is specified.
SCB_I2C_MODE_NO_STOP	Execute transfer without a Stop. The following transfer expected to perform ReStart.

Return Value: **uint32**: Error status.

Error Status constants	Description
SCB_I2C_MSTR_NO_ERROR	Function complete without error. The master started the transfer.
SCB_I2C_MSTR_BUS_BUSY	Bus is busy. Nothing was sent on the bus. The attempt has to be retried.
SCB_I2C_MSTR_NOT_READY	Master is not ready for to start transfer. A master still has not completed previous transaction or a slave operation is in progress (in multi-master-slave configuration). Nothing was sent on the bus. The attempt has to be retried.

uint32 SCB_I2CMasterReadBuf(uint32 slaveAddress, uint8 * rdData, uint32 cnt, uint32 mode)

Description: Automatically reads an entire buffer of data from a slave device. Once the data transfer is initiated by this function, further data transfer is handled by the included ISR.

Enables the I²C interrupt and clears SCB_ I2C_MSTAT_RD_CMPLT status.

Parameters: uint32 slaveAddress: Right-justified 7-bit Slave address (valid range 8 to 120).

uint8 rdData: Pointer to buffer where to put data from slave.

uint32 cnt: Number of bytes of buffer to read.

uint32 mode: Transfer mode defines:

(1) Whether a start or restart condition is generated at the beginning of the transfer, and

(2) Whether the transfer is completed or halted before the stop condition is generated on the bus.

Transfer mode, mode constants may be ORed together. See SCB_I2CMasterWriteBuf() function for constants.

Return Value: uint32: Error status.

Error Status constants	Description
SCB_I2C_MSTR_NO_ERROR	Function complete without error. The master started the transfer.
SCB_I2C_MSTR_BUS_BUSY	Bus is busy. Nothing was sent on the bus. The attempt has to be retried.
SCB_I2C_MSTR_NOT_READY	Master is not ready for to start transfer. A master still has not completed previous transaction or a slave operation is in progress (in multi-master-slave configuration). Nothing was sent on the bus. The attempt has to be retried.

uint32 SCB_I2CMasterGetReadBufSize(void)

Description: Returns the number of bytes that has been transferred with an SCB_I2CMasterReadBuf() function.

Return Value: uint32: Byte count of transfer. If the transfer is not yet complete, it returns the byte count transferred so far.

Side Effects: This function returns an invalid value if SCB_I2C_MSTAT_ERR_ARB_LOST or SCB_I2C_MSTAT_ERR_BUS_ERROR occurred during the read transfer.

uint32 SCB_I2CMasterGetWriteBufSize(void)

Description: Returns the number of bytes that have been transferred with an SCB_I2CMasterWriteBuf() function.

Return Value: uint32: Byte count of transfer. If the transfer is not yet complete, it returns zero unit transfer completion.

Side Effects: This function returns an invalid value if SCB_I2C_MSTAT_ERR_ARB_LOST or SCB_I2C_MSTAT_ERR_BUS_ERROR occurred during the write transfer.

void SCB_I2CMasterClearReadBuf(void)

Description: Resets the read buffer pointer back to the first byte in the buffer.

void SCB_I2CMasterClearWriteBuf(void)

Description: Resets the write buffer pointer back to the first byte in the buffer.

uint32 SCB_I2CMasterSendStart(uint32 slaveAddress, uint32 bitRnW)

Description: Generates Start condition and sends slave address with read/write bit. Disables the I^2C interrupt.

This function is blocking. It does not return until the Start condition and address byte are sent, a ACK/NAK is received, or errors have occurred.

Parameters: uint32 slaveAddress: Right justified 7-bit Slave address (valid range 8 to 120).

uint32 bitRnW: Direction of the following transfer. It is defined by read/write bit within address byte.

Direction constants	Description
SCB_I2C_WRITE_XFER_MODE	Set write direction for the following transfer.
SCB_I2C_READ_XFER_MODE	Set read direction for the following transfer.

Return Value: uint32: Error status.

Error Status constants	Description
SCB_I2C_MSTR_NO_ERROR	Function complete without error.
SCB_I2C_MSTR_BUS_BUSY	Bus is busy. Nothing was sent on the bus. The attempt has to be retried.
SCB_I2C_MSTR_NOT_READY	Master is not ready for to start transfer. A master still has not completed previous transaction or a slave operation is in progress (in multi-master-slave configuration). Nothing was sent on the bus. The attempt has to be retried.
SCB_I2C_MSTR_ERR_LB_NAK	**Error condition**: Last byte was NAKed.
SCB_I2C_MSTR_ERR_ARB_LOST	**Error condition**: Master lost arbitration.
SCB_I2C_MSTR_ERR_BUS_ERR	**Error condition**: Master encountered a bus error. Bus error is misplaced start or stop detection.
SCB_I2C_MSTR_ERR_ABORT_START	**Error condition**: The start condition generation was aborted due to beginning of Slave operation. This error condition is only applicable for Multi-Master-Slave mode.

uint32 SCB_I2CMasterSendRestart(uint32 slaveAddress, uint32 bitRnW)

Description: Generates ReStart condition and sends slave address with read/write bit.

If the last transaction was a read the NAK is sent before the ReStart to complete the transaction.

This function is blocking and does not return until the ReStart condition and address are sent, a ACK/NAK is received, or errors have occurred.

Parameters: uint32 slaveAddress: Right-justified 7-bit Slave address (valid range 8 to 120).

uint32 bitRnW: Direction of the following transfer. It is defined by read/write bit within address byte. See SCB_I2CMasterSendStart() function for constants.

Return Value: uint32: Error status. See SCB_I2CMasterSendStart() function for constants.

Side Effects: A valid Start or ReStart condition must be generated before calling this function. This function does nothing if Start or ReStart conditions failed before this function was called.

For read transaction, at least one byte has to be read before ReStart generation.

uint32 SCB_I2CMasterSendStop(void)

Description: Generates Stop condition on the bus. The NAK is generated before Stop in case of a read transaction.

At least one byte has to be read if a Start or ReStart condition with read direction was generated before.

This function is blocking and does not return until a Stop condition is generated or error occurred.

Return Value: uint32: Error status. See the SCB_MasterSendStart() command for constants.

Side Effects: A valid Start or ReStart condition must be generated before calling this function. This function does nothing if Start or ReStart condition failed before this function was called.

For read transaction, at least one byte has to be read before Stop generation.

uint32 SCB_I2CMasterWriteByte(uint32 theByte)

Description: Sends one byte to a slave.

This function is blocking and does not return until the byte is transmitted or an error occurs.

Parameters: uint32 theByte: Data byte to send to the slave.

Return Value: uint32: Error status.

Error Status constants	Description
SCB_I2C_MSTR_NO_ERROR	Function complete without error.
SCB_I2C_MSTR_NOT_READY	Master is not active master on the bus. A Slave operation may be in progress. Nothing was sent on the bus. The attempt has to be retried.
SCB_I2C_MSTR_ERR_LB_NAK	**Error condition**: Last byte was NAKed.
SCB_I2C_MSTR_ERR_ARB_LOST	**Error condition**: Master lost arbitration.
SCB_I2C_MSTR_ERR_BUS_ERR	**Error condition**: Master encountered a bus error. Bus error is misplaced start or stop detection.

Side Effects: A valid Start or ReStart condition must be generated before calling this function. This function does nothing if Start or ReStart conditions failed before this function was called.

uint32 SCB_I2CMasterReadByte(uint32 ackNack)

Description: Reads one byte from a slave and generates ACK or prepares to generate NAK. The NAK will be generated before Stop or ReStart condition by SCB_I2CMasterSendStop() or SCB_I2CMasterSendRestart() function appropriately.

This function is blocking. It does not return until a byte is received or an error occurs.

Parameters: uint32 ackNack: Response to received byte.

Response constants	Description
SCB_I2C_ACK_DATA	Generates ACK. The master notifies slave that transfer continues.
SCB_I2C_NAK_DATA	Prepares to generate NAK. The master will notify slave that transfer is completed.

Return Value: uint32: Byte read from the slave. In case of error the MSB of returned data is set to 1.

Side Effects: A valid Start or ReStart condition must be generated before calling this function. This function does nothing and returns invalid byte value if Start or ReStart conditions failed before this function was called.

Global Variables

Knowledge of these variables is not required for normal operations.

Variable	Description
SCB_initVar	SCB_initVar indicates whether the SCB Component has been initialized. The variable is initialized to 0 and set to 1 the first time SCB_Start() is called. This allows the Component to restart without reinitialization after the first call to the SCB_Start() routine. If reinitialization of the Component is required, then the SCB_Init() function can be called before the SCB_Start() or SCB_Enable() function.

I2C Function Appliance

Function	Slave	Master	Multi-Master	Multi-Master-Slave
SCB_I2CInit()	+	+	+	+
SCB_I2CSlaveStatus()	+	–	–	+
SCB_I2CSlaveClearReadStatus()	+	–	–	+
SCB_I2CSlaveClearWriteStatus()	+	–	–	+
SCB_I2CSlaveSetAddress()	+	–	–	+
SCB_I2CSlaveSetAddressMask()	+	–	–	+
SCB_I2CSlaveInitReadBuf()	+	–	–	+
SCB_I2CSlaveInitWriteBuf()	+	–	–	+
SCB_I2CSlaveGetReadBufSize()	+	–	–	+
SCB_I2CSlaveGetWriteBufSize()	+	–	–	+
SCB_I2CSlaveClearReadBuf()	+	–	–	+
SCB_I2CSlaveClearWriteBuf()	+	–	–	+
SCB_I2CMasterStatus()	–	+	+	+
SCB_I2CMasterClearStatus()	–	+	+	+
SCB_I2CMasterWriteBuf()	–	+	+	+
SCB_I2CMasterReadBuf()	–	+	+	+
SCB_I2CMasterSendStart()	–	+	+	+
SCB_I2CMasterSendRestart()	–	+	+	+
SCB_I2CMasterSendStop()	–	+	+	+
SCB_I2CMasterWriteByte()	–	+	+	+
SCB_I2CMasterReadByte()	–	+	+	+

Function	Slave	Master	Multi-Master	Multi-Master-Slave
SCB_I2CMasterGetReadBufSize()	–	+	+	+
SCB_I2CMasterGetWriteBufSize()	–	+	+	+
SCB_I2CMasterClearReadBuf()	–	+	+	+
SCB_I2CMasterClearWriteBuf()	–	+	+	+

Bootloader Support

The SCB Component in I²C mode can be used as a communication Component for the Bootloader. You should use the following configurations to support communication protocol from an external system to the Bootloader:

- Mode: Slave or Multi-Master-Slave
- Data Rate: Must match Host (boot device) data rate
- Slave Address: Must match Host (boot device) selected slave address

For more information about the Bootloader, refer to the Bootloader Component datasheet.

The following API functions are provided for Bootloader use.

Function	Description
SCB_CyBtldrCommStart()	Starts the I²C Component and enables its interrupt.
SCB_CyBtldrCommStop()	Disable the I²C Component and disables its interrupt.
SCB_CyBtldrCommReset()	Sets read and write I²C buffers to the initial state and resets the slave status.
SCB_CyBtldrCommRead()	Allows the caller to read data from the bootloader host (the host writes the data).
SCB_CyBtldrCommWrite()	Allows the caller to write data to the bootloader host (the host writes the data).

void SCB_CyBtldrCommStart(void)

Description: Starts the I²C Component and enables its interrupt.

Every incoming I²C write transaction is treated as a command for the bootloader.

Every incoming I²C read transaction returns 0xFF until the bootloader provides a response to the executed command.

void SCB_CyBtldrCommStop(void)

Description: Disables the I²C Component and disables its interrupt.

void SCB_CyBtldrCommReset(void)

Description: Sets read and write I²C buffers to the initial state and resets the slave status.

cystatus SCB_CyBtldrCommRead(uint8 pData[], uint16 size, uint16 * count, uint8 timeOut)

Description: Allows the caller to read data from the bootloader host (the host writes the data). The function handles polling to allow a block of data to be completely received from the host device.

Parameters: uint8 pData[]: Pointer to the block of data to be read from bootloader host.

uint16 size: Number of bytes to be read from bootloader host.

uint16 *count: Pointer to variable to write the number of bytes actually read by the bootloader host.

uint8 timeOut: Number of units in 10 ms to wait before returning because of a timeout.

Return Value: cystatus: Returns CYRET_SUCCESS if no problem was encountered or returns the value that best describes the problem. For more information, refer to the “Return Codes” section of the *System Reference Guide*.

cystatus SCB_CyBtldrCommWrite(const uint8 pData[], uint16 size, uint16 * count, uint8 timeOut)

Description: Allows the caller to write data to the bootloader host (the host reads the data). The function does not use timeout and returns after data has been copied into the slave read buffer. This data available to be read by the bootloader host until following host data write.

Parameters: const uint8 pData[]: Pointer to the block of data to send to the bootloader host.

uint16 size: Number of bytes to send to bootloader host.

uint16 *count: Pointer to variable to write the number of bytes actually written to the bootloader host.

uint8 timeOut: The timeout is not used by this function. The function returns as soon as data is copied into the slave read buffer.

Return Value: cystatus: Returns CYRET_SUCCESS if no problem was encountered or returns the value that best describes the problem. For more information refer to the “Return Codes” section of the *System Reference Guide*.

I2C Functional Description

This Component supports I²C Slave, Master, Multi-Master, and Multi-Master-Slave configurations. The following sections provide an overview of how to use the Component in these configurations.

This Component requires that you enable global interrupts since the I²C hardware is interrupt-driven. Even though this Component requires interrupts, you do not need to add any code to the ISR (interrupt service routine). The Component services all interrupts (data transfers) independent of your code. The memory buffers allocated for this interface look like simple dual-port memory between your application and the I²C master/slave.

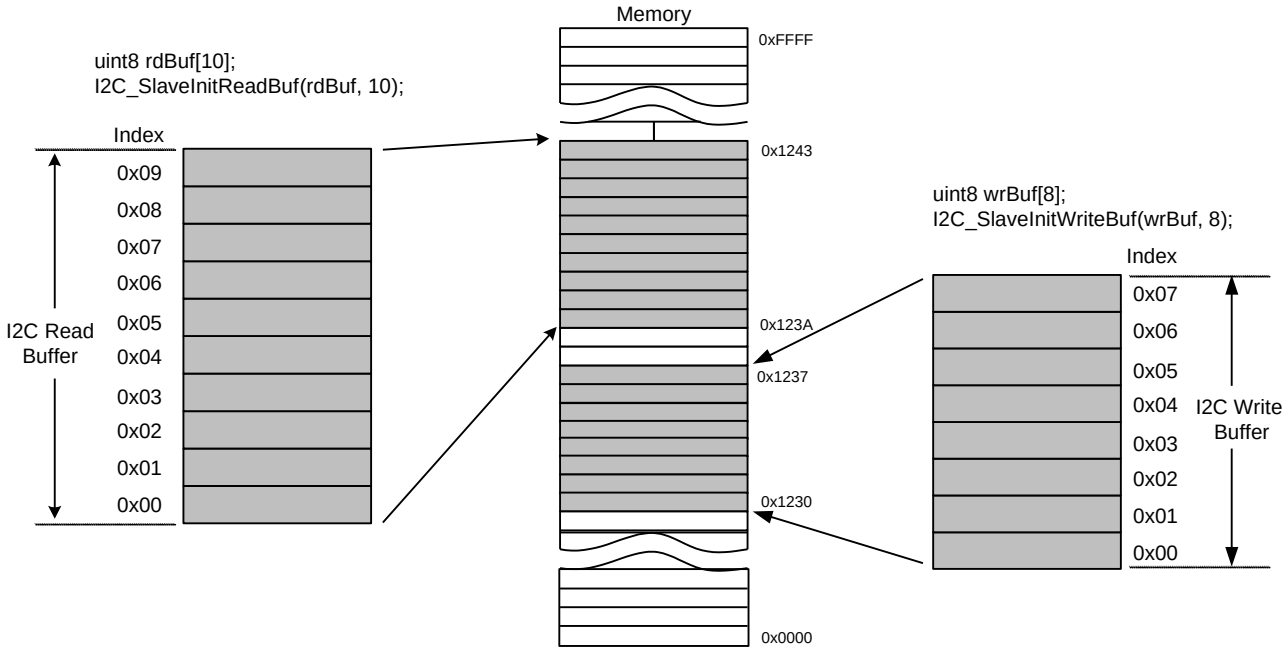
Slave Operation

The slave interface consists of two buffers in memory, one for data written to the slave by a master and a second buffer for data read by a master from the slave. Remember that reads and writes are from the perspective of the I²C master. The I²C slave read and write buffers are set by the initialization commands below. These commands do not allocate memory, but instead copy the array pointer and size to the internal Component variables. You must instantiate the arrays used for the buffers because they are not automatically generated by the Component. The same buffer may be used for both read and write buffers, but you must be careful to manage the data properly.

```
void SCB_I2CSlaveInitReadBuf(uint8 * rdBuf, uint32 bufSize)
void SCB_I2CSlaveInitWriteBuf(uint8 * wrBuf, uint32 bufSize)
```

Using the functions above sets a pointer and byte count for the read and write buffers. The bufSize for these functions may be less than or equal to the actual array size, but it should never be larger than the available memory pointed to by the rdBuf or wrBuf pointers.

Figure 2. Slave Buffer Structure



When the SCB_I2CSlaveInitReadBuf() or SCB_I2CSlaveInitWriteBuf() function is called, the internal index is set to the first value in the array pointed to by rdBuf and wrBuf, respectively. As bytes are read or written by the I²C master, the index is incremented until the offset is one less than the bufSize. At any time the number of bytes transferred may be queried by calling either SCB_I2CSlaveGetReadBufSize() or SCB_I2CSlaveGetWriteBufSize() for the read and write buffers, respectively. Reading or writing more bytes than are in the buffers causes an overflow. The overflow status is set in the slave status byte and may be read with the SCB_I2CSlaveStatus() API.

To reset the index back to the beginning of the array, use the following commands:

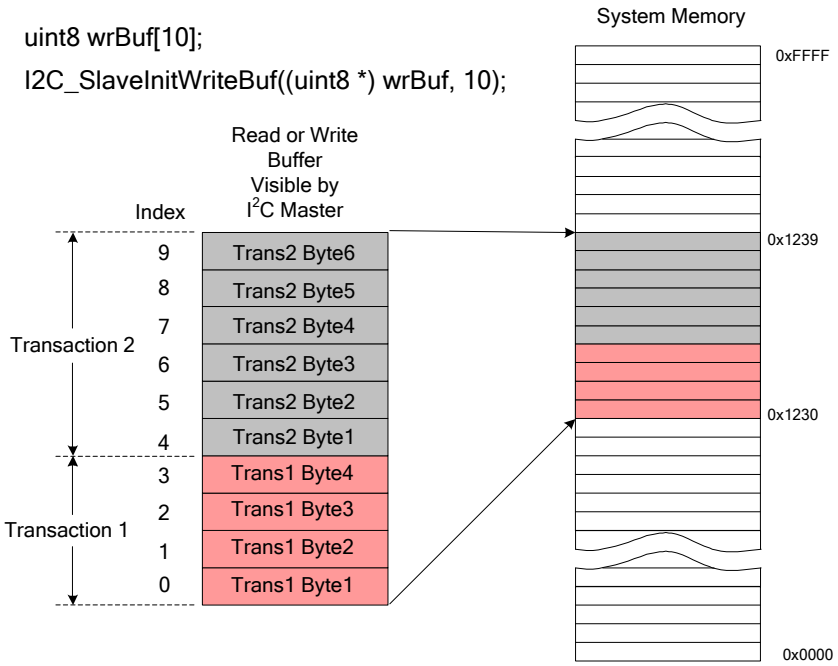
```
void SCB_I2CSlaveClearReadBuf(void)
void SCB_I2CSlaveClearWriteBuf(void)
```

This resets the index back to zero. The next byte read or written by the I²C master is the first byte in the array. Before these clear buffer commands are used, the data in the arrays should be read or updated.

Multiple reads or writes by the I²C master continue to increment the array index until the clear buffer commands are used or the array index attempts to grow beyond the array size. Figure 3 shows an example where an I²C master has executed two write transactions. The first write was four bytes and the second write was six bytes. The sixth byte in the second transaction was NAKed by the slave to signal that the end of the buffer had occurred. If the master tried to write a seventh byte for the second transaction or started to write more bytes with a third transaction, each byte would be NAKed and discarded until the buffer is reset.

Using the SCB_I2CSlaveClearWriteBuf() function after the first transaction resets the index back to zero and causes the second transaction to overwrite the data from the first transaction. Make sure data is not lost by overflowing the buffer. The data in the buffer should be processed by the slave before resetting the buffer index.

Figure 3. System Memory



Both the read and write buffers have four status bits to signal transfer complete, transfer in progress, and buffer overflow. When a transfer starts, the busy flag is set. When the transfer is complete, the transfer complete flag is set and the busy flag is cleared. If a second transfer is started, both the busy and transfer complete flags may be set at the same time. The following table shows read and write status flags.

Slave Status Constants	Description
SCB_I2C_SSTAT_RD_CMPLT	Slave read transfer complete.
SCB_I2C_SSTAT_RD_BUSY	Slave read transfer in progress (busy).
SCB_I2C_SSTAT_RD_OVFL	Master attempted to read more bytes than are in buffer.
SCB_I2C_SSTAT_RD_ERR	Slave captured error on the bus while read transfer.
SCB_I2C_SSTAT_WR_CMPLT	Slave write transfer complete.
SCB_I2C_SSTAT_WR_BUSY	Slave Write transfer in progress (busy).
SCB_I2C_SSTAT_WR_OVFL	Master attempted to write past end of buffer.
SCB_I2C_SSTAT_WR_ERR	Slave captured error on the bus while write transfer.

The following code example initializes the write buffer then waits for a transfer to complete. Once the transfer is complete, the data is then copied into a working array to handle the data. In many applications, the data does not have to be copied to a second location, but instead can be processed in the original buffer. You could create an almost identical read buffer example by replacing the write functions and constants with read functions and constants. Processing the data may mean new data is transferred into the slave buffer instead of out.

```
uint8 wrBuf[10u];
uint8 userArray[10u];
uint32 byteCnt;
uint32 status;

/* Initialize write buffer before call SCB_Start */
SCB_I2CSlaveInitWriteBuf((uint8 *) wrBuf, 10u);

/* Start I2C Slave operation */
SCB_Start();

/* The code below is not protected from the interruption. This might be required
to not cause buffer update by the following I2C write transaction while it is
handled.*/

/* Wait for I2C master to complete a write */

status = SCB_I2CSlaveStatus();
if(0u != (status & SCB_I2C_SSTAT_WR_CMPLT))
{
    if(0u == (status & SCB_I2C_SSTAT_WR_ERR))
    {
        byteCnt = SCB_I2CSlaveGetWriteBufSize();
        for(i=0; i < byteCnt; i++)
        {
            userArray[i] = wrBuf[i]; /* Copy data to local array */
        }
    }
    /* Clean-up status and buffer pointer */
    SCB_I2CSlaveClearWriteStatus();
    SCB_I2CSlaveClearWriteBuf();
}
```

Multiple address support

The I²C slave Component is able to support more than a single slave address. Multiple slave addresses are handled by a user written callback function that is registered with the Component. Whenever an address is received, the hardware will stretch the clock while the user callback function is called. The callback function is responsible for evaluating the received address and returning an ACK or NACK depending on whether or not the address is valid. This is also an opportunity for the application to store the received address and change I²C buffer pointers based on the received address, if needed. Once the callback function returns, the hardware will handle performing the ACK or NACK on the I²C bus depending on the return value from the callback function.

The callback function is registered with the Component using the SCB_SetI2cAddressCustomInterruptHandler() function by passing a pointer to the callback function as an argument. If the function is not registered, all accepted addresses are ACKed but the same I²C buffer will be used for all I²C communication.

The Component provides two options to enable multiple addresses reception: accept matching address RX FIFO and accept general call. The following chapters describe the usage of these options.

Accept matching address RX FIFO

The I²C slave has two settings to configure the slave address: slave address and mask. The slave address defines a specific slave address while the mask defines a range of accepted addresses. This range may differ from a single address to 128 different addresses. The accepted addresses are called matched as they match acceptance criteria. Refer to section Slave address mask for more information on how to configure the slave address and mask to accept more than a single slave address.

Enabling the “Accept matching address RX FIFO” option in the I2C Basic Tab allows an application to evaluate two or more slave addresses. This option forces the Component to place all matched addresses in the RX FIFO and call the user defined custom callback function, which is responsible for evaluating the matched address and deciding whether the address should be ACK’d or NACK’d and perform any additional address specific processing.

The following code provides an example of custom function which handles two address addresses (7-bits): 0x24 and 0x30. The slave address is 0x24 (7-bits) and slave mask is 0xD6 (8-bits). The accepted matched addresses (7-bits) are 0x20, 0x30, 0x24 and 0x34.

```
/* Address 1 read and write buffers */
#define ADDR1_BUFFER_SIZE   (10u)
uint8 addr1BufRead[ADDR1_BUFFER_SIZE];
uint8 addr1BufWrite[ADDR1_BUFFER_SIZE];

/* Address 2 read and write buffers */
#define ADDR2_BUFFER_SIZE   (20u)
uint8 addr2BufRead[ADDR2_BUFFER_SIZE];
uint8 addr2BufWrite[ADDR2_BUFFER_SIZE];

/* Store the address which was more recently accessed */
uint8 activeAddress;
#define I2C_SLAVE_ADDRESS1  (0x24u)
#define I2C_SLAVE_ADDRESS2  (0x34u)

uint32 AddressAccepted(void)
{
    uint32 response;

    /* Set default response as NAK */
    response = SCB_I2C_NAK_ADDR;

    /* Read 7-bits right justified slave address */
    activeAddress = SCB_GET_I2C_7BIT_ADDRESS(SCB_RX_FIFO_RD_REG);
```

```
    switch(activeAddress)
    {
        case (I2C_SLAVE_ADDRESS1):
            /* Address 1: Setup buffers for read and write */
            SCB_I2CSlaveInitReadBuf (addr1BufRead, ADDR1_BUFFER_SIZE);
            SCB_I2CSlaveInitWriteBuf(addr1BufWrite, ADDR1_BUFFER_SIZE);

            response = SCB_I2C_ACK_ADDR;
            break;

        case (I2C_SLAVE_ADDRESS2):
            /* Address 2: Setup buffers for read and write */
            SCB_I2CSlaveInitReadBuf (addr2BufRead, ADDR2_BUFFER_SIZE);
            SCB_I2CSlaveInitWriteBuf(addr2BufWrite, ADDR2_BUFFER_SIZE);

            response = SCB_I2C_ACK_ADDR;
            break;

        default:
            /* NAK all other accepted addresses.
            * The SCB_I2C_SSTAT_WR_CMPLT or SCB_I2C_SSTAT_RD_CMPLT flags are not
            * affected when address is NACKed */
            break;
    }

    return (response);
}


int main()
{
    /* Register address callback function */
    SCB_SetI2cAddressCustomInterruptHandler(&AddressAccepted);

    /* Start I2C slave operation */
    SCB_Start();

    CyGlobalIntEnable;

    for(;;)
    {
        if (0u != (SCB_I2CSlaveStatus() & SCB_I2C_SSTAT_WR_CMPLT))
        {
            if (I2C_SLAVE_ADDRESS1 == activeAddress)
            {
                /* Handle slave address 1: master writes */
            }
            else
            {
                /* Handle slave address 2: master writes */
            }

            /* Clean-up status and buffer pointer */
            SCB_I2CSlaveClearWriteBuf();
```

```
            SCB_I2CSlaveClearWriteStatus();
        }

        if (0u != (SCB_I2CSlaveStatus() & SCB_I2C_SSTAT_RD_CMPLT))
        {
            if (I2C_SLAVE_ADDRESS1 == activeAddress)
            {
                /* Handle slave address 1: master reads */
            }
            else
            {
                /* Handle slave address 2: master reads */
            }

            /* Clean-up status and buffer pointer */
            SCB_I2CSlaveClearReadBuf();
            SCB_I2CSlaveClearReadStatus();
        }
    }
}
```

Note All slave functions return the values related to the most recent slave address which was accessed by the master.

Note Any slave matched address wakes device from deep sleep independently whether it will be ACKed or NACKed.

Accept General Call

The general call address is used for addressing every device connected to the I²C-bus at the same time. In the default I²C configuration, the I²C slave ignores the general call address and will generate a NAK response. Enabling the “Accept general call address” option in the I2C Basic Tab forces the Component to accept the general call address and will call the user generated custom callback function after an address (the specific slave address or general call address) is received. The interrupt source SCB_INTR.SLAVE_I2C_GENERAL notifies that general call address is received.

The following code provides an example of a custom function which handles the general call address and a single slave address.

```
/* Slave read and write buffers */
#define SLAVE_BUFFER_SIZE   (10u)
uint8 slaveBufWrite[SLAVE_BUFFER_SIZE];
uint8 slaveBufRead[SLAVE_BUFFER_SIZE];

/* Gen call write buffer */
#define GEN_CALL_BUFFER_SIZE   (2u)
uint8 genCallBufWrite[GEN_CALL_BUFFER_SIZE];

/* Store the address which was more recently accessed */
uint8 activeAddress;
#define I2C_SLAVE_ADDRESS           (SCB_I2C_SLAVE_ADDRESS)
#define I2C_GENERAL_CALL_ADDRESS    (0x00u)
```

```
uint32 AddressAccepted(void)
{
    uint32 response;

    /* ACK slave address or general call address access */
    response = SCB_I2C_ACK_ADDR;

    /* Prepare for general call address */
    if (0u != (SCB_GetSlaveInterruptSourceMasked() & SCB_INTR_SLAVE_I2C_GENERAL))
    {
        /* Setup only write buffer as R/W bit is always 0 */
        SCB_I2CSlaveInitWriteBuf(genCallBufWrite, GEN_CALL_BUFFER_SIZE);

        /* Set active address to be general call */
        activeAddress = I2C_GENERAL_CALL_ADDRESS;
    }
    /* Prepare for slave address access */
    else
    {
        /* Restore slave write buffer */
        SCB_I2CSlaveInitWriteBuf(slaveBufWrite, SLAVE_BUFFER_SIZE);

        /* Set active address to be slave address */
        activeAddress = I2C_SLAVE_ADDRESS;
    }

    return (response);
}

int main()
{
    /* Register address callback function */
    SCB_SetI2cAddressCustomInterruptHandler(&AddressAccepted);

    /* Start I2C slave operation */
    SCB_Start();

    CyGlobalIntEnable;

    for(;;)
    {
        if (0u != (SCB_I2CSlaveStatus() & SCB_I2C_SSTAT_WR_CMPLT))
        {
            if (I2C_SLAVE_ADDRESS == activeAddress)
            {
                /* Handle slave address: master writes */
            }
            else
            {
                /* Handle general call address: master writes */
            }

            /* Clean-up status and buffer pointer */
            SCB_I2CSlaveClearWriteBuf();
```

```
                SCB_I2CSlaveClearWriteStatus();
            }
        }
    }
```

Note All slave functions return the values related to the most recent slave address which was accessed by the master.

Note The general call address wakes up the device from deep sleep.

Master/Multi-Master Operation

Master and Multi-Master operation are basically the same, with two exceptions. When operating in Multi-Master mode, the bus should always be checked to see if it is busy. Another master may already be communicating with another slave. In this case, the program must wait until the current operation is complete before issuing a start transaction. The program looks at the return value, which sets a busy status if another master has control of the bus.

The second difference is that, in Multi-Master mode, two masters can start at the exact same time. If this happens, one of the two masters loses arbitration. You must check for this condition after each byte is transferred. The Component automatically checks for this condition and responds with an error if arbitration is lost.

There are two options when operating the I^2C master: manual and automatic. In automatic mode, a buffer is created to hold the entire transfer. In the case of a write operation, the buffer is prefilled with the data to be sent. If data is to be read from the slave, a buffer at least the size of the packet needs to be allocated. To write an array of bytes to a slave in automatic mode, use the following function.

```
uint32 SCB_I2CMasterWriteBuf(uint32 slaveAddress, uint8 * wrData, uint32 cnt,
uint32 mode)
```

The slaveAddress variable is a right-justified 7-bit slave address of 0 to 127. The Component API automatically appends the write flag to the LSb of the address byte. The array of data to transfer is pointed to with the second parameter, wrData. The cnt parameter is the number of bytes to transfer. The last parameter, mode, determines how the transfer starts and stops. A transaction may begin with a restart instead of a start, or halt before the stop sequence. These options allow back-to-back transfers where the last transfer does not send a stop and the next transfer issues a restart instead of a start.

A read operation is almost identical to the write operation. The same parameters with the same constants are used.

```
uint32 SCB_I2CMasterReadBuf(uint32 slaveAddress, uint8 * rdData, uint32 cnt,
uint32 mode);
```

Both of these functions return status. See the status table for the SCB_I2CMasterStatus() function return value. Since the read and write transfers complete in the background during the I^2C interrupt code, the SCB_I2CMasterStatus() function can be used to determine when the transfer is complete. A code snippet that shows a typical write to a slave follows.

```
SCB_I2CMasterClearStatus(); /* Clear any previous status */
SCB_I2CMasterWriteBuf(8u, (uint8 *) wrData, 10u, SCB_I2C_MODE_COMPLETE_XFER);
for(;;)
{
   if(0u != (SCB_I2CMasterStatus() & SCB_I2C_MSTAT_WR_CMPLT))
   {

      /* Transfer complete. Check Master status to make sure that transfer
         completed without errors. */

      break;
   }
}
```

The I²C master can also be operated manually. In this mode, each part of the write transaction is performed with individual commands.

```
status = SCB_I2CMasterSendStart(8u, SCB_I2C_WRITE_XFER_MODE);
if(SCB_I2C_MSTR_NO_ERROR == status)   /* Check if transfer completed without
errors */
{
   /* Send array of 5 bytes */
   for(i=0; i<5u; i++)
   {
      status = SCB_I2CMasterWriteByte(userArray[i]);
      if(SCB_I2C_MSTR_NO_ERROR != status)
      {
         break;
      }
   }
}
SCB_I2CMasterSendStop();      /* Send Stop */
```

A manual read transaction is similar to the write transaction except the last byte should be NAKed. The example below shows a typical manual read transaction.

```
status = SCB_I2CMasterSendStart(8u, SCB_I2C_READ_XFER_MODE);
if(SCB_I2C_MSTR_NO_ERROR == status)   /* Check if transfer completed without
errors */
{
   /* Read array of 5 bytes */
   for(i=0; i<5u; i++)
   {
      if(i < 4u)
      {
         userArray[i] = SCB_I2CMasterReadByte(SCB_I2C_ACK_DATA);
      }
      else
      {
         userArray[i] = SCB_I2CMasterReadByte(SCB_I2C_NAK_DATA);
      }
   }
}
SCB_I2CMasterSendStop();    /* Send Stop */
```

Multi-Master-Slave Mode Operation

Both Multi-Master and Slave are operational in this mode. The Component may be addressed as a slave, but firmware may also initiate master mode transfers. In this mode, when a master loses arbitration during an address byte, the slave hardware checks which winning master addressed it. In case of an address match, the slave becomes active.

For Master and Slave operation examples look at the Slave Operation and Master sections.

Note The master and slave share the same SCB hardware block. The master cannot address its own slave because the hardware and firmware cannot run both roles simultaneously. Any attempt to do this will cause unpredictable behavior. You must not allow the master address its own slave.

Low power modes

The Component in I²C mode is able to be a wakeup source from Sleep and Deep Sleep low power modes.

Sleep mode is identical to Active from a peripheral point of view. No configuration changes are required in the Component or code before entering/exiting sleep. Any communication intended to the slave causes an interrupt to occur and leads to wakeup. Any master activity that involves an interrupt to occur leads to wakeup.

Master modes (Master, Multi-Master) are not able to be a wakeup source from Deep Sleep. This capability is only available for slave modes (Slave, Multi-Master-Slave). The slave has to be configured properly to enable this functionality. The “Enable wakeup from Deep Sleep Mode” must be checked in the I2C configuration dialog. The SCB_Sleep() and SCB_Wakeup() functions must be called before/after entering/exiting Deep Sleep.

The wakeup event is a slave address match. The externally clocked logic performs address matching, when the address matches an interrupt request is generated, thus waking up the device. The slave stretches the SCL line until control is passed to its interrupt routine to ACK the address. The wakeup interrupt source is disabled in the interrupt handler or by SCB_Wakeup() after address match has occurred.

Before entering Deep Sleep, the ongoing transaction intended for the slave has to be completed. The following code is suggested:

```
/* Enter critical section to lock the slave state */
uint8 intState = CyEnterCriticalSection();

/* Check if slave is busy */
status = (SCB_I2CSlaveStatus() & (SCB_I2C_SSTAT_RD_BUSY | SCB_I2C_SSTAT_WR_BUSY));

if (0u == status)
{
    /* Slave is not busy: enter Deep Sleep */
    SCB_Sleep();      /* Configure the slave to be wakeup source */
```

```
        CySysPmDeepSleep();

        /* Exit critical section to continue slave operation */
        CyExitCriticalSection(intState);
        SCB_Wakeup();     /* Configure the slave to active mode operation */
    }
    else
    {
        /* Slave is busy. Do not enter Deep Sleep.           */
        /* Exit critical section to continue slave operation */
        CyExitCriticalSection(intState);
    }
```

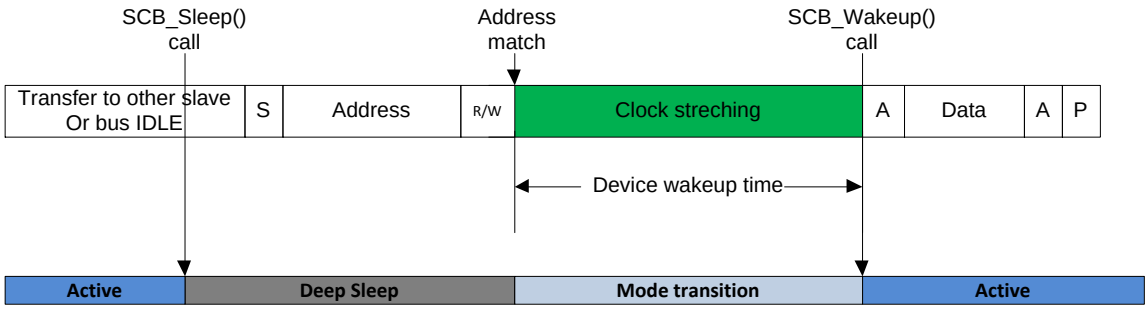
For devices **other than** PSoC 4100 / PSoC 4200, the **Component clock** must be disabled before calling SCB_Sleep(), and then enabled after calling SCB_Wakeup(); otherwise, the SCL will lock up after wakeup from Deep Sleep. Disabling and re-enabling the Component clock is managed by the SCB_Sleep() and SCB_Wakeup() APIs when the Clock from terminal option is disabled. Otherwise, when the Clock from terminal option is enabled, the code provided above requires modification to enable and disable the clock source connected to the SCB Component. Review the following modified code and highlighted in blue (ScbClock – the instance name of clock Component connected to the SCB):

```
    if(0u == status)
    {
        SCB_Sleep();     /* Configure the slave to be wakeup source */
        ScbClock_Stop(); /* Disable the SCB clock */
        CySysPmDeepSleep();

        /* Exit critical section to continue slave operation */
        CyExitCriticalSection(intState);
        SCB_Wakeup();     /* Configure the slave to active mode operation */
        ScbClock _Start(); /* Enable the SCB clock */
    }
```

For devices **other than** PSoC 4100 / PSoC 4200 configured in Multi-Master-Slave mode only, in order for the Component to be a wake-up source from deep sleep, the configuration of the Component must be changed before deep sleep and after the part wakes from deep sleep. This configuration change occurs automatically in the SCB_Sleep() function, and any function that starts an I^2C master transaction. During this configuration change the Component is disabled. After the configuration has been changed, it is re-enabled. During the time it is disabled, any incoming addresses to the slave will be NAKed; the external master will have to retry to access the slave.

Figure 4. Master transaction wakes up device on slave address match



Data rate configuration

For correct operation of I²C mode the Component must meet the data rate requirement of the connected I²C bus. For master mode this means the master data rate cannot be faster than the slowest slave in the system. For slave mode this means the slave cannot be slower than the fastest master in the system.

For slave mode the frequency of the connected clock source is the only parameter used in determining the maximum data rate the slave can operate at. The connected clock is the clock that runs the SCB, not SCL. The frequency of the connected clock source must be fast enough to provide enough oversampling of the SCL and SDA signals to ensure that all I²C specifications are meet. Table 2 provides the ranges of allowed clock frequencies for the standard I²C data rates (Standard Mode, Fast Mode, and Fast-mode Plus). There are two ways to control the frequency of the connected clock for slave mode:

1. Use a clock Component that is internal to the SCB Component (this clock still uses clock divider resources). Based on the data rate set in the GUI the Component asks PSoC Creator to create a clock with a frequency in the range provided in Table 2 on page 16.
2. Connect a user configurable clock to the SCB Component. This option is enabled by checking the “Clock from terminal” control. In this mode it is the user’s responsibility to ensure the connected clock frequency is in the range provided in Table 2 on page 16. If the frequency is not in that range then proper I2C operation is no longer guaranteed.

Independent of the chosen method the Component will display the actual data rate. This is the maximum data rate at which the slave can operate. If the system data rate is faster than the displayed actual data rate correct I²C operation is no longer guaranteed.

For I²C master mode the data rate is determined by the connected Component clock, and the oversampling factor. These two factors are used to set the frequency of SCL, one SCL period is equal to the period of the connected clock multiplied by the oversampling factor. The oversampling factor is divided into low and high to enable independent control of the high and low phases of SCL. The low and high oversampling factor can be configured independently but their sum has to be equal to overall oversampling. In order to ensure that the master meets all I²C specifications the connected clock frequency and oversampling factor must be within a specified range. Table 3 on page 16 provides a range of clock frequencies and oversampling factors for the standard I²C data rates.

The Component provides three methods to configure data rate:

1. Set the desired data rate and disable Manual oversampling control. This option uses a clock Component that is internal to the SCB Component (this clock still uses clock divider resources). Based on the data rate set in the GUI the Component asks PSoC Creator to create a clock with a frequency in the range provided in Table 3 on page 16. When available clock frequency is returned the oversampling factors low and high are calculated to meet the set data rate, and the oversampling ranges provided in Table 3 on page 16.
2. Select desired data rate and enable Manual oversampling control. This option uses a clock Component that is internal to the SCB Component (this clock still uses clock divider resources). The Component asks PSoC Creator to create a clock frequency equal to desired (Data rate * Oversampling). The oversampling is controlled by the user. This method is left to provide backward compatibility with previous versions of Component.
3. Connect a user configurable clock to the SCB Component. This option is enabled by checking the “Clock from terminal” control. The user still uses the GUI to configure the oversampling factor low and high. This method provides full control of the data rate configuration.

Independent of chosen method the Component displays actual data rate for Master. This data rate might differ from the observed data rate on the bus due to the t_R and t_F time.

I²C spec parameters calculation

The ranges provided in Table 3 on page 16 assume worst case conditions on the bus; often a bus will never experience worst case conditions. The following section describes how to calculate various I²C parameters based on the connected clock frequency and oversampling factors. This information can be used to determine if the chosen connected clock frequency and oversampling factor meet I²C specifications on your I²C bus.

To find the frequency of the connected clock open the PSoC Creator Design-Wide Resources (DWR) file, and open the Clock Tab. If you used an internal clock look for a clock name that contains the Component instance name with the suffix “_SCBCLK”. If you used the clock from terminal option, look for the name of your clock. The Nominal frequency has to be taken but it might differ from the Desired frequency due to design clock configuration.

Also the clock accuracy should be taken to account. The master device generates f_{SCL} with the accuracy of the provided clock source. Therefore when maximum data rate (for selected data rate mode) is used the slave has to tolerate this inaccuracy otherwise the f_{SCL} has to be reduced or more accurate clock source provided.

The slave device is less sensitive to clock accuracy than the master as only when clock frequency is close to low or high limit (for the selected data rate mode) is provided the clock source accuracy has to be taken into account. The clock should not run too slow due negative deviation as well as too fast due to positive deviation. The slave has wide range of allowed clocks therefore selecting clock frequency in range (low limit + negative deviation) to (high limit – positive deviation) eliminates effect of the clock source accuracy.

For master modes Table 3 on page 16 contains the ranges of clock frequencies for the selected data rate. Keeping the clock frequency within these ranges ensures that $t_{VD;DAT}$ and $t_{VD;ACK}$ parameters from I^2C spec are met.

For Data rates of 0-400 kbps:

$$t_{VD;DAT} = (3/ f_{SCBCLK}) + t_{R_0\%_70\%} + 90 \text{ nsec}$$

For Data rates of 401-1000 kbps:

$$t_{VD;DAT} = (4/ f_{SCBCLK}) + t_{R_0\%_70\%}$$

Note $t_{R_0\%_70\%}$ is the rising time from 0% to 70% to be measured for specific I^2C bus.

Note The same equation applies for $t_{VD;ACK}$

Meeting $t_{VD;DAT}$ parameter ensures that $t_{SU;DAT}$ parameters is also met.

Meeting t_{LOW} and t_{HIGH} parameter ensures that t_{BUF}, $t_{SU;STA}$, $t_{HD;STA}$ and $t_{SU;STO}$ parameters are also met. To calculate t_{LOW} and t_{HIGH} the use following equation:

$$t_{LOW} = ((1/ f_{SCBCLK}) * \text{Oversampling factor Low}) – t_F$$

$$t_{HIGH} = ((1/ f_{SCBCLK}) * \text{Oversampling factor High}) – t_R$$

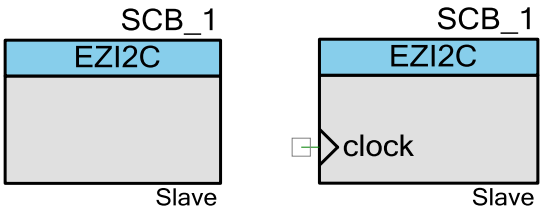
f_{SCBCLK} is a frequency of the connected Component clock; Oversampling factor Low and High are parameters of the Component.

Note The t_F and t_R values have to be measured for specific I^2C bus.

Note Calculated t_{HIGH} value might be less than observed on the bus due to clock synchronization in the device. The device resets its internal counter of t_{HIGH} when it detects a low level on SCL line while expecting high level. Therefore when t_R and internal device delay is greater than one Component clock period – t_{HIGH} is extended. This causes the data rate to be less than expected.

For the slave mode the Table 2 on page 16 contains the ranges of clock frequencies for the selected data rate. Keep the clock frequency within these ranges to ensure that the slave meets all parameters of I^2C specification.

EZI2C [4]



The I²C bus is an industry standard, two-wire hardware interface developed by Philips®. The master initiates all communication on the I²C bus and supplies the clock for all slave devices. The EZI2C Slave implements an I²C register-based slave device. It is compatible [1] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I2C-bus specification.

The EZI2C Slave is a unique implementation of an I²C slave in that all communication between the master and slave is handled in the ISR (Interrupt Service Routine) and requires no interaction with the main program flow. The interface appears as shared memory between the master and slave. Once the EZI2C_Start() function is called, there is little need to interact with the API.

Input/Output Connections

This section describes the various input and output connections for the SCB Component. An asterisk (*) in the list of terminals indicates that the terminal may be hidden on the symbol under the conditions listed in the description of that terminal.

clock – Input*

Clock that operates this block. The presence of this terminal varies depending on the Clock from terminal parameter.

Internal Pins Configuration

The I²C SCL and SDA pins are buried inside Component: SCB_scl and SCB_sda. These pins are buried because they use dedicated connections and are not routable as general purpose signals. Refer to the *I/O System* section in the device *Technical Reference Manual (TRM)* for more information.

Note The instance name is not included into the Pin Names provided in the following table.

---

4 This is a firmware implementation of the EZI2C protocol on top of I2C (non-EZ mode). All communication between the master and slave is handled in the ISR (Interrupt Service Routine). The data buffer has to be allocated in the RAM. The SCB Component does not support EZI2C (EZ-mode), which uses a 32-bytes hardware buffer.

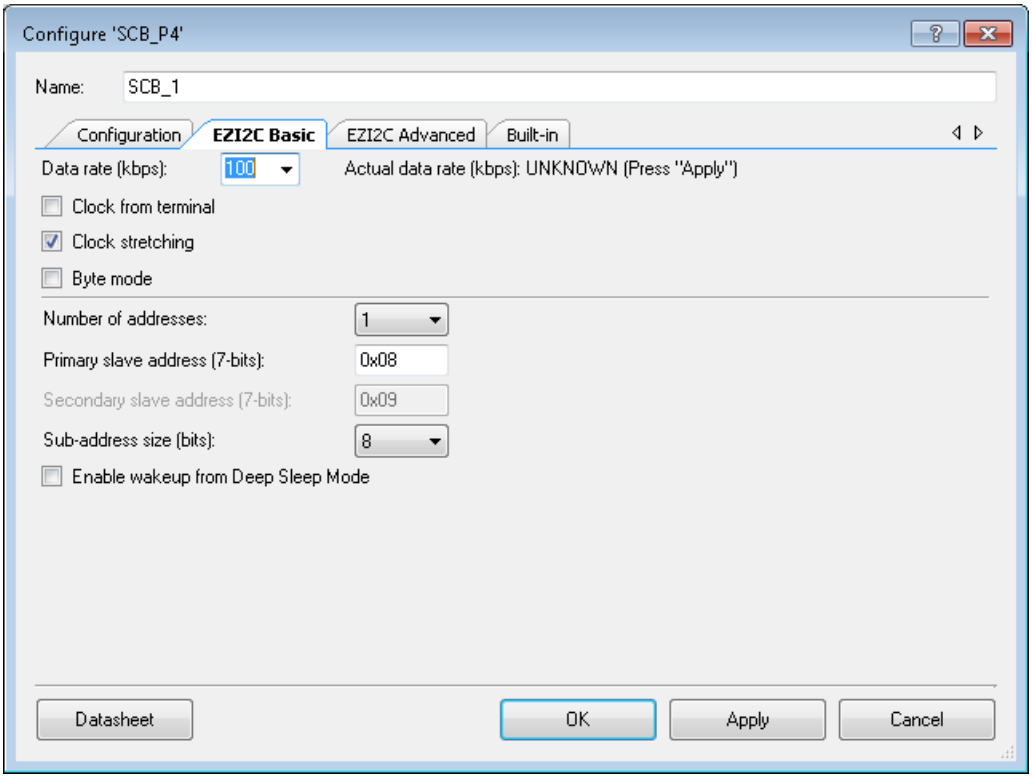
Table 6. I2C Pins Configuration

Pin Name	Direction	Drive Mode	Initial Drive State	Threshold	Slew Rate	Descriptiion
scl	Bidirectional	Open Drain Drives Low	High	CMOS	Fast	Serial clock (SCL) is the master-generated I2C clock. This pins configuration requires connection of external pulls on the I2C bus. The other option is applying internal pull-ups which is described in the Internal Pull-Ups section. For PSoC 4100 / PSoC 4200 devices I^2C pins output enable is assigend to 0 to make High-Z state when I^2C device does not drive the bus. This behaviour supresses usage of internal pull-ups (changing Drive Mode to Resistive pull-up has no effect). For other devices: I^2C pins output enable tied to 1 and pin state depends on drive mode and output signal. The internal pull-ups can be used
sda	Bidirectional	Open Drain Drives Low	High	CMOS	Fast	Serial data (SDA) is the I2C data pin. This pins configuration requires connection of external pulls on the I2C bus. The other option is applying internal pull-ups which is described in the Internal Pull-Ups section. For PSoC 4100 / PSoC 4200 devices I^2C pins output enable is assigend to 0 to make High-Z state when I^2C device does not drive the bus. This behaviour supresses usage of internal pull-ups (changing Drive Mode to Resistive pull-up has no effect). For other devices: I^2C pins output enable tied to 1 and pin state depends on pin's drive mode and output signal. The internal pull-ups can be used.

The Input threshold level CMOS should be used for the vast majority of application connections. The Output slew rate can be changed use Slew rate parameter. The other Input and Output pin's parameters are set to default. Refer to pin Component datasheet for more information about parameters values.

To change I^2C pins configuration the pin's Component APIs should be used or direct pin registers configuration. For example refer to the Internal Pull-Ups section.

Basic EZI2C Parameters



The **EZI2C Basic** tab has the following parameters:

Data rate

This parameter is used to set the I^2C data rate value up to 1000 kbps (400 kbps for PSoC 4000 family); the actual data rate may differ from the selected data rate due to available clock frequency. The standard data rates are 100 (default), 400, and 1000 kbps. The **Data rate** is limited to a maximum of 400 kbps if the **Clock stretching** option is disabled. This parameter has no effect if the **Clock from terminal** parameter is enabled.

Actual data rate

Actual data rate displays the data rate at which the Component will operate with current settings. The selected data rate could be different from actual data rate. The factors that affect the actual data rate calculation are: system clock and accuracy of the Component clock (internal or external). When a change is made to any of the Component parameters that affect the actual data rate, it becomes unknown. To calculate the new actual data rate press the Apply button.

Note The actual data rate always provides maximum value for the selected data rate mode (Standard-mode (100 kbps), Fast-mode (400 kbps), Fast-mode Plus (1000 kbps)).

Clock from terminal

This parameter allows choosing between an internally configured clock (by the Component) or an externally configured clock (by the user) for the Component operation.

When this control is enabled, the Component does not control the data rate, but displays the actual data rate based on the user-connected clock source frequency. When this control is not enabled, the clock configuration is provided by the Component. The clock source frequency is selected by the Component based on the Data rate parameter. The table below shows the valid ranges for the Component clock for each data rate. When using clock from terminal ensure that the external clock is within these ranges.

Table 7. EZI2C Slave clock frequency ranges

Parameter	Standard-mode (0-100 kbps)		Fast-mode (0-400 kbps)		Fast-mode Plus (0-1000 kbps)		Units
	Min	Max	Min	Max	Min	Max	
f_{SCB}	1.55	12.8	7.82	15.38	15.84	48.0	MHz

Note When the clock frequency is less than the lower limit of 1.55 MHz, an error is generated while building the project.

Note PSoC Creator is responsible for providing requested clock frequency (internal or external clock) based on current design clock configuration. When the requested clock frequency with requested tolerance cannot be created, a warning about the clock accuracy range is generated while building the project. This warning contains the actual clock frequency value created by PSoC Creator. To remove this warning you must either change the system clock, Component settings or external clock to fit the clocking system requirements.

Clock stretching

This parameter applies clock stretching on the SCL line if the EZ I^2C slave is not ready to respond. Enabling this option ensures consistent slave operation for any EZ I^2C slave interrupt latency because the I^2C transaction is paused by clock stretching. Without the clock stretching option enabled, the design needs to service the EZ I^2C slave interrupt fast enough to provide correct slave operation.

Byte mode

This option is only applicable for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices. It allows doubling the TX and RX FIFO depth from 8 to 16 bytes. Increasing the FIFO depth improves performance of EZ I^2C operation when clock stretching is enabled, as more bytes can be transmitted or received without software interaction. This option does not improve EZ I^2C operation when clock stretching is disabled; therefore, it is not available for this mode.

Number of addresses

This option determines whether 1 (default) or 2 independent I^2C slave addresses are recognized. If two addresses are recognized, then address detection will be performed in software. When the **Clock Stretching** option is **disabled**, the number of address choices is restricted to 1.

Primary slave address (7-bits)

This is an I^2C address that will be recognized by the slave as the primary address. This address is the 7-bit right-justified slave address and does not include the R/W bit. A slave address between 0x08 and 0x7F may be selected; the default is 0x08.

The value may be entered as decimal or hexadecimal; for hexadecimal numbers type ‘0x’ before the address.

Secondary slave address (7-bits)

This is an I^2C address that will be recognized by the slave as the secondary address. This address is the 7-bit right-justified slave address and does not include the R/W bit. A slave address between 0x08 and 0x7F may be selected; the default is 0x09. Refer to Preferable Secondary Address Choice.

The value may be entered as decimal or hexadecimal; for hexadecimal numbers type ‘0x’ before the address.

Sub-address size

This option determines what range of data can be accessed. You can select a sub-address of 8 bits (default) or 16 bits. If you use a sub-address size of 8 bits, the master can only access data offsets between 0 and 255. You may also select a sub-address size of 16 bits. That will allow the I^2C master to access data arrays of up to 65,535 bytes.

Enable wakeup from Deep Sleep Mode

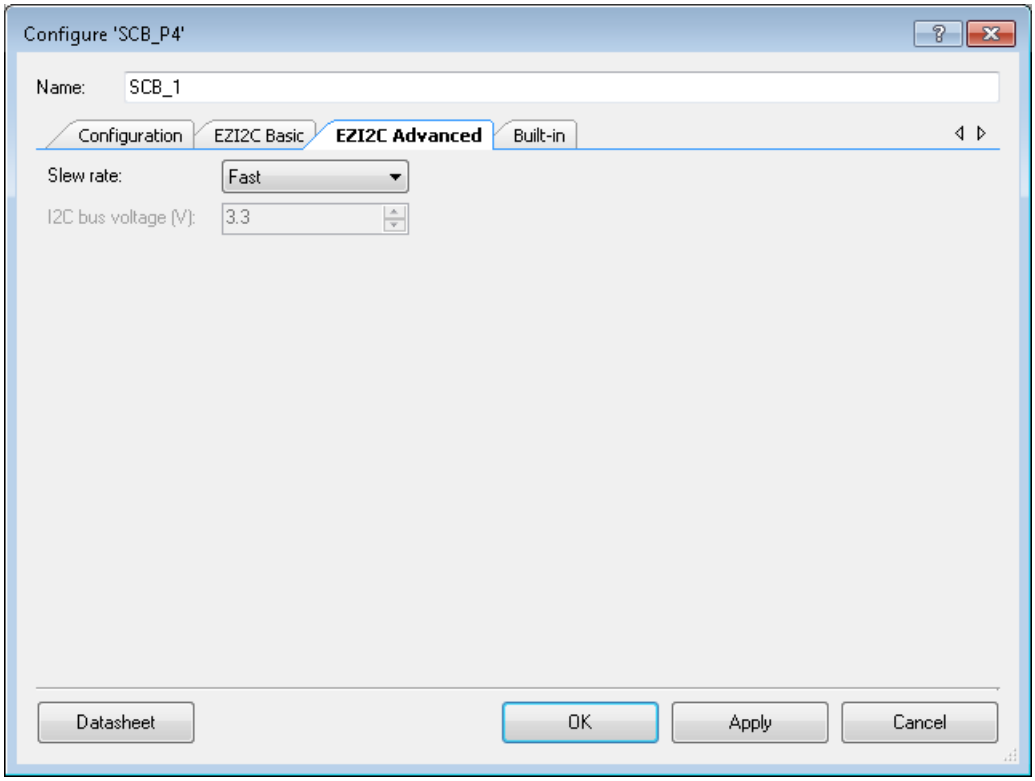
Use this option to enable the Component to wake the system from Deep Sleep when a slave address match occurs.

Enabling this option adds the following restrictions (only for PSoC 4100/PSoC 4200 devices):

- Clock stretching must be enabled
- Slave address (7-bits) must be even (bit 0 equal zero)

Refer to the Low power modes section in the EZI2C chapter of this document and *Power Management APIs* section of the *System Reference Guide* for more information.

Advanced EZI2C Parameters



The **EZI2C Advanced** tab contains the following parameters:

Slew rate

This option allows to control slew rate setting of the SCL and SDA pins. The slow slew rate increases the fall time on the lines, reducing EMI and coupling with neighboring signals. For devices supporting GPIO Over-Voltage Tolerance (GPIO_OVT) pins, I2C FM+ options should be used when I^2C data rate is greater than 400 kbps. This option also requires the I2C bus voltage to be defined. Refer to the *Device Datasheet* to determine which pins are GPIO_OVT capable. Default is fast.

Notes

- GPIO_OVT pins are fully compliant with the I^2C specification but the slew rate must be set appropriately:
  - **Slew rate** "Slow" for Standard mode (100 kbps) and Fast mode (400 kbps)
  - **Slew rate** "I2C FM+" for Fast mode plus (1 Mbps)

  Common GPIO pins are not completely compliant with the I^2C specification. Refer to the *Device Datasheet* for the details.
- **Slew rate** settings are applied to all pins of the associated port.

I2C bus voltage (V)

This option is only applicable for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L devices. It specifies the voltage applied to the I^2C pull up resistors when Slew rate is I2C FM+. The voltage no less than applied to I^2C pulls up resistors must be provided by the V_{DDD} supply input, otherwise the I^2C pins cannot be placed. Valid values of V_{DDD} are determined by the settings in the Design-Wide Resources System Editor (in the *<project>.cydwr* file). This range check is performed outside this dialog; the results appear in the Notice List window if the check fails. Default is 3.3 V.

External Electrical Connections

Refer to the External Electrical Connections section for I^2C.

Internal pull ups

Refer to the Internal Pull-Ups section for I^2C.

EZI2C APIs

Application Programming Interface (API) functions allow you to configure the Component using software. The following table lists and describes the interface to each function. The subsequent section discusses each function in more detail.

By default, PSoC Creator assigns the instance name “SCB_1” to the first instance of a Component in a given design. You can rename the instance to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is “SCB”.

Function	Description
SCB_Start()	Starts the SCB Component.
SCB_Init()	Initialize the SCB Component according to defined parameters in the customizer.
SCB_Enable()	Enables the SCB Component operation.
SCB_Stop()	Disable the SCB Component.
SCB_Sleep()	Prepares the SCB Component to enter Deep Sleep.
SCB_Wakeup()	Prepares Component for Active mode operation after Deep Sleep.
SCB_EzI2CInit()	Configures the SCB Component for operation in EZ I^2C mode. Only applicable when the Component is in unconfigured mode.
SCB_EzI2CGetActivity()	Returns EZ I^2C slave status.
SCB_EzI2CSetAddress1()	Sets the primary EZ I^2C slave address.
SCB_EzI2CGetAddress1()	Returns the primary EZ I^2C slave address.

Function	Description
SCB_EzI2CSetBuffer1()	Sets up the data buffer to be exposed to the I²C master on a primary slave address request.
SCB_EzI2CSetReadBoundaryBuffer1()	Sets the read only boundary of the data buffer to be exposed by I²C master by the primary address request.
SCB_EzI2CSetAddress2()	Sets the secondary EZ I²C slave address.
SCB_EzI2CGetAddress2()	Returns the secondary EZ I²C slave address.
SCB_EzI2CSetBuffer2()	Sets up the data buffer to be exposed to the I²C master on a secondary slave address request.
SCB_EzI2CSetReadBoundaryBuffer2()	Sets the read boundary of the data buffer to be exposed by I²C master by the secondary address request.

void SCB_Start(void)

Description: Invokes SCB_Init() and SCB_Enable(). After this function call the Component is enabled and ready for operation. This is the preferred method to begin Component operation.

When configuration is set to “Unconfigured SCB”, the Component must first be initialized to operate in one of the following configurations: I²C, SPI, UART or EZ I²C. Otherwise this function does not enable Component.

void SCB_Init(void)

Description: Initializes the SCB Component to operate in one of the selected configurations: I²C, SPI, UART or EZ I²C.

When configuration set to “Unconfigured SCB”, this function does not do any initialization. Use mode-specific initialization APIs instead: SCB_I2CInit, SCB_SpiInit, SCB_UartInit or SCB_EzI2CInit.

void SCB_Enable(void)

Description: Enables SCB Component operation; activates the hardware and internal interrupt. It also restores TX interrupt sources disabled after the SCB_Stop() function was called (note that level-triggered TX interrupt sources remain disabled to not cause code lock-up).

For I²C and EZ I²C modes the interrupt is internal and mandatory for operation. For SPI and UART modes the interrupt can be configured as none, internal or external.

The SCB configuration should be not changed when the Component is enabled. Any configuration changes should be made after disabling the Component.

When configuration is set to “Unconfigured SCB”, the Component must first be initialized to operate in one of the following configurations: I²C, SPI, UART or EZ I²C, Using the mode-specific initialization API. Otherwise this function does not enable the Component.

void SCB_Stop(void)

Description: Disables the SCB Component: disable the hardware and internal interrupt. It also disables all TX interrupt sources so as not to cause an unexpected interrupt trigger because after the Component is enabled, the TX FIFO is empty.

Refer to the function SCB_Enable() for the interrupt configuration details.

This function disables the SCB Component without checking to see if communication is in progress. Before calling this function it may be necessary to check the status of communication to make sure communication is complete. If this is not done then communication could be stopped mid byte and corrupted data could result.

void SCB_Sleep(void)

Description: Prepares Component to enter Deep Sleep.

The “Enable wakeup from Deep Sleep Mode” selection has an influence on this function implementation:

- Checked: configures the Component to be wakeup source from Deep Sleep.
- Unchecked: stores the current Component state (enabled or disabled) and disables the Component. See SCB_Stop() function for details about Component disabling.

Call the SCB_Sleep() function before calling the CyPmSysDeepSleep() function. Refer to the PSoC Creator *System Reference Guide* for more information about power management functions.

This function should not be called before entering Sleep.

void SCB_Wakeup(void)

Description: Prepares Component to Active mode operation after Deep Sleep.

The “Enable wakeup from Deep Sleep Mode” selection influences this function implementation:

- Checked: restores the Component Active mode configuration.
- Unchecked: enables the Component if it was enabled before enter Deep Sleep.

This function should not be called after exiting Sleep.

Side Effects: Calling the SCB_Wakeup() function without first calling the SCB_Sleep() function may produce unexpected behavior.

void SCB_EzI2CInit(SCB_EZI2C_INIT_STRUCT *config)

Description: Configures the SCB for EZ I²C operation.

This function is **intended specifically** to be used when the SCB configuration is set to "Unconfigured SCB" in the customizer. After initializing the SCB in EZ I²C mode, the Component can be enabled using the SCB_Start() or SCB_Enable() function.

This function uses a pointer to a structure that provides the configuration settings. This structure contains the same information that would otherwise be provided by the customizer settings.

Parameters: config: pointer to a structure that contains the list of fields. These fields match the selections available in the customizer. Refer to the customizer for further description of the settings.

Field	Description
uint32 enableClockStretch	0 – disable 1 – enable When enabled the SCL is stretched as required for proper operation.
uint32 enableMedianFilter	This field is left for compatibility and its value is ignored. Median filter is disabled for EZI2C mode.
uint32 numberOfAddresses	Number of supported addresses: SCB_EZI2C_ONE_ADDRESS SCB_EZI2C_TWO_ADDRESSES
uint32 primarySlaveAddr	Primary 7-bit slave address.
uint32 secondarySlaveAddr	Secondary 7-bit slave address.
uint32 subAddrSize	Size of sub-address: SCB_EZI2C_SUB_ADDR8_BITS SCB_EZI2C_SUB_ADDR16_BITS
uint32 enableWake	0 – disable 1 – enable When enabled the matching address generates a wakeup request.
uint8 enableByteMode	Ignored for all devices other than PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor. 0 – disable 1 – enable When enabled the TX and RX FIFO depth is 16 bytes.

uint32 SCB_EzI2CGetActivity(void)

Description: Returns EZ I²C slave status.

The read, write and error status flags reset to zero after this function call.

The busy status flag is cleared when the transaction intended for the EZ I²C slave completes.

This function disables EZ I²C slave interrupt during execution to operate correctly. This may have significant impact to correctness of EZ I²C slave operation when the clock stretching option is disabled. The amount of time that the interrupt is disabled should be less than the maximum EZ I²C slave interrupt latency. Refer to section Clock Stretching Disable for more details.

Return Value: uint32: Current status of EZ I²C slave.

This status incorporates a number of status constants. Each constant is a bit field value. The value returned may have multiple bits set to indicate the status of the transfer.

Slave Status Constants	Description
SCB_EZI2C_STATUS_READ1	Read transfer complete. The transfer used the primary slave address. The error condition status bit must be checked to ensure that read transfer was completed successfully.
SCB_EZI2C_STATUS_WRITE1	Write transfer complete. The buffer content was modified. The transfer used the primary slave address. The error condition status bit must be checked to ensure that write transfer was completed successfully.
SCB_EZI2C_STATUS_READ2	Read transfer complete. The transfer used the secondary slave address. The error condition status bit must be checked to ensure that read transfer was completed successfully.
SCB_EZI2C_STATUS_WRITE2	Write transfer complete. The buffer content was modified. The transfer used the secondary slave address The error condition status bit must be checked to ensure that write transfer was completed successfully.
SCB_EZI2C_STATUS_BUSY	A transfer intended for the primary or secondary address is in progress. The status bit is set after an address match and cleared on a Stop or ReStart condition.
SCB_EZI2C_STATUS_ERR	An error occurred during a transfer intended for the primary or secondary slave address. The sources of error are: misplaced Start or Stop condition or lost arbitration while slave drives SDA. The write buffer may contain invalid byte or part of the transaction when SCB_EZI2C_STATUS_ERR and SCB_EZI2C_STATUS_WRITE1/2 is set. It is recommended to discard buffer content in this case.

void SCB_EzI2CSetAddress1(uint32 address)

Description: Sets the primary EZ I²C slave address.

Parameters: uint32 address: primary I²C slave address.

This address is the 7-bit right-justified slave address and does not include the R/W bit.

The address value is not checked to see if it violates the I²C spec. The preferred addresses are in the range between 8 and 120 (0x08 to 0x78).

uint32 SCB_EzI2CGetAddress1(void)

Description: Returns primary the EZ I²C slave address.

This address is the 7-bit right-justified slave address and does not include the R/W bit.

Return Value: uint32: Primary I²C slave address.

void SCB_EzI2CSetBuffer1(uint32 bufSize, uint32 rwBoundary, volatile uint8 * buffer)

Description: Sets up the data buffer to be exposed to the I²C master on a primary slave address request.

Parameters: uint32 bufSize: Size of the data buffer in bytes.

uint32 rwBoundary: number of data bytes starting from the beginning of the buffer with read and write access. Data bytes located at offset rwBoundary or greater are read only.

This value must be less than or equal to the buffer size.

uint8* buffer: Pointer to the data buffer.

Side Effects: Calling this function in the middle of a transaction intended for the primary slave address leads to unexpected behavior.

void SCB_EzI2CSetReadBoundaryBuffer1(uint32 rwBoundary)

Description: Sets the read only boundary in the data buffer to be exposed to the I²C master on a primary slave address request.

Parameters: uint32 rwBoundary: number of data bytes starting from the beginning of the buffer with read and write access. Data bytes located at offset rwBoundary or greater are read only.

This value must be less than or equal to the buffer size.

Side Effects: Calling this function in the middle of a transaction intended for the primary slave address leads to unexpected behavior.

void SCB_EzI2CSetAddress2(uint32 address)

Description: Sets the secondary EZ I²C slave address.

Parameters: uint32 address: secondary I²C slave address.

This address is the 7-bit right-justified slave address and does not include the R/W bit.

The address value is not checked to see if it violates the I2C spec. The preferred addresses are in the range between 8 and 120 (0x08 to 0x78).

uint32 SCB_EzI2CGetAddress2(void)

Description: Returns the secondary EZ I²C slave address.

This address is the 7-bit right-justified slave address and does not include the R/W bit.

Return Value: uint32: Secondary I²C slave address.

void SCB_EzI2CSetBuffer2(uint32 bufSize, uint32 rwBoundary, volatile uint8 * buffer)

Description: Sets up the data buffer to be exposed to the I²C master on a secondary slave address request.

Parameters: uint32 bufSize: Size of the data buffer in bytes.

uint32 rwBoundary: number of data bytes starting from the beginning of the buffer with read and write access. Data bytes located at offset rwBoundary or greater are read only.

This value must be less than or equal to the buffer size.

uint8* buffer: Pointer to the data buffer.

Side Effects: Calling this function in the middle of a transaction intended for the secondary slave address leads to unexpected behavior.

void SCB_EzI2CSetReadBoundaryBuffer2(uint32 rwBoundary)

Description: Sets the read only boundary in the data buffer to be exposed to the I²C master on a secondary address request.

Parameters: uint32 rwBoundary: number of data bytes starting from the beginning of the buffer with read and write access. Data bytes located at offset rwBoundary or greater are read only.

This value must be less than or equal to the buffer size.

Side Effects: Calling this function in the middle of a transaction intended to the secondary slave address leads to unexpected behavior.

Global Variables

Knowledge of these variables is not required for normal operations.

Variable	Description
SCB_initVar	SCB_initVar indicates whether the SCB Component has been initialized. The variable is initialized to 0 and set to 1 the first time SCB_Start() is called. This allows the Component to restart without reinitialization after the first call to the SCB_Start() routine. If reinitialization of the Component is required, then the SCB_Init() function can be called before the SCB_Start() or SCB_Enable() function.

Bootloader Support

The SCB Component in EZ I²C mode **cannot** be used as a communication Component for the Bootloader.

EZI2C Functional Description

This Component supports an I²C slave device with one or two I²C addresses. Either address may access a memory buffer defined in RAM or flash data space. Flash memory buffers are read only, while RAM buffers may be read/write. The addresses are right justified.

When using this Component, you must enable global interrupts because the I²C hardware is interrupt driven. Even though this Component requires interrupts, you do not need to add any code to the ISR (Interrupt Service Routine). The Component services all interrupts (data transfers) independently from your code. The memory buffers allocated for this interface look like simple dual-port memory between your application and the I²C master.

If required, you can create a higher-level interface between a master and slave by defining semaphores and command locations in the data structure.

Memory Interface

To an I²C master the interface looks very similar to a common I²C EEPROM. The EZ I²C buffer can be configured as a variable, array, or structure but it is preferable to use an array. The buffer acts as a shared memory interface between your program and an I²C master through the I²C bus. The Component permits read and write I²C master access to the specified buffer memory and prevents any access outside the buffer or write access into a read only region.

For example, the buffer for the primary slave address is configured using the code below. The buffer elements from 4 to 9 are read only.

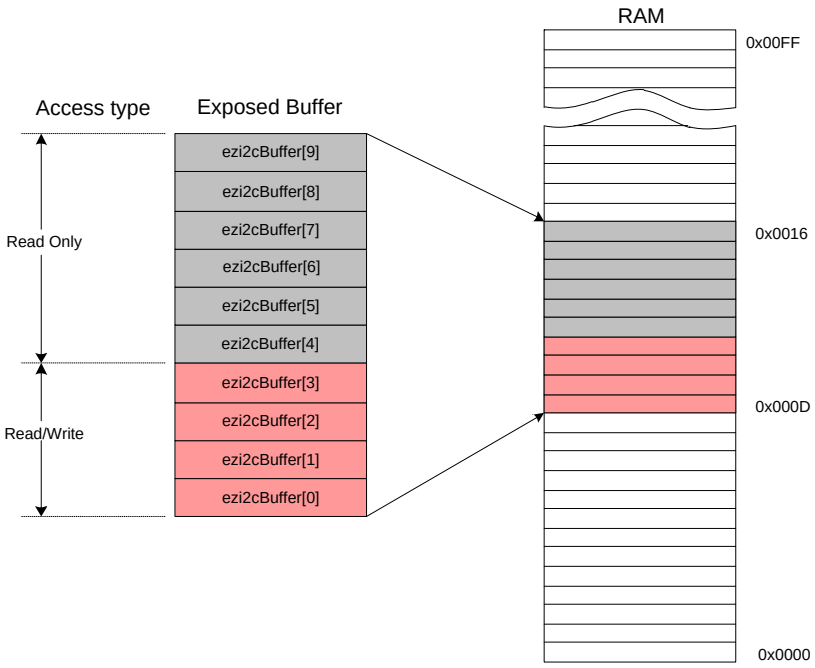
```
#define BUFFER_SIZE             (0x0Au)
#define BUFFER_RW_BOUNDARY      (0x04u)

uint8 ezi2cBuffer[BUFFER_SIZE];

SCB_EzI2CSetBuffer1(BUFFER_SIZE, BUFFER_RW_BOUNDARY, ezi2cBuffer);
```

The buffer ezi2cBuffer is allocated in memory as shown in Figure 5.

Figure 5. EZ I²C buffer exposed to an I²C master



To configure the whole buffer for read and write access, the buffer size and read/write boundary need to use the same value. For example:

```
SCB_EzI2CSetBuffer1(BUFFER_SIZE, BUFFER_SIZE, ezi2cBuffer);
```

Handling endianness

The EZ I²C buffer can be set up as a variable. A variable with a size of more than one byte will require knowledge of endianness (little-endian or big-endian). The endianness will determine the byte order on the I²C bus. It is the I²C master's responsibility to handle byte ordering properly.

```
uint16 ezi2cBuffer = 0xAABB;
#define BUFFER_SIZE (2u)

SCB_EzI2CSetBuffer1(BUFFER_SIZE, BUFFER_SIZE, (uint8 *) &ezi2cBuffer);
```

All PSoC 4 devices are little-endian devices, so the master will read these two bytes in order as: 0xBB 0xAA.

Handling structures

The EZ I²C buffer can be set up as structure. The compiler lays out structures in memory and may add extra bytes. This is called byte padding. The compiler will add these bytes to align the fields of the structure to match the requirements of the Cortex-M0. This processor does not support unaligned access to multi-byte fields. When using a structure, the application must take

this alignment into account. If fields need to be packed, then a byte array should be used instead of a structure.

Handling a status byte

To define a higher level protocol, a status byte placed inside the EZ I²C buffer may be required. This status byte would be modified by the I²C master, but the compiler is not aware that an interrupt routine may modify this buffer. This can result in the compiler optimizing a while loop that tests for a change in the status byte. The keyword volatile must be used to inform the compiler that the status byte might change state even though no statements in the program appear to change it.

Code example:

```
#define BUFFER_SIZE       (0x0Au)
#define STATUS_BYTE_POS   (0u)

volatile uint8 ezi2cBuffer[BUFFER_SIZE];

SCB_EzI2CSetBuffer1(BUFFER_SIZE, BUFFER_SIZE, ezi2cBuffer);

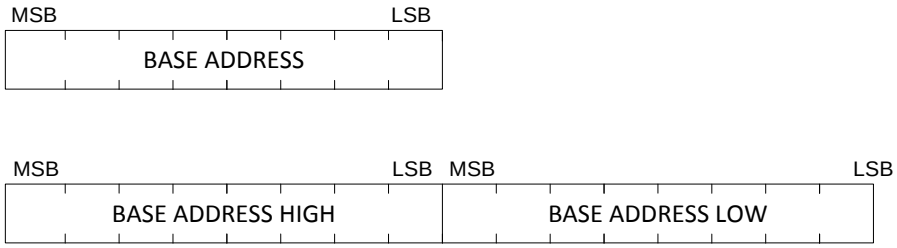
ezi2cBuffer[STATUS_BYTE_POS] = 0x01u;
while(0x01u == ezi2cBuffer[STATUS_BYTE_POS])
{
    /* Wait for status byte to be changed by the master */
}
```

Interface as Seen by an External Master

The EZ I²C slave Component supports basic read and write operations for the read/write region and read operations for the read-only region. The two I²C address interfaces contain separate data buffers that are addressed with separate base addresses. The base address is an index within the EZ I²C buffer, its range is 0 to buffer size - 1. The base address comes first, followed by the data bytes. The base address size depends on **Sub-address size** parameter: one byte (Sub-address size = 8bits) or two bytes (Sub-address size = 16bits). The sub-address size of 8 bits is used to access buffers up to 256 bytes and sub-address size of 16 bits is used for buffers up to 65535 bytes. In the case of a two byte address, the first byte is the high byte and the second is the low byte of the 16-bit value Figure 6.

For example, the desired base address to access is 0x0201: high byte is 0x02 and low is 0x01.

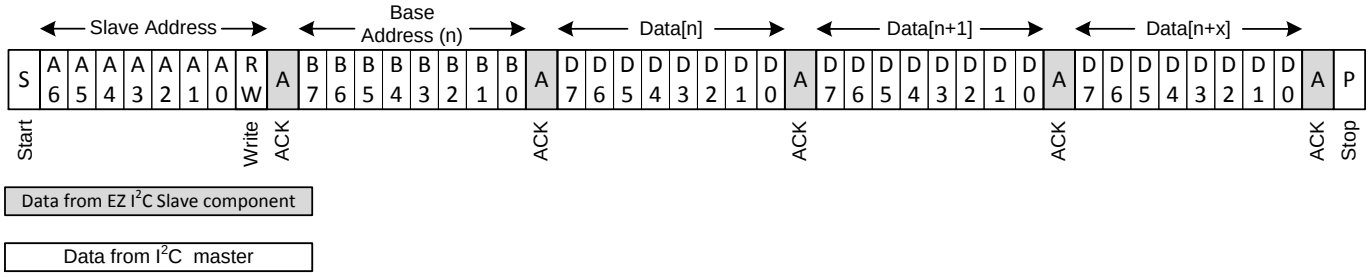
Figure 6. The 8-bit and 16-bit Sub-Address Size



For write operations, a base address is always provided and is one or two bytes depending on the configuration. This base address is retained and will be used for later read operations. Following the base address is a sequence of bytes that are written into the buffer starting from the base address location. The buffer index is incremented for each written byte, but this does not affect the base address, which is retained. The length of a write operation is **limited** by the maximum buffer read/write region size. The EZ I^{2}C slave behaves differently on the I^{2}C bus when a master attempts to write outside the read/write region or past the end of the buffer depending on the setting for Clock Stretching:

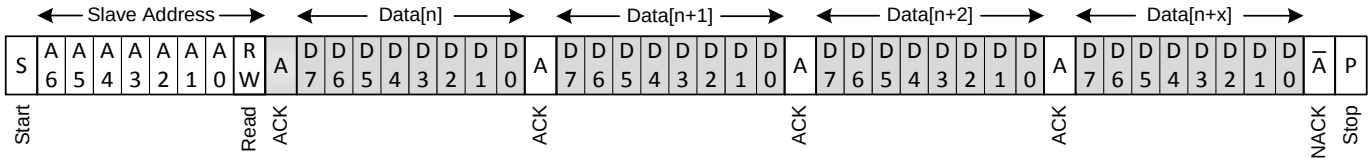
- Enabled: the byte is NAKed by the slave and the master has to stop the current transaction. The NAKed byte is discarded by the slave.
- Disabled: all written bytes are ACKed by the slave, but these bytes are discarded.

Figure 7. I^{2}C Master writes X bytes to the EZ I^{2}C Slave buffer



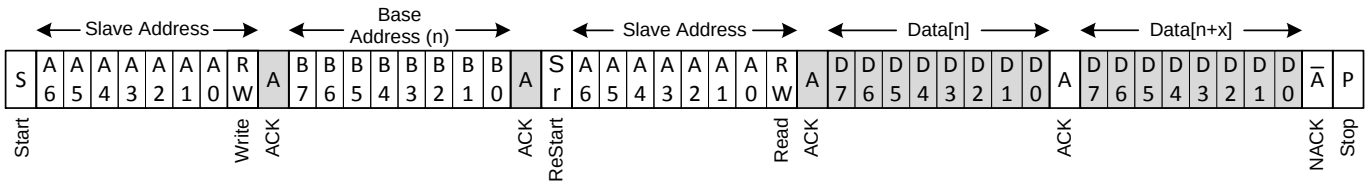
A read operation **always starts** from the base address set by the most recent write operation. The buffer index is incremented for each read byte. Two sequential read operations start from the same base address no matter how many bytes were read. The length of a read operation is **not limited** by the maximum size of the data buffer. The EZ I^{2}C slave returns 0xFF bytes if the read operation passes the end of the buffer.

Figure 8. I²C Master reads X bytes from the EZ I²C Slave buffer



Typically, a read operation requires the base address to be updated before starting the read. In this case, the write and read operations need to be combined together. The I²C master may use ReStart or Stop/Start conditions to combine the operations. The write operation only sets the base address and the following read operation will start reading from the new base address. In cases where the base address remains the same, there is no need for a write operation to be performed.

Figure 9. I²C Master sets the base address and reads X bytes from the EZ I²C Slave buffer



Detailed descriptions of the I²C bus and its implementation are available in the complete I²C specification on the NXP website, and by referring to the device datasheet.

Data Coherency

Although a data buffer may include a data structure larger than a single byte, a Master read or write operation consists of multiple single-byte operations. This can cause a data coherency problem, because there is no mechanism to guarantee that a multi-byte read or write will be synchronized on both sides of the interface (Master and Slave). For example, consider a buffer that contains a single two-byte integer. While the master is reading the two-byte integer one byte at a time, the slave may have updated the entire integer between the time the master read the first byte of the integer (LSB) and was about to read the second byte (MSB). The data read by the master may be invalid, since the LSB was read from the original data and the MSB was read from the updated value.

You must provide a mechanism on the master, slave, or both that guarantees that updates from the master or slave do not occur while the other side is reading or writing the data. The SCB_EzI2CGetActivity() function can be used to develop an application-specific mechanism.

Note The buffer setup APIs are not interrupt protected and must be called when the Component is disabled or the slave is not busy.

Clock Stretching

Clock stretching pauses a transaction by holding the SCL line low. The transaction cannot continue until the SCL line is released allowing the signal to go high again. The support of clock stretching is an optional feature of the I^2C spec. For that reason, the EZ I^2C slave provides an option to enable or disable this feature.

Clock Stretching Enable

Enabling the clock stretching option makes is possible for the slave to insert a pause into the transaction at the byte level. This allows for consistent EZ I^2C slave operation for any slave interrupt latency. The drawback is that the master has to support clock stretching as well.

Clock Stretching Disable

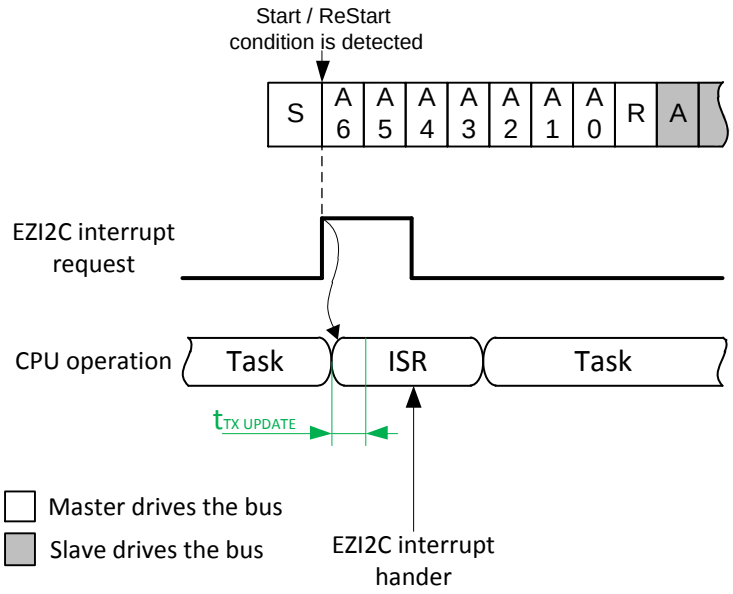
Disabling clock stretching configures the EZ I^2C slave to operate with an optimized interrupt service routine. This allows the EZ I^2C slave to operate without clock stretching. Despite the optimization, the slave interrupt still must be serviced fast enough. The maximum time that the slave interrupt service can be delayed is defined as the maximum EZ I^2C slave interrupt latency. A design that does not satisfy the required maximum EZ I^2C slave interrupt latency will cause erroneous slave behavior. It is recommended to enable clock stretching if the design cannot satisfy the required maximum EZ I^2C slave interrupt latency. When selecting the clock stretching disable option, refer also to the following:

- Maximum slave interrupt latency
- Transactions chained with ReStart
- Slave busy management

Maximum slave interrupt latency

All master transactions begin with a Start condition. The slave hardware detects this condition and generates an interrupt request, which starts slave operation (Figure 10). The ReStart condition has the same effect on the slave as Start condition, except previous transaction completion flags have to be set; service of the ReStart condition has greater priority.

Figure 10. EZ I²C slave starts operation



The time between starting the slave interrupt handler to the moment when the TX FIFO has been updated with the first byte is referred as $t_{TX\ UPDATE}$[5] [6] (Figure 10). The TX FIFO update consists of clearing the TX FIFO and writing a byte from the slave buffer into the TX FIFO. The TX FIFO update must be completed before the master starts reading the first data byte. Otherwise, a number of issues can occur, including: reading old the TX FIFO content, clock stretching when the TX FIFO is cleared [7], or reading a partial byte due to the TX FIFO clear in the middle of the byte transfer.

The constraint applied to the TX FIFO update during the master read transaction causes the maximum slave interrupt latency to be defined as maximum delay, which can be inserted from the Start condition detection by the slave hardware, to the start of the execution of the slave interrupt handler (Figure 11 on page 76).

5 This time depends on design settings such as CPU clock, compiler, optimization, etc.

6 This time does not include interrupt latency of the Cortext-M0 processor.

7 The slave hardware stretches the clock when TX FIFO is empty.

Therefore, the maximum interrupt latency must be less than the master address byte transmit time ($t_{ADDRESS}$) plus slave ACK bit transmit time (t_{ACK}). But taking to account TX FIFO update constraint, the maximum interrupt latency must be less than:

$$t_{MAX\ LATENCY} = (t_{ADDRESS} + t_{ACK}) - t_{TX\ UPDATE} = (8bits / f_{SCL} + 1bit / f_{SCL}) - t_{TX\ UPDATE} = 9 / f_{SCL} - t_{TX\ UPDATE}$$

For example I^2C data rate of 100 kbps, the maximum interrupt latency must be less than:

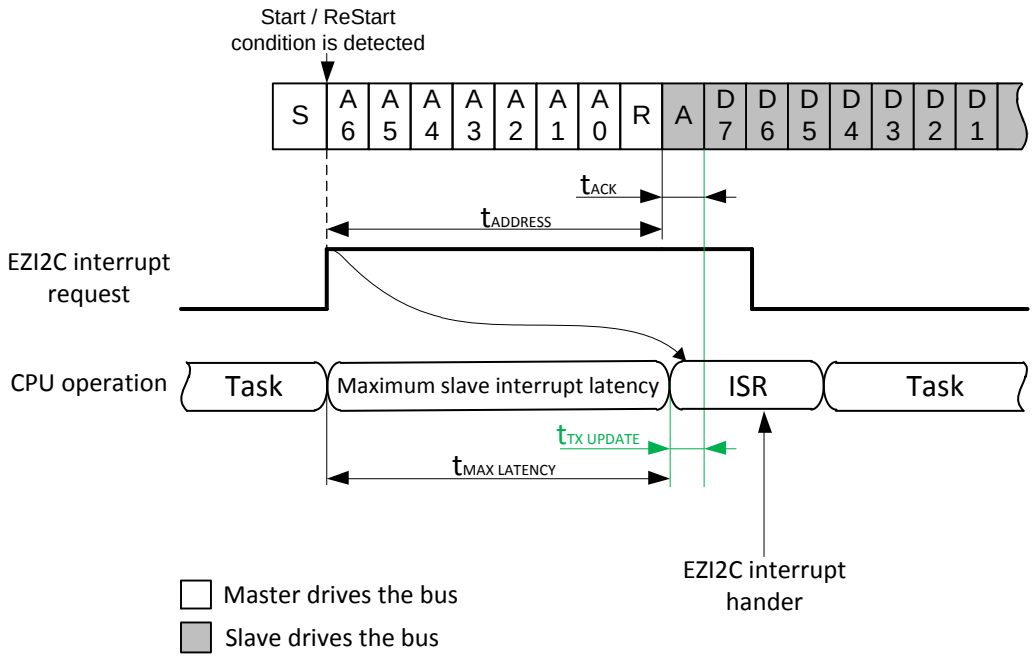
$$t_{MAX\ LATENCY} = 9 / f_{SCL} - t_{TX\ UPDATE} = 90\ uS - t_{TX\ UPDATE}$$

The number of CPU cycles to put the first byte into TX FIFO is calculated in the EZ I^2C interrupt. This number is equal to 71 cycles (mode Release, Compiler GCC, optimization Size). Taking into account that the maximum interrupt latency of the Cortext-M0 processor is 16 cycles; the number of cycles is increased to 87.

With the assumption that clock configuration of the design is internal IMO and HFCLK = SYSCLK = 24 MHz, the $t_{MAX\ LATENCY}$ is calculated for the I^2C data rate of 100 kbps. The accuracy of the internal IMO is +/-2%; therefore, the number of CPU cycles is increased by 2% and equal to ~89 cycles. The $t_{TX\ UPDATE}$ = 89 / SYSCLK = 3.71uS. Referring to the above equation, the maximum interrupt latency is equal to:

$$t_{MAX\ LATENCY} = 9 / f_{SCL} - t_{TX\ UPDATE} = 90\ uS - t_{TX\ UPDATE} = 90\ uS - 3.71\ uS = 86.29\ uS$$

Figure 11. EZ I2C slave maximum interrupt latency



Design recommendations:

1. Use the highest possible SYSCLK frequency, as it runs the CPU to reduce execution time of the EZ I^2C slave interrupt.

2. Use optimization options of the compiler as it reduces the number of instructions to execute in the EZ I^2C slave interrupt.
3. Set the EZ I^2C interrupt priority to be the highest in the design. If there are other interrupts with the same priority, make sure that their execution time is less than EZ I^2C maximum interrupt latency.
4. Calculate the duration of the each critical section in the design and compare with the EZ I^2C maximum interrupt latency to make sure that design meets criteria.

Transactions chained with ReStart

A common use case is for the master to write the base address, and then using a repeated start (no Stop) read data from the slave starting at the base address (Figure 12 on page 78). The base address (or data byte) written by the master is received into the RX FIFO and must be serviced by the slave interrupt handler (Figure 12, case 1). The service of the RX FIFO has greater priority than the ReStart condition service because the base address may have been updated by the master write transaction, and it is used for the TX FIFO update. The time spent to service the RX FIFO might affect the service of the ReStart condition. If this is the case (Figure 12, case 2), the maximum interrupt latency is reduced by the time it takes to service the RX FIFO after the ReStart condition is detected:

$$t_{MAX\ LATENCY} = 9 / f_{SCL} – (t_{RX\ DELAY} + t_{TX\ UPDATE})$$

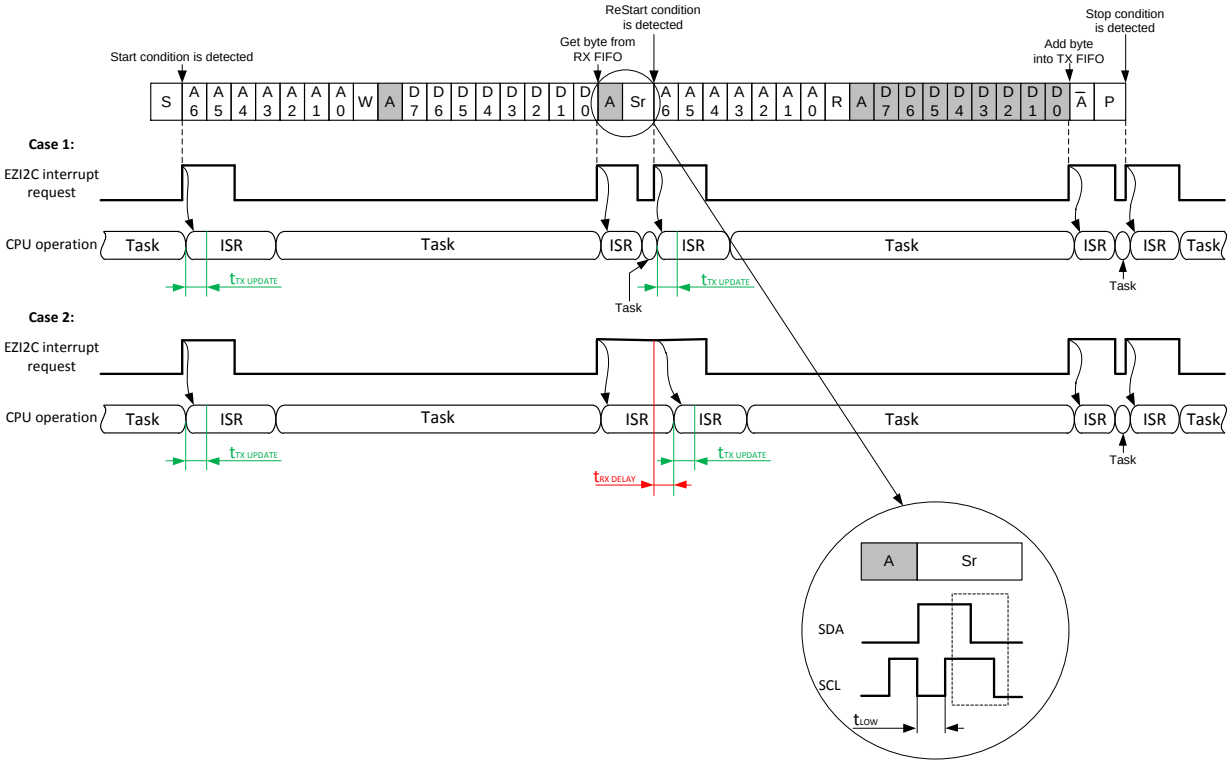
The RX FIFO service will affect $t_{MAX\ LATENCY}$ when it takes longer than (1bit / f_{SCL} + t_{LOW} + $t_{SU;STA}$), (where 1bit / f_{SCL} is duration of ACK condition generation, t_{LOW} and $t_{SU;STA}$ minimum values for the selected bus speed mode). For data rate 100 kbps this time equal to: 10 uS + 4.7 uS + 4.7 uS = 19.4 uS.

The longest RX FIFO service path in the EZ I^2C interrupt is consumed by the handling of base address written by the master ($t_{RX\ SERVICE}$). It consumes 100 CPU cycles (mode Release, Compiler GCC, optimization Size). Taking into account that the maximum interrupt latency of the Cortext-M0 processor is 16 cycles; the number of cycles is increased to 116.

With the assumption that clock configuration of the design is internal IMO and HFCLK = SYSCLK = 24 MHz, the $t_{RX\ SERVICE}$ is calculated. The accuracy of the internal IMO is +/-2%; therefore, the number of CPU cycles is increased by 2% and equal to ~118 cycles. The $t_{RX\ SERVICE}$ = 118 / SYSCLK = 4.92 uS which is less than 19.4 uS, therefore $t_{RX\ DELAY}$ = 0 uS.

The master ReStart timings must be examined; the I^2C spec provides minimum values. Some masters before ReStart generation extend t_{LOW} to prepare for the next transaction, but it is device specific. If there is possibility to control this time, the RX FIFO service effect on the maximum interrupt latency can be eliminated by increasing t_{LOW} before ReStart until $t_{RX\ DELAY}$ is equal to zero.

Figure 12. Master set base address and read data



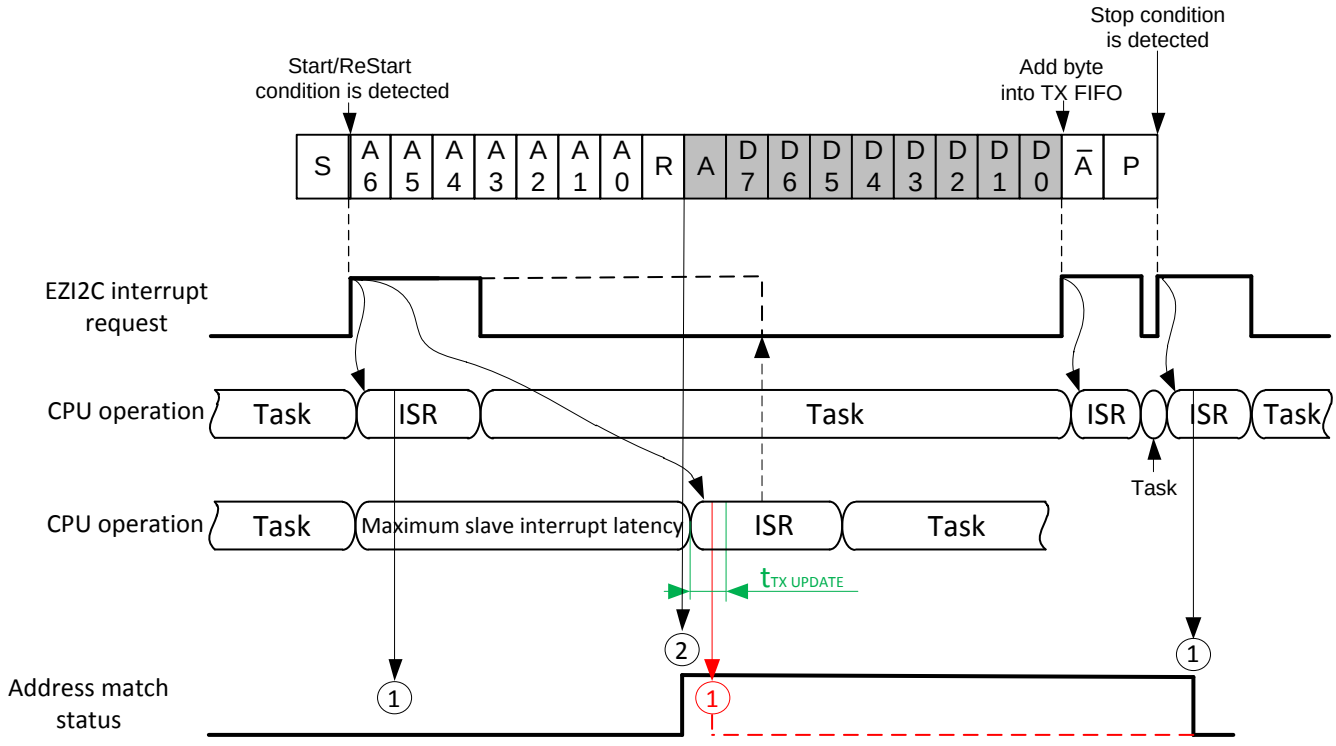
Slave busy management

The SCB_EzI2CGetActivity() API and SCB_Sleep() API use address match status to track slave busy status. This event is triggered by hardware on the rising edge of 8th SCL within the address byte for PSoC 4100 / PSoC 4200 devices and on falling edge of 8th SCL for other PSoC4 devices (Figure 13, black circle 2).

To be used as slave busy status, the address match is cleared by firmware on the Start / ReStart or Stop condition (Figure 13, black circle 1). If Start / ReStart interrupt service is delayed for maximum interrupt latency, the address match status is cleared too early (Figure 13, red circle 1).

This causes incorrect slave busy reporting. For correct slave busy status reporting, the maximum interrupt latency must be reduced to 1.5 bit / f_{SCL} for PSoC 4100 / PSoC 4200 devices and to 1 bit / f_{SCL} for other PSoC4 devices. As an alternative, the SCB hardware bus busy status can be used to manage bus activity. See the *SCB_I2C_STATUS* register bit *SCB_BUS_BUSY* description in *Technical Reference Manual (TRM)* for more information.

Figure 13. Slave busy management



(1) Address match status is cleared by firmware

(2) Address match status is set by hardware

Preferable Secondary Address Choice

The hardware address-match-logic uses address bit masking to support both addresses. The address mask defines which bits in the address are treated as non-significant while performing an address match. One non-significant bit results in two matching addresses; two bits will match 4 and so on. Due to this reason, it is preferable to select a secondary address that is different from the primary by one bit. The address mask in this case makes one bit non-significant. If the two addresses differ by more than a single bit, then the extra addresses that will pass the hardware match and will rely on firmware address matching to generate a NAK.

For example:

- Primary address = 0x24 and secondary address = 0x34, only one bit differs. Only the two addresses are treated as matching by the hardware.
- Primary address = 0x24 and secondary address = 0x30, two bits differ. Four addresses are treated as matching by the hardware: **0x24**, 0x34, 0x20 and **0x30**. Firmware is required to ACK only the primary and secondary addresses 0x24 and 0x30 and NAK all others 0x20 and 0x34.

Low power modes

The Component in EZ I^2C mode is able to be a wakeup source from Sleep and Deep Sleep low power modes.

Sleep mode is identical to Active from a peripheral point of view. No configuration changes are required in the Component or code before entering/exiting this mode. Any communication intended to the slave causes interrupt to occur and leads to wakeup.

Deep Sleep mode requires that the slave be properly configured to be a wakeup source. The “Enable wakeup from Deep Sleep Mode” must be checked in the I2C configuration dialog. The SCB_Sleep() and SCB_Wakeup() functions must be called before/after entering/exiting Deep Sleep.

The wakeup event is slave address match. The externally clocked logic performs address matching and when a matched address is detected the hardware generated an interrupt request. But the slave behavior after address match depends on clock stretching option selection.

Clock stretching enable: the slave stretches SCL line until control is passed to the slave interrupt routine to ACK the address.

Before entering Deep Sleep, the on-going transaction intended for the slave must be completed as suggested in the following code:

```
/* Enter critical section to lock the slave state */
uint8 intState = CyEnterCriticalSection();

/* Check if slave is busy */
status = (SCB_EzI2CGetActivity() & SCB_EZI2C_STATUS_BUSY);

if (0u == status)
{
```

```
        /* Slave is not busy: enter Deep Sleep */
        SCB_Sleep();      /* Configure the slave to be wakeup source */
        CySysPmDeepSleep();

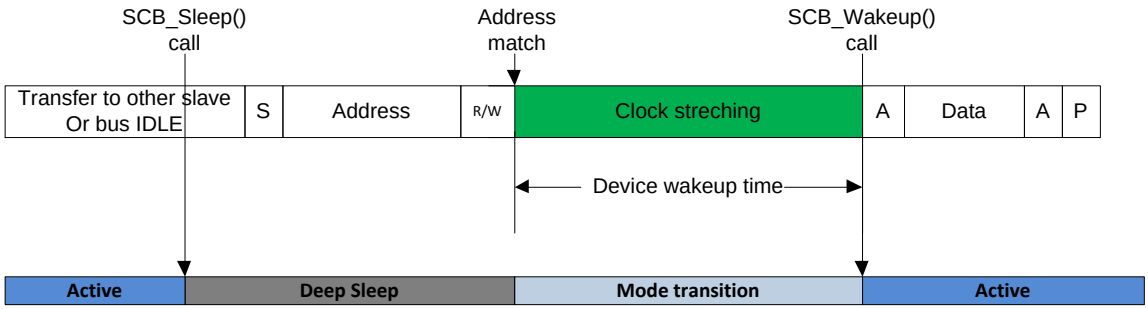
        /* Exit critical section to continue slave operation */
        CyExitCriticalSection(intState);
        SCB_Wakeup();     /* Configure the slave to active mode operation */
    }
    else
    {
        /* Slave is busy. Do not enter Deep Sleep.           */
        /* Exit critical section to continue slave operation */
        CyExitCriticalSection(intState);
    }
```

For devices **other than** PSoC 4100 / PSoC 4200, the **Component clock** must be disabled before calling SCB_Sleep(), and then enabled after calling SCB_Wakeup(); otherwise, the SCL will lock up after wakeup from Deep Sleep. Disabling and re-enabling the Component clock is managed by the SCB_Sleep() and SCB_Wakeup() APIs when the Clock from terminal option is disabled. Otherwise, when the Clock from terminal option is enabled, the code provided above requires modification to enable and disable the clock source connected to the SCB Component. Review the following modified code and highlighted in blue (ScbClock – the instance name of clock Component connected to the SCB):

```
    if (0u == status)
    {
        /* Slave is not busy: enter to Deep Sleep */
        SCB_Sleep();      /* Configure the slave to be wakeup source */
        ScbClock_Stop();  /* Disable the SCB clock */
        CySysPmDeepSleep();

        /* Exit critical section to continue slave operation */
        CyExitCriticalSection(intState);
        ScbClock _Start(); /* Enable SCB clock */
    }
```

Figure 14. Master transfer wakes up device on slave address match (Clock stretching enable)



Note The values for the primary and secondary addresses affect the range of matched addresses. The preferable choice for the secondary address is when it differs from the primary

only by one bit. If it differs by more than one bit, then some transactions that are not intended for this device will still wake the device from deep sleep. The address is going to be NAKed in this case.

Clock stretching disable: the slave NAKs the matched address and any subsequent transactions until the device wakes up.

Before entering Deep Sleep, the ongoing transaction intended for the slave must be completed. The waiting loop is implemented inside the SCB_Sleep() function. This function is blocking and waits until the slave is free to configure it to be a wakeup source. For proper SCB_Sleep() function operation the slave busy status has to be managed properly by the EZI2C slave(refer to the Slave busy management section for more information). After reconfiguration, the sampling of the address match event is started and the device has time to enter Deep Sleep mode. To operate correctly in active mode, the slave configuration must be restored back by SCB_Wakeup(). The agreement between slave and master must be concluded so as not to access the slave after wakeup until SCB_Wakeup() is executed. The following code is suggested:

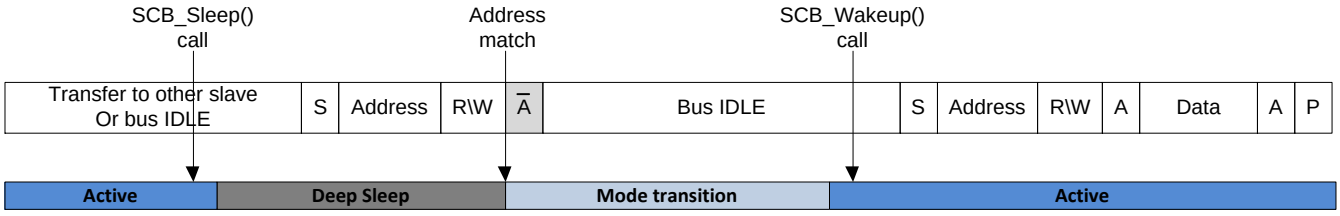
```
SCB_Sleep(); /* Wait for the slave to be free and configures it to be wakeup
source */

CySysPmDeepSleep();

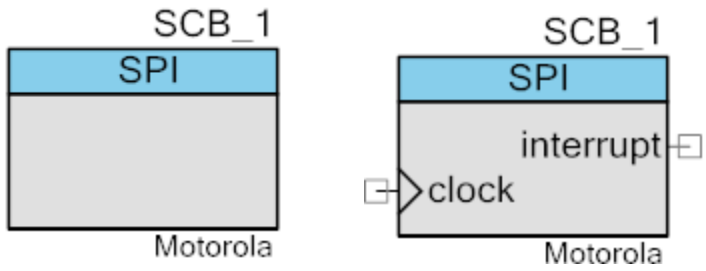
SCB_Wakeup(); /* Configure the slave to active mode operation */
```

Note The interrupts are required for the slave operations and global interrupts must be enabled before calling SCB_Sleep().

Figure 15. Master transfer wakes up device on slave address match (Clock stretching disable)



SPI



This Component provides an industry-standard, 4-wire SPI interface. Three different SPI protocols or modes are supported:

- Original SPI protocol as defined by Motorola.
- TI: Uses a short pulse on “spi_select” to indicate start of transaction.
- National Semiconductor (Microwire): Transmission and Receptions occur separately.

In addition to the standard 8-bit word length, the Component supports a configurable 4 to 16-bit data width for communicating at nonstandard SPI data widths.

Input/Output Connections

This section describes the various input and output connections for the SCB Component. An asterisk (*) in the list of terminals indicates that the terminal may be hidden on the symbol under the conditions listed in the description of that terminal.

clock – Input*

Clock that operates this block. The presence of this terminal varies depending on the Clock from terminal parameter.

interrupt – Output*

This signal can only be connected to an interrupt Component or left unconnected. The presence of this terminal varies depending on the Interrupt parameter.

rx_tr_out – Output*

This signal can only be connected to a DMA channel trigger input. This signal is used to trigger a DMA transaction. The output of this terminal is controlled by the RX FIFO level. The presence of this terminal varies depending RX Output parameter.

tx_tr_out – Output*

This signal can only be connected to a DMA channel trigger input. This signal is used to trigger a DMA transaction. The output of this terminal is controlled by the TX FIFO level. The presence of this terminal varies depending TX Output parameter.

The interface-specific pins are buried inside Component because these pins use dedicated connections and are not routable as general purpose signals. See the *I/O System* section in the device *Technical Reference Manual (TRM)* for more information.

Note The input buffer of buried output pins is disabled so as not to cause current linkage in low power mode. Reading the status of these pins always returns zero. To get the current status, the input buffer must be enabled before status read.

Internal Pins Configuration

The SPI Slave and Master pins are buried inside Component: SCB_miso_s, SCB_mosi_s, SCB_sclk_s, SCB_ss_s and SCB_miso_m, SCB_mosi_m, SCB_sclk_m, SCB_ss0_m, SCB_ss1_m, SCB_ss2_m, SCB_ss3_m. These pins are buried because they use dedicated connections and are not routable as general purpose signals. Refer to the *I/O System* section in the device *Technical Reference Manual (TRM)* for more information.

Note The instance name is not included into the Pin Names provided in the following tables.

Table 8. SPI Slave Pins Configuration

Pin Name	Direction	Drive Mode	Initial Drive State	Threshold	Slew Rate	Descriptiion
mosi_s	Input	High Impedance Digital	Low	CMOS	–	The mosi_s input pin receives the Master Output Slave Input (MOSI) signal from a master device. This pin presents if the Remove MOSI is unchecked. The pin output enable is tied to 0 to make pin state High-Z. The Drive Mode settings has no effect.
sclk_s	Input	High Impedance Digital	Low	CMOS	–	The sclk_s input pin receives the Serial Clock (SCLK) signal. It provides the slave synchronization clock input to the device. The pin output enable is tied to 0 to make pin state High-Z. The Drive Mode settings has no effect.
ss_s	Input	High Impedance Digital	Low	CMOS	–	The ss_s input pin receives the Slave Select (SS) signal to the device. The pin output enable is tied to 0 to make pin state High-Z. The Drive Mode settings has no effect.
miso_s	Output	Strong Drive	High	–	Fast	The s_miso output pin drives the Master In Slave Out (MISO) signal to the master device on the bus. This pin presents if the Remove MISO is unchecked.The pin output enable is assigend to 0 when slave is not selected. The Drive Mode settings has no effect in that moment and pins state is High-Z.

Table 9. SPI Master Pins Configuration

Pin Name	Direction	Drive Mode	Initial Drive State	Threshold	Slew Rate	Descriptiion
miso_m	Input	High Impedance Digital	Low	CMOS	–	The miso_m input pin receives the Master In Slave Out (MISO) signal from a slave device. This pin presents if the Remove MOSI is unchecked. The pin output enable is tied to 0 to make pin state High-Z. The Drive Mode settings has no effect.
mosi_m	Output	Strong Drive	High	_	Fast	The mosi_m output pin drives the Master Output Slave Input (MOSI) signal from the master device on the bus. This pin presents if the Remove MISO is unchecked.
sclk_m	Output	Strong Drive	High	_	Fast	The sclk_m output pin drives the Serial Clock (SCLK) signal. It provides the master synchronization clock output to the slave devices on the bus. This pin presents if the Remove SCLK is unchecked.
ss0_m – ss3_m	Output	Strong Drive	High	–	Fast	The ss0_m – ss3_m output pin drives the Slave Select (SS) signal to the slave devices on the bus. The master is capable to provide up to 4 hardware controlled slave select lines. This number depends on value of Number of SS parameter.

The Input threshold level for **input pins** is CMOS which should be used for the vast majority of application connections.

The Input Buffer for **output pins** is disabled so as not to cause current linkage in low power mode. Reading the status of these pins always returns zero. To get the current status, the input buffer must be enabled before a status read.

The other **input pins** and **output pins** parameters are set to default. Refer to pin Component datasheet for more information about default parameters values.

To change SPI buried pins configuration the pin's Component APIs should be used or direct pin registers configuration. For example:

```
/* Change SPI slave MISO pin drive mode to Open Drain Drives Low. */
SCB_miso_s_SetDriveMode(SCB_miso_s_DM_OD_LO);
```

Note Refer to Table 8 on page 84 to ensure that Drive Mode settings are not overridden by the SCB block connection to pin.

Glitch Avoidance at System Reset

The SPI outputs are in High Impedance Digital state when device is coming out of System Reset this can cause glitches on the outputs. This is important if you are concerned with SPI Master SS0 – SS3 (ss0_m – ss3_m) or SCLK (sclk_m) output pins activity at either chip startup or when coming out of Hibernate mode. The external pull-up or pull-down resistor has to be connected to the output pin to keep it in the inactive state.

The inactive state of SPI Master SS0 – SS3 pins depends on SS0-SS3 polarity parameters and inactive state of SCLK depends on SCLK mode parameter.

The Component takes care and sets SPI master SS0 – SS3 (ss0_m – ss3_m) and SCLK (sclk_m) outputs in the inactive state when Component is disabled or in Deep Sleep mode.

SmartIO support

The following connections are shown only if Enable SmartIO support option is enabled. Additional visibility conditions are listed in the following input and output descriptions. Only the Pin or SmartIO Component **is allowed** to be connected to these terminals.

Note The SCB block performs synchronization of the inputs internally therefore **Sync Input** option in the Digital Input Pin Component must be set to **Transparent**.

*s_mosi – Input **

The slave s_mosi input carries the Master Output Slave Input (MOSI) signal from a master device. This input is visible if the Remove MOSI is disabled. It must be connected if visible.

*s_sclk– Input **

The slave s_sclk input carries the Serial Clock (SCLK) signal. It provides the slave synchronization clock input to the device. This input is always visible and must be connected.

*s_ss – Input **

The slave s_ss input carries the Slave Select (SS) signal to the device. This input is always visible and must be connected.

*s_miso – Output **

The slave s_miso output carries the Master In Slave Out (MISO) signal to the master device on the bus. This output is visible if the Remove MISO is disabled.

*m_miso – Input **

The master m_miso input carries the MISO signal from a slave device. This input is visible if the Remove MOSI is disabled. It must be connected if visible.

*m_mosi – Output **

The master m_mosi output carries the MOSI signal from the master device on the bus. This output is visible if the Remove MISO is disabled.

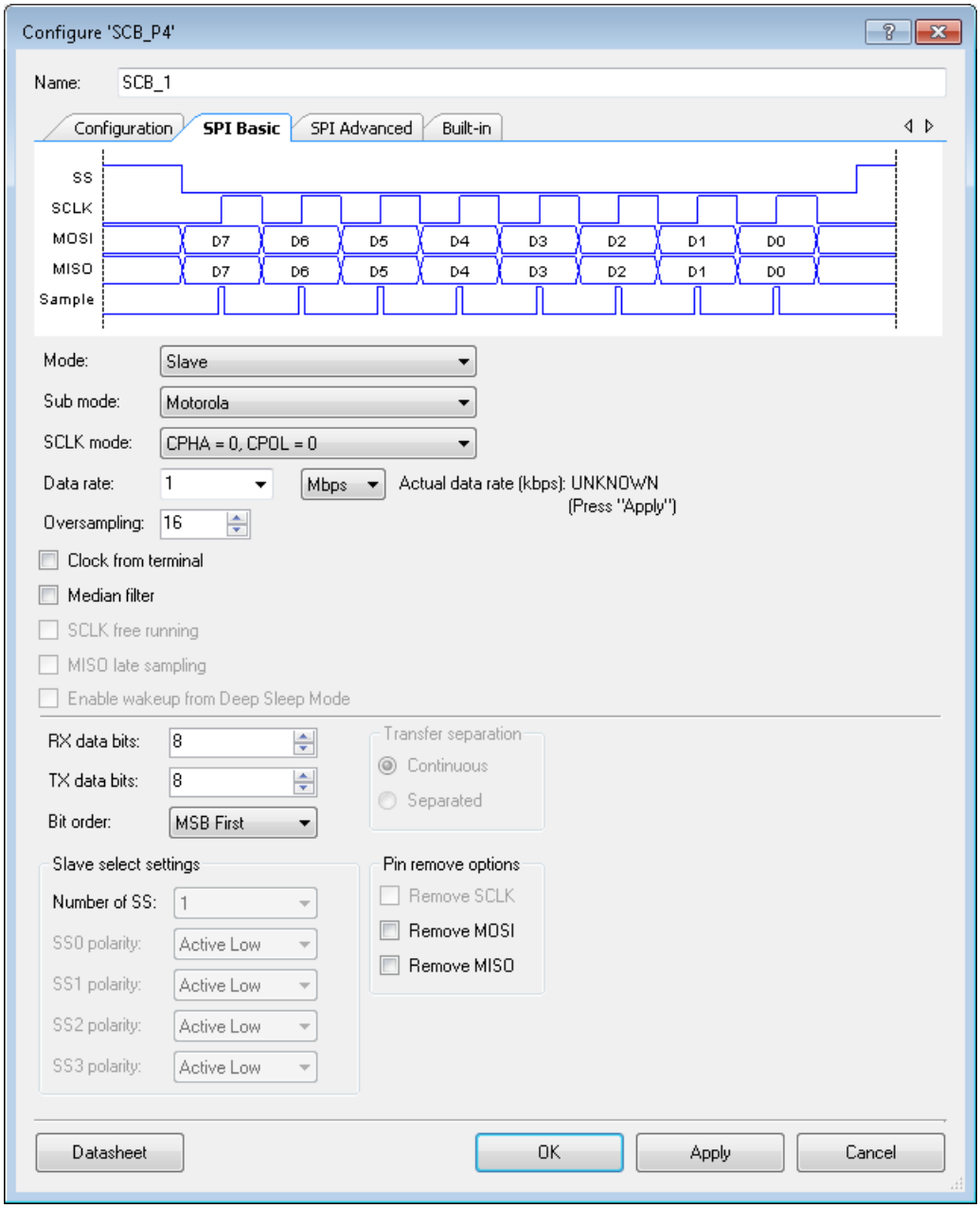
*m_sclk– Output **

The master m_sclk output carries the Serial Clock (SCLK) signal. It provides the master synchronization clock output to the slave devices on the bus. This output is visible if the Remove SCLK is disabled.

*m_ss0 – m_ss3 – Output **

The master ss0-ss3 outputs carries the Slave Select (SS) signal to the slave devices on the bus. The master is capable to provide up to 4 hardware controlled slave select lines. This number depends on value of Number of SS parameter.

Basic SPI Parameters



The **SPI Basic** tab contains the following parameters:

Mode

This option determines in which SPI mode the SCB operates.

- **Slave** – Slave only operation (default).
- **Master** – Master only operation.

Note For Slave activation the in the Motorola or National Semiconductor (Microwire) mode it is not enough to tie the slave select input to the active level. The initial falling edge for slave select active low or rising edge for slave select active high is required after slave was enabled.

Sub mode

This option determines what SPI sub-modes are supported:

- **Motorola** – The original SPI protocol as defined by Motorola (default).
- **TI (Start Coincides)** – The Texas Instruments' SPI protocol.
- **TI (Start Precedes)** – The Texas Instruments' SPI protocol.
- **National Semiconductor (Microwire)** – The National Semiconductor's Microwire protocol.

SCLK mode

This parameter defines the serial clock phase and clock polarity mode for communication.

- **CPHA = 0, CPOL= 0 –** Data is driven on a falling edge of SCLK. Data is captured on a rising edge of SCLK. SCLK idles low. This is default mode.
- **CPHA = 0, CPOL= 1** – Data is driven on a rising edge of SCLK. Data is captured on a falling edge of SCLK. SCLK idles high.
- **CPHA = 1, CPOL= 0** – Data is driven on a rising edge of SCLK. Data is captured on a falling edge of SCLK. SCLK idles low
- **CPHA = 1, CPOL= 1** – Data is driven on a falling edge of SCLK. Data is captured on a rising edge of SCLK. SCLK idles high

Refer to the section Motorola sub mode operation in the SPI chapter of this document for more information.

Data rate

This parameter is used to set the SPI data rate value up to 8000 kbps; the actual rate may differ based on available clock frequency and Component settings. The standard data rates are 500, 1000 (default), 2000, 4000 to 8000 in multiples of 2000 kbps. This parameter has no effect if the **Clock from terminal** parameter is enabled.

Actual data rate

The actual data rate displays the data rate at which the Component will operate with current settings. The factors that affect the actual data rate calculation are: the accuracy of the Component clock (internal or external) and oversampling factor (only for the Master mode). When a change is made to any of the Component parameters that affect actual data rate, it becomes unknown. To calculate the new actual data rate press the Apply button.

Note For Slave mode the actual data rate always provides maximum value for the selected clock frequency. As external Master parameters are unknown, the assumption was made that MISO is sampled in the leading edge of SCLK.

Refer to the Slave data rate section for actual data rate calculation which takes to account external environment timing conditions.

Oversampling

This parameter defines the oversampling factor of the SPI clock; the number of Component clocks within one SPI clock period. Oversampling factor is used to calculate the internal Component clock frequency required to achieve this amount of oversampling as follows: SCBCLK = Data rate * Oversampling factor.

- For **Slave** mode, only the Component clock source frequency is important. The oversampling value is used to create a clock fast enough to operate at the selected data rate. Refer to the Maximum data rate calculation section for more information. The created clock is equal to the (data rate * Oversampling).
- For **Master** mode, the oversampling value is used for serial clock signal (SCLK) generation. The oversampling is equal to number of Component clocks within one SPI clock period. When the oversampling is even the first and second phase of the clock period are the same. Otherwise the first phase of the clock signal period is one Component clock cycle longer than the second phase. The level of the first phase of the clock period depends on CPOL settings: 0 – low level and 1 – high level.

An oversampling factor maximum value is 16 and minimum depends on Component settings. For **Master** the minimum oversampling factor value is 6. For **Slave** the minimum oversampling value 6 (Median filter is disabled) or 8 (Median filter is enabled).

Clock from terminal

This parameter allows choosing between an internally configured clock (by the Component) or an externally configured clock (by the user) for the Component operation. Refer to the **Oversampling** section to understand relationship between Component clock frequency and the Component parameters.

When this option is enabled, the Component does not control the data rate, but displays the actual data rate based on the user-connected clock source frequency and the Component oversampling factor (only for the Master mode). When this option is not enabled, the clock

configuration and Oversampling factor (only for the Master mode) is provided by the Component. The clock source frequency is calculated by the Component based on the Data rate parameter.

Note PSoC Creator is responsible for providing requested clock frequency (internal or external clock) based on current design clock configuration. When the requested clock frequency with requested tolerance cannot be created, a warning about the clock accuracy range is generated while building the project. This warning contains the actual clock frequency value created by PSoC Creator. To remove this warning you must either change the system clock, Component settings or external clock to fit the clocking system requirements.

Median filter

This parameter applies 3 taps digital median filter on the input line. The master has one input line: MISO, and the slave has three input lines: SCLK, MOSI, and SS. This filter reduces the susceptibility to errors. However, minimum oversampling factor value is increased. The default value is a **Disabled**.

SCLK free running

This option is only applicable for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices in Master mode. It allows master to generate SCLK continually. It is useful when master SCLK is connected to the slave device which uses it for functional operation rather than just SPI functionality.

The default value is a **Disabled**.

Enable late MISO sample

This option allows the master to sample the MISO signal by half of SCLK period later (on the alternate serial clock edge). Late sampling addresses the round-trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. The default value is a **Disabled**.

Enable wakeup from Deep Sleep Mode

Use this option to enable the Component to wake the system from Deep Sleep when slave select occurs.

To enable this option all of the following restrictions must be met:

- Sub mode is Motorola
- SCLK mode is CPHA = 0, CPOL = 0 (only for PSoC 4100/PSoC 4200 devices)
- Interrupt is Internal

Refer to the Low power modes section under the SPI chapter in this document and *Power Management APIs* section of the *System Reference Guide* for more information.

TX data bits

This option defines the bit width in a transmitted data frame. The default number of bits is a single byte (8 bits). Any integer from 4 to 16 is a valid setting.

RX data bits

This option defines the bit width in a received data frame. The default number of bits is a single byte (8 bits). Any integer from 4 to 16 is a valid setting.

Note The number of **TX data bits** and **RX data bits** should be set the same for **Motorola** and **Texas Instruments** sub-modes; they can be set different for **National Semiconductor** sub-mode.

Bit order

The **Bits order** parameter defines the direction in which the serial data is transmitted. When set to **MSB first**, the most-significant bit is transmitted first. When set to **LSB first**, the least-significant bit is transmitted first.

Remove SCLK

This option allows removal of the SCLK pin from the SPI interface. If selected, this pin is no longer available in the Design-Wide Resources System Editor (in the *<project>.cydwr* file) on the Pins Tab. The SCLK pin cannot be removed in Slave mode.

Remove MOSI

This option allows removal of the MOSI pin from the SPI interface. If selected, this pin is no longer available in the Design-Wide Resources System Editor (in the *<project>.cydwr* file) on the Pins Tab.

Remove MISO

This option allows removal of the MISO pin from the SPI interface. If selected, this pin is no longer available in the Design-Wide Resources System Editor (in the *<project>.cydwr* file) on the Pins Tab.

Number of SS

This parameter determines the number of SPI slave select lines. Only one slave select line is available in Slave mode and it is not optional. The values between 0 and 4 are valid choices in Master mode. The default number of lines is 1.

Transfer separation

This parameter determines if individual data transfers are separated by slave select de-selection (only applicable for Master mode):

- **Continuous –** The slave select line is held in active state until the end of transfer (default).

  The master assigns the slave select output after data has been written into the TX FIFO and keeps it active as long as there are data elements to transmit. The slave select output becomes inactive when all data elements have been transmitted from the TX FIFO and shifter register.

  Note This can happen even in the middle of the transfer if the TX FIFO is not loaded fast enough by the CPU or DMA. To overcome this behavior, the slave select can be controlled by firmware. For more information about slave select control, refer to the Slave select lines section.

- **Separated –** Every data frame 4-16 bits is separated by slave select line de-selection by one SCLK period.

SS0-SS3 polarity

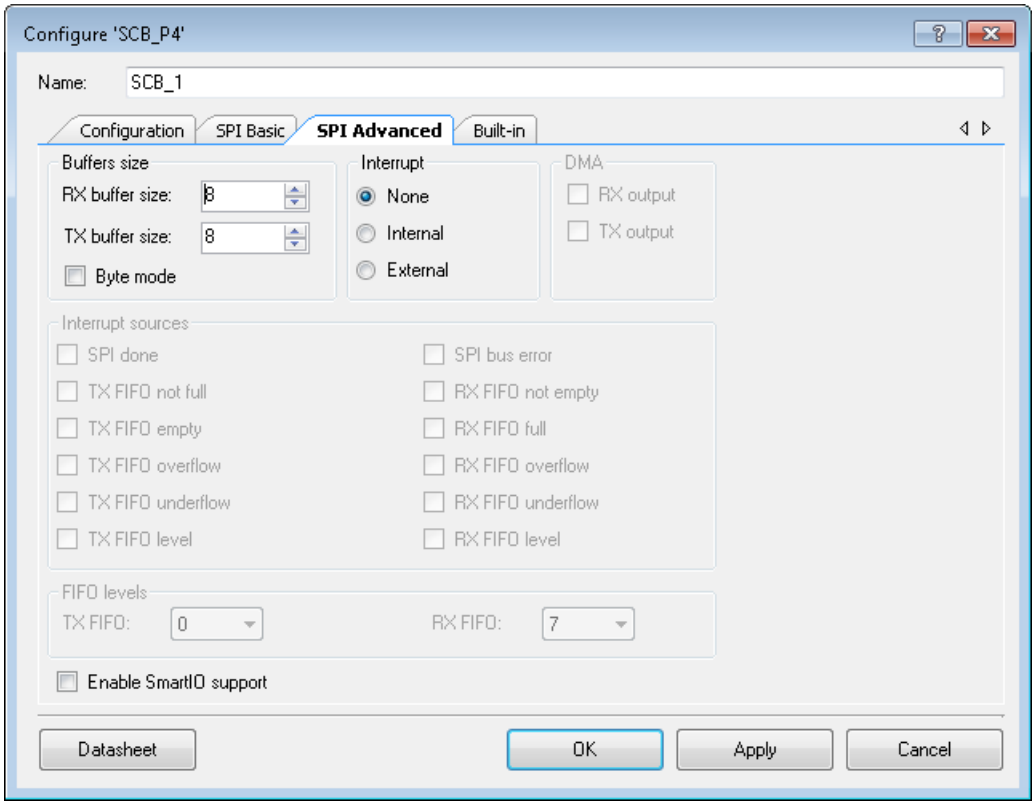
This option is only applicable for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices. It determines the active polarity of the slave select signal as Active Low (default) or Active High. For other devices, only Active Low is available.

Each slave select line active polarity can be configured independently.

For Texas Instruments precede/coincide sub-modes the active polarity logic is inverted:

- **Active Low –** Slave select line is inactive low and generated pulse is active high.
- **Active High –** Slave select line is inactive high and generated pulse is active low.

Advanced SPI Parameters



The **SPI Advanced** tab contains the following parameters:

RX buffer size

The **RX buffer size** parameter defines the size (in bytes/words) of memory allocated for a receive data buffer. The minimum value is equal to the RX FIFO depth. The RX FIFO is implemented in hardware. Values greater than the RX FIFO depth up to (2^{32} – 2) imply using the RX FIFO, a circular software buffer controlled by the supplied APIs, and the internal interrupt handler. The software buffer size is limited only by the available memory. The interrupt mode is automatically set to internal and the RX FIFO not empty interrupt source is reserved to manage software buffer operation: move data from the RX FIFO into the circular software buffer.

- For 4100/PSoC 4200 devices, the RX and TX FIFO depth is equal to 8 bytes/words.
- For PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices, the RX and TX FIFO depth is equal to 8 bytes/words or 16 bytes; refer to Byte mode for more information.

TX buffer size

The **TX buffer size** parameter defines the size (in bytes/words) of memory allocated for a circular transmit data buffer. The TX buffer size minimum value is equal to the TX FIFO depth. The TX FIFO is implemented in hardware. Values greater than the TX FIFO depth up to (2^{32} – 1) imply using the TX FIFO, circular software buffer controlled by the supplied APIs, and the internal interrupt handler. The software buffer size is limited only by the available memory. The interrupt mode is automatically set to the internal and the TX FIFO not full interrupt source is reserved to manage software buffer operation: move data from the circular software buffer into the TX FIFO.

- For 4100/PSoC 4200 devices, the RX and TX FIFO depth is equal to 8 bytes/words.
- For PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices, the RX and TX FIFO depth is equal to 8 bytes/words or 16 bytes; refer to Byte mode for more information.

Byte mode

This option is only applicable to PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices. It allows doubling the TX and RX FIFO depth from 8 to 16 bytes, by reducing the FIFO width from 16bits to 8 bits. This implies that the number of TX and RX data bits must be less than or equal to 8 bits. Increasing FIFO depth improves performance of SPI operation as more bytes can be transmitted or received without software interaction.

Interrupt

This option determines what interrupt modes are supported None, Internal or External.

- **None** – This option removes the internal interrupt Component.
- **Internal** – This option leaves the interrupt Component inside the SCB Component. The predefined internal interrupt handler is hooked up to the interrupt. The **Interrupt sources** option sets one or more interrupt sources, which trigger the interrupt. To add your own code to the interrupt service routine you need to register a function using the SCB_SetCustomInterruptHandler() function.
- **External** – This option removes the internal interrupt and provides an output terminal. Only an interrupt Component can be connected to this terminal if an interrupt handler is desired. The **Interrupt sources** option sets one or more interrupt sources, which trigger the interrupt output.

Note For buffer sizes greater than the hardware FIFO depth, the Component automatically enables the internal interrupt sources required for proper internal software buffer operations. In addition, the global interrupt enable must be explicitly enabled for proper buffer handling.

DMA

DMA is only available in PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC Analog Coprocessor devices. The **RX Output** and **TX Output** options determine if DMA output trigger terminals are available on the Component symbol.

RX Output

This option determines if the rx_tr_out terminal is available on the Component symbol. This signal can only be connected to a DMA channel trigger input. The output of this terminal is controlled by the RX FIFO level. This option is active only when RX buffer size equal to FIFO depth.

TX Output

This option determines if the tx_tr_out terminal is available on the Component symbol. This signal can only be connected to a DMA channel trigger input. The output of this terminal is controlled by the TX FIFO level. This option is active only when TX buffer size equal to FIFO depth.

Interrupt sources

The interrupt sources are either level or pulse. Level-triggered interrupt sources in the following list are indicated with an asterisk (*). Refer to sections TX FIFO interrupt sources and RX FIFO interrupt sources for more information about level interrupt sources operation. The SPI supports interrupts on the following events:

- **SPI done** – Master transfer done event: all data elements from the TX FIFO are sent. This interrupt source triggers later than TX FIFO empty by the amount of time it takes to transmit a single data element. The TX FIFO empty triggers when the last data element from the TX FIFO goes to the shifter register. However, SPI done triggers after this data element has been transmitted. This means SPI done will be asserted one SCLK clock cycle earlier than the reception of the data element has been completed. It is recommended to use SCB_SpiIsBusBusy() after checking SPI done to determine when the data element reception has been fully completed. As an alternative, the number of received data elements can be checked to make sure that it is equal to the number of the transmitted data elements.
- **TX FIFO not full * –** TX FIFO is not full. At least one data element can be written into the TX FIFO.
- **TX FIFO empty * –** TX FIFO is empty.
- **TX FIFO overflow –** Firmware attempts to write to a full TX FIFO.
- **TX FIFO underflow * –** Hardware attempts to read from an empty TX FIFO.

Note For SPI master, this interrupt source is level-triggered. It sets whenever there is no data to transmit (it can be used as an indication that the transfer is finished). For SPI slave, it is not level triggered and sets when the slave does not have any data to transmit on master request.

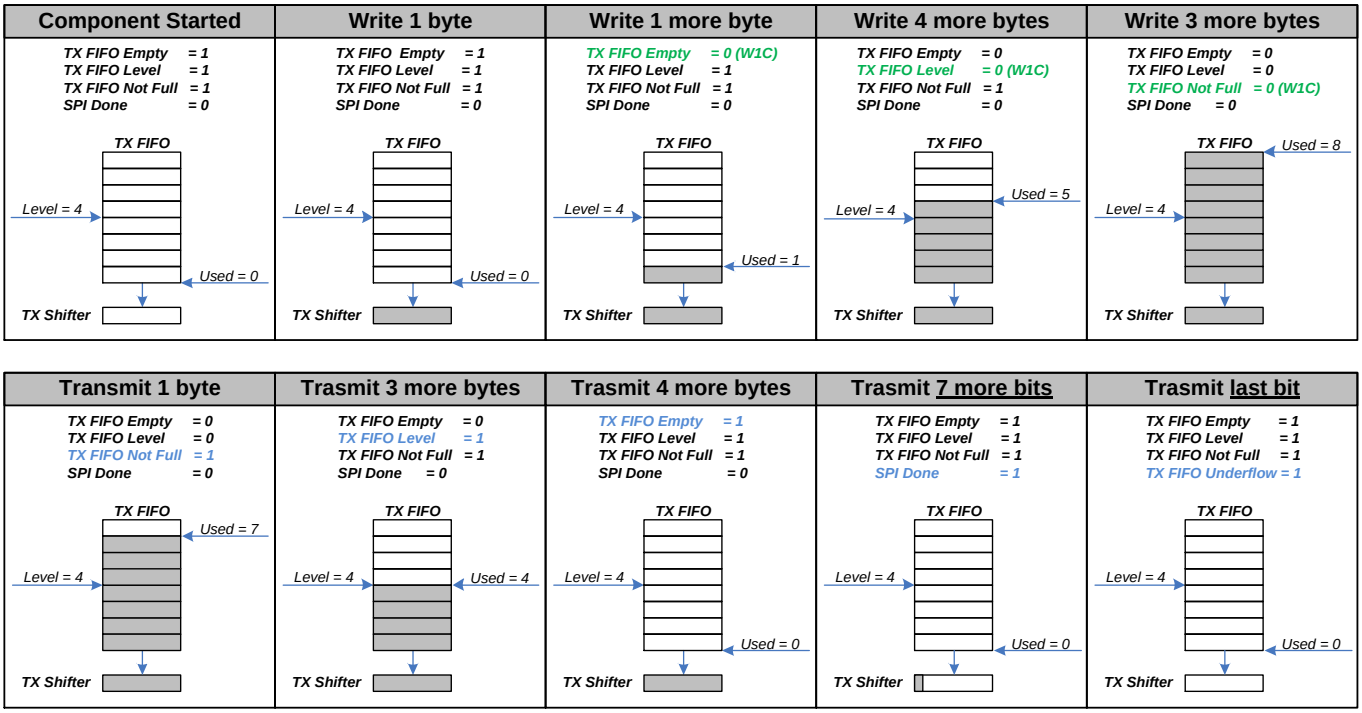
- **TX FIFO level * –** An interrupt request is generated whenever the number of data elements in the TX FIFO is less than the value of TX FIFO level.
- **SPI bus error –** SPI slave deselected at an unexpected time during the SPI transfer.
- **RX FIFO not empty * –** RX FIFO is not empty. At least one data element is available in the RX FIFO to be read.
- **RX FIFO full * –** RX FIFO is full.
- **RX FIFO overflow –** Hardware attempts to write to a full RX FIFO.
- **RX FIFO underflow –** Firmware attempts to read from an empty RX FIFO.
- **RX FIFO level * –** An interrupt request is generated whenever the number of data elements in the RX FIFO is greater than the value of RX FIFO level.

Notes

When **RX buffer size** is greater than the RX FIFO depth, the **RX FIFO not empty** interrupt source is reserved by the Component and used for the internal interrupt.

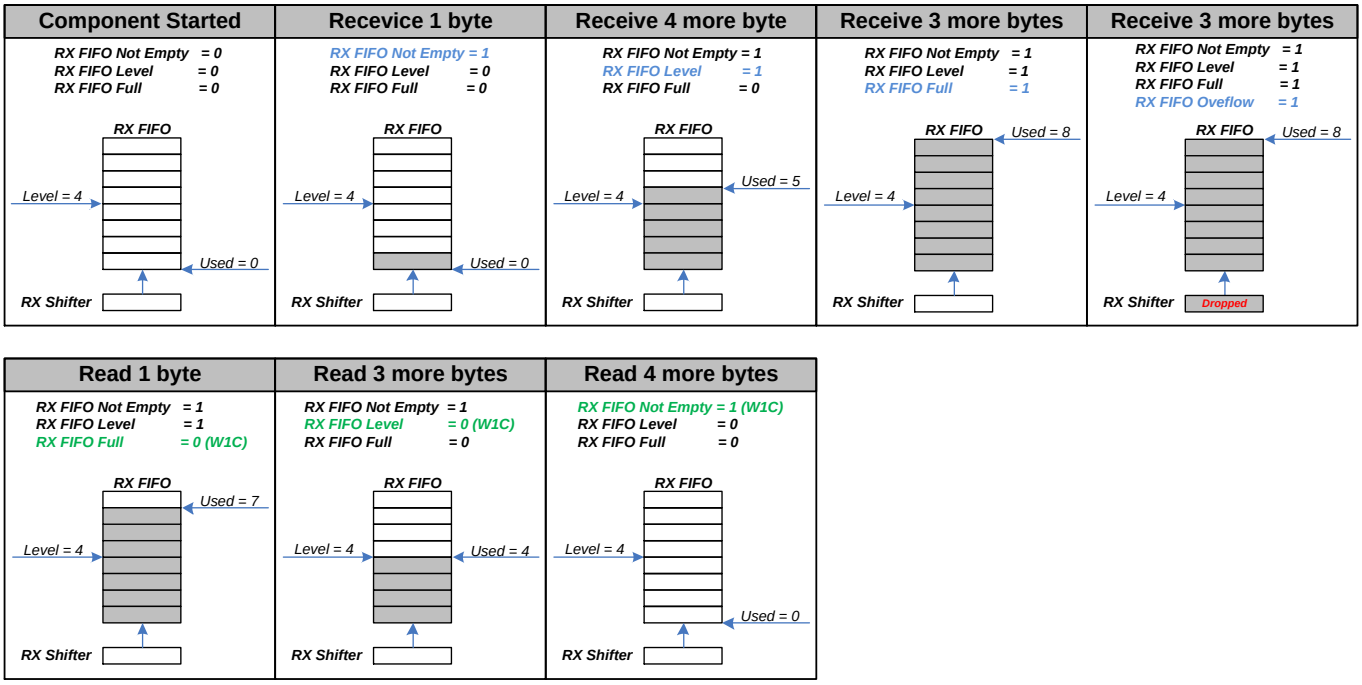
When **TX buffer size** is greater than the TX FIFO depth, the **TX FIFO not full** interrupt source is reserved by the Component and used for the internal interrupt.

Figure 16. TX interrupt sources operation



Note W1C – Write One to Clear interrupt source. The firmware has to execute this action to clear interrupt source.
Note TX FIFO interrupt sources Empty, Level and Full are level triggered. It means that interrupt source active state is restored after clear operation if FIFO state is not changed.
For example: the TX FIFO Empty interrupt source cannot be cleared if hardware still have bytes to transmit from TX FIFO.

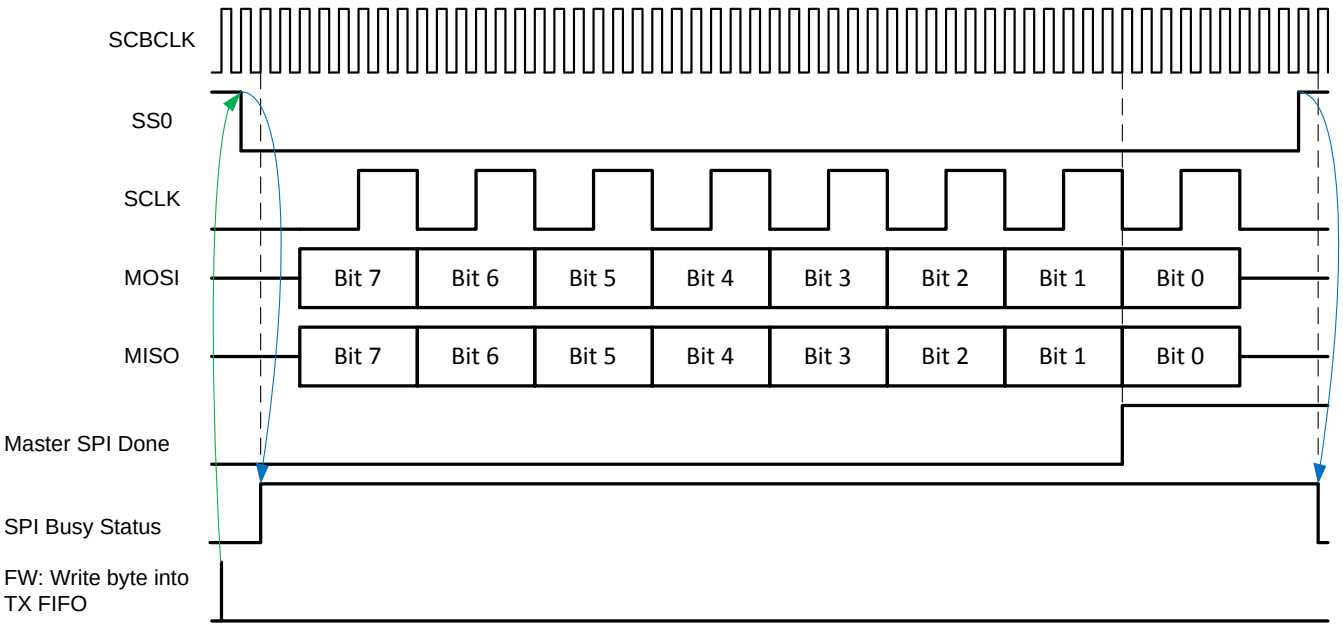
Figure 17. RX interrupt sources operation



Note W1C – Write One to Clear interrupt source. The firmaware has to execute this action to clear interrupt source.
Note RX FIFO interrupt sources Not Empty, Level and Full are level triggered. It means that interrupt source active state is restored after clear operation if FIFO state is not changed.
For example: the RX FIFO Full interrupt source cannot be cleared if firmware is not read at least single byte from full RX FIFO.

Figure 18. SPI Master (Motorola) single byte transfer

CPOL = 0, CPHA = 0
Oversampling = 6 (1 SCLK period contains 6 SCBCLK periods), Median filter = disabled.



FIFO level

The RX and TX FIFO level settings control behavior of the appropriate level interrupt sources as well as RX and TX DMA triggers outputs.

RX FIFO

The interrupt or DMA trigger output signal remains active until the number of data elements in the RX FIFO is greater than the value of RX FIFO level.

For example, the RX FIFO has 8 data elements and the RX FIFO level is 0. The DMA trigger signal remains active until DMA does not read all data from the RX FIFO.

TX FIFO

The interrupt or DMA trigger output signal remains active until the number of data elements in the TX FIFO is less than the value of TX FIFO level.

For example, the TX FIFO has 0 data elements (empty) and the TX FIFO level is 7. The DMA trigger signal remains active until DMA does not load TX FIFO with 7 data elements.

Enable SmartIO support

This option removes buried SPI pins inside the Component and exposes appropriate input and output terminals for the slave or master. Only the Pin or SmartIO Component is allowed to be connected to these terminals. See Input/Output Connections section for descriptions of these terminals. This option is disabled by default and supported only by PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices.

Note The SCB Component stops managing the pin states when the Component is disabled or the device is in low power, when the Enable SmartIO support option is enabled. In this case, you must take care of these pin states.

SPI APIs

APIs allow you to configure the Component using software. The following table lists and describes the interface to each function. The subsequent sections discuss each function in more detail.

By default, PSoC Creator assigns the instance name “SCB_1” to the first instance of a Component in a given design. You can rename the instance to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is “SCB”.

Function	Description
SCB_Start()	Starts the SCB.

Function	Description
SCB_Init()	Initialize the SCB Component according to defined parameters in the customizer.
SCB_Enable()	Enables SCB Component operation.
SCB_Stop()	Disable the SCB Component.
SCB_Sleep()	Prepares Component to enter Deep Sleep.
SCB_Wakeup()	Prepares Component for Active mode operation after Deep Sleep.
SCB_SpiInit()	Configures the SCB for SPI operation.
SCB_SpiIsBusBusy()	Returns the current status on the bus.
SCB_SpiSetActiveSlaveSelect()	Selects the active slave select line. Only applicable in Master mode.
SCB_SpiSetSlaveSelectPolarity()	Sets active polarity for the slave select line.
SCB_SpiUartWriteTxData()	Places a data entry into the transmit buffer to be sent at the next available bus time.
SCB_SpiUartPutArray()	Places an array of data into the transmit buffer to be sent.
SCB_SpiUartGetTxBufferSize()	Returns the number of elements currently in the transmit buffer.
SCB_SpiUartClearTxBuffer()	Clears the transmit buffer and TX FIFO.
SCB_SpiUartReadRxData()	Retrieves the next data element from the receive buffer.
SCB_SpiUartGetRxBufferSize()	Returns the number of received data elements in the receive buffer.
SCB_SpiUartClearRxBuffer()	Clears the receive buffer and RX FIFO.

void SCB_Start(void)

Description: Invokes SCB_Init() and SCB_Enable(). After this function call the Component is enabled and ready for operation. This is the preferred method to begin Component operation.

When configuration is set to “Unconfigured SCB”, the Component must first be initialized to operate in one of the following configurations: I²C, SPI, UART or EZ I²C. Otherwise this function does not enable Component.

void SCB_Init(void)

Description: Initializes the SCB Component to operate in one of the selected configurations: I²C, SPI, UART or EZ I²C.

When configuration is set to “Unconfigured SCB”, this function does not do any initialization. Use mode-specific initialization APIs instead: SCB_I2CInit, SCB_SpiInit, SCB_UartInit or SCB_EzI2CInit.

void SCB_Enable(void)

Description: Enables SCB Component operation; activates the hardware and internal interrupt. It also restores TX interrupt sources disabled after the SCB_Stop() function was called (note that level-triggered TX interrupt sources remain disabled to not cause code lock-up).

For I^2C and EZ I^2C modes the interrupt is internal and mandatory for operation. For SPI and UART modes the interrupt can be configured as none, internal or external.

The SCB configuration should be not changed when the Component is enabled. Any configuration changes should be made after disabling the Component.

When configuration is set to “Unconfigured SCB”, the Component must first be initialized to operate in one of the following configurations: I^2C, SPI, UART or EZ I^2C. Otherwise this function does not enable Component.

void SCB_Stop(void)

Description: Disables the SCB Component: disable the hardware and internal interrupt. It also disables all TX interrupt sources so as not to cause an unexpected interrupt trigger because after the Component is enabled, the TX FIFO is empty.

Refer to the function SCB_Enable() for the interrupt configuration details.

This function disables the SCB Component without checking to see if communication is in progress. Before calling this function it may be necessary to check the status of communication to make sure communication is complete. If this is not done then communication could be stopped mid byte and corrupted data could result.

void SCB_Sleep(void)

Description: Prepares Component to enter Deep Sleep.

The “Enable wakeup from Deep Sleep Mode” selection has an influence on this function implementation:

- Checked: configures the Component to be wakeup source from Deep Sleep.
- Unchecked: stores the current Component state (enabled or disabled) and disables the Component. See SCB_Stop() function for details about Component disabling.

Call the SCB_Sleep() function before calling the CyPmSysDeepSleep() function. Refer to the PSoC Creator *System Reference Guide* for more information about power-management functions.

This function should not be called before entering Sleep.

void SCB_Wakeup(void)

Description: Prepares Component for Active mode operation after Deep Sleep.

The “Enable wakeup from Deep Sleep Mode” selection has influence to on this function implementation:

- Checked: restores the Component Active mode configuration.
- Unchecked: enables the Component if it was enabled before enter Deep Sleep.

This function should not be called after exiting Sleep.

Side Effects: Calling the SCB_Wakeup() function without first calling the SCB_Sleep() function may produce unexpected behavior.

void SCB_SpiInit(SCB_SPI_INIT_STRUCT *config)

Description: Configures the SCB for SPI operation.

This function is **intended specifically** to be used when the SCB configuration is set to “Unconfigured SCB” in the customizer. After initializing the SCB in SPI mode, the Component can be enabled using the SCB_Start() or SCB_Enable() function.

This function uses a pointer to a structure that provides the configuration settings. This structure contains the same information that would otherwise be provided by the customizer settings.

Parameters: config: pointer to a structure that contains the following list of fields. These fields match the selections available in the customizer. Refer to the customizer for further description of the settings.

Field	Description
uint32 mode	Mode of operation for SPI. The following defines are available choices: SCB_SPI_SLAVE SCB_SPI_MASTER
uint32 submode	Submode of operation for SPI. The following defines are available choices: SCB_SPI_MODE_MOTOROLA SCB_SPI_MODE_TI_COINCIDES SCB_SPI_MODE_TI_PRECEDES SCB_SPI_MODE_NATIONAL
uint32 sclkMode	Determines the sclk relationship for Motorola submode. Ignored for other submodes. The following defines are available choices: SCB_SPI_SCLK_CPHA0_CPOL0 SCB_SPI_SCLK_CPHA0_CPOL1 SCB_SPI_SCLK_CPHA1_CPOL0 SCB_SPI_SCLK_CPHA1_CPOL1
uint32 oversample	Oversampling factor for the SPI clock. Ignored for Slave mode operation.
uint32 enableMedianFilter	0 – disable 1 – enable
uint32 enableLateSampling	0 – disable 1 – enable Ignored for slave mode.
uint32 enableWake	0 – disable 1 – enable Ignored for master mode.
uint32 rxDataBits	Number of data bits for RX direction. Different dataBitsRx and dataBitsTx are only allowed for National submode.
uint32 txDataBits	Number of data bits for TX direction. Different dataBitsRx and dataBitsTx are only allowed for National submode.
uint32 bitOrder	Determines the bit ordering. The following defines are available choices: SCB_BITS_ORDER_LSB_FIRST SCB_BITS_ORDER_MSB_FIRST
uint32 transferSeperation	Determines whether transfers are back to back or have SS disabled between words. Ignored for slave mode. The following defines are available choices: SCB_SPI_TRANSFER_CONTINUOUS SCB_SPI_TRANSFER_SEPARATED

uint32 rxBufferSize	Size of the RX buffer in bytes/words (depends on rxDataBits parameter). A value equal to the RX FIFO depth implies the usage of buffering in hardware. A value greater than the RX FIFO depth results in a software buffer. The SCB_INTR _RX_NOT_EMPTY interrupt has to be enabled to transfer data into the software buffer. For PSoC 4100 / PSoC 4200 devices, the RX and TX FIFO depth is equal to 8 bytes/words. For PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices, the RX and TX FIFO depth is equal to 8 bytes/words or 16 bytes (Byte mode is enabled).
uint8* rxBuffer	Buffer space provided for a RX software buffer: • A NULL pointer must be provided to use hardware buffering. • A pointer to an allocated buffer must be provided to use software buffering. The buffer size must equal (rxBufferSize + 1) in bytes if dataBitsRx is less or equal to 8, otherwise (2 * (rxBufferSize + 1)) in bytes. The software RX buffer always keeps one element empty. For correct operation the allocated RX buffer has to be one element greater than maximum packet size expected to be received.
uint32 txBufferSize	Size of the TX buffer in bytes/words(depends on txDataBits parameter). A value equal to the TX FIFO depth implies the usage of buffering in hardware. A value greater than the TX FIFO depth results in a software buffer. For PSoC 4100 / PSoC 4200 devices, the RX and TX FIFO depth is equal to 8 bytes/words. For PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices, the RX and TX FIFO depth is equal to 8 bytes/words or 16 bytes (Byte mode is enabled).
uint8* txBuffer	Buffer space provided for a TX software buffer: • A NULL pointer must be provided to use hardware buffering. • A pointer to an allocated buffer must be provided to use software buffering. The buffer size must equal txBufferSize if dataBitsTx is less or eqal to 8, otherwise (2* txBufferSize).
uint32 enableInterrupt	0 – disable 1 – enable The interrupt has to be enabled if software buffer is used.
uint32 rxInterruptMask	Mask of enabled interrupt sources for the RX direction. This mask is written regardless of the setting of the enable Interrupt field. Multiple sources are enabled by providing a value that is the OR of all of the following sources to enable: • SCB_INTR_RX_FIFO_LEVEL • SCB_INTR_RX_NOT_EMPTY • SCB_INTR_RX_FULL • SCB_INTR_RX_OVERFLOW • SCB_INTR_RX_UNDERFLOW • SCB_INTR_SLAVE_SPI_BUS_ERROR
uint32 rxTriggerLevel	FIFO level for an RX FIFO level interrupt. This value is written regardless of whether the RX FIFO level interrupt source is enabled.

uint32 txInterruptMask	Mask of enabled interrupt sources for the TX direction. This mask is written regardless of the setting of the enable Interrupt field. Multiple sources are enabled by providing a value that is the OR of all of the following sources to enable: • SCB_INTR_TX_FIFO_LEVEL • SCB_INTR_TX_NOT_FULL • SCB_INTR_TX_EMPTY • SCB_INTR_TX_OVERFLOW • SCB_INTR_TX_UNDERFLOW • SCB_INTR_MASTER_SPI_DONE
uint32 txTriggerLevel	FIFO level for a TX FIFO level interrupt. This value is written regardless of whether the TX FIFO level interrupt source is enabled.
uint8 enableByteMode	Ignored for all devices other than PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor. 0 – disable 1 – enable When enabled the TX and RX FIFO depth is 16 bytes. This implies that number of TX and RX data bits must be less than or equal to 8.
uint8 enableFreeRunSclk	Ignored for all devices other than PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor. Enables continuous SCLK generation by the SPI master. 0 – disable 1 – enable
uint8 polaritySs	Ignored for all devices other than PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor. Active polarity of slave select lines 0-3. This is bitmask where bit SCB_SPI_SLAVE_SELECT0 corresponds to slave select 0 polarity, bit SCB_SPI_SLAVE_SELECT1 – slave select 1 polarity and so on. Polarity constants are: SCB_SPI_SS_ACTIVE_LOW SCB_SPI_SS_ACTIVE_HIGH

uint32 SCB_SpiIsBusBusy(void)

Description: Returns the current status on the bus. The bus status is determined using the slave select signal.

- Motorola and National Semiconductor sub-modes: The bus is busy after the slave select line is activated and lasts until the slave select line is deactivated.
- Texas Instrument sub-modes: The bus is busy at the moment of the initial pulse on the slave select line and lasts until the transfer is complete.

SPI Master does not assign slave select line immediately after the first word is written into TX FIFO. It takes up to 2 SCLK clocks to assign slave select. Until this happens the bus considered not busy.

If SPI Master is configured to use "separated transfers" (see Continuous versus Separated Transfer Separation), the bus is busy during each element transfer and is free between each element transfer.

Return Value: uint32: Current status on the bus. If the returned value is nonzero, the bus is busy. If zero is returned, the bus is free. The bus status is determined using the slave select signal.

void SCB_SpiSetActiveSlaveSelect(uint32 slaveSelect)

Description: Selects one of the four slave select lines to be active during the transfer. After initialization the active slave select line is 0.

The Component should be in one of the following states to change the active slave select signal source correctly:

- The Component is disabled
- The Component has completed transfer

This function does not check that these conditions are met.

This function is only applicable to SPI Master mode of operation.

Parameters: uint32 slaveSelect: slave select line that will be active after the transfer.

Active Slave Select constants	Description
SCB_SPI_SLAVE_SELECT0	Slave select 0
SCB_SPI_SLAVE_SELECT1	Slave select 1
SCB_SPI_SLAVE_SELECT2	Slave select 2
SCB_SPI_SLAVE_SELECT3	Slave select 3

void SCB_SpiSetSlaveSelectPolarity(uint32 slaveSelect, uint32 polarity)

Description: Sets active polarity for the slave select line.

The Component should be in one of the following states to change the active slave select signal correctly:

- The Component is disabled
- The Component has completed transfer

This function does not check that these conditions are met.

Only available for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices.

Parameters: uint32 slaveSelect: slave select line to change active polarity.

Slave Select constants	Description
SCB_SPI_SLAVE_SELECT0	Slave select 0. For SPI slave mode the slave select 0 is only valid argument due to slave select placement constraint.
SCB_SPI_SLAVE_SELECT1	Slave select 1
SCB_SPI_SLAVE_SELECT2	Slave select 2
SCB_SPI_SLAVE_SELECT3	Slave select 3

uint32 Polarity: active polarity of slave select line.

Active Slave Select constants	Description
SCB_SPI_SS_ACTIVE_LOW	Slave select is active low
SCB_SPI_SS_ACTIVE_HIGH	Slave select is active high

void SCB_SpiUartWriteTxData(uint32 txData)

Description: Places a data entry into the transmit buffer to be sent at the next available bus time.

This function is blocking and waits until there is space available to put the requested data in the transmit buffer.

Parameters: uint32 txData: the data to be transmitted.

The amount of data bits to be transmitted depends on TX data bits selection (the data bit counting starts from LSB of txDataByte).

void SCB_SpiUartPutArray(const uint16/uint8 wrBuf[], uint32 count)

Description: Places an array of data into the transmit buffer to be sent.

This function is blocking and waits until there is a space available to put all the requested data in the transmit buffer.

The array size can be greater than transmit buffer size.

Parameters: const uint16/uint8 wrBuf[]: pointer to an array of data to be placed in transmit buffer. The width of the data to be transmitted depends on TX data width selection (the data bit counting starts from LSB for each array element).

uint32 count: number of data elements to be placed in the transmit buffer.

uint32 SCB_SpiUartGetTxBufferSize(void)

Description: Returns the number of elements currently in the transmit buffer.

TX software buffer is disabled: Returns the number of used entries in TX FIFO.

TX software buffer is enabled: Returns the number of elements currently used in the transmit buffer. This number does not include used entries in the TX FIFO. The transmit buffer size is zero until the TX FIFO is not full.

Return Value: uint32: Number of data elements ready to transmit.

void SCB_SpiUartClearTxBuffer(void)

Description: Clears the transmit buffer and TX FIFO.

uint32 SCB_SpiUartReadRxData(void)

Description: Retrieves the next data element from the receive buffer.

RX software buffer is disabled: Returns data element retrieved from RX FIFO. Undefined data will be returned if the RX FIFO is empty.

RX software buffer is enabled: Returns data element from the software receive buffer. Zero value is returned if the software receive buffer is empty.

Return Value: uint32: Next data element from the receive buffer. The amount of data bits to be received depends on RX data bits selection (the data bit counting starts from LSB of return value).

uint32 SCB_SpiUartGetRxBufferSize(void)

Description: Returns the number of received data elements in the receive buffer.

RX software buffer is disabled: Returns the number of used entries in RX FIFO.

RX software buffer is enabled: Returns the number of elements that were placed in the receive buffer. This does not include the hardware RX FIFO.

Return Value: uint32: Number of received data elements

void SCB_SpiUartClearRxBuffer(void)

Description: Clears the receive buffer and RX FIFO.

Global Variables

Knowledge of these variables is not required for normal operations.

Variable	Description
SCB_initVar	SCB_initVar indicates whether the SCB Component has been initialized. The variable is initialized to 0 and set to 1 the first time SCB_Start() is called. This allows the Component to restart without reinitialization after the first call to the SCB_Start() routine. If reinitialization of the Component is required, then the SCB_Init() function can be called before the SCB_Start() or SCB_Enable() function.
SCB_rxBufferOverflow	SCB_rxBufferOverflow sets when internal software receive buffer overflow was occurred.
SCB_IntrTxMask	This global variable stores TX interrupt sources after SCB_Stop() is called. Only these TX interrupt sources will be restored on a subsequent SCB_Enable() call.

Bootloader Support

The SCB Component in SPI mode can be used as a communication Component for the Bootloader. You should use the following configuration to support the SPI communication protocol from an external system to the Bootloader:

- SPI Mode: Slave
- Sub Mode: Motorola
- Data Lines: MOSI, MISO, SCLK, SS
- TX data bits and RX data bits: 8
- SCLK mode: Must match Host (boot device)
- Data rate: Must not be less than Host (boot device)

Note The slave uses input signal oversampling to allow the master to successfully communicate with the slave at a data rate lower than what is selected in the Configure dialog. However, when the Component is used for the bootloading, the selected data rate is used to calculate the byte-to-byte timeout interval. This timeout interval can be too small if the data rate, used by the master to communicate with the slave, is significantly lower than the data rate set in the Configure dialog. If the timeout interval is too small, bootloading will fail because the slave is not able to receive data before the byte-to-byte timeout expired. Refer to the SCB_CyBtldrCommRead details section for more information about byte-to-byte timeout interval and options to change it.

- Bit order: Must match Host (boot device)
- RX buffer size: Must match or be greater that maximum size of packet received from Host. The recommended RX buffer size value to select for bootloading use Bootloader Host Tool (shipped with PSoC Creator) is **64**.
- TX buffer size: Must match or be greater that maximum size of packet transmitted to the Host. The recommended TX buffer size value to select for bootloading use Bootloader Host Tool (shipped with PSoC Creator) is **64**.

For more information about the Bootloader, refer to the Bootloader Component datasheet.

The following API functions are provided for Bootloader use.

Function	Description
SCB_CyBtldrCommStart()	Starts the SPI Component and enables its interrupt.
SCB_CyBtldrCommStop()	Disables the SPI Component and its interrupt.
SCB_CyBtldrCommReset()	Resets SPI receive and transmit buffers.
SCB_CyBtldrCommRead()	Allows the caller to read data from the bootloader host (the host writes the data).
SCB_CyBtldrCommWrite()	Allows the caller to write data to the bootloader host (the host reads the data).

void SCB_CyBtldrCommStart(void)

Description: Starts the SPI Component and enables its interrupt (if TX or RX buffer size is greater than FIFO depth).

Every incoming SPI transfer is treated as a command for the bootloader.

void SCB_CyBtldrCommStop(void)

Description: Disables the SPI Component and its interrupt.

void SCB_CyBtldrCommReset(void)

Description: Resets SPI receive and transmit buffers.

cystatus SCB_CyBtldrCommRead(uint8 pData[], uint16 size, uint16 * count, uint8 timeOut)

Description: Allows the caller to read data from the bootloader host (the host writes the data). The function handles polling to allow a block of data to be completely received from the host device.

Parameters: uint8 pData[]: Pointer to the block of data to be read from bootloader host.

uint16 size: Number of bytes to be read from bootloader host.

uint16 *count: Pointer to variable to write the number of bytes actually read by bootloader host.

uint8 timeOut: Number of units in 10 ms to wait before returning because of a timeout.

Return Value: cystatus: Returns CYRET_SUCCESS if no problem was encountered or returns the value that best describes the problem. For more information, refer to the “Return Codes” section of the *System Reference Guide*.

cystatus SCB_CyBtldrCommWrite(const uint8 pData[], uint16 size, uint16 * count, uint8 timeOut)

Description: Allows the caller to write data to the bootloader host (the host reads the data). The function handles polling to allow a block of data to be completely sent to the host device.

Parameters: const uint8 pData[]: Pointer to the block of data to send to the bootloader host.

uint16 size: Number of bytes to send to bootloader host.

uint16 *count: Pointer to variable to write the number of bytes actually written to bootloader host.

uint8 timeOut: Number of units in 10 ms to wait before returning because of a timeout.

Return Value: cystatus: Returns CYRET_SUCCESS if no problem was encountered or returns the value that best describes the problem. For more information refer to the “Return Codes” section of the *System Reference Guide*.

SCB_CyBtldrCommRead details

The SPI interface does not provide start and stop conditions to define the start and end of a transfer like I^{2}C. Therefore, the following approach is used to define when command packet from the host is received:

1. To determine when the start of a packet has occurred, the RX buffer is checked at a one millisecond interval until the buffer size is non-zero or timeout is expired. As soon as at least one data element has been received the communication Component knows a packet transfer has started and immediately begins looking for the end of the packet.

2. The transfer is completed if no new data elements are received within the byte-to-byte timeout interval. This time interval is defined as the time consumed to transfer two data elements with selected data rate. It is calculated by the Component based on current data rate selection. If needed, the byte-to-byte interval can be changed by using global defines. Open project Build Settings -> Compiler -> Command line and provide global define of the interval in microseconds. For example, to change the interval to 40 microseconds:

```
-D SCB_SPI_BYTE_TO_BYTE=40
```

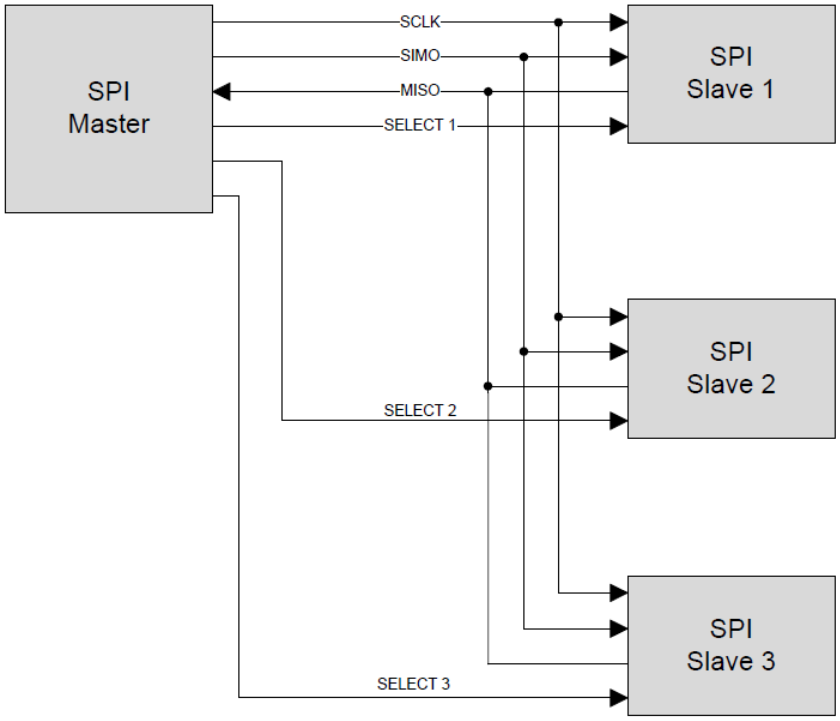
SPI Functional Description

The Serial Peripheral Interface (SPI) protocol is a synchronous serial interface, with “single-master-multi-slave” topology. Devices operate in either master or slave mode. The master initiates transfers of data frames. Multiple slaves are supported with individual slave select lines.

The SPI interface consists of four signals:

- **SCLK** – Serial clock (output from master, input to the slave).
- **MOSI** – Master output, slave input (output from the master, input to the slave).
- **MISO** – Master input, slave output (input to the master, output from the slave).
- **SELECT** – Slave select (typically an active low signal, output from the master, input to the slave).

Figure 19. SPI Bus Connections Example



Motorola sub mode operation

This is the original SPI protocol defined by Motorola. It is a full duplex protocol: transmission and reception occur at the same time.

The Motorola SPI protocol has four different modes that determine how data is driven and captured on the MOSI and MISO lines. These modes are determined by clock polarity (CPOL) and clock phase (CPHA).

- **CPHA = 0, CPOL= 0 –** Data is driven on a falling edge of SCLK. Data is captured on a rising edge of SCLK. The idle state of SCLK line is low.
- **CPHA = 0, CPOL= 1** – Data is driven on a rising edge of SCLK. Data is captured on a falling edge of SCLK. The idle state of SCLK line is high.
- **CPHA = 1, CPOL= 0** – Data is driven on a rising edge of SCLK. Data is captured on a falling edge of SCLK. The idle state of SCLK line is low.
- **CPHA = 1, CPOL= 1** – Data is driven on a falling edge of SCLK. Data is captured on a rising edge of SCLK. The idle state of SCLK line is high.

Figure 20 illustrates driving and capturing of MOSI/MISO data as a function of CPOL and CPHA.

Figure 20. SPI Motorola frame format

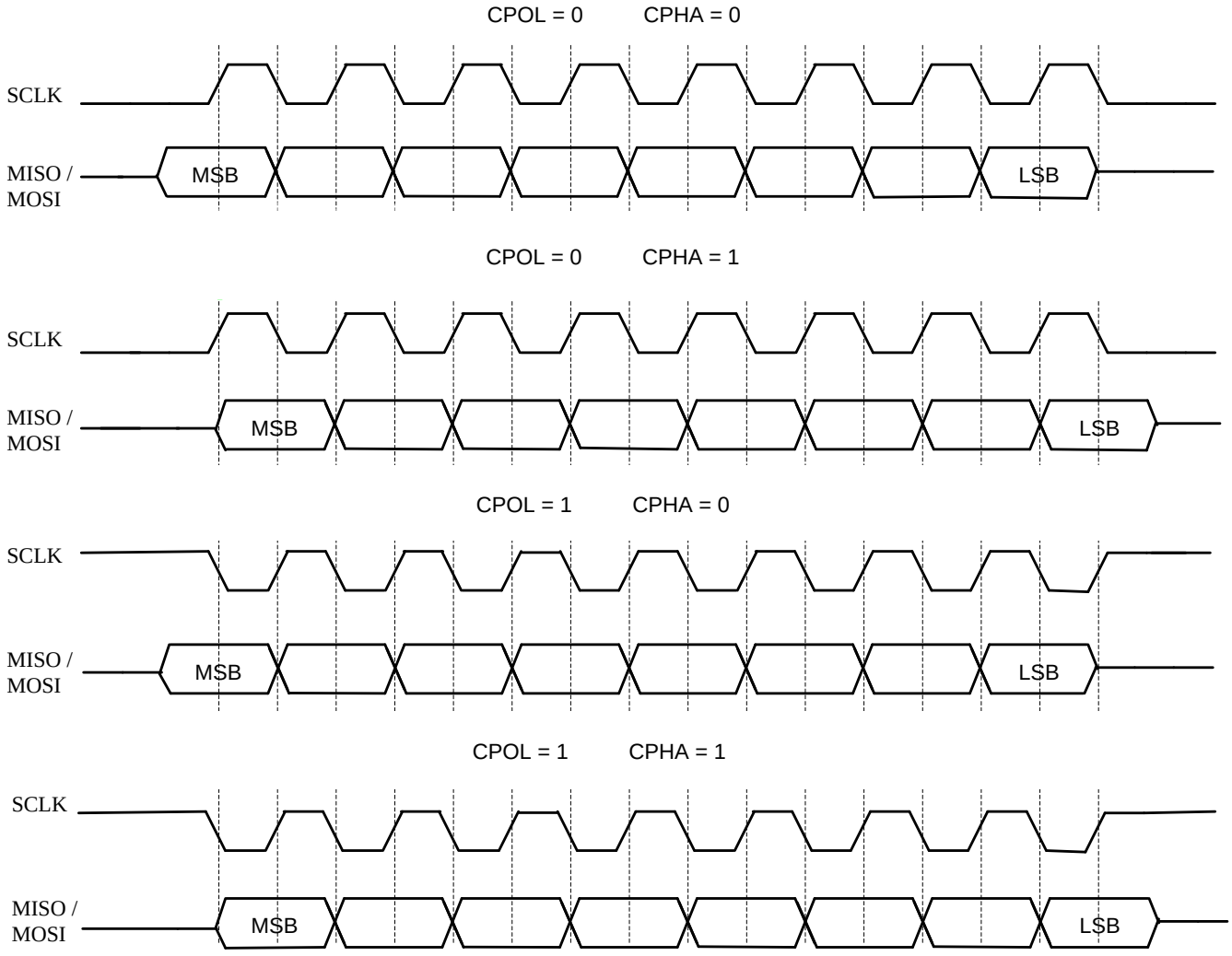
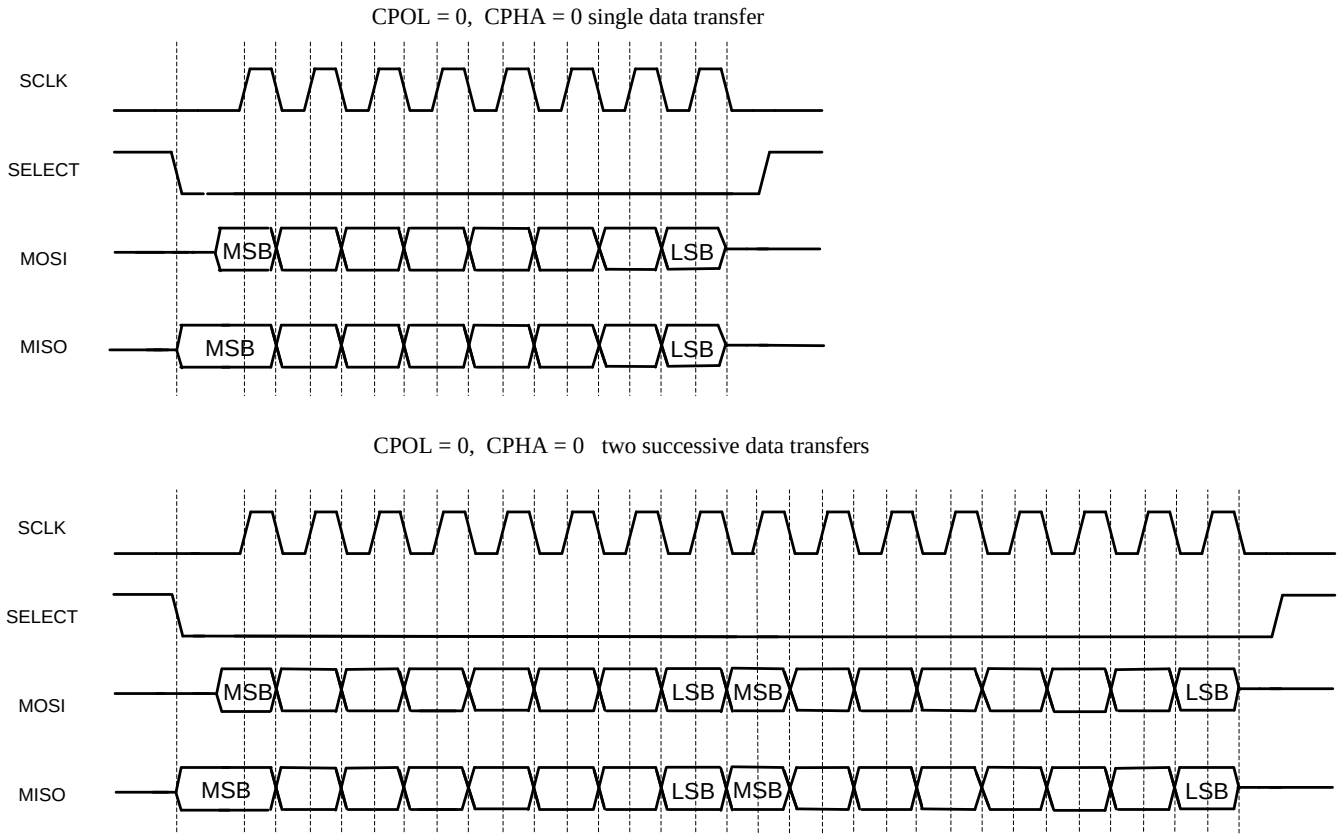


Figure 21 illustrates a single 8-bit data transfer and two successive 8-bit data transfers in mode 0 (CPOL is '0', CPHA is '0').

Figure 21. SPI Motorola Data Transfer Example



Texas Instruments sub modes operation

The Texas Instruments' SPI protocol redefines the use of the SS signal. It uses the signal to indicate the start of a data transfer, rather than a low active slave select signal. This protocol only supports CPHA = 1, CPOL= 0.

The start of a transfer is indicated by a high active pulse of a single bit transfer period. This pulse may precede the transfer of the first data frame bit on one SCLK period, or may coincide with the transmission of the first data bit. The transmitted clock SCLK is a free running clock.

Figure 22 illustrates a single 8-bit data transfer and two successive 8-bit data transfers. The SS pulse precedes the first data bit.

Note The SELECT pulse of the second data transfer coincides with the last data bit of the first data transfer.

Figure 22. TI (Precede) Data Transfer Example

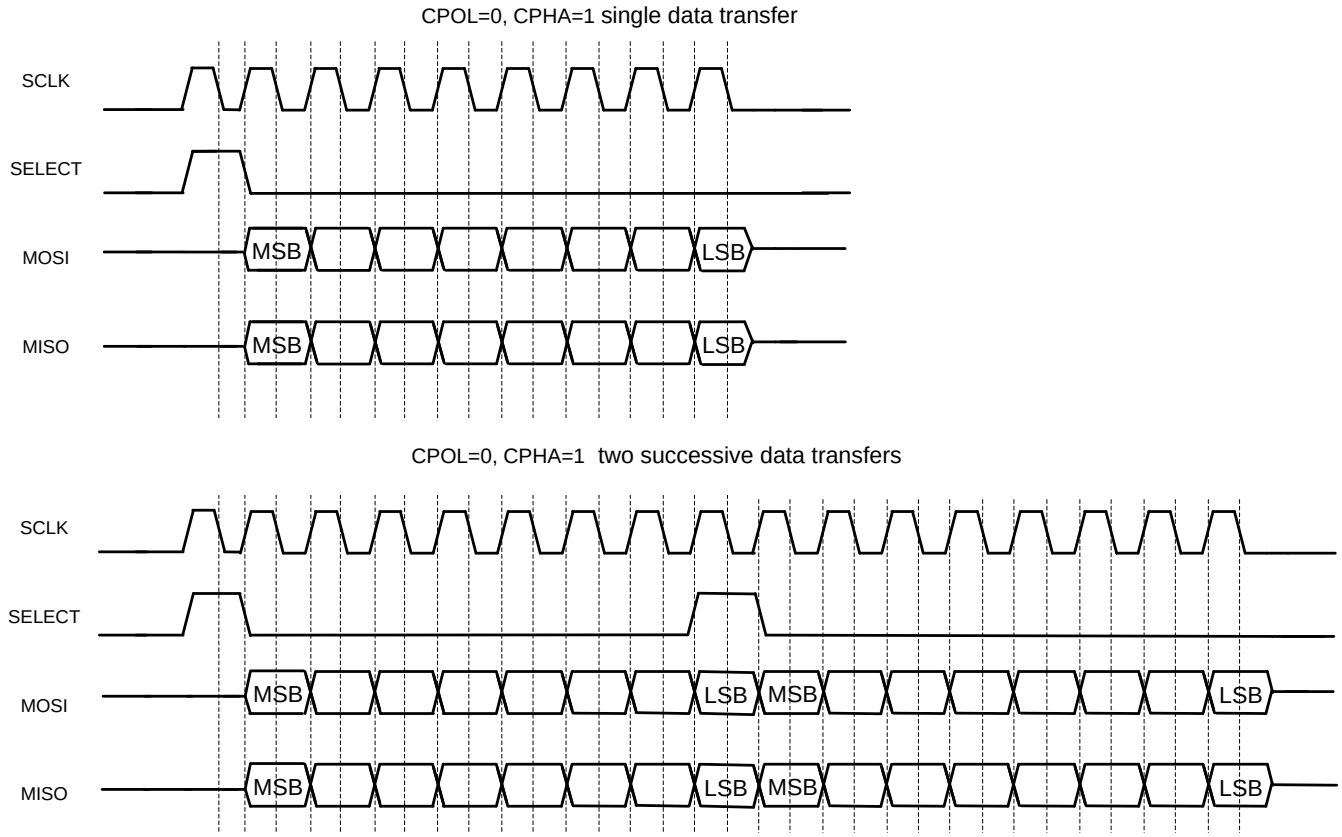
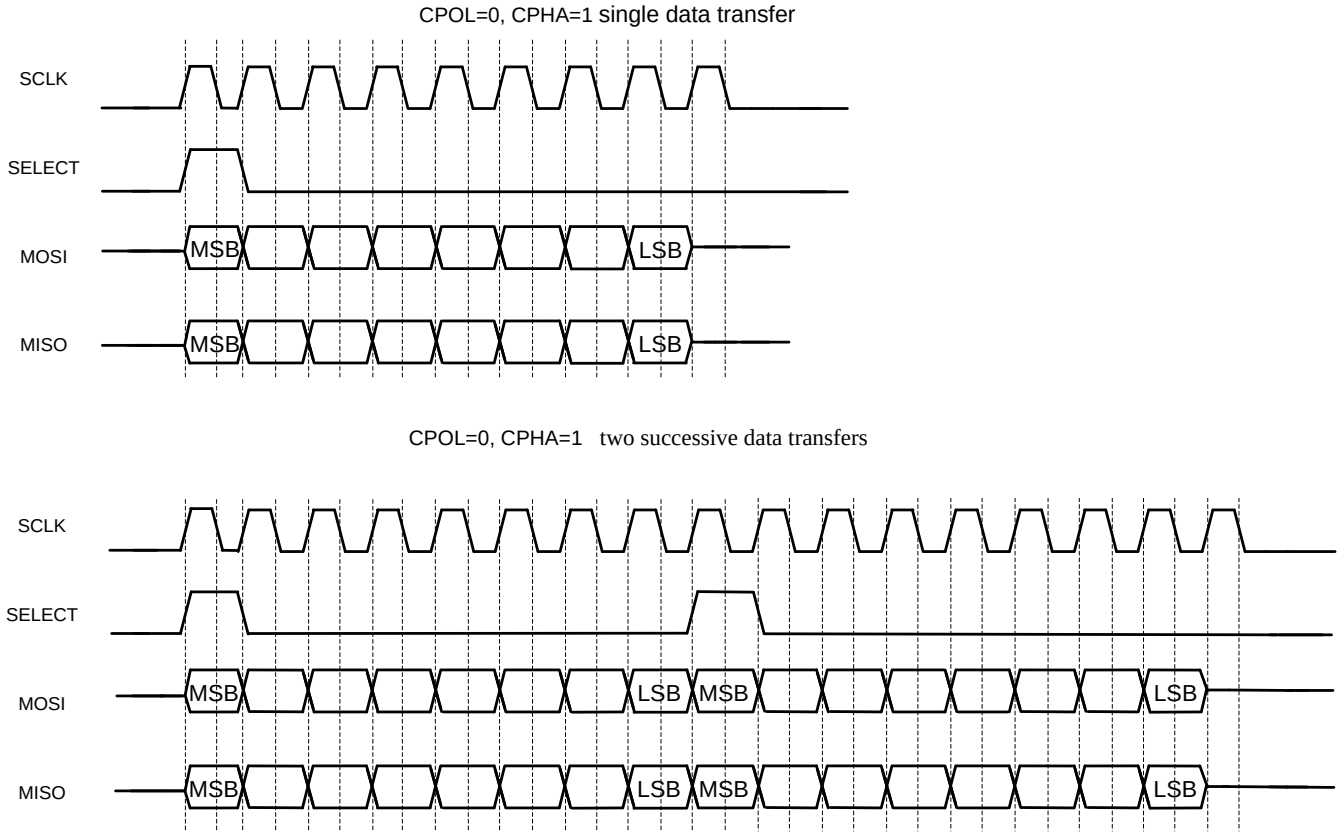


Figure 23 illustrates a single 8-bit data transfer and two successive 8-bit data transfers. The SS pulse coincides with the first data bit.

Figure 23. TI (Coincide) Data Transfer Example



National Semiconductor's (Microwire) sub modes operation

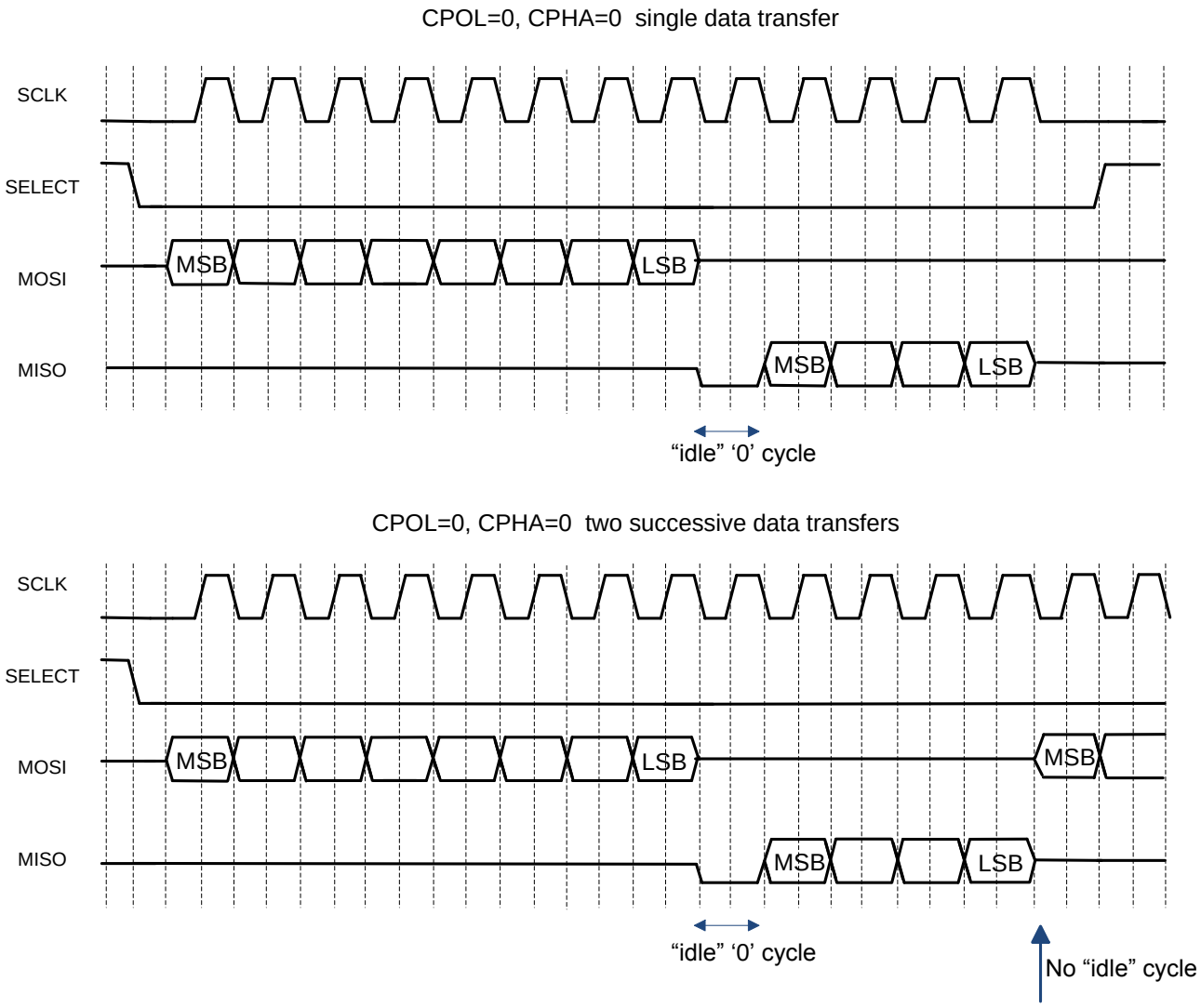
The National Semiconductor's Microwire protocol is a half-duplex protocol. Rather than transmission and reception occurring at the same time, transmission and reception take turns (transmission happens before reception). A single "idle" bit transfer period separates transmission from reception. This protocol only supports CPHA = 1, CPOL= 0.

Note The successive data transfers (transmission and reception) are NOT separated by an "idle" bit transfer period.

The transmission data transfer size and reception data transfer size may differ.

Figure 24 illustrates a single data transfer and two successive data transfers. In both cases the transmission data transfer size is 8 bits and the reception transfer size is 4 bits.

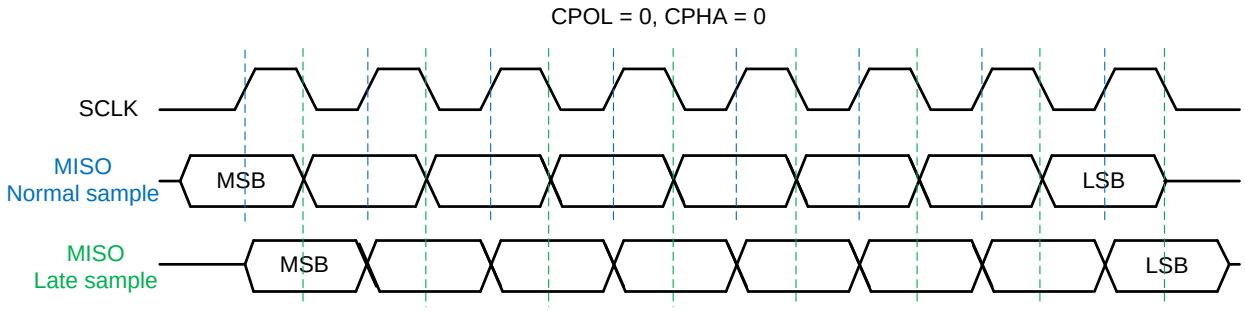
Figure 24. National Semiconductor's Microwire Data Transfer Example



MISO late sampling

The MISO is captured by Master by half of SCLK period later (on the alternate serial clock edge). Late sampling addresses the round-trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master.

Figure 25. Late MISO sampling example



Slave select lines

The slave select lines are used by the master to notify the slave device that it will communicate with it. The master has control of four slave select lines, and one of them has to be chosen as active before starting communication. To start communication, the data is written into the TX FIFO. The master hardware then asserts the active slave select line and sends data to the MOSI.

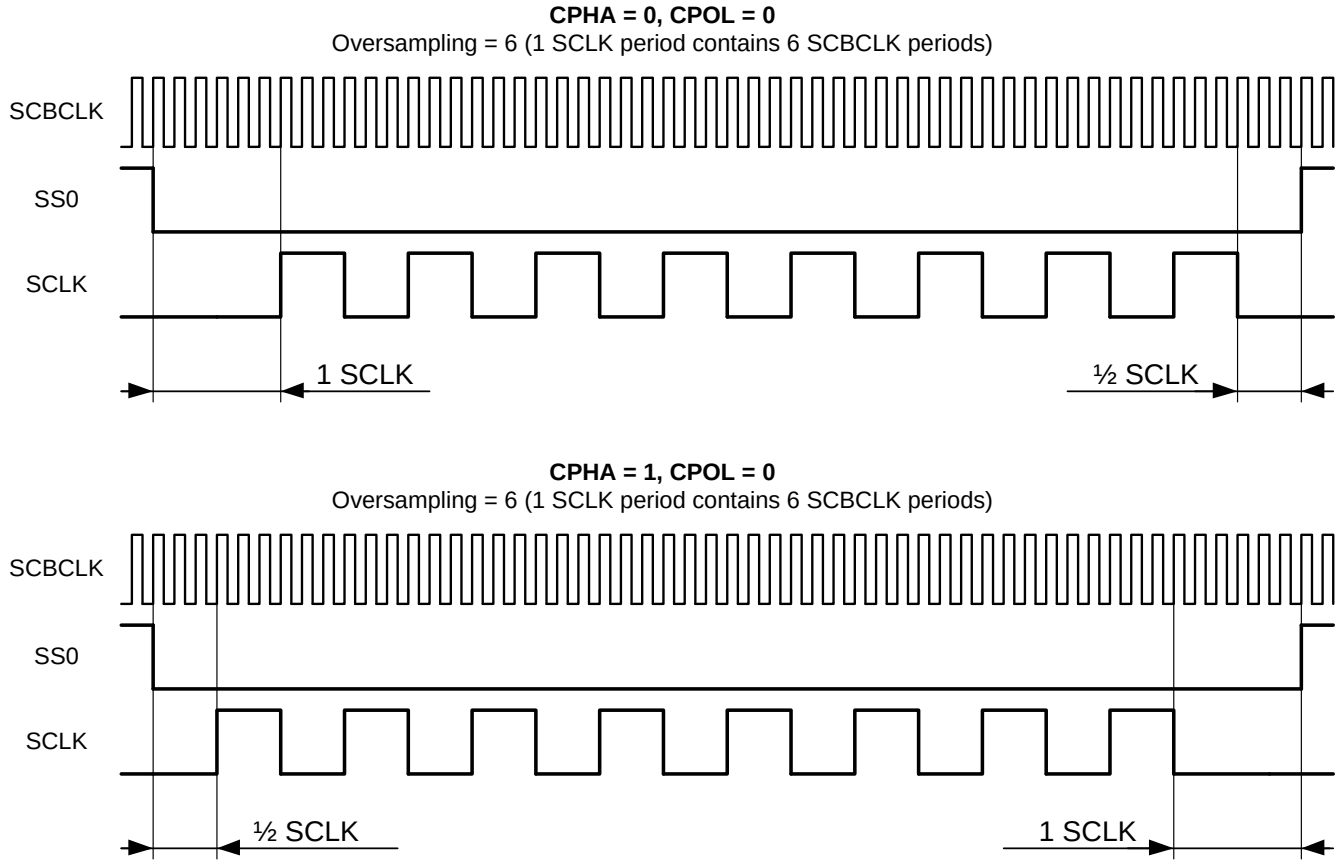
There are cases when firmware control of the slave select line is desired. In this case, the slave select lines that are controlled by the master hardware need to be deactivated. There are two options to do this:

- Set the active slave select line to one that is not routed out to the pin. This option is recommended when less than four slave select lines are used by the master. Example: SPI master consumes 3 slave select lines SS0, SS1 and SS2. Call SCB_SpiSetActiveSlaveSelect(SCB_SPIM_ACTIVE_SS3) to deactivate hardware controlled slave select lines SS0-SS2.
- Change the source of the control of the active slave select line in HSIOM (High Speed I/O Matrix) from the SCB SPI interface to GPIO (CPU firmware control). Refer to the High-Speed I/O Matrix description in the *Technical Reference Manual (TRM)* for more information. This option is recommended when the master uses four slave select lines or when multiplexing between hardware controlled and firmware controlled slave select lines is required.

SELECT and SCLK Timing Correlation

The master activates SELECT before starting the transfer and makes it inactive when the transfer is completed for Motorola and National Semiconductor's (Microwire) modes. A minimum time is guaranteed before SELECT activation and the first SCLK edge and SELECT deactivation and last SCLK edge. This time depends on the master sampling edge, which is defined by CPHA settings. Thus, two combinations are available.

Figure 26. SELECT and SCLK Timing Correlation (PSoC 4100/PSoC 4200)

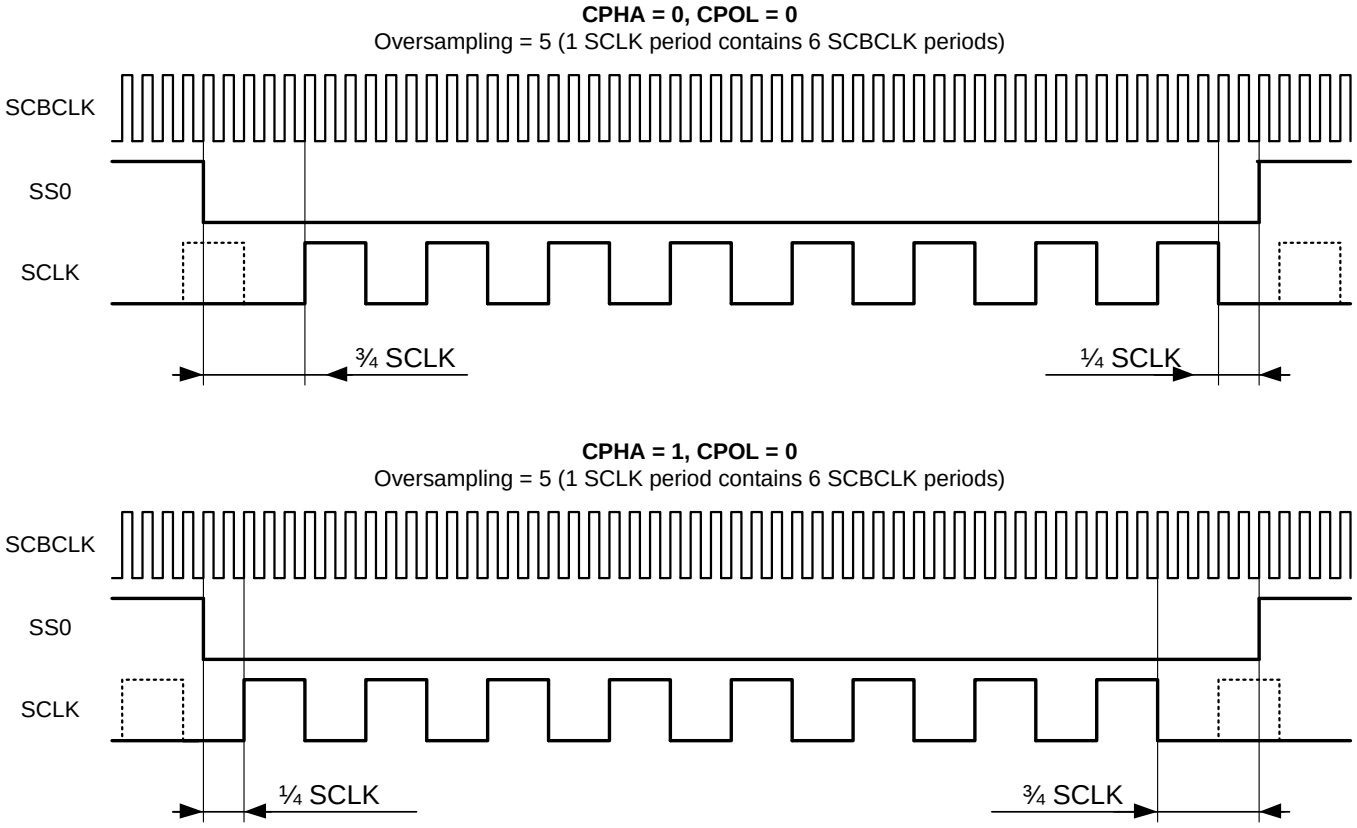


For example above: OversamplingReg = 6 – 1 = 5.
1 * SCLK = (5 + 1) * SCBCLK = 6 * SCBCLK,
½ * SCLK = ((5 / 2) + 1) * SCBCLK) = (2 + 1) * SCBCLK = 3 * SCBCLK.

Note The value 1 * SCLK is equal to ((OversamplingReg + 1) * SCBCLK, where OversamplingReg = Oversampling – 1.
The value ½ * SCLK is equl to ((OversamplingReg / 2) + 1) * SCBCLK.
The result of any division operation is rounded down to the nearest integer.
Note The provided timings are guaranteed by SCB block but do not take into account signal propagation time from SCB block to pins.

Note PSoC 4100 / PSoC 4200 devices support only SCLK gated and active low SELECT polarity.

Figure 27. SELECT and SCLK Timing Correlation (PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor)



For example above: OversamplingReg = 6 – 1 = 5.
¾ * SCLK = ((5 / 2) + 1) + (5 / 4 + 1)) * SCBCLK = (3 + 2) * SCBCLK = 5 * SCBCLK.
¼ * SCLK = ((5 / 4) + 1) * SCBCLK = 2 * SCBCLK.

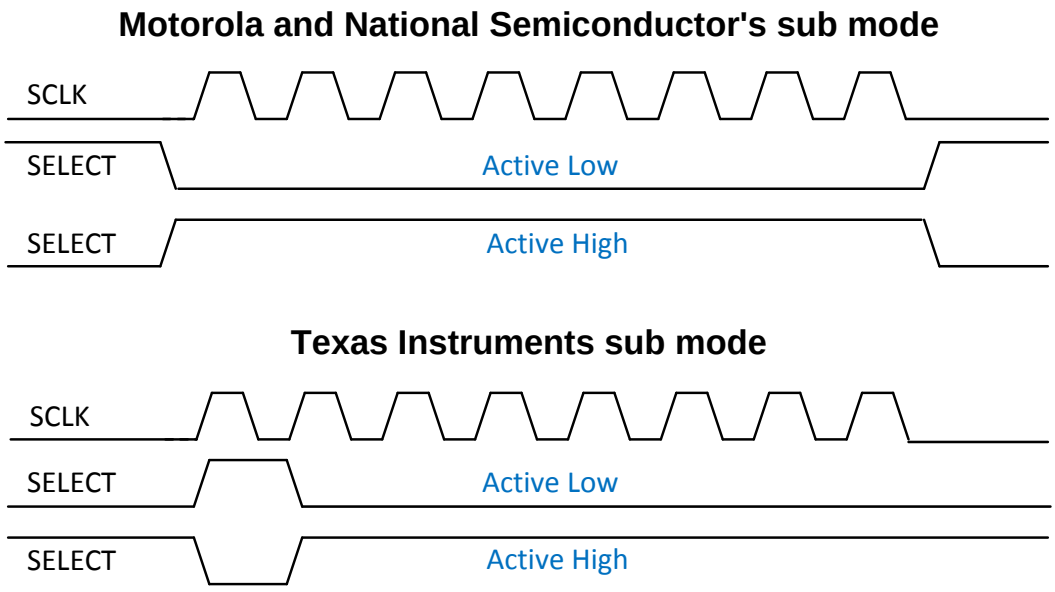
Note The value ¾ * SCLK is equal to (((OversamplingReg / 2) + 1) + (OversamplingReg / 4) + 1)), where OversamplingReg = Oversampling – 1.
The value ¼ * SCLK is equal to ((OversamplingReg / 4) + 1).
The result of any division operation is rounded down to the nearest integer.
Note The provided timings are guaranteed by SCB block but do not take into account signal propagation time from SCB block to pins.

Note PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices support SCLK gated and free running, as well as active low and high SELECT polarity. For all configurations, the same correlation is preserved.

SELECT polarity

The SELECT line polarity for PSoC 4100 / PSoC 4200 devices is active low. PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices provide the capability to select the active polarity of the line as active low or active high.

Figure 28. SELECT line polarity



Continuous versus Separated Transfer Separation

During separated data transfer, the SELECT line always changes from active to inactive state between the individual data frames until completion of the transfer.

During continuous data transfer, the individual data frame is not necessarily separated by the SELECT line inactivation. At the start of data transfer, the SELECT line is activated and keeps its state active until the end of transfer. The end of transfer is defined as all data from the TX FIFO and shifter register has been sent out. The alternative approach is to use the SPI Done interrupt source (refer to the Interrupt sources section to understand the limitations of this approach). Figure 21 on page 115 illustrates two continuous 8-bit data transfers in SCLK mode: CPHA=0, CPOL= 0.

FIFO depth

The hardware provides two FIFOs. One is used for the receive direction, RX FIFO, and the other for transmit direction, TX FIFO. The FIFO depth is 8 data elements. The width of each data element is 16 bits. The data frame width is configurable from 4-16 bits. One element from the FIFO is consumed regardless of the data frame width.

PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices provide the ability to double the FIFO depth to be 16 data elements when the data frame width is 4-8 bits.

Software Buffer

Selecting RX or TX Buffer Size values greater than the FIFO depth enables usage of the RX or TX FIFO and a circular software buffer. An array of the requested size is allocated internally by the Component for the TX software buffer. The allocated array for RX software buffer has one extra element that remains empty while in operation. Keeping this element empty simplifies circular buffer operation. The interrupt option is automatically set to Internal, and the RX or TX interrupt source is reserved to provide software buffer operation.

The internal interrupt is connected to the interrupt output. This interrupt runs a predefined interrupt service routine. Its main purpose is to provide interaction between software buffers and hardware RX or TX FIFO. The software buffer overflow can happen only for the RX direction. The data elements read from the RX FIFO that do not fit into the software buffer are discarded. This event is reported via global variable SCB_rxBufferOverflow. For the TX direction, the provided APIs do not allow the software buffer overflow.

Interrupts

When **RX buffer size** or **TX buffer size** is greater than the FIFO depth, the **RX FIFO not empty** or **TX FIFO not full** interrupt sources are reserved by the Component for the internal software buffers operations. **Do not clear or disable them** because it causes incorrect software buffer operation. However, it is the user's responsibility to clear interrupt events from other enabled interrupt sources because they are not cleared automatically. Create a custom function that clears these interrupt sources and register it using SCB_SetCustomInterruptHandler(). Each time an internal interrupt handler executes, the custom function is called before handling software buffer operation.

In case **RX buffer size** or **TX buffer size** is equal to the FIFO depth instead of software buffer only the hardware TX or RX FIFO is used. In the **Internal** interrupt mode the interrupts are not cleared automatically. It is user responsibility to do this. The **External** or **None** interrupt selection is preferred in this case.

Low power modes

The Component in SPI mode is able to be a wakeup source from Sleep and Deep Sleep low power modes.

Sleep mode is identical to Active from a peripheral point of view. No configuration changes are required in the Component or code before entering/exiting this mode. Any communication intended for the slave causes an interrupt to occur and leads to wakeup. Any master activity that causes an interrupt to occur leads to wakeup.

The master mode is not able to be a wakeup source from Deep Sleep. This capability is only available in slave mode. Deep Sleep mode requires that the slave be properly configured to be a

wakeup source. The Enable wakeup from Deep Sleep Mode must be checked in the SPI configuration dialog. The SCB_Sleep() and SCB_Wakeup() functions must be called before/after entering/exiting Deep Sleep.

The content of TX and RX FIFOs is cleared when the device enters Deep Sleep mode. Therefore, received data should be stored in the SRAM buffer and transmit data should be transferred before entering Deep Sleep mode to avoid data loss. Note that functions that return TX or RX buffer size (SCB_SpiUartGetTxBufferSize() / SCB_SpiUartGetRxBufferSize()) might return different values for hardware and software buffer after exit Deep Sleep: for hardware buffer returned value is always 0 (because FIFOs content is cleared) whereas for software buffer it is equal to number of bytes in available in the Component SRAM buffer. This is applies to both **Master** and **Slave** modes.

In **Master** mode, the ongoing transfer is stopped asynchronously when the SCB_Sleep() API is called because this function disables the Component. The following code is suggested to ensure that transfer is completed before entering Deep Sleep mode. It occurs when all data elements have been transferred from the software buffer (if utilized), TX FIFO, and shift register. Also, the slave select line must be deactivated. This method works reliably for any choice of slave select Transfer separation configuration.

```
/* Wait until SPI Master completes transfer data */
while (0u != (SCB_SpiUartGetTxBufferSize() + SCB_GET_TX_FIFO_SR_VALID))
{
}

/* Wait until SPI Master deactivates slave select to ensure that the last
* data element has been completely tranferred.
*/
while (0u != SCB_SpiIsBusBusy())
{
}

/* SPI Master is ready to enter Deep Sleep mode. */
SCB_Sleep();
CySysPmDeepSleep();
```

In **Slave** mode, data transmission is stopped asynchronously while the device enters Deep Sleep mode. The moment that the stop occurs depends on the Enable wakeup from Deep Sleep Mode option. When the option is disabled, the SCB_Sleep() API disables the Component and the slave stops driving the MISO line at that moment. Otherwise, when the Enable wakeup from Deep Sleep Mode option is enabled, the slave stops driving the MISO line at the moment when the device enters Deep Sleep mode.

The slave wakes up the device from Deep Sleep on detecting slave select activation. Waking up takes time ($T_{DEEPSLEEP}$) and the ongoing SPI transfer is negatively acknowledged – "0xFF" bytes are sent out on the MISO line, the data on MOSI is ignored. The master must poll the Component again after the device wake-up time is passed and data is loaded in the RX buffer.

The following code is suggested to ensure that SPI slave does not communicate with SPI master and ready to enter Deep Sleep mode.

```
/* Check if there is data in the RX buffer to handle. */
if (0u == SCB_SpiUartGetRxBufferSize())
{
    /* Enter critical section to force all enabled and active interrupts become
    * pending. It is required to not miss any activity that should wake up
    * device before CySysPmDeepSleep() is called.
    */
    intState = CyEnterCriticalSection();

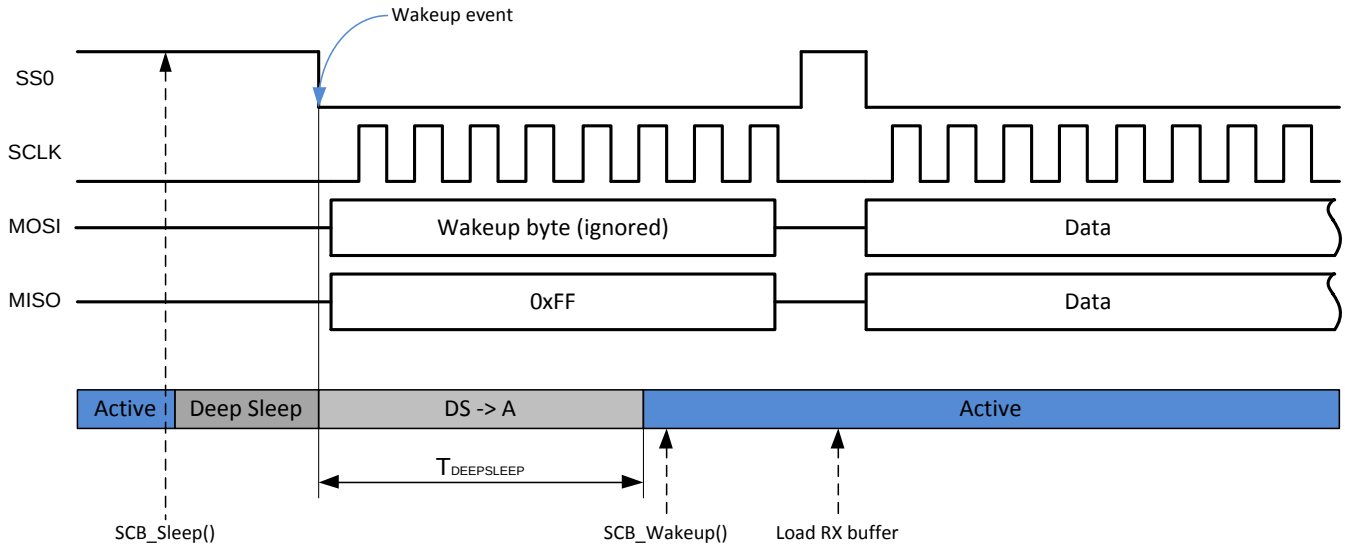
    /* Clear and enable SPI wakeup interrupt source.
    * Clear operation is required because SPI wakeup source is activated
    * while active mode communication.
    */
    SCB_Sleep();

    /* Enter Deep Sleep only if SPI bus is in idle state after SPI wakeup
    * interrupt source was cleared.
    */
    if (0u == SCB_SpiIsBusBusy())
    {
        CySysPmDeepSleep();
    }

    /* Exit critical section to allow interrupt handling. */
    CyExitCriticalSection(intState);

    /* Disable SPI wakeup interrupt source. */
    SCB_Wakeup();
}
```

Figure 29. SPI Slave is awaken up from Deep Sleep (Motorola, CPHA = 0, CPOL = 0)



Slave data rate calculations

The SPI GUI calculates the actual data rate for master or slave devices. This value is based on the parameters of the Component and does not take to account such factors as: parameters of external master or slave device as well as PCB delays. The master and slave parameters for PSoC4 can be found in the DC and AC Electrical Characteristics of this document or Device datasheet.

The main factor limiting the maximum data rate between master and slave is the round trip path delay. This delay includes the PCB delay from the falling edge of SCLK at the pin of the master to the SCLK pin of the slave, the internal slave delay from the falling edge of SCLK to MISO transition, the PCB delay from the slave MISO pin to the master MISO pin, and the master setup time. The following equation takes to account delays listed above:

$$t_{ROUND_TRIP_DELAY} = t_{SCLK_PD_PCB} + t_{DSO_SLAVE} + t_{MISO_PD_PCB} + t_{DSI_MASTER}$$

- $t_{SCLK_PD_PCB}$ is the PCB path delay of SCLK from the pin of the master device to the pin of the slave device.
- t_{DSO_SLAVE} is the time it takes the slave to change MISO after SCLK clock driving edge is captured. This parameter commonly listed in the slave device datasheet.
- $t_{MISO_PD_PCB}$ is the PCB path delay of MISO from the pin of the slave device to the pin of the master device.
- t_{DSI_MASTER} is the setup time of MISO signal to be sampled correctly by the master (the MISO must be valid before SCLK clock capturing edge). This parameter commonly listed in the master device datasheet.

When $t_{ROUND_TRIP_DELAY}$ was calculated, the maximum communication data rate between master and slave can be defined as following:

f_{SCLK} (max) = 1 / (2* $t_{ROUND_TRIP_DELAY}$)

The assumption is made that master samples the MISO signal a half SCLK period after the driving edge.

When master is capable of sampling the MISO signal a full of SCLK period after the driving edge (late MISO sampling) the communication data rate is doubled and calculated as following:

f_{SCLK} (max) = 1 / $t_{ROUND_TRIP_DELAY}$

Refer to the section MISO late sampling for more information about MISO sampling by the master device.

As an example the f_{SCLK} (max) is calculated for SCB SPI Master and Slave implemented on PSoC 4100/PSoC 4200 devices. The design clock settings are following: IMO = HFCLK = SYSCLK = 48 MHz. The clock source frequency connected to the SCB SPI Slave and Master Components is equal to 48MHz as well.

$t_{DSO_SLAVE} = T_{DSO} = 42 + 3*t_{SCB} = 42 + 3 * (1 / 48\ MHz) = 105$ ns

$t_{DSI_MASTER} = T_{DSI} = 20$ ns (Full clock, late MISO Sampling used)

For simplicity of the calculations assume that $t_{SCLK_PD_PCB} = 0$ ns and $t_{MISO_PD_PCB} = 0$ ns.

$t_{ROUND_TRIP_DELAY} = t_{SCLK_PD_PCB} + t_{DSO_SLAVE} + t_{MISO_PD_PCB} + t_{DSI_MASTER} = 0 + 105 + 20 + 0 = 125$ ns

f_{SCLK} (max) = 1 / $t_{ROUND_TRIP_DELAY}$ = 1 / 125 ns = 8 MHz

The SPI master is capable to generate maximum $F_{SPI} = 8$ MHz and accordingly to calculation above the MISO line will be sampled properly for this data rate.

For real applications the PCB delays would need to be added, and t_{DSO_SLAVE} and t_{DSI_MASTER} adjusted to match the real master or slave device.

DMA Support

DMA is only available in PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC Analog Coprocessor devices.

The SPI mode provides interface to DMA controller. The signals for transmit and receive direction can be used to trigger a DMA transfer. To enable this signal, the “RX output” or “TX output” option must be enabled on the Component Advanced parameter tab. The RX and TX trigger output signals are hard-wired to the DMA controller; their connection to another source will result in a build error. These signals are level sensitive and require the RX or TX FIFO level to be set. The signal behavior for the triggers is as follows:

- RX trigger output – the signal remains active until the number of data elements in the RX FIFO is greater than the value of RX FIFO level.

- TX trigger output – the signal remains active until the number of data elements in the TX FIFO is less than the value of TX FIFO level.

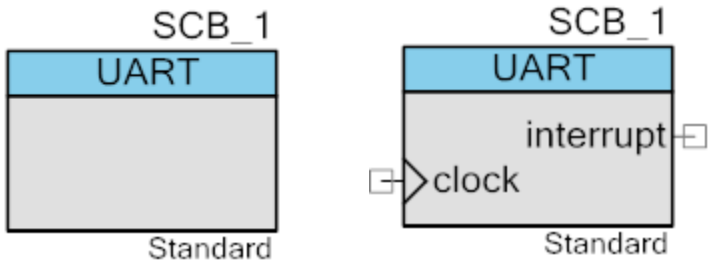
The following table specifies what DMA Component configuration should be used when it is connected to the SCB (SPI mode) Component.

DMA Source / Destination name	Direction	Source / Destination transfer width	DMA request signal	DMA trigger type	Description
SCB_RX_FIFO_RD_PTR	Source	Word / Byte or Halfword	rx_tr_out	Level sensitive	Receive FIFO
SCB_TX_FIFO_WR_PTR	Destination	Data bits / Byte or Halfword	tx_tr_out	Level sensitive	Transmit FIFO

Note If the number of data bits selected is less or equal to 8 bits the transfer data element width is byte, if the number of data bits is between 9 and 16 bits the width is halfword.

Note The SCB (SPI mode) clears request signal within 4 SYSCLK cycles therefore level sensitive configuration of DMA has to be “wait 4 SYSCLK”.

UART



The UART provides asynchronous communications commonly referred to as RS-232. Three different UART-like serial interface protocols are supported:

- UART – this is the standard UART.
  - UART Hardware flow control
- SmartCard – similar to UART, but with the possibility to send a negative acknowledgement.
- IrDA – modification to the modulation scheme used for infrared communication.

Input/Output Connections

This section describes the various input and output connections for the SCB Component. An asterisk (*) in the list of terminals indicates that the terminals may be hidden on the symbol under the conditions listed in the description of that terminals.

clock – Input*

Clock that operates this block. The presence of this terminal varies depending on the Clock from terminal parameter.

interrupt – Output*

This signal can only be connected to an interrupt Component or left unconnected. The presence of this terminal varies depending on the Interrupt parameter.

rx_tr_out – Output*

This signal can only be connected to a DMA channel Component. This signal is used to trigger a DMA transaction. The output of this terminal is controlled by the RX FIFO level. The presence of this terminal varies depending RX Output parameter.

tx_tr_out – Output*

This signal can only be connected to a DMA channel Component. This signal is used to trigger a DMA transaction. The output of this terminal is controlled by the TX FIFO level. The presence of this terminal varies depending TX Output parameter.

Internal Pins Configuration

The UART RX, TX, CTS, RTS and TX_RX pins are buried inside Component: SCB_rx (SCB_rx_wake), SCB_tx, SCB_cts, SCB_rts and SCB_tx_rx. These pins are buried because they use dedicated connections and are not routable as general purpose signals. Refer to the *I/O System* section in the device *Technical Reference Manual (TRM)* for more information.

Note The instance name is not included into the Pin Names provided in the following table.

Table 10 UART Pins Configuration

Pin Name	Direction	Drive Mode	Initial Drive State	Threshold	Slew Rate	Descriptiion
rx / rx_wake	Input	High Impedance Digital	Low	CMOS	–	The rx or rx_wake input pin receives the serial data from another device on the serial bus. This pin presents if the Mode parameter is Standard or IrDA and Direction is set to **RX Only** or **TX + RX**. When Enable wakeup from Deep Sleep Mode is checked the rx pin replaced with rx_wake pin which has the same configuration except interrupt on falling edge is enabled for device wakeup. The pin output enable is tied to 0 to make pin state High-Z. The Drive Mode settings has no effect.
cts	Input	High Impedance Digital	Low	CMOS	–	The cts input pin accepts notification that another device is ready to receive data. This pin presents if the CTS parameter is enabled. The pin output enable is tied to 0 to make pin state High-Z. The Drive Mode settings has no effect.
tx	Output	Strong Drive	High	–	Fast	The tx_out output pin drives the output serial data to another device on the serial bus. This pin presents if the Mode parameter is Standard or IrDA and Direction is set to **TX Only** or **TX + RX**. The pin output enable is tied to 1 therefore drive mode and output signal detemines the pin state.
rts	Output	Strong Drive	High	–	Fast	The rts output pin notifies another device that this device is ready to receive data. This pin presents if the RTS parameter is enabled. The pin output enable is tied to 1; therefore, drive mode and output signal detemine the pin state.
rx_tx	Bidirectional	Open Drain Drvies Low	High	CMOS	Fast	The rx_tx bi-directional pin receives and transmits data from/to another device on the bus. This pin presents if the Mode parameter is SmartCard. The pin output enable is controlled in such way that internal pull-up can be used (the pin Drive mode has to be changed to Resistive pull-up).

The Input threshold level for **input pins** is CMOS which should be used for the vast majority of application connections.

The Input Buffer for **output pins** is disabled so as not to cause current linkage in low power mode. Reading the status of these pins always returns zero. To get the current status, the input buffer must be enabled before a status read.

The other **input pins** and **output pins** parameters are set to default. Refer to pin Component datasheet for more information about default parameters values.

To change UART buried pins configuration the pin's Component APIs should be used or direct pin registers configuration. For example:

```
/* Change UART TX pin drive mode to Open Drain Drives Low. */
SCB_tx_SetDriveMode(SCB_tx_DM_OD_LO);
```

Note Refer to Table 10 on page 130 to ensure that Drive Mode settings are not overridden by the SCB block connection to pin.

Glitch Avoidance at System Reset

The UART outputs are in High Impedance Digital state when device is coming out of System Reset this can cause glitches on the outputs. This is important if you are concerned with UART TX or RTS output pins activity at either chip startup or when coming out of Hibernate mode. The external pull-up or pull-down resistor has to be connected to the output pin to keep it in the inactive state.

The inactive state of UART TX pin is high and pull-up resistor has to be connected. The inactive state of UART RTS pin depends on RTS Polarity parameter.

The Component takes care and sets UART TX and RTS outputs in the inactive state when Component is disabled or in Deep Sleep mode.

SmartIO support

The following connections are shown only if the Enable SmartIO support option is enabled. Additional visibility conditions are listed in the input and output description. Only the Pin or SmartIO Component is allowed to be connected to these terminals.

Note The Component performs synchronization of the inputs internally therefore **Sync Input** option in the Digital Input Pin Component must be set to **Transparent**.

*rx_in **

The rx_in input carries the input serial data from another device on the serial bus. This input is visible if the Mode parameter is Standard or IrDA and Direction is set to **RX Only** or **TX + RX**. It must be connected if visible.

*cts_in **

The cts_in input notifies that another device is ready to receive data. This input is visible when the CTS parameter is enabled. It must be connected if visible.

*tx_out **

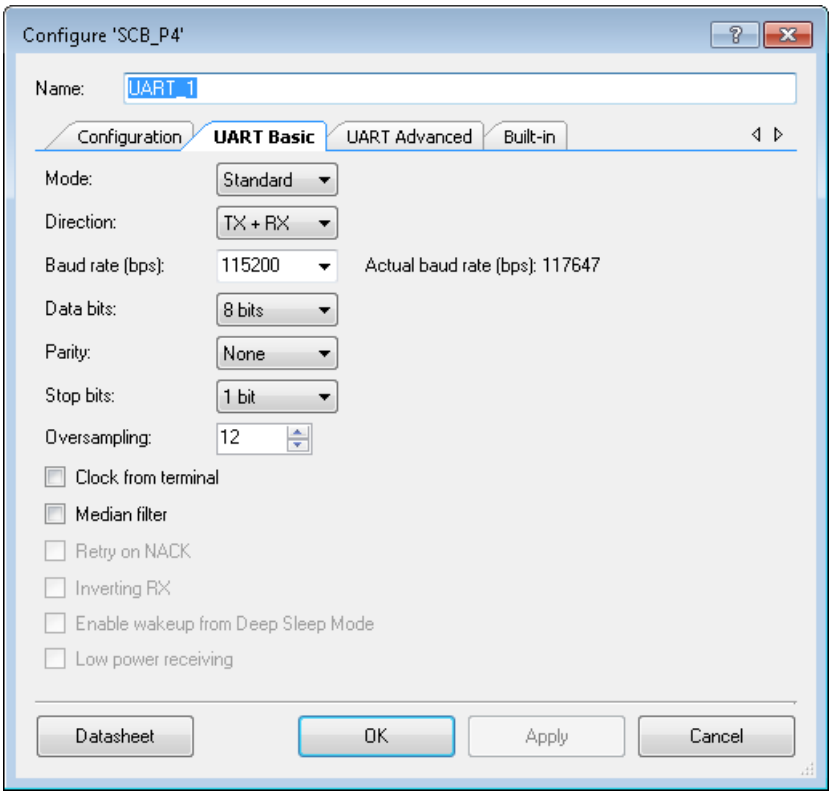
The tx_out output carries the output serial data to another device on the serial bus. This output is visible if the Mode parameter is Standard or IrDA and Direction is set to **TX Only** or **TX + RX**.

*rts_out **

The rts_out output notifies another device that your device is ready to receive data. This output is visible when the RTS parameter is enabled.

Refer to section Internal Pins Configuration for more information about UART pins configuration.

Basic UART Parameters



The **UART Basic** tab contains the following parameters:

Mode

This option determines the operating mode of the UART: Standard, SmartCard or IrDA. The default mode is **Standard**.

Direction

This parameter defines the functional Components you want to include in the UART. This can be setup to be a bidirectional **TX + RX** (default), Receiver (**RX only**) or Transmitter (**TX only**).

Baud rate

This parameter defines the baud-rate configuration of the hardware for baud rate generation up to 921600. The actual baud rate may differ based on available clock frequency and Component settings. This parameter has no effect if the **Clock from terminal** parameter is enabled. The default is 115200.

Note The integer clock divider is used to provide the desired internal clock frequency to obtain the specified baud rate (Clock from terminal option is disabled). To use a different clock source configuration (for example: fractional clock divider), the clock must be provided externally to the Component by enabling the Clock from terminal option.

Actual baud rate

The actual data rate displays the data rate at which the Component will operate with current settings. The factors that affect the actual data rate calculation are: the accuracy of the Component clock (internal or external) and oversampling factor. When a change is made to any of the Component parameters that affect actual data rate, it becomes unknown. To calculate the new actual data rate press the Apply button

Data bits

This parameter defines the number of data bits transmitted between start and stop of a single UART transaction. Options are **5**, **6**, **7**, **8** (default), or **9**.

- Eight data bits is the default configuration, sending a byte per transfer.
- The 9-bit mode does not transmit 9 data bits; the ninth bit takes the place of the parity bit as an indicator of address or data.

Parity

This parameter defines the functionality of the parity bit location in the transfer. This can be set to **None** (default), **Odd** or **Even**.

Stop bits

This parameter defines the number of stop bits implemented in the transmitter. This parameter can be set to **1** (default), **1.5** or **2** data bits.

Oversampling

This parameter defines the oversampling factor of the UART interface; the number of the Component clocks within one UART bit time. Oversampling factor is used to calculate the internal Component clock frequency required to achieve this amount of oversampling for the selected Data rate. An oversampling factor between 8 and 16 is the range of valid values. The default is 12.

For **IrDA** mode the oversampling values are predefined and Median filter is always enabled.

Clock from terminal

This parameter allows choosing between an internally configured clock (by the Component) or an externally configured clock (by the user) for Component operation. Refer to the Oversampling section to understand relationship between Component clock frequency and the Component parameters.

When this option is enabled the Component does not control the data rate, but displays the actual data rate based on the user-connected clock source frequency and the Component oversampling factor. When this option is not enabled the clock configuration is provided by the Component. The clock source frequency is calculated or selected by the Component based on the Data rate parameter and Oversampling factor.

Note PSoC Creator is responsible for providing requested clock frequency (internal or external clock) based on current design clock configuration. When the requested clock frequency with requested tolerance cannot be created, a warning about the clock accuracy range is generated while building the project. This warning contains the actual clock frequency value created by PSoC Creator. To remove this warning you must either change the system clock, Component settings or external clock to fit the clocking system requirements.

Median filter

This parameter applies 3 taps digital median filter on input path of RX line. This filter reduces the susceptibility to errors. The default value is a **Disabled**.

Retry on NACK

This option is applicable only for **SmartCard** mode. It enables retry on NACK feature. The Data frame is retransmitted when a negative acknowledgement is received.

Inverting RX

This option is applicable only for **IrDA** mode. It enables the inversion of the incoming RX line signal.

Enable wakeup from Deep Sleep Mode

Use this option to enable the Component to wake the system from Deep Sleep on the start bit. It is applicable for Standard mode when **RX Direction** is enabled.

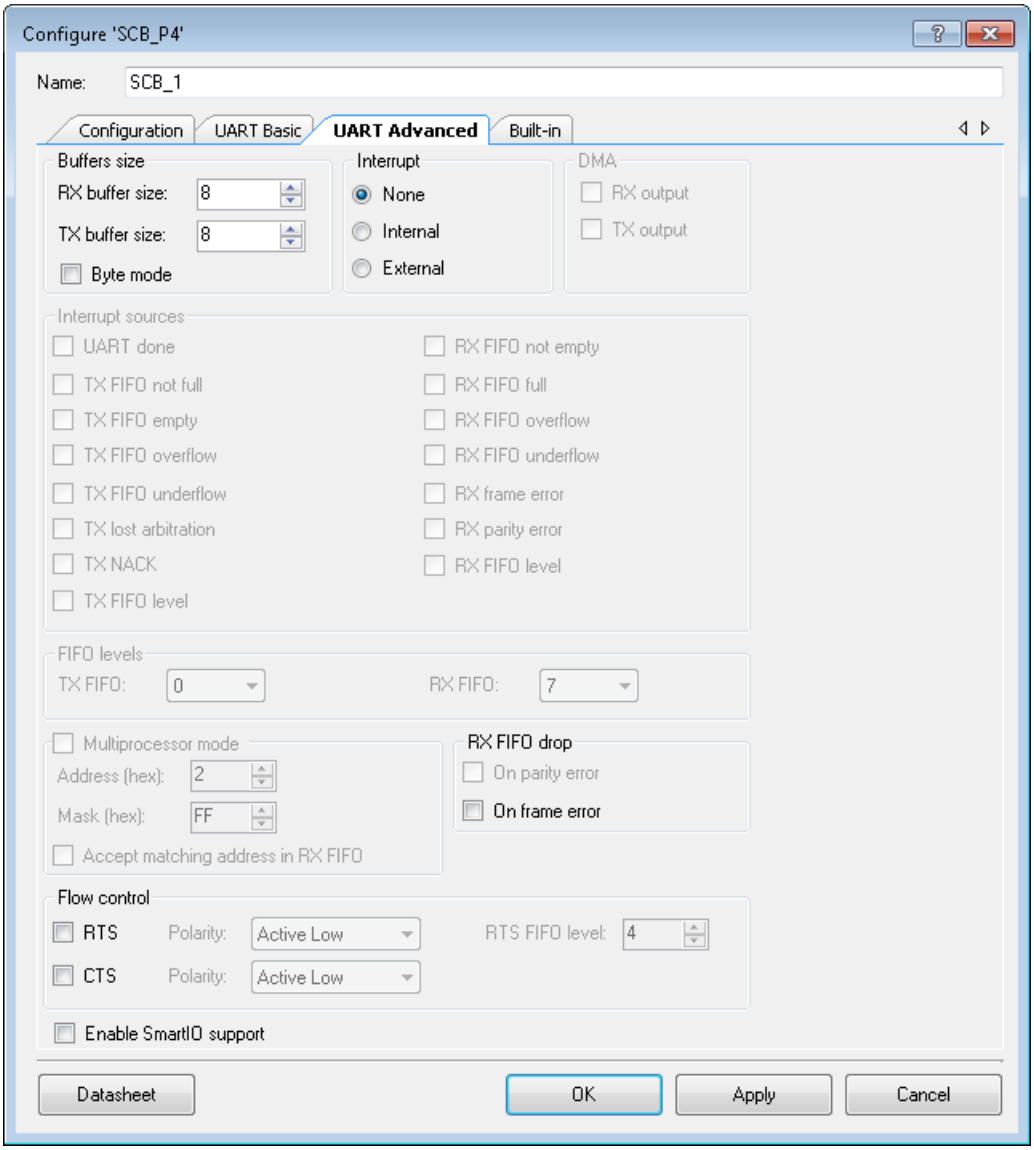
Refer to the Low power modes section under UART chapter in this document and *Power Management APIs* section of the *System Reference Guide* for more information.

Note The UART rx_wake pin must be placed on a port at which an interrupt is capable of waking the device from Deep Sleep. Refer to the selected device datasheet for more information about ports.

Low power receiving

This option is applicable only when **RX Direction** is enabled. It enables IrDA low power receiver mode.

Advanced UART Parameters



The **UART Advanced** tab contains the following parameters:

RX buffer size

The **RX buffer size** parameter defines the size (in bytes/words) of memory allocated for a receive data buffer. The RX buffer size minimum value is equal to the RX FIFO depth. The RX FIFO is implemented in hardware. Values greater than the RX FIFO depth up to (2^{32} – 2) imply usage of the RX FIFO, a circular software buffer controlled by the supplied APIs, and internal ISR. The software buffer size is limited only by the available memory. The interrupt mode is automatically set to internal and the RX FIFO not empty interrupt source is reserved to manage software buffer operation: move data from the RX FIFO into the circular software buffer.

- For PSoC 4100 / PSoC 4200 devices, the RX and TX FIFO depth is equal to 8 bytes/words.
- For PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor, the RX and TX FIFO depth is equal to 8 bytes/words or 16 bytes; refer to Byte mode for more information.

TX buffer size

The **TX buffer size** parameter defines the size (in bytes/words) of memory allocated for a transmit data buffer. The TX buffer size minimum value is equal to the RX FIFO depth. The TX FIFO is implemented in hardware. Values greater than the TX FIFO depth up to (2^{32} – 1) imply usage of the TX FIFO, a circular software buffer controlled by the supplied APIs, and internal ISR. The software buffer size is limited only by the available memory. The interrupt mode is automatically set to the internal and the TX FIFO not full interrupt source is reserved to manage software buffer operation: move data from the circular software buffer into the TX FIFO.

- For PSoC 4100 / PSoC 4200 devices, the RX and TX FIFO depth is equal to 8 bytes/words.
- For PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices, the RX and TX FIFO depth is equal to 8 bytes/words or 16 bytes; refer to Byte mode for more information.

Byte mode

This option is only applicable for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices. It allows doubling the TX and RX FIFO depth from 8 to 16 bytes. This implies that the number of data bits must be less than or equal to 8 bits. Increasing the FIFO depth improves performance of UART operation as more bytes can be transmitted or received without software interaction.

Interrupt

This option determines what interrupt modes are supported None, Internal or External.

- **None** – This option removes the internal interrupt Component.

- **Internal** – This option leaves the interrupt Component inside the SCB Component. The predefined internal interrupt handler is hooked up to the interrupt. The **Interrupt sources** option sets one or more interrupt sources, which trigger the interrupt. To add your own code to the interrupt service routine you need to register a function using the SCB_SetCustomInterruptHandler() function.
- **External** – This option removes the internal interrupt and provides an output terminal. Only an interrupt Component can be connected to the terminal if an interrupt handler is desired. The **Interrupt sources** option sets one or more interrupt sources, which trigger the interrupt output.

Note For buffer sizes greater than the hardware FIFO depth, the Component automatically enables the internal interrupt sources required for proper internal software buffer operations. In addition, the global interrupt enable must be explicitly enabled for proper buffer handling.

DMA

DMA is only available in PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC Analog Coprocessor devices. The provided options determine if DMA output trigger terminals are available on the Component symbol.

RX Output

This option determines if the rx_tr_out terminal is available on the Component symbol. This signal can only be connected to a DMA channel trigger input. The output of this terminal is controlled by the RX FIFO level. This option is active only when RX buffer size equal to FIFO depth.

TX Output

This option determines if the tx_tr_out terminal is available on the Component symbol. This signal can only be connected to a DMA channel trigger input. The output of this terminal is controlled by the TX FIFO level. This option is active only when TX buffer size equal to FIFO depth.

Interrupt sources

The interrupt sources are either level or pulse. Level-triggered interrupt sources in the following list are indicated with an asterisk (*). Refer to sections TX FIFO interrupt sources and RX FIFO interrupt sources for more information about level interrupt sources operation. The UART supports interrupts on the following events:

- **UART done –** UART transmitter done event: all data elements from the TX FIFO are sent. This interrupt source triggers later than TX FIFO empty by time it takes to transmit a single data element. The TX FIFO empty triggers when the last data element from the TX FIFO goes to the shifter register. However UART done triggers after this data element has been transmitted.

- **TX FIFO not full * –** TX FIFO is not full. At least one data element can be written into the TX FIFO.
- **TX FIFO empty * –** TX FIFO is empty.
- **TX FIFO overflow –** Firmware attempts to write to a full TX FIFO.
- **TX FIFO underflow * –** Hardware attempts to read from an empty TX FIFO.

  Note This interrupt source is level-triggered. It sets whenever there is no data to transmit (it can be used as an indication that the transfer is finished).
- **TX lost arbitration –** UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is useful when transmitter and receiver share a TX/RX line. This is the case in SmartCard mode.
- **TX NACK –** UART transmitter received a negative acknowledgement in SmartCard mode.
- **TX FIFO level * –** An interrupt request is generated whenever the number of data elements in the TX FIFO is less than the value of TX FIFO level.
- **RX FIFO not empty * –** RX FIFO is not empty. At least one data element is available in the RX FIFO to be read.
- **RX FIFO full * –** RX FIFO is full.
- **RX FIFO overflow** – Hardware attempts to write to a full RX FIFO.
- **RX FIFO underflow** – Firmware attempts to read from an empty RX FIFO.
- **RX frame error** – Frame error in received data frame. This can be either a start or stop bit(s) error:
  - Start bit error – after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1').

    Note A start bit error is detected BEFORE a data frame is received.
  - Stop bit error: the RX line is sampled as '0', but a '1' was expected.

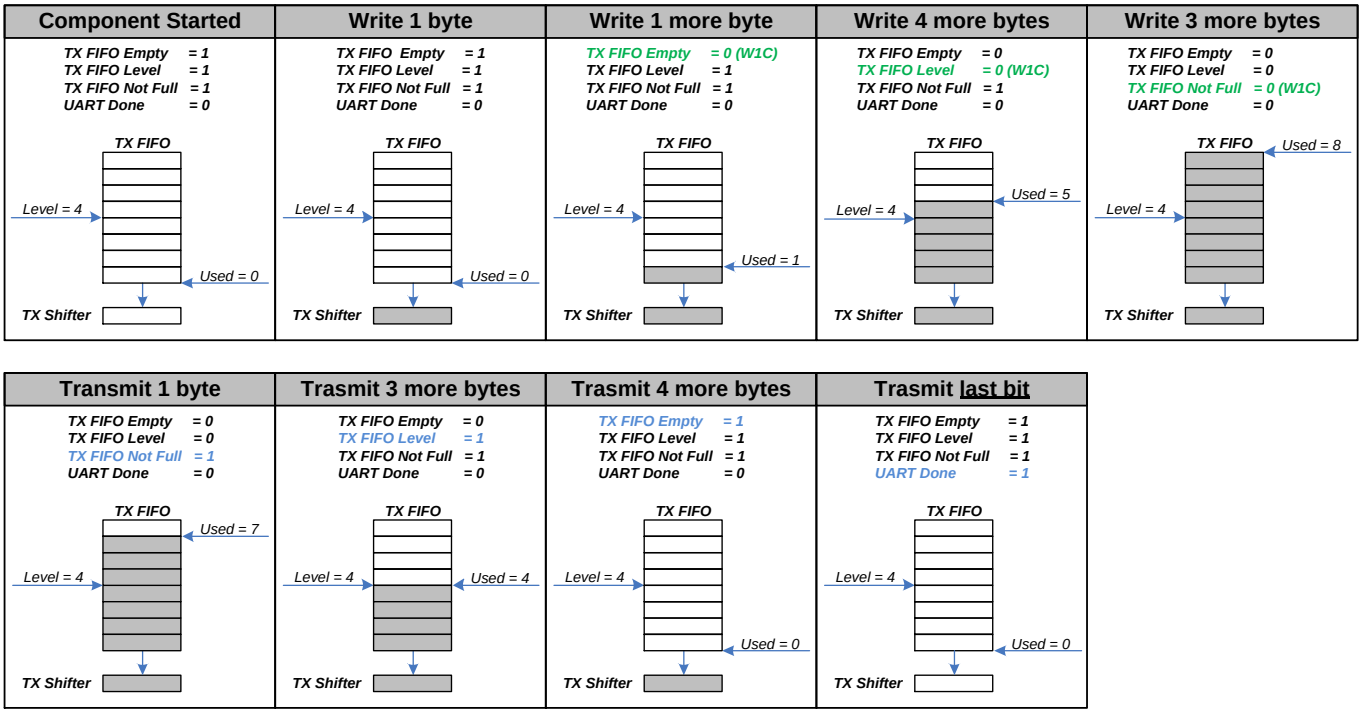
    Note A stop bit error may result in failure to receive successive data frame(s). A stop bit error is detected AFTER a data frame is received.
- **RX parity error –** Parity error in received data frame.
- **RX FIFO level * –** An interrupt request is generated whenever the number of data elements in the RX FIFO is greater than the value of RX FIFO level.

Notes

When **RX buffer size** is greater than the RX FIFO depth, the **RX FIFO not empty** interrupt source is reserved by the Component and used for the internal interrupt.

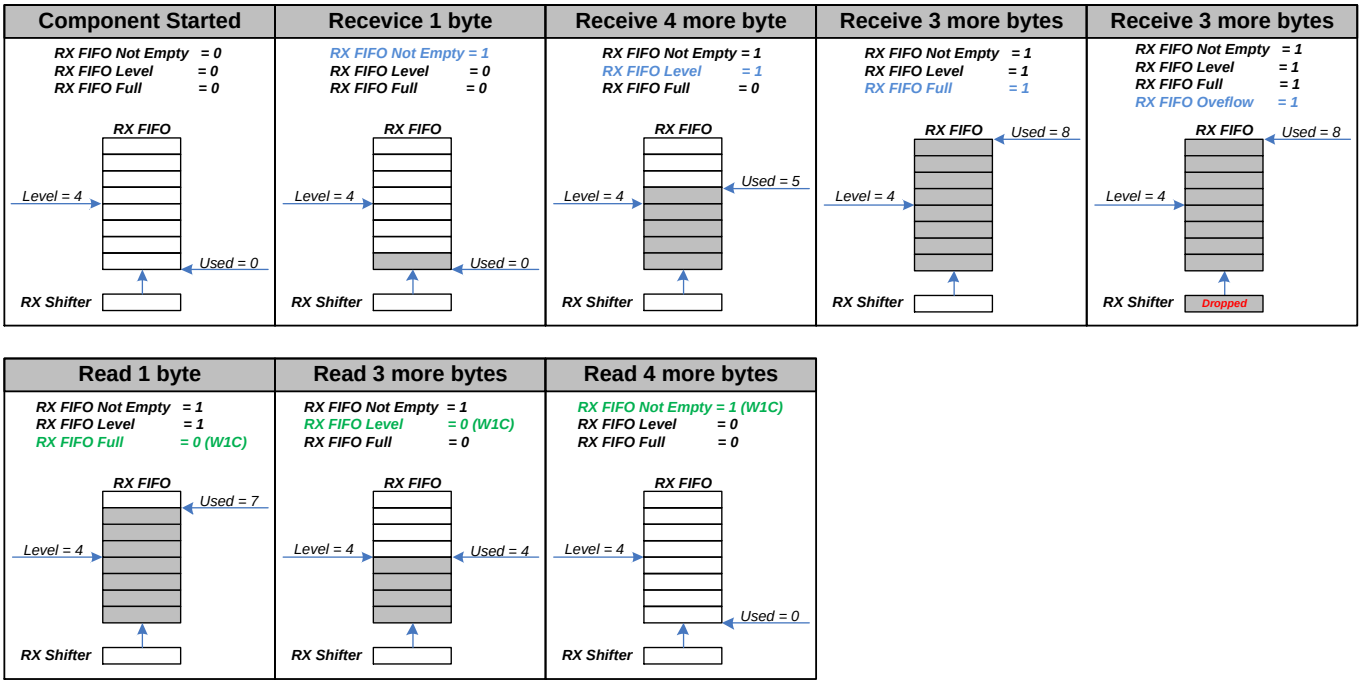
When **TX buffer size** is greater than the TX FIFO depth, the **TX FIFO not full** interrupt source is reserved by the Component and used for the internal interrupt.

Figure 30. TX interrupt sources operation



Note W1C – Write One to Clear interrupt source. The firmaware has to execute this action to clear interrupt source.
Note TX FIFO interrupt sources Empty, Level and Full are level triggered. It means that interrupt source active state is restored after clear operation if FIFO state is not changed.
For example: the TX FIFO Empty interrupt source cannot be cleared if hardware still have bytes to transmit from TX FIFO.

Figure 31. RX interrupt sources operation



Note W1C – Write One to Clear interrupt source. The firmaware has to execute this action to clear interrupt source.
Note RX FIFO interrupt sources Not Empty, Level and Full are level triggered. It means that interrupt source active state is restored after clear operation if FIFO state is not changed.
For example: the RX FIFO Full interrupt source cannot be cleared if firmware is not read at least single byte from full RX FIFO.

FIFO level

The RX and TX FIFO level settings control behavior of the appropriate level interrupt sources as well as RX and TX DMA triggers outputs.

RX FIFO

The interrupt or DMA trigger output signal remains active until the number of data elements in the RX FIFO is greater than the value of RX FIFO level.

For example, the RX FIFO has 8 data elements and the RX FIFO level is 0. The DMA trigger signal remains active until DMA does not read all data from the RX FIFO.

TX FIFO

The interrupt or DMA trigger output signal remains active until the number of data elements in the TX FIFO is less than the value of TX FIFO level.

For example, the TX FIFO has 0 data elements (empty) and the TX FIFO level is 7. The DMA trigger signal remains active until DMA does not load TX FIFO with 7 data elements.

Multiprocessor mode

This parameter enables the multiprocessor mode where the 9th bit (in the place of the parity bit) indicates an address. The default value is a **Disabled**. The number of Data bits must be set to 9 bits to get possibility to enable this option.

Address (hex)

Slave device address. Used to match when multiprocessor mode is enabled. The default value is 0x02.

Mask (hex)

Slave device address mask. These bits are used when matching to the slave address. The default value is **0xFF**.

- Bit value 0 – excludes bit from address comparison.
- Bit value 1 – the bit needs to match with the corresponding bit of the address.

Accept matching address in RX FIFO

This parameter determines whether to accept a matched address in the RX FIFO.

Note Non-matching addresses are never put in the RX FIFO.

RX FIFO drop

Provides hardware data drop options for RX FIFO.

- **On parity error** – Defines behavior when a parity check fails. When parity check is passed, received data is sent to the RX FIFO. Otherwise, received data is dropped and lost. Only applicable in **Standard** and **SmartCard** modes.
- **On frame error** – Defines behavior when a frame error is detected. When no frame error is captured, received data is sent to the RX FIFO. Otherwise, received data is dropped and lost.

RTS

This parameter is only applicable for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices. It enables the Ready to Send (RTS) output signal. The RTS signal is the part of flow control functionality used by the receiver. As long as the receiver is ready to accept more data it will keep the RTS signal active. The RTS FIFO level parameter determines if RTS remains active. The default value is a **Disabled**.

RTS Polarity

This parameter defines active polarity of the RTS output signal as Active Low (default) or Active High.

RTS FIFO level

This parameter is only available for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices. It determines whether the RTS signal remains active. While the RX FIFO has fewer entries than the RTS FIFO level, the RTS signal remains active; otherwise, the RTS signal becomes inactive. The RTS remains inactive unit data from RX FIFO will be read to match RTS FIFO level. The default value is 4.

CTS

This parameter is only applicable for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices. It enables the Clear to Send (CTS) input signal to be routed-out to the pin. The CTS signal is the part of flow control functionality utilized by the transmitter. The transmitter checks whether CTS signal is active before sending data from the TX FIFO. The transmission of data is suspended if CTS signal is inactive and will be resumed when CTS signal becomes active again. The default value is a **Disabled**.

CTS Polarity

This parameter defines active polarity of CTS input signal as Active Low (default) or Active High.

Enable SmartIO support

This option removes the buried UART pins inside the Component and exposes appropriate input and output terminals. Only the Pin or SmartIO Component is allowed to be connected to these terminals. See Input/Output Connections section for descriptions of these terminals. This option is disabled by default and supported only in Standard or IrDA UART modes. Also the Enable wakeup from Deep Sleep Mode is not supported when this option is enabled because wakeup requires interrupt from the internal rx pin which is removed. The supported devices are PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor.

Note that SCB Component stops managing pins state when Component is disabled or device is in low power when Enable SmartIO support option is enabled. It becomes user responsibility to take care about the pins.

UART APIs

APIs allow you to configure the Component using software. The following table lists and describes the interface to each function. The subsequent sections discusses each function in more detail.

By default, PSoC Creator assigns the instance name “SCB_1” to the first instance of a Component in a given design. You can rename the instance to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is “SCB”.

Function	Description
SCB_Start()	Starts the SCB.
SCB_Init()	Initialize the SCB Component according to defined parameters in the customizer.
SCB_Enable()	Enables SCB Component operation.
SCB_Stop()	Disable the SCB Component.
SCB_Sleep()	Prepares Component to enter Deep Sleep.
SCB_Wakeup()	Prepares Component for Active mode operation after Deep Sleep.
SCB_UartInit()	Configures the SCB for UART operation. Only used when using the SCB in unconfigured mode.
SCB_UartPutChar()	Places a byte of data in the transmit buffer to be sent at the next available bus time.
SCB_UartPutString()	Places a NULL terminated string in the transmit buffer to be sent at the next available bus time.
SCB_UartPutCRLF()	Places byte of data followed by a carriage return (0x0D) and line feed (0x0A) to the transmit buffer
SCB_UartGetChar()	Retrieves next data element from receive buffer.
SCB_UartGetByte()	Retrieves next data element from the receive buffer.
SCB_UartSetRxAddress()	Sets the hardware detectable receiver address for the UART in Multiprocessor mode.
SCB_UartSetRxAddressMask()	Sets the hardware address mask for the UART in Multiprocessor mode.
SCB_UartSetRtsPolarity()	Sets active polarity of RTS input signal.
SCB_UartSetRtsFifoLevel()	Sets level in the RX FIFO to activate RTS signal.
SCB_UartEnableCts()	Enables usage of CTS input signal by the UART transmitter.
SCB_UartDisableCts()	Disables usage of CTS input signal by the UART transmitter
SCB_UartSetCtsPolarity()	Sets active polarity of CTS input signal.

Function	Description
SCB_SpiUartWriteTxData()	Places a data entry into the transmit buffer to be sent at the next available bus time.
SCB_SpiUartPutArray()	Places an array of data into the transmit buffer to be sent.
SCB_SpiUartGetTxBufferSize()	Returns the number of elements currently in the transmit buffer.
SCB_SpiUartClearTxBuffer()	Clears the transmit buffer and TX FIFO.
SCB_SpiUartReadRxData()	Retrieves the next data element from the receive buffer.
SCB_SpiUartGetRxBufferSize()	Returns the number of received data elements in the receive buffer.
SCB_SpiUartClearRxBuffer()	Clears the receive buffer and RX FIFO.

void SCB_Start(void)

Description: Invokes SCB_Init() and SCB_Enable(). After this function call the Component is enabled and ready for operation. This is the preferred method to begin Component operation.

When configuration is set to “Unconfigured SCB”, the Component must first be initialized to operate in one of the following configurations: I²C, SPI, UART or EZ I²C. Otherwise this function does not enable Component.

void SCB_Init(void)

Description: Initializes the SCB Component to operate in one of the selected configurations: I²C, SPI, UART or EZ I²C.

When configuration is set to “Unconfigured SCB”, this function does not do any initialization. Use mode-specific initialization functions instead: SCB_I2CInit, SCB_SpiInit, SCB_UartInit or SCB_EzI2CInit.

void SCB_Enable(void)

Description: Enables SCB Component operation; activates the hardware and internal interrupt. It also restores TX interrupt sources disabled after the SCB_Stop() function was called (note that level-triggered TX interrupt sources remain disabled to not cause code lock-up).

For I²C and EZ I²C modes the interrupt is internal and mandatory for operation. For SPI and UART modes the interrupt can be configured as none, internal or external. The SCB configuration should be not changed when the Component is enabled. Any configuration changes should be made after disabling the Component.

When configuration is set to “Unconfigured SCB”, the Component must first be initialized to operate in one of the following configurations: I²C, SPI, UART or EZ I²C using the mode-specific functions: SCB_I2CInit, SCB_SpiInit, SCB_UartInit or SCB_EzI2Cinit. Otherwise this function does not enable Component.

void SCB_Stop(void)

Description: Disables the SCB Component: disable the hardware and internal interrupt. It also disables all TX interrupt sources so as not to cause an unexpected interrupt trigger because after the Component is enabled, the TX FIFO is empty.

Refer to the function SCB_Enable() for the interrupt configuration details.

This function disables the SCB Component without checking to see if communication is in progress. Before calling this function it may be necessary to check the status of communication to make sure communication is complete. If this is not done then communication could be stopped mid byte and corrupted data could result.

void SCB_Sleep(void)

Description: Prepares Component to enter Deep Sleep.

The “Enable wakeup from Deep Sleep Mode” selection has an influence on this function implementation:

- Checked: configures the Component to be wakeup source from Deep Sleep.
- Unchecked: stores the current Component state (enabled or disabled) and disables the Component. See SCB_Stop() function for details about Component disabling.

Call the SCB_Sleep() function before calling the CyPmSysDeepSleep() function.

Refer to the PSoC Creator *System Reference Guide* for more information about power-management functions.

This function should not be called before entering Sleep.

void SCB_Wakeup(void)

Description: Prepares Component for Active mode operation after Deep Sleep.

The “Enable wakeup from Deep Sleep Mode” selection has influence to on this function implementation:

- Checked: restores the Component Active mode configuration.
- Unchecked: enables the Component if it was enabled before enter Deep Sleep.

This function should not be called after exiting Sleep.

Side Effects: Calling the SCB_Wakeup() function without first calling the SCB_Sleep() function may produce unexpected behavior.

Void SCB_UartInit(SCB_UART_INIT_STRUCT *config)

Description: Configures the SCB for UART operation.

This function is **intended specifically** to be used when the SCB configuration is set to "Unconfigured SCB" in the customizer. After initializing the SCB in UART mode, the Component can be enabled using the SCB_Start() or SCB_Enable() function.

This function uses a pointer to a structure that provides the configuration settings. This structure contains the same information that would otherwise be provided by the customizer settings.

Parameters config: pointer to a structure that contains the following ordered list of fields. These fields match the selections available in the customizer. Refer to the customizer for further description of the settings.

Field	Description
uint32 mode	Mode of operation for the UART. The following defines are available choices: SCB_UART_MODE_STD SCB_UART_MODE_SMARTCARD SCB_UART_MODE_IRDA
uint32 direction	Direction of operation for the UART. The following defines are available choices: SCB_UART_TX_RX SCB_UART_RX SCB_UART_TX
uint32 dataBits	Number of data bits
uint32 parity	Determines the parity. The following defines are available choices: SCB_UART_PARITY_EVEN SCB_UART_PARITY_ODD SCB_UART_PARITY_NONE
uint32 stopBits	Determines the number of stop bits. The following defines are available choices: SCB_UART_STOP_BITS_1 SCB_UART_STOP_BITS_1_5 SCB_UART_STOP_BITS_2
uint32 oversample	Oversampling factor for the UART. **Note** The oversampling factor values are changed when enableIrdaLowPower is enabled: SCB_UART_IRDA_LP_OVS16 SCB_UART_IRDA_LP_OVS32 SCB_UART_IRDA_LP_OVS48 SCB_UART_IRDA_LP_OVS96 SCB_UART_IRDA_LP_OVS192 SCB_UART_IRDA_LP_OVS768 SCB_UART_IRDA_LP_OVS1536
uint32 enableIrdaLowPower	IrDA low power RX mode is enabled. 0 – disable 1 – enable The TX functionality does not work when enabled.

Parameters (cont):

Uint32 enableMedianFilter	0 – disable 1 – enable
uint32 enableRetryNack	0 – disable 1 – enable Ignored for modes other than SmartCard.
Uint32 enableInvertedRx	0 – disable 1 – enable Ignored for modes other than IrDA.
Uint32 dropOnParityErr	Drop data from RX FIFO if parity error is detected. 0 – disable 1 – enable
uint32 dropOnFrameErr	Drop data from RX FIFO if a frame error is detected. 0 – disable 1 – enable
uint32 enableWake	0 – disable 1 – enable Ignored for modes other than standard UART. The RX functionality has to be enabled.
uint32 rxBufferSize	Size of the RX buffer in words: • The value equal to the RX FIFO depth implies the usage of buffering in hardware. • A value greater than the RX FIFO depth results in a software buffer. The SCB_INTR _RX_NOT_EMPTY interrupt has to be enabled to transfer data into the software buffer. For PSoC 4100 / PSoC 4200 devices, the RX FIFO and TX FIFO depth is equal to 8 bytes/words. For PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices, the RX FIFO and TX FIFO depth is equal to 8 bytes/words or 16 bytes (Byte mode is enabled).
uint8* rxBuffer	Buffer space provided for a RX software buffer: • A NULL pointer must be provided to use hardware buffering. • A pointer to an allocated buffer must be provided to use software buffering. The buffer size must equal (rxBufferSize + 1) in bytes if dataBits is less or equal to 8, otherwise (2 * (rxBufferSize + 1)) in bytes. The software RX buffer always keeps one element empty. For correct operation allocated RX buffer has to be one element greater than maximum packet size expected to be received.
uint32 txBufferSize	Size of the TX buffer in words: • The value equal to the RX FIFO depth implies the usage of buffering in hardware. • A value greater than the RX FIFO depth results in a software buffer. For PSoC 4100 / PSoC 4200 devices, the RX and TX FIFO depth is equal to 8 bytes/words. For PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices, the RX and TX FIFO depth is equal to 8 bytes/words or 16 bytes (Byte mode is enabled).

uint8* txBuffer	Buffer space provided for a TX software buffer: • A NULL pointer must be provided to use hardware buffering. • A pointer to an allocated buffer must be provided to use software buffering. The buffer size must equal txBufferSize if dataBits is less or equal to 8, otherwise (2* txBufferSize).
uint32 enableMultiproc	Enables multiprocessor mode. 0 – disable 1 – enable
uint32 multiprocAcceptAddr	Enables matched address to be accepted. 0 – disable 1 – enable
uint32 multiprocAddr	8 bit address to match in Multiprocessor mode. Ignored for other modes.
Uint32 multiprocAddrMask	8 bit mask of address bits that are compared for a Multiprocessor address match. Ignored for other modes.
Uint32 enableInterrupt	0 – disable 1 – enable The interrupt has to be enabled if software buffer is used.
Uint32 rxInterruptMask	Mask of interrupt sources to enable in the RX direction. This mask is written regardless of the setting of the enableInterrupt field. Multiple sources are enabled by providing a value that is the OR of all of the following sources to enable: SCB_INTR_RX_FIFO_LEVEL SCB_INTR_RX_NOT_EMPTY SCB_INTR_RX_FULL SCB_INTR_RX_OVERFLOW SCB_INTR_RX_UNDERFLOW SCB_INTR_RX_FRAME_ERROR SCB_INTR_RX_PARITY_ERROR
uint32 rxTriggerLevel	FIFO level for an RX FIFO level interrupt. This value is written regardless of whether the RX FIFO level interrupt source is enabled.
Uint32 txInterruptMask	Mask of interrupt sources to enable in the TX direction. This mask is written regardless of the setting of the enableInterrupt field. Multiple sources are enabled by providing a value that is the OR of all of the following sources to enable: SCB_INTR_TX_FIFO_LEVEL SCB_INTR_TX_NOT_FULL SCB_INTR_TX_EMPTY SCB_INTR_TX_OVERFLOW SCB_INTR_TX_UNDERFLOW SCB_INTR_TX_UART_DONE SCB_INTR_TX_UART_NACK SCB_INTR_TX_UART_ARB_LOST
uint32 txTriggerLevel	FIFO level for a TX FIFO level interrupt. This value is written regardless of whether the TX FIFO level interrupt source is enabled.

Uint8 enableByteMode	Ignored for devices other than PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor. 0 – disable 1 – enable When enabled the TX and RX FIFO depth is 16 bytes. This implies that number of Data bits must be less than or equal to 8.
Uint8 enableCts	Ignored for all devices other than PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor. Enables usage of CTS input signal by the UART transmitter. 0 – disable 1 – enable
uint8 ctsPolarity	Ignored for all devices other than PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor. Sets active polarity of CTS input signal. SCB_UART_CTS_ACTIVE_LOW SCB_UART_CTS_ACTIVE_HIGH
uint8 rtsRxFifoLevel	Ignored for all devices other than PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor. RX FIFO level for RTS signal activation. While the RX FIFO has fewer entries than the RTS FIFO level value the RTS signal remains active, otherwise the RTS signal becomes inactive. By setting this field to 0, RTS signal activation is disabled.
uint8 rtsPolarity	Ignored for all devices other than PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor. Sets active polarity of RTS output signal. SCB_UART_RTS_ ACTIVE_LOW SCB_UART_RTS_ACTIVE_HIGH

void SCB_UartPutChar(uint32 txDataByte)

Description: Places a byte of data in the transmit buffer to be sent at the next available bus time. This function is blocking and waits until there is a space available to put requested data in the transmit buffer.

For UART Multi Processor mode this function can send 9-bits data as well. Use SCB_UART_MP_MARK to add a mark to create an address byte.

Note This function is implemented as macro which calls SCB_SpiUartWriteTxData().

Parameters: uint32 txDataByte: the data to be transmitted.

void SCB_UartPutString(const char8 string[])

Description: Places a NULL terminated string in the transmit buffer to be sent at the next available bus time.

This function is blocking and waits until there is a space available to put requested data in transmit buffer.

Parameters: const char8 string[]: pointer to the null terminated string array to be placed in the transmit buffer.

void SCB_UartPutCRLF(uint32 txDataByte)

Description: Places byte of data followed by a carriage return (0x0D) and line feed (0x0A) in the transmit buffer

This function is blocking and waits until there is a space available to put all requested data in transmit buffer.

Parameters: uint32 txDataByte : the data to be transmitted

uint32 SCB_UartGetChar(void)

Description: Retrieves next data element from receive buffer. This function is designed for ASCII characters and returns a char where 1 to 255 are valid characters and 0 indicates an error occurred or no data is present.

RX software buffer is disabled: Returns data element retrieved from RX FIFO.

RX software buffer is enabled: Returns data element from the software receive buffer.

Return Value: uint32: Next data element from the receive buffer. ASCII character values from 1 to 255 are valid. A returned zero signifies an error condition or no data available.

Side Effects: The errors bits may not correspond with reading characters due to RX FIFO and software buffer usage.

RX software buffer is enabled: The internal software buffer overflow is not treated as an error condition. Check SCB_rxBufferOverflow to capture that error condition.

Uint32 SCB_UartGetByte(void)

Description: Retrieves next data element from the receive buffer, returns received byte and error condition.

RX software buffer disabled: Returns data element retrieved from RX FIFO. Undefined data will be returned if the RX FIFO is empty

RX software buffer enabled: Returns data element from the software receive buffer

Return Value: uint32: Bits 7-0 contain the next data element from the receive buffer and other bits contain the error condition. The error condition constants are provided below:

RX error conditions	Description
SCB_UART_RX_OVERFLOW	Attempt to write to a full receiver FIFO.
SCB_UART_RX_UNDERFLOW	Attempt to read from an empty receiver FIFO.
SCB_UART_RX_FRAME_ERROR	UART framing error detected.
SCB_UART_RX_PARITY_ERROR	UART parity error detected.

Side Effects: The errors bits may not correspond with reading characters due to RX FIFO and software buffer usage.

RX software buffer is disabled: Internal software buffer overflow is not returned as status by this function. Check SCB_rxBufferOverflow to capture that error condition.

Void SCB_UartSetRxAddress(uint32 address)

Description: Sets the hardware detectable receiver address for the UART in Multiprocessor mode.

Parameters: uint32 address: Address for hardware address detection.

void SCB_UartSetRxAddressMask(uint32 addressMask)

Description: Sets the hardware address mask for the UART in Multiprocessor mode.

Parameters: uint32 addressMask: Address mask.

Bit value 0 – excludes bit from address comparison.

Bit value 1 – the bit needs to match with the corresponding bit of the address.

void SCB_UartSetRtsPolarity(uint32 polarity)

Description: Sets active polarity of RTS input signal.

Only available for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices.

Parameters: uint32 polarity: Active polarity of RTS input signal.

Active RTS polarity constants	Description
SCB_UART_RTS_ACTIVE_LOW	RTS signal is active low
SCB_UART_RTS_ACTIVE_HIGH	RTS signal is active high

void SCB_UartSetRtsFifoLevel (uint32 level)

Description: Sets level in the RX FIFO for RTS signal activation. While the RX FIFO has fewer entries than the RTS FIFO level the RTS signal remains active, otherwise the RTS signal becomes inactive.

Only available for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices.

Parameters: uint32 level: Level in the RX FIFO for RTS signal activation.

The range of valid level values is between 0 and RX FIFO depth – 1. Setting level value to 0 disables RTS signal activation.

void SCB_UartEnableCts(void)

Description: Enables usage of CTS input signal by the UART transmitter.

Only available for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices.

void SCB_UartDisableCts(void)

Description: Disables usage of CTS input signal by the UART transmitter.

Only available for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices.

void SCB_UartSetCtsPolarity(uint32 polarity)

Description: Sets active polarity of CTS input signal.

Only available for PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices.

Parameters: uint32 polarity: Active polarity of CTS input signal.

Active CTS polarity constants	Description
SCB_UART_CTS_ACTIVE_LOW	CTS signal is active low
SCB_UART_CTS_ACTIVE_HIGH	CTS signal is active high.

void SCB_SpiUartWriteTxData(uint32 txData)

Description: Places a data entry into the transmit buffer to be sent at the next available bus time. The data transmit direction is LSB.

This function is blocking and waits until there is space available to put the requested data in the transmit buffer.

For UART Multi Processor mode this function can send 9-bits data. Use SCB_UART_MP_MARK to add a mark to create an address byte.

Parameters: uint32 txData: the data to be transmitted.

The amount of data bits to be transmitted depends on Data bits selection (the data bit counting starts from LSB of txDataByte).

void SCB_SpiUartPutArray(const uint16/uint8 wrBuf[], uint32 count)

Description: Places an array of data into the transmit buffer to be sent.

This function is blocking and waits until there is a space available to put all the requested data in the transmit buffer.

The array size can be greater than transmit buffer size.

Parameters: const uint16/uint8 wrBuf[]: pointer to an array with data to be placed in transmit buffer. The amount of data bits to be transmitted as one array entry depends on Data bits selection (the data bit counting starts from LSB for each array entry).

Uint32 count: number of data elements to be placed in the transmit buffer.

uint32 SCB_SpiUartGetTxBufferSize(void)

Description: Returns the number of elements currently in the transmit buffer.

TX software buffer is disabled: Returns the number of used entries in TX FIFO.

TX software buffer is enabled: Returns the number of elements currently used in the transmit buffer. This number does not include used entries in the TX FIFO; therefore, the transmit buffer size is zero until the TX FIFO is not full.

Return Value: uint32: Number of data elements ready to transmit.

void SCB_SpiUartClearTxBuffer(void)

Description: Clears the transmit buffer and TX FIFO.

uint32 SCB_SpiUartReadRxData(void)

Description: Retrieves the next data element from the receive buffer.

RX software buffer is disabled: Returns data element retrieved from RX FIFO. Undefined data will be returned if the RX FIFO is empty.

RX software buffer is enabled: Returns data element from the software receive buffer. Zero value will be returned if receive software buffer is empty.

Return Value: uint32: Next data element from the receive buffer.

The amount of data bits to be received depends on Data bits selection (the data bit counting starts from LSB of return value).

uint32 SCB_SpiUartGetRxBufferSize(void)

Description: Returns the number of received data elements in the receive buffer.

RX software buffer is disabled: Returns the number of used entries in RX FIFO.

RX software buffer is enabled: Returns the number of elements that were placed in the receive buffer. This does not include the hardware RX FIFO.

Return Value: uint32: Number of received data elements

void SCB_SpiUartClearRxBuffer(void)

Description: Clears the receive buffer and RX FIFO.

Global Variables

Knowledge of these variables is not required for normal operations.

Variable	Description
SCB_initVar	SCB_initVar indicates whether the SCB Component has been initialized. The variable is initialized to 0 and set to 1 the first time SCB_Start() is called. This allows the Component to restart without reinitialization after the first call to the SCB_Start() routine. If re-initialization of the Component is required, then the SCB_Init() function can be called before the SCB_Start() or SCB_Enable() function.
SCB_rxBufferOverflow	SCB_rxBufferOverflow sets when internal software receive buffer overflow was occurred.

Variable	Description
SCB_skipStart	This global variable determines whether to enable Skip Start functionality when SCB_Sleep() is called: 0 – disable, other values – enable. Default value is 1. It is only available when Enable wakeup from Deep Sleep Mode option is enabled.
SCB_IntrTxMask	This global variable stores TX interrupt sources after SCB_Stop() is called. Only these TX interrupt sources will be restored on a subsequent SCB_Enable() call.

Bootloader Support

The SCB Component in UART mode can be used as a communication Component for the Bootloader. The following configuration should be used to support UART communication protocol from an external system to the Bootloader:

- Mode: Standard
- Direction: TX+RX
- Data bits: 8 bits
- Baud rate: Must match Host (boot device)
- Parity: Must match Host (boot device).
- Stop Bits: Must match Host (boot device).
- RX buffer size: Must match or be greater than the maximum size of the packet received from Host. The recommended RX buffer size value to select for bootloading when using the Bootloader Host Tool (shipped with PSoC Creator) is **64**.
- TX buffer size: Must match or be greater than the maximum size of the packet transmitted to Host. The recommended TX buffer size to select for bootloading when using the Bootloader Host Tool (shipped with PSoC Creator) is **64**.

For more information about the Bootloader, refer to the Bootloader Component datasheet.

The following API functions are provided for Bootloader use.

Function	Description
SCB_CyBtldrCommStart()	Starts the UART Component and enables its interrupt.
SCB_CyBtldrCommStop()	Disables the UART Component and its interrupt.
SCB_CyBtldrCommReset()	Resets UART receive and transmit buffers.
SCB_CyBtldrCommRead()	Allows the caller to read data from the bootloader host (the host writes the data).
SCB_CyBtldrCommWrite()	Allows the caller to write data to the bootloader host (the host reads the data).

void SCB_CyBtldrCommStart(void)

Description: Starts the UART Component and enables its interrupt (if TX or RX buffer size is greater than FIFO depth).

Every incoming UART transfer is treated as a command for the bootloader.

void SCB_CyBtldrCommStop(void)

Description: Disables the UART Component and its interrupt.

void SCB_CyBtldrCommReset(void)

Description: Resets UART receive and transmit buffers.

cystatus SCB_CyBtldrCommRead(uint8 pData[], uint16 size, uint16 * count, uint8 timeOut)

Description: Allows the caller to read data from the bootloader host (the host writes the data). The function handles polling to allow a block of data to be completely received from the host device.

Parameters: uint8 pData[]: Pointer to the block of data to be read from bootloader host.

uint16 size: Number of bytes to be read from bootloader host.

uint16 *count: Pointer to variable to write the number of bytes actually read by bootloader host.

uint8 timeOut: Number of units in 10 ms to wait before returning because of a timeout.

Return Value: cystatus: Returns CYRET_SUCCESS if no problem was encountered or returns the value that best describes the problem. For more information, refer to the “Return Codes” section of the *System Reference Guide*.

cystatus SCB_CyBtldrCommWrite(const uint8 pData[], uint16 size, uint16 * count, uint8 timeOut)

Description: Allows the caller to write data to the bootloader host (the host reads the data). The function does not use timeout and returns after data has been copied into the transmit buffer. The data transmission starts immediately after the first data element is written into the buffer and lasts until all data elements from the buffer are sent.

Parameters: const uint8 pData[]: Pointer to the block of data to send to the bootloader host.

uint16 size: Number of bytes to send to bootloader host.

uint16 *count: Pointer to variable to write the number of bytes actually written to bootloader host.

uint8 timeOut: The timeout is not used by this function. The function returns as soon as data is copied into the transmit buffer.

Return Value: cystatus: Returns CYRET_SUCCESS if no problem was encountered or returns the value that best describes the problem. For more information refer to the “Return Codes” section of the *System Reference Guide*.

SCB_CyBtldrCommRead details

The UART interface does not provide start and stop conditions to define the start and end of a transfer like I^{2}C. Therefore, the following approach is used to define when a command packet from the host is received:

1) To determine when the start of a packet has occurred, the RX buffer is checked at a one millisecond interval until the buffer size is non-zero or timeout is expired. As soon as at least one data element has been received the communication Component knows a packet transfer has started and immediately begins looking for the end of the packet.
2) The transfer is completed if no new data elements are received within byte-to-byte interval. This time interval is defined as the time consumed to transfer two data elements with selected data rate. It is calculated by the Component based on current data rate selection. If needed, the byte-to-byte interval can be changed using global defines. Open project Build Settings -> Compiler -> Command line and provide the global define of the interval in microseconds. For example, to change interval to 40 microseconds:

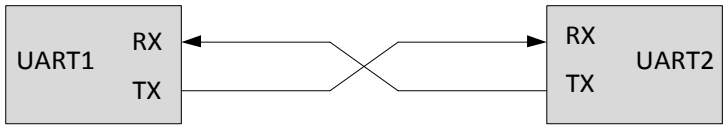
```
-D SCB_UART_BYTE_TO_BYTE=40
```

UART Functional Description

The Universal Asynchronous Receiver/Transmitter (UART) protocol is an asynchronous serial interface. The UART transmit and receive interfaces consists of 2 signals:

- **TX** – Transmitter
- **RX** – Receiver

Figure 32. UART typical connection



Standard mode operation

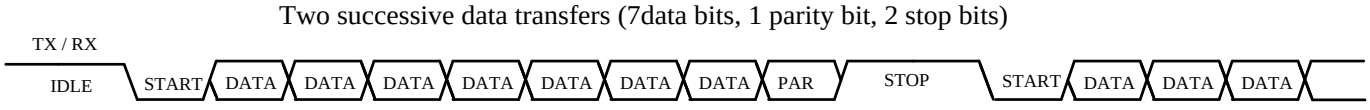
Standard UART is defined with “peer to peer” topology.

A typical UART transfer consists of a “Start Bit” followed by multiple “Data Bits”, optionally followed by a “Parity Bit” and finally completed by one or more “Stop Bits”. The “Start Bit” value is always ‘0’, the “Data Bits” values are dependent on the data transferred, the “Parity Bit” value is set to a value guaranteeing an even or odd parity over the “Data Bits” and the “Stop Bits” value is ‘1’. The “Parity Bit” is generated by the transmitter and can be used by the receiver to detect single bit transmission errors. When not transmitting data, the TX line is ‘1’; i.e. the same value as the “Stop Bits”.

The transition of a “Stop Bit” to a “Start Bit” is represented by a change from ‘1’ to ‘0’ on the TX line. This transition can be used by the receiver to synchronize with the transmitter clock. Synchronization at the start of each data transfer allows error-free transmission even in the presence of frequency drift between transmitter and receiver clocks. The required clock accuracy is dependent on the data transfer size.

The stop period or the amount of “Stop Bits” between successive data transfers is typically agreed upon between transmitter and receiver, and is typically in the range of 1 to 3 bit transfer periods.

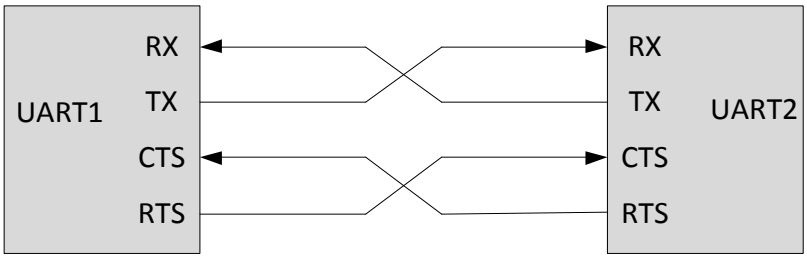
Figure 33. UART Protocol



Flow control

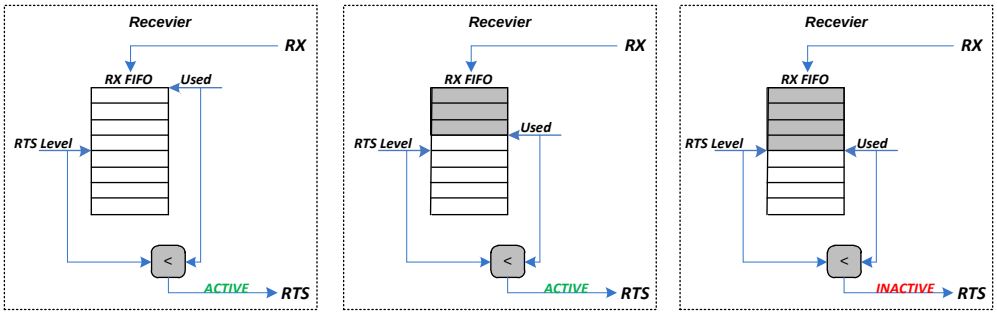
Flow control is a method used to provide reliable communication between the receiver and transmitter without data loss. This method implies that a receiver tells a transmitter to stop (suspend) or start (resume) transmitting. Hardware flow control is supported by the UART in Standard mode by PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices. The two extra lines for hardware flow control are needed in addition to data lines. They are called RTS and CTS. These lines are cross-coupled between the two devices, so the RTS line on one device is connected to the CTS line on the other device and vice versa. The Configure dialog provides independent control of RTS and CTS signals.

Figure 34. UART hardware flow control typical connection



As long as the receiver is ready to accept more data it will keep the RTS signal active. The RTS FIFO level parameter determines how the RTS remains active as follows: while the RX FIFO has fewer entries than the RX FIFO level the RTS signal remains active, otherwise the RTS signal becomes inactive. The RTS remains inactive unit data from RX FIFO is read to match RTS activation condition.

Figure 35. UART RTS signal activation



Initial state: RTS is active | Data reception: RTS is active | Data reception: RTS is inactive

The transmitter checks whether the CTS signal is active before sending data from the TX FIFO on the bus. The transmission of data is suspended if the CTS signal is inactive and will be resumed when CTS signal becomes active again.

Typically, the RTS and CTS signals are active low. However, there is a possibility to change the active polarity of these signals.

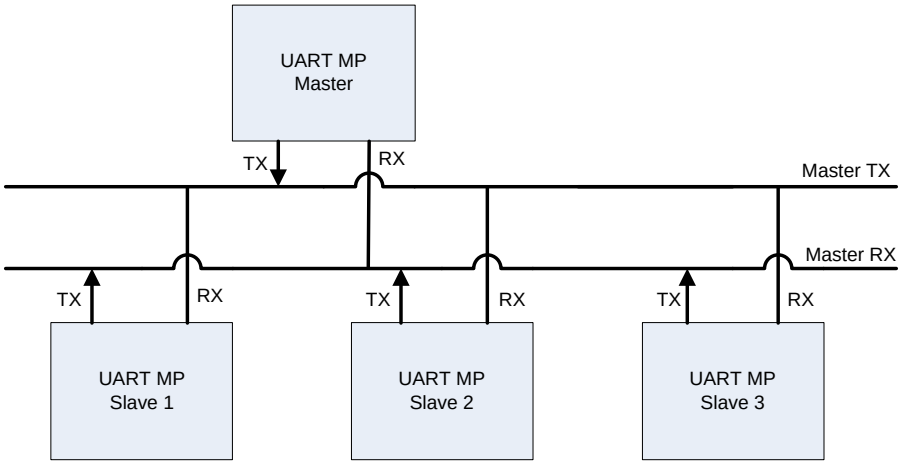
Multiprocessor mode operation

This mode is defined with “single-master-multi-slave” topology. The multiprocessor mode is also known as UART 9-bits protocol, while standard UART protocol uses a 5-bit to 8-bit data field.

The main properties of multiprocessor mode are:

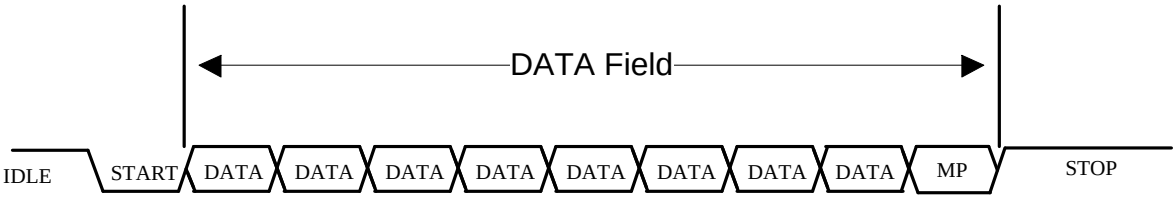
- Single master with multiple slave concept (multi-drop network)
- Each slave is identified by a unique address
- Using 9 bits data field, with the 9th bit (MSB) as address/data flag. When set ‘1’, it indicates an address byte; when set ‘0’ it indicates a data byte.
- Parity bit is disabled

Figure 36. Multiprocessor Bus Connections



To enable Multiprocessor mode, configure the UART with the following options: **Mode**: Standard, **Data bits**: 9 bits, **Parity**: None.

Figure 37. UART data frame in Multiprocessor mode



Because the data link layer of a multi-drop network is a user-defined protocol, it offers a flexible way of composing the data field.

All the bits in an address frame can be used to represent a device address. Alternatively, some bit can be used to represent the address, while the remaining bits can represent a command to the slave device, and some bits can represent the length of data in following data frames.

The SCB can be used as a master or slave device in multiprocessor mode.

When UART works as slave device, the received address is matched with Address and Mask. The matched address is written in the RX FIFO when Accept matching address in RX FIFO is checked. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of no match, subsequent received data is dropped, until next address received for compare.

UART 9th data bit usage

The 9th bit is sent in the parity bit position and most typically used to define whether the data sent was an address or standard data. A mark (1) in the parity bit indicates an address was sent and a space (0) in the parity bit indicates data was sent. The data flow is "Start Bit, Data Bits, Parity, Stop Bits," similar to the other parity modes but this bit has to be controlled by user firmware before the transfer rather than being calculated based on the data bit values.

```
tx_data = 0x31;
tx_data |= UART_UART_MP_MARK; /* Set 9th bit to indicate address */
UART_SpiUartWriteTxData(tx_data);
```

SmartCard (ISO7816) mode operation

ISO7816 is an asynchronous serial interface, defined with “single-master-single-slave” topology. Only the master (reader) function is supported in the Component.

SCB provides the basic physical layer support with asynchronous character transmission, and only “I/O” pin interface of standard ISO7816 [8] pin list is provided. SCB UART TX line will be connected to SmartCard I/O line, by internally multiplexing between TX and RX control modules.

The higher level protocol implementation is left for firmware to handle from the user level.

SmartCard data transfer

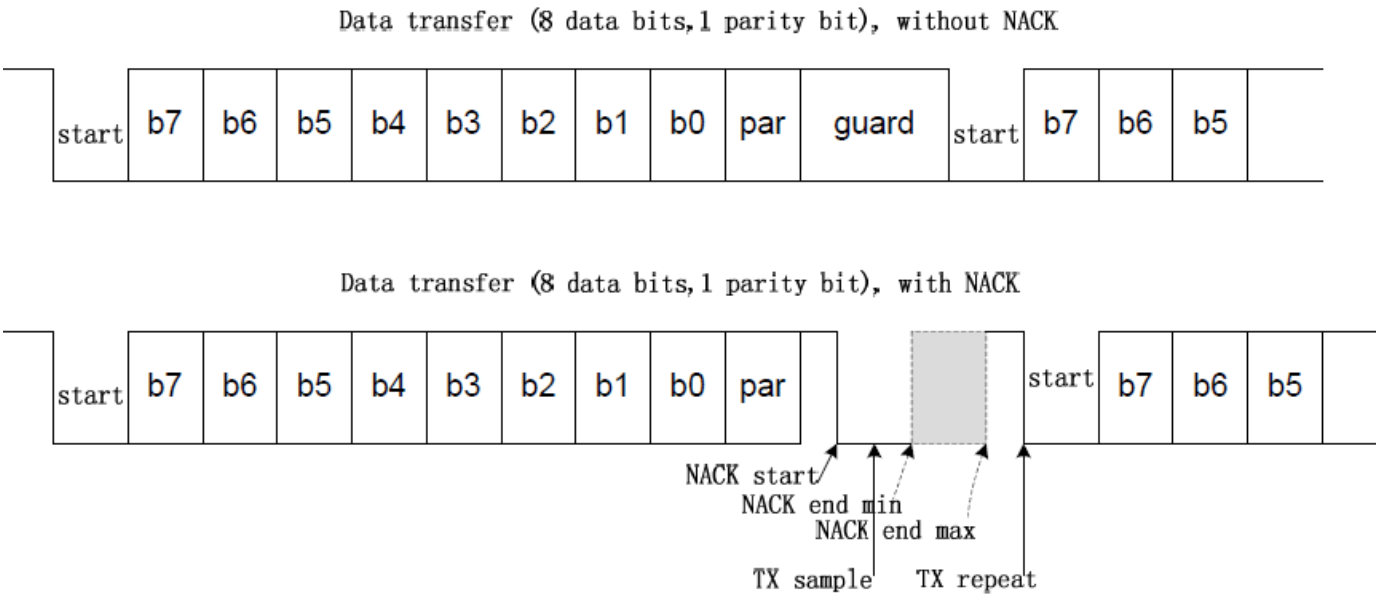
The SmartCard transfer is similar to a UART transfer, with the addition of a negative acknowledgement (NACK) that may be sent from the receiver to the transmitter. A NACK is always ‘0’. Both transmitter and receiver may drive the same I/O line, although never at the same time. Figure 38 illustrates the SmartCard protocol.

Typically, implementations use a tri-state driver with a pull-up resistor, such that when the line is not driven, its value is ‘1’ (the same value as when not transmitting data or the value of the “Stop Bit”).

---

8 Refer to *the ISO/IEC 7816-3:2006 – Identification cards – Integrated circuit cards – Part 3: Cards with contacts – Electrical interface and transmission protocols* (1997) on the ISO web site at www.iso.org

Figure 38. SmartCard Data Transfer Example



A SmartCard transfer has the transmitter drive the “Start Bit” and “Data Bits” and a “Parity Bit”. After these bits, it enters its stop period by releasing the bus. Releasing results in the line being ‘1’ (the value of a “Stop Bit”). After half bit transfer period into the stop period, the receiver may drive a NACK on the line (a value of ‘0’) for one to two bit transfer period. This NACK is observed by the transmitter, which reacts by extending its stop period by one bit transfer period. For this protocol to work, the stop period should be larger than one bit transfer period.

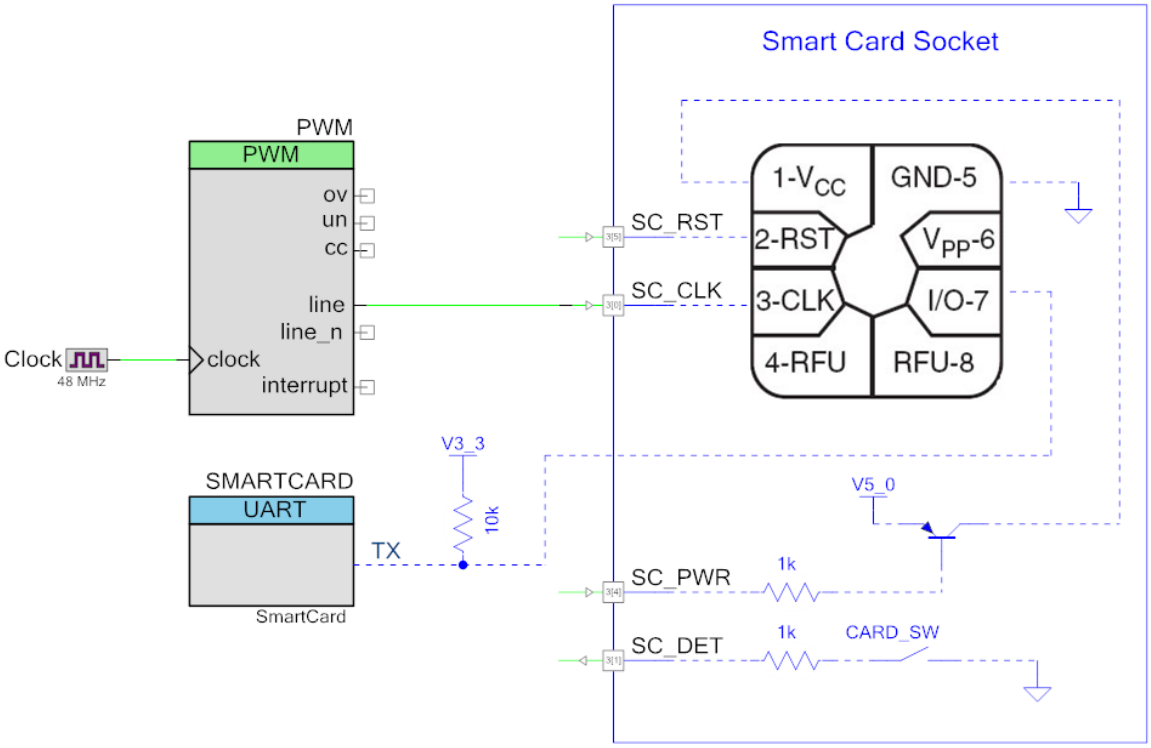
Note Data transfer with a NACK takes one bit transfer period longer than a data transfer without a NACK.

Example implementation of SmartCard reader

You have to consider how to implement a complete SmartCard system with other available system resources for “RST” signal, “CLK” signal, card detect signal, card power supply control signals.

Figure 39 is example of implementing SmartCard reader function with TCPWM and pins Components.

Figure 39. SmartCard reader implementation example



The UART Component is connected to I/O card contact, a pull-up resistor must be connected to this line. SC_RST, SC_CLK are standard card contacts. SC_DET is for card insertion detection. SC_PWR is for control of card power on or off. Refer to the *ISO7816 specification* for more details.

IrDA mode operation

IrDA is defined with “peer to peer” topology. SCB only provides support [9] for IrDA from the basic physical layer with rates from 1200 bps to 115200 bps. The physical layer is responsible for the definition of hardware transceivers for the data transmission. The higher level protocol implementation is left for firmware to handle from the user level.

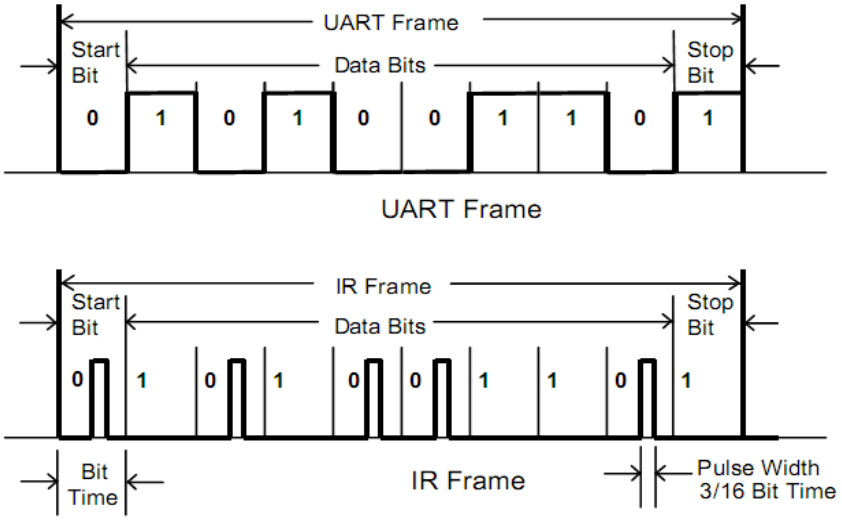
The minimum demand for transmission rates for IrDA is only 9600 bps. All transmissions must be started at this rate to enable compatibility. Higher rates are a matter of negotiation of the ports after establishing the links.

The IrDA protocol adds a modulation scheme to the UART signaling. At the transmitter, bits are modulated. At the receiver, bits are demodulated. The modulation scheme uses a Return-to-Zero-Inverted (RZI) format. A bit value of ‘0’ is signaled by a short ‘1’ pulse on the line and a bit value of ‘1’ is signaled by holding the line to ‘0’. IrDA is using 3/16 RZI modulation.

9 Refer to the *IrPHY (IrDA Physical Layer Link Specification)* (Rev. 1.4 from May 2001) on the IrDA web site at www.irda.org

The Figure 40 shows UART frame and IR frame, comprised a Start Bit, 8 Data Bits, no Parity Bit and ending with a Stop Bit.

Figure 40. UART Frame and IR Frame example



Oversampling Selection

IrDA is using 3/16 RZI modulation, so the sampling clock frequency should be set 16x of selected **Baud rate**, by configuring **Oversampling**. **Oversampling** should always be 16 for IrDA.

Normal versus Low power transmitting

There are two modes of IrDA operation:

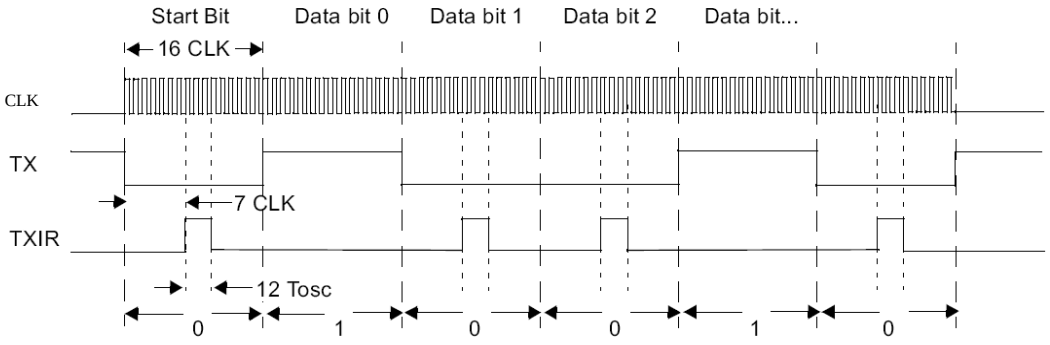
- **Normal transmission** – pulse width is roughly 3/16 of the bit period (for all baud rates)
- **Low power transmission** – pulse width is potentially smaller (down to 1.62 µs typical and 1.41µs minimal) than 3/16 of the bit period (for rates less 115200 bps). Supported only for **RX only** direction.

Inverting RX

This option is used to support two possible demodulation schemes described below.

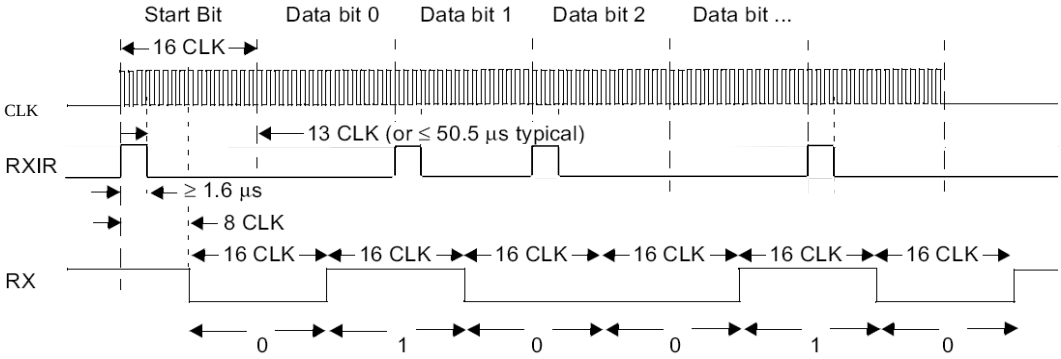
According to the IrPHY specification, the IR frame modulation (encoding) scheme is shown in Figure 41.

Figure 41. IR frame modulation scheme



The IR frame demodulation (decoding) scheme is shown in Figure 42. RXIR line voltage level is default low, active high.

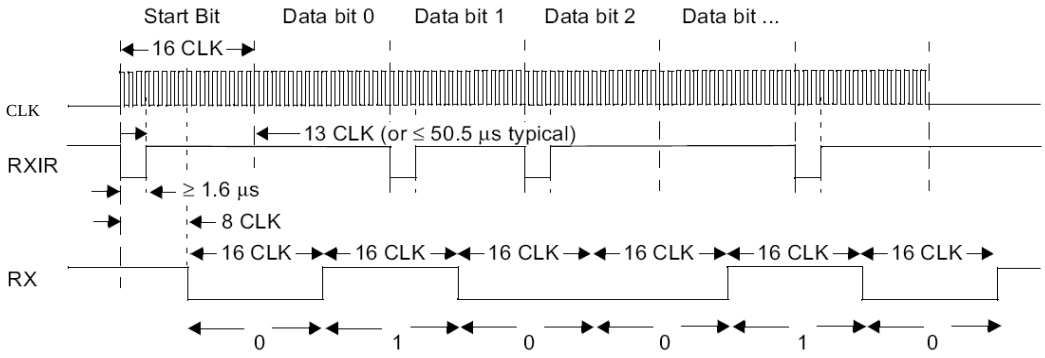
Figure 42. IR frame demodulation scheme 1 (active high)



Note There is a delay from receiving RXIR and decoding RX.

In an application, the RXIR frame output from IrDA transceiver is often pull-up, default high, active low. Figure 43 shows another demodulation scheme.

Figure 43. IR frame demodulation scheme 2 (active low)



FIFO depth

The hardware provides two FIFOs. One is used for receive direction, RX FIFO, and the other for transmit direction, TX FIFO. The FIFO depth is 8 data elements. The width of each data element is 16 bits. The data frame width is configurable from 4-16 bits. One FIFO element is consumed regardless of the data frame width.

PSoC 4100 BLE / PSoC 4200 BLE / PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor devices provide the ability to double the FIFO depth to 16 data elements when the data frame width is 4-8 bits.

Software Buffer

Selecting RX or TX Buffer Size values greater than the FIFO depth enables usage of the RX or TX FIFO and a circular software buffer. The array of requested size is allocated internally by the Component for the TX software buffer. The allocated array for the RX software buffer has one extra element that remains empty while in operation. Keeping this element empty simplifies circular buffer operation. The interrupt option is automatically updated to Internal, and the RX or TX interrupt source are reserved to provide software buffer operation. The internal interrupt handler is hooked up to the interrupt. Its main purpose is to provide interaction between software buffers and the hardware RX or TX FIFO.

The software buffer overflow can happen only for the RX direction when the UART flow control signal RTS is disabled. The data elements read from the RX FIFO that do not fit into the software buffer are discarded. This event is reported via global variable SCB_rxBufferOverflow.

The software buffer overflow is not expected when the RTS signal is enabled. When the RX software buffer becomes full, the RX Not empty interrupt source is disabled and data elements stop reading from the RX FIFO. However, the transfer continues until the number of data elements in the RX FIFO is not equal to the RTS trigger level. Then, the RTS signal is activated

to notify the transmitter to pause the transfer. As soon as the data element has been read from the RX software buffer, the RX Not empty interrupt source is enabled and transfer continues.

For the TX direction, the provided APIs do not allow software buffer overflow.

Interrupts

When **RX buffer size** or **TX buffer size** is greater than the FIFO depth, the **RX FIFO not empty** or **TX FIFO not full** interrupt sources are reserved by the Component for internal software buffer operations. **Do not clear or disable them** because it can cause incorrect software buffer operation. However, it is the user's responsibility to clear interrupts from other enabled interrupt because they are not cleared automatically. Create a custom function that clears these interrupt sources and register it using SCB_SetCustomInterruptHandler(). Each time internal interrupt handler executes the custom function is called before handling software buffer operation. In case **RX buffer size** or **TX buffer size** is equal to the FIFO depth only the hardware TX or RX FIFO is used. In the **Internal** interrupt mode the interrupts are not cleared automatically. It is the user's responsibility to do this. The **External** interrupt mode is preferred in this case.

Low power modes

The Component in UART mode is able to be a wakeup source from Sleep and Deep Sleep low power modes.

Sleep mode is identical to Active from a peripheral point of view. No configuration changes are required in the Component or code before entering/exiting this mode. Any UART activity in TX or RX direction that involves an interrupt to occur leads to wakeup.

Deep Sleep mode requires that the UART be properly configured to be a wakeup source. The Enable wakeup from Deep Sleep Mode option must be checked in the UART configuration dialog (the RX direction must be enabled to allow wakeup). The SCB_Sleep() and SCB_Wakeup() functions must be called before/after entering/exiting Deep Sleep.

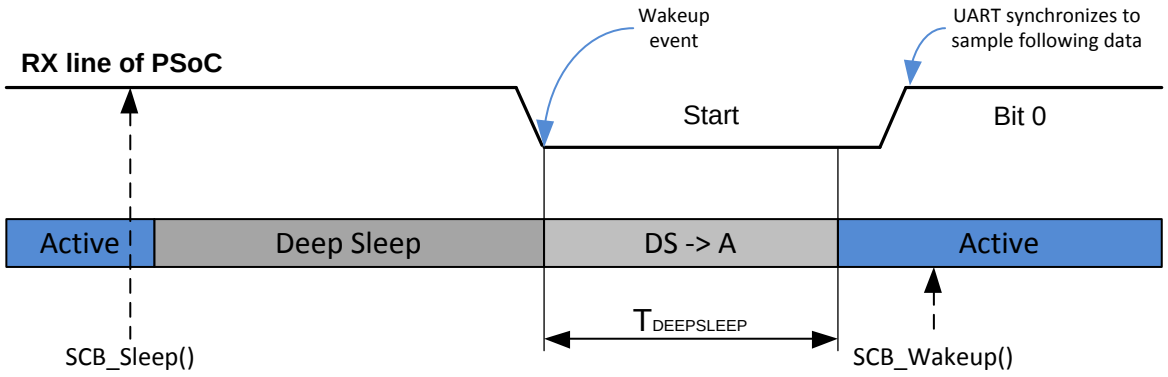
Note The UART rx_wake pin must be placed on a port at which an interrupt is capable of waking the device from Deep Sleep. Refer to the selected device datasheet for more information about ports.

A RX GPIO falling edge event that is generated by the incoming start bit will wake up the device. Note that a RX GPIO interrupt restricts usage of all GPIO interrupts from the port where the UART rx_wake pin is placed.

The SCB block provides feature to skip start and synchronize on the 1st data bit. Usage of this feature implies two constrains:

- The 1st data bit of wakeup transfer has to be '1' to synchronize the UART receiver.
- The wakeup time $T_{DEEPSLEEP}$ of the device must be less than one UART bit duration. Typical $T_{DEEPSLEEP}$ is equal to 25 µs (check selected device datasheet to get actual number of $T_{DEEPSLEEP}$). **This reduces the UART baud rate approximately to 40 kbps**.

Figure 44. UART wakeup (Skip Start enabled)



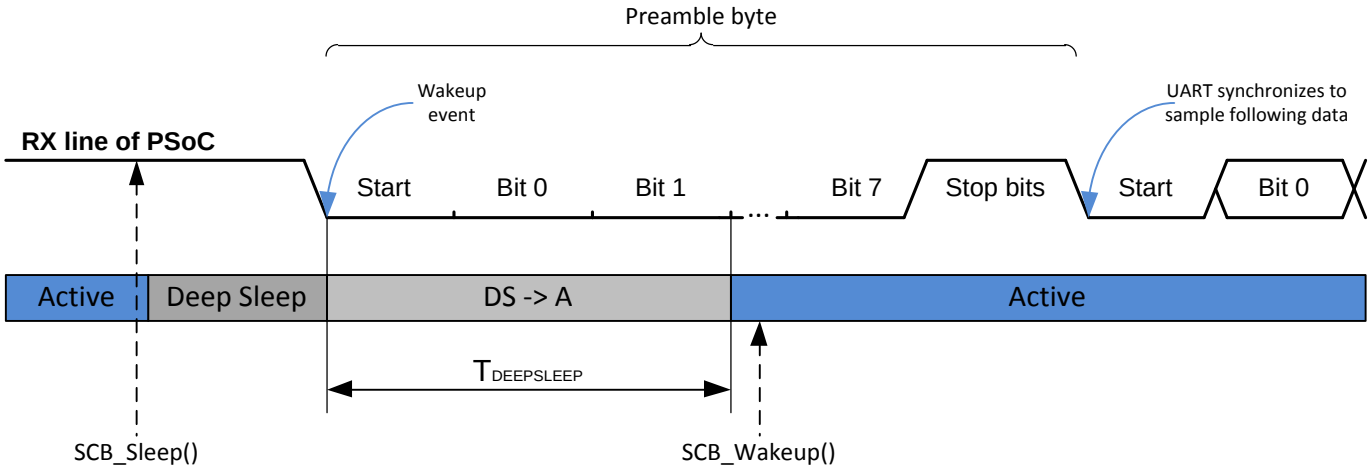
If synchronization does not occur because of violation of the conditions listed below, the UART receiver will synchronize to the 1st bit which is equal to `1` and received byte or all transfer would be corrupted.

Note The UART starts sample data after wakeup when it observes that RX line is high state (not rising edge). This behavior causes that dummy byte is received when wakeup source is not UART and RX line is in idle.

To overcome **UART baud rate limitation and undesired byte reception when other wakeup sources available** the following steps should be done:

- The skip start feature has to be disabled. The SCB_skipStart global variable is provided to manage whether to enable or disable skip start functionality when SCB_Sleep() is called. Set SCB_skipStart equal to 0 after SCB_Start() was called.
- The UART transfer which wakeup the device has to start with preamble which will be discarded while wakeup. The preamble is used to provide enough time for device to wakeup. The number of bytes in the preamble depends on $T_{DEEPSLEEP}$ and UART baud rate. It is recommended to use byte 0x00 for preamble because it does not contain 1 to 0 transition while data bits transfer. Such transition is interpreted by UART as a Start bit and it starts sample data in the middle of data byte therefore following data will not be sampled correctly.

Figure 45. UART wakeup (Skip Start disabled)



The content of TX and RX FIFOs is cleared when the device enters Deep Sleep mode. Therefore, received data should be stored in the SRAM buffer and transmit data should be transferred before entering Deep Sleep mode to avoid data loss. Note that functions that return TX or RX buffer size (SCB_SpiUartGetTxBufferSize() / SCB_SpiUartGetRxBufferSize()) might return different values for hardware and software buffer after exit Deep Sleep: for hardware buffer returned value is always 0 (because FIFOs content is cleared) whereas for software buffer it is equal to number of bytes in available in the Component SRAM buffer.

The transmission is stopped asynchronously while the device enters Deep Sleep mode. The moment that the stop occurs depends on the Enable wakeup from Deep Sleep Mode option. When the option is disabled the SCB_Sleep() API disables the Component and transfer is stopped at that moment. Otherwise, when the Enable wakeup from Deep Sleep Mode is enabled, the transfer is stopped at the moment when the device enters Deep Sleep mode.

The following code is suggested to ensure that transmitter and receiver is ready to enter Deep Sleep mode: transmitter transfer all data from the TX FIFO and shifter register and receiver does not have bytes to handle and it is not started to receive the data.

```
/* For UART baud rate 115200 bps the UART bit period is equal to 8.68us. */
#define SCB_UART_BIT_TIME        (9u) /* unit is 1us */
#define SCB_UART_BITS_TO_WAIT    (2u) /* constant */

void UART_DeepSleepFlow(void)
{
    uint8 intState;
    uint8 bitsToWait = SCB_UART_BITS_TO_WAIT;
    uint8 enterDeepSleep = 1u;

    /* Wait until UART completes transfer data. */
    while (0u != (SCB_SpiUartGetTxBufferSize() + SCB_GET_TX_FIFO_SR_VALID))
    {
    }

    /* Check if there is data in the RX buffer to handle. */
    if (0u == SCB_SpiUartGetRxBufferSize())
```

```
    {
        /* Enter critical section to force all enabled and active interrupts
        * become pending. It is required to not miss any activity that should
        * wake up device before CySysPmDeepSleep() is called.
        */
        intState = CyEnterCriticalSection();

        /* Clear and enable UART wakeup interrupt source.
        * Clear operation is required because UART wakeup source is activated
        * while active mode communication.
        */
        SCB_Sleep();

        /* Wait 2 UART bit periods to make sure that RX line remains in idle
        * state or reception of a byte is started after UART wakeup interrupt
        * source was cleared.
        */
        while (0u != bitsToWait)
        {
            CyDelayUs(SCB_UART_BIT_TIME);
            --bitsToWait;

            /* Check if UART is started sampling the byte.
            * SCB_GET_RX_FIFO_SR_VALID: it is set at the middle of first data
            * bit reception and cleared at the end of (stop bits - 1).
            */
            if (0u != SCB_GET_RX_FIFO_SR_VALID)
            {
                /* Do not allow to enter Deep Sleep. UART started
                * receiving the byte.
                */
                enterDeepSleep = 0u;
                break;
            }
        }

        /* Enter Deep Sleep if RX line is still in idle state. */
        if (0u != enterDeepSleep)
        {
            CySysPmDeepSleep();

            /* Exit critical section to allow interrupt handling. */
            CyExitCriticalSection(intState);

            /* Disable UART wakeup interrupt source. */
            SCB_Wakeup();
        }
        else
        {
            /* Exit critical section to allow interrupt handling. */
            CyExitCriticalSection(intState);
        }
    }
}
```

Printf() function Usage Model

The printf() function formats a series of strings and numeric values and builds a string to write to an output stream. This function can be used in conjunction with a UART to simplify the formatting and transmission of data. This section describes the code required to allow the use of the printf() function with a UART Component.

The printf() function has different implementations in different compilers. Each compiler provides a function that is responsible to send data. These functions are listed below for the supported compilers:

Compiler	Function Name
GCC	_write()
MDK	fputc()
RVDS	fputc()
IAR	__write()

The application should revise these functions to call the communication Component API to send data via the selected interface (in this case, the UART interface).

Note The following code example uses an instance name of "SCB" for the SCB UART Component:

```
#include <project.h>
#include <stdio.h>

#if defined (__GNUC__)
    /* Add an explicit reference to the floating point printf library to allow
       the usage of floating point conversion specifier. */
    asm (".global _printf_float");

    /* For GCC compiler revise _write() function for printf functionality */
    int _write(int file, char *ptr, int len)
    {
        int i;
        for (i = 0; i < len; i++)
        {
            SCB_UartPutChar(*ptr++);
        }

        return(len);
    }

#elif defined(__ARMCC_VERSION)
    /* For MDK/RVDS compiler revise fputc() function for printf functionality */
    struct __FILE
    {
        int handle;
    };

    enum
    {
```

```
        STDIN_HANDLE,
        STDOUT_HANDLE,
        STDERR_HANDLE
    };

    FILE __stdin = {STDIN_HANDLE};
    FILE __stdout = {STDOUT_HANDLE};
    FILE __stderr = {STDERR_HANDLE};

    int fputc(int ch, FILE *file)
    {
        int ret = EOF;

        switch(file->handle)
        {
            case STDOUT_HANDLE:
                SCB_UartPutChar(ch);
                ret = ch;
                break;

            case STDERR_HANDLE:
                ret = ch;
                break;

            default:
                file = file;
                break;
        }

        return(ret);
    }

#elif defined (__ICCARM__)
    /* For IAR compiler revise __write() function for printf functionality */
    size_t __write(int handle, const unsigned char * buffer, size_t size)
    {
        size_t nChars = 0;

        for (/* Empty */; size != 0; --size)
        {
            SCB_UartPutChar(*buffer++);
            ++nChars;
        }

        return (nChars);
    }

#endif /* (__GNUC__) */

int main()
{
    uint32 i = 444444444;
    float f = 55.555f;

    CyGlobalIntEnable;  /* Enable interrupts */
```

```
    SCB_Start();        /* Start communication Component */

    /* Use printf() function which will send formatted data through
    * UART (SCB mode) */
    printf("Test printf function. long: %ld, float: %f \n",i,f);

    for(;;)
    {
        /* Place your application code here. */
    }
}
```

The log from terminal software:

```
Test printf function. long: 444444444, float: 55.555000
```

Note The printf() function prepares the text stream in the buffer and transmits it when new-line character '\n' is reached.

DMA Support

DMA is only available in PSoC 4100M / PSoC 4200M / PSoC 4200L / PSoC Analog Coprocessor devices.

The UART mode may interface with the DMA controller. Signals for transmit and receive direction can be used to trigger a DMA transfer. To enable this signal, the "RX output" or "TX output" option must be enabled in the Component Advanced parameter tab. The RX and TX trigger output signals are hard-wired to the DMA controller; their connection to another source will result in a build error. These signals are level sensitive therefore require the RX or TX FIFO level to be set. The FIFO level signal behavior is as follows:

- RX trigger output – the signal remains active until the number of data elements in the RX FIFO is greater than the value of RX FIFO level.
- TX trigger output – the signal remains active until the number of data elements in the TX FIFO is less than the value of TX FIFO level.

The following table specifies what DMA Component configuration should be used when it is connected to the SCB (UART mode) Component.

DMA Source / Destination name	Direction	Source / Destination transfer width	DMA request signal	DMA trigger type	Description
SCB_RX_FIFO_RD_PTR	Source	Word / Byte or Halfword	rx_tr_out	Level sensitive	Receive FIFO
SCB_TX_FIFO_WR_PTR	Destination	Data bits / Byte or Halfword	tx_tr_out	Level sensitive	Transmit FIFO

Note If the number of data bits are less than or equal to 8 bits the transfer data element width is byte, if the number of data bits are between 9 and 16 bits the width is halfword.

Note The SCB (UART mode) clears request signal within 4 SYSCLK cycles therefore level sensitive configuration of DMA has to be “wait 4 SYSCLK”.

Common SCB Component Information

Macro Callbacks

Macro callbacks allow users to execute code from the API files that are automatically generated by PSoC Creator. Refer to the PSoC Creator Help and *Component Author Guide* for the more details.

In order to add code to the macro callback present in the Component's generated source files, perform the following:

- Define a macro to signal the presence of a callback (in *cyapicallbacks.h*). This will "uncomment" the function call from the Component's source code.
- Write the function declaration (in *cyapicallbacks.h*). This will make this function visible by all the project files.
- Write the function implementation (in any user file).

Callback Function [10]	Associated Macro	Description
SCB_EZI2C_STRETCH_ISR_EntryCallback	SCB_EZI2C_STRETCH_ISR_ENTRY_CALLBACK	Used at the beginning of the SCB_EZI2C_STRETCH_ISR() interrupt handler to perform additional application-specific actions.
SCB_EZI2C_STRETCH_ISR_ExitCallback	SCB_EZI2C_STRETCH_ISR_EXIT_CALLBACK	Used at the end of the SCB_EZI2C_STRETCH_ISR() interrupt handler to perform additional application-specific actions.
SCB_EZI2C_NO_STRETCH_ISR_EntryCallback	SCB_EZI2C_NO_STRETCH_ISR_ENTRY_CALLBACK	Used at the beginning of the SCB_EZI2C_NO_STRETCH_ISR() interrupt handler to perform additional application-specific actions.
SCB_EZI2C_NO_STRETCH_ISR_ExitCallback	SCB_EZI2C_NO_STRETCH_ISR_EXIT_CALLBACK	Used at the end of the SCB_EZI2C_NO_STRETCH_ISR() interrupt handler to perform additional application-specific actions.
SCB_I2C_ISR_EntryCallback	SCB_I2C_ISR_ENTRY_CALLBACK	Used at the beginning of the SCB_I2C_ISR() interrupt handler to perform additional application-specific actions.
SCB_I2C_ISR_ExitCallback	SCB_I2C_ISR_EXIT_CALLBACK	Used at the end of the SCB_I2C_ISR() interrupt handler to perform additional application-specific actions.
SCB_SPI_UART_ISR_EntryCallback	SCB_SPI_UART_ISR_ENTRY_CALLBACK	Used at the beginning of the SCB_SPI_UART_ISR() interrupt handler to perform additional application-specific actions.
SCB_SPI_UART_ISR_ExitCallback	SCB_SPI_UART_ISR_EXIT_CALLBACK	Used at the end of the SCB_SPI_UART_ISR() interrupt handler to perform additional application-specific actions.
SCB_UART_WAKEUP_ISR_EntryCallback	SCB_UART_WAKEUP_ISR_ENTRY_CALLBACK	Used at the beginning of the SCB_UART_WAKEUP_ISR() interrupt handler to perform additional application-specific actions.

10 The callback function name is formed by Component function name optionally appended by short explanation and "Callback" suffix.

Callback Function [10]	Associated Macro	Description
SCB_UART_WAKEUP_ISR_ ExitCallback	SCB_UART_WAKEUP_ISR_ EXIT_CALLBACK	Used at the end of the SCB_UART_WAKEUP_ISR() interrupt handler to perform additional application-specific actions.

Interrupt APIs

These functions are common for most SCB modes.

By default, PSoC Creator assigns the instance name “SCB_1” to the first instance of a Component in a given design. You can rename it to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is “SCB.”

Function	Description
SCB_EnableInt()	Enables the interrupt in the NVIC (when an internal interrupt is used).
SCB_DisableInt()	Disables the interrupt in the NVIC (when an internal interrupt is used).
SCB_GetInterruptCause()	Returns a mask of bits showing the source of the current triggered interrupt.
SCB_SetCustomInterruptHandler()	Registers a function to be called by the internal interrupt handler.
SCB_SetI2cAddressCustomInterruptHandler()	Registers a function to be called by the I^2C slave interrupt handler during the I^2C interrupt address processing
SCB_GetTxInterruptSource()	Returns TX interrupt request register. This register contains current status of TX interrupt sources.
SCB_SetTxInterruptMode()	Writes TX interrupt mask register. This register configures which bits from TX interrupt request register will trigger an interrupt event.
SCB_GetTxInterruptMode()	Returns TX interrupt mask register.
SCB_GetTxInterruptSourceMasked()	Returns TX interrupt masked request register. This register contains logical AND of corresponding bits from TX interrupt request and mask registers.
SCB_ClearTxInterruptSource()	Clears TX interrupt sources in the interrupt request register.
SCB_SetTxInterrupt()	Sets TX interrupt sources in the interrupt request register.
SCB_SetTxFifoLevel()	Sets level in the TX FIFO to generate TX level interrupt.
SCB_GetRxInterruptSource()	Returns RX interrupt request register. This register contains current status of RX interrupt sources.
SCB_SetRxInterruptMode()	Writes RX interrupt mask register. This register configures which bits from RX interrupt request register will trigger an interrupt event.

Function	Description
SCB_GetRxInterruptMode()	Returns RX interrupt mask register.
SCB_GetRxInterruptSourceMasked()	Returns RX interrupt masked request register. This register contains logical AND of corresponding bits from RX interrupt request and mask registers.
SCB_ClearRxInterruptSource()	Clears RX interrupt sources in the interrupt request register.
SCB_SetRxInterrupt()	Sets RX interrupt sources in the interrupt request register.
SCB_SetRxFifoLevel()	Sets level in the RX FIFO to generate RX level interrupt.
SCB_GetMasterInterruptSource()	Returns Master interrupt request register. This register contains current status of Master interrupt sources.
SCB_SetMasterInterruptMode()	Writes Master interrupt mask register. This register configures which bits from Master interrupt request register will trigger an interrupt event.
SCB_GetMasterInterruptMode()	Returns Master interrupt mask register.
SCB_GetMasterInterruptSourceMasked()	Returns Master interrupt masked request register. This register contains logical AND of corresponding bits from Master interrupt request and mask registers.
SCB_ClearMasterInterruptSource()	Clears Master interrupt sources in the interrupt request register.
SCB_SetMasterInterrupt()	Sets Master interrupt sources in the interrupt request register.
SCB_GetSlaveInterruptSource()	Returns Slave interrupt request register. This register contains current status of Slave interrupt sources.
SCB_SetSlaveInterruptMode()	Writes Slave interrupt mask register. This register configures which bits from Slave interrupt request register will trigger an interrupt event.
SCB_GetSlaveInterruptMode()	Returns Slave interrupt mask register.
SCB_GetSlaveInterruptSourceMasked()	Returns Slave interrupt masked request register. This register contains logical AND of corresponding bits from Slave interrupt request and mask registers.
SCB_ClearSlaveInterruptSource()	Clears Slave interrupt sources in the interrupt request register.
SCB_SetSlaveInterrupt()	Sets Slave interrupt sources in the interrupt request register.

void SCB_EnableInt(void)

Description: When using an Internal interrupt, this enables the interrupt in the NVIC. When using an external interrupt the API for the interrupt Component must be used to enable the interrupt.

void SCB_DisableInt(void)

Description: When using an Internal interrupt, this disables the interrupt in the NVIC. When using an external interrupt the API for the interrupt Component must be used to disable the interrupt.

uint32 SCB_GetInterruptCause(void)

Description: Returns a mask of bits showing the source of the current triggered interrupt. This is useful for modes of operation where an interrupt can be generated by conditions in multiple interrupt source registers.

Return Value: uint32: Mask with the OR of the following conditions that have been triggered:

Interrupt causes constants	Description
SCB_INTR_CAUSE_MASTER	Interrupt from Master
SCB_INTR_CAUSE_SLAVE	Interrupt from Slave
SCB_INTR_CAUSE_TX	Interrupt from TX
SCB_INTR_CAUSE_RX	Interrupt from RX

void SCB_SetCustomInterruptHandler(void (*func) (void))

Description: Registers a function to be called by the internal interrupt handler. First the function that is registered is called, and then the internal interrupt handler performs any operations such as software buffer management functions. It is user's responsibility to not break the software buffer operations. Only one custom handler is supported; which is the function provided by the most recent call. At initialization time no custom handler is registered.

Parameters: func: Pointer to the function to register. The value NULL indicates to remove the current custom interrupt handler.

void SCB_SetI2cAddressCustomInterruptHandler(uint32 (*func) (void))

Description: Registers a function to be called by the I^2C slave interrupt handler during the I^2C interrupt address processing. This function should be used when multiple I^2C addresses need to be decoded or general call address supported. The registered function must return decision whether to ACK or NACK accepted address. Only one I^2C address handler is supported, which is the function provided by the most recent call. At initialization time no I^2C address handler is registered.

Parameters: func: Pointer to the function to register. The value NULL indicates to remove the current custom interrupt handler.

The registered function must return decision whether to ACK or NACK accepted address: 0 – ACK, other values – NACK. The registered callback function does not perform the ACK/NACK, this operation is performed in the I2C ISR.

uint32 SCB_GetTxInterruptSource(void)

Description: Returns TX interrupt request register. This register contains current status of TX interrupt sources.

Return Value: uint32: Current status of TX interrupt sources.

Each constant is a bit field value. The value returned may have multiple bits set to indicate the current status.

TX interrupt sources	Description
SCB_INTR_TX_FIFO_LEVEL	The number of data elements in the TX FIFO is less than the value of TX FIFO level.
SCB_INTR_TX_NOT_FULL	Transmitter FIFO is not full.
SCB_INTR_TX_EMPTY	Transmitter FIFO is empty.
SCB_INTR_TX_OVERFLOW	Attempt to write to a full transmitter FIFO.
SCB_INTR_TX_UNDERFLOW	Attempt to read from an empty transmitter FIFO.
SCB_INTR_TX_UART_NACK	UART received a NACK in SmartCard mode.
SCB_INTR_TX_UART_DONE	UART transfer is complete. All data elements from the TX FIFO are sent.
SCB_INTR_TX_UART_ARB_LOST	Value on the TX line of the UART does not match the value on the RX line.

void SCB_SetTxInterruptMode(uint32 interruptMask)

Description: Writes TX interrupt mask register. This register configures which bits from TX interrupt request register will trigger an interrupt event.

Parameters: uint32 interruptMask: TX interrupt sources to be enabled (refer to SCB_GetTxInterruptSource() function for bit field values).

uint32 SCB_GetTxInterruptMode(void)

Description: Returns TX interrupt mask register This register specifies which bits from TX interrupt request register will trigger an interrupt event.

Return Value: uint32: Enabled TX interrupt sources (refer to SCB_GetTxInterruptSource() function for return values).

uint32 SCB_GetTxInterruptSourceMasked(void)

Description: Returns TX interrupt masked request register. This register contains logical AND of corresponding bits from TX interrupt request and mask registers.

This function is intended to be used in the interrupt service routine to identify which of enabled TX interrupt sources cause interrupt event.

Return Value: uint32: Current status of enabled TX interrupt sources (refer to SCB_GetTxInterruptSource() function for return values).

void SCB_ClearTxInterruptSource(uint32 interruptMask)

Description: Clears TX interrupt sources in the interrupt request register.

Parameters: uint32 interruptMask: TX interrupt sources to be cleared (refer to SCB_GetTxInterruptSource() function for return values).

Side Effects: The side effects are listed in the table below for each affected interrupt source. Refer to section TX FIFO interrupt sources for detailed description.

TX interrupt sources	Description
SCB_INTR_TX_FIFO_LEVEL	Interrupt source is not cleared when transmitter FIFO has less entries than level.
SCB_INTR_TX_NOT_FULL	Interrupt source is not cleared when transmitter FIFO has empty entries.
SCB_INTR_TX_EMPTY	Interrupt source is not cleared when transmitter FIFO is empty.
SCB_INTR_TX_UNDERFLOW	Interrupt source is not cleared when transmitter FIFO is empty and I2C mode with clock stretching is selected. Put data into the transmitter FIFO before clearing it. This behavior only applicable for PSoC 4100/PSoC 4200 devices.

void SCB_SetTxInterrupt(uint32 interruptMask)

Description: Sets TX interrupt sources in the interrupt request register.

Parameters: uint32 interruptMask: TX interrupt sources to set in the TX interrupt request register (refer to SCB_GetTxInterruptSource() function for return values).

void SCB_ SetTxFifoLevel(uint32 level)

Description: Sets level in the TX FIFO to generate a TX level interrupt.

When the TX FIFO has more entries than the TX FIFO level an TX level interrupt request is generated.

Parameters: uint32 level: Level in the TX FIFO to generate TX level interrupt

The range of valid level values is between 0 and TX FIFO depth - 1.

uint32 SCB_GetRxInterruptSource(void)

Description: Returns RX interrupt request register. This register contains current status of RX interrupt sources.

Return Value: uint32: Current status of RX interrupt sources.

Each constant is a bit field value. The value returned may have multiple bits set to indicate the current status.

RX interrupt sources	Description
SCB_INTR_RX_FIFO_LEVEL	The number of data elements in the RX FIFO is greater than the value of RX FIFO level.
SCB_INTR_RX_NOT_EMPTY	Receiver FIFO is not empty.
SCB_INTR_RX_FULL	Receiver FIFO is full.
SCB_INTR_RX_OVERFLOW	Attempt to write to a full receiver FIFO.
SCB_INTR_RX_UNDERFLOW	Attempt to read from an empty receiver FIFO.
SCB_INTR_RX_FRAME_ERROR	UART framing error detected.
SCB_INTR_RX_PARITY_ERROR	UART parity error detected.

void SCB_SetRxInterruptMode(uint32 interruptMask)

Description: Writes RX interrupt mask register. This register configures which bits from RX interrupt request register will trigger an interrupt event.

Parameters: uint32 interruptMask: RX interrupt sources to be enabled (refer to SCB_GetRxInterruptSource() function for bit fields values).

uint32 SCB_GetRxInterruptMode(void)

Description: Returns RX interrupt mask register This register specifies which bits from RX interrupt request register will trigger an interrupt event.

Return Value: uint32: Enabled RX interrupt sources (refer to SCB_GetRxInterruptSource() function for return values).

uint32 SCB_GetRxInterruptSourceMasked(void)

Description: Returns RX interrupt masked request register. This register contains logical AND of corresponding bits from RX interrupt request and mask registers.

This function is intended to be used in the interrupt service routine to identify which of enabled RX interrupt sources cause interrupt event.

Return Value: uint32: Current status of enabled RX interrupt sources (refer to SCB_GetRxInterruptSource() function for return values).

void SCB_ClearRxInterruptSource(uint32 interruptMask)

Description: Clears RX interrupt sources in the interrupt request register.

Parameters: uint32 interruptMask: RX interrupt sources to be cleared (refer to SCB_GetRxInterruptSource() function for return values).

Side Effects: The side effects are listed in the table below for each affected interrupt source. Refer to section RX FIFO interrupt sources for detailed description.

RX interrupt sources	Description
SCB_INTR_RX_FIFO_LEVEL	Interrupt source is not cleared when the receiver FIFO has more entries than level.
SCB_INTR_RX_NOT_EMPTY	Interrupt source is not cleared when receiver FIFO is not empty.
SCB_INTR_RX_FULL	Interrupt source is not cleared when receiver FIFO is full.

void SCB_SetRxInterrupt(uint32 interruptMask)

Description: Sets RX interrupt sources in the interrupt request register.

Parameters: uint32 interruptMask: RX interrupt sources to set in the RX interrupt request register (refer to SCB_GetRxInterruptSource() function for return values).

void SCB_SetRxFifoLevel (uint32 level)

Description: Sets level in the RX FIFO to generate a RX level interrupt.

When the RX FIFO has more entries than the RX FIFO level an RX level interrupt request is generated.

Parameters: uint32 level: Level in the RX FIFO to generate RX level interrupt.

The range of valid level values is between 0 and RX FIFO depth - 1.

uint32 SCB_GetMasterInterruptSource(void)

Description: Returns Master interrupt request register. This register contains current status of Master interrupt sources.

Return Value: uint32: Current status of Master interrupt sources.

Each constant is a bit field value. The value returned may have multiple bits set to indicate the current status.

Master interrupt sources	Description
SCB_INTR_MASTER_SPI_DONE	SPI master transfer is complete. Refer to Interrupt sources section for detailed description.
SCB_INTR_MASTER_I2C_ARB_LOST	I2C master lost arbitration.
SCB_INTR_MASTER_I2C_NACK	I2C master received negative acknowledgement (NAK).
SCB_INTR_MASTER_I2C_ACK	I2C master received acknowledgement.
SCB_INTR_MASTER_I2C_STOP	I2C master generated STOP.
SCB_INTR_MASTER_I2C_BUS_ERROR	I2C master bus error (detection of unexpected START or STOP condition).

void SCB_SetMasterInterruptMode(uint32 interruptMask)

Description: Writes Master interrupt mask register. This register configures which bits from Master interrupt request register will trigger an interrupt event.

Parameters: uint32 interruptMask: Master interrupt sources to be enabled (refer to SCB_GetMasterInterruptSource() function for bit field values).

uint32 SCB_GetMasterInterruptMode(void)

Description: Returns Master interrupt mask register This register specifies which bits from Master interrupt request register will trigger an interrupt event.

Return Value: uint32: Enabled Master interrupt sources (refer to SCB_GetMasterInterruptSource() function for return values).

uint32 SCB_GetMasterInterruptSourceMasked(void)

Description: Returns Master interrupt masked request register. This register contains logical AND of corresponding bits from Master interrupt request and mask registers.

This function is intended to be used in the interrupt service routine to identify which of enabled Master interrupt sources cause interrupt event.

Return Value: uint32: Current status of enabled Master interrupt sources (refer to SCB_GetMasterInterruptSource() function for return values).

void SCB_ClearMasterInterruptSource(uint32 interruptMask)

Description: Clears Master interrupt sources in the interrupt request register.

Parameters: uint32 interruptMask: Master interrupt sources to be cleared (refer to SCB_GetMasterInterruptSource() function for return values).

void SCB_SetMasterInterrupt(uint32 interruptMask)

Description: Sets Master interrupt sources in the interrupt request register.

Parameters: uint32 interruptMask: Master interrupt sources to set in the Master interrupt request register (refer to SCB_GetMasterInterruptSource() function for return values).

uint32 SCB_GetSlaveInterruptSource(void)

Description: Returns Slave interrupt request register. This register contains current status of Slave interrupt sources.

Return Value: uint32: Current status of Slave interrupt sources.

Each constant is a bit field value. The value returned may have multiple bits set to indicate the current status.

Slave interrupt sources	Description
SCB_INTR_SLAVE_I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line.
SCB_INTR_SLAVE_I2C_NACK	I2C slave received negative acknowledgement (NAK).
SCB_INTR_SLAVE_I2C_ACK	I2C slave received acknowledgement (ACK).
SCB_INTR_SLAVE_I2C_WRITE_STOP	Stop or Repeated Start event for write transfer intended for this slave (address matching is performed).
SCB_INTR_SLAVE_I2C_STOP	Stop or Repeated Start event for (read or write) transfer intended for this slave (address matching is performed).
SCB_INTR_SLAVE_I2C_START	I2C slave received Start condition.
SCB_INTR_SLAVE_I2C_ADDR_MATCH	I2C slave received matching address.
SCB_INTR_SLAVE_I2C_GENERAL	I2C Slave received general call address.
SCB_INTR_SLAVE_I2C_BUS_ERROR	I2C slave bus error (detection of unexpected START or STOP condition).
SCB_INTR_SLAVE_SPI_BUS_ERROR	SPI slave deselected at an expected time in the SPI transfer.

void SCB_SetSlaveInterruptMode(uint32 interruptMask)

Description: Writes Slave interrupt mask register. This register configures which bits from Slave interrupt request register will trigger an interrupt event.

Parameters: uint32 interruptMask: Slave interrupt sources to be enabled (refer to SCB_GetSlaveInterruptSource() function for bit field values).

uint32 SCB_GetSlaveInterruptMode(void)

Description: Returns Slave interrupt mask register This register specifies which bits from Slave interrupt request register will trigger an interrupt event.

Return Value: uint32: Enabled Slave interrupt sources (refer to SCB_GetSlaveInterruptSource() function for return values).

uint32 SCB_GetSlaveInterruptSourceMasked(void)

Description: Returns Slave interrupt masked request register. This register contains logical AND of corresponding bits from Slave interrupt request and mask registers.

This function is intended to be used in the interrupt service routine to identify which of enabled Slave interrupt sources cause interrupt event.

Return Value: uint32: Current status of enabled Slave interrupt sources (refer to SCB_GetSlaveInterruptSource() function for return values).

void SCB_ClearSlaveInterruptSource(uint32 interruptMask)

Description: Clears Slave interrupt sources in the interrupt request register.

Parameters: uint32 interruptMask: Slave interrupt sources to be cleared (refer to SCB_GetSlaveInterruptSource() function for return values).

void SCB_SetSlaveInterrupt(uint32 interruptMask)

Description: Sets Slave interrupt sources in the interrupt request register.

Parameters: uint32 interruptMask: Slave interrupt sources to set in the Slave interrupt request register (refer to SCB_GetSlaveInterruptSource() function for return values).

Interrupt Function Appliance

Function	I2C	EZI2C	SPI	UART
SCB_EnableInt()	+	+	+	+
SCB_DisableInt()	+	+	+	+
SCB_GetInterruptCause()	+	+	+	+
SCB_SetCustomInterruptHandler() [11]	+	+	+/-	+/-
SCB_SetI2cAddressCustomInterruptHandler()	+	-	-	-
SCB_GetTxInterruptSource()	+	+	+	+
SCB_SetTxInterruptMode()	+	+	+	+
SCB_GetTxInterruptMode()	+	+	+	+
SCB_GetTxInterruptSourceMasked()	+	+	+	+
SCB_ClearTxInterruptSource()	+	+	+	+
SCB_SetTxInterrupt()	+	+	+	+

11 Only available when SPI and UART provide internal interrupt handler.

Function	I2C	EZI2C	SPI	UART
SCB_SetTxFifoLevel()	+	+	+	+
SCB_GetRxInterruptSource()	+	+	+	+
SCB_SetRxInterruptMode()	+	+	+	+
SCB_GetRxInterruptMode()	+	+	+	+
SCB_GetRxInterruptSourceMasked()	+	+	+	+
SCB_ClearRxInterruptSource()	+	+	+	+
SCB_SetRxInterrupt()	+	+	+	+
SCB_SetRxFifoLevel()	+	+	+	+
SCB_GetMasterInterruptSource()	+	–	+	–
SCB_SetMasterInterruptMode()	+	–	+	–
SCB_GetMasterInterruptMode()	+	–	+	–
SCB_GetMasterInterruptSourceMasked()	+	–	+	–
SCB_ClearMasterInterruptSource()	+	–	+	–
SCB_SetMasterInterrupt()	+	–	+	–
SCB_GetSlaveInterruptSource()	+	+	+	–
SCB_SetSlaveInterruptMode()	+	+	+	–
SCB_GetSlaveInterruptMode()	+	+	+	–
SCB_GetSlaveInterruptSourceMasked()	+	+	+	–
SCB_ClearSlaveInterruptSource()	+	+	+	–
SCB_SetSlaveInterrupt()	+	+	+	–

Clock Selection

The SCB is clocked by a single dedicated clock connection. Depending on the mode of operation the frequency of this clock may be calculated by the Component based on the customizer configuration or may be provided externally.

Since the Unconfigured mode customizer is not aware of the end mode of operation the clock must be provided externally in this case.

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the Component. There are two types of deviations defined:

- project deviations – deviations that are applicable for all PSoC Creator Components

- specific deviations – deviations that are applicable only for this Component

This section provides information on Component-specific deviations. Project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment.

The SCB Component has the following specific deviations:

MISRA-C: 2004 Rule	Rule Class [12]	Rule Description	Description of Deviation(s)
1.1	R	This rule states that code shall conform to C ISO/IEC 9899:1990 standard.	Nesting of control structures (statements) exceeds 15 - program does not conform strictly to ISO:C90. In practice, most compilers will support a much more liberal nesting limit and therefore this limit may only be relevant when strict conformance is required. By comparison, ISO:C99 specifies a limit of 127 "nesting levels of blocks. The supported compilers (GCC 4.1.1, RVDS and MDK) support larger number nesting of control structures.
17.4	R	Array indexing shall be the only allowed form of pointer arithmetic.	Component uses array indexing operation to access buffers. The buffer size is checked before access. It is safe operation unless user provides incorrect buffer size.
19.7	A	A function should be used in preference to a function-like macro.	Deviated since function-like macros are used to allow more efficient code.

This Component has the following embedded Components: Pins and Interrupt. Refer to the corresponding Component datasheets for information on their MISRA compliance and specific deviations.

Sample Firmware Source Code

PSoC Creator provides many example projects that include schematics and example code in the Find Example Project dialog. For Component-specific examples, open the dialog from the Component Catalog or an instance of the Component in a schematic. For general examples, open the dialog from the Start Page or **File** menu. As needed, use the **Filter Options** in the dialog to narrow the list of projects available to select.

Refer to the “Find Example Project” topic in the PSoC Creator Help for more information.

Interrupt Service Routine

The SCB supports interrupts on the various events, depending on the mode of operation. All of the interrupt events are ORed together before being sent to the interrupt controller, so the SCB

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can only generate a single interrupt request to the controller at any given time. This signal goes high when any of the enabled interrupt sources are true.

Some of the modes expose this signal as terminal when it is not needed for internal operation as described in the Input/Output Connections section. If it is needed for internal operation the terminal is not present.

Software can service multiple interrupt events in a single interrupt service routine by using various interrupt APIs.

PSoC Creator generates the necessary interrupt service routines for handling internal operation. However it is possible to register a custom function using *SCB_SetCustomInterruptHandler()* function. This user function will be called first, before the internal interrupt handler performs any operations such as software buffer management functions. Only one custom handler is supported.

Note Interrupt sources managed by user are not cleared automatically. It is user responsibility to do that. Interrupt sources are cleared by writing a '1' in corresponding bit position. The preferred way to clear interrupt sources is usage APIs (for example: `SCB_ClearRxInterruptSource()`).

```
void CustomInterruptHandler(void);
void main()
{
    /* Register custom function */
    SCB_SetCustomInterruptHandler(&CustomInterruptHandler);

    /* Initialize SCB Component in UART mode.
    * The SCB_INTR_RX_PARITY_ERROR is already enabled in GUI:
    * UART Advanced Tab.
    */
    SCB_Start();
    CyGlobalIntEnable; /* Enable global interrupts. */
    for (;;)
    {
        /* Place your application code here. */
    }
}

/* User interrupt handler to insert into SCB interrupt handler.
* Note: SCB interrupt set to Internal in GUI.
*/
void CustomInterruptHandler(void)
{
    if (0u != (SCB_GetRxInterruptSourceMasked() & SCB_INTR_RX_PARITY_ERROR))
    {
        /* Interrupt sources does not clear automatically if it is managed by
        * user. The interrupt sources clearing becomes user responsibility.
        */
        SCB_ClearRxInterruptSource(SCB_INTR_RX_PARITY_ERROR);

        /*
        * Add user interrupt code to manage SCB_INTR_RX_PARITY_ERROR.
        */
    }
```

```
}
```

TX FIFO interrupt sources

The following TX interrupt sources have level-sensitive behavior:

- TX FIFO empty
- TX FIFO not full
- TX FIFO level

These interrupt sources trigger the current status of the TX FIFO, and keep it until a clear operation. Clearing these interrupt sources does not make any sense if the current status of the TX FIFO still triggers them, because they are restored back.

The restore operation takes one clock cycle; therefore, the interrupt source is cleared during this time. The restore time causes false clearing of interrupt sources, which might have an undesired impact on the design.

The suggested flow to start TX FIFO interrupt sources processing is as follows:

1. Fill the TX FIFO with data. While filling the TX FIFO, it is better to monitor the number of entries in it rather than try to clear the TX FIFO interrupt source after each byte put in the TX FIFO.
2. Clear the “old” triggered interrupt source. To clear interrupt source, write ‘1’ to the corresponding bit position.
3. Enable the interrupt source.

Note The TX FIFO level interrupt source behavior depends on the level value.

Note The described behavior applies only to PSoC 4100 / PSoC 4200 devices. After the SCB Component is disabled, the TX FIFO becomes empty. It is not possible to clear them due to the restore nature. Therefore, the Component interrupt or TX interrupt sources must be disabled to not cause locking in the interrupt handler after the Component was disabled. For other devices, this behavior is fixed; after the SCB Component is disabled all interrupts are cleared.

RX FIFO interrupt sources

The following RX interrupt sources have level-sensitive behavior:

- RX FIFO not empty
- RX FIFO full
- RX FIFO level

These interrupt sources trigger the current status of the RX FIFO, and keep it until a clear operation. Clearing these interrupt sources does not make any sense if the current status of the RX FIFO still triggers them, because they are restored back. The restore operation takes one clock cycle; therefore, the interrupt source is cleared during this time.

The restore time causes false clearing of RX interrupt sources, which might have an undesired impact on the design.

The suggested flow to start RX FIFO interrupt sources processing is as follows:

1. Clear the “old” triggered interrupt source. To clear interrupt source, write ‘1’ to the corresponding bit position.
2. Then enable the interrupt source.

In most cases the clear operation is not required. While getting data from the RX FIFO, it is better to monitor the number of entries in it rather than try to clear the RX FIFO interrupt source after each byte read from the RX FIFO.

Note The RX FIFO level interrupt source behavior depends on level value.

Note The described behavior applies only to PSoC 4100 / PSoC 4200 devices. After the SCB Component is disabled, the triggered RX FIFO interrupt sources are not cleared automatically. The explicit clear operation must be executed.

Placement

The SCB is placed as Fixed Function block and all placement information is provided to the API through the *cyfitter.h* file. The SCB pins placement information is available in the **Pins** tab of the PSoC Creator Design-Wide Resources (DWR) file. See the *Device datasheet* section *Pinout* for pins functions and placement information.

Generally, debug pins have an alternate function to be SCB pins. To use these pins for SCB functionality, debug capability needs to be disabled in the **System** tab of the PSoC Creator DWR file. Set **Debug Select** option to GPIO to allow the tool to use the alternate function.

Note The debugger will not be functional after choosing this option.

This is specifically important for **PSoC 4000** devices, which have a limited number of pins. The debug pins for this device are P3[0] (SWD_IO) and P3[1] (SWD_CLK). The alternate function of these pins is I^2C functionality SCB[0] (SDA) and SCB[0] (SCL). For other devices, refer to the appropriate device datasheet to determine alternate functions of debug pins.

Registers

See the chip *Technical Reference Manual (TRM)* for more information about registers.

Component Debug Window

PSoC Creator allows you to view debug information about Components in your design. Each Component window lists the memory and registers for the instance. For detailed hardware registers descriptions, refer to the appropriate device technical reference manual.

To open the Component Debug window:

1. Make sure the debugger is running or in break mode.
2. Choose **Windows > Components…** from the **Debug** menu.
3. In the Component Window Selector dialog, select the Component instances to view and click **OK**.

The selected Component Debug window(s) will open within the debugger framework. Refer to the "Component Debug Window" topic in the PSoC Creator Help for more information.

Resources

The SCB is implemented as a fixed-function block.

Configuration			Resource Type		
			Interrupts	Clocks	SCB (Fixed blocks)
Unconfigured SCB			1	1	1
I^2C	Slave / Master / Multi-Master / Multi-Master-Slave		1	1	1
EZ I^2C	Clock stretching: enabled / disabled		1	1	1
SPI	Master / Slave	Hardware buffers [13]	–	1	1
		Software buffers [14]	1	1	1
UART	Standard /Smart Card /IrDA	Hardware buffers [13]	–	1	1
		Software buffers [14]	1	1	1

13 Hardware buffers – The TX and RX buffer size is equal to FIFO depth which is implemented in the hardware; no memory is allocated for the TX or RX buffer. The RX and TX FIFO depth is equal to 8 bytes/words or 16 bytes; refer to Byte mode for more information.

14 Software buffers – The TX and RX buffer size is greater than FIFO depth; the TX and RX FIFOs are still used but the memory is allocated for TX and RX buffer. Internal interrupt handler is automatically enabled to transfer data between the hardware FIFOs and RX and TX memory buffers.

API Memory Usage

The Component memory usage varies significantly, depending on the compiler, device, number of APIs used and Component configuration. The following table provides the memory usage for all APIs available in the given Component configuration.

The measurements have been done with the associated compiler configured in Release mode with optimization set for Size. For a specific design the map file generated by the compiler can be analyzed to determine the memory usage.

Configuration			PSoC 4 (GCC)					
			PSoC 4000		PSoC 4100 / PSoC 4200		All Other PSoC 4	
			Flash	RAM	Flash	RAM	Flash	RAM
Unconfigured SCB			7480	162	11238	180	12378	180
I^2C	Slave		1624	43	1672	43	1572	43
	Master		2560	46	2792	46	2568	46
	Multi-Master		2560	46	2792	46	2568	46
	Multi-Master-Slave		3884	79	4092	79	3832	79
	Slave, Bootloader communication		1700	174	1748	174	1648	174
EZI^2C	Clock stretching enabled	One address	1320	26	1352	26	1268	26
		Two addresses	1752	50	1824	50	1696	50
	Clock stretching disabled [15]	One address	1256	23	1036	24	1212	23
SPI	Slave	Hardware buffers [13]	N/A	N/A	638	5	678	5
		Software buffers [14]	N/A	N/A	1050	25 + BUF_{RAM}	1090	25 + BUF_{RAM}
		Bootloader communication [16]	N/A	N/A	1230	25 + BUF_{RAM}	1230	25 + BUF_{RAM}
	Master	Hardware buffers [13]	N/A	N/A	814	5	862	5
		Software buffers [14]	N/A	N/A	1226	25 + BUF_{RAM}	1274	25 + BUF_{RAM}
UART	Standard [17]	Hardware buffers [13]	N/A	N/A	784	6	1008	6
		Software buffers [14]	N/A	N/A	1260	26 + BUF_{RAM}	1528	26 + BUF_{RAM}
		Bootloader communication [16]	N/A	N/A	1166	26 + BUF_{RAM}	1186	26 + BUF_{RAM}

15 The “Enable wakeup from Deep Sleep Mode” is enabled for all devices other than PSoC 4100 / PSoC 4200.

16 The software buffers are used for bootloader communication operation.

17 The hardware flow control feature is enabled for devices other than PSoC 4100 / PSoC 4200.

BUF_{RAM} = ((RX buffer size + 1) * $BytesNumber_{RX}$) + ((TX buffer size) * $BytesNumber_{TX}$)

where:

- RX buffer size and TX buffer size is equal to appropriate settings on the Advanced Tab for SPI or UART mode.
- $BytesNumber_{RX}$ is number of bytes to store the RX data element. The $BytesNumber_{RX}$ = 1 when RX data bits <= 8 bits and $BytesNumber_{RX}$ = 2 when RX data bits > 8 bits.
- $BytesNumber_{TX}$ is number of bytes to store the TX data element. The $BytesNumber_{TX}$ = 1 when TX data bits <= 8 bits and $BytesNumber_{TX}$ = 2 when RX data bits > 8 bits.

  Note For UART mode the TX and RX data bits options are combined into the single option Data bits which value must be used for BUF_{RAM} calculations instead of $BytesNumber_{RX}$ and $BytesNumber_{TX}$.

DC and AC Electrical Characteristics

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Note Final characterization data for PSoC Analog Coprocessor devices is not available at this time. Once the data is available, the Component datasheet will be updated on the Cypress web site.

PSoC 4000

I^2C DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{I2C1}	Block current consumption at 100 KHz	–	–	10.5	µA	
I_{I2C2}	Block current consumption at 400 KHz	–	–	135	µA	
I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	2.5	µA	

I^2C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{I2C1}	Bit rate	–	–	400	Kbps	

PSoC 4100/PSoC 4200

I²C DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{I2C1}	Block current consumption at 100 KHz	–	–	10.5	µA	
I_{I2C2}	Block current consumption at 400 KHz	–	–	135	µA	
I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	
I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	

I²C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{I2C1}	Bit rate	–	–	1	Mbps	

UART DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	9	µA	
I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	

UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{UART}	Bit rate	–	–	1	Mbps	

SPI DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA	
I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA	
I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA	

SPI AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	

SPI Master AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{DMO}	MOSI valid after Sclock driving edge	–	–	15	ns	
T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns	
T_{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns	

SPI Slave AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	
T_{DSO}	MISO valid after Sclock driving edge	–	–	42 + 3 × Tscb	ns	
T_{HSO}	Previous MISO data hold time	0	–	–	ns	
$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	

PSoC 4100 BLE/PSoC 4200 BLE

I²C DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{I2C1}	Block current consumption at 100 KHz	–	–	50	µA	
I_{I2C2}	Block current consumption at 400 KHz	–	–	155	µA	
I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	
I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	

I²C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{I2C1}	Bit rate	–	–	1	Mbps	

UART DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	µA	
I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	

UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{UART}	Bit rate	–	–	1	Mbps	

SPI DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA	
I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA	
I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA	

SPI AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	

SPI Master AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{DMO}	MOSI valid after Sclock driving edge	–	–	18	ns	
T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns	
T_{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns	

SPI Slave AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	
T_{DSO}	MISO valid after Sclock driving edge	–	–	42 + 3 × Tscb	ns	
T_{HSO}	Previous MISO data hold time	0	–	–	ns	
$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	

PSoC 4100M/PSoC 4200M

I²C DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{I2C1}	Block current consumption at 100 KHz	–	–	50	µA	
I_{I2C2}	Block current consumption at 400 KHz	–	–	135	µA	
I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	
I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	

I²C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{I2C1}	Bit rate	–	–	1	Mbps	

UART DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	µA	
I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	

UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{UART}	Bit rate	–	–	1	Mbps	

SPI DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA	
I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA	
I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA	

SPI AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	

SPI Master AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{DMO}	MOSI valid after Sclock driving edge	–	–	15	ns	
T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns	
T_{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns	

SPI Slave AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	
T_{DSO}	MISO valid after Sclock driving edge	–	–	42 + 3 × Tscb	ns	
T_{HSO}	Previous MISO data hold time	0	–	–	ns	
$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	

PSoC 4100L

I²C DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{I2C1}	Block current consumption at 100 KHz	–	10.5	55	µA	
I_{I2C2}	Block current consumption at 400 KHz	–	–	135	µA	
I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	
I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	

I²C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{I2C1}	Bit rate	–	–	1	Mbps	

UART DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{UART1}	Block current consumption at 100 Kbits/sec	–	9	55	µA	
I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	

UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{UART}	Bit rate	–	–	1	Mbps	

SPI DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA	
I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA	
I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA	

SPI AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	

SPI Master AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{DMO}	MOSI valid after Sclock driving edge	–	–	15	ns	
T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns	
T_{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns	

SPI Slave AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	
T_{DSO}	MISO valid after Sclock driving edge	–	–	42 + 3 × Tscb	ns	
T_{HSO}	Previous MISO data hold time	0	–	–	ns	
$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	

PSoC 4000S / PSoC 4100S

I²C DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{I2C1}	Block current consumption at 100 KHz	–	–	50	µA	–
I_{I2C2}	Block current consumption at 400 KHz	–	–	135	µA	–
I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	–
I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	–

I²C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{I2C1}	Bit rate	–	–	1	Mbps	–

UART DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	µA	–
I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	–

UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{UART}	Bit rate	–	–	1	Mbps	–

SPI DC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA	–
I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA	–
I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA	–

SPI AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	–

SPI Master AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{DMO}	MOSI valid after Sclock driving edge	–	–	15	ns	–
T_{DSI}	MISO valid before Sclock capturing edge	20	–	–	ns	Full clock, late MISO sampling
T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

SPI Slave AC Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
T_{DSO}	MISO valid after Sclock driving edge	–	–	42 + 3 × Tscb	ns	Tscb = 1 / Fscb[18]
T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	–	–	100	ns	–

Component Errata

This section lists known problems with the Component.

Cypress ID	Component Version	Problem	Workaround
243067	3.20	When operating in UART mode and “Byte mode” is selected, Interrupt is Internal, and “RX FIFO not empty” interrupt source is enabled, the next time you open the Configure dialog, it shows that the “RX FIFO not empty” interrupt source is **disabled**. This is a visibility problem; “RX FIFO not empty” is enabled in the Component. However, you can enable “RX FIFO not empty” interrupt source to make sure.	Enable the “RX FIFO not empty” interrupt source on the UART Configure dialog’s **Advanced** tab.

254433	All	When operating in Unconfigured mode and the configuration is set by calling SCB_SpiInit() or SCB_UartInit(), the RX and TX buffer sizes from the configuration structure are casted to uint8. This will cause the Component to fail if the requested buffer size is greater than 255 bytes.	Assign Component variables that store buffer size after SCB_SpiInit() or SCB_UartInit() is called.
			Code example for UART:
			`SCB_UartInit(&configUart);`
			`SCB_rxBufferSize = configUart.rxBufferSize;`
			`SCB_txBufferSize = configUart.txBufferSize;`

[18] Fscb – clock frequency provided to the SCB block.

Cypress ID	Component Version	Problem	Workaround

260180	All	When operating in I²C Master modes and the master attempts to start the transfer the noise on SDA line can cause multiple bus error conditions from which the firmware cannot recover. After this failure the master drives Start condition on the bus and then holds SCL and SDA lines low. The firmware might lock up in the I²C interrupt handler.	The master command to generate Start condition must be cleared after any error condition was detected.
			The code below catches the master error conditions before it is handed inside the interrupt hander and clears master command register (the I²C entry callback is used):
			`void SCB_I2C_ISR_EntryCallback(void)`
			`{`
			`  if(`
			`  SCB_CHECK_INTR_MASTER_MASKED(`
			`  SCB_INTR_MASTER_I2C_BUS_ERROR) ||`
			`  SCB_CHECK_INTR_MASTER_MASKED(`
			`  SCB_INTR_MASTER_I2C_ARB_LOST)`
			`  )`
			`  {`
			`  /* Clear command register in`
			`  * case of error.`
			`  */`
			`  SCB_I2C_MASTER_CMD_REG = 0UL;`
			`  }`
			`}`

298314	All	When calling the SCB_I2CMasterWriteBuf() function to execute an I2C write transaction with a restart condition, the master might send the first data byte instead of the address byte. This will occur if execution of the function is interrupted for a time longer than the restart condition, between setting the restart generation command and writing the address byte into the TX FIFO.	Call the SCB_I2CMasterWriteBuf() function inside the critical section so it will not be interrupted when you need to execute a write transaction with a restart condition.

Component Changes

This section lists the major changes in the Component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
3.20.e	Updated datasheet.	Added errata for issue 298314.
3.20.d	Minor datasheet edits.	
3.20.c	Updated datasheet.	Added errata for issue 260180. Minor datasheet updates. Added final characterization data for PSoC 4100S device.

Version	Description of Changes	Reason for Changes / Impact
3.20.b	Updated datasheet.	Added errata for issues 243067 and 254433. Updated description of SCB_SpiIsBusBusy() function to reflect hardware behavior. Added final characterization data for PSoC 4000S device.
3.20.a	Updated SCB_Enable() function to restore TX interrupt sources which are not level-triggered after SCB_Stop() was called. Only applicable for SPI and UART modes. Added global variable SCB_IntrTxMask which contains TX interrupt sources which will be enabled after SCB_Enable() is called.	All TX interrupt sources are disabled when SCB_Stop() is called and not restored when block is enabled.
	Updated datasheet.	Provide examples for TX and RX level operation. Final characterization data for PSoC 4000S, PSoC 4100S and PSoC Analog Coprocessor devices is not available at this time. Once the data is available, the Component datasheet will be updated on the Cypress web site.
3.20	Added PSoC 4000S, PSoC 4100S and PSoC Analog Coprocessor devices support.	New devices support.
	Added SmartIO support for SPI and UART modes.	Support for new feature.
	Fixed Configure dialog behavior of UART “RX FIFO not empty” interrupt source the RX buffer size is equal to 16 data elements and the “Byte mode” parameter is enabled.	Fixed Errata for previous Component versions.
	Added global variable SCB_skipStart to control if enable or disable UART skip start feature when SCB_Sleep() is called.	Enhancement of UART wakeup from Deep Sleep functionality. Refer to UART Low power modes section for the details.
	Datasheet update.	Added diagrams with TX and RX interrupt sources. Updated SPI and UART Low Power modes sections. Provided code examples about how to enter low power mode.
3.10	Added PSoC 4200L device support.	New device support.
3.0.b	Datasheet update.	Added Macro Callbacks section.
3.0.a	Edited datasheet to add Component Errata section.	Document an issue with “RX FIFO not empty” interrupt source when operating in UART mode.
3.0	Added support for PSoC 4100M / PSoC 4200M/ PSoC 4200L devices.	
	Added support of General call address, as well as improved access to addresses received into the RX FIFO for I2C mode.	

Version	Description of Changes	Reason for Changes / Impact
	Added support of SPI pins remove.	
	Added support of bootloader communication for SPI and UART modes.	
	Made pin names consistent among all devices in SCB Unconfigured mode.	Version 3.0 is not completely backward compatible with the previous Component version 2.0 but only for SCB Unconfigured mode. Due to pin names change the compilation error will occur if you use buried pin APIs. Update APIs with new names to fix the compilation error.
	Fixed SCB_RX_BUFFER_SIZE define to be equal to RX software buffer size. This define is equal to the RX software buffer size plus one in the previous Component versions.	This change is not backward compatible with the previous Component versions.
	Noted that the SCB_Stop() also disables all TX interrupt sources so as not to cause an unexpected interrupt trigger because after the Component is enabled, the TX FIFO is empty.	This change is not backward compatible with the previous Component versions. The Component restores TX interrupt sources which it utilizes but not the user configured TX interrupt sources. They have to be restored by the user.
	Fixed SPI master and UART output pins behavior when the Component is disabled. The SPI master SCLK and/or SS0-SS3 and UART TX and/or RTS pins keep inactive state.	The SPI master and UART output pins becomes High-Z when the Component is disabled. This can cause false SPI slave or UART receiver activation.
	Removed timeout from I2C bootloader write function SCB_CyBtldrCommWrite(). The function does not use timeout and returns after data has been copied into the slave read buffer.	The slave read buffer available to be read by the bootloader host until following host data write.
	Fixed RX software buffer processing which allows buffer to be overflown when UART flow control is enabled.	The RTS signal has to protect UART receiver from overflow event to occur.
	Minor improvements to the interrupt handler for EZI2C without clock stretching.	
	Datasheet updates.	Updated sample code in I²C Low power modes and EZI²C Low power modes sections to use CyEnterCriticalSection() / CyExitCriticalSection() instead of CyGlobalIntEnable / CyGlobalIntDisable. Updated I²C External Electrical Connections and added Internal Pull-Ups sections. Updated SPI Low power modes and UART Low power modes sections. Updated DC and AC Electrical Characteristics section with PSoC 4100M/ PSoC 4200M/ PSoC 4200L data.

Version	Description of Changes	Reason for Changes / Impact
2.0.a	Datasheet updates.	Fixed a few summary tables to add/remove tables, plus a few minor edits. Updated descriptions for a few APIs. Updated the characterization data.
2.0	Added support for Bluetooth Low Energy devices.	
	Improved internal clock selection logic for all modes. Restricted the I2C master and slave clock frequency requirements to meet I2C specification parameters.	Version 2.0 is not completely backward compatible with the previous Component version 1.20. Internal clock selection has changed for I2C, EZI2C, SPI and UART modes. To make version 2.0 backward compatible the “Clock from terminal” option with previous clock settings should be used. To do this you need to discover the clock frequency for the SCB that was used in version 1.20. This can be found by looking at the Clock tab of the .cydwr file. Find a clock that ends in _SCBCLK. In version 2.0 enable the “Clock from terminal” option in the Component. Next, connect a clock Component to the clock terminal on the SCB Component. Set this clock frequency to the same frequency as the clock used in version 1.20. The I2C Slave restricts the input clock frequency to be no less than 1.58 MHz. The clock frequency must be increased to reach minimum requirement to build the project.
	Removed Median filter option from the I2C and EZ I2C modes. The median filter option is set depends on the selected data rate.	The analog filters applied to I2C lines for most data rate modes. There is no reason to apply both filters: analog and median (digital). For I2C master modes with data rate greater than 400 kbps (Fast Plus) only median (digital) filter is applied. If Unconfigured SCB was utilized with previous version of the Component and configured to I2C mode the dataRate field of configuration structure has to be initialized for correct filter selection.
	The SCB_Sleep() and SCB_Wakeup() functions were modified for I2C and EZI2C slave (clock stretching enabled) modes for PSoC 4000. For more information refer to Low power modes section of the appropriate mode.	This change intended to address the SCL lock up after wakeup from Deep Sleep on address match event.
	Fixed the I2C master operation in the Multi-Master-Slave mode when Enable wakeup from Deep Sleep Mode option is enabled for PSoC 4000.	The master was not able to able to start communication.

Version	Description of Changes	Reason for Changes / Impact
	Added APIs to set level in the RX and TX FIFO to generate appropriate level interrupt: void SCB_SetRxFifoLevel(uint32 level) void SCB_SetTxFifoLevel(uint32 level)	
	Removed SPI Master slave select routing constrains.	SPI Master slave select output pin can be placed to the any allowed slave select location, ss0-ss3.
	The Number of SS lines is allowed to be 0 for SPI Master.	This allows removal of all hardware slave select lines in Master mode. It is useful when slave select control required to be implemented in firmware.
	Changed SPI Master minimum Oversampling value to 6 and removed dependencies from other parameters.	Fixed incorrect oversampling limitations.
	Added API function to access SPI bus state: SCB_SpiIsBusBusy()	This function facilitates detection that SPI transfer is completed.
	Add protection from the Component interruption to the following APIs: SCB_I2CSlaveInitReadBuf() SCB_I2CSlaveInitWriteBuf() SCB_I2CSlaveClearReadStatus() SCB_I2CSlaveClearWriteStatus() SCB_I2CMasterClearStatus() SCB_I2CMasterStatus() SCB_I2CMasterClearWriteBuf() SCB_I2CMasterClearReadBuf() SCB_EzI2CSetBuffer1() SCB_EzI2CSetBuffer2()	I2C and EZI2C operations executed by the listed functions are atomic.
1.20	Fixed EZ I2C with clock stretching operation when SCB Unconfigured mode is selected.	The complier gives warning while compilation.
	Fixed EZ I2C mode with clock stretching buffer update when master writes number of bytes multiplied of 8 and starts from base address multiplied of 8.	The EZ I2C slave completes transfer too early and last 8 bytes remains in the RX FIFO. The buffer is not updated properly.
	Fixed EZ I2C current address behavior for buffer size equal to 256 bytes.	When buffer read or write overflow is occurred the current address wraps around to first element instead point to outside the buffer.
	Improved interrupt handling timings for EZ I2C mode without clock stretching.	

Version	Description of Changes	Reason for Changes / Impact
	Added support of PSoC 4000 devices.	
1.10	EZ I2C mode added.	
	SPI/UART internal interrupt source to transfer data from the internal software buffer into the TX FIFO is changed from TX_EMPTY to TX_NOT_FULL.	This change will result in the TX FIFO being kept full when data is available in the software buffer. This will reduce the likelihood that the FIFO will become empty during a transmission due to a long interrupt response time.
1.0.a	Edits to the Component datasheet to match the GUI.	
1.0	The first release of the SCB Component	

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