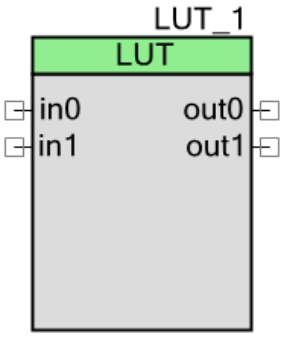
Lookup Table (LUT)
1.50

Features



- 1 to 5 inputs
- 1 to 8 outputs
- Configuration tool
- Optionally registered outputs

General Description

You can set up the Lookup Table (LUT) component to perform any logic function with up to five inputs and eight outputs. This is done by generating logic equations that are realized in the UDB PLDs. Optionally, the outputs can be registered. These registers are implemented in PLD macrocells. All macrocell flip-flops are initialized to a 0 value at power up and after any reset of the device.

When to Use a Digital LUT

Use the LUT any time you need a particular input combination to generate a specific set of outputs. The LUT allows you to easily specify the input to output relationship without having to generate specific gate-level combinatorial logic. You can use the optional registered output mode to generate sequential logic. You can also create state machines by registering the outputs and routing some of the outputs back to the LUT inputs.

Input/Output Connections

This section describes the various input and output connections for the LUT. An asterisk (*) in the list of I/Os states that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

in0 to in4 – Input

At least one input is required for this component. You can add up to four additional inputs.

clock – Input *

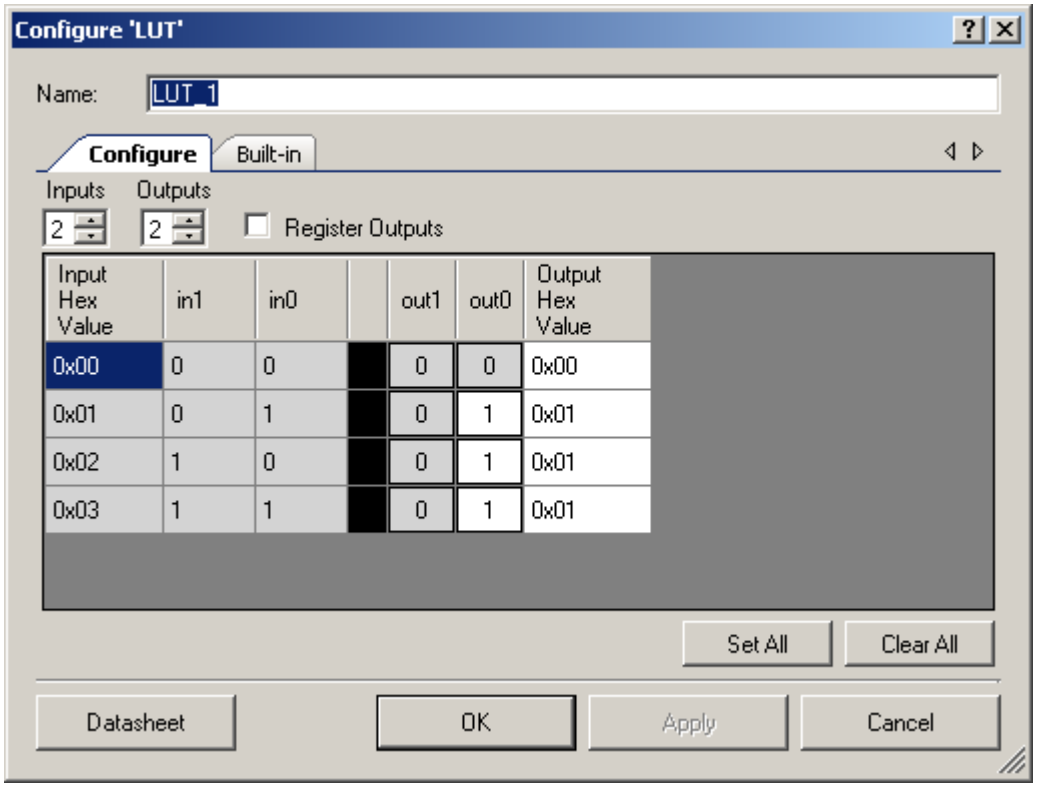
Select the **Register Outputs** option to enable the clock input.

out0 to out7– output

At least one output is required for this component. You can add up to seven additional outputs.

Component Parameters

Drag a LUT component onto your design and double-click it to open the **Configure** dialog.



The LUT provides the following parameters.

Hardware Configuration Options

The LUT can configure all of its outputs for all of the possible input combinations. Additionally it can be configured to register the output data on the rising edge of an input clock.

Software Configuration Options

The LUT is a hardware-only block and therefore does not have any software configuration options.

Default Configuration

When first instantiated, the default LUT is configured with two inputs and two outputs. The **Register Outputs** option is not selected.

Clock Selection

The Clock input of the LUT is only available if the **Register Outputs** option is selected. All outputs will be registered on the rising edge of this clock. You may select any clock in the system, but if any of the outputs go to an I/O they will not work correctly if the LUT is operating faster than 33 MHz (the fastest I/O operating speed).

Resources

The LUT component is implemented with logic expressions and therefore are synthesized and mapped into PLD blocks within the UDB array. The number of component inputs and outputs determine the size of the logic equations and thus the number of PLDs used.

Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
1.50.c	Minor datasheet edits and updates	
1.50.b	Minor datasheet edits and updates	
1.50.a	Minor datasheet edits and updates	
1.50	Updated Configure dialog.	Disabled the Expression View to allow only using the Configure tab.

© Cypress Semiconductor Corporation, 2008-2012. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

PSoC® is a registered trademark, and PSoC Creator™ and Programmable System-on-Chip™ are trademarks of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein are property of the respective corporations.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.