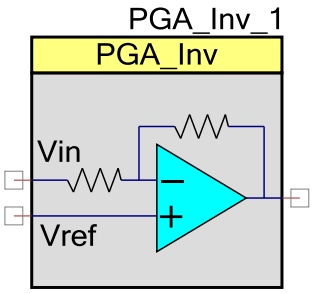
Inverting Programmable Gain Amplifier (PGA_Inv)

1.50

Features

- Gain steps from -1 to -49
- High input impedance
- Adjustable power settings



General Description

The Inverting Programmable Gain Amplifier (PGA_Inv) component implements an opamp-based inverting amplifier with user-programmable gain. It is derived from the SC/CT block.

The inverting gain can be between -1.0 (0 dB) and -49.0 (+33.8 dB). The gain can be selected via configuration or changed at run-time using the provided API. The maximum bandwidth is limited by the gain-bandwidth of the opamp and is reduced as the gain is increased. The input of the PGA_Inv operates from rail to rail, but the maximum input swing (difference between Vin and Vref) is limited to Vdda/Gain. The output of the PGA_Inv is class A, and is rail to rail for sufficiently high load resistance.

The PGA_Inv is used when an input signal has insufficient amplitude and the preferred output polarity is the inverse of the input. A PGA_Inv may be placed in front of a comparator, ADC, or mixer to increase the signal amplitude. A unity gain PGA_Inv may be used following another gain stage or buffer to generate differential outputs.

Input/Output Connections

This section describes the various input and output connections for the PGA_Inv. An asterisk (*) in the list of I/Os indicates that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

Vin – Analog

Vin is the input signal terminal.

Vref – Analog

Vref is the input terminal for a reference signal. The reference input has a high impedance and may be connected to fixed reference (e.g., Vdda/2), VDAC output or routed to a pin.

Vout – Analog

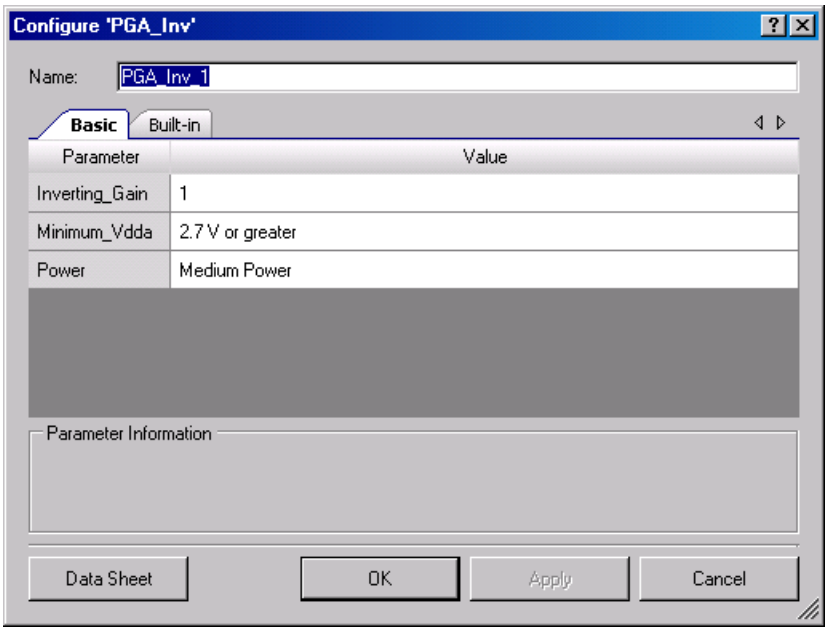
Vout is the output voltage signal terminal. Vout is a function of (Vin - Vref) times the Gain:

*Vout = Vref + (Vin-Vref) * Gain* where Gain is a negative value

Parameters and Setup

Drag a PGA_Inv component onto your design and double-click it to open the Configure dialog.

Figure 1 Configure PGA_Inv Dialog



Inverting_Gain

This parameter is used to set the default gain of the amplifier. The allowable inverting gains provided are: -1 (default), -3, -7, -15, -22, -24, -31, -47, and -49.

Minimum_Vdda

This parameter is determined by the minimum analog supply voltage expected for the PSoC in the design. The parameter can be set to one of two values:

- 2.7 V or greater (default)
- Less than 2.7 V

For an analog supply voltage below 2.7 V, the amplifier makes use of an internal boost circuit. The component implementation uses an additional 10 MHz clock to drive the boost circuit for the amplifier block.

Power

This sets the initial drive power of the PGA_Inv. The **Power** setting determines the speed with which the PGA_Inv responds to changes in the input signal. There are four **Power** settings: Minimum, Low, Medium (default), and High. A Low setting results in the slowest response time and a High setting results in the fastest response time. The **Power** setting can be set at runtime using the SetPower() API.

Placement

There are no placement specific options.

Resources

The PGA_Inv uses one SC/CT block. Additional details on this block can be found in the applicable device data sheet and the Technical Reference Manual (TRM). These documents are available on the Cypress web site.

Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software. The following table lists and describes the interface to each function. The subsequent sections cover each function in more detail.

By default, PSoC Creator assigns the instance name "PGA_Inv_1" to the first instance of a component in a given design. You can rename the instance to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is "PGA_Inv".

Function	Description
void PGA_Inv_Init(void)	Initializes or restores default PGA_Inv configuration.
void PGA_Inv_Enable(void)	Enables the PGA_Inv.
void PGA_Inv_Start(void)	Start the PGA_Inv.
void PGA_Inv_Stop(void)	Power down the PGA_Inv.
void PGA_Inv_SetGain(uint8 gain)	Set gain to pre-defined constants.
void PGA_Inv_SetPower(uint8 power)	Set drive power to one of four settings.

Function	Description
void PGA_Inv_Sleep(void)	Stops and saves the user configurations.
void PGA_Inv_Wakeup(void)	Restores and enables the user configurations.
void PGA_Inv_SaveConfig(void)	Empty function. Provided for future usage.
void PGA_Inv_RestoreConfig(void)	Empty function. Provided for future usage.

Global Variables

Variable	Description
PGA_Inv_initVar	Indicates whether the PGA_Inv has been initialized. The variable is initialized to 0 and set to 1 the first time PGA_Inv_Start() is called. This allows the component to restart without reinitialization after the first call to the PGA_Inv_Start() routine. If reinitialization of the component is required, then the PGA_Inv_Init() function can be called before the PGA_Inv_Start() or PGA_Inv_Enable() function.

void PGA_Inv_Init(void)

Description: Initializes or restores default PGA_Inv configuration.

Parameters: None

Return Value: None

Side Effects: All registers will be reset to their initial values. This will re-initialize the component.

void PGA_Inv_Enable(void)

Description: Enables the PGA_Inv.

Parameters: None

Return Value: None

Side Effects: None

void PGA_Inv_Inv_Start(void)

Description: Turns on the PGA_Inv and sets the power level.

Parameters: None

Return Value: None

Side Effects: None

void PGA_Inv_Stop(void)

Description: Turn off PGA_Inv and enable its lowest power state.

Parameters: None

Return Value: None

Side Effects: None. Does not affect power or gain settings.

void PGA_Inv_SetGain(uint8 gain)

Description: Set gain of amplifier between -1 and -49. The table below shows the valid gain settings.

Parameters: Uint8 gain: Set the gain to a specific value. See table below for valid gain settings.

Gain Setting	Notes
PGA_Inv_GAIN_01	Gain = -1
PGA_Inv_GAIN_03	Gain = -3
PGA_Inv_GAIN_07	Gain = -7
PGA_Inv_GAIN_15	Gain = -15
PGA_Inv_GAIN_22	Gain = -22
PGA_Inv_GAIN_24	Gain = -24
PGA_Inv_GAIN_31	Gain = -31
PGA_Inv_GAIN_47	Gain = -47
PGA_Inv_GAIN_49	Gain = -49

Return Value: None

Side Effects: None

void PGA_Inv_SetPower(uint8 power)

Description: Sets the drive power to one of four settings; minimum, low, medium, or high.

Parameters: (uint8) power: Sets the power level to one of three settings, low, medium, or high.

Power Setting	Notes
PGA_Inv_MINPOWER	Minimum active power and slowest reaction time.
PGA_Inv_LOWPOWER	Low power and speed.
PGA_Inv_MEDPOWER	Medium power and speed.
PGA_Inv_HIGHPOWER	Highest active power and fastest reaction time.

Return Value: None

Side Effects: None

void PGA_Inv_Sleep(void)

Description: Stops the component operation. Saves the configuration registers and the component enable state. Should be called just prior to entering sleep

Parameters: None

Return Value: None

Side Effects: None

void PGA_Inv_Wakeup(void)

Description: Restores the component enable state and configuration registers. Should be called just after awaking from sleep

Parameters: None

Return Value: None

Side Effects: None

void PGA_Inv_SaveConfig(void)

Description: Empty function. Provided for future usage.

Parameters: None

Return Value: None

Side Effects: None

void PGA_Inv_RestoreConfig(void)

Description: Empty function. Provided for future usage.

Parameters: None

Return Value: None

Side Effects: None

Sample Firmware Source Code

The following is a C language example demonstrating the basic functionality of the PGA_Inv component. This example assumes the component has been placed in a design with the default name "PGA_Inv_1."

Note If you rename your component you must also edit the example code as appropriate to match the component name you specify.

```
#include <device.h>

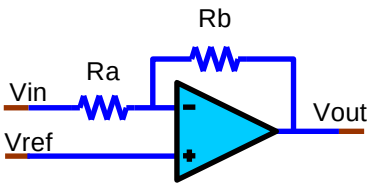
void main()
{
    PGA_Inv_1_Start();
    PGA_Inv_1_SetGain(PGA_Inv_1_GAIN_24);
    PGA_Inv_1_SetPower(PGA_Inv_1_MEDPOWER);
    PGA_Inv_1_Sleep();
    PGA_Inv_1_Wakeup();
}
```

Functional Description

The PGA_Inv is constructed from a generic SC/CT block. The gain is selected by adjusting two resistors, Ra and Rb. (See the following figure.). Ra may be set to either 20K or 40K ohms,

depending on selected gain. Rb may be set between 20K and 1000K ohms, to generate the possible gain values selectable in either the Configure dialog or the SetGain function.

Figure 2 PGA_Inv Schematic



The block has a programmable capacitor in parallel with the feedback resistor, Rb. The capacitor value is configured for each gain selection to achieve guaranteed stability. Reassigning Rb values without also selecting the appropriate feedback capacitor value may result in PGA_Inv instability. You are strongly advised to use the provided APIs for gain changes.

The input resistance of the PGA_Inv is finite. The gain accuracy is dependent on the routing resistance between the source and the Vin input. The gain specifications accommodate the nominal variation in the routing resistance.

Registers

The PGA_Inv component configuration is implemented in registers SC[0..3]_CR0, SC[0..3]_CR1 and SC[0..3]_CR2. These can be accessed in user code by reference to the instantiated component name, e.g., PGA_Inv_1_CR0_REG. The register contents can be reviewed in the PSoC Creator component debug window. Refer to the applicable TRM, available on the Cypress web site, for a detailed description of each register. The following registers are displayed in the PGA component debug window.

Register:	PGA_Inv_1_CR0_REG
Name:	Switched Capacitor Control Register 0
Description:	Register bits 3:1 configure the switch capacitor block operating mode. This field is set to 110b for the PGA component.
Register:	PGA_Inv_1_CR1_REG
Name:	Switched Capacitor Control Register 1
Description:	Register fields configure drive mode, compensation capacitor values, and gain setting of the switch capacitor block.

Register: PGA_Inv_1_CR2_REG

Name: Switched Capacitor Control Register 2

Description: Register fields configure the input impedance, feedback impedance and the reference ground selection for the switch capacitor block.

Register: PGA_Inv_1_PM_ACT_CFG_REG

Name: Active Power Mode Configuration Register 9

Description: Register bits 3:0 enable power to the four switch capacitor blocks.

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the tables below, all T_A = 25° C, V_{dd} = 5.0 V, Power HIGH, opamp bias LOW, output referenced to Analog Ground = V_{ssa} .

5.0V/3.3V DC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
Input						
Vos	Input Offset Voltage	Vdda=3.3 V, 25 C, P=Min	na	tbc	tbc	mV
		Vdda=3.3 V, 25 C, P=Low	na	tbc	tbc	mV
		Vdda=3.3 V, 25 C, P=Med	na	tbc	tbc	mV
		Vdda=3.3 V, 25 C, P=High	na	tbc	tbc	mV
TCVos	Temp Coeff Input Offset Voltage	P=Min (Absolute value)	na	tbc	tbc	uV/deg C
		P=Low (Absolute value)	na	tbc	tbc	uV/deg C
		P=Med (Absolute value)	na	tbc	tbc	uV/deg C
		P=High (Absolute value)	na	tbc	tbc	uV/deg C

Parameter	Description	Conditions	Min	Typ	Max	Units
Rin	Input resistance	Gain = -1	na	20	na	k ohms
Cin	Input capacitance	Gain = -1, routing dependent	na	tbc	tbc	pF
Ge_1	Gain accuracy, deviation from nominal	G=-1, Vdda=5.0 V, P=High, Vref connected to Vdda/2	na	tbc	tbc	%
Ge_15		G=-15, Vdda=5.0 V, P=High, Vref connected to Vdda/2	na	tbc	tbc	%
Ge_49		G=-49, Vdda=5.0 V, P=High, Vref connected to Vdda/2	na	tbc	tbc	%
Gain Drift	Gain change vs temp					ppm/deg C
Gd_1			na	tbc	tbc	
Gd_15			na	tbc	tbc	
Gd_49			na	tbc	tbc	
Ge_ref_ext	Gain routing dependency, ref	Gain = -15, Vin connected to internally routed buffer (add PGA)	tbc	tbc	tbc	%
Ge_ref_pin	Gain routing dependency, pin	Gain = -15, Vin connected to pin	tbc	tbc	tbc	%
Output swing		Gain = -1, Rload = 100k to Vdda/2	tbc	tbc	tbc	
PSRR	Power supply rejection ratio	Gain=1	tbc	tbc		dB
Idda	Operating current	Vdda=1.71 V, P=Min		tbc	tbc	uA
		Vdda=5.0 V, P=High		tbc	tbc	

Figures

Histogram offset voltage 100 parts, 4 per part X axis mV Y axis % in bins	Voffset vs temperature, Vdda=5.0V X axis: temp -40 to 85 C Y axis Voffset 1 max 2 typ 3 min
Gain deviation, 25C, Vdda=3.3V, P=med X axis Gain steps= 1,2,4,8,16,24,32,48,50 Y axis Diff from nominal, % 1 mean+3sigma 2 mean 3 mean -3sigma	Gain deviation vs Temp, Vdda=5.0V, P=high X axis temp -40 to 85 C Y axis mean % deviation from nominal 1 G=-1 2 G=-3 3 G=-7 4 G=-15 5 G=-24 6 G=-31 7 G=-47
Gain deviation vs Temp, Vdda=5.0V, P=high X axis temp -40 to 85 C Y axis max |%| deviation from nominal 1 G=-1 2 G=-3 3 G=-7 4 G=-15 5 G=-24	Gain deviation vs Temp, Vdda=5.0V, P=high X axis temp -40 to 85 C Y axis |%| deviation from nominal 1 G=-31 2 G=-47 3 G=-49
Operating current vs voltage, P=min X axis Vdda, 1.7, 2.7, 3.3, 5.0 Y axis Op current uA 1 max at worst temp 2 typ at 25C	Operating current vs voltage, P=low X axis Vdda, 1.7, 2.7, 3.3, 5.0 Y axis Op current uA 1 max at worst temp 2 typ at 25C
Operating current vs voltage, P=med X axis Vdda, 1.7, 2.7, 3.3, 5.0 Y axis Op current uA 1 max at worst temp 2 typ at 25C	Operating current vs voltage, P=high X axis Vdda, 1.7, 2.7, 3.3, 5.0 Y axis Op current uA 1 max at worst temp 2 typ at 25C
Operating current vs temp, P=min X axis Temp, -40 to +85C Y axis op current uA 1 Typ at 2.7V 2 Max at 2.7V 3 Typ at 5.5V 4 Max at 5.5V	Operating current vs temp, P=low X axis Temp, -40 to +85C Y axis op current uA 1 Typ at 2.7V 2 Max at 2.7V 3 Typ at 5.5V 4 Max at 5.5V

Operating current vs temp, P=med X axis Temp, -40 to +85C Y axis op current uA 1 Typ at 2.7V 2 Max at 2.7V 3 Typ at 5.5V 4 Max at 5.5V	Operating current vs temp, P=high X axis Temp, -40 to +85C Y axis op current uA 1 Typ at 2.7V 2 Max at 2.7V 3 Typ at 5.5V 4 Max at 5.5V
Output voltage vs load current, Vdda=2.7V, P=min X axis output current uA Y axis output voltage 1 Voh at -40 2 Voh at 25 3 Voh at 85 4 Vol at -40 5 Vol at 25 6 Vol at 85	Output voltage vs load current, Vdda=2.7V, P=low X axis output current uA Y axis output voltage 1 Voh at -40 2 Voh at 25 3 Voh at 85 4 Vol at -40 5 Vol at 25 6 Vol at 85
Output voltage vs load current, Vdda=2.7V, P=med X axis output current uA Y axis output voltage 1 Voh at -40 2 Voh at 25 3 Voh at 85 4 Vol at -40 5 Vol at 25 6 Vol at 85	Output voltage vs load current, Vdda=2.7V, P=high X axis output current uA Y axis output voltage 1 Voh at -40 2 Voh at 25 3 Voh at 85 4 Vol at -40 5 Vol at 25 6 Vol at 85
Output voltage vs load current, Vdda=5.0V, P=min X axis output current uA Y axis output voltage 1 Voh at -40 2 Voh at 25 3 Voh at 85 4 Vol at -40 5 Vol at 25 6 Vol at 85	Output voltage vs load current, Vdda=5.0V, P=low X axis output current uA Y axis output voltage 1 Voh at -40 2 Voh at 25 3 Voh at 85 4 Vol at -40 5 Vol at 25 6 Vol at 85

Output voltage vs load current, Vdda=5.0V, P=med X axis output current uA Y axis output voltage 1 Voh at -40 2 Voh at 25 3 Voh at 85 4 Vol at -40 5 Vol at 25 6 Vol at 85	Output voltage vs load current, Vdda=5.0V, P=high X axis output current uA Y axis output voltage 1 Voh at -40 2 Voh at 25 3 Voh at 85 4 Vol at -40 5 Vol at 25 6 Vol at 85

5.0V/3.3V AC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
Gain Bandwidth			tbc	tbc		MHz
GBW_L	Gain Bandidth Product, P=Low	Gain=-1, Vdda=1.71 V, 25 C, P=Low	tbc	tbc	na	
GBW_H	Gain Bandwidth Product, P=High	Gain=-1, Vdda=5.0 V, 25 C, P=High	tbc	tbc	na	
SR_Pmin	Slew Rate	20 - 80%, Gain=1, P=Min	tbc	tbc	na	V/uS
SR_Plow	Slew Rate	20 - 80%, Gain=1, P=Low	tbc	tbc	na	V/uS
SR_PMed	Slew Rate	20 - 80%, Gain=1, P=Med	tbc	tbc	na	V/uS
SR+PHigh	Slew Rate	20 - 80%, Gain=1, P=HIgh	tbc	tbc	na	V/uS
Tsettle_Pmin	Settling time to	1.0 V step to 0.1%, CLoad= 15 pF Vdda= 5.0 V, G=-1, P=Min	na	tbc	tbc	nsec
Tsettle_Plow		1.0 V step to 0.1%, CLoad= 15 pF Vdda= 5.0 V, G=-1, P=Low	na	tbc	tbc	nsec
Tsettle_Pmed		1.0 V step to 0.1%, CLoad= 15 pF Vdda= 5.0 V, G=-1, P=Med	na	tbc	tbc	nsec
Tsettle_Phigh		1.0 V step to 0.1%, CLoad= 15 pF Vdda= 5.0 V, G=-1, P=High	na	tbc	tbc	nsec
Vn_Pmin	Noise	f=10 kHz, P=Min	na	tbc	na	nV/rtHz

Parameter	Description	Conditions	Min	Typ	Max	Units
Vn_Plow		f=10 kHz, P=Low	na	tbc	na	nV/rtHz
Vn_Pmed		f=10 kHz, P=Med	na	tbc	na	nV/rtHz
Vn_Phigh		f=10 kHz, P=High	na	tbc	na	nV/rtHz

Figures

Typical Gain vs freq, 3.3V, P=min X axis 10 kHz to 10 MHz Y axis Gain, dB 1 G=-1 2 G=-3 3 G=-7 4 G=-15 5 G=-24 6 G=-31 7 G=-47	Typical Gain vs freq, 3.3V, P=low X axis 10 kHz to 10 MHz Y axis Gain, dB 1 G=-1 2 G=-3 3 G=-7 4 G=-15 5 G=-24 6 G=-31 7 G=-47
Typical Gain vs freq, 3.3V, P=med X axis 10 kHz to 10 MHz Y axis Gain, dB 1 G=-1 2 G=-3 3 G=-7 4 G=-15 5 G=-24 6 G=-31 7 G=-47	Typical Gain vs freq, 3.3V, P=high X axis 10 kHz to 10 MHz Y axis Gain, dB 1 G=-1 2 G=-3 3 G=-7 4 G=-15 5 G=-24 6 G=-31 7 G=-47
Gain deviation vs freq, Vdda=2.7V, P=low G=50, Difference from nominal X axis 10 kHz to 10 MHz Y axis Gain error (dB or %, tbd) 1 Min at -40 2 Mean at -40 3 Max at -40 4 Min at 85 5 Mean at 85 6 Max at 85	Gain deviation vs freq, Vdda=2.7V, P=high G=50, Difference from nominal X axis 10 kHz to 10 MHz Y axis Gain error (dB or %, tbd) 1 Min at -40 2 Mean at -40 3 Max at -40 4 Min at 85 5 Mean at 85 6 Max at 85

Gain deviation vs freq, Vdda=5V, P=low G=50, Difference from nominal X axis 10 kHz to 10 MHz Y axis Gain error (dB or %, tbd) 1 Min at -40 2 Mean at -40 3 Max at -40 4 Min at 85 5 Mean at 85 6 Max at 85	Gain deviation vs freq, Vdda=5V, P=high G=50, Difference from nominal X axis 10 kHz to 10 MHz Y axis Gain error (dB or %, tbd) 1 Min at -40 2 Mean at -40 3 Max at -40 4 Min at 85 5 Mean at 85 6 Max at 85
-3dB BW (Typ, max) vs Vdda X axis Vdda 1,7, 2.7, 3.3, 5.0 Y axis BW kHz 1 P=min, typ 2 P=min, min 3 P=low, typ 4 P=low, min 5 P=med, typ 6 P=med, min 7 P=high, typ 8 P=high, min	
-3dB BW (Typ) vs Temp, P=min X axis Temp deg C Y axis -3dB BW kHz 1 G=-1 2 G=-3 3 G=-7 4 G=-15 5 G=-24 6 G=-31 7 G=-47	-3dB BW (Typ) vs Temp, P=low X axis Temp deg C Y axis -3dB BW kHz 1 G=-1 2 G=-3 3 G=-7 4 G=-15 5 G=-24 6 G=-31 7 G=-47
-3dB BW (Typ) vs Temp, P=med X axis Temp deg C Y axis -3dB BW kHz 1 G=-1 2 G=-3 3 G=-7 4 G=-15 5 G=-24 6 G=-31 7 G=-47	-3dB BW (Typ) vs Temp, P=high X axis Temp deg C Y axis -3dB BW kHz 1 G=-1 2 G=-3 3 G=-7 4 G=-15 5 G=-24 6 G=-31 7 G=-47
Voltage noise, Vdda = 5.0V, P=high Xaxis freq kHz .01 to 1000 kHz Yaxis voltage noise nV/rtHz	PSRR vs freq, Vdda = 5.0V, P=high X axis freq 100 Hz to 1.0 MHz Y axis dB

Note More specifications at other voltages and graphs may be added after characterization.

Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
1.50.b	Minor datasheet edit.	
1.50.a	Minor datasheet edit.	
1.50	Added Sleep/Wakeup and Init/Enable APIs.	To support low power modes, as well as to provide common interfaces to separate control of initialization and enabling of most components.
	Removed Gain setting of 23.	The gain of 23 was too close to 22 and 24 and therefore offered no value.
	Updated the symbol and Configure dialog.	These were updated to comply with corporate standards.

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