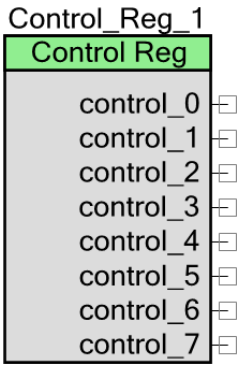
Control Register

1.80



Features

- Up to 8-bit Control Register

General Description

The Control Register allows the firmware to output digital signals.

When to Use a Control Register

Use a Control Register when the firmware needs to interact with a digital system. You can also use the Control Register as a configuration register, allowing the firmware to specify the desired behavior of the digital system.

Input/Output Connections

This section describes the input and output connections for the Control Register. An asterisk (*) indicates that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

clock – Input *

This optional pin is present if the **Mode** parameter is set to **SyncMode** or **PulseMode**. Otherwise, the clock input does not show.

reset – Input *

This optional input is used to reset Control Register bits. This input is shown on the symbol when you enable the **External reset** parameter, and set the **Mode** parameter to **SyncMode** or **PulseMode**. The reset input may be left floating with no external connection. If nothing is connected to the reset line, the component will assign it a constant logic 0.

control_0 - control_7 – Output *

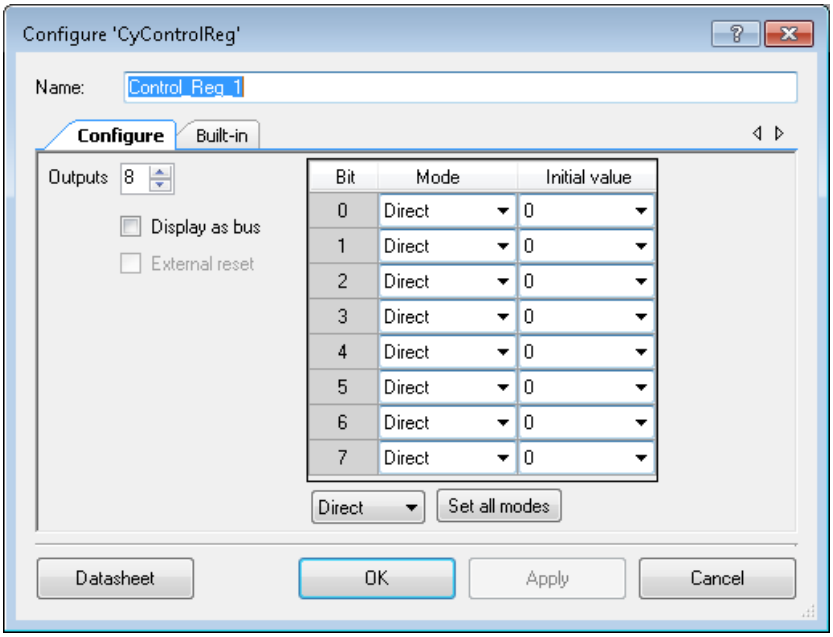
The Control Register contains up to eight outputs. The firmware sets the values of the output terminals by writing to the Control Register. The number of outputs depends on the setting for the **Outputs** parameter.

control[N:0] – Output *

This optional output sweeps the individual output terminals into a single bus terminal. This pin is visible when **Display as bus** parameter is enabled. N is the number of outputs - 1.

Component Parameters

Drag a control register onto your design and double-click it to open the Configure dialog.



Outputs

Number of output terminals (1 to 8). The default value is **8**. Bit0 is the LSB and corresponds to the control_0 terminal.

Display as bus

This parameter displays the outputs as a bus instead of individual terminals. This option is unchecked by default.

External reset

This check box is used to enable the reset input on the symbol. This option is unchecked by default. **External reset** is not valid when all the bits in the **Mode** parameter are configured as **DirectMode**. In this case this option is disabled.

Set all modes

This button sets all bits to **DirectMode**, **SyncMode** or **PulseMode**, depending on the mode selected in the combo box in the left hand side of this button.

Mode

These parameters are used to set specific bits of the Control Register to one of three settings:

- **DirectMode –** In this mode, when the control register is written with bus clock, the data is driven directly into the routing.
- **SyncMode –** Resamples (single-synched) the control bit input from the bus clock to the selected SC clock before it is driven into the routing.
- **PulseMode –** This mode is similar to SyncMode, in that the Control bit input is resampled from the bus clock to the selected SC clock and a single SC clock period pulse is generated. The output of the control bit into the routing is asserted for one full SC clock period. At the end of the pulse, the control bit is automatically reset.

Initial value

These parameters allow to set the default value of 0 or 1 for each bit in the Control Register. By default, the initial value is 0.

Low Power Mode Behavior

None of the Control Register content is retained during low power modes (sleep, deep sleep, and hibernate). The low power API functions are optional. If not used, the value in the each bit of the Control Register component is initialized with a ‘0’ value when the device wakes up from low power mode.

Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software. The following table lists and describes the interface to each function. The subsequent sections cover each function in more detail.

By default, PSoC Creator assigns the instance name “Control_Reg_1” to the first instance of a control register in any given design. You can rename the component to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following tables is “Control_Reg.”

Functions

Function	Description
Control_Reg_Write()	Writes a byte to a control register
Control_Reg_Read()	Reads the current value assigned to a control register
Control_Reg_SaveConfig()	Saves the control register value
Control_Reg_RestoreConfig()	Restores the control register value
Control_Reg_Sleep()	Prepares the component for entering the low power mode
Control_Reg_Wakeup()	Restores the component after waking up from the low power mode

void Control_Reg_Write (uint8 control)

Description: Writes a byte to the control register

Parameters: control: The value to be assigned to the control register

Side Effects: Sets the state of the control register’s outputs

uint8 Control_Reg_Read (void)

Description: Reads the current value assigned to the control register

Return Value: Returns the current value assigned to the control register

void Control_Reg_SaveConfig (void)

Description: Saves the control register value

Side Effects: Sets the state of the control register’s outputs

void Control_Reg_RestoreConfig (void)

Description: Restores the control register value

void Control_Reg_Sleep (void)

Description: Prepares the component for entering the low power mode

void Control_Reg_Wakeup (void)

Description: Restores the component after waking up from the low power mode

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined:

- project deviations – deviations that are applicable for all PSoC Creator components
- specific deviations – deviations that are applicable only for this component

This section provides information on component-specific deviations. Non PSoC 6 project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment. For PSoC 6, refer to PSoC Creator Help > Building a PSoC Creator Project > Generated Files (PSoC 6) for information on MISRA compliance and deviations for files generated by PSoC Creator.

The Control Register component does not have any specific deviations.

Sample Firmware Source Code

PSoC Creator provides numerous code examples that include schematics and example code in the Find Code Example dialog. For component-specific examples, open the dialog from the Component Catalog or an instance of the component in a schematic. For general examples, open the dialog from the Start Page or **File** menu. As needed, use the **Filter Options** in the dialog to narrow the list of projects available to select.

Refer to the “Find Code Example” topic in the PSoC Creator Help for more information.

API Memory Usage

The component memory usage varies significantly, depending on the compiler, device, number of APIs used and component configuration. The following table provides the memory usage for all APIs available in the given component configuration.

The measurements have been done with the associated compiler configured in Release mode with optimization set for Size. For a specific design the map file generated by the compiler can be analyzed to determine the memory usage.

Configuration	PSoC 3 (Keil_PK51)		PSoC 4 (GCC)		PSoC 5LP (GCC)		PSoC 6 (GCC)	
	Flash (Bytes)	RAM (Bytes)	Flash (Bytes)	RAM (Bytes)	Flash (Bytes)	RAM (Bytes)	Flash (Bytes)	RAM (Bytes)
Default	38	1	80	1	72	1	80	1

Resources

The Control Register component uses one control cell in the UDB array.

DMA

The DMA component can be used to write data directly from RAM to the Control Register. The DMA Wizard can be used to configure DMA operations as follows:

Name of DMA Source/Destination in DMA Wizard	Direction	DMA Req Signal	DMA Req Type	Description
Control_Reg_Control_PTR	Destination	N/A	N/A	Stores Control Register value.

Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
1.80.b	Updated MISRA section. Updated API Memory section. Added PSoC 6 support.	
1.80.a	Corrected API instance names.	Component datasheet improvement.
1.80	Added Low power management APIs	Component improvement
	Updated the datasheet.	Updated Application Programming Interface section. Updated API Memory Usage section. Updated Low Power Mode Behavior section.
1.70.c	Updated the datasheet.	Added low power mode behavior section.
	Updated the table appearance in the Configure dialog.	Corrected a display problem at 120 dpi resolution.
1.70.b	Updated datasheet with memory usage for PSoC 4.	
1.70.a	Added MISRA Compliance section.	The component does not have any specific deviations.
1.70	Added support for PSoC 5LP silicon.	
	Updated the Configure dialog.	Added Display as bus option; Set all modes button and minor design changes.
	Added display as bus option for output terminals.	To have output terminals as bus
	Added the Sync Mode support for PSoC 5LP silicon and implemented DMA capabilities and Debug window support.	PSoC 5LP silicon supports Sync mode.
1.60	Updated the Configure dialog	Changed the Bit display and addressed minor Configure dialog issues
1.50.b	Minor datasheet edits and updates	
1.50.a	Minor datasheet edits and updates	
1.50	Updated the Configure dialog.	Created a customized interface. Added "Set All" and “Clear All” buttons and changed Number of Inputs field to allow keyboard entry. Updated the dialog to comply with corporate standards.
	Added reset input and ExternalReset parameter to control visibility of reset input	This was added for PSoC 3 Production silicon to control the reset behavior of the control register
	Added BitValue parameter	To set control register Initial Value.

Version	Description of Changes	Reason for Changes / Impact
	Added Bit mode parameter to pick different control register modes (Direct, Sync and Pulse Mode).	New modes (Sync, Pulse Mode) were added to give the possibility to select a mode that resamples necessary Control Register bits to the UDB clock. This new mode can be used for PSoC 3 Production or later.
	Added Clock pin	Clock pin was added to support Sync and Pulse Mode which is exposed only when these modes are selected.

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