

Maximize advantages in hard and soft-switching applications with optimal use of a modern SiC MOSFET with low output capacitance

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Abstract

Silicon carbide (SiC) MOSFETs have superior properties at high voltage and high power compared to silicon (Si) devices in almost all aspects due to their material advantages such as three times larger band gap, three times larger thermal conductivity, ten times higher critical electric field, two times higher saturation velocity and so on. SiC MOSFETs can thus significantly improve the performance of the system. In addition to the well-known advantages of SiC MOSFETs over Si MOSFETs and IGBTs, a deeper understanding and right usage of SiC MOSFETs can help enhance device performance and maximize system value propositions. In this paper, a parameters-oriented approach is proposed to select the right SiC MOSFET device corresponding to the requirements of each application. The proposed approach has been validated by PLECS simulation results of representative hard and soft switching applications.

Introduction

Silicon carbide (SiC) devices are increasingly being adopted in power electronic applications as they provide significant advantages over silicon (Si) devices. For example, higher system efficiency, superior device performance, smaller system form factors, and faster switching frequency. Conventional approaches for selecting a SiC MOSFET for target applications focus mainly on the typical $R_{DS(on)}$ value. In some cases, total switching losses are also considered in the

selection process, especially in case of hard-switching applications. There are, however, other parameters that are often neglected in the design process. These parameters can significantly improve device performances when applied properly. This paper analyzes in detail the impact of dead time and the output capacitance of the SiC MOSFET (C_{oss}).

Figure 1 is a graph comparing the C_{oss} of Infineon's recently released 1200 V 26 mΩ CoolSiC™ SiC MOSFET second generation (G2) and its predecessor (30 mΩ CoolSiC™ SiC MOSFET G1) with the latest products in the market in the similar $R_{DS(on)}$ range. As not all manufacturers provide the energy-related C_{oss} , $C_{o(er)}$, and the time-related C_{oss} , $C_{o(tr)}$, values that require raw data for calculation in the data sheet, an accurate numerical comparison is unfortunately not available. However, from the graph it is obvious that the $C_{o(er)}$ and $C_{o(tr)}$ values of Infineon's SiC MOSFET G2 are significantly smaller. This is possible due to Infineon's highly advanced gate trench SiC MOSFET technology [1, 2].

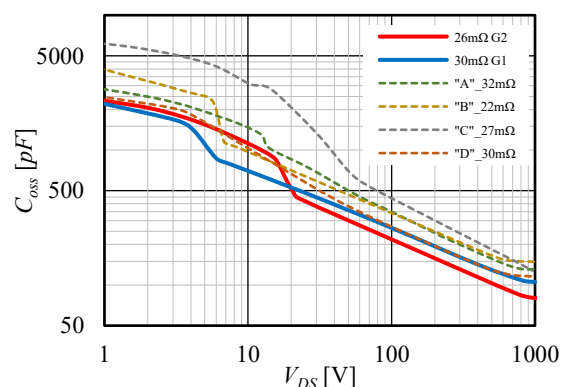


Fig. 1: Comparison of C_{oss} values between 1200 V SiC MOSFETs

The most common structure in which SiC

MOSFETs are used, regardless of a hard or soft-switching application, is the one-bridge leg structure shown in Figure 2. It consists of high and low-side arms. In a one-bridge leg structure, the dead time is essential to prevent the device from failing due to a shoot-through current during the transition of each switch. However, in both hard and soft-switching applications with SiC MOSFETs a longer than necessary dead time can cause unwanted losses and inhibit system efficiency. System efficiency can be maximized by applying an appropriate dead time.

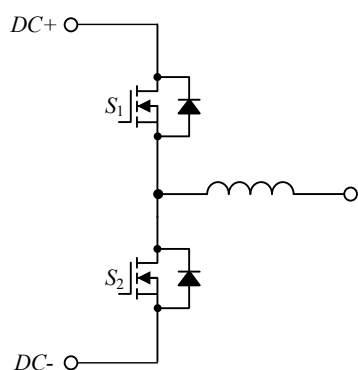


Fig. 2: A one-bridge leg with a SiC MOSFET

In soft-switching applications, choosing a SiC MOSFET with the lowest time-related output capacitance, $C_{o(tr)}$, at a working voltage from equivalent R_{DSon} class gives system designers room to lower the magnetizing current [8 – 11]. This can improve system efficiency, especially in LLC resonant converter applications. An analysis of the efficiency characteristics of hard-switching applications based on the dead time, the effect of the SiC MOSFET's C_{oss} on the design of a soft-switching LLC converter, and the resulting efficiency characteristics are presented in this paper. Simulations were conducted on a 3-phase B6 power factor correction (PFC) converter – a representative hard-switching application and an LLC converter – the most representative soft-switching application, to verify the improvement in system performance when optimal dead time is used.

Effects of dead time on a SiC MOSFET in the hard commutation mode

SiC MOSFETs enable the implementation of systems with high efficiency and high-power density at a higher level than IGBTs. In the one-bridge leg structure shown in Figure 2, in which a pair of switches alternately turn on and

turn off, the dead time must be applied between the intervals of each switch to prevent the device from getting destroyed by the shoot-through current. In many hard-switching applications, the body diode of the SiC MOSFET conducts a freewheeling current for the remaining dead time period after the switching time ends.

The effect of dead time on the turn-off behavior of the SiC MOSFET's body diode in a bridge leg with current has been studied by many researchers [2 – 7]. When the body diode starts conducting current, it gradually accumulates plasma until an equilibrium between carrier generation and recombination is achieved. The diode voltage is initially high but it decreases to a steady state value as the plasma concentration increases. If the dead time set is very short the plasma in the drift region, at the instant when the body diode is turned off, cannot be fully constructed by the opposite SiC MOSFET that turns on. In such a scenario, the amount of charge that is discharged from the drift region is lesser than that in the case of a longer dead time. The reverse recovery current of the body diode consequently reduces leading to a lower recovery energy, E_{rr} .

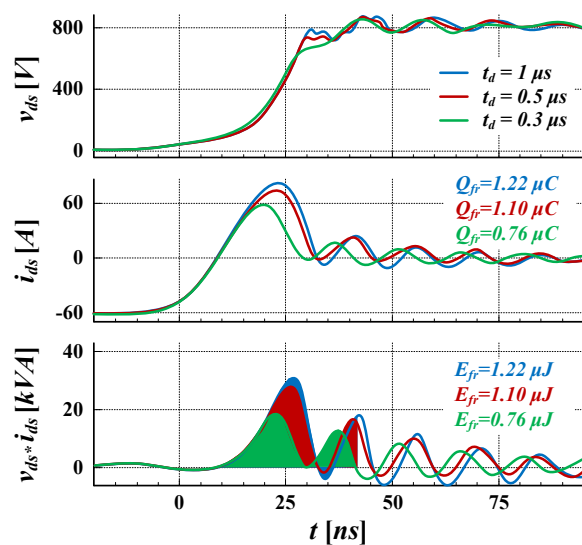


Fig. 3: Behavioral turn-off waveforms of a SiC MOSFET's body diode for different dead times at 175°C

On the other hand, when the bridge leg operates in the commutation mode, the reverse recovery loss of the SiC MOSFET's body diode is added to the turn-on energy, E_{on} , of the opposite switch. In Figure 3, the impact of different dead times is illustrated. Compared to 1 μ s, a significant reduction in reverse recovery charge can be observed for a dead time of 300 ns, and a smaller

value can be obtained by applying a smaller dead time. Meanwhile, the plasma concentration in the drift region saturates somewhere between 500 ns and 1 μs. At a dead time ≥ 1 μs, no difference is observed in the reverse recovery behavior.

Due to the reduced plasma concentration, a short dead time can significantly reduce the recovery losses, overvoltage, and associated oscillation behavior. System performance can be maximized by minimizing the dead time, but there are practical limitations on how much it can be reduced in a typical application.

Selecting the optimum dead time in hard-switching applications

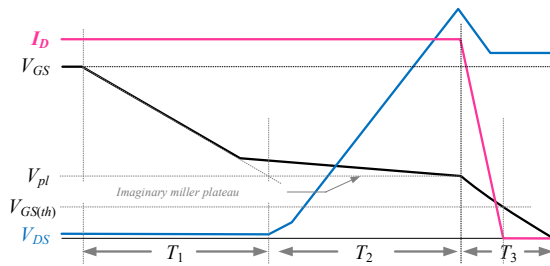


Fig. 4: Turn off behavior of a SiC MOSFET

In hard-switching applications, the dead time relies highly on the device's switching behavior. The simplest approach for predicting the switching speed of a power semiconductor device is to consider the total gate charge, Q_g , of the device. This is because when the gate voltage reaches the driving voltage level completely, it has been observed that the turn-on process of the device is complete. Conversely, when the gate voltage reaches 0, it means that the device's turn-off process is complete.

The theoretical switching turn-off waveform of a SiC MOSFET is shown in Figure 4. As shown in the figure, the switching turn-off transition is complete when $V_{gs}(t)$ reaches the threshold voltage, $V_{gs,th}$, level. Therefore, the minimum dead time can be obtained by:

$$DT_{min} \geq k_{at}(T_1 + T_2 + T_3) \quad (1)$$

Where,

$$T_1 \geq R_{G,tot} \cdot C_{iss} \cdot \ln\left(\frac{V_{GS}}{V_{pl}}\right) \quad (2)$$

$$T_2 \geq R_{G,tot} \cdot C_{rss} \left(\frac{V_{DD}}{V_{pl}}\right) \quad (3)$$

and,

$$T_3 \geq R_{G,tot} \cdot C_{iss} \cdot \ln\left(\frac{V_{pl}}{V_{th,low}}\right) \quad (4)$$

Here k_{at} is an additional time margin constant considering the propagation delay of the gate driver IC and the parameter distribution of the SiC MOSFET. A value between 1.5 and 2 is appropriate in most of the cases. Meanwhile, to avoid additional time delay by a limited driving current, the output current capability, I_{Go} , of a driver IC should be:

$$I_{Go,min} \geq \frac{V_{GS}}{R_{g,tot}} \quad (5)$$

Overall, the dead time in real systems can be shorter than what is currently applied. To ensure proper system reliability, the minimum dead time must be confirmed by measuring the switching behavior in the target application.

Simulating the effect of dead time in hard-switching applications

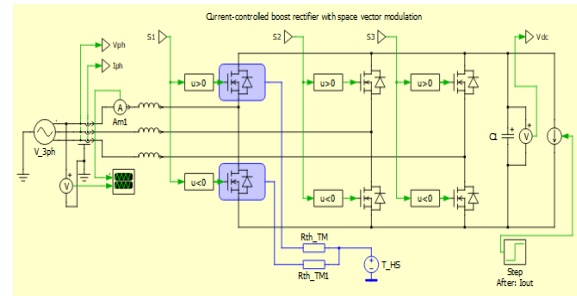


Fig. 5: PLECS simulation diagram for a 2-level, 3-phase B6 PFC

To verify the validity of the effect of dead time in hard-switching applications, a simulation of a 3-phase, 2-level PFC stage was carried out using the PLECS software. The schematic of the simulation is shown in Figure 5.

Simulations were performed using the following parameters values:

- MOSFET: IMZC120R026M2H
- AC input voltage, V_{ac} : 380 V
- DC output voltage, V_{OUT} : 800 V
- Maximum output power, $P_{o,max}$: 22 kW
- AC input frequency, f_{ac} : 50 Hz
- Switching frequency, f_{sw} : 60 kHz
- Gate resistance, R_g : 3 Ω
- Inductance, L : 300 μH
- Dead time, DT : 75/100/250/500 ns

Where, AC stands for alternative current, and DC for direct current.

Figure 6 shows a comparison between the system efficiency results in accordance with the output power of the system shown in Figure 5, based on different dead times.

The simulation results clearly show that a lower

dead time results in better system performance. With a dead time of 100 ns, a maximum of 0.15% higher system efficiency is expected for overall operating conditions. This is equivalent to 36 W in a 24 kW system.

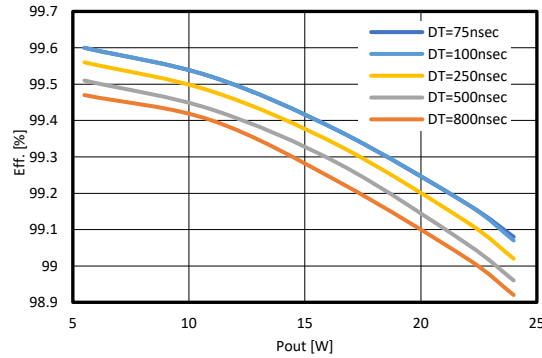


Fig. 6: Efficiency comparison based on different dead times in a B6 converter

Meanwhile, the dead time of 75 ns is negligible in its effectiveness compared to 100 ns and it might also be insufficient when taking typical propagation delays of gate drivers into account. A minimum dead time of 100 ns can, therefore, be considered reasonable.

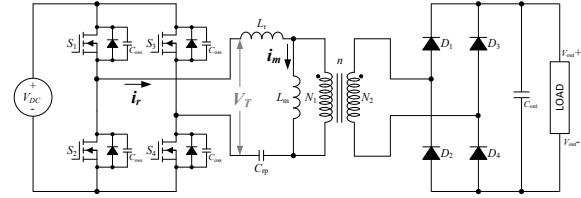
Selecting the optimum SiC MOSFET for soft-switching applications

In soft-switching applications, the turn-on switching losses and body diode's reverse recovery losses are practically negligible. Consequently, the effect of dead time on the system performance is not as significant as in hard-switching applications. Nevertheless, the SiC MOSFET's C_{oss} should still be considered important in system design even in soft switching applications. The effect of this parameter is analyzed in this section, with a focus on an LLC converter topology as the representative topology for soft-switching applications.

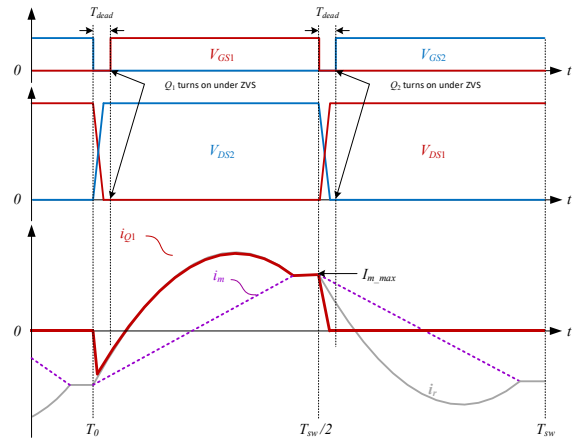
Figure 7 shows a full-bridge LLC converter and its operating waveforms. The dead time for LLC converter topologies depends more on the system parameters, especially magnetizing inductance of the transformer, than on the intrinsic device parameters.

In an LLC converter, a zero-voltage switching (ZVS) turn-on is achieved by the reverse conduction mode during dead time. However, the voltage drop, V_{SD} , across the SiC MOSFET's body diode (usually greater than 4 V) is significantly higher than the voltage drop

associated with R_{Dson} . Therefore, it is beneficial to minimize the conduction time of the body diode as much as possible by selecting the minimum possible dead time. This minimizes any extra conduction loss during the freewheeling modes.



(a) Circuit diagram



(b) Operating waveforms

Fig. 7: Circuit diagram and the operating waveforms of a full-bridge LLC converter topology

On the other hand, the charging and discharging time of a SiC MOSFET's output capacitance in an LLC converter depends largely on the magnetizing current level at device turn-off, which is largely determined by the magnetizing inductance, L_m , of the transformer. The energy stored in L_m must be larger than the energy stored in the device's total output capacitance, C_{oss} , to achieve the ZVS condition before the other switch turns on. This is defined in the following equation:

$$\frac{1}{2} L_m * I_{m,pk}^2 \geq \frac{1}{2} C_{o(tr)} * V_{DC}^2 \quad (5)$$

Where, $C_{o(tr)}$ is the time-related output capacitance, which is calculated by:

$$C_{o(tr)} = \frac{1}{V_{DC}} \int_0^{V_{DC}} C_{oss}(v) dv \quad (6)$$

and $I_{m,pk}$ is calculated by:

$$I_{m,pk} = \frac{V_T * t_{sw}}{4L_m} \quad (7)$$

Additionally, when either the high-side or the low-side SiC MOSFET turns off, two $C_{o(tr)}$ are charged and discharged at the same time by $I_{m,pk}$. Thus, the required minimum dead time can be:

$$t_{dead} \geq \frac{2C_{o(tr)} * V_{DC}}{I_{m,pk}} \quad (8)$$

The LLC converter is controlled by pulse-frequency modulation (PFM) and $I_{m,pk}$ varies in accordance with the switching frequency. Consequently, the required dead time for the LLC converter has to be a function of the switching frequency. From Equations 7, and 8, the dead time for a half-bridge and a full-bridge LLC converter can be derived using the following equations, respectively:

$$t_{dead_HB} \geq 16 * C_{o(tr)} * L_m * f_{sw,max} \quad (9)$$

$$t_{dead_FB} \geq 8 * C_{o(tr)} * L_m * f_{sw,max} \quad (10)$$

Where the voltage applied to the primary side of the transformer, V_T , is equal to V_{DC} for full-bridge and $V_{DC}/2$ for half-bridge respectively. Selecting a SiC MOSFET with low $C_{o(tr)}$ helps in reducing the magnetizing current required for achieving ZVS, as described in Equation 5. A lower magnetizing current of an LLC converter translates in a larger magnetizing inductance value of the transformer. The magnetizing inductance, in turn, greatly affects the input/output gain characteristics of the LLC converter, as shown in Equation 11 and Figure 7. [8 – 14]

$$K(Q, m, F) = \left| \frac{V_{oac}(S)}{V_{inac}(s)} \right| = \frac{F_x^2(m-1)}{\sqrt{(m \cdot F_x^2 - 1)^2 + F_x^2 \cdot (F_x^2 - 1)^2 \cdot (m-1)^2 \cdot Q^2}} \quad (11)$$

Where,

$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac}}, R_{ac} = \frac{8}{\pi^2} \cdot \frac{N_p^2}{N_s^2} \cdot R_o, F_x = \frac{f_s}{f_r}, f_r = \frac{1}{2\pi\sqrt{L_r C_r}}, \text{ and } m = \frac{L_r + L_m}{L_r} \text{ respectively.}$$

Increasing the magnetizing inductance is clearly advantageous in terms of an LLC converter's efficiency due to reduced losses in the transformer. This is particularly advantageous for conventional SMPS applications in which the variation in the input and the output voltage are relatively small. However, if L_m becomes too large, the gain of the LLC converter will decrease and consequently the switching frequency modulation range for output control increases. This degrades the performance of the line and load regulation of the LLC converter.

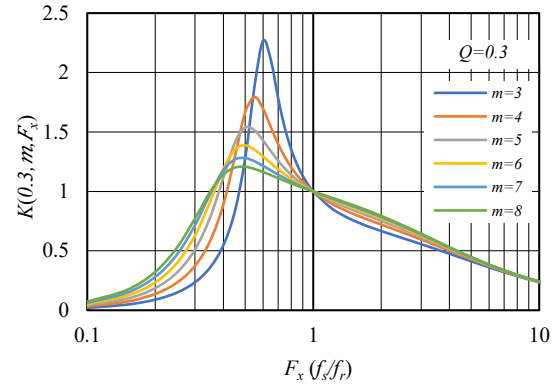


Fig. 8: LLC gain characteristics by m ratio

In applications such as EV chargers, which require large gain values due to the nature of the system, the value of the magnetizing inductance must be limited to reasonable values.

Consequently, a trade-off exists between the optimizing conduction losses of the SiC MOSFET's body diode and minimizing the magnetizing current. System designers have to select the best trade-off on a case-to-case basis. In all the cases though, a small $C_{o(tr)}$ of the SiC MOSFET is beneficial in minimizing the body-diode dead time.

To this end, an important figure of merit (FoM) of the SiC MOSFET is the $R_{DSon} * C_{o(tr)}$ factor. It indicates how small dead time or magnetizing current in LLC converter can be for a given R_{DSon} value. Infineon's new 1200 V CoolSiC™ SiC MOSFET G2 with the best in class $R_{DSon} * C_{o(tr)}$ value gives LLC converter designers additional freedom either to minimize the body-diode conduction time by maintaining the same magnetizing inductance of the transformer, or vice versa, allowing lower magnetizing current of the transformer at the same dead time.

Verifying the validity of small $C_{o(tr)}$ in LLC converters through simulation

Figure 9 shows the PLECS simulation circuit used for verifying the validity of SiC MOSFETs with low $C_{o(tr)}$ parameter in an LLC converter. Simulations were performed using the following parameters:

- MOSFET: IMZC120R026M2H
- Maximum output power, $P_{o,max}$: 20 kW
- Resonant frequency, f_r : 180 kHz
- DC input voltage, V_{IN} : 800 V
- DC output voltage, V_{OUT} : 650 V
- Dead time, DT: 100/250 ns
- Inductance ratio, m value, $(L_m + L_r)/L_r$: 3 – 8

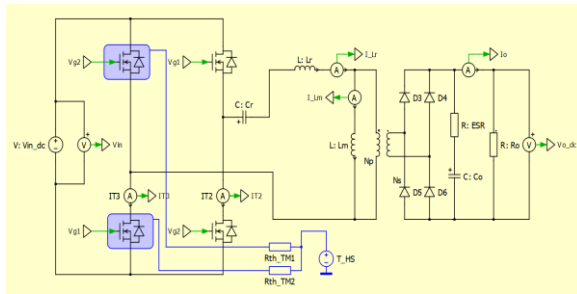


Fig. 9: The PLECS simulation diagram for a full-bridge LLC converter

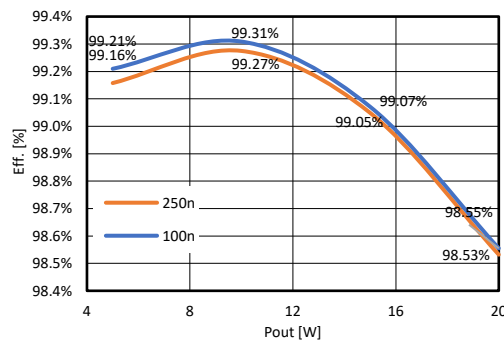


Fig. 10: Comparing efficiency with different dead times in the LLC converter

The dead time of the LLC converter must be shorter than the body-diode freewheeling cycle of SiC MOSFET to implement the ZVS turn-on. There is not much room to set a dead time, especially when the resonance frequency is high. Figure 10 shows a comparison of system efficiency between a dead time of 100 ns and 250 ns. As per the simulation results shown in Figure 10, for a dead time of 100 ns, the system efficiency improves by up to 0.05% at 5 kW P_{out} compared to a dead time of 250 ns.

Meanwhile, increasing the magnetizing inductance lowered the peak transformer magnetizing current and increased the required dead time, resulting in large conduction losses for the body diode. However, the overall losses of the entire circuit is reduced due to the smaller magnetizing current, as the reduction in conduction losses for the entire system overcompensate the increase in body diode's conduction time and loss.

Figure 11 shows the result of an LLC converter's efficiency simulation based on the value of m . It can be clearly seen that as m increases (as a consequence of L_m increase), the efficiency of the LLC converter increases. In particular, it shows that the effect is remarkable at the maximum load at which the magnetizing current reaches its maximum value. In particular, the increase in efficiency at $m = 8$ at maximum load is almost 1%

higher than at $m = 3$. However, the efficiency increment reduces if m is equal to 6 or more. On the other hand, as the switching-frequency modulation range required for the output control of the converter widens, it is important to select an appropriate value of m in terms of load and line regulation.

These results verify that the difference in efficiency characteristics because of m is more dominant than the difference due to dead time in the LLC converter. Therefore, system designers should first select the maximum m value that satisfies the system's input-output control requirements, and then select an optimal dead time based on the magnetizing inductance and the $C_{o(tr)}$ value of the SiC MOSFET. In this way, the efficiency of the LLC converter can be maximized.

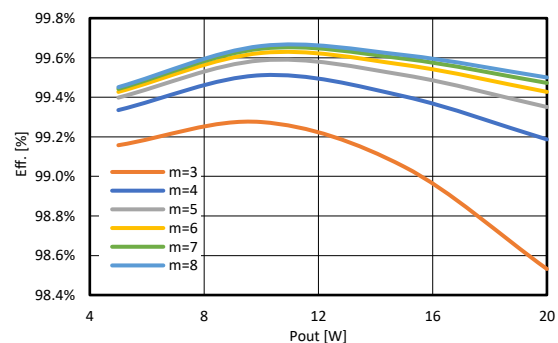


Fig. 11: Comparing efficiency with different m values in the LLC converter

Conclusion

In this paper, several design options that can help maximize system efficiency when designing hard and soft-switching applications were investigated using two SiC MOSFETs parameters that are often not considered while selecting the device. First, it was discussed how setting an optimal dead time is fundamental in reducing the switching losses of a SiC MOSFET when it operates in hard-switching applications. To prove this, a simulation was conducted on a 24 kW B6 converter topology. The simulation results showed that a dead time of 100 ns can improve the system efficiency by about 0.15% over the entire load area compared to a dead time of 800 ns. This was equivalent to a loss of about 34 W in the 24 kW system. Meanwhile, the simulation results for a 20 kW LLC converter showed that the smaller the dead time, the lower the conduction loss of the SiC MOSFET's body diode. This can improve efficiency, especially under light loads.

In soft-switching applications, optimizing the dead time has lesser impact. In the case of an LLC converter it was shown that a more significant increase in efficiency is possible by minimizing the magnetizing current. To lower the magnetizing current while fulfilling the ZVS condition, the $C_{o(tr)}$ of SiC MOSFET must be as small as possible. The results of the simulation with a latest generation of the 1200 V SiC MOSFET, IMZC120R026M2H, proved that the efficiency of the converter can be increased by up to 1% by selecting an optimal m value – $(L_m + L_r)/L_r$.

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