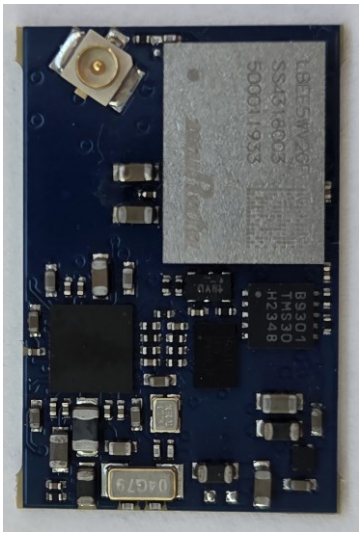
Product_SalesCode: SP006276993
Infineon Industrial Data Connect (IIDC)

Features



- Small SoM Size: (22,9 x 15,5 x 2,5) x mm (L x W x H) x mm
- Ready to use with only 3.3V power supply
- TrustM for Security
- PSOC62 provides
    - 32-bit Dual CPU Subsystem
        - 150MHz Arm6®-Cortex®.M4F (CM4)
        - 100MHz Cortex M0+ (CM0+)
    - Quad-SPI (QSPI)/Serial Memory Interface (SMIF)
    - Audio Subsystem (PDM/PCM)
    - Flexible Clocking Options (32Mhz and 32kHz on Board)
    - Possible of
        - 5x Full Standard SPI or
        - 6x UART
        - 5x I2C
    - USB2 (with 3V power supply)
    - Debug and Tracing capabilitys
- 34 free programmable GPIOs
- Memory Subsystem
    - 2048-KB application flash, 32-KB auxiliary flash (AUXflash), and 32-KB supervisory flash (Sflash); read-while-write (RWW) support. Two 8-KB flash caches, one for each CPU.
- OTA Memory 64Mbit QSPI (SMIF)
- Murata 2GF provides
    - 2,4 / 5 Ghz (Infineon CYW43022, 802.11 a/b/g/n/ac
    - Bluetooth
- U.FL Antenna Connector

Potential applications

- Industrial Internet of Things (IIOT)
- Sensing
- Preprocessing on the Edge with definded Algorithms
- Connectivity library
- Open Source Firmware with secured conenctivity backend and easy Integration and Fleet Management

Product validation
Description

The purpose of this document is to outline the functionality and configuration of the Infineon Industrial Data Connect (IIDC). It offers a brief summary of its various features and instructions for connecting and getting started.

This document is designed for customers who have purchased the IIDC, as well as for solution providers, system integrators, application developers, and product marketers interested in assessing and testing the performance of the Infineon products.

Ordering information

SP006276993. Please contact Infineon IIDC Sales Team.

Table of contents

1 Overview

1.1 Used Main Components on SoM

There you can find an overview image of the used parts of the IIDC on the SoM. The table xx describes the main parts.

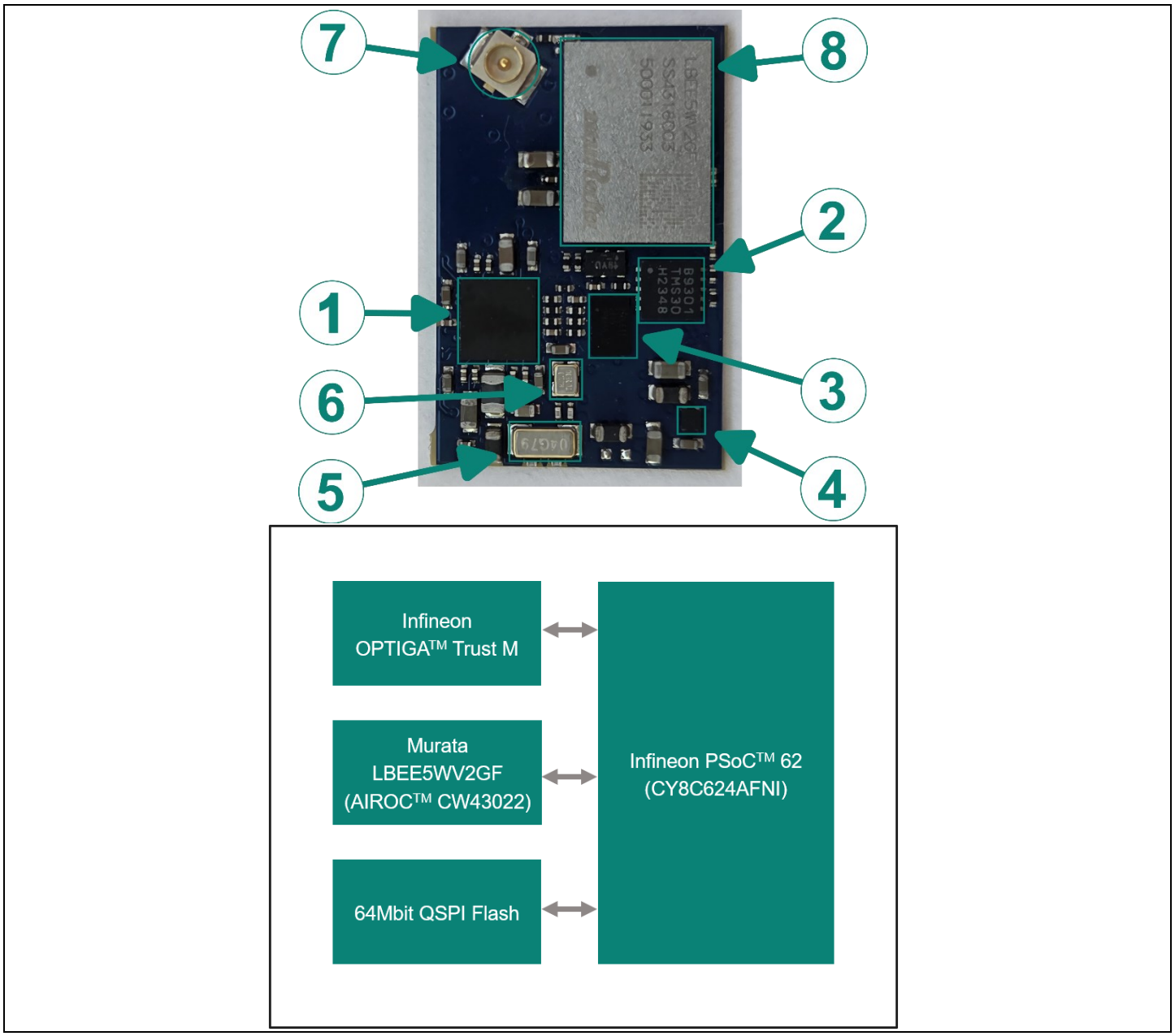


Figure 1

Table 1

Number in figure	Product name	Manufacturer	Function	Description
1	CY8C624AFNI-S2D43T	Infineon	PSoC 62	Main controller

Number in figure	Product name	Manufacturer	Function	Description
2	OPTIGA Trust M SLS_32AIA010ML	Infineon	Security HW Key	
3	64Mbit AT25QL641	Renesas	OTA Memory	
4	NCP115AMX18 0TBG	onSemi	1.8V DCDC	
5	YSX1610SK 32kHz-XTAL	YXC	RTC crystal	
6	NX1612SA 32Mhz XTAL	NDK	PSoC crystal	
7	U.FL-R-SMT-1(10(	Hirose	Antenna connector	
8	LBEE5WV2GF	Murata	Wifi / BLE Module	Wifi Module with BLE functionality

2 Industrial Data Connect Architecture

With our solution you get an complete open source ecosystem developed with ModusToolbox and web technologies to bring your device up and running in no time. You only need to integrate your custom code to handle your software. The secured connectivity is done by Infineon.

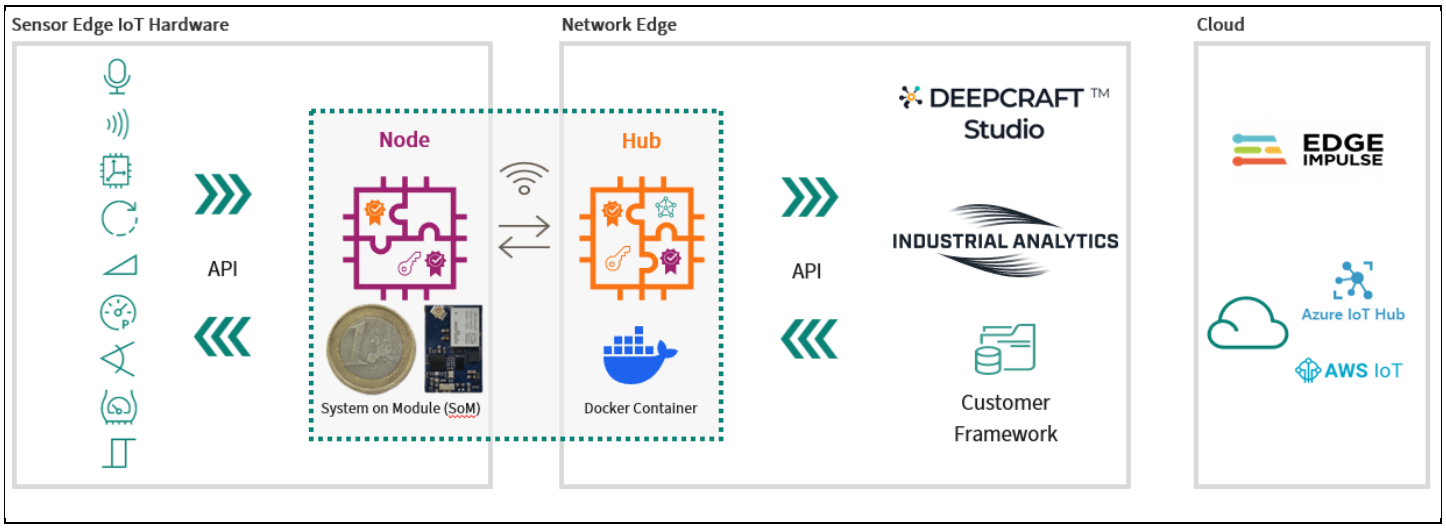


Figure 2

2.1 Modus Toolbox

To develop your own solutions. Infineon provides a complete development set with Modus Toolbox at https://www.infineon.com/design-resources/development-tools/sdk/modustoolbox-software

3 Pinouts

The Pinouts refer to the main PSOC 6 MCU CY8Cdatasheet specifications. There is the pinout

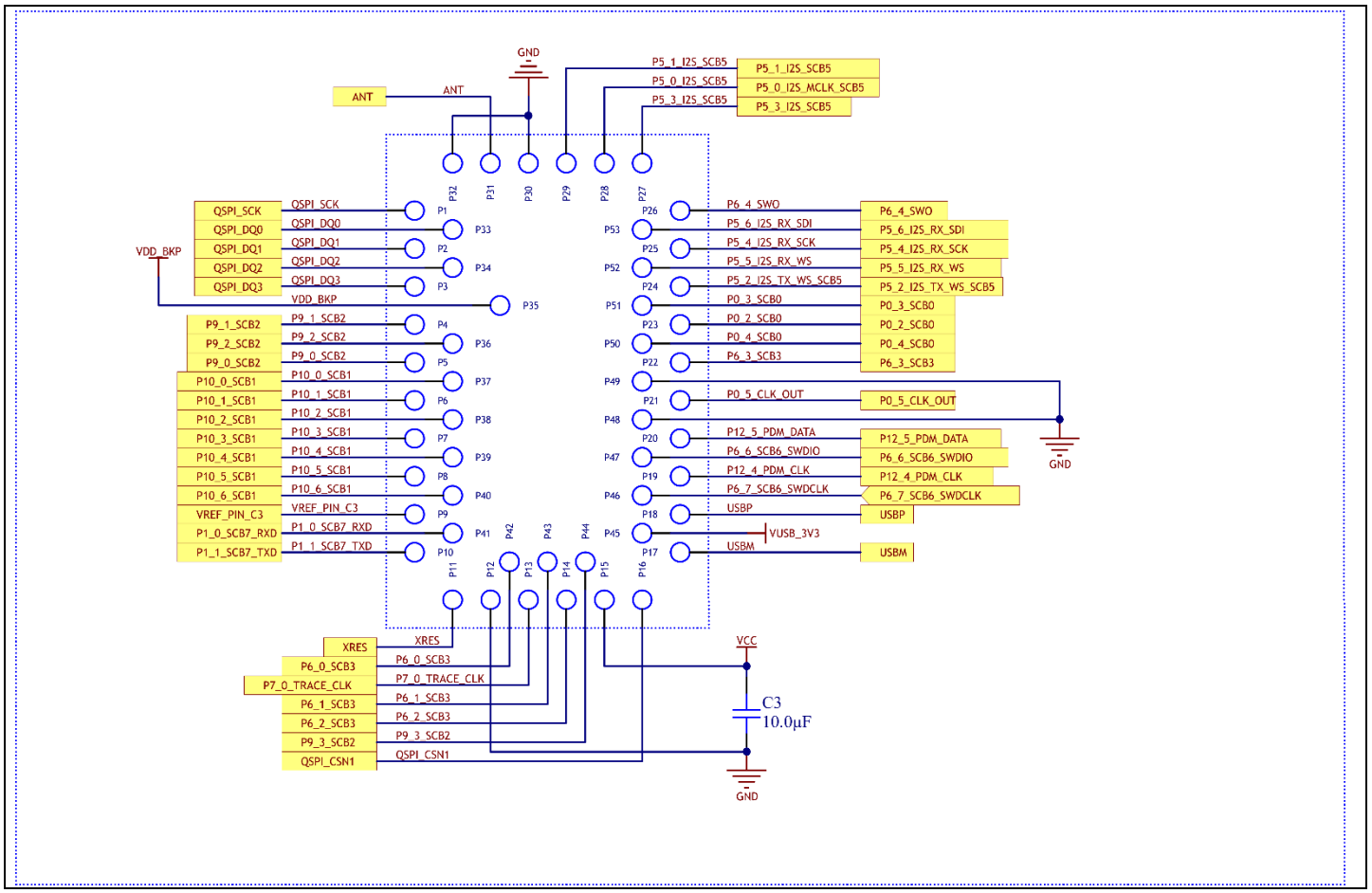


Figure 3 Raw Pinout out of Altium

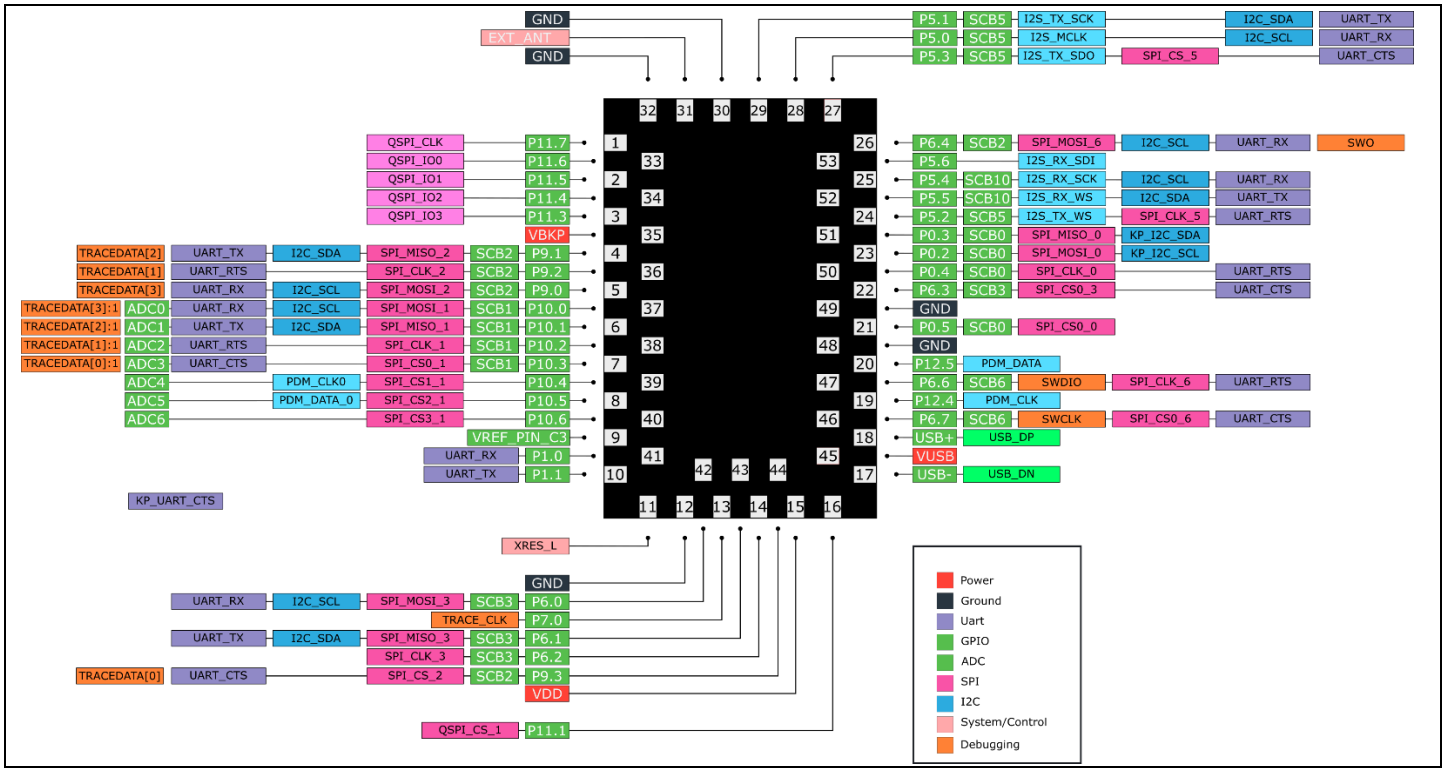


Figure 4 Descriptive Pinout with pin specials

Table 2 Table of Pinouts merged with pin special out of Datasheet from Infineon

SOM PIN	Port Pin @PSOC62	Description/ Function	SCB	Datasheet Page	Alternative Count
9	VREF			External Voltage reference for CSD and Comparator (0.6V to (VDDA - 0.6)V) DS.p57	17
48	GND			Main Ground	36
49	GND			Main Ground	38
30	AND GND				51
32	ANT GND				53
26	P6.4	DEBUG_SWO			47
31	ANT0	EXT ANTENNA CONNECTOR			52
51	P0.3	GPIO	[SCB0]		42
22	P6.3	GPIO	[SCB3]		39
14	P6.2	GPIO,	[SCB3]		25
37	P10.0	GPIO, AIN0			10
6	P10.1	GPIO, AIN1			11
38	P10.2	GPIO, AIN2			12
7	P10.3	GPIO, AIN3			13
39	P10.4	GPIO, AIN4			14
19	P12.4	GPIO, AUDIO PDM CLK		18	33

SOM PIN	Port Pin @PSOC62	Description/ Function	SCB	Datasheet Page	Alternative Count
20	P12.5	GPIO, AUDIO PDM DATA		18	35
47	P6.7	GPIO, DEBUG SWDCLK			34
46	P6.6	GPIO, DEBUG SWDIO			32
50	P0.4	GPIO, Exernal Input/ WAKEUP	[SCB0]		40
21	P0.5	GPIO, ExT Clock Out	[SCB0]		37
28	P5.0	GPIO, I2S MCLK	[SCB5]		49
53	P5.6	GPIO, I2S RS SDI	[SCB10]		46
25	P5.4	GPIO, I2S RX SCLK	[SCB10]		45
52	P5.5	GPIO, I2S RX WS	[SCB10]		44
29	P5.1	GPIO, I2S TX SCLK	[SCB5]		50
27	P5.3	GPIO, I2S TX_SDO	[SCB5]		48
24	P5.2	GPIO, I2S TX_WS	[SCB5]		43
23	P0.2	GPIO, MAIN I2C	[SCB3]		41
36	P9.2	GPIO, MAIN SPI CLK	[SCB2]		8
44	P9.3	GPIO, MAIN SPI CS	[SCB2]		26
4	P9.1	GPIO, MAIN SPI MISO	[SCB2]		7
5	P9.0	GPIO, MAIN SPI MOSI	[SCB2]		9
41	P1.0	GPIO, MAIN UART RX	[SCB7]		18
10	P1.1	GPIO, MAIN UART TX	[SCB7]		19
16	P11.1	GPIO, SMIF SPI CHIP SELECT 1			28
13	P7.0	GPIO, TRACE CLK			23
42	P6.0	GPIO, UART RX	[SCB3]		22
43	P6.1	GPIO, UART TX	[SCB3]		24
8	P10.5	GPIO,AIN5			15
40	P10.6	GPIO,AIN6			16
12	GND	Ground for SoM			21
15	VCC	MAIN VCC			27
11	XRES	N RESET PIN			20
1	P11.7	SMIF SPI CLK			1
33	P11.6	SMIF SPI DATA 0			2
2	P11.5	SMIF SPI DATA 1			3
34	P11.4	SMIF SPI DATA 2			4
3	P11.3	SMIF SPID DATA 3			5
17	USBM	USB NEGATIVE PORT		16	29
18	USBP	USB POSITIVE PORT		16	31
35	VDD_BKP	VDD BACKUP		VDD Battery Backup	6

SOM PIN	Port Pin @PSOC62	Description/ Function	SCB	Datasheet Page	Alternative Count
45	VUSB	VUSB 3V3		Connect to GND if USB not used	30

3.1 GPIO

Overview of

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Hold mode for latching previous state (used for retaining the I/O state in system Hibernate mode)
- Selectable slew rates for dV/dt-related noise control to improve EMI
- Every pin can generate an interrupt if enabled; each port has an interrupt request (IRQ) associated with it.
- The port 1 pins are capable of overvoltage-tolerant (OVT) operation, where the input voltage may be higher than VDDD. OVT pins are commonly used with I2C, to allow powering the chip OFF while maintaining a physical connection to an operating I2C bus without affecting its functionality.

3.2 Notes

1. *If the USB pins are not used, connect VDDUSB to ground and leave the P14.0/USBDP and P14.1/USBDM pins unconnected.*
2. *Voltage must be applied to the VDDD pin, and the VDDA pin as noted above, for correct device initialization and operation. If an I/O port is not being used, applying voltage to the corresponding VDDx pin is optional.*
3. *Battery Connection to V_{BACKUP}*

Figure 19. Separate Battery Connection to V_{BACKUP}

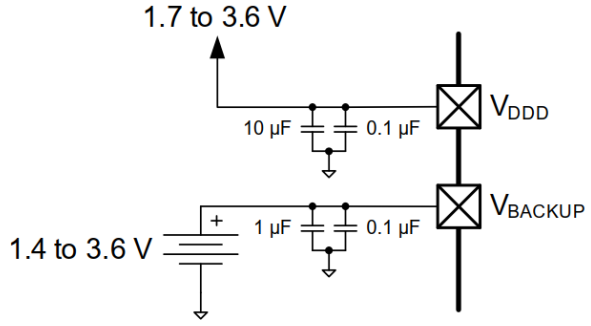


Figure 5

4 Electrical Specifications

There you find the minimum overview of the maximum ratings for the main components used on the module.

We could define an overall data table - this needs to be discussed how to present

4.1 PSOC 62

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted.

Table 3 Absolute Maximum Ratings

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details
SID1	V_{DD_ABS}	Analog or digital supply relative to VSS (VSSD = VSSA)	-0.5	-	4	V	
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to VSSD	-0.5	-	1.2	V	
SID3	V_{GPIO_ABS}	GPIO voltage; VDDD or VDDA	-0.5	-	VDD+0.5	V	
SID4	I_{GPIO_ABS}	Current per GPIO	-25	-	25	mA	
SID5	$I_{GPIO\_Injection}$	GPIO injection current per pin	-0.5	-	0.5	mA	
SID3A	ESD_HBM	Electrostatic discharge Human Body Model	2200	-	-	V	
SID4A	ESD_CDM	Electrostatic discharge Charged Device Model	500	-	-	V	
SID5A	LU	Pin current for latchup-free operation	-100	-	100	mA	

4.2 Murata 2GF

Table 4 Parameter

Parameter	Minimum	Typical	Maximum	Unit
Operating Voltage	-20	25	+70	°C
Supply Voltage VBAT	3.2	3.6	4.4	V
Supply Voltage VDDIO	1.62	1.8	1.98	V
Peak current VBAT			450	mA

4.3 TrustM

5 Volt tolerant IC

4.4 AT25QL641

Table 5 Operating Ranges

Parameter	Symbols	Conditions	Min	Max	Units
Supply Voltage	V_{CC}	fR=133MhZ (Single/Dual/qSPI) fr = 50Mhz (Read Data 03h)	1.7	2.0	V
Ambient Operating Voltage	TA	Industrial	-40	+85	°C

Table 6 Endurance and Data retentions

Parameter	Conditions	Min	Max	Units
Erase/Program Cycles	4kB block, 32-/64-kB block, or full chip	100,000		Cycles
Data Retention	Full temperature range		20	Years

4.5 Device-Level Specifications

This Table summarizes these specifications, for rapid review of CPU currents under common conditions. Note that the max frequency for CM4 is 150 MHz, and for CM0+ is 100 MHz. IMO and FLL are used to generate the CPU clocks; FLL is not used when the CPU clock frequency is 8 MHz.

Table 7 CPU Current Specifications Summary

Condition	Range	Typ Range	Max Range
LP Mode, VDDD = 3.3 V			
CM4 active, CM0+ sleep, WIFI off/sleep			
CM4 sleep, CM0+ active, WIFI off/sleep			
CM4 sleep, CM0+ sleep			
CM0+ sleep, CM4 off			
tbc.			

5 Packaging: tape & reel specification

All IIDC modules come in a tape & reel package suitable for pick and place machines. Small quantities are delivered as cut-tape. There are 2 kinds of reels available with 100pcs and 500pcs per reel (see section ordering information) Except the number of modules, all parameters are same to booth reel sizes:

- 13” reel size
- 44mm tape width
- tape pocket dimensions 29mm x 19mm x 4mm
- module spacing 24mm
- 2mm hole in the middle of the module body
- 1.5mm tape holes for transport

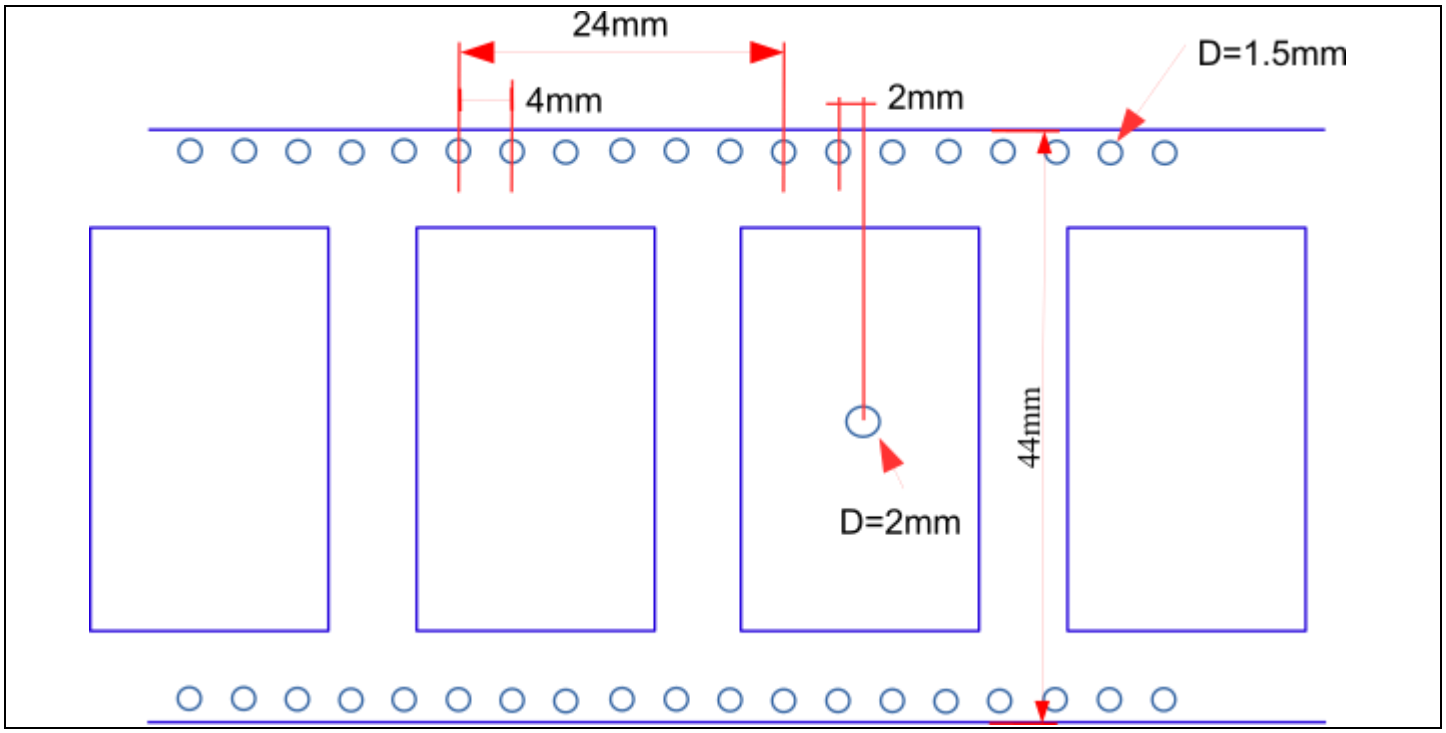


Figure 6

6 Reflow Temperature Profile

The single most critical stage in the automated assembly process is the reflow stage. The reflow profile shall not exceed the following maximum ratings:

- heating gradients <3°C/sec
- peak zone temperature of the module <245°C
- time in peak zone <40 sec.
- time above 220°C <80 sec.

Excessive temperatures, transport times and shocks during the reflow process MUST not be applied to the module.

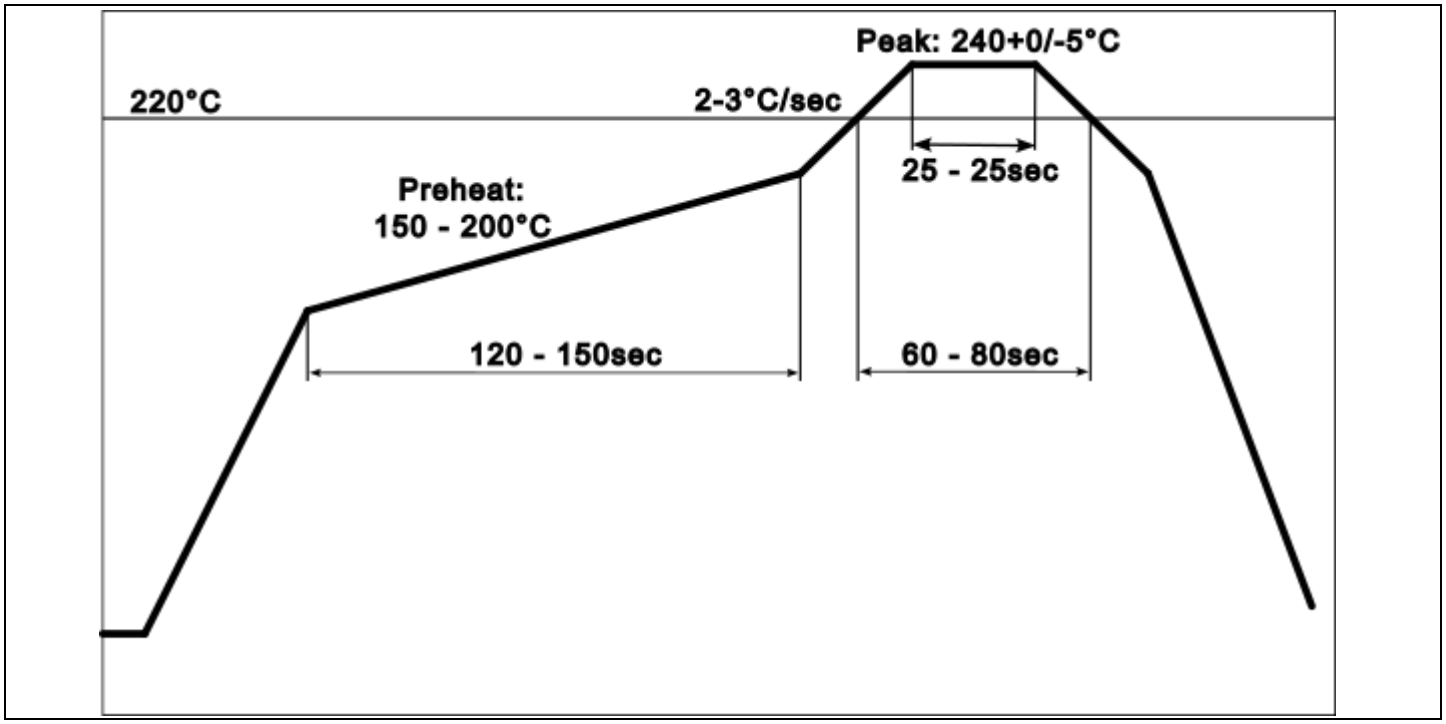


Figure 7

6.1 Washability

The IIDC modules are wash-resistant, but are not sealed. In-Circuit recommends manufacturing without washing. If washing is needed make sure that a drying time is provided to the modules before applying electrical power. The drying time should be sufficient to allow any moisture that may have migrated into the module to evaporate, thus eliminating the potential for shorting damage during power-up or testing. If the wash contains contaminants, the performance may be adversely affected, even after drying.

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Glossary

AA
active authentication (AA)

AAUI
application activation user interface (AAUI)

AC
alternating current (AC)

AC
access control (AC)

ACLB
advanced contactless bridge (ACLB)
The ACLB interface is used to connect the security controller acting in the role of contactless IC (CIC) to an external analog contactless frontend (ACF), both together forming (part of) a “Boosted NFC” system. The data exchange via the ACLB interface is based on symbol level.

API
Application Programming Interface (API)

BDT
buffered data transfer (BDT)
The controller is in a low-power state while a communication peripheral transfers data to or from an I/O buffer.

BER
basic encoding rules (BER)

BIST
built-in self-test (BIST)
A mechanism that permits the chip to test itself.

FOTA
Firmware-over-the-air-update (FOTA)

HAL
Hardware Abstaction Layer (HAL)

HSM
Hardware Security Module (HSM)

MCU
Microcontroller Unit (MCU)

SoM
System-on-Module (SoM)

Revision history

Document revision	Date	Description of changes
0.1	2025-11-12	Initial version

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