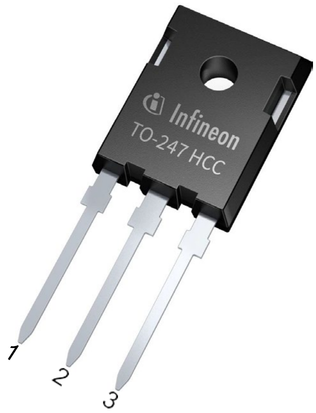
最终数据手册

英飞凌工业用CoolSiC™ 1700 V SiC 沟槽 MOSFET： 碳化硅MOSFET

特性

- V_{DSS} = 1700 V at T_{vj} = 25°C
- I_{DDC} = 10 A at T_C = 25°C
- $R_{DS(on)}$ = 450 mΩ at V_{GS} = 12 V, T_{vj} = 25°C
- 针对反激式拓扑进行了优化
- 12 V / 0 V 栅极源电压与大多数反激式控制器兼容
- 开关损耗非常低
- 基准栅极阈值电压，$V_{GS(th)}$ = 4.5V
- 完全可控的 dv/dt，用于 EMI 优化
- 英飞凌.XT 互连技术，实现、行业领先的热性能



Halogen-free
Green
Lead-free
RoHS

潜在应用

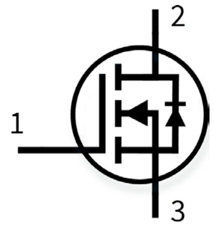
- 通用驱动器 (GPD)
- 电动汽车充电
- 储能系统(ESS)
- 组串式逆变器
- UPS（不间断电源）

产品验证

- 符合JEDEC47/20/22相关测试的工业应用要求

描述

1 – 栅极
2 - 漏极
3 - 来源



Type	Package	Marking
IMWH170R450M1	PG-TO247-3-STD-NN4.8	170M1450

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。 为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

目录

1 封装

表1 特征值

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Internal source inductance measured 5 mm (0.197 in.) from case	L_S			13		nH
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	wave soldering 1.6 mm (0.063 in.) from case for 10 s			260	°C
Mounting torque	M	M3 screw, Maximum of mounting processes: 3			0.6	Nm
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			1.04	1.35	K/W

2 MOSFET

表2 最大额定值

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1700	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 12$ V	$T_c = 25$ °C	10	A
			$T_c = 100$ °C	7.1	
Peak drain current, t_p limited by $T_{vj(max)}$	I_{DM}	$V_{GS} = 12$ V		25.6	A
Gate-source voltage, max. transient voltage[1)]	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10/20	V
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25$ °C	111	W
			$T_c = 100$ °C	55	

1) 重要提示：正、负栅极源电压的选择会影响器件的长期行为。为了确保器件在计划使用寿命内的正常运行，必须考虑应用说明AN2018-09中描述的设计指南。

表 3 建议值

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		12...15	V
Recommended turn-off gate voltage	$V_{GS(off)}$		0	V

表4 **特征值**

Parameter	Symbol	Note or test condition		Values Min.	Values Typ.	Values Max.	Unit
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 2 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 12 V		450		mΩ
			T_{vj} = 100 °C, $V_{GS(on)}$ = 12 V		638		
			T_{vj} = 175 °C, $V_{GS(on)}$ = 12 V		917		
			T_{vj} = 25 °C, $V_{GS(on)}$ = 15 V		364	390	
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 2.6 mA, V_{DS} = V_{GS} (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.5	5.7	V
			T_{vj} = 175 °C		3.6		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1700 V, V_{GS} = 0 V	T_{vj} = 25 °C		0.9	11	µA
			T_{vj} = 175 °C		10		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = 20 V			100	nA
			V_{GS} = -10 V			-100	
Forward transconductance	g_{fs}	I_D = 2 A, V_{DS} = 20 V			0.9		S
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			20		Ω
Input capacitance	C_{iss}	V_{DD} = 1000 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			506		pF
Output capacitance	C_{oss}	V_{DD} = 1000 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			19.4		pF
Reverse transfer capacitance	C_{rss}	V_{DD} = 1000 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			1.2		pF
C_{oss} stored energy	E_{oss}	V_{DD} = 1000 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			3.5		µJ
Total gate charge	Q_G	V_{DD} = 1000 V, I_D = 2 A, V_{GS} = 0/12 V, turn-on pulse			11.7		nC
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 1000 V, I_D = 2 A, V_{GS} = 0/12 V, turn-on pulse			4		nC
Gate-to-drain charge	Q_{GD}	V_{DD} = 1000 V, I_D = 2 A, V_{GS} = 0/12 V, turn-on pulse			2.9		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 1000 V, I_D = 2 A, V_{GS} = 0/12 V, $R_{G,ext}$ = 6.9 Ω, L_σ = 40 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		21		ns
			T_{vj} = 175 °C		18		

（表格续下页......）

表 4（续） 特征值

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Rise time	t_r	V_{DD} = 1000 V, I_D = 2 A, V_{GS} = 0/12 V, $R_{G,ext}$ = 6.9 Ω, L_σ = 40 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		12		ns
			T_{vj} = 175 °C		10		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 1000 V, I_D = 2 A, V_{GS} = 0/12 V, $R_{G,ext}$ = 6.9 Ω, L_σ = 40 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		26		ns
			T_{vj} = 175 °C		29		
Fall time	t_f	V_{DD} = 1000 V, I_D = 2 A, V_{GS} = 0/12 V, $R_{G,ext}$ = 6.9 Ω, L_σ = 40 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		23		ns
			T_{vj} = 175 °C		23		
Turn-on energy	E_{on}	V_{DD} = 1000 V, I_D = 2 A, V_{GS} = 0/12 V, $R_{G,ext}$ = 6.9 Ω, L_σ = 40 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		114		µJ
			T_{vj} = 175 °C		118		
Turn-off energy	E_{off}	V_{DD} = 1000 V, I_D = 2 A, V_{GS} = 0/12 V, $R_{G,ext}$ = 6.9 Ω, L_σ = 40 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		26		µJ
			T_{vj} = 175 °C		29		
Total switching energy	E_{tot}	V_{DD} = 1000 V, I_D = 2 A, V_{GS} = 0/12 V, $R_{G,ext}$ = 6.9 Ω, L_σ = 40 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		140		µJ
			T_{vj} = 175 °C		147		
Virtual junction temperature	T_{vj}			-55		175	°C

注意：为了获得最佳的使用寿命和可靠性，英飞凌建议工作条件不超过本数据手册中所述最大额定值的 80%。

该芯片技术的特征高达200 kV/µs。测量的dV/dt 受到测量测试设置和封装的限制。

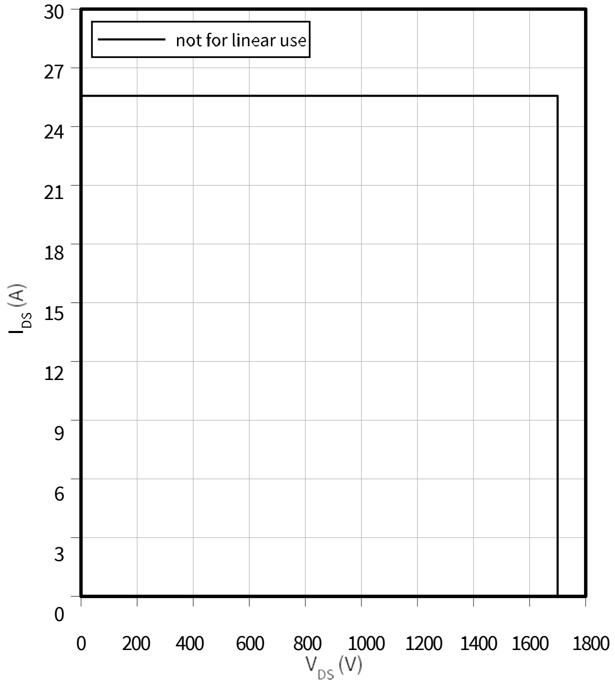
动态测试电路见图F。

3 特性图

Reverse bias safe operating area (RBSOA)

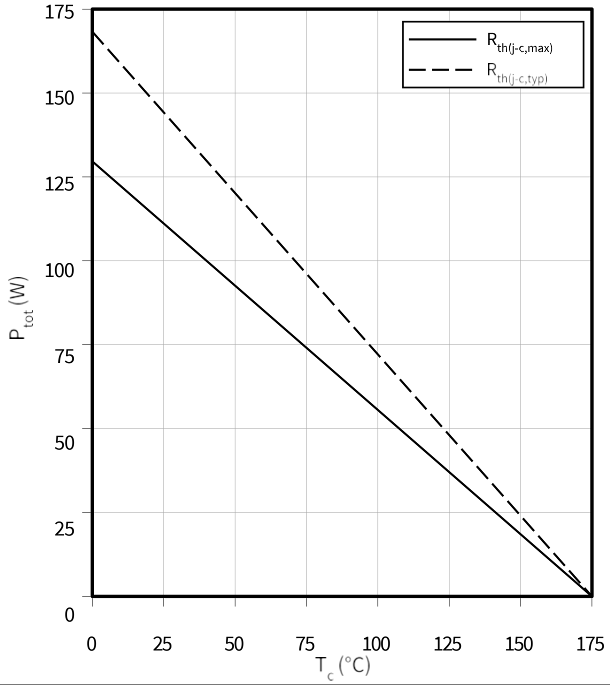
$I_{DS} = f(V_{DS})$

$T_{vj} \leq 175$ °C, $V_{GS} = 0/12$ V, $T_c = 25$ °C



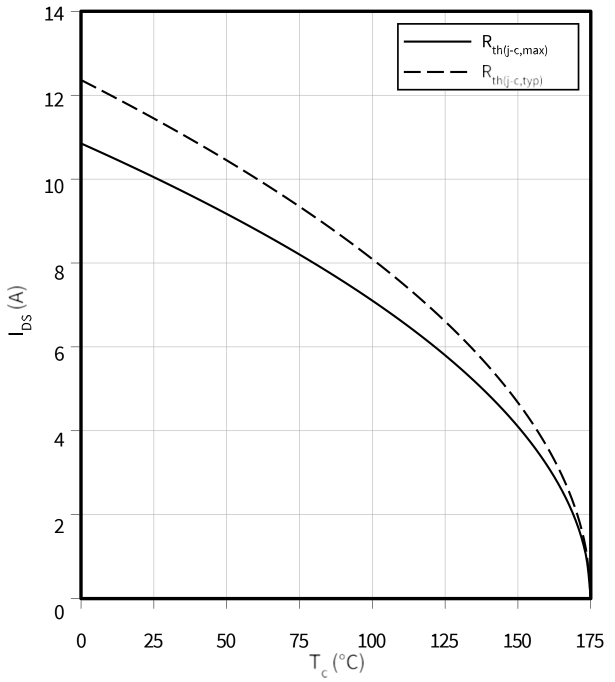
Power dissipation as a function of case temperature limited by bond wire

$P_{tot} = f(T_c)$



Maximum DC drain to source current as a function of case temperature limited by bond wire

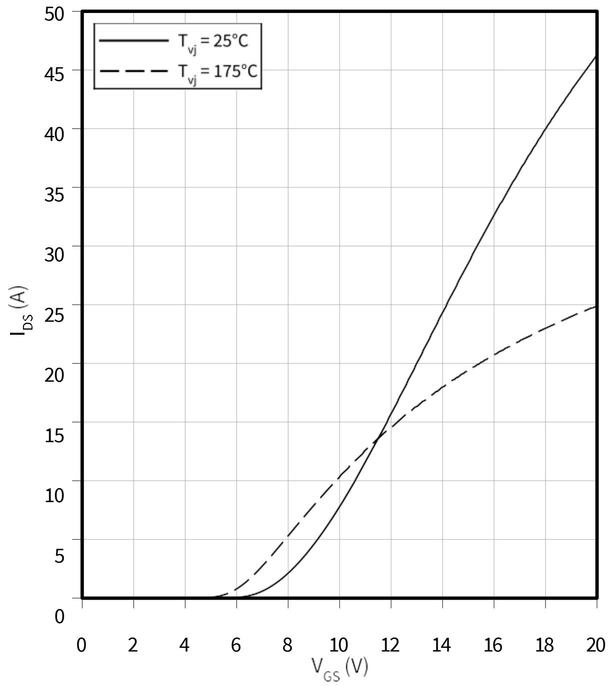
$I_{DS} = f(T_c)$

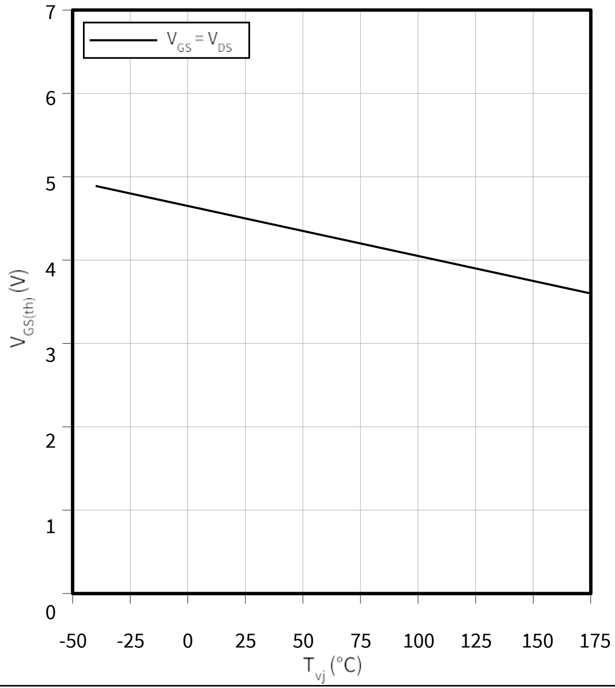
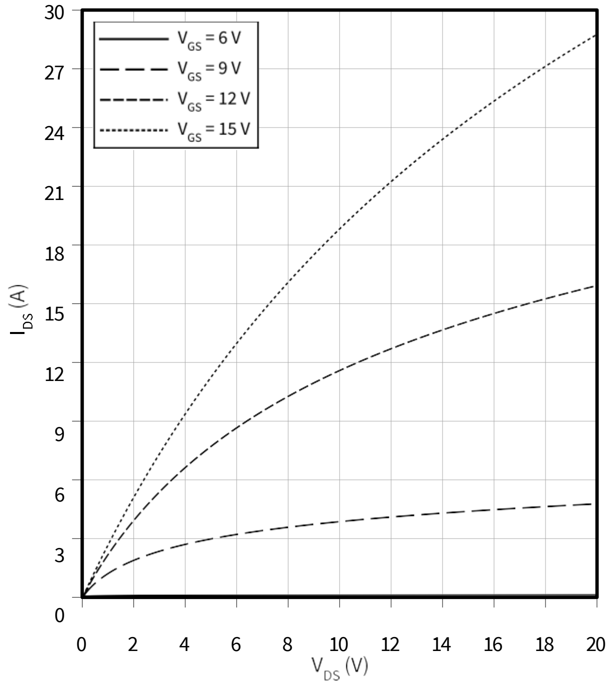
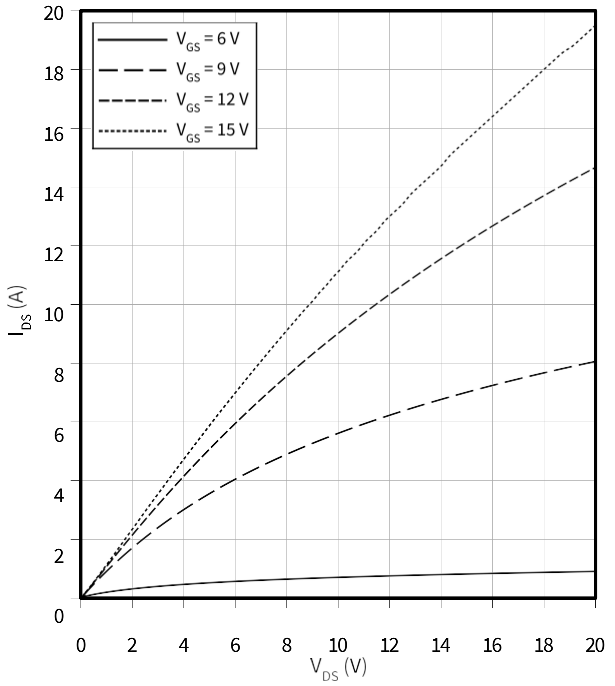
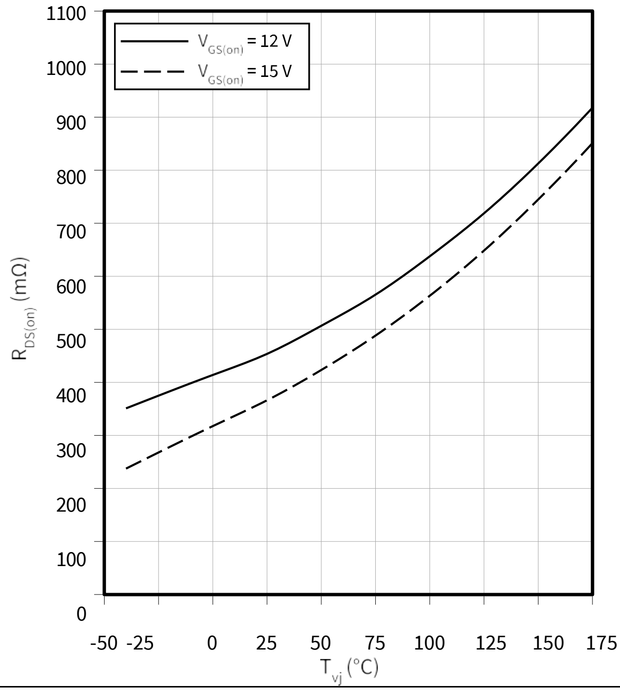


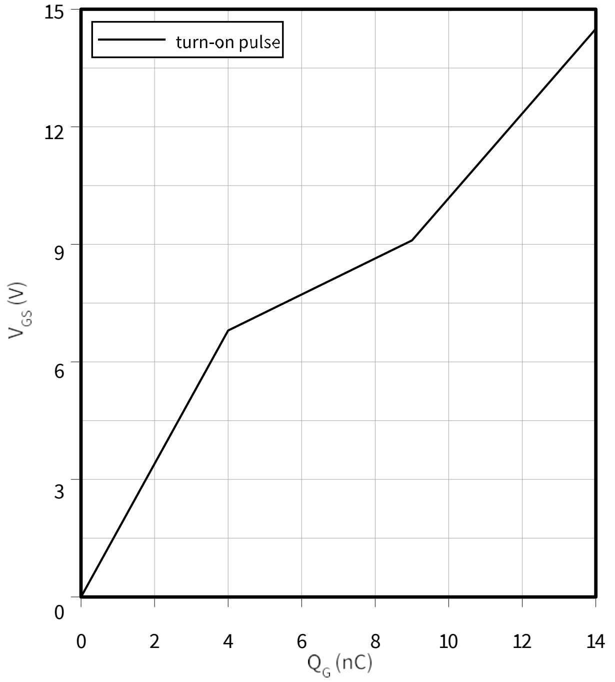
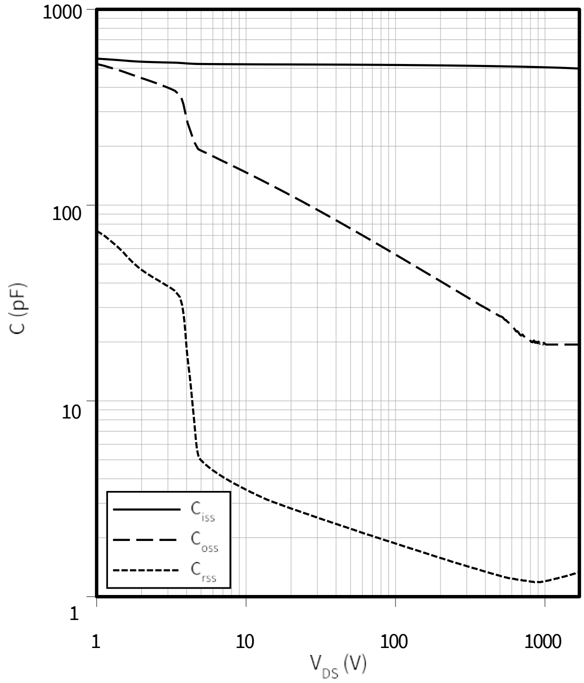
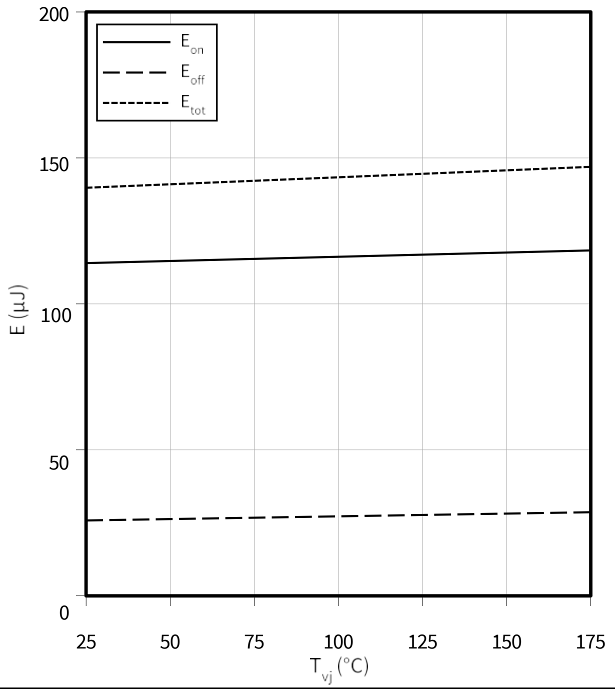
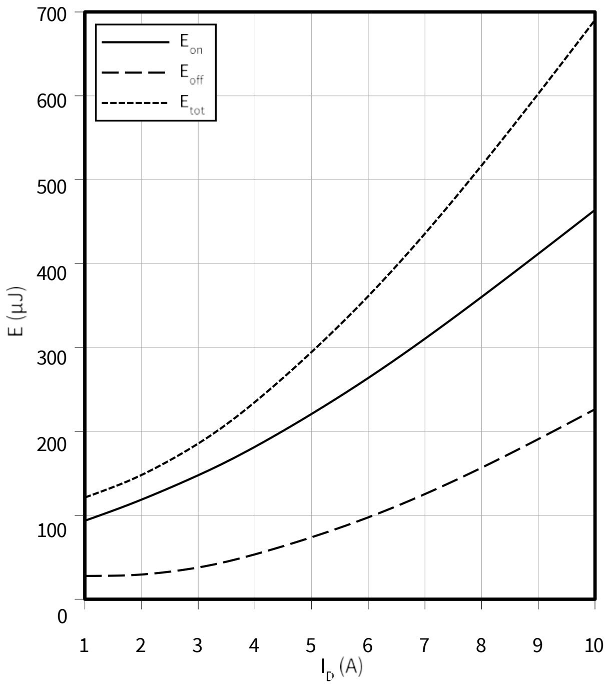
Typical transfer characteristic

$I_{DS} = f(V_{GS})$

$V_{DS} = 20$ V, $t_p = 20$ µs



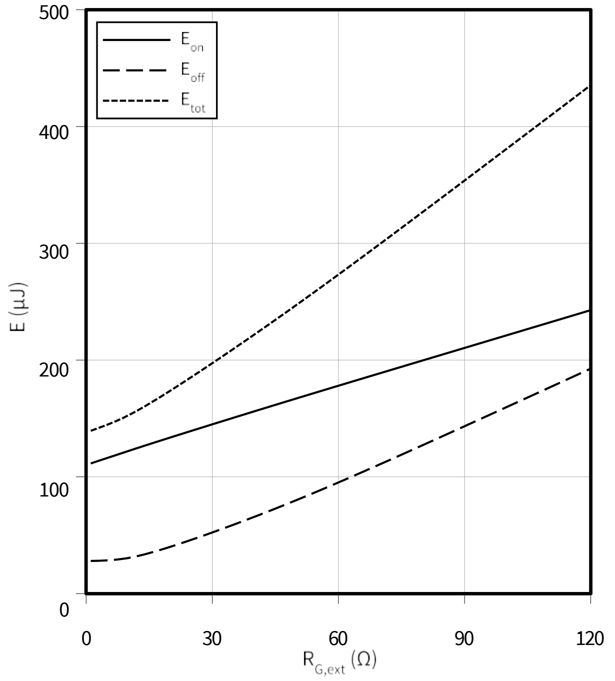
Typical gate-source threshold voltage as a function of junction temperature $V_{GS(th)} = f(T_{vj})$ $I_D = 2.6$ mA	**Typical output characteristic, V_{GS} as parameter** $I_{DS} = f(V_{DS})$ $T_{vj} = 25$ °C, $t_p = 20$ µs
	
Typical output characteristic, V_{GS} as parameter $I_{DS} = f(V_{DS})$ $T_{vj} = 175$ °C, $t_p = 20$ µs	**Typical on-state resistance as a function of junction temperature** $R_{DS(on)} = f(T_{vj})$ $I_D = 2$ A
	

Typical gate charge $V_{GS} = f(Q_G)$ $I_D = 2$ A, $V_{DS} = 1000$ V	**Typical capacitance as a function of drain-source voltage** $C = f(V_{DS})$ f = 100 kHz, $V_{GS} = 0$ V
	
Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0$ V $E = f(T_{vj})$ $V_{GS} = 0/12$ V, $I_D = 2$ A, $R_{G,ext} = 6.9$ Ω, $V_{DD} = 1000$ V	**Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0$ V** $E = f(I_D)$ $V_{GS} = 0/12$ V, $T_{vj} = 175$ °C, $R_{G,ext} = 6.9$ Ω, $V_{DD} = 1000$ V
	

Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(R_{G,ext})$

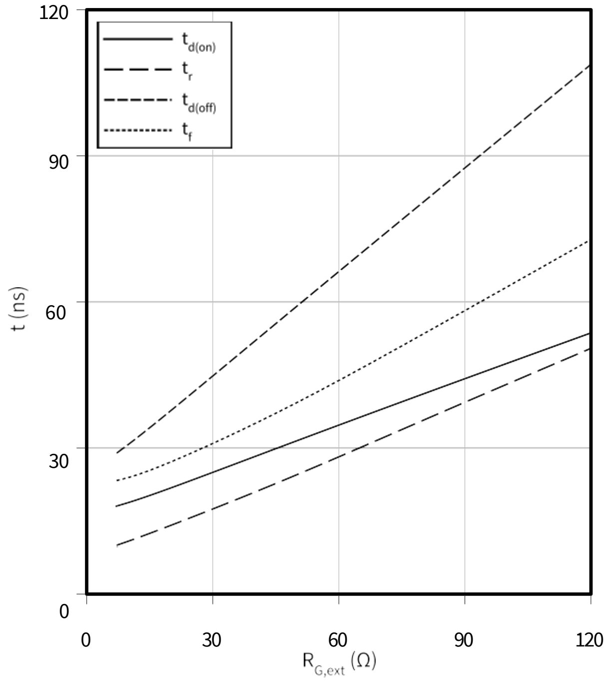
V_{GS} = 0/12 V, I_D = 2 A, T_{vj} = 175 °C, V_{DD} = 1000 V



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$t = f(R_{G,ext})$

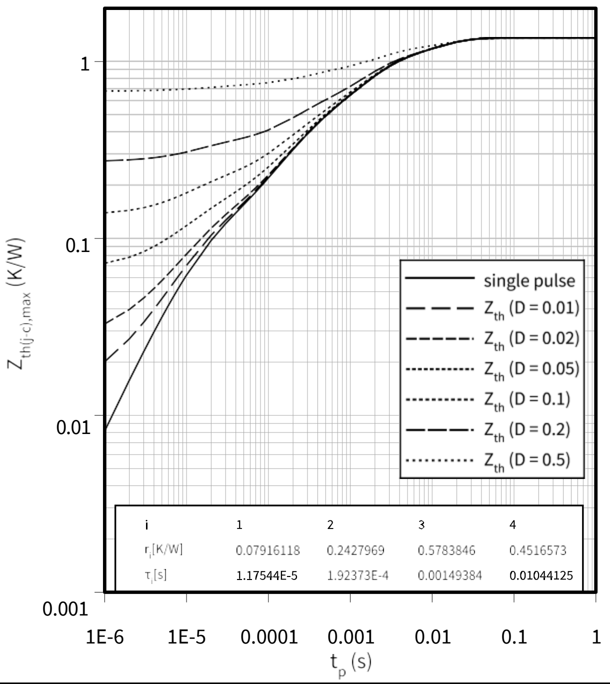
V_{GS} = 0/12 V, I_D = 2 A, T_{vj} = 175 °C, V_{DD} = 1000 V



Max. transient thermal impedance (MOSFET/diode)

$Z_{th(j\text{-}c),max} = f(t_p)$

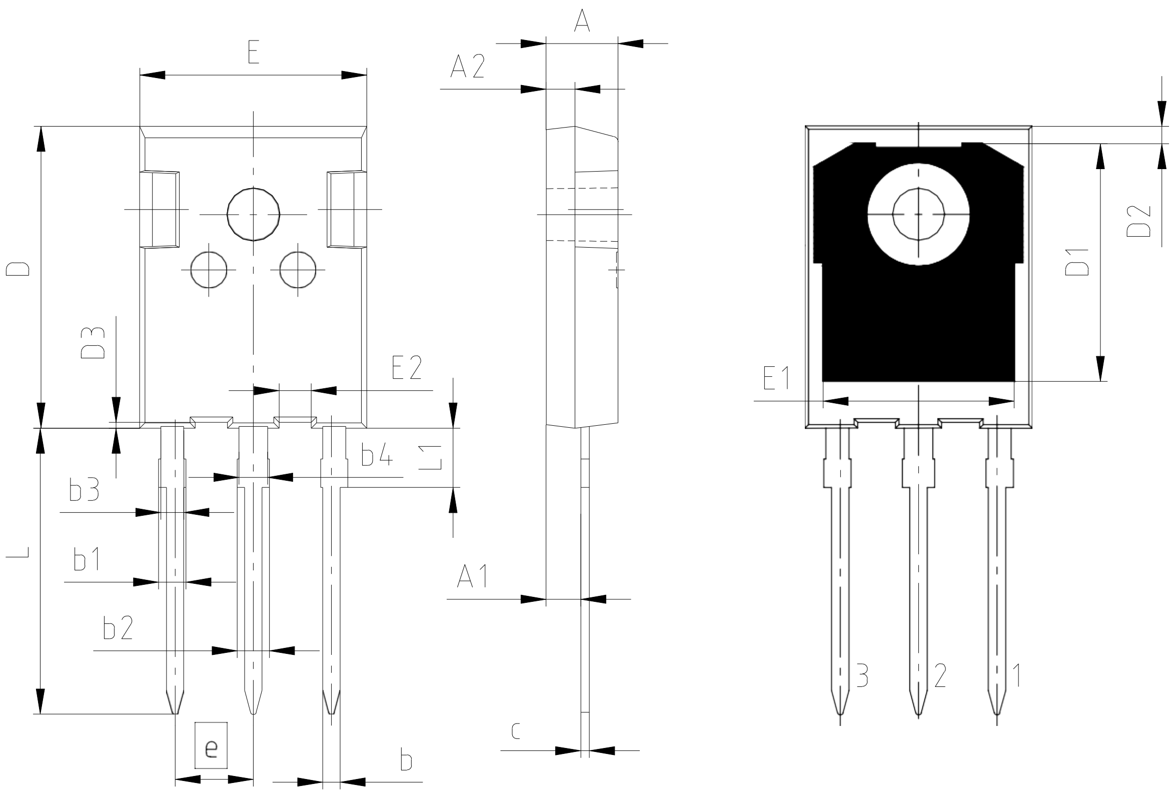
$D = t_p/T$



i	1	2	3	4
r_i[K/W]	0.07916118	0.2427969	0.5783846	0.4516573
τ_i[s]	1.17544E-5	1.92373E-4	0.00149384	0.01044125

4 封装外形

PG-TO247-3-STD-NN4.8



PACKAGE - GROUP NUMBER:	PG-TO247-3-U04	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.90	5.10
A1	2.31	2.51
A2	1.90	2.10
b	1.16	1.26
b1		1.90
b2		2.30
b3	1.55	1.65
b4	1.96	2.06
c	0.59	0.66
D	20.90	21.10
D1	16.25	16.85
D2	1.05	1.35
D3	0.55	0.65
E	15.70	15.90
E1	13.10	13.50
E2	2.14	2.34
e	5.44	
N	3	
L	19.80	20.10
L1	3.95	4.30

图 1

5 测试条件

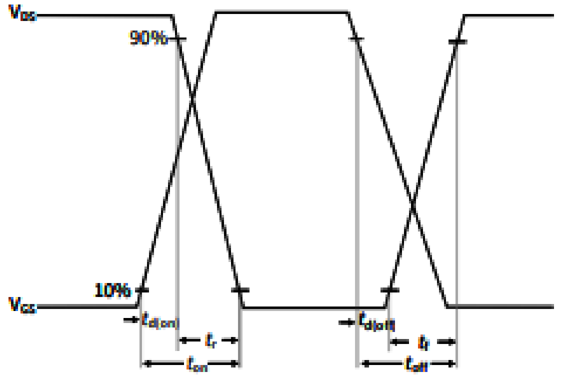


Figure A. **Definition of switching times**

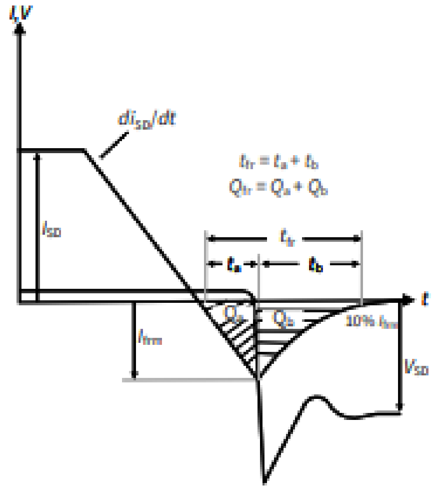


Figure B. **Definition of body diode switching characteristics**

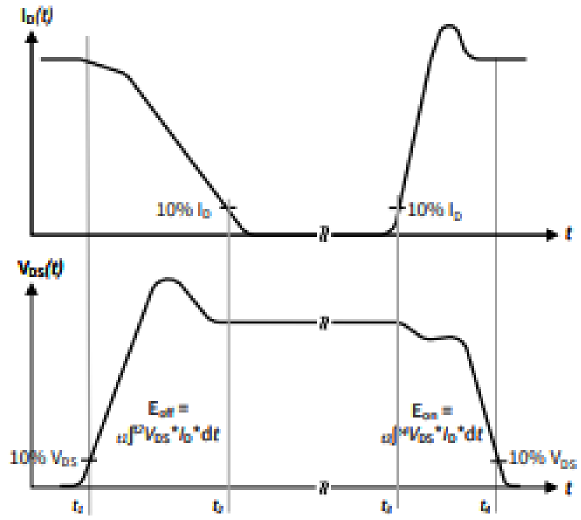


Figure C. **Definition of switching losses**

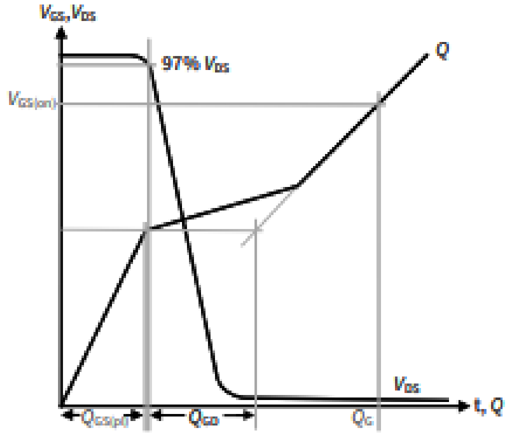


Figure D. **Definition of QGD**

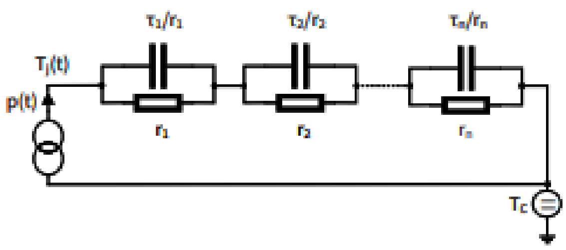


Figure E. **Thermal equivalent circuit**

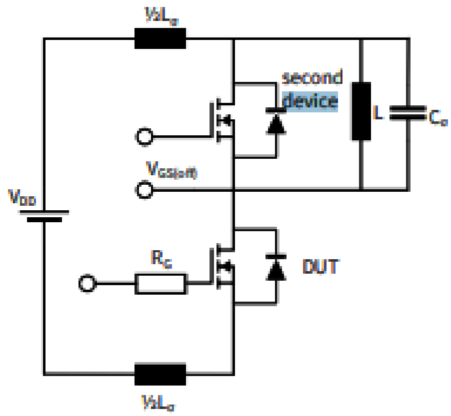


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

修订记录

Document revision	Date of release	Description of changes
1.00	2024-03-25	Final datasheet

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