15 kW two-level PV boost converter reference design

REF-15KW2LBOOST

About this document

Scope and purpose

This user guide describes the two-level boost converter reference design REF-15KW2LBOOST with its main features, key data, pin assignments, mechanical dimensions, and electrical interfaces.

Intended audience

This user guide is meant for engineers and technical specialists working on solar photovoltaic solutions and similar domains. The concept of this power conversion reference design is modular. The hardware can be reused for various power converter applications and use cases, with a special focus on solar photovoltaic solutions.

Reference design

This reference design is not a qualified and certified commercial product. Its hardware does not necessarily meet any safety, EMI, or quality standard (for example, UL, CE) requirements.

Figure 1 **Power conversion board REF-15KW2LBOOST**

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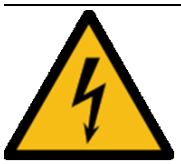
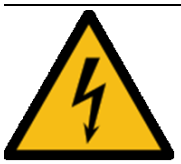
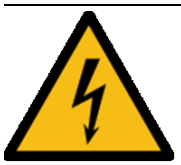
Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 **Safety precautions**

	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *controller board must be connected with the main power board before powering the DC bus.*
	**Warning:** *There is no inrush current limitation on the board, the DC source should be powered up from 0V slowly or set the DC source with a current limitation to 12.5A during startup.*
	**Warning:** *Remove or disconnect power from the system before you disconnect or reconnect wires or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the system until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sinks and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with power electronics should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 The power conversion reference design at a glance

1.1 Introduction

REF-15KW2LBOOST comes as a kit that includes different boards to help users build and operate a three-channel boost converter. The kit includes:

- REF-15KW2LBOOST main board: The three-channel boost DC-DC converter main board
- ISODRV-3240C3P15N05-1: A three-channel gate driver card
- PB-APS-24V-5V ISO: A 24 V – 5 V isolated auxiliary power supply
- Filter-REF-15KW2LBOOST: A boost inductor and EMI filter board
- PB-CAPTANK-1.1KV: An output DC-link capacitor board

The REF-15KW2LBOOST main board contains three basic boost DC-DC converters and carries power semiconductors, gate drivers, and an auxiliary power supply. It also includes connectors that users can use to connect their own passives.

Users can get an XMC7200-based control board separately. This board comes with all the signal-conditioning circuits, a power conversion software, and a GUI that helps operate the 15 kW boost converter as a three-channel interleaved boost in open-loop and closed-loop configurations.

Figure 2 shows the completely assembled 15 kW boost converter reference design, including an XMC7200-based control board connected to the main board. This control board is available under the name REF-CLBXMC7PEC.

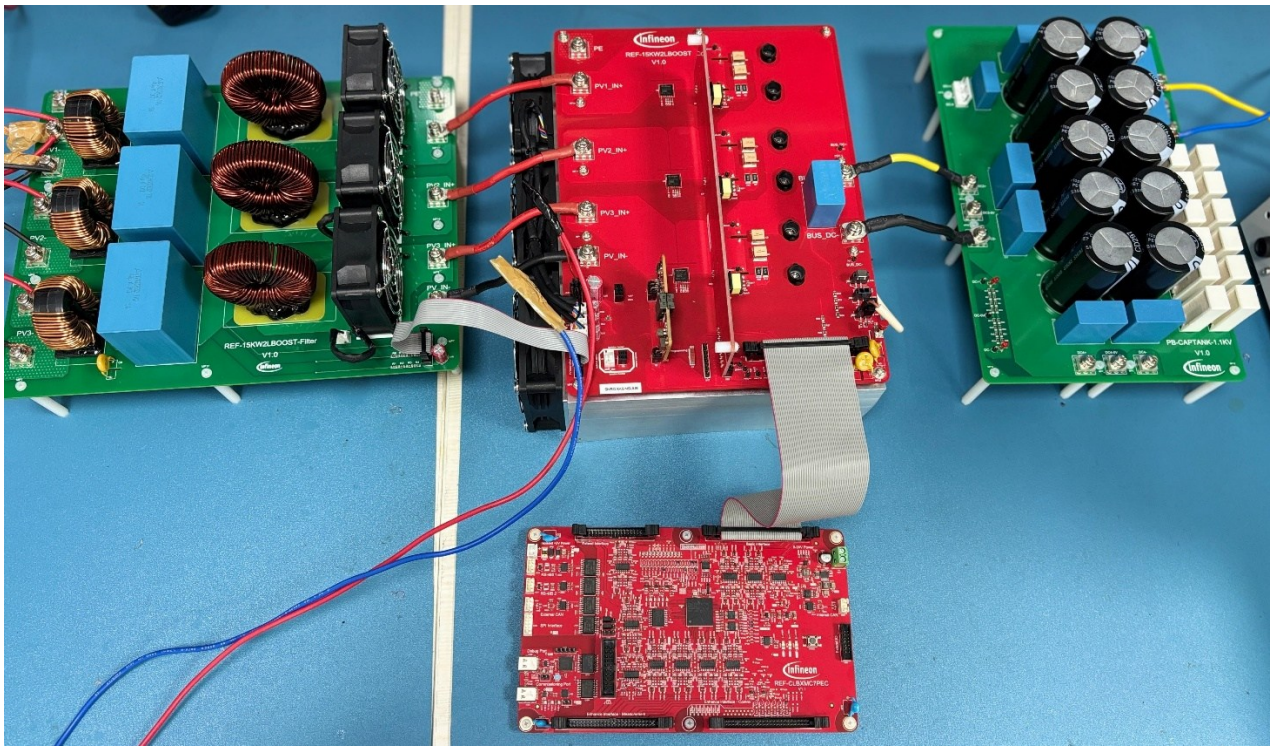


Figure 2 **Power conversion reference design REF-15KW2LBOOST**

1.2 Top-level specifications

Table 2 Specifications

Parameter	Typical	Maximum	Unit
Input voltage		1000[1]	V_{dc}
Output voltage	750	850	V_{dc}
Output power per channel		5	kW
Output power		15	kW
Switching frequency	24	24	kHz

[1] REF-15KW2LBOOST can handle a maximum input voltage of 1000 V. The output voltage is produced while the system runs. When the converter is off, the output may exceed 850 V, but it drops quickly after the converter restarts.

1.3 Key design building blocks

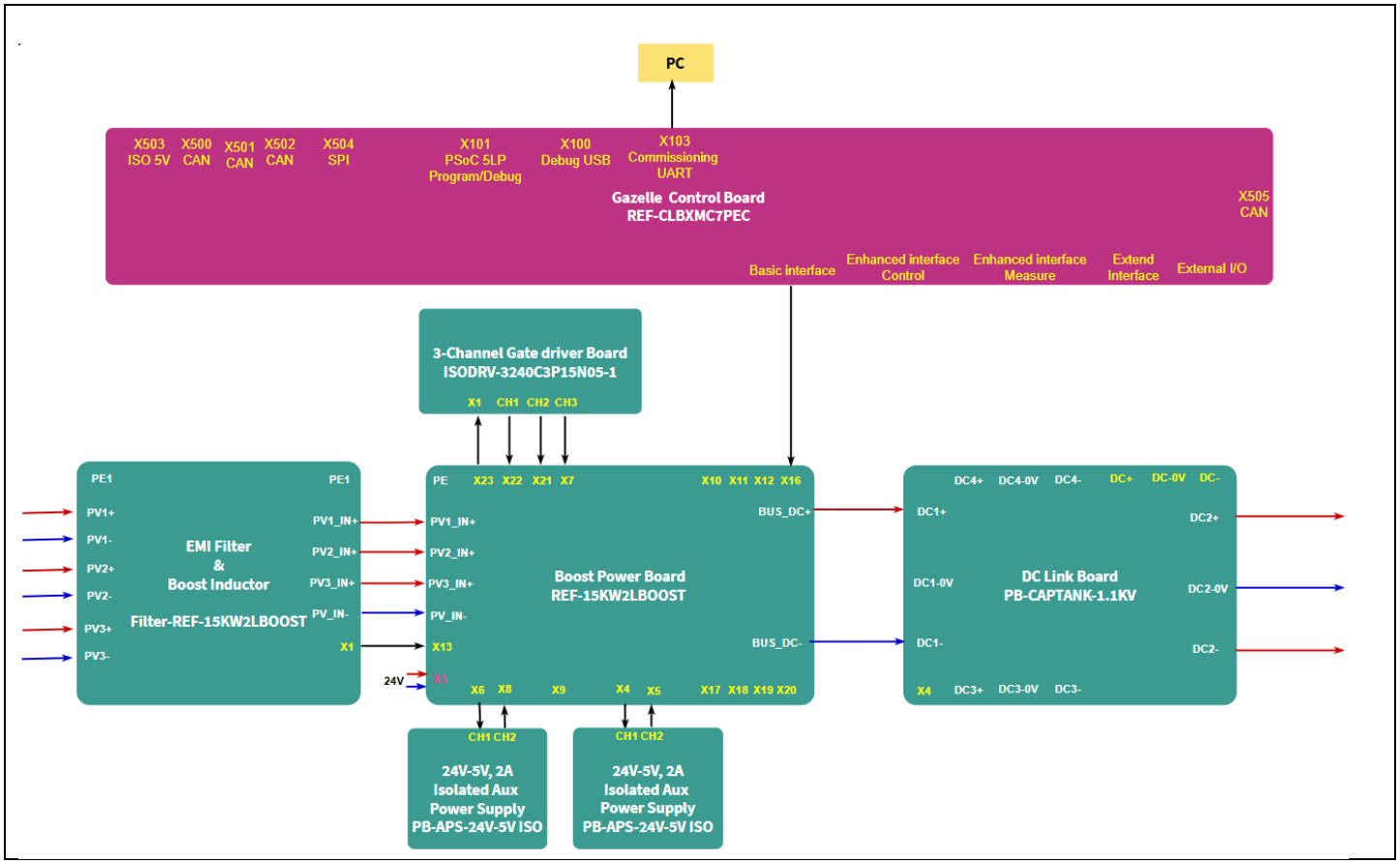


Figure 3 **Assembly diagram**

Figure 3 shows how the different boards are connected to construct the three-channel boost DC-DC converter. Starting from the left, the EMI filter board consists of an EMI filter and a boost inductor for the three channels. The filter board is connected to the boost power conversion board. The negative terminals of the three boost converters are connected internally. The boost power conversion board also contains a gate driver card and two auxiliary power supply cards. Only one is delivered with the current system setup. The second power supply card is intended for powering the communication card in future. Finally, the boost power conversion board is connected to the output DC-link board.

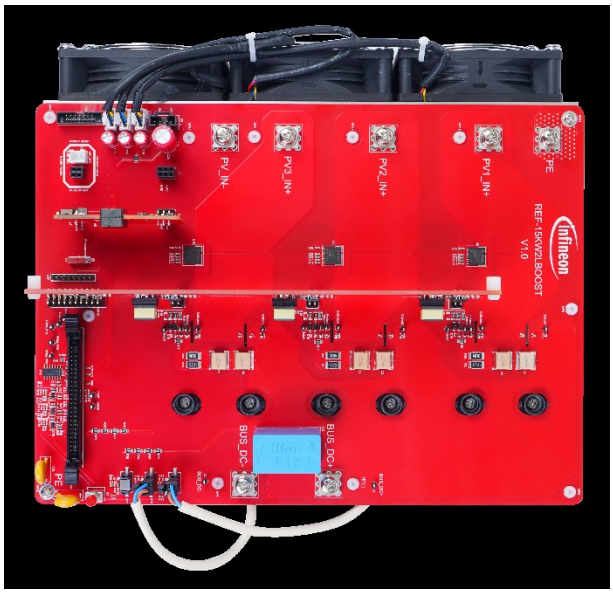


Figure 4 **Main power conversion board: REF-15KW2LBOOST**

Figure 5 **Gate driver board: ISODRV-3240C3P15N05-1**

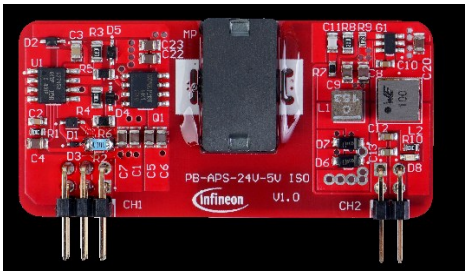


Figure 6 **Auxiliary power supply board: PB-APS-24V-5V ISO**

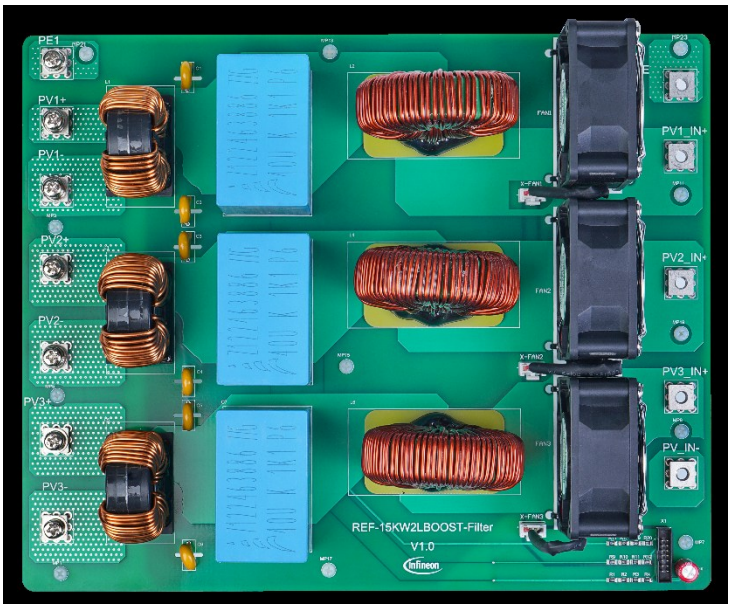


Figure 7 **EMI filter and boost inductor: Filter-REF-15KW2LBOOST**

Figure 8 **DC-link board: PB-CAPTANK-1.1KV**

1.4 Preferred components

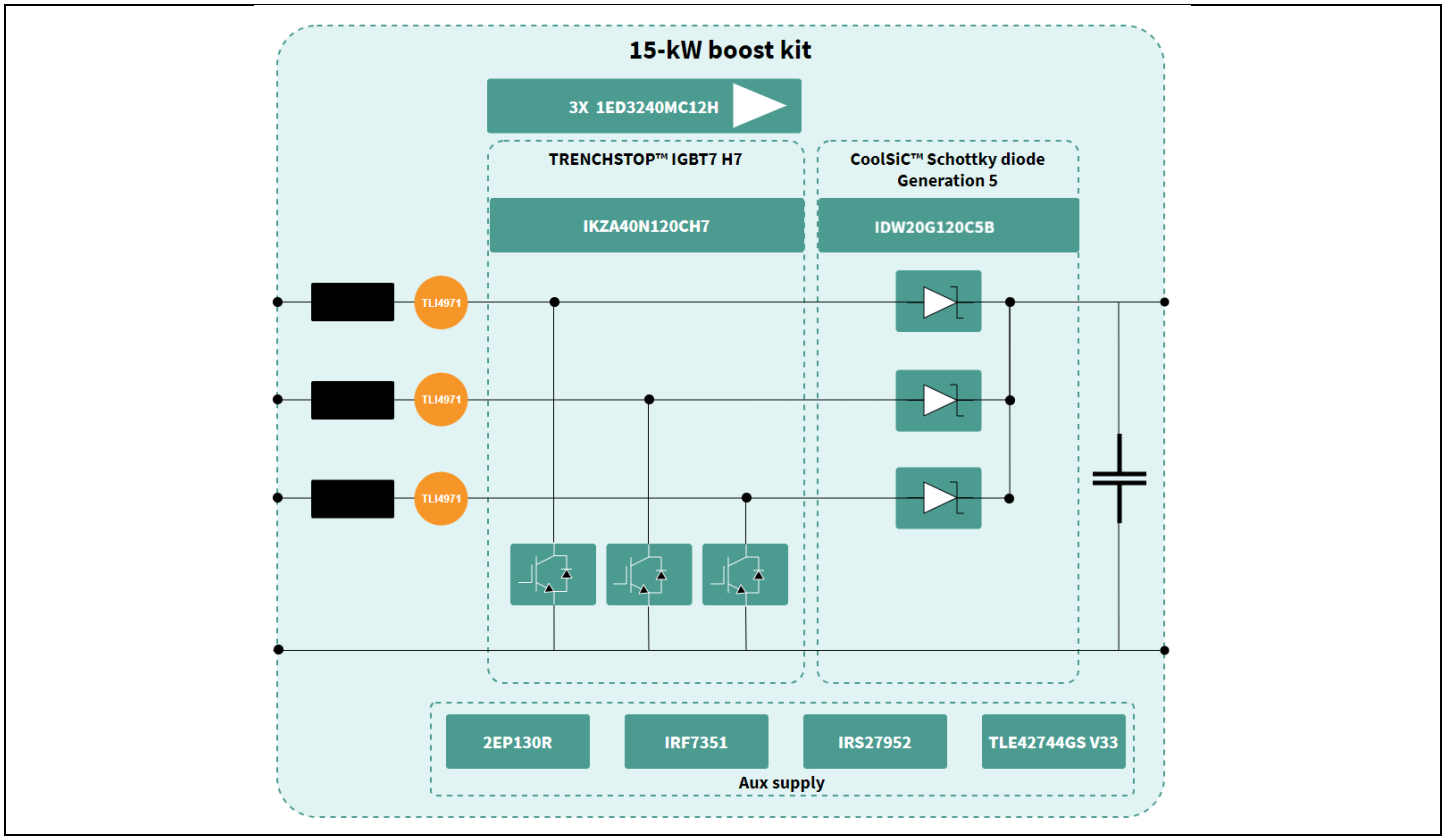


Figure 9 **Block diagram of the power conversion board**

Figure 9 shows the main semiconductors offered in the 15 kW boost converter reference design.

- Power semiconductors:
  - TRENCHSTOP™ IGBT7 H7: IKZA40N120CH7
  - CoolSiC™ Schottky diode generation 5: IDW20G120C5B
- Gate driver:
  - Single-channel, isolated gate driver with two-level slew rate control: 1ED3240MC12H
- Current sensor:
  - XENSIV™ magnetic current sensor: TLI4971
- Auxiliary power supply:
  - Full-bridge transformer driver: 2EP130R
  - Half-bridge controller IC: IRS27952
  - 60 V dual N-channel HEXFET power MOSFET: IRF7351

2 Functional description of the board

This chapter lists the features available for the 15 kW boost converter reference design.

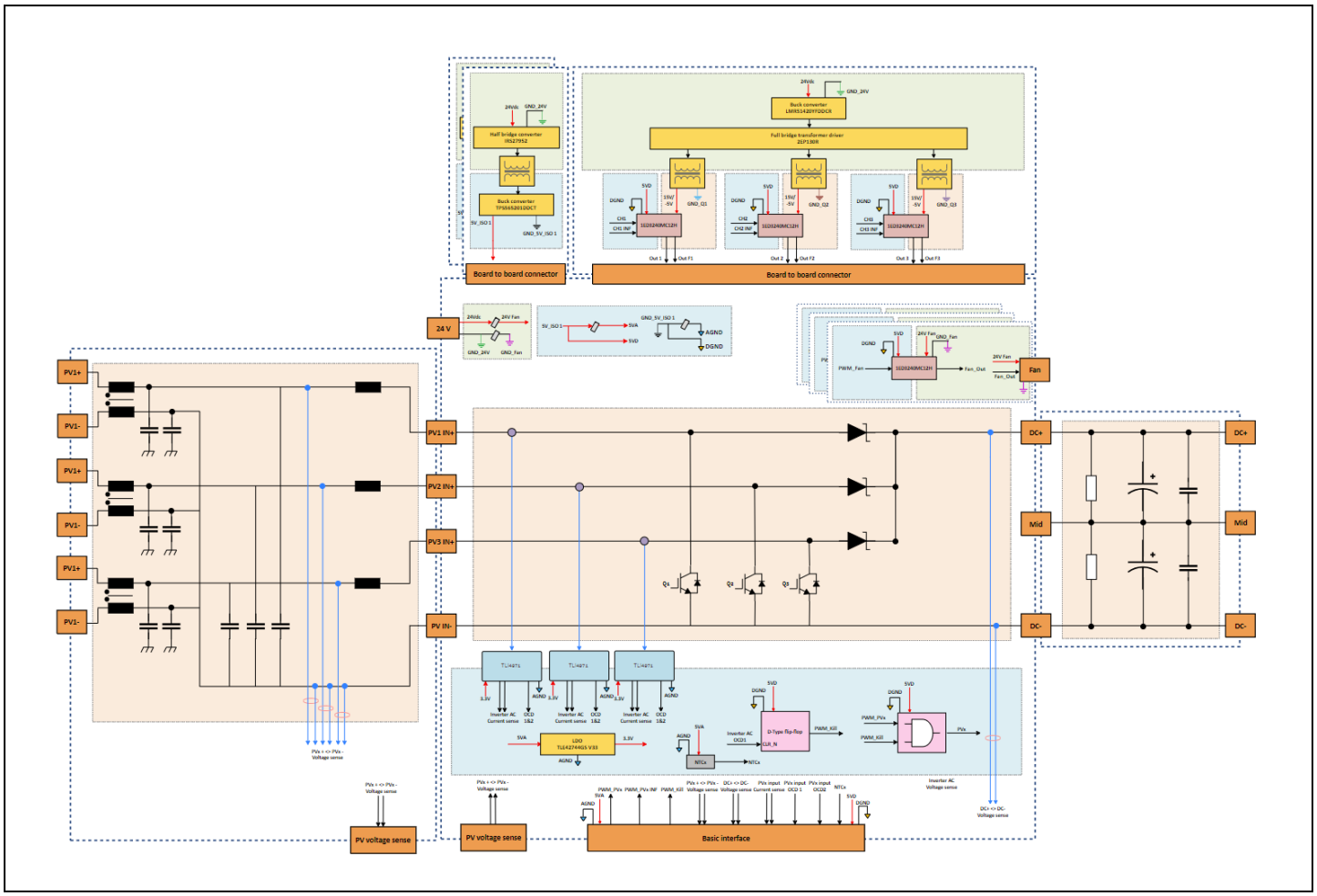


Figure 10 **Block diagram of REF-15KW2LBOOST**

2.1 Description of the functional blocks

2.1.1 Switching devices

The boost power stage is realized using the TRENCHSTOP™ IGBT7 H7 IKZA40N120CH7 and the CoolSiC™ Schottky diode IDW20G120C5B, shown in Figure 11.

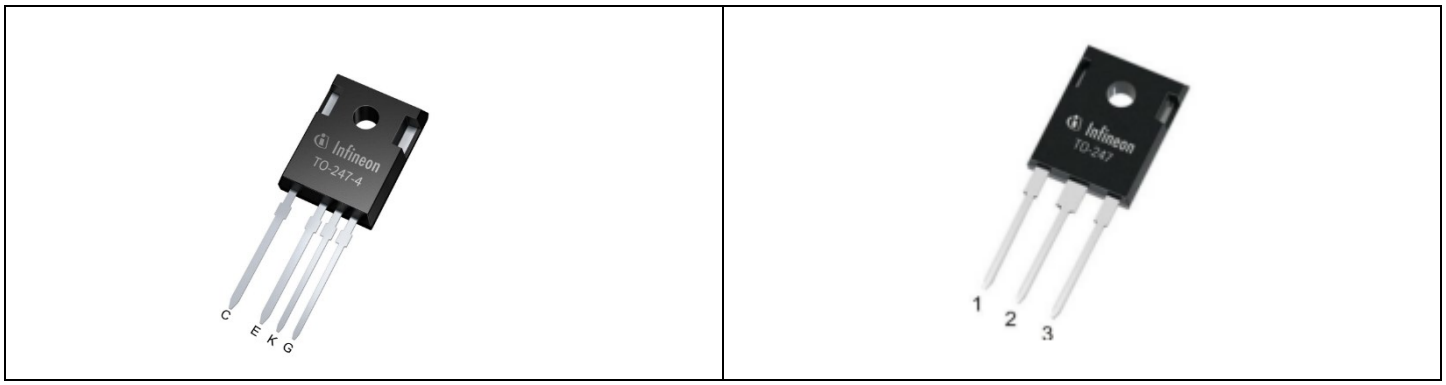


Figure 11 **IKZA40N120CH7 and IDW20G120C5B**

IKZA40N120CH7 is a TRENCHSTOP™ IGBT7 H7 discrete in a TO-247-4pin package technology. It has been developed for applications that focus on decarbonization such as solar photovoltaic, uninterruptible power supplies, and battery chargers.

IDW20G120C5B is a part of the CoolSiC™ Schottky diode generation 5 1200 V, 20 A in a TO-247-3 package. It presents a leading-edge technology for SiC Schottky barrier diodes. The expanded 8.7 mm creepage and clearance distances in the new package offer extra safety in environments with high pollution. Other than negligible switching losses – a signature feature of the SiC Schottky – the CoolSiC™ generation 5 offers best-in-class forward voltage (V_F), the slightest increase of V_F with temperature, and highest surge-current capability. The result is a series of products that deliver market-leading efficiency and higher system reliability at an attractive cost point.

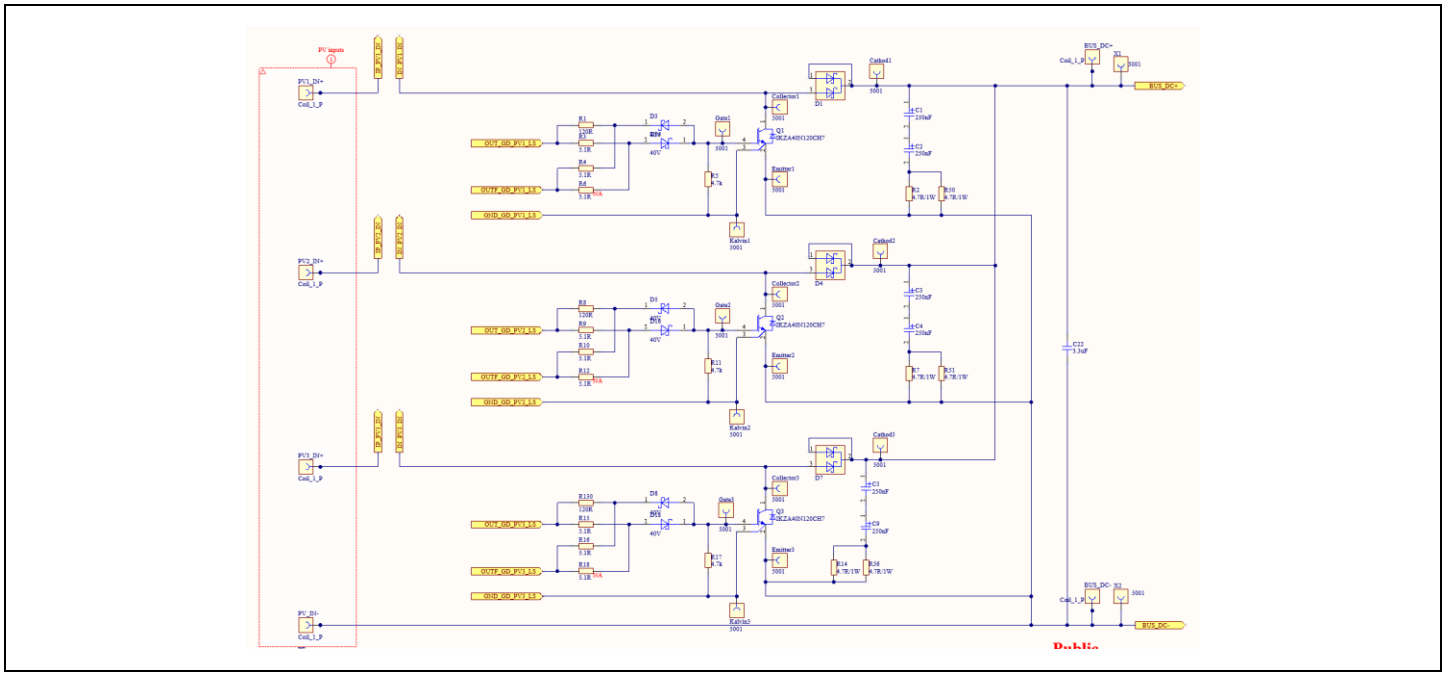


Figure 12 **Functional block diagram of the power stage**

2.1.2 Gate driver

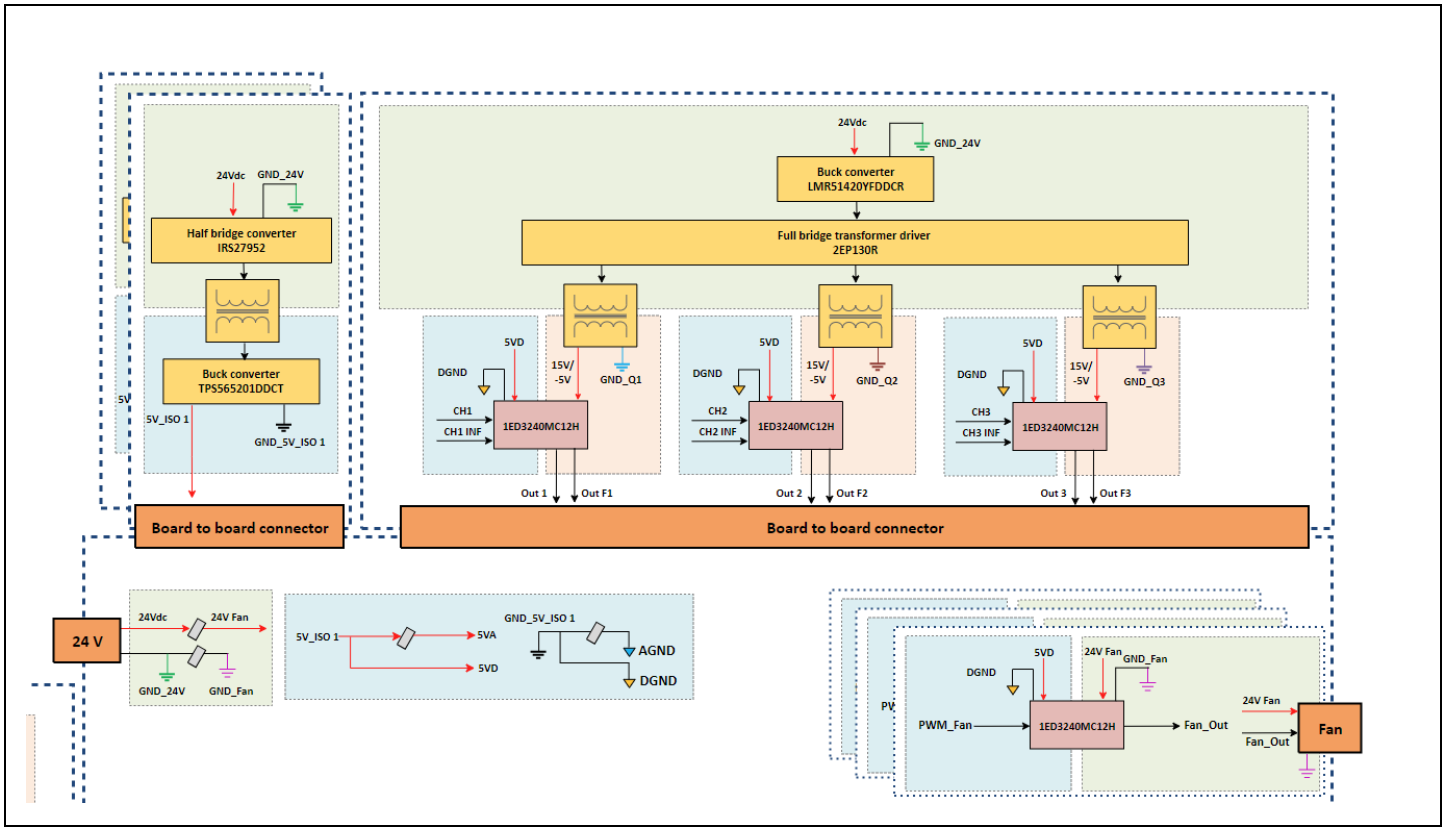


Figure 13 **Functional block diagram of the gate driver card**

Three 1ED3240MC12H single-channel isolated gate drivers are used to drive the three IGBTs.

Figure 14 **1ED3240MC12H**

1ED3240MC12H belongs to the EiceDRIVER™ 2L-SRC Compact 1ED32xx family. It is a single-channel isolated gate driver with two-level slew-rate control (2L-SRC) and a typical sinking and sourcing peak output current of 10 A. It comes in a DSO-8 wide-body package with large creepage distance (> 8 mm) for IGBTs, MOSFETs, and SiC MOSFETs. 1ED3240MC12H offers two separate outputs with 10 A typical peak output current to control two independent gate resistances for both turn-on and turn-off thus enabling two-level slew-rate control. This gate driver can operate over a wide range of supply voltages, both unipolar and bipolar.

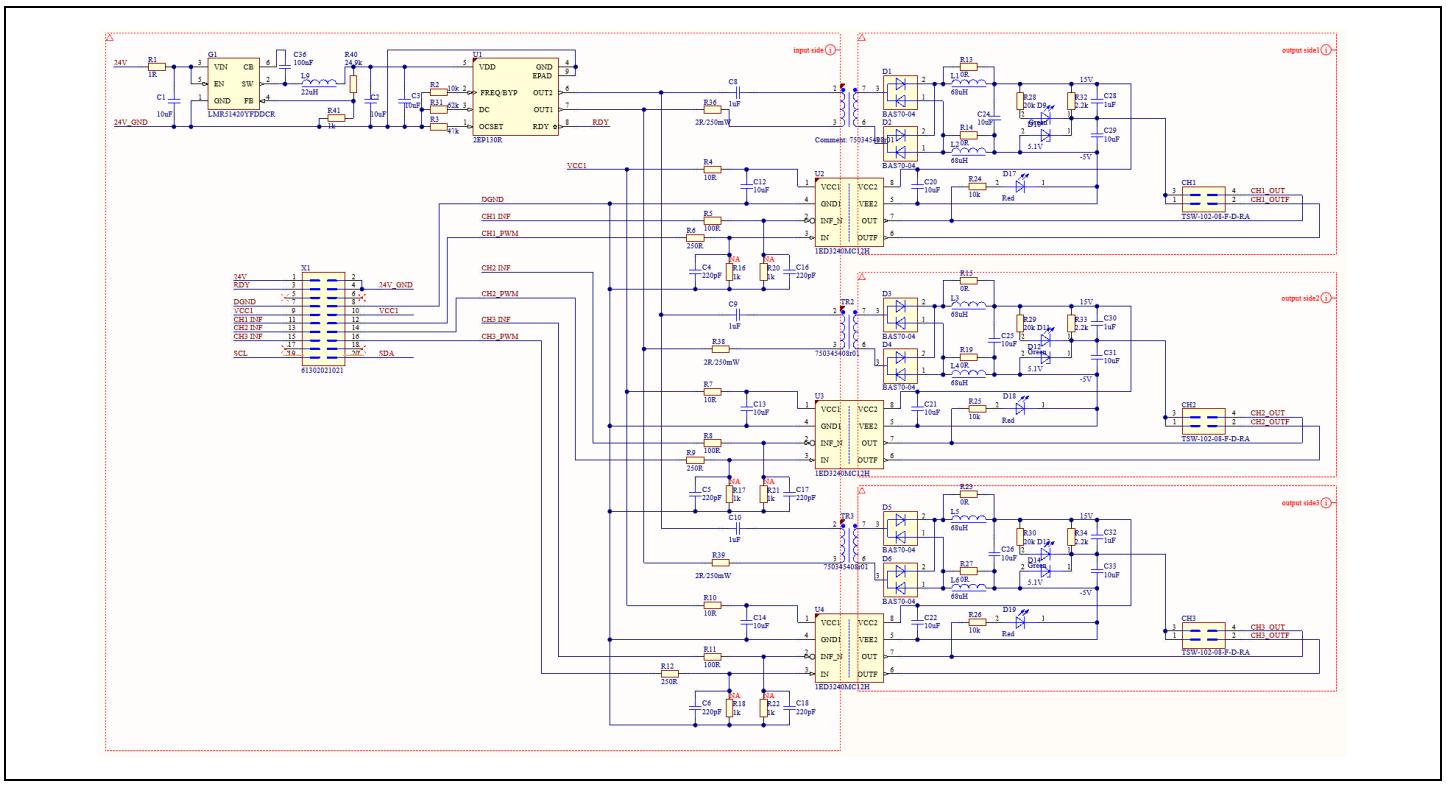


Figure 15 **Gate driver card**

The 24 V voltage and the PWM signals that come from the power board are used as an input for the gate drive card. This voltage is then stepped down and used as an input for the 2EP130R full-bridge transformer driver. A transformer provides functional isolation and the voltages 15 V and -5 V are generated on the rectifier side. These are used as the positive and negative voltage for driving the IGBTs on the power board. The gate resistors are located on the power board.

The two-level slew rate control provides different on and off gate resistors depending on the control signal sent to the INF pin. This also gives users more flexibility to optimize the design. The usual use cases can be seen in Figures 16, 17, and 18.

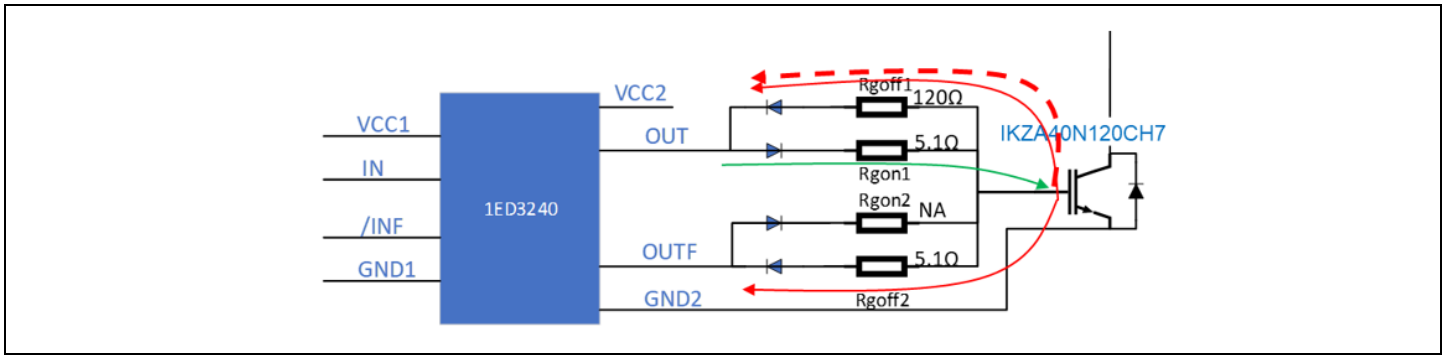


Figure 16 **Schematic implementation of the usual two-level slew-rate control gate-drive**

This flexibility can be utilized to increase the value of the turn-off resistor during abnormal conditions, such as when an overcurrent fault is detected by the current sensor. Increasing the value of the turn-off resistor leads to a slower turn-off during fault conditions. Figure 17 shows how this soft turn-off can be implemented. During the implementation, ensure that the INF signal becomes lower than the IN signal when the PWM kill signal arrives. For this, use a combination of logic gates and an RC filter with a larger time constant on the IN pin.

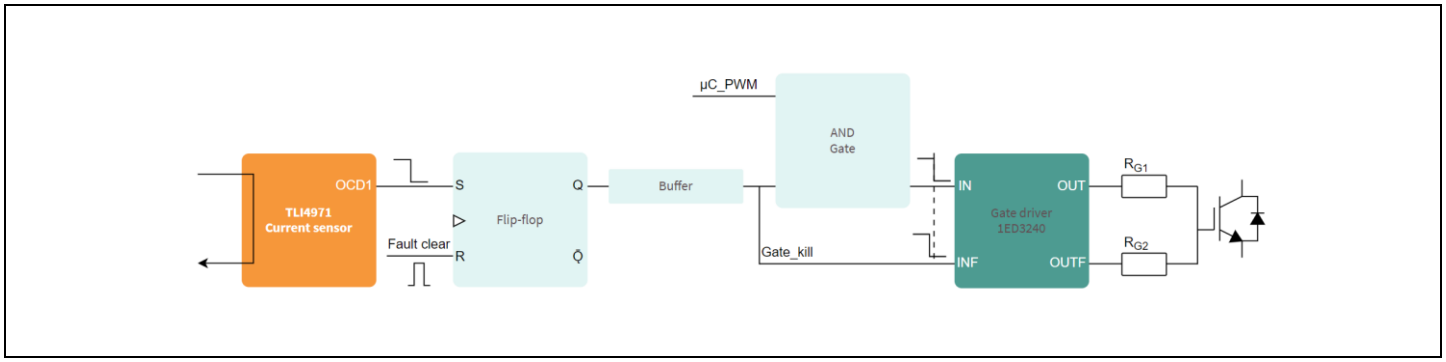


Figure 17 **Soft turn-off implementation**

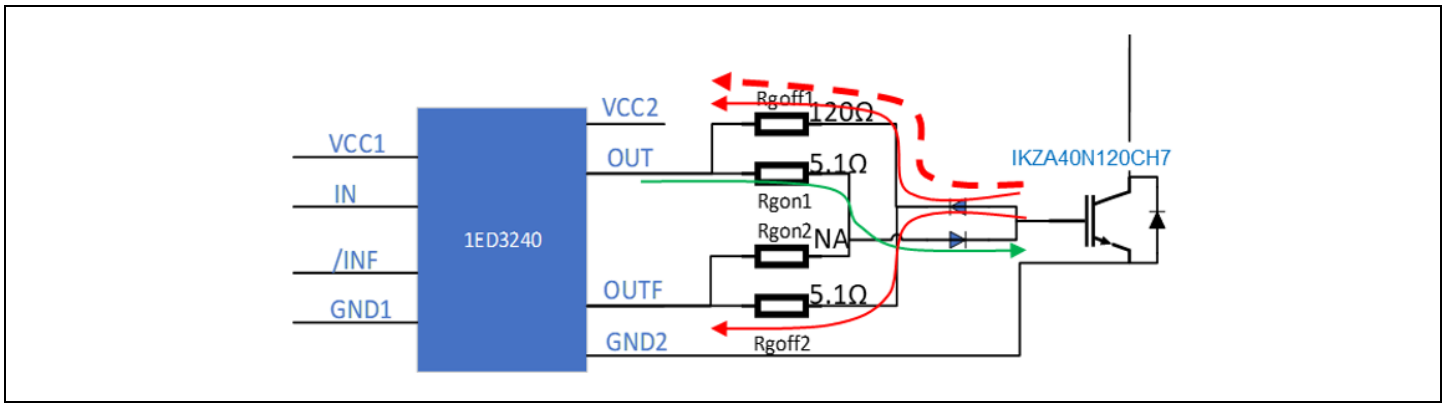


Figure 18 **Two-level slew-rate control gate driver implementation**

During normal operation:

- /INF = High (OUTF is enabled at turn-off and disabled at turn-on)
- R_{gon} = 5.1 Ω and R_{goff} = 5.1 Ω//120 Ω = 4.89 Ω

During abnormal turn-off:

- /INF = Low (OUTF is disabled at turn-off and enabled at turn-on)
- R_{gon} = 5.1 Ω and R_{goff} = 120 Ω

2.1.3 Internal auxiliary power supplies

Users must provide an external voltage supply of 24 V to the power board. This voltage is fed to a power supply card that generates an isolated 5 V. Both 24 V and the isolated 5 V are then fed to the gate driver card that generates the isolated 15 V/-5 V needed to drive the IGBTs.

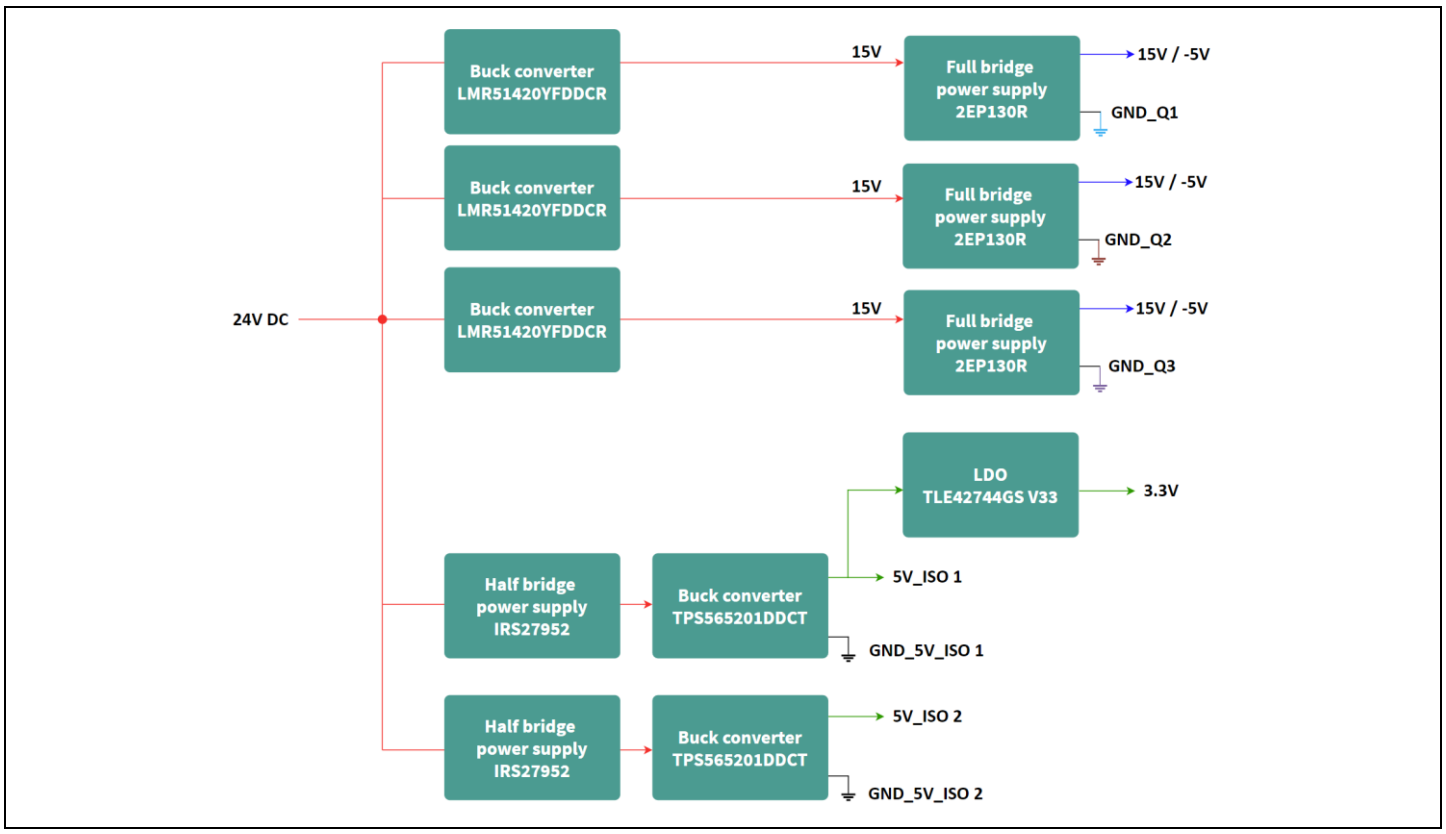


Figure 19 **Auxiliary power supply tree**

The specifications of the auxiliary power supply card are listed in Table 3.

Table 3 Specifications of the auxiliary power supply card

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	21.6	24	26.4	V_{dc}
Input current			0.5	A
Output voltage	4.75	5	5.25	V_{dc}
Output current	0		2	A
Switching frequency		226		kHz
Half bridge IC used	IRS27952			-
Isolation	Reinforced isolation			

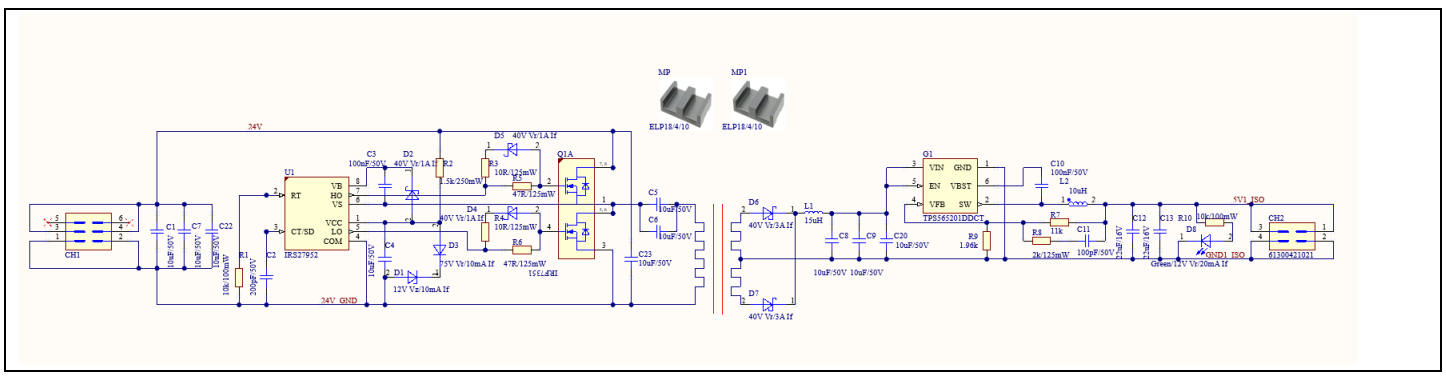


Figure 20 **Schematics of the auxiliary power supply card**

2.1.4 Sensing and protection

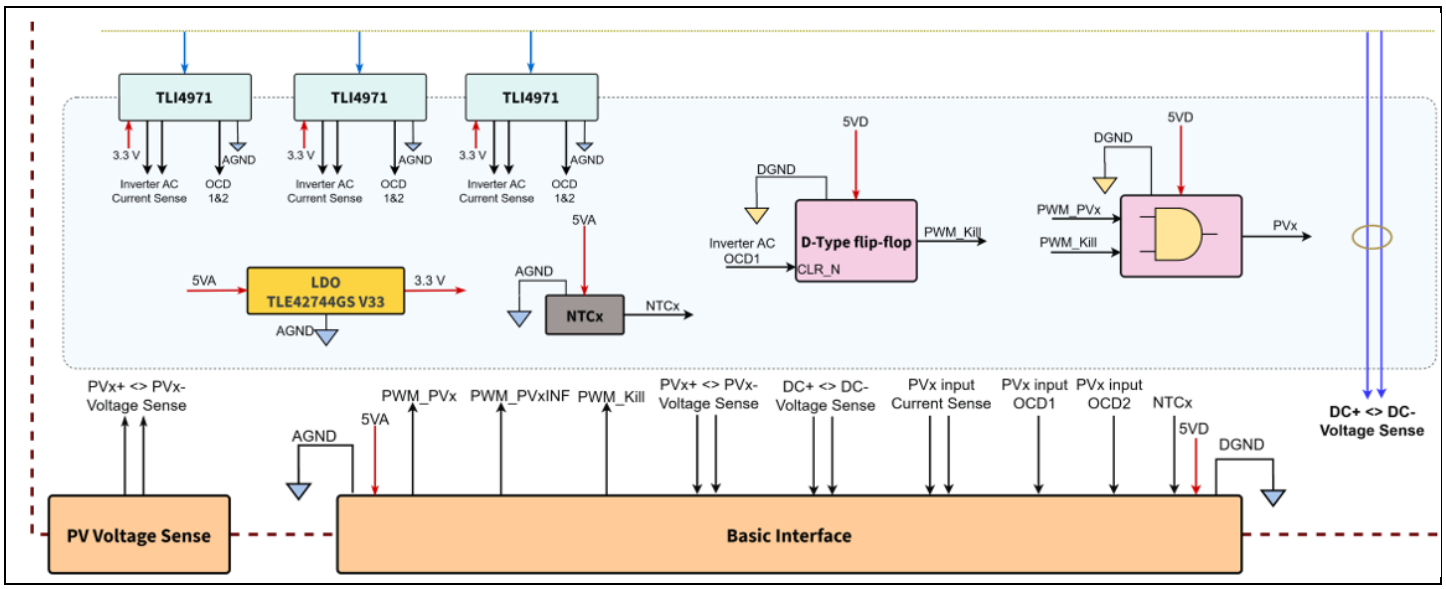


Figure 21 **Functional block diagram of the measurement signals**

2.1.4.1 Current sense

The inductor currents are sensed using the TLI4971 current sensor.

XENSIV™ TLI4971-A120T5-U-E0001 is an Infineon high-precision, miniature coreless magnetic current sensor for AC and DC measurements. It has an analog interface and dual fast overcurrent detection outputs. The two overcurrent detection (OCD) pins are used to implement protection at both hardware and software levels.

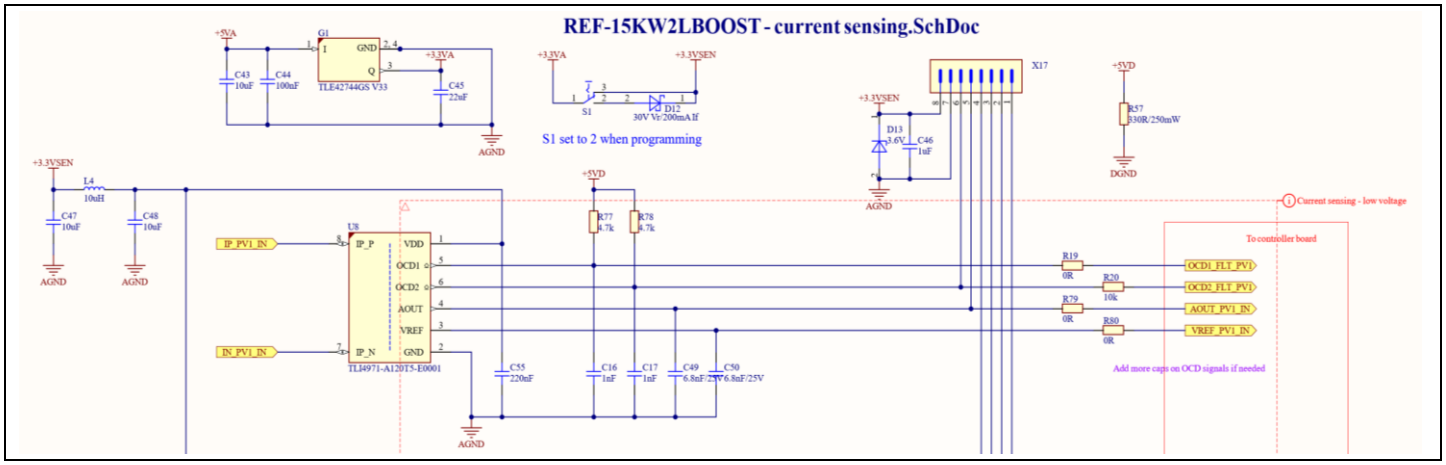


Figure 22 **The current sense circuits**

One way to reprogram the current sensor if needed is by using the XENSIV™ - TLI4971, TLE4972 current sensor programmer board. Details are provided in the board's user guide.

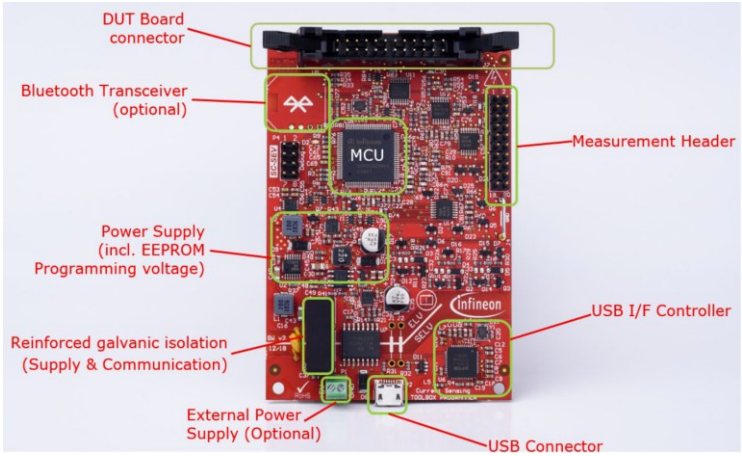


Figure 23 **Current sensor programmer board**

The current sensor programmer board should be connected to a PC and the DUT board connector should be connected with the power board.

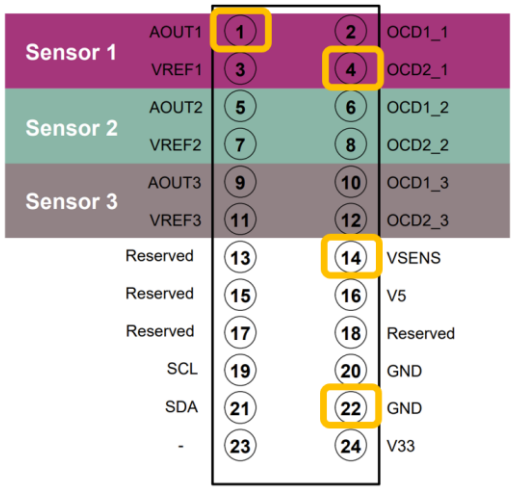


Figure 24 **DUT board connector on the programmer board**

Figure 25 show the two connectors that have to be interfaced together on the programming board and the power board. Make the following connections:

- Connect X17 pin 7 to GND of the DUT board connector
- Connect pin 8 to VSENS
- Connect X17 pin 1 to pin 6 to provide the pins AOUT and OCD2 of all three devices according to the schematic in Figure 22.

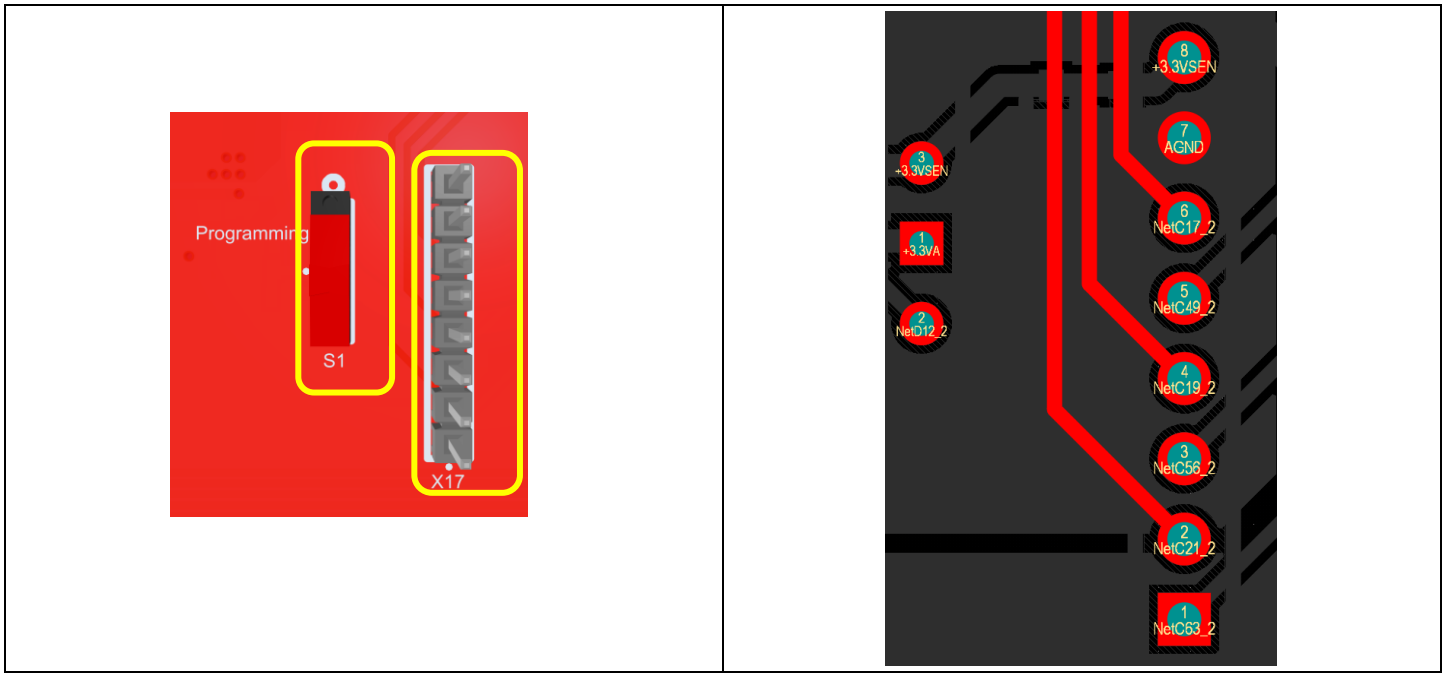


Figure 25 **Current sensor programming connector on the power board**

Steps to reprogram the current sensor are as follows:

1. Connect the programmer board with X17 on the power board and also with a USB cable to the PC.
2. Place switch S1 in programming mode.
3. Start the TLI4971 programming software.
4. In the GUI, go to Memory and then choose Basic Configuration.
5. Set all the data and then click Burn EEPROM.
6. Repeat steps 1 – 5 to program the other current sensors.
7. Remove all the connections.
8. Place switch S1 back into the default mode.

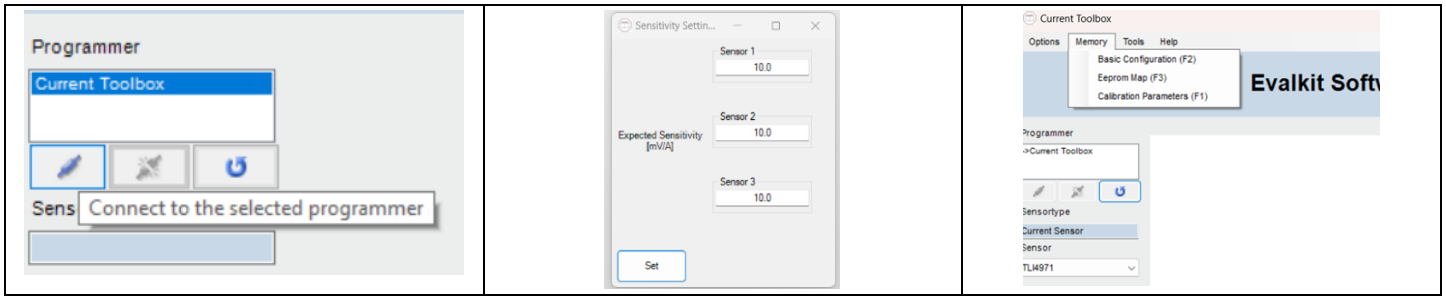


Figure 26 **GUI for the current sensor**

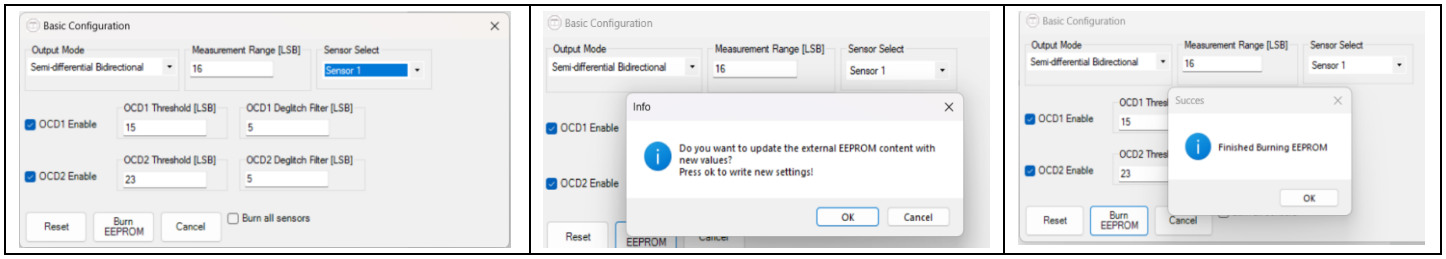


Figure 27 **GUI for the current sensor**

2.1.4.2 Voltage sense

The DC-link voltages are measured on the power board. The voltage at the input of each boost channel is measured on the filter board. Both measurements are taken using voltage dividers.

WARNING: The controller board must be connected to the main power board before the DC bus is powered up. Failure to do so can lead to a hazardous situation.

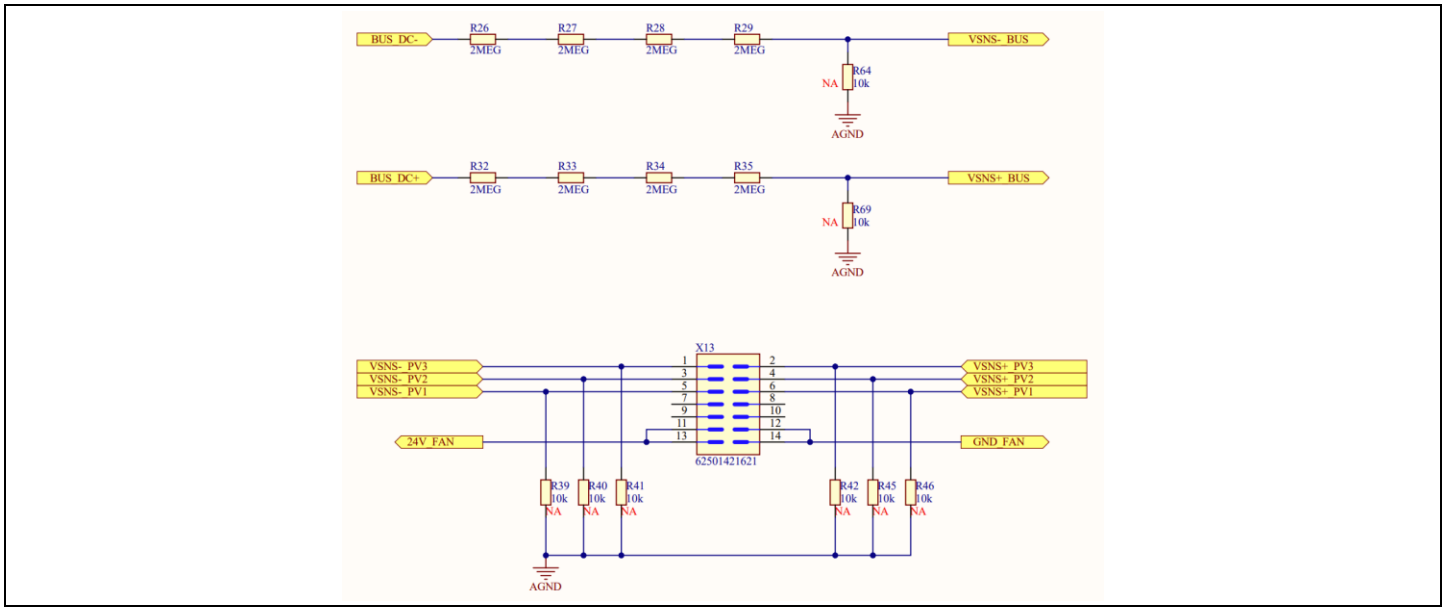


Figure 28 **Voltage sensing circuits**

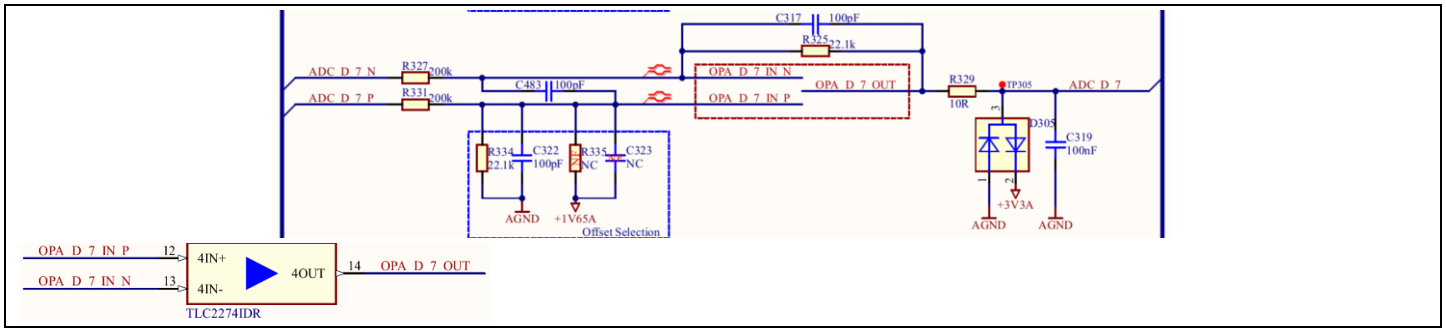


Figure 29 **The signal conditioning circuit used on the control board**

2.1.4.3 Temperature sense

Three temperature measurements are provided on the board using NTCs. The NTC used is B57703M0502A006.

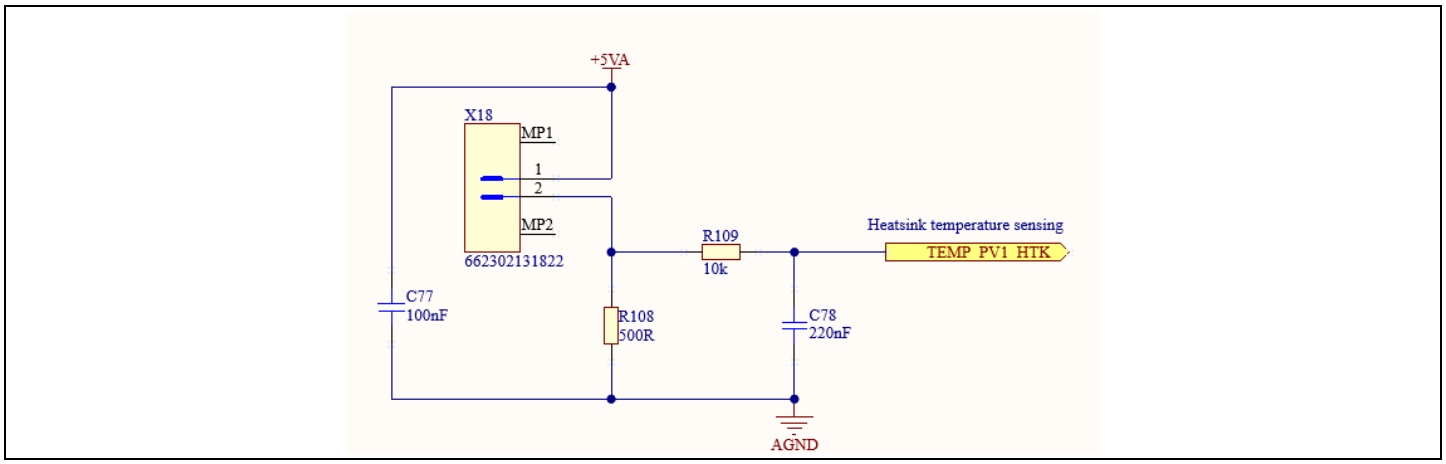


Figure 30 **Temperature sensing circuit**

Table 4 lists the voltage versus temperature values for the temperature sensing circuit.

Table 4 Voltage versus temperature

T (°C)	R (Ω)	Interface voltage (V)
-40	169157	0.014735614
-35	121795	0.020442373
-30	88766	0.028006184
-25	65333	0.037974876
-20	48614	0.050901983
-15	36503	0.06756209
-10	27680	0.088715401
-5	21166	0.115388166
0	16330	0.148544266
5	12696	0.189451349
10	9951	0.239211559
15	7855	0.299222023
20	6246	0.370589979
25	5000	0.454545455
30	4029	0.551998234
35	3266	0.663834307
40	2665	0.789889415
45	2186	0.930752048
50	1803	1.085540599
55	1495	1.253132832
60	1247	1.431024614
65	1044	1.619170984

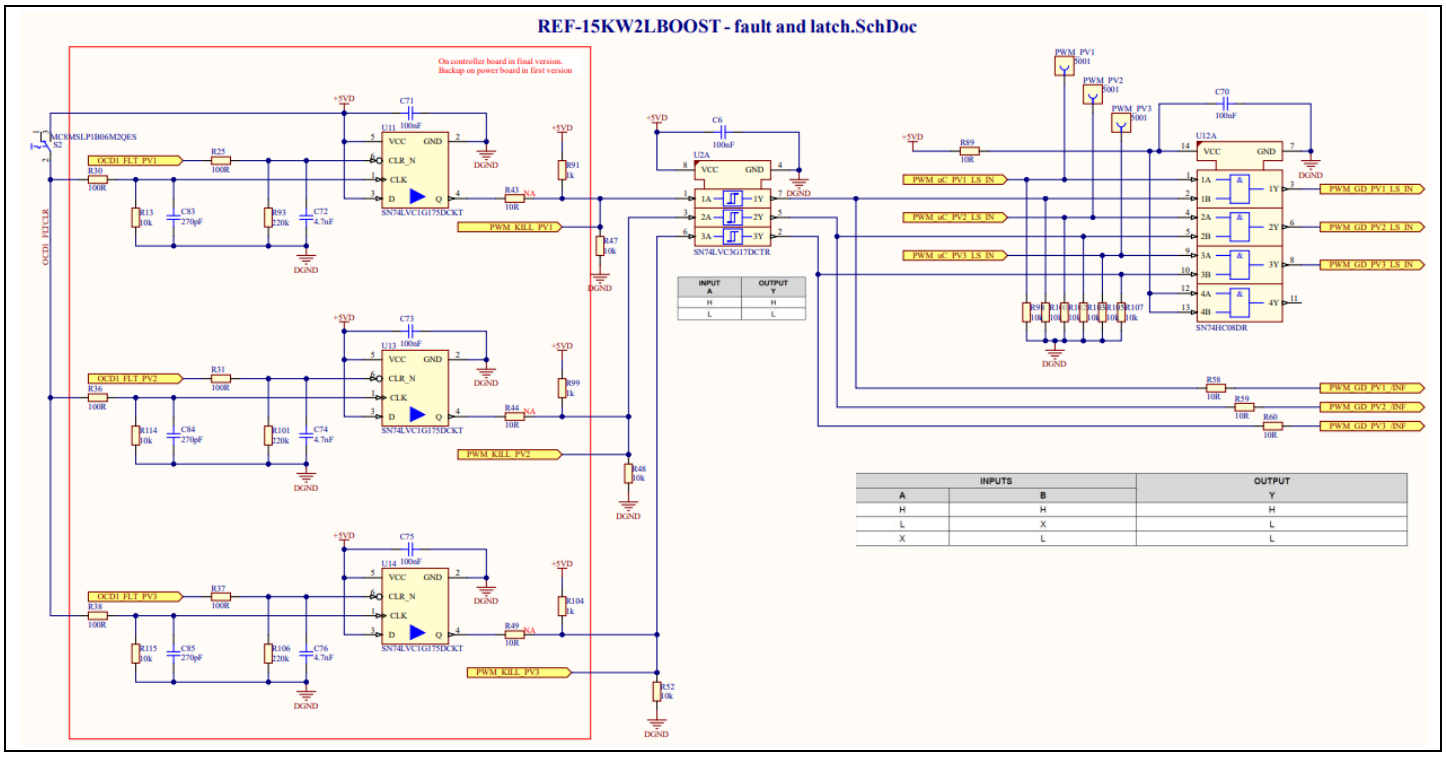
70	878.9	1.813039379
75	743.1	2.011101279
80	631	2.210433245
85	538.2	2.40801387
90	460.8	2.601998335
95	396.1	2.789867202
100	341.8	2.969826562
105	296.2	3.139914594

2.1.4.4 Fault and latch circuit

Fault and latch circuits are provided to disable the PWMs in the case of a fault event. Figure 31 shows a fault and latch circuit for REF-15KW2LBOOST.

TLI4971 has two levels of overcurrent threshold settings – OCD2 for the lower threshold and OCD1 for the higher threshold. OCD1 is usually used to protect from a short-circuit event. Once OCD1 is triggered, the output of the D-type flip-flop SN74LVC1G175DCKT will turn to a low state to shut down the PWM signal permanently.

The same OCD1 protection circuit is integrated into the controller board. Consequently, the identical function on the main power board is not utilized by desoldering R43, R44, and R49.



The SN74LVC1G175 device has an asynchronous clear ($\overline{CLR}$) input. When $\overline{CLR}$ is high, data from the input pin (D) is transferred to the output pin (Q) on the clock's (CLK) rising edge. When $\overline{CLR}$ is low, Q is forced into the low state, regardless of the clock edge or data on D.

Table 1. Function Table

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
H	↑	L	L
H	↑	H	H
H	H or L	X	Q_0
L	X	X	L

PIN		I/O	
NAME	NO.		
CLK	1	I	Clock Input
$\overline{CLR}$	6	I	Clear Data Input
D	3	I	Data Input
GND	2	—	Ground
Q	4	O	Output
V_{CC}	5	—	Power

Figure 31 **Fault and latch circuit**

2.1.5 Fan control

A fan comes with the power board. The fan's duty cycle can be controlled by the GUI and ambient temperature.

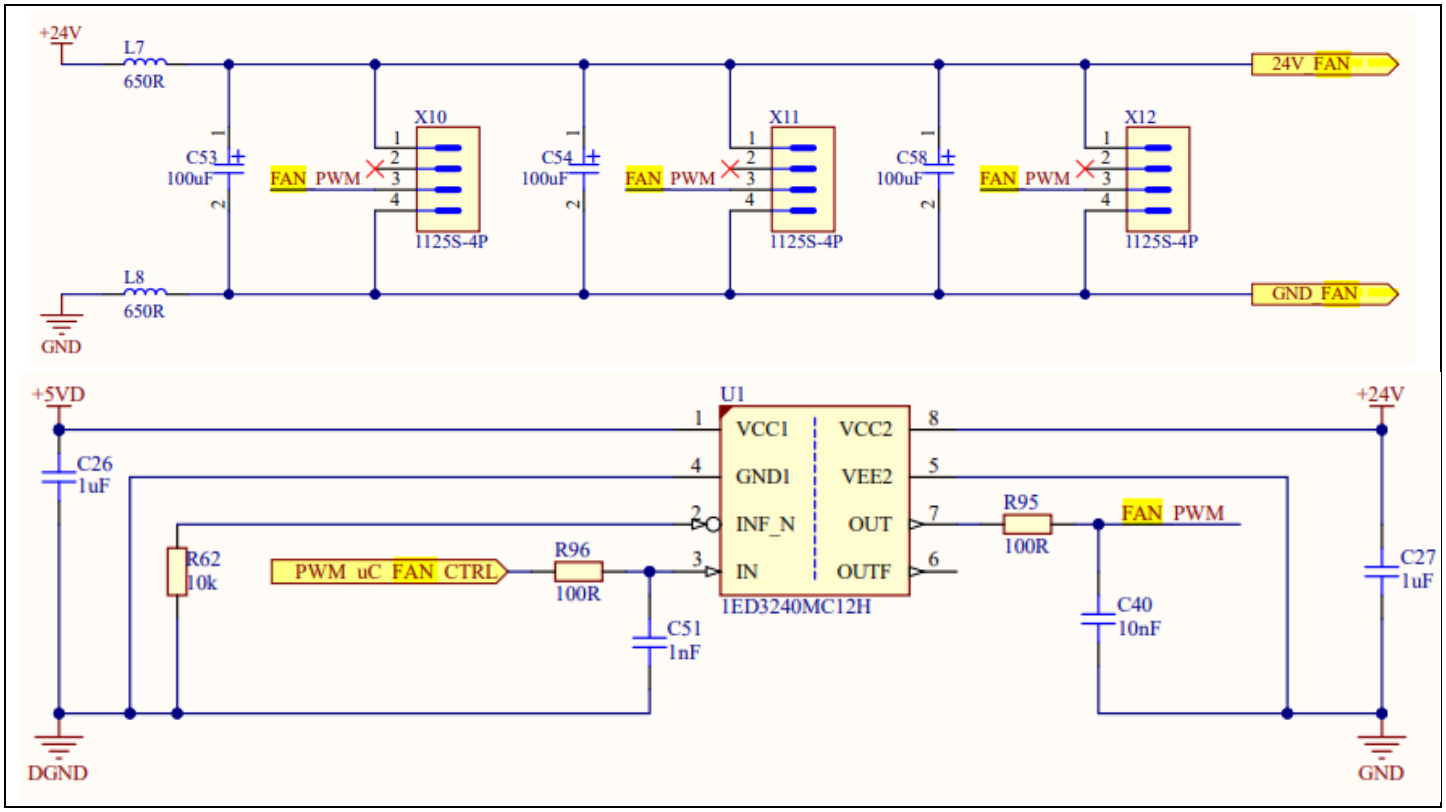


Figure 32 **Fan control circuits**

2.1.6 Connectors

2.1.6.1 Signal connectors

2.1.6.1.1 Input voltage sense interface

The input voltage is measured on the filter board and is transferred to the power board through the X13 connector. The signals are shown in Figure 33.

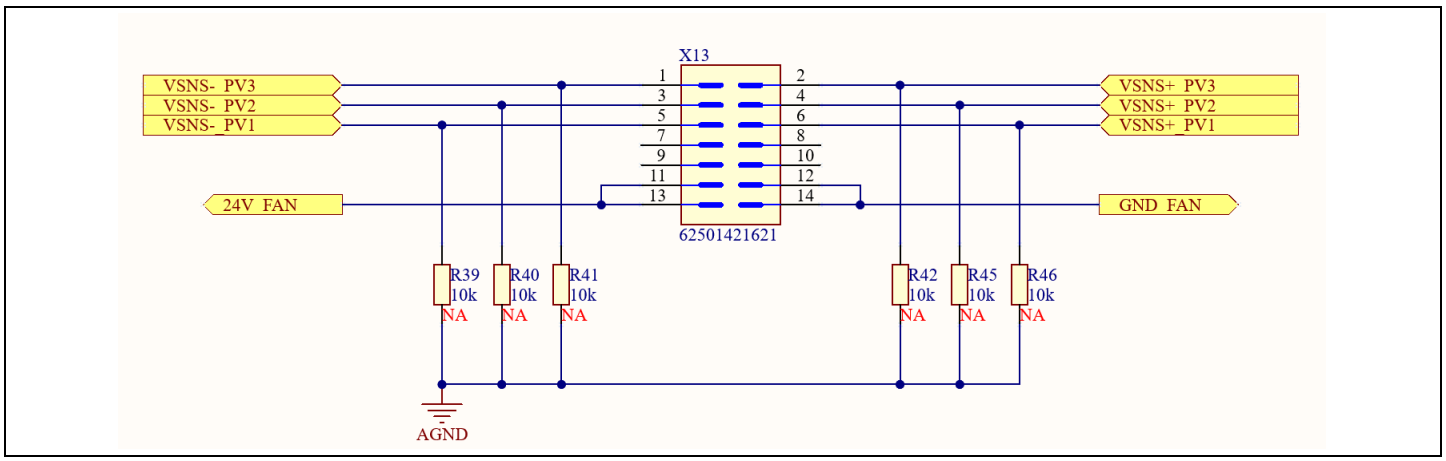


Figure 33 **Input voltage sense interface**

Note: The filter board must be connected to the power board before applying voltage on the input.

Table 5 Input voltage sense interface

Input voltage sense interface		
Pin	**Signal**	**Description**
1	VSNS- PV3	PV3 voltage N
2	VSNS+ PV3	PV3 voltage P
3	VSNS- PV2	PV2 voltage N
4	VSNS+ PV2	PV2 voltage P
5	VSNS- PV1	PV1 voltage N
6	VSNS+ PV1	PV1 voltage P
7	NC	NC
8	NC	NC
9	NC	NC
10	NC	NC
11	24V FAN	24 V used for powering up the fans on the filter board
12	GND FAN	24 V ground
13	24V FAN	24 V used for powering up the fans on the filter board
14	GND FAN	24 V ground

2.1.6.1.2 Basic interface

The X16 connector contains all the signals that are required for controlling the three-channel boost converter. It can also be interfaced with the control board REF-CLBXMC7PEC that has the same connector under the name Basic interface. The signals of the basic interface are shown in Figure 34.

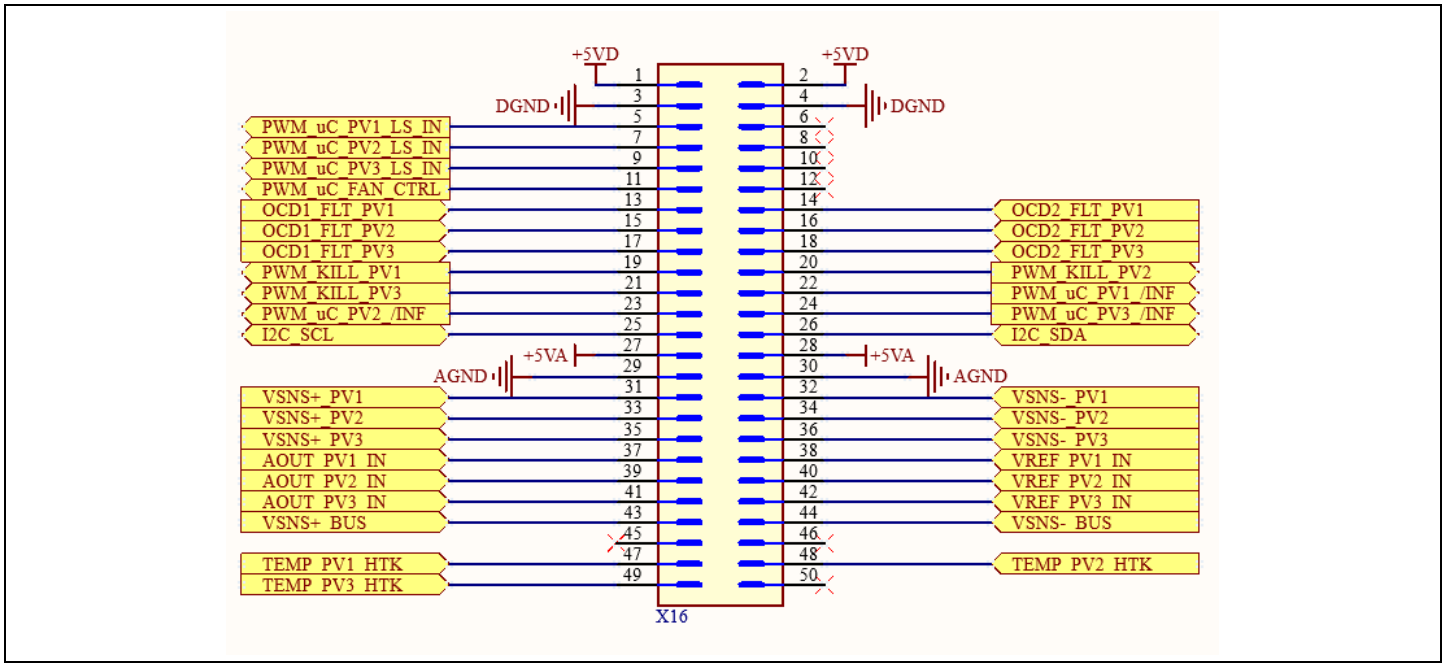


Figure 34 **Basic control interface**

Table 6 Basic interface signals

Basic interface		
Pin	**Signal**	**Description**
1	+5VD	Digital power
2	+5VD	Digital power
3	DGND	Digital power
4	DGND	Digital power
5	PWM_uC_PV1_LS_IN	PV 1 PWM
6	NC	NC
7	PWM_uC_PV2_LS_IN	PV 2 PWM
8	NC	NC
9	PWM_uC_PV3_LS_IN	PV 3 PWM
10	NC	NC
11	PWM_uC_FAN_CTRL	PV fan control
12	NC	NC
13	OCD1_FLT_PV1	PV1 current sensor ODC1
14	OCD2_FLT_PV1	PV1 current sensor ODC2
15	OCD1_FLT_PV2	PV2 current sensor ODC1
16	OCD2_FLT_PV2	PV2 current sensor ODC2

17	OCD1_FLT_PV3	PV3 current sensor ODC1
18	OCD2_FLT_PV3	PV3 current sensor ODC2
19	PWM_KILL_PV1	PV 1 PWM kill
20	PWM_KILL_PV2	PV 2 PWM kill
21	PWM_KILL_PV3	PV 3 PWM kill
22	PWM_uC_PV1_/INF	PV1 gate driver control
23	PWM_uC_PV2_/INF	PV2 gate driver control
24	PWM_uC_PV3_/INF	PV3 gate driver control
25	I2C_SCL	Gate driver config (if required)
26	I2C_SDA	Gate driver config (if required)
27	+5VA	Analog power
28	+5VA	Analog power
29	AGND	Analog power
30	AGND	Analog power
31	VSNS+_PV1	PV1 voltage P
32	VSNS-_PV1	PV1 voltage N
33	VSNS+_PV2	PV2 voltage P
34	VSNS-_PV2	PV2 voltage N
35	VSNS+_PV3	PV3 voltage P
36	VSNS-_PV3	PV3 voltage N
37	AOUT PV1 IN	PV1 current P
38	VREF PV1 IN	PV1 current N
39	AOUT PV2 IN	PV2 current P
40	VREF PV2 IN	PV2 current N
41	AOUT PV3 IN	PV3 current P
42	VREF PV3 IN	PV3 current N
43	VSNS+ BUS	Bus voltage P
44	VSNS- BUS	Bus voltage N
45	NC	NC
46	NC	NC
47	TEMP PV1 HTK	PV1 temperature
48	TEMP PV2 HTK	PV2 temperature
49	TEMP PV3 HTK	PV3 temperature
50	NC	NC

2.1.7 Isolation coordination

The 15 kW boost converter follows a hot-side control structure where all the measurements and gate-drive power supply offer functional isolation. There are two microcontrollers on the REF-CLBXMC7PEC control board:

- XMC7200 is located on the hot side and controls the converter
- CY8C58LP is located on the cold side. It is separated from the main micro-controller by digital isolators for debugging purposes.

IEC 62109-1 is used for clearance and creepage requirements.

3 Converter control design

3.1 Converter topology and its switching strategy

3.1.1 Introduction to the three-channel DC-DC boost converter

REF-15KW2LBOOST has a three-leg or three-channel interleaved DC-DC boost converter. The circuit diagram for the three-phase interleaved boost converter is shown in Figure 35. Parasitic circuits of the inductor and capacitor have been ignored. The switch and diode are assumed to be ideal devices for further mathematical analysis.

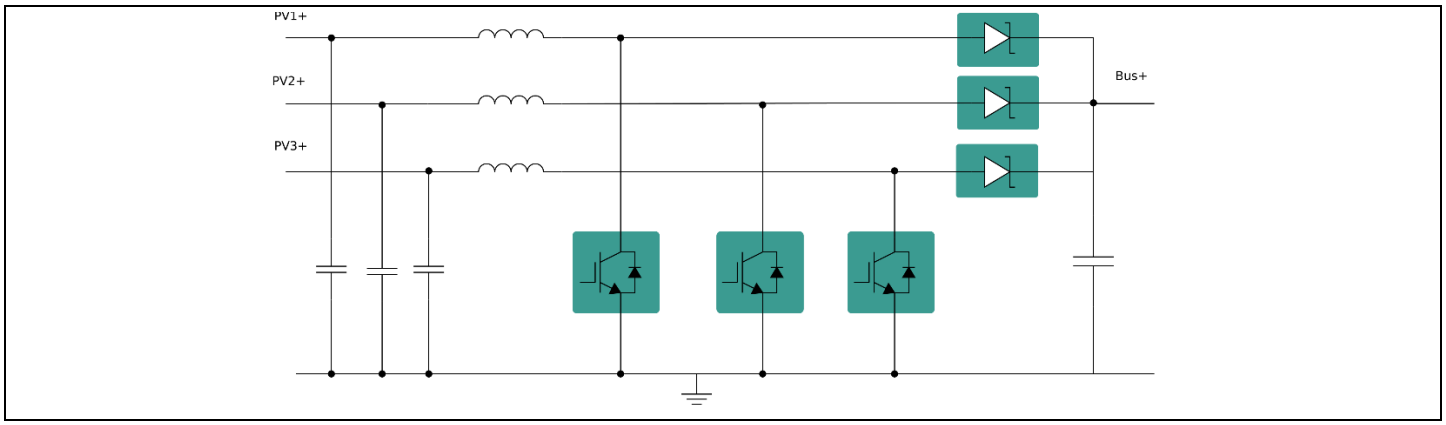


Figure 35 **Circuit diagram of an interleaved boost converter**

3.1.2 Principle of an interleaved boost operation

The operation of a three-channel interleaved boost converter involves three individual boost converter stages working together in parallel but with a phase shift between them.

Each channel of the interleaved boost converter operates with a specific phase shift (360/n, where n is the number of phases) relative to others that have the same duty ratio. Typically, the channels are spaced evenly at 120-degree intervals, ensuring that the current pulses are distributed evenly overtime, as shown in Figure 36.
Fundamentally, each phase of the converter will operate in the same manner as the conventional boost converter.

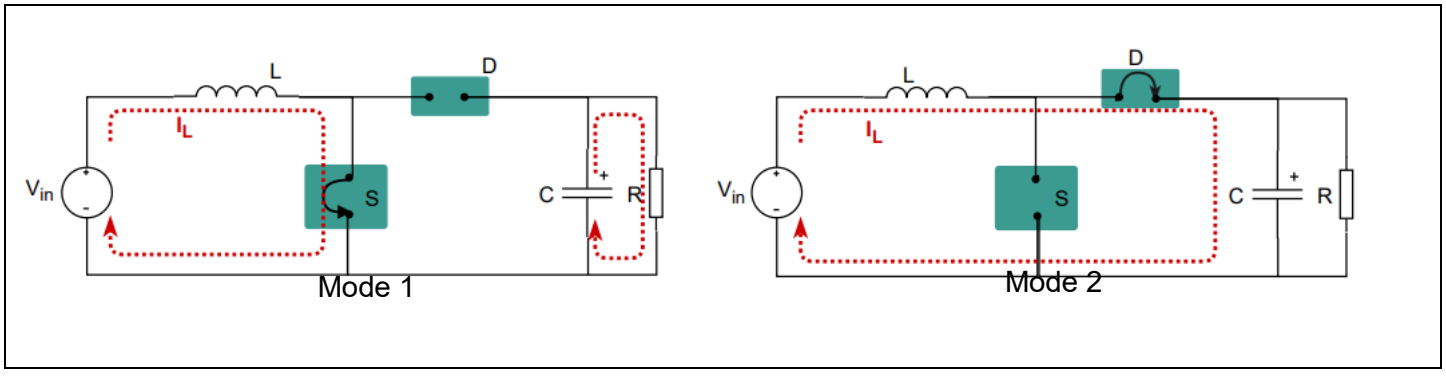


Figure 36 **Operating modes of a conventional boost converter**

Mode 1: When the switch is on, the inductor enters the charging process. During this time, the switch in the circuit diagram can be replaced by a wire, and the diode is equivalent to an open circuit. The power supply charges the inductor and the charging current remains basically unchanged. At the same time, the voltage on the capacitor supplies power to the load. As the capacitor is very large, the output voltage also remains mostly unchanged.

Mode 2: When the switch is closed, current flows through the inductor. It is the nature of inductance to resist changes in the current flow. Therefore, when the switch opens, the inductor current continues to flow and takes the only pathway available – through the diode.

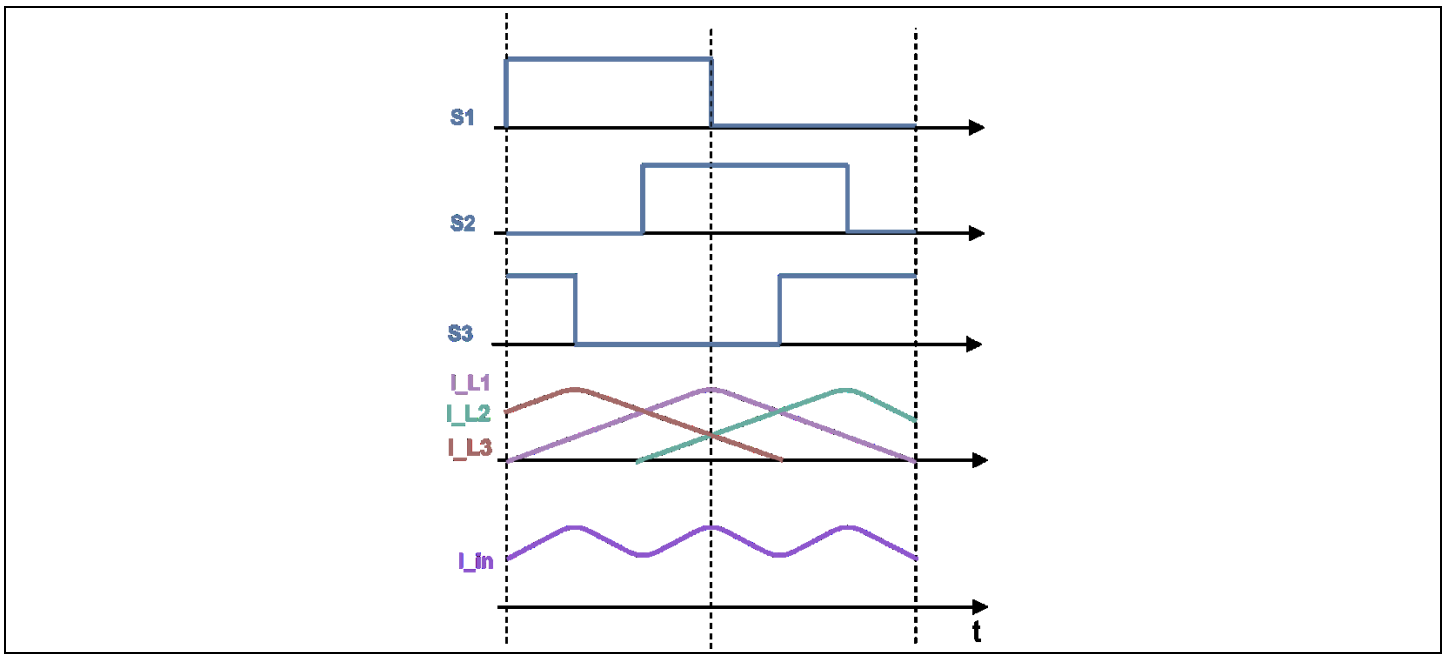


Figure 37 **Inductor current waveforms with a duty ratio D = 0.5**

3.2 Control mode and control loop design

3.2.1 Introducing the control mode

The implementation of a controlling two-level boost converter comprises four control modes as shown in Figure 38.

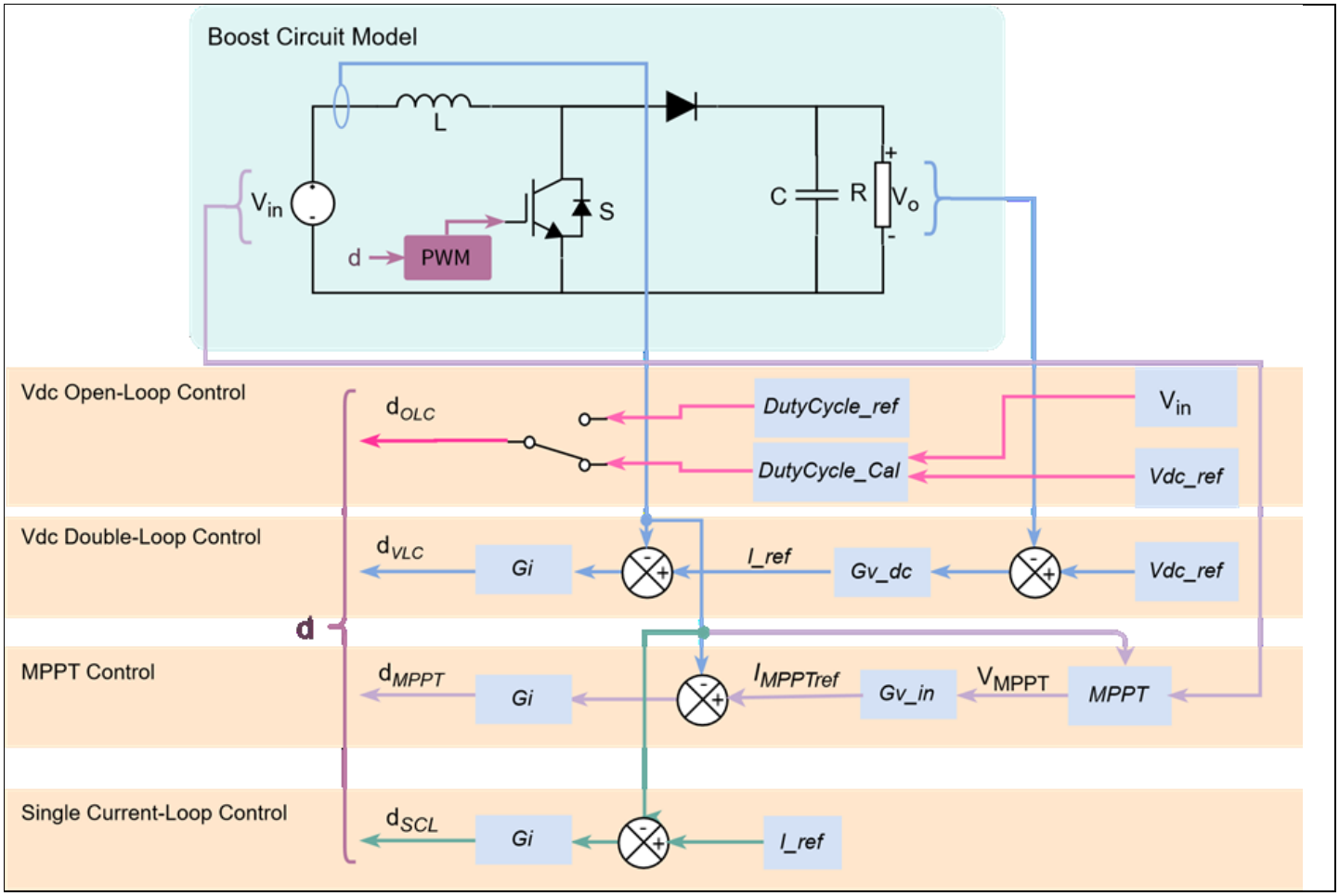


Figure 38 **The overall control block diagram**

The detailed explanation of the algorithm of every control loop of the interleaved boost converter is discussed in the following sections.

3.2.2 Control loop and algorithm

Vdc open-loop control

In the V_{dc} open-loop control, the interleaved boost converter operates without feedback from the output to the input, resulting in an unregulated output voltage. To achieve a desired output voltage, a referenced duty cycle is required. It is typically calculated based on the desired output voltage (V_o) and the input voltage (V_{in}). The duty cycle is set to a predetermined value, allowing the boost converter to produce an output voltage close to the desired value.
For open-loop control of the output voltage, the boost converter must work in CCM (Continuous Conduction Mode) mode.

The duty cycle can be calculated using the equation:

$$Duty\ ratio, D = \frac{V_o - V_{in}}{V_o}$$

V_{dc} double-loop control design

To design the closed-loop control system of a boost converter, it is necessary to model the dynamic behavior of the converter. The state-space averaging method uses the state-space description of dynamic systems to derive the

small-signal averaged equations of PWM switching converters. In the state-space averaging method, an exact state-space description of the power stage is formulated initially. This description is called the switched-state space model. The power stage dynamics during an ON-time period can be expressed in the form of a state-space equation, as follows:

a. When the switch is ON $(0, dT_s)$:

$$L\frac{di_L(t)}{dt} = v_{in}(t) \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (1)$$

$$C\frac{dv_o(t)}{dt} = -\frac{v_o(t)}{R} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (2)$$

b. When the switch is $(dT_s,\ T_s)$

$$\boldsymbol{L\frac{di_L(t)}{dt} = v_{in}(t) - v_o(t)} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (\mathbf{3})$$

$$C\frac{dv_o(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (4)$$

The switching function is introduced. q(t) is periodic with a period equal to the switching period and its cyclic average value gives a discrete sequence that is the same as the duty ratio sequence.

$$q(t) = \begin{cases} 1, & t = (0, dT_s] \\ 0, & t = (dT_s,\ T_s] \end{cases}$$

Duty ratio function, $d(t) = \frac{1}{T_s}\int_{t-T_s}^{t} q(t)dt$

Using this switching function, the two state-space descriptions given earlier can be combined into a single state-space equation as follows:

$$L\frac{di_L(t)}{dt} = q(t)v_{in}(t) + \big(1 - q(t)\big)[v_{in}(t) - v_o(t)] \dots\dots\dots\dots\dots\dots\dots (5)$$

$$C\frac{dv_o(t)}{dt} = -q(t)\frac{v_o(t)}{R} + (1 - q(t))[i_L(t) - \frac{v_o(t)}{R}] \dots\dots\dots\dots\dots\dots\dots (6)$$

Taking the average of equations 5 and 6,

$$L\frac{d\overline{i_L}(t)}{dt} = \overline{v_{in}}(t) - \big(1 - d(t)\big)[\overline{v_o}(t)] \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (7)$$

$$C\frac{d\overline{v_o}(t)}{dt} = \big(1 - d(t)\big)\overline{i_L}(t) - \frac{\overline{v_o}(t)}{R} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (8)$$

The input variables and state variables decompose into the sum of DC components and perturbations, and the small disturbance analysis is carried out as:

$$\frac{d(I_L + \hat{\imath_L})}{dt} = \frac{(V_{in} + \widehat{v_{in}}) - \big(1 - (D + \hat{d})\big)[V_o + \widehat{v_o}]}{L} \dots\dots\dots\dots\dots\dots\dots (9)$$

$$\frac{d(V_o + \widehat{v_o})}{dt} = \frac{\big(1 - (D + \hat{d})\big)(I_L + \hat{\imath_L}) - \frac{V_o + \widehat{v_o}}{R}}{C} \dots\dots\dots\dots\dots\dots\dots (10)$$

When the converter reaches the steady state, the change of inductive current and capacitor voltage can be considered as 0. Now, set the left side of equations 9 and 10 to 0 to obtain the steady state value of each state variable. This can be expressed as:

$$\frac{dI_L}{dt} = 0 \ \& \ \frac{dV_o}{dt} = 0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(11)}$$

From equations 9, 10, and 11, and considering $\widehat{v_{in}} = 0$ because the boost converter is operating in V_{out} control mode, we get:

$$\frac{d\widehat{\iota_L}(t)}{dt} = \frac{-D'\,\widehat{v_o}(t) + \hat{d}(t)V_o}{L} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(12)}$$

$$\frac{d\widehat{v_o}}{dt} = \frac{D'i_L(t) - \frac{\widehat{v_o}(t)}{R} - \hat{d}(t)I_L}{C} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(13)}$$

Where D'=1-D.

The time-domain equation can be transformed into a frequency-domain equation through Laplace transformation:

Current gain with respect to duty ratio $G_{id}(s) = \frac{\hat{\imath}(s)}{\hat{d}(s)}|_{\widehat{v_{in}}(s)=0} = \frac{V_oRCs+2V_o}{RLCs^2+Ls+RD'^2}$

Output voltage gain with respect to duty ratio $G_{vd}(s) = \frac{\hat{v}(s)}{\hat{d}(s)}|_{\widehat{v_{in}}(s)=0} = -\frac{V_{in}}{D'^2}\frac{-RD'^2+Ls}{RLCs^2+Ls+RD'^2}$

Output voltage gain with respect to current $G_{V\_dc}(s) = \frac{\hat{v}(s)}{\hat{\imath}(s)}|_{\widehat{v_{in}}(s)=0} = \frac{RD'^2-Ls}{D'RCs+2D'}$

Current inner-loop design

The most commonly used PI controller is selected as the controller for the current inner-loop. The structure diagram of the current inner-loop is shown in Figure 39.

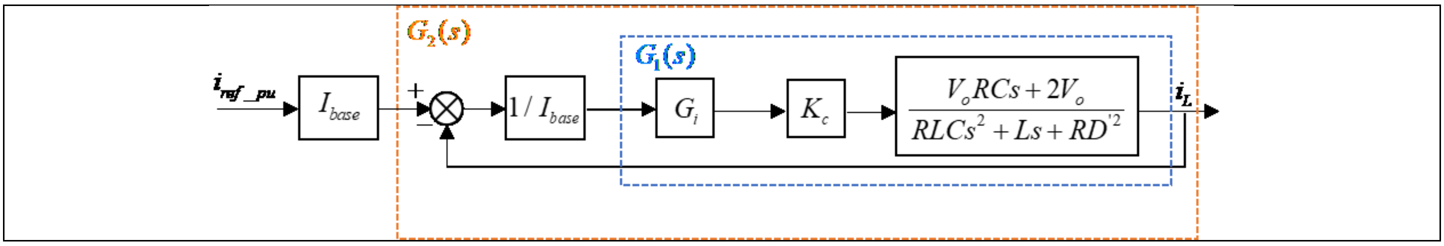


Figure 39 **Structure diagram of the current inner-loop**

$$G_i = k_{pi} + \frac{k_{ii}}{s}$$

After the PI controller is introduced, the open loop transfer function of the inner current loop is given as:

$$G_1 = G_iG_{id}(s) = (k_{pi} + \frac{k_{ii}}{s})\frac{V_oRCs + 2V_o}{RLCs^2 + Ls + RD'^2}$$

The controller is designed by specifying the loop-gain crossover frequency (i.e., 1/20th of the switching frequency) and the required phase margin of 45 degrees. Through this the values of k_{pi} & k_{ii} can be calculated, which come out to be 0.216 and 582.177 respectively.

Voltage outer loop design

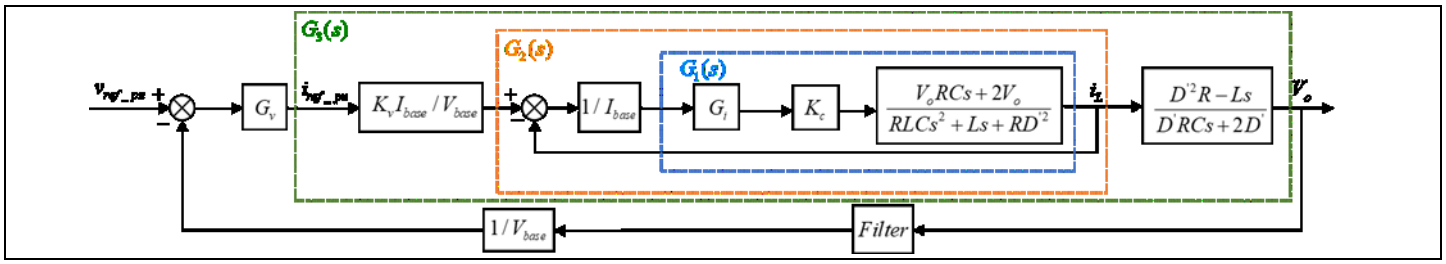


Figure 40 **The voltage-loop control block diagram**

$$G_v = k_{pv} + \frac{k_{iv}}{s}$$

$$G_3(s) = \frac{I_{base}}{V_{base}} G_v(s) G_2(s) G_{vi}(s) = (k_{pv} + \frac{k_{iv}}{s}) G_2(s) \frac{RD'^2 - Ls}{D'RCs + 2D'} \frac{I_{base}}{V_{base}}$$

The controller is designed by specifying the loop-gain crossover frequency (i.e., 1/10th of the switching frequency) and the required phase margin of 45 degrees. Through this the values of k_{pv} and k_{iv} value can be calculated, which comes out to be 8.696 and 3946.98 respectively.

MPPT control loop

Maximum power point tracking (MPPT) is the process for tracking the voltage and current from a solar module to determine the point where the power peaks to extract the maximum power.

In Figure 41, the purple curve is the current-voltage characteristic for a particular solar panel under a specified condition of light incidence. The green curve is of power showing the point where the peak occurs, which is in the knee of the I-V curve (blue dot) at I_{MMP} and V_{MMP}. If the light incidence decreases, the curves shift down.

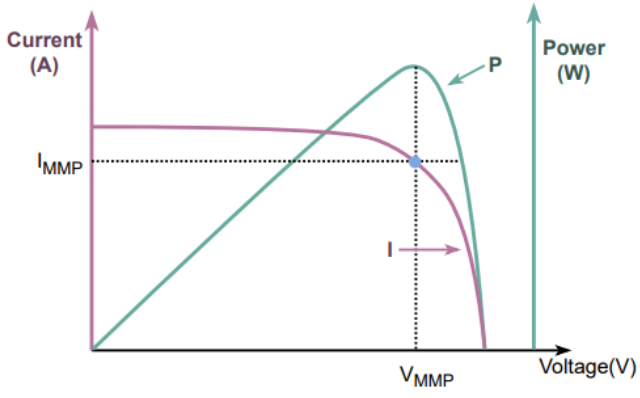


Figure 41 **I-V and P-V characteristics of a particular solar panel**

The output current of a solar module varies directly with the amount of light (irradiance). With changing temperature, the output voltage changes inversely, while the current remains relatively constant.

Maximum power point tracking (MPPT) utilizes an algorithm, which consists of a series of steps or procedures to achieve a specific outcome. One effective method for developing these control strategies is the incremental conductance method. This algorithm uses the instantaneous conductance I/V and the incremental conductance dI/dV for MPPT.

At the peak power point:

$$\frac{dP}{dV}I + V\frac{dI}{dV} = 0$$

$$\frac{1}{V}\frac{dP}{dV} = \frac{1}{V} + \frac{dI}{dV} = 0$$

If the operating point is to the right of the curve:

$$\frac{dP}{dV} < 0, then\ if$$

$$\frac{1}{V} + \frac{dI}{dV} < 0, \qquad V\ is\ decreased$$

$$\frac{1}{V} + \frac{dI}{dV} > 0, \qquad V\ is\ increased$$

If the operating point is to the right of the curve:

$$\frac{dP}{dV} > 0, then\ if$$

$$\frac{1}{V} + \frac{dI}{dV} > 0, \qquad V\ is\ decreased$$

$$\frac{1}{V} + \frac{dI}{dV} < 0, \qquad V\ is\ increased$$

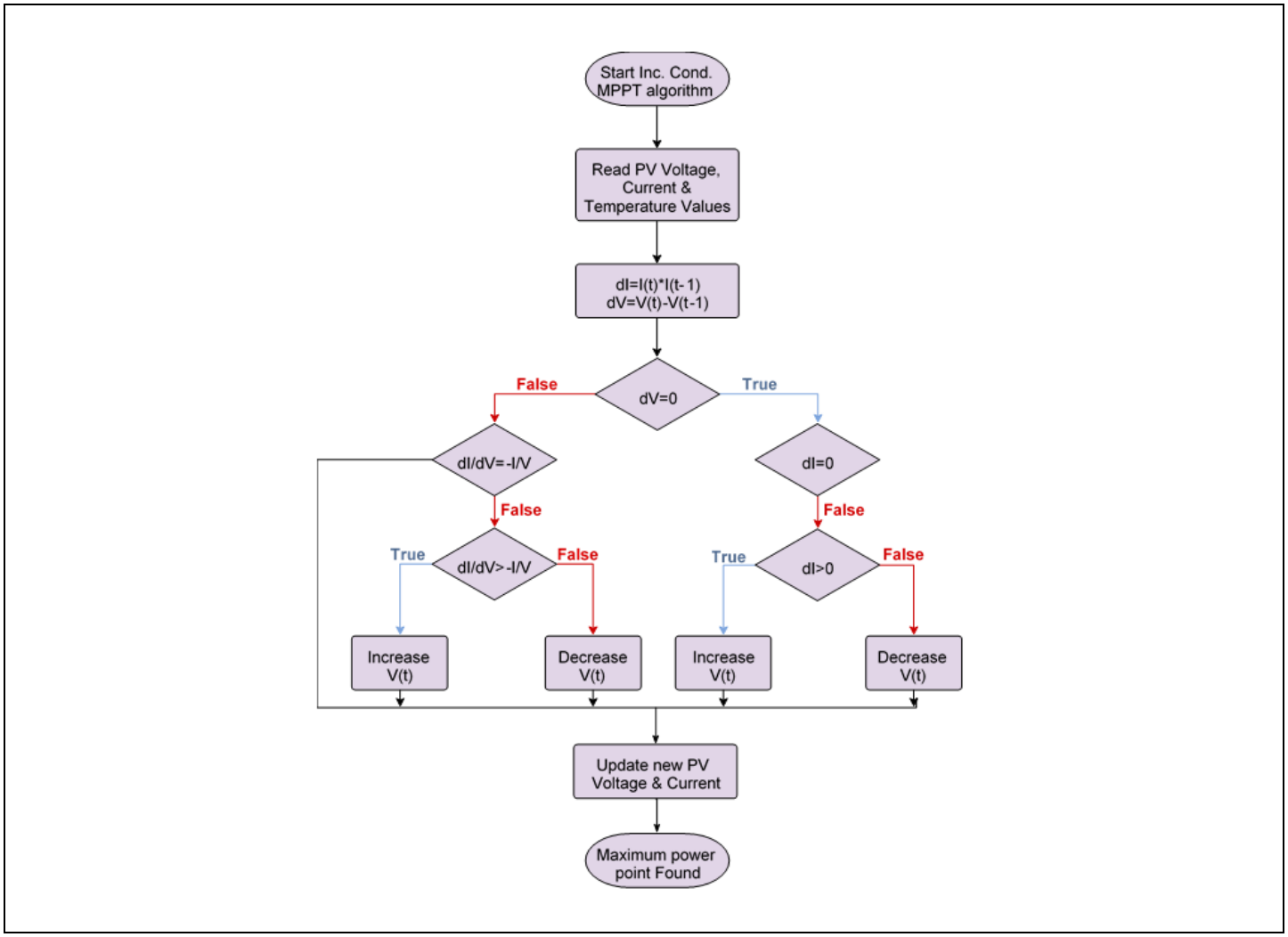


Figure 42 **Flowchart of the incremental conductance algorithm**

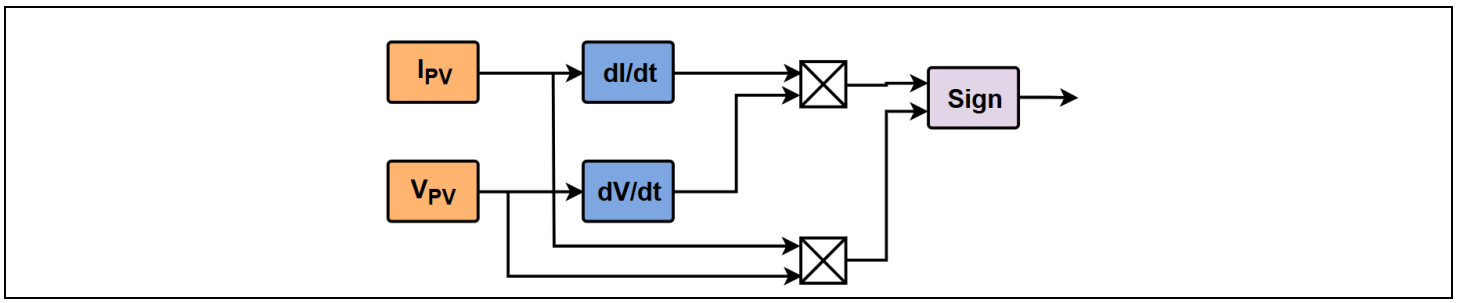


Figure 43 **Implementation of the incremental conductance method**

Single current control

The single-current control loop uses the same design as that of the current inner-loop for V_{dc} double-loop control.

3.3 Introducing the functional architecture and tasks

3.3.1 Functional architecture of the control software

The tasks discussed in the previous sections are distributed in the software platform, as shown in Figure 44. The application control software has the following functionalities:

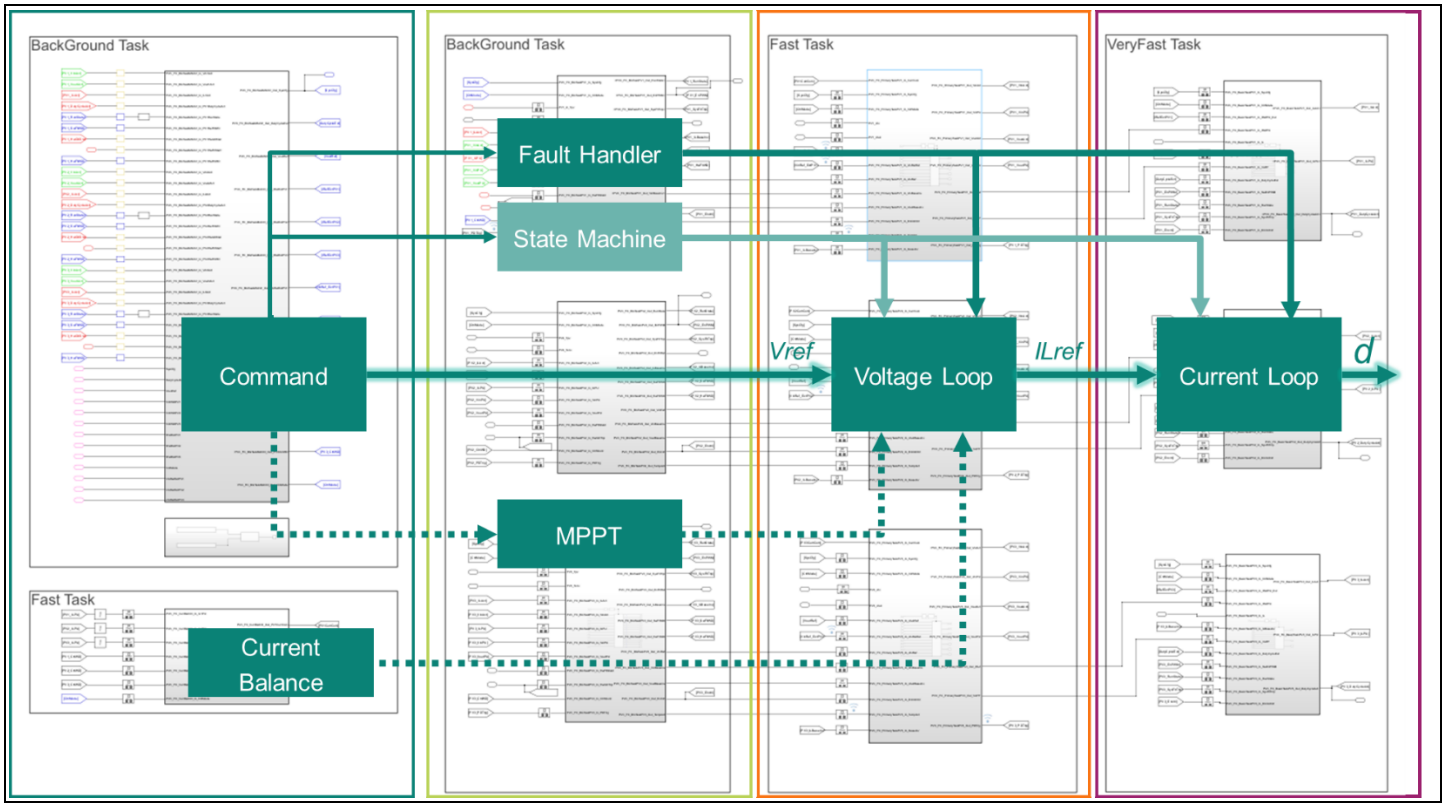


Figure 44 **Distribution diagram of the software platform**

Master control

The master control task is mainly responsible for delivering reference value instructions to the control loop. When the boost converter is activated, the master control task receives the command order and reference instructions. It mathematizes the reference value instructions and then sends them to the control tasks.

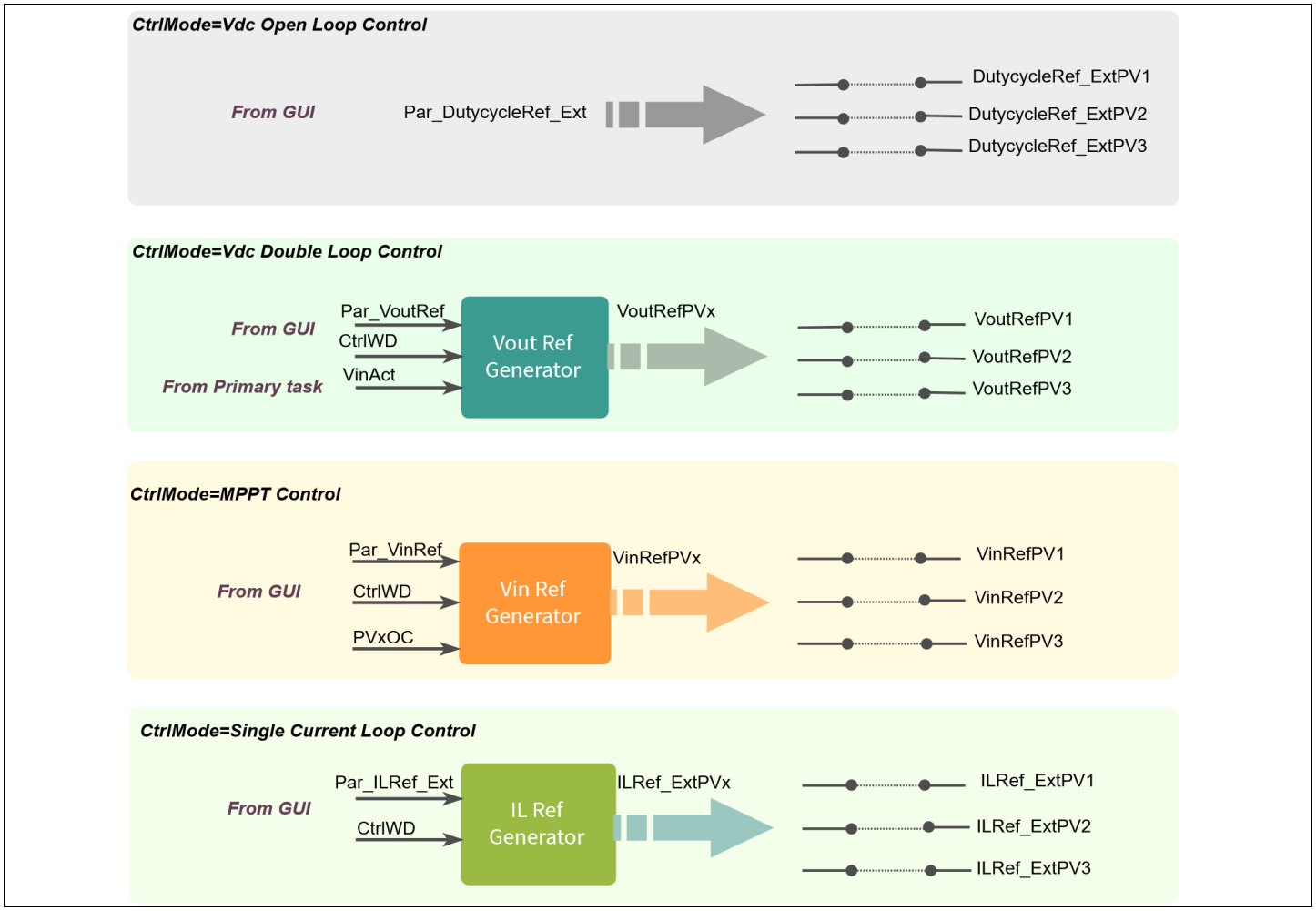


Figure 45 **Interface description of master control**

State machine

Figure 46 shows a state machine for the background task. It begins in the **STOPPED** state with control and PWM disabled. When a start command and ready signal are received, the system moves to **RUNNING**, enabling control and PWM. If the Stop command is given or if the readiness fails, the system transitions to **SHUTDOWN**, where control remains active briefly before being disabled. A fault condition (**FltTrip == 1**) causes a transition to the **FAULT** state from RUNNING, SHUTDOWN, or STOPPED states. In the FAULT state, control is disabled and the fault handling logic decrements a reset counter and checks for recovery. If the fault clears and reset conditions are met, the system returns to STOPPED. This design ensures safe operation and automatic recovery from faults.

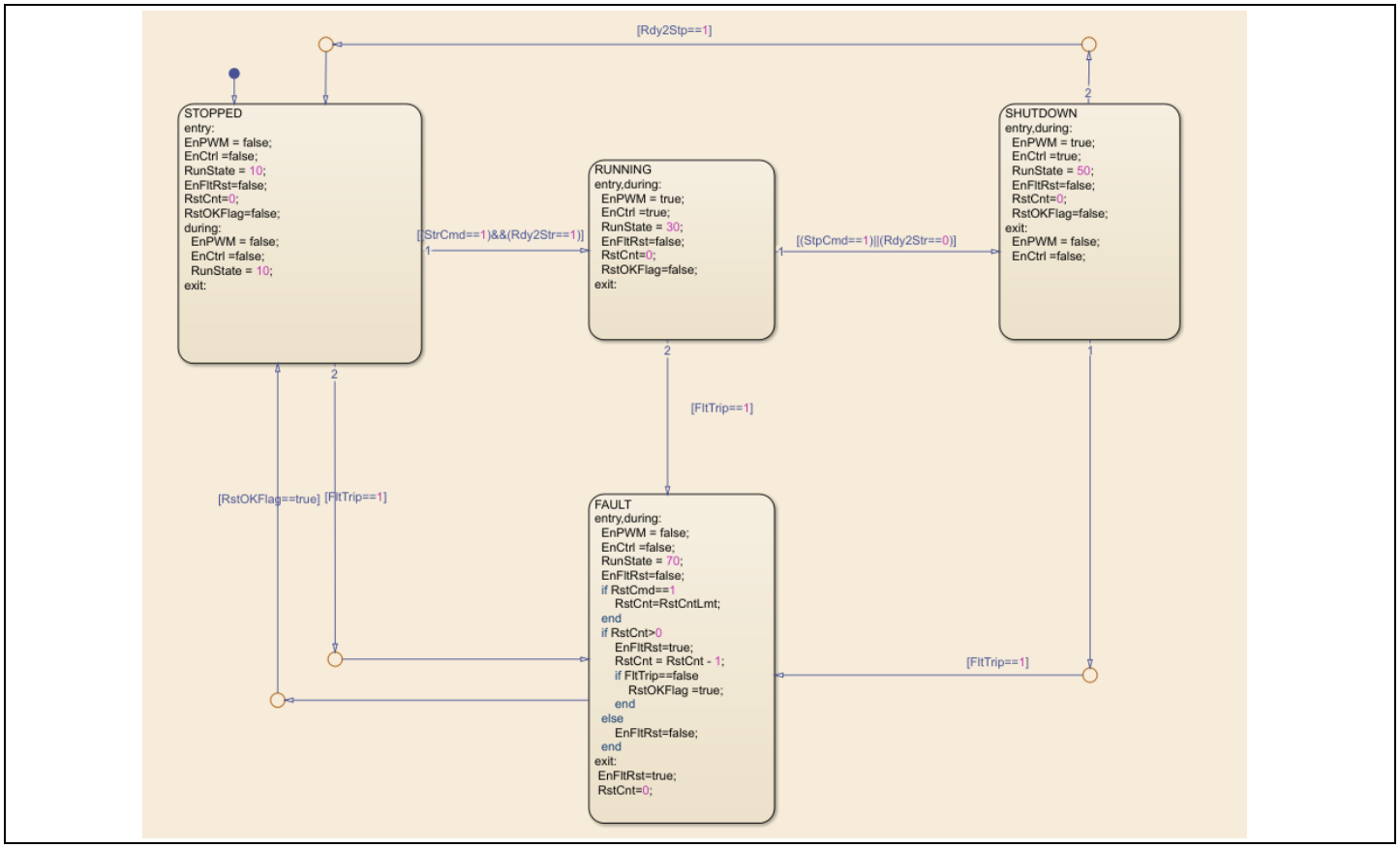


Figure 46 **State machine diagram of background tasks**

Fault check

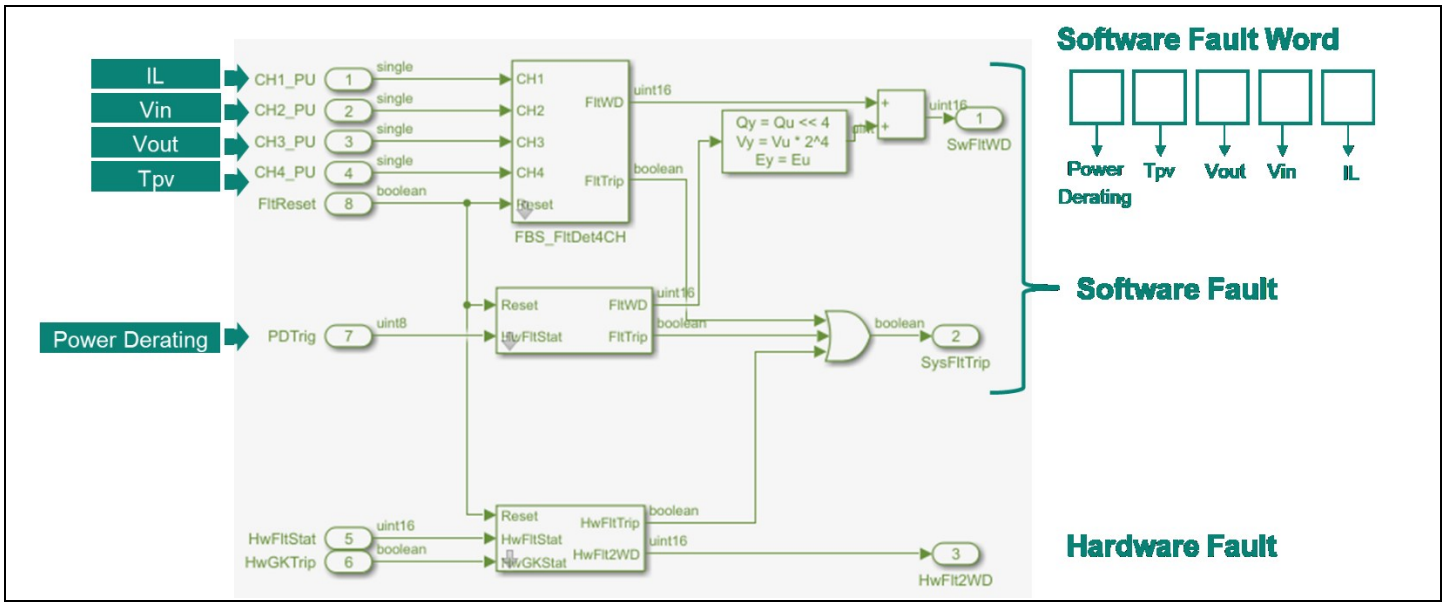


Figure 47 **Fault check**

MPPT control loop

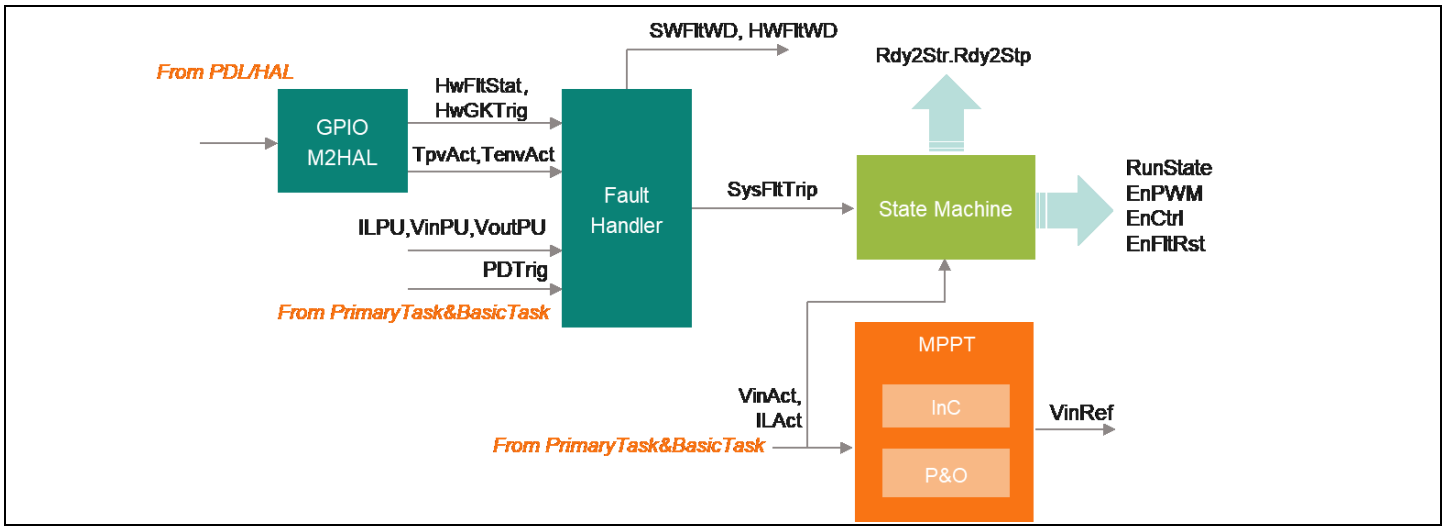


Figure 48 **Interface description of the background task**

Voltage-loop control

The primary task here is to control the voltage loop.

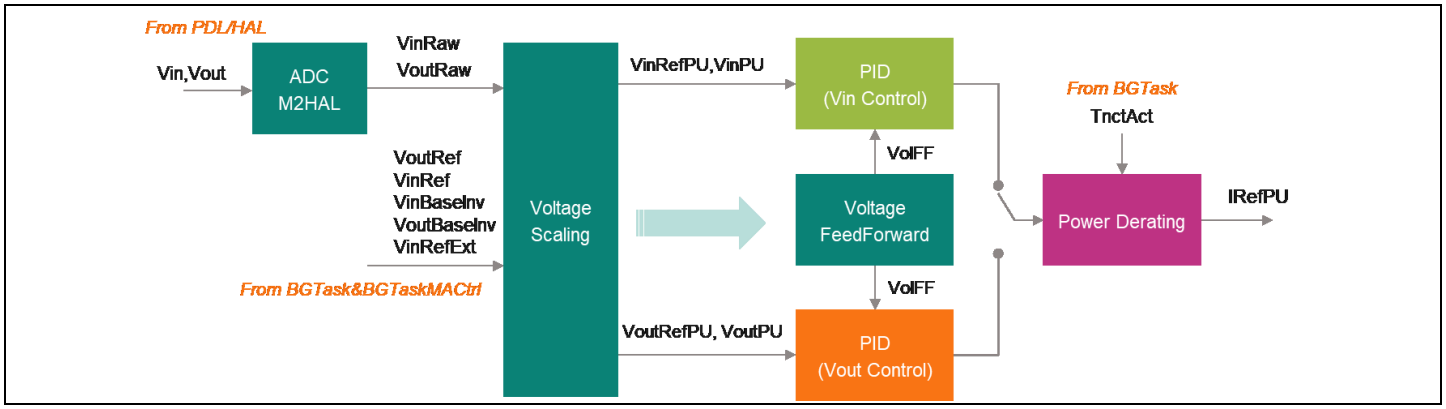


Figure 49 **Interface description of a voltage loop**

Current-loop control

The basic control task is mainly responsible for the current-loop control.

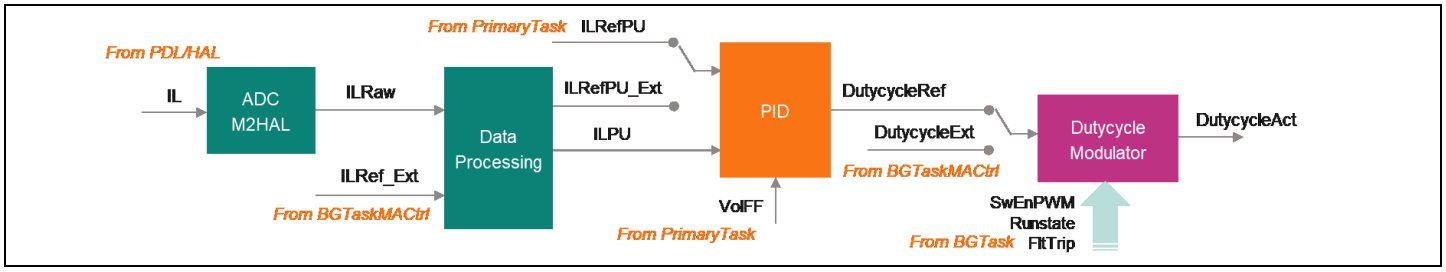


Figure 50 **Interface description of a current loop**

Current balancing

The current-balance control task is responsible for inhibiting the circulation of current between the PVs when multiple PVs are running in the V_{out} control mode at the same time.

First, the difference between the inductor current, IL of each PV and the average value of the output IL of multiple PVs is calculated. Then the compensation value of each PV is obtained by P control and input to the primary task.

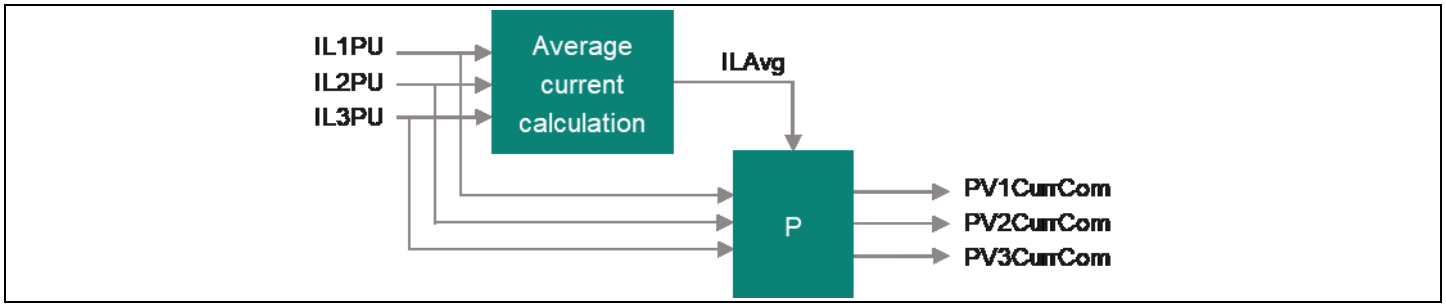


Figure 51 **Interface description for current balance**

Fan controller

The fan control is responsible for driving the fan that can be adjusted using the fan's DutyCycleRef parameter in the GUI.

Table 7 Fan control PWM duty versus ambient temperature

Ambient temperature	Fan PWM duty
35	0%
36	10%
37	20%
38	30%
39	40%
40	50%
41	60%
42	70%
43	80%
44	90%
>=45	100%

Figure 52 shows the fan-control system flow. The fan control process starts with two inputs i.e., Enable and Fan DutycycleRef which are provided by the GUI input. When enabling fan control, the fan speed can be controlled by the input duty cycle.

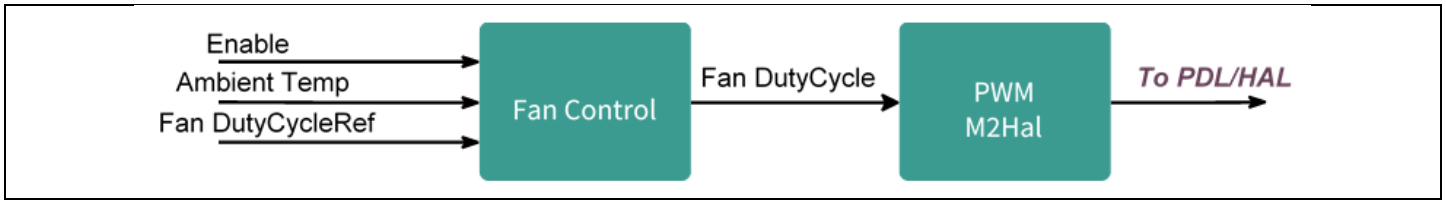


Figure 52 **Interface description of fan control**

3.3.2 Deployment and scheduling of the execution tasks

The interfaces between the hardware and the software are shown in **Error! Reference source not found.**.

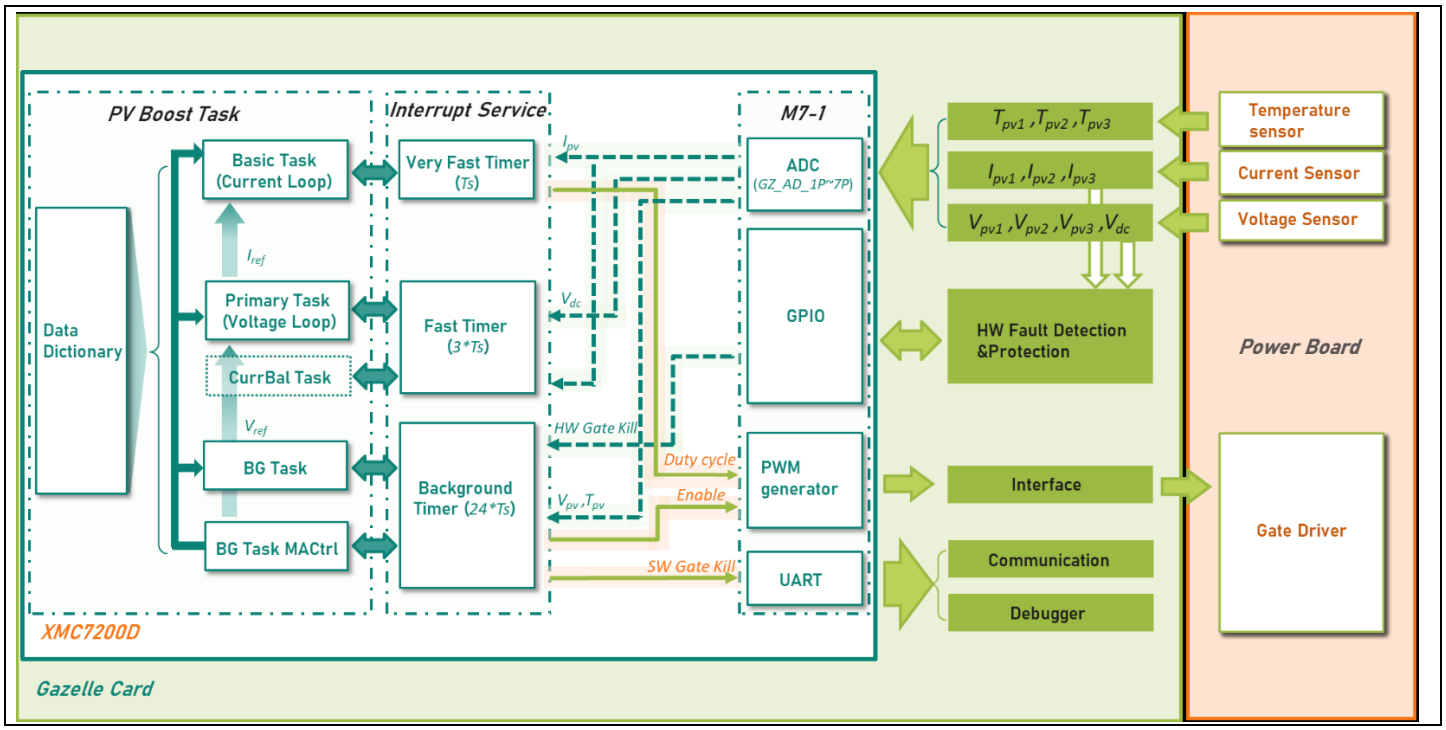


Figure 53 **The interfaces between hardware and software (Ts = 1/24000s)**

Table 8 shows how the execution tasks scheduled with the hardware timer and ISR (Interrupt Service Routine) are triggered.

Table 8 PV boost task

Functionalities	Execution task	ISR timer
Master control	Background task	Background timer
State machine	Background task	Background timer
Fault handler	Background task	Background timer
Fan control	Background task	Background timer
MPPT control	Background task	Background timer
Voltage control loop	Primary task	Fast timer
Current balancing	Primary task	Fast timer
Current control loop	Basic task	Very fast timer

4 Operation

The 15 kW boost converter has been tested using the XMC7200-based power control board reference design REF-CLBXMC7PEC that can be purchased separately. It was operated in the open and closed-loop modes and tested using a DC electronic load.
Install the MHI Graphical User Interface available at Infineon Developer Center.
The default installation path of the tool is C:\Users\<username>\Infineon\Tools\MHI-GUI-2LPVBoost\ MHI-GUI-2LPVBoost <version>\

4.1 Introduction to the GUI

Figure 54 shows the two-level PV boost converter GUI.

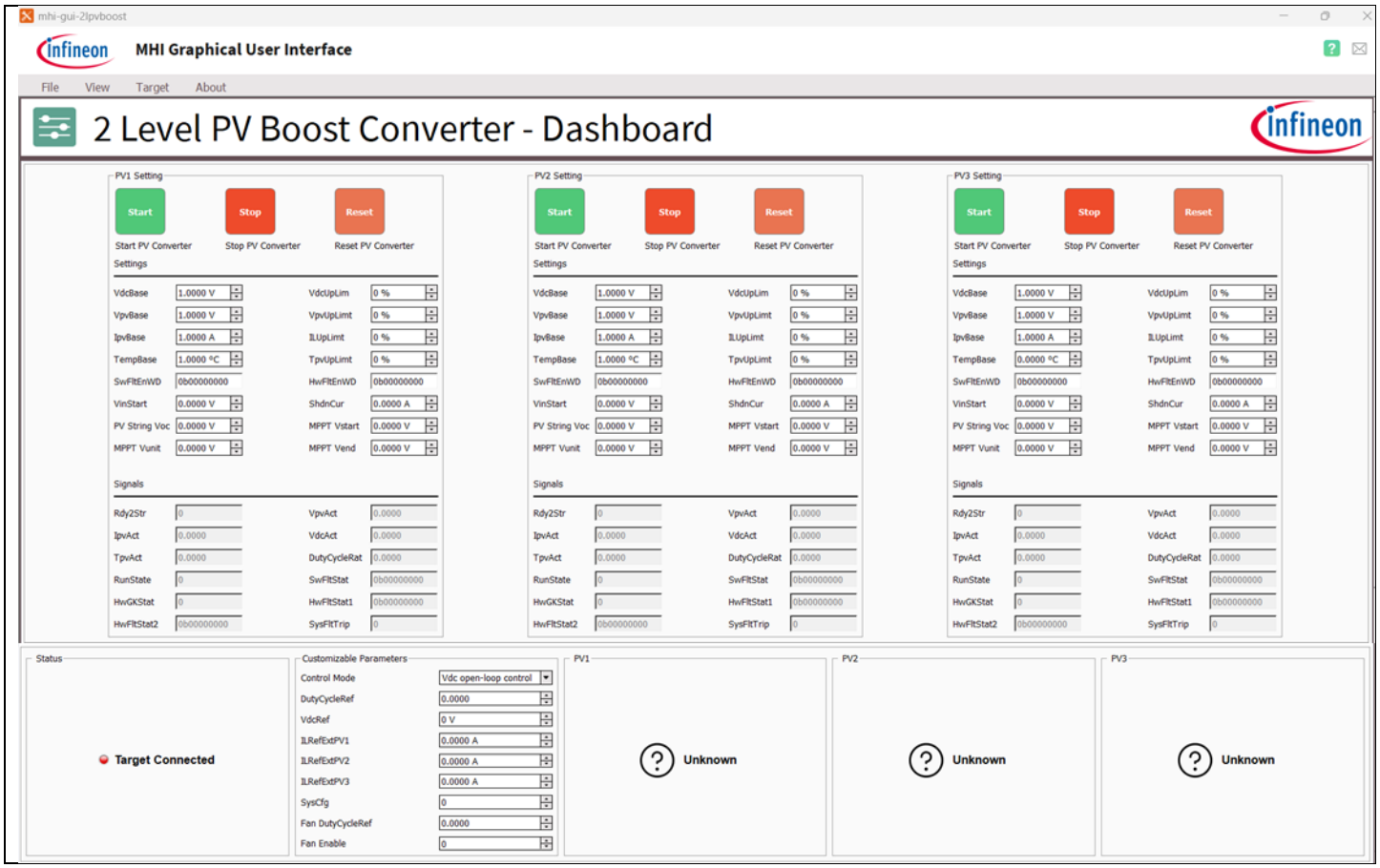


Figure 54 **2 Level PV Boost Converter GUI**

Different functionalities of some GUI sections are explained in the following sections.

4.1.1 Target panel

Target panel is used to flash the firmware to the target and connect to the hardware.

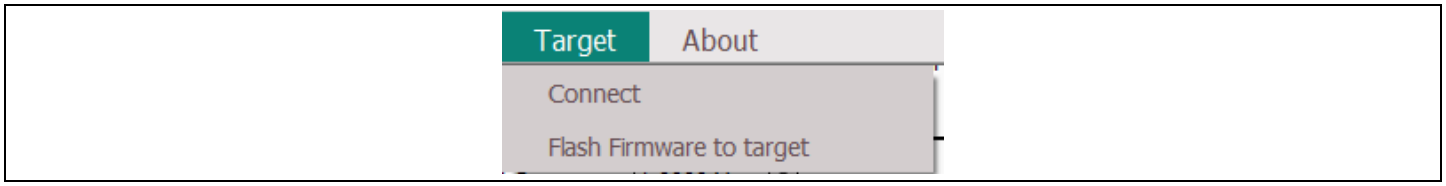


Figure 55 **Target panel**

4.1.2 Start, stop, and reset

This section is used to start, stop, and reset the individual channels. A reset button can be used after a fault is cleared. At the beginning of the evaluation users must click Reset.

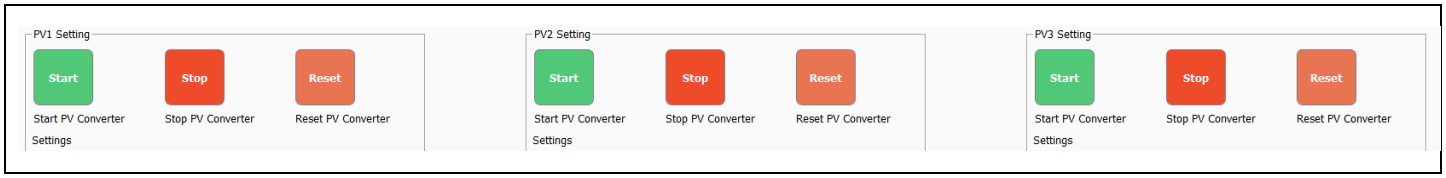


Figure 56 **Control section**

4.1.3 Converter status

This section shows the current status of the individual channels.

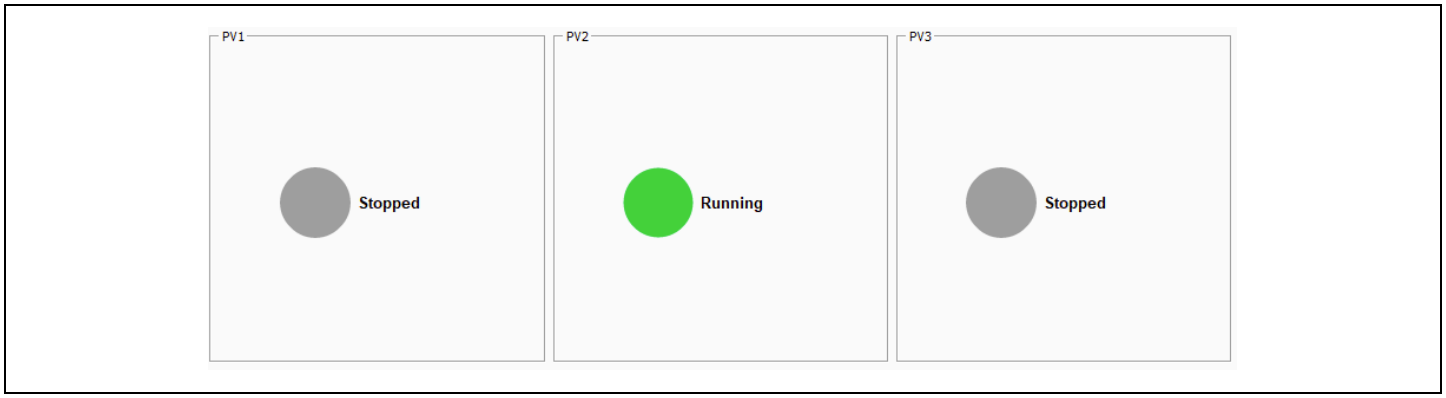


Figure 57 **Status section**

4.1.4 Customizable parameters

This section is used to set the parameters of the individual channels including the duty cycle and fan enablement. Both the duty cycle and vdcRef (reference output voltage) can be used to control the duty cycle. While using one parameter the other parameter must be set to 0.

The parameter SysCfg can have 7 values:

- SysCfg = 1: Changes only apply to channel 1
- SysCfg = 2: Changes only apply to channel 2
- SysCfg = 3: Changes apply to channel 1 and channel 2
- SysCfg = 4: Changes only apply to channel 3
- SysCfg = 5: Changes apply to channel 1 and channel 3
- SysCfg = 6: Changes apply to channel 2 and channel 3
- SysCfg = 7: Changes apply to all the three channels

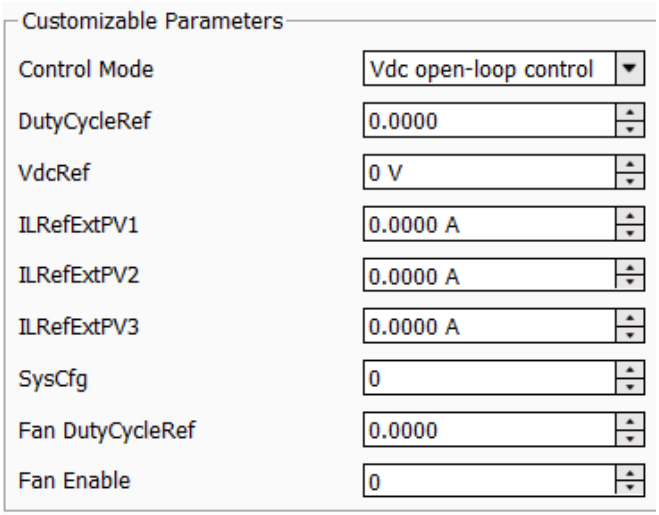


Figure 58 **Customizable parameters**

4.1.5 Protection thresholds

This section is used to set the software protection thresholds for individual channels.

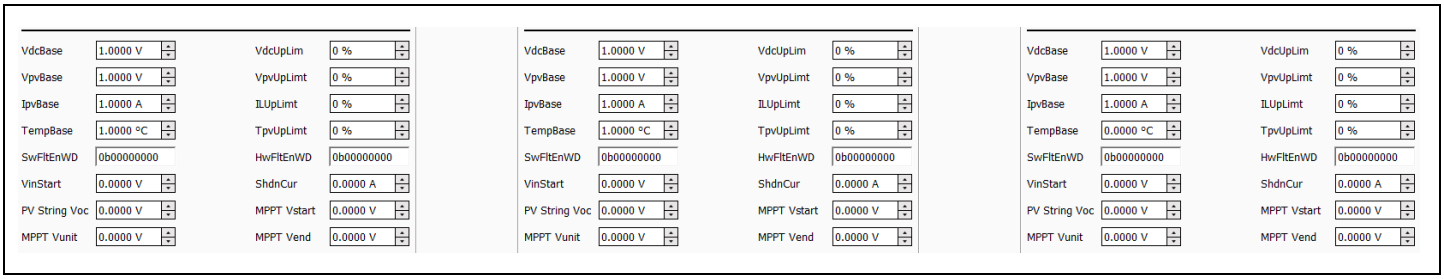


Figure 59 **Protection thresholds**

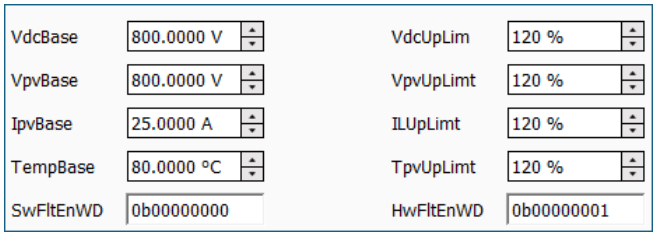


Figure 60 **Protection thresholds used during testing**

4.1.6 GUI parameters

Table 9 GUI parameters

No.	Name	Min	Max	Step	Unit	Description	Comment
Settings (Setpoints)							
1	Start	n/a	n/a	n/a	n/a	Start the converter	
2	Stop	n/a	n/a	n/a	n/a	Stop the converter	
3	Reset	n/a	n/a	n/a	n/a	Reset the fault words/status	This is a button
4	VdcBase	1	1100	0.0001	V	The base value of output voltage of PV converter	No
5	VpvBase	1	1100	0.0001	V	The base value of input voltage of PV converter	No
6	IpvBase	1	100	0.0001	A	The base value of current of PV1	No
7	TempBase	1	150	0.0001	°C	The base value of temperature of NTC	No
8	VdcUplimt	0	120	1	%	Vdc OV threshold (%) based on VdcBase	No
9	VpvUplimt	0	120	1	%	Vpv OV threshold (%) based on VpvBase	No
10	IpvUplimt	0	120	1	%	Ipv OC threshold (%) based on IpvBase	No
11	TempUplimt	0	120	1	%	IGBT OT threshold (%) based on TempBase	No
12	SwFltEnWD	n/a	n/a	n/a	n/a	Software fault enable word Bit0: Vdc_OV Bit1: Tpv_OT Bit2: Vpv_OV Bit3: Ipv_OC Bit4: Power derating Bit5~Bit7: Rsd	No
13	HwFltEnWD	n/a	n/a	n/a	n/a	Hardware fault enable word Bit0: PV_OC2 Bit1~Bit7: Rsd	No
14	VinStart	0	500	0.0001	V	Start voltage of the PV converter	
15	ShdnCur	0	10	0.0001	A	Shutdown current	• When the user stops the converter, if the current in the PV is more than the value of ShdnCur,

							the converter will switch to the Shutdown state to lower the current • When the current is less than the value of ShdnCur, the converter will disable PWM and switch into the Stopped state
16	PV String Voc	0	1100	1	V	Open circuit voltage of the PV string	
17	MPPT Vunit	0	50	1	V	Minimum step size for MPPT	
18	MPPT Vstart	0	800	1	V	MPPT start voltage	
19	MPPT Vend	0	800	1	V	MPPT end voltage	
Signals (Actual value)							
1	VpvAct	0	1500	n/a	V	Input voltage display value	No
2	VdcAct	0	1500	n/a	V	Output voltage display value	No
3	IpvAct	0	500	n/a	A	Average current value of inductance	No
4	TpvAct	0	200	n/a	°C	The temperature of IGBT	Only positive temperature values are displayed
5	DutyCyclRat	0	1	n/a	n/a	The output duty cycle rate	No
6	RunState	n/a	n/a	n/a	n/a	The states of PV converter 10: Stopped state 30: Running state 50: Shutdown state 70: Fault state	No
7	SwFltStat	n/a	n/a	n/a	n/a	Software fault state word 1: fault; 0: normal Bit0: Vdc_OV Bit1: Tpv_OT Bit2: Vpv_OV Bit3: Ipv_OC Bit4~Bit7: Rsd	This hardware fault can be enabled or disabled by the parameter SwFltEnWD
8	HwGKStat	n/a	n/a	n/a	n/a	Gate kill fault state word 1: fault; 0: normal	No

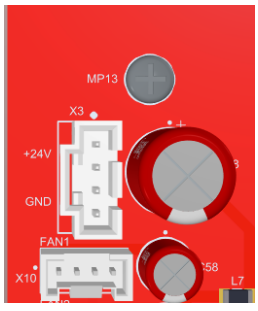
9	HwFltStat1	n/a	n/a	n/a	n/a	Hardware fault state word (type 1) 1: fault; 0: normal Bit0: PV_OC1 Bit1: PV_OV Bit2: Vdc_OV Bit3~Bit7: Rsd	This is the fault signal from the gate kill pin of the MCU and cannot be disabled
10	HwFltStat2	n/a	n/a	n/a	n/a	Hardware fault state word (type 1) 1: fault; 0: normal Bit0: PV_OC2 Bit1~Bit7: Rsd	This hardware fault can be enabled or disabled by the parameter HwFltEnWD
11	SysFltTrip	0	1	n/a	n/a	Fault Flag 1: fault; 0: normal	Whatever be the hardware fault or software fault, this parameter will be set 1
12	Rdy2Str	0	1	n/a	n/a	Converter is ready for start	No
Customization parameters (Setpoints)							
1	SysCfg	1	7	n/a	n/a	Hardware configuration word Bit 1 = 1: PV1 is active Bit 2 = 1: PV2 is active Bit 3 = 1: PV1 & PV2 is active Bit 4 = 1: PV3 is active Bit5 = 1: PV1 & PV3 is active Bit6 = 1: PV2 & PV3 is active Bit 7 = 1: PV1, PV2, and PV3 are active	From master control to define which PV converter is active in the hardware
2	Control Mode	0	5	n/a	n/a	0: V_{dc} open-loop control 2: V_{dc} double-loop control 3: MPPT control 5: Single current control	No
3	DutyCycleRef	0	0.8	0.01		Reference value of duty cycle	• If the input signal of DutycycleRef is not equal to zero, the duty cycle reference (DutycycleRef) becomes the input command • If the input signal of DutycycleRef is

							equal to zero and VoutRef is not equal to zero, the duty cycle reference (VoutRef) becomes the input command
4	VdcRef	0	1100	1	V	Reference value of output voltage	
5	ILRefExtPV1	0	100	0.1	A	Reference value of IL1	No
6	ILRefExtPV2	0	100	0.1	A	Reference value of IL2	No
7	ILRefExtPV3	0	100	0.1	A	Reference value of IL3	No
8	Fan DutyCycleRef	0	1	0.01	n/a	Reference value for Fan duty cycle	No
9	Fan Enable	0	1	n/a	n/a	Enable/disenable word for fan control 1: enable 0: disable	No

4.1.7 The power board and control board connection

Steps to establish a connection between the PC and control board

1. Ensure that the boost board and the control board are connected as shown in Section 5. The signal cables from the power board provide power to the control board. No external power supply needs to be connected to the control board.
2. Connect the 24 V supply to the power board with the help of the X3 connector that comes with the power board as shown in Table 3.



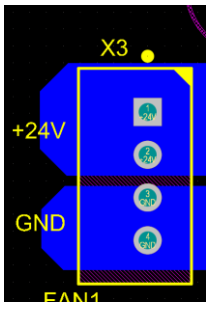


Figure 61 **24 V connector**

3. In the COM port setting in the GUI, choose the COM port to which the control board is connected. This can be checked in the device manager.
4. Click Open COM.
5. If everything is set correctly, the Measurement section (right) will display the values.
6. After the bench setup is set, click Start to start evaluating the hardware.

4.2 Flashing the firmware

Steps to flash the firmware

1. Shut down the power stage to put it into safe state.
2. Connect the 24 V supply to the control board.
3. Add three jumper headers as shown in Figure 62.
4. Connect the debug port of the control board to the PC using a USB cable.

Figure 62 **REF-CLBXMC7PEC debug configuration**

5. Start the MHI-GUI-2LPVBoost application.

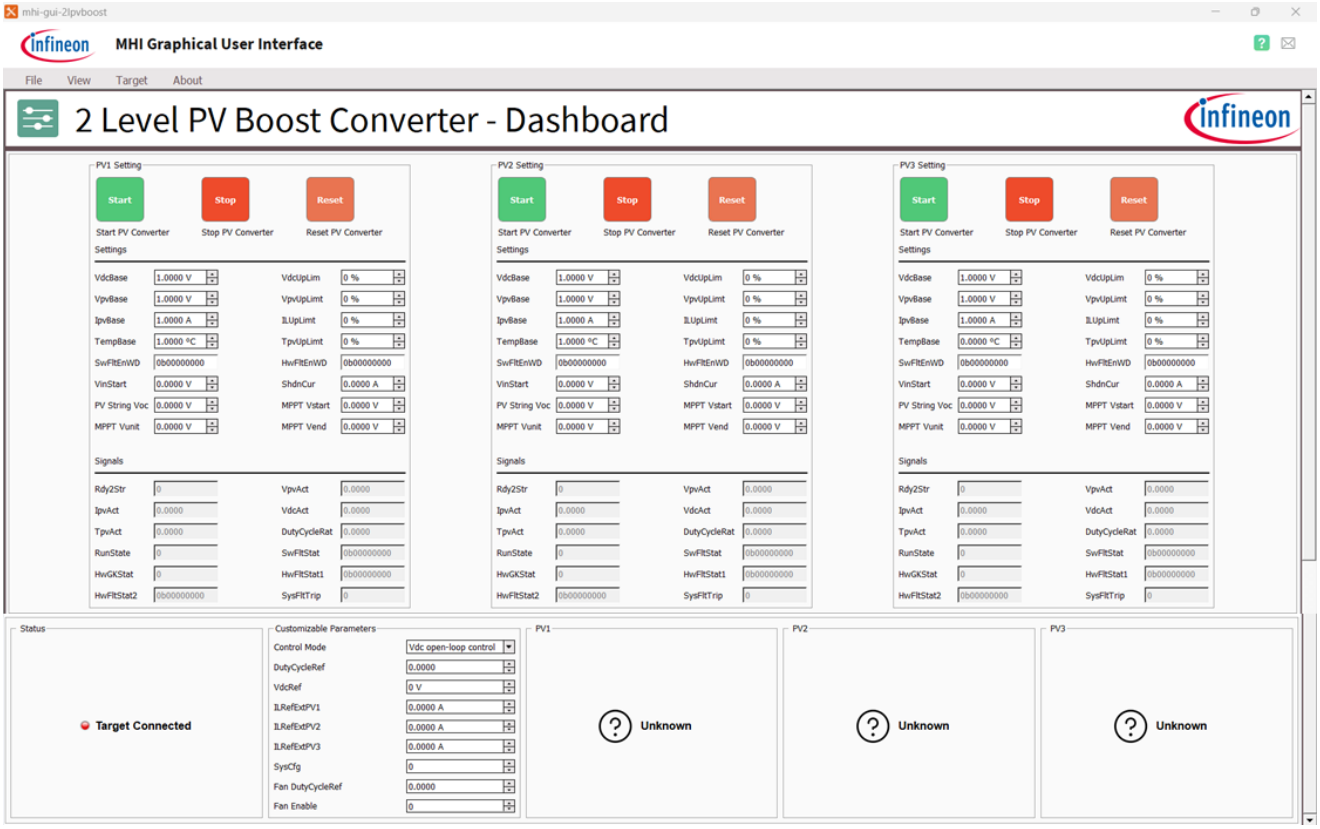


Figure 63 **GUI**

6. Click on Flash firmware to target in the MHI-Monitor and wait until the tool flashes the firmware to the target. A message appears after the operation is complete. Please note that this operation needs to be done only once.

Figure 64 **Flashing the firmware**

7. Click Connect, then click Connect to server.
8. Choose the COM port (defined in the device manager) from the dropdown list.
9. Click Connect and then click Close.

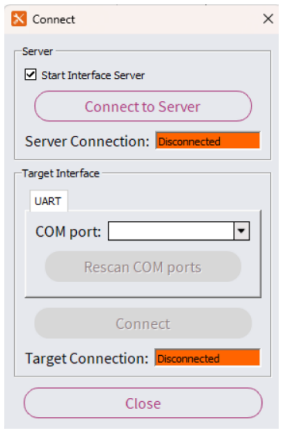


Figure 65 **Connecting to target**

10. Disconnect the external 24 V power supply.

4.3 Operating in the V_{dc} open-loop control mode

To operate the boost converter in open loop, set the control mode to V_{dc} open-loop control. Adjust the duty cycle reference (DutyCycleRef) in the GUI as required. The duty cycle reference should lie in the range of 0 to 0.80. For duty ratios over 0.8, the GUI sets the default value of 0.8 duty ratio.

The open-loop control shown in Figure 38 supports voltage reference and duty cycle reference:

- If the input signal of DutycycleRef is not equal to zero, the duty cycle reference (DutycycleRef) becomes the input command.
- If the input signal of DutycycleRef is equal to zero, but VoutRef is not equal to zero, the duty cycle reference (VoutRef) becomes the input command

Steps to operate in the open-loop control mode

1. Set the control mode to V_{dc} open-loop control as shown in Figure 66.
2. Reset the PV converter to avoid errors.
3. Adjust the duty cycle reference in the GUI.
4. Click Start to start the operations.
5. Provide the needed supply and load to the converter.
6. Change the reference value during operation.
7. Click Stop to stop the converter.

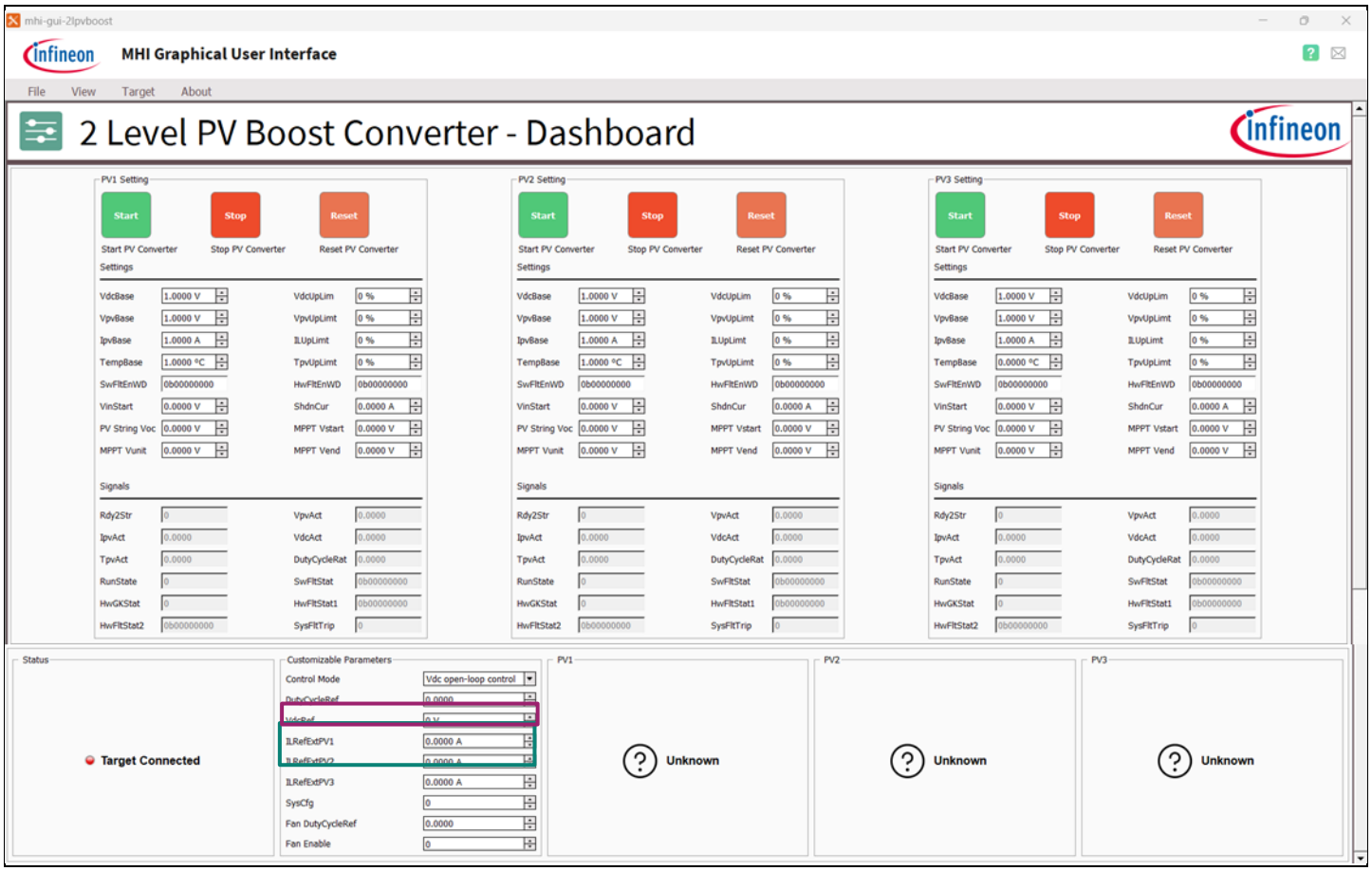


Figure 66 **Open-loop control mode operation**

4.4 Operation in the V_{dc} double-loop control mode

Select V_{dc} double-loop control as the control mode, and the boost will run at V_{dc} double-loop control. If the system works properly, the V_{dc} voltage of the boost tracks the given VdcRef with a certain slope.

The boost converter will now have an input DC source. The controller will sense the DC-link bus voltage and compare it with the DC reference voltage. The DC reference voltage (VdcRef) value can be adjusted through the GUI.

Steps to operate in V_{dc} double-loop control mode

1. Set the control mode to V_{dc} double-loop control as shown in Figure 67.
2. Reset the PV converter to avoid errors.
3. Adjust the VdcRefvalue in the GUI.
4. Click Start to start the operations.
5. Provide the needed supply and load to the converter.
6. Change the reference value during operation.
7. Click Stop to stop the converter.

When several PV inputs are enabled, a circulation current inevitably occurs between different boosts. Therefore, a current balance algorithm is added. When the software detects that multiple PVs are enabled in the V_{dc} control mode, the current balancing algorithm starts automatically.

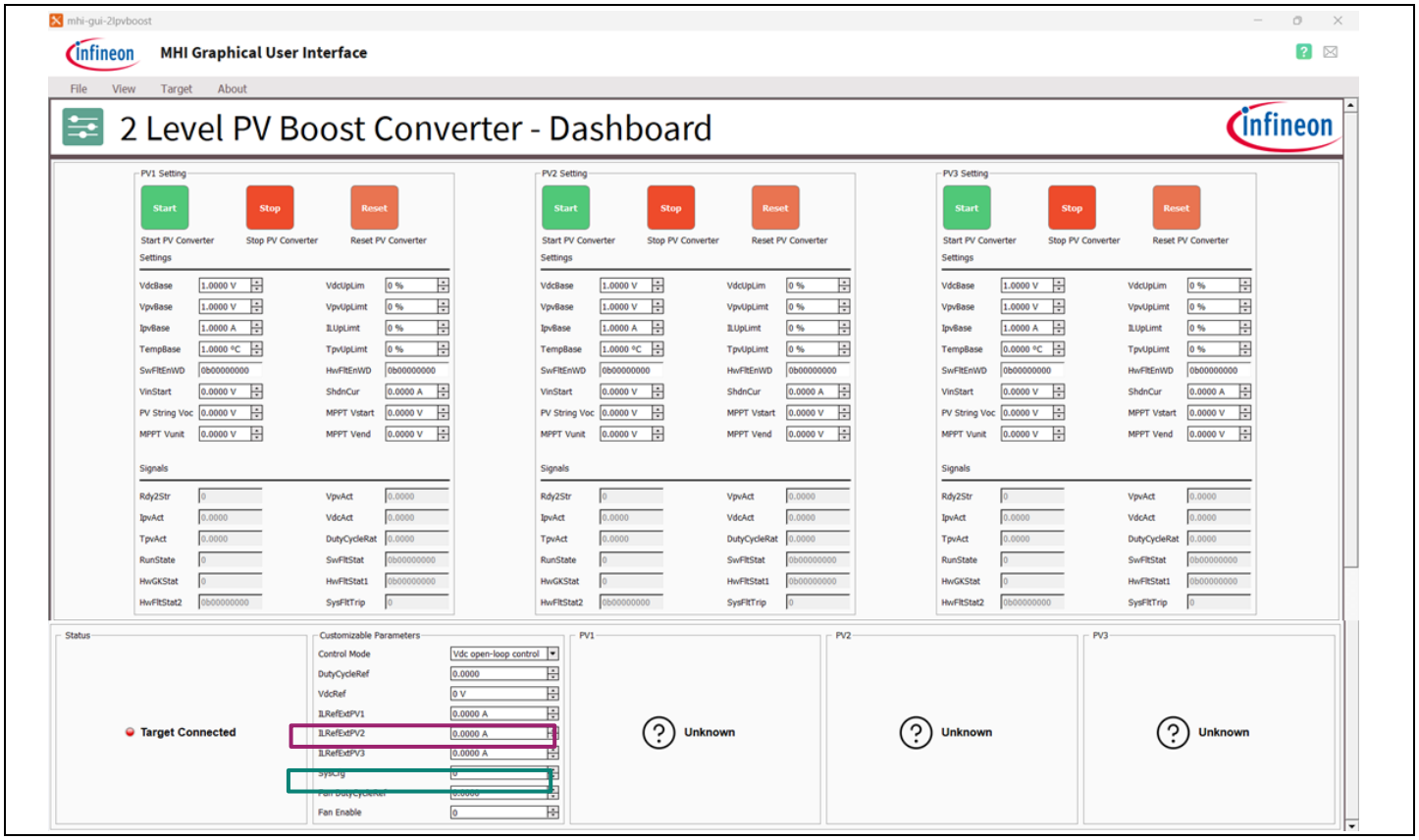


Figure 67 **Operating in the V_{dc} double-loop control mode**

4.5 Operating in the MPPT control loop

Set up the test platform as shown in Figure 75 and follow the instructions to operate in the MPPT mode.

1. Open the MHI monitor and reset the PV converter to avoid errors.

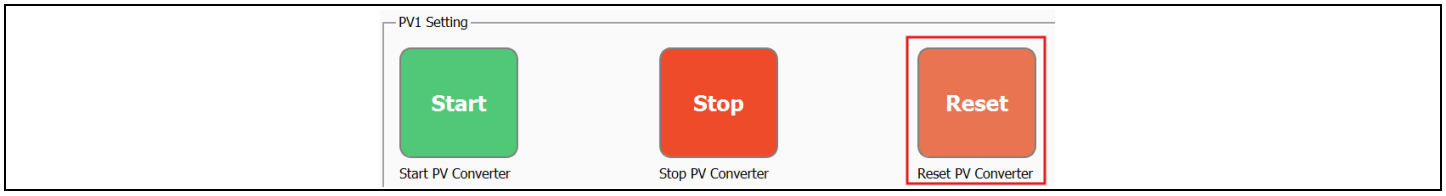


Figure 68 **Reset the PV converter**

2. Select MPPT control as the control mode. Other parameters remain default. Refer to Table7 for a detailed description of the parameters.

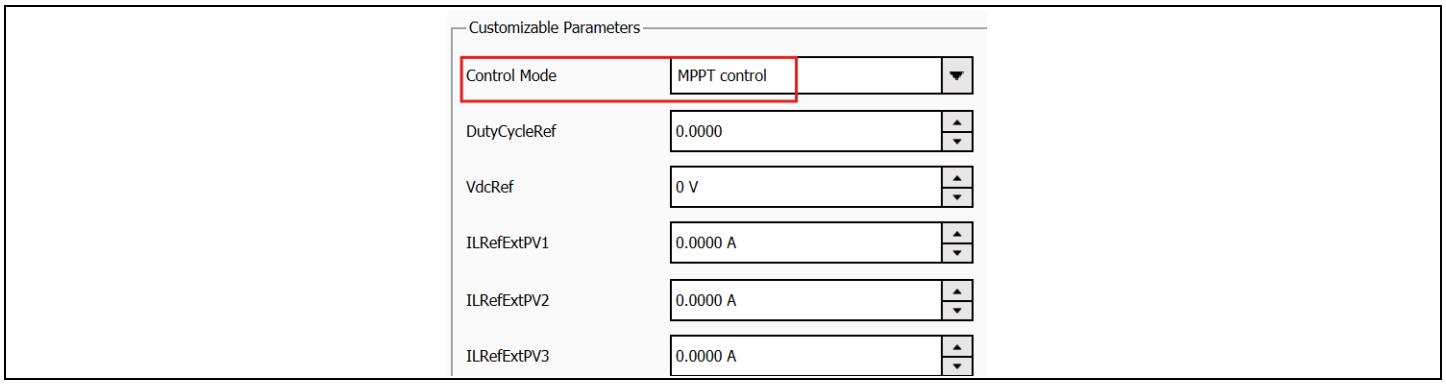


Figure 69 **MPPT control mode**

3. Use the solar array simulation tool to simulate the PV curve. Different PV cells correspond to different curves. Here, LR7-72HYD-660M is used. The parameters given in Table 10 below can be found in LONGi. The actual test simulated 10 PV panels of LR7-72HYD-660M in series.

Table 10 PV panel LR7-72HYD-660M application parameters

Maximum power (P_{max}/W)	660
Open-circuit voltage (V_{oc}/V)	54.00
Short-circuit current (I_{sc}/A)	15.41
Peak power voltage (V_{mp}/V)	44.85
Peak power current (I_{mp}/A)	14.72
Temperature coefficient of the short-circuit current (I_{sc})	+0.005%/°C
Temperature coefficient of the open-circuit voltage (V_{oc})	-0.200%/°C
Temperature coefficient of the peak power (P_{max})	-0.260%/°C

4. The parameters mentioned in Table 10 are used for simulating PV curves under different operating conditions, getting the corresponding results, and then using the four-point method (Voc/Vmp /Isc/Imp) to simulate the curve in the solar array simulation tool.

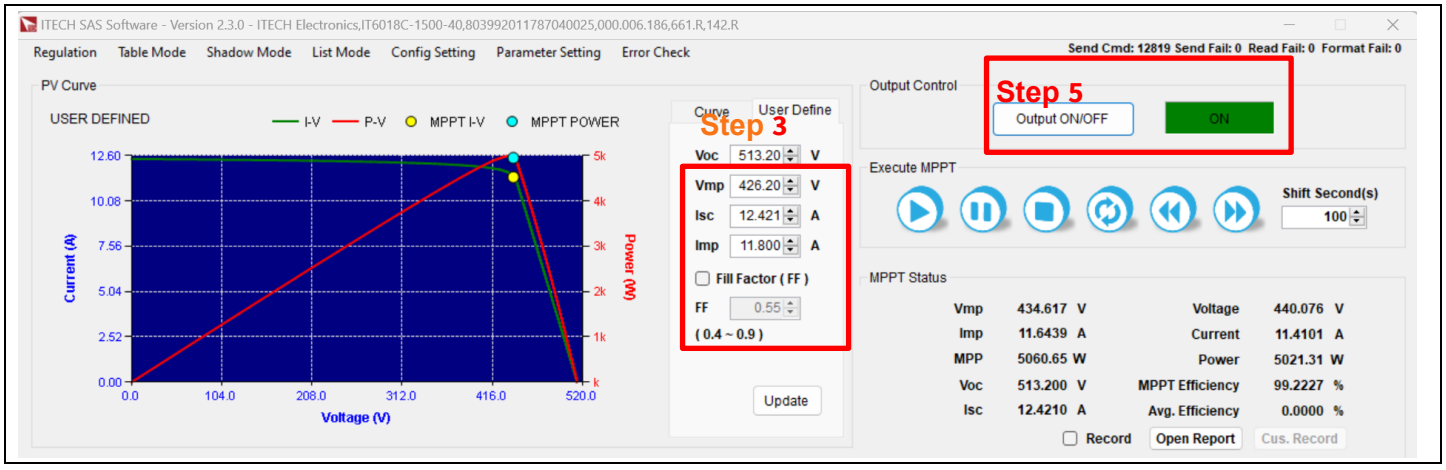


Figure 70 **Solar array simulation tool**

5. Set the corresponding parameters in the MHI monitor to match those used in the solar array simulation tool. The ‘MPPT Vunit’ corresponds to the steps, with a recommendation of 2. It can be increased to achieve faster tracking speed and better accuracy. The minimum MPPT Vunit is 1. The MPPT V_{end} needs to be set higher than V_{mp}.

Figure 71 **GUI parameters for MPPT control**

6. For the voltage source acting as the DC bus, do the following configurations:
   - Set the running mode as CV,
   - Set the upper current limit to 20 A
   - Set the lower current limit to -20 A.
   - Set the output voltage value to 650 V, ensuring the stability of the output.

Figure 72 **DC source for constant V_{out} in IT6018C-1500-40**

7. In the simulation tool, click Output ON/OFF in the Output Control tab.
8. Click Start PV Converter in the MHI monitor, and you can see the curve in the simulation tool at the point of maximum power.

Figure 73 **Start PV Converter**

9. Use an oscilloscope to observe the corresponding parameters.

4.6 Operating in the single-current loop control mode

In this control loop, the controller reads the inductor current for every channel.

Steps to operate in the single-current loop control mode

1. Set the control mode to single-current loop control.
2. Reset the PV converter to avoid errors.
3. Adjust the ILRefExtPV1, ILRefExtPV2, and ILRefExtPV3 values in the GUI.
4. Click Start to start the operations.
5. Provide the needed supply and load to the converter.
6. Change the reference value during operation.
7. Click Stop to stop the converter.

Operation

If the system works properly, the inductor current of the boost converter tracks the given ILRefExt for all PVs.

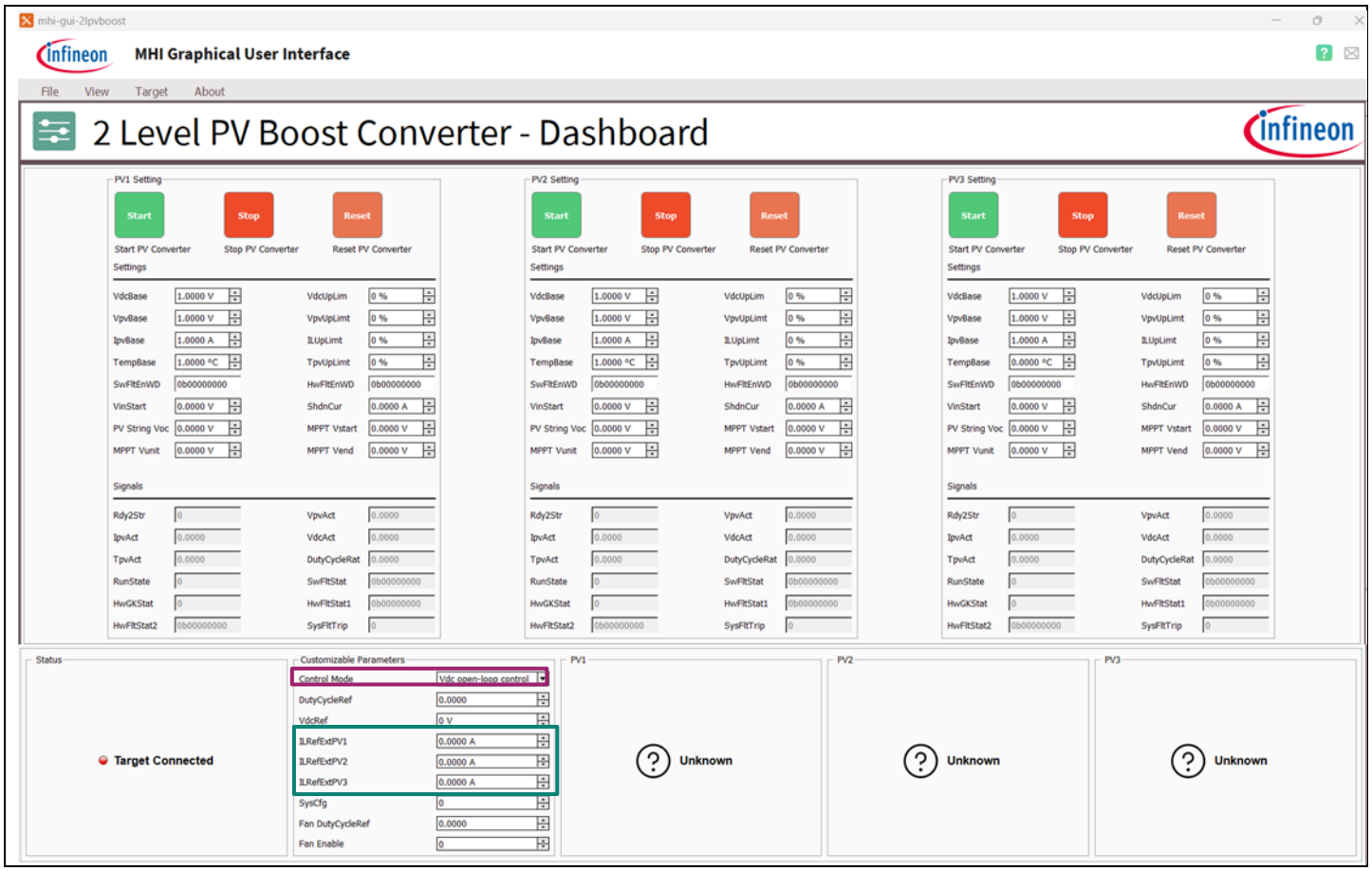


Figure 74 **Operating in a single-current loop control**

5 Performance and test results

5.1 Test bench setup

The converter can be operated using all the controlling strategies discussed in Chapter 0.
For the boost topology, the outputs cannot be operated in open-circuit mode. It can work in CCM (continuous conduction mode) or DCM (discontinuous conduction mode), but for the open-loop control of output voltage, it must work in the CCM mode.

The MPPT control test setup, illustrated in Figure 75, differs from the test setup used for other controls, as shown in Figure 76Figure 76.

The following equipment was used for the testing:

- 15 kW boost kit
    - REF-15KW2LBOOST V1.0 power conversion main board
    - REF-15KW2LBOOST -Filter input filter board
    - REF-CLBXMC7PEC control board
    - PB-CAPTANK-1.1KV bus capacitor board
- GUI
    - MHI-GUI-2LPVBoost-v2.1.0
- DC power source
    - IT6018C-1500-40: MPPT control
    - PAT1000-8TS (SPEC21295): V_{dc} open-loop, V_{dc} double-loop, and single-current loop control
- Electronic load
    - IT6018C-1500-40: MPPT control
    - PLZ2005WH2: V_{dc} open-loop, V_{dc} double-loop, and single-current loop control

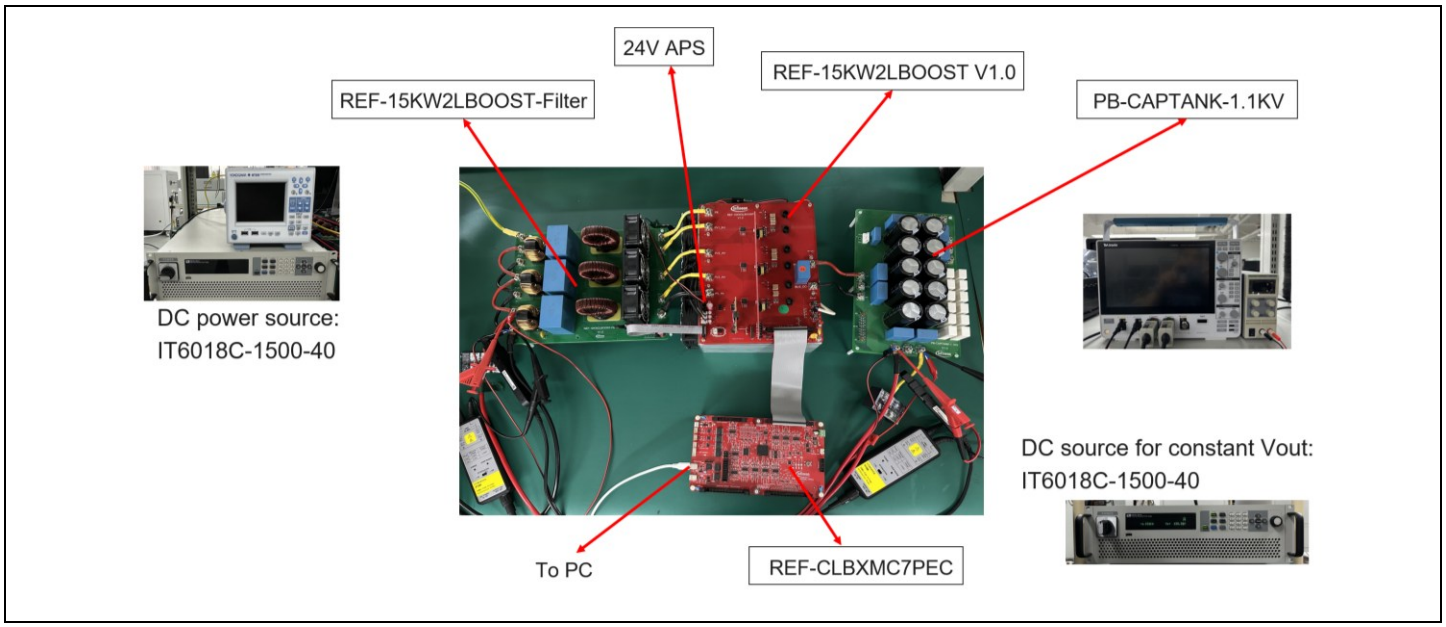


Figure 75 **Test setup for MPPT control**

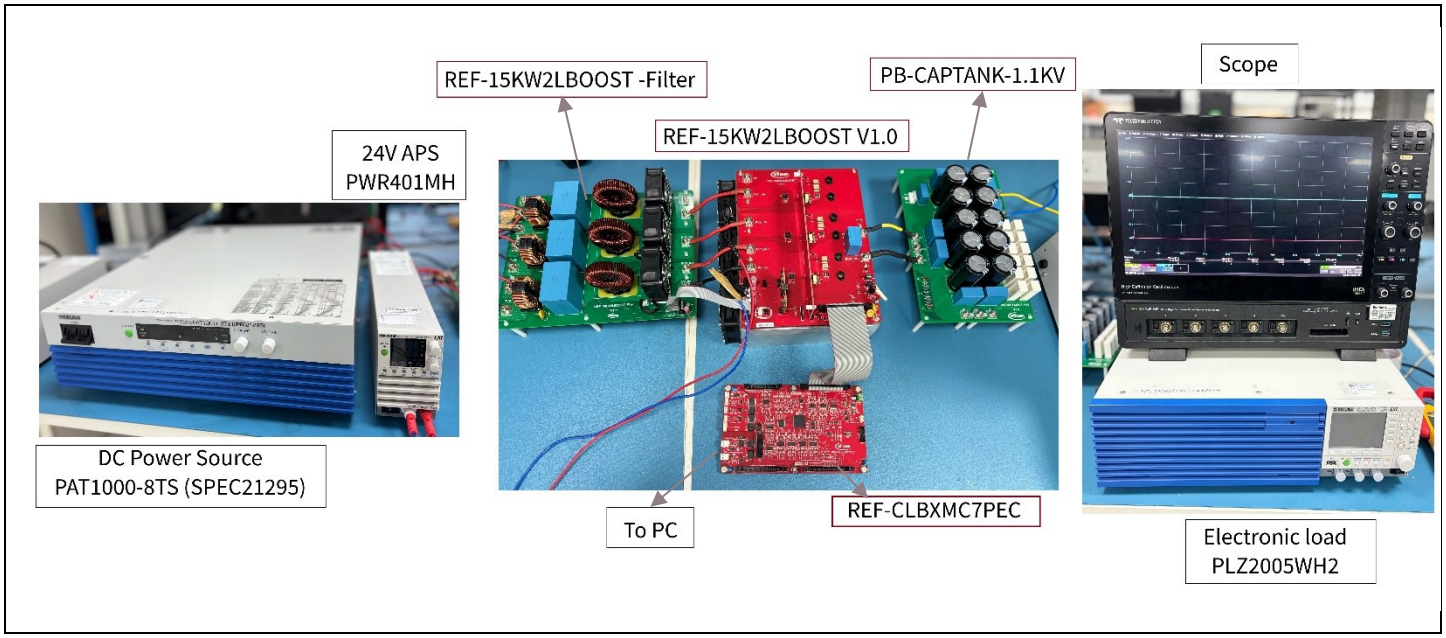


Figure 76 **Test setup for control V_{dc} open-loop, V_{dc} double-loop, and single-current loop control.**

5.2 Test results

5.2.1 V_{dc} open-loop control

Table 11 Test specification

Input voltage	350 V
Duty Cycle	0.5
Current	5.5 A
Output power	3.8 kW
Legend	Ch1: V_{gk}, Ch2: channel 1 output voltage, Ch3: inductor current

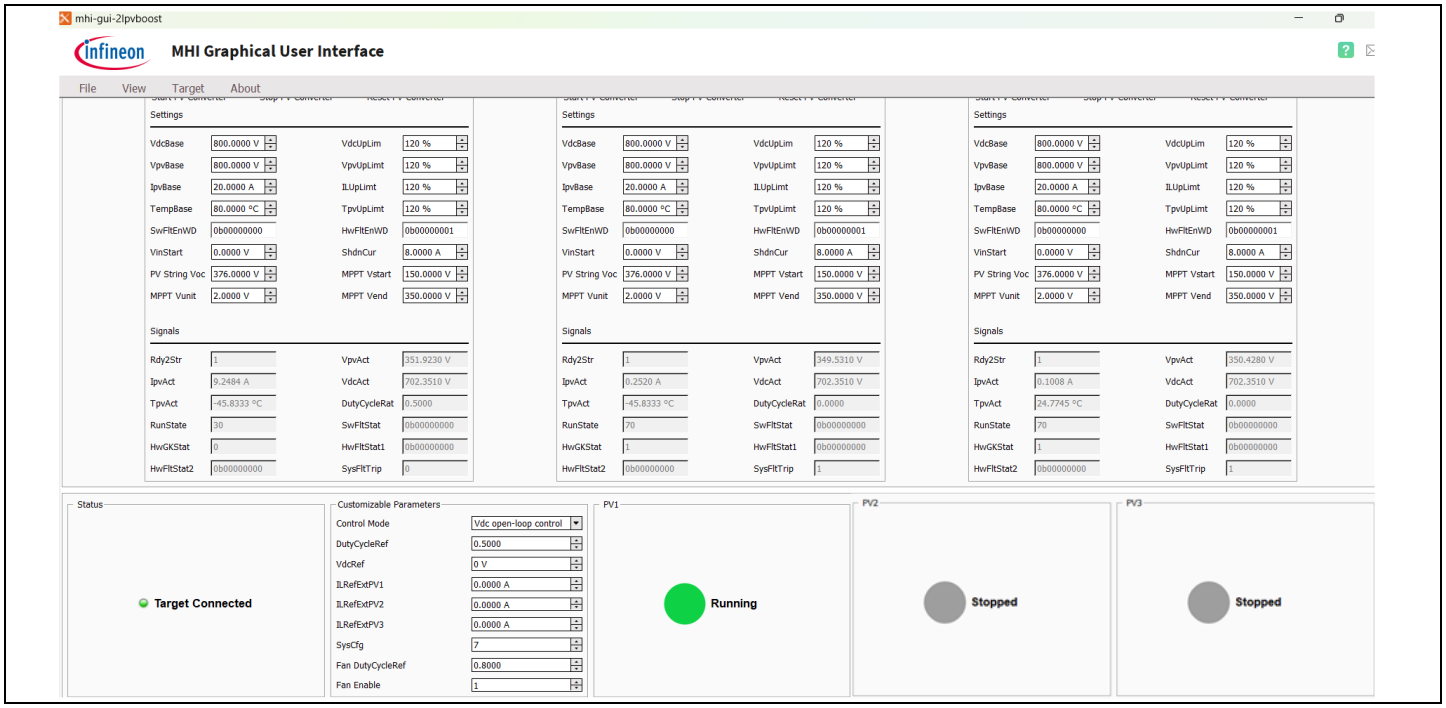


Figure 77 **GUI for V_{dc} open-loop control operation for channel 1**

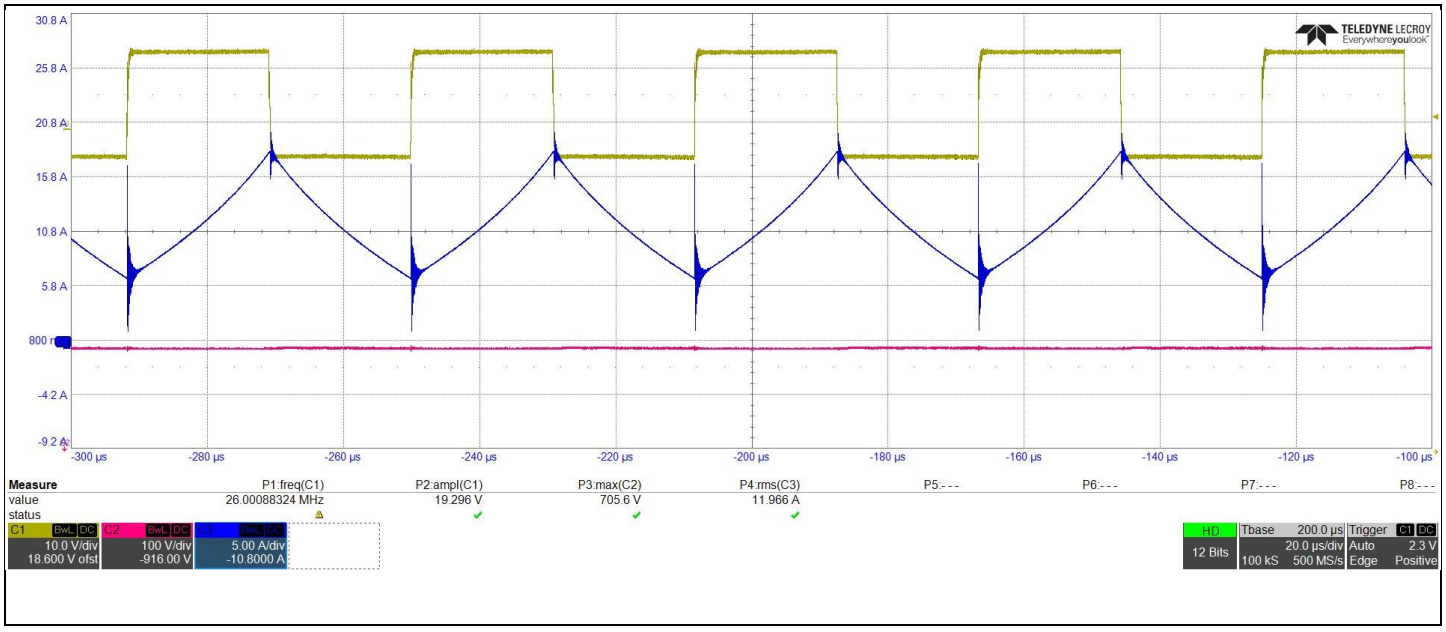


Figure 78 **Waveforms for V_{dc} open- loop control operation at d = 0.5**

5.2.2 V_{dc} double-loop control

Table 12 Test specification

Input voltage	350 V
Output voltage	710 V
Output current	5.5 A
Output power	3.9 kW
Legend	Ch1: Vgk, Ch2: channel 1 output voltage, Ch3: inductor current

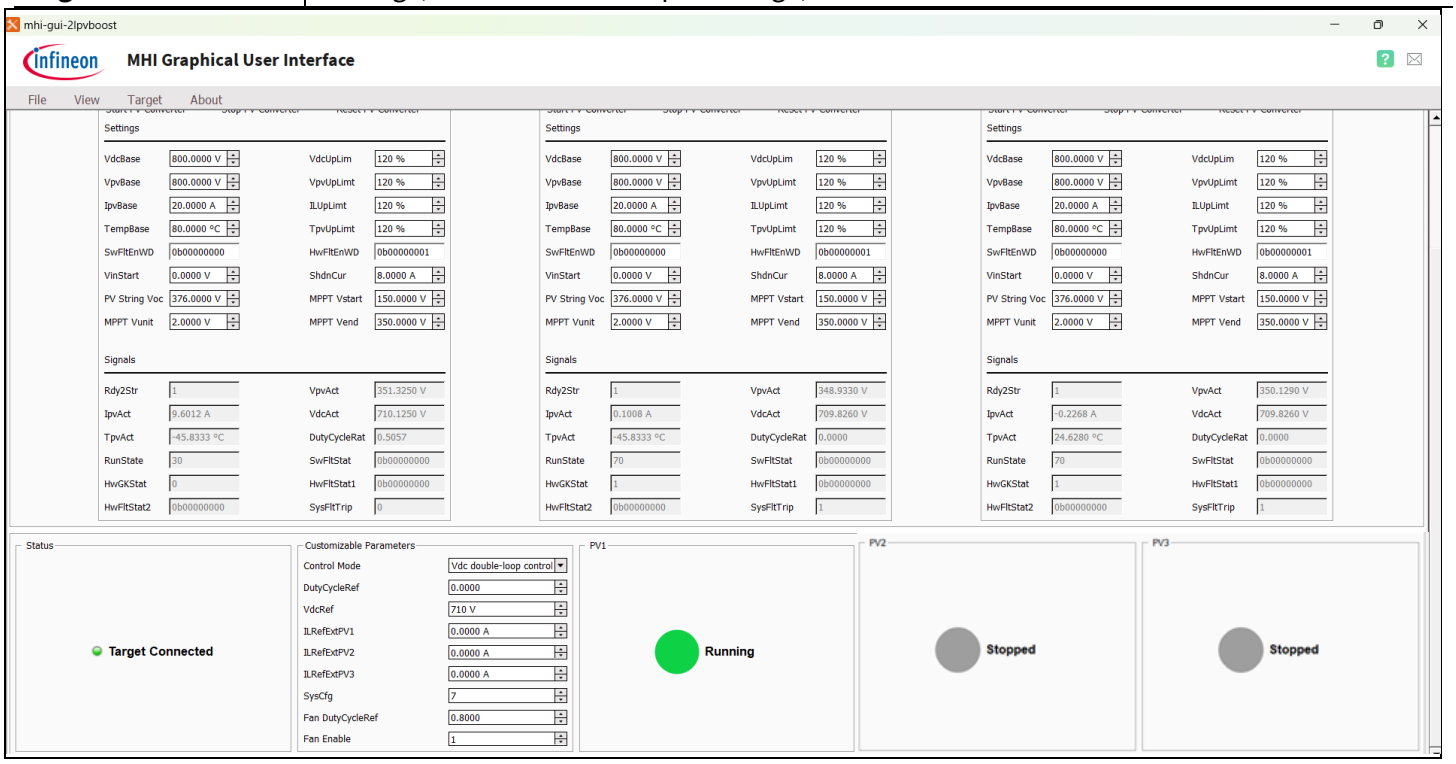


Figure 79 **GUI for V_{dc} double-loop control operation for channel 1**

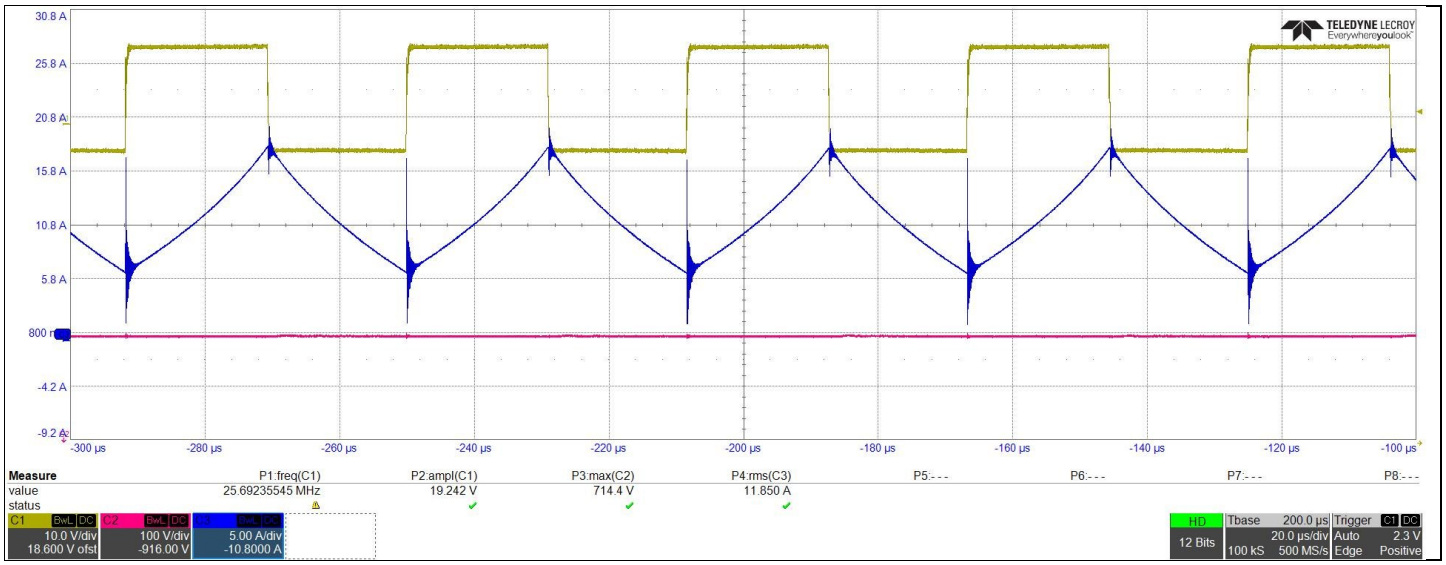


Figure 80 **Channel 1 waveforms**

5.2.3 MPPT control

Two different experiments were conducted to verify the effectiveness of MPPT control, one was steady state performance test, and the other one was dynamic performance test. For the steady state performance test, the DC bus was set to 650 V, the light intensity to 1000 W/m², and the temperature was set to 25°C. The results are shown in Figure 81.

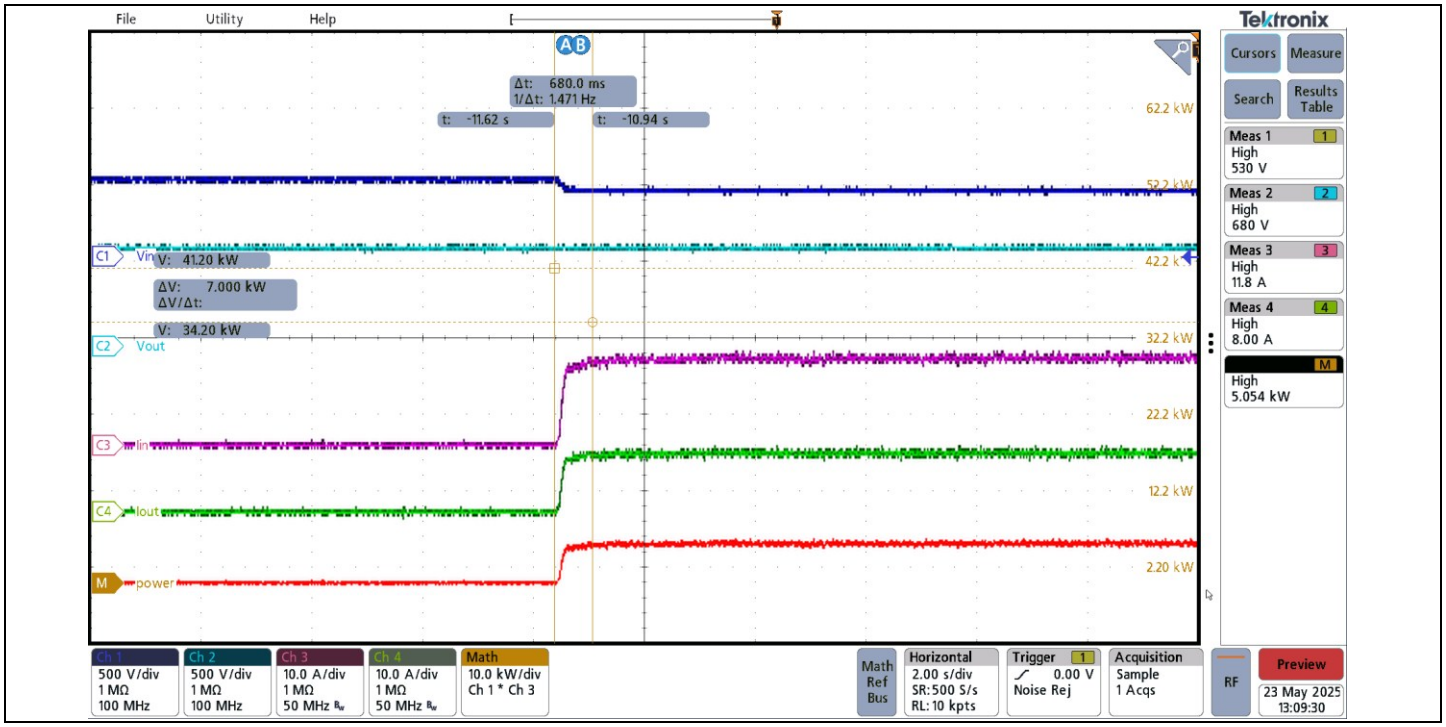


Figure 81 **650 V output voltage, 1000 W/m² light intensity, 25°C**

- Channel 1: Input voltage
- Channel 2: Output voltage
- Channel 3: Input current
- Channel 4: Output current
- Channel 5: Power

The efficiency result of the 650 V output voltage along with 1000 W/m² light intensity and 25°C are shown in Figure 822.

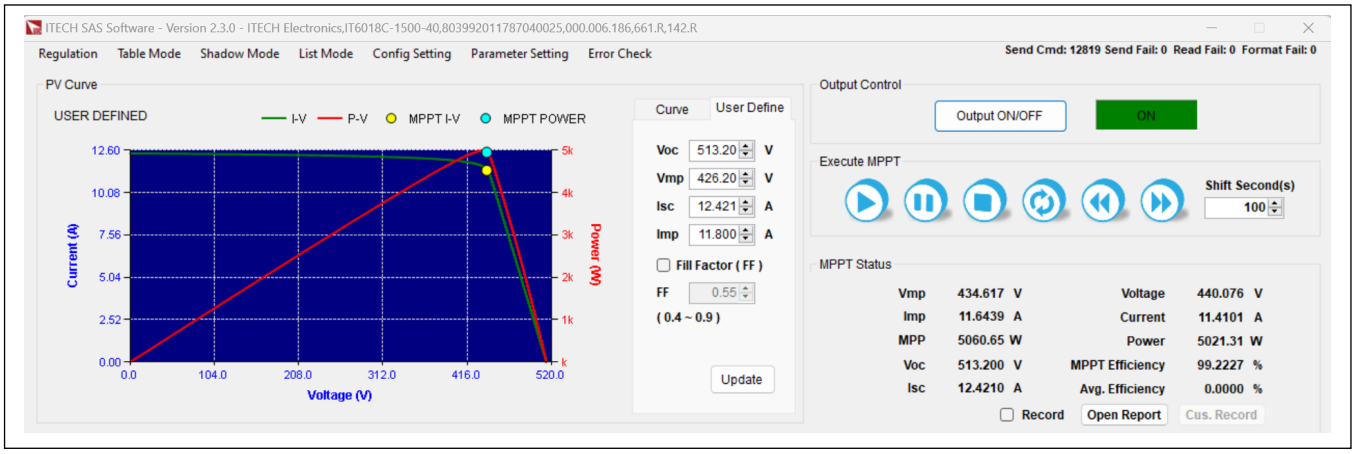


Figure 82 **Efficiency result of 650 V output voltage, 1000 W/m² light intensity, 25°C**

For the dynamic performance test, the DC bus was set to 650 V, temperature was 25°C, the light intensity was changed from 600 W/m² to 1000 W/m². The results are shown in Figure 83.

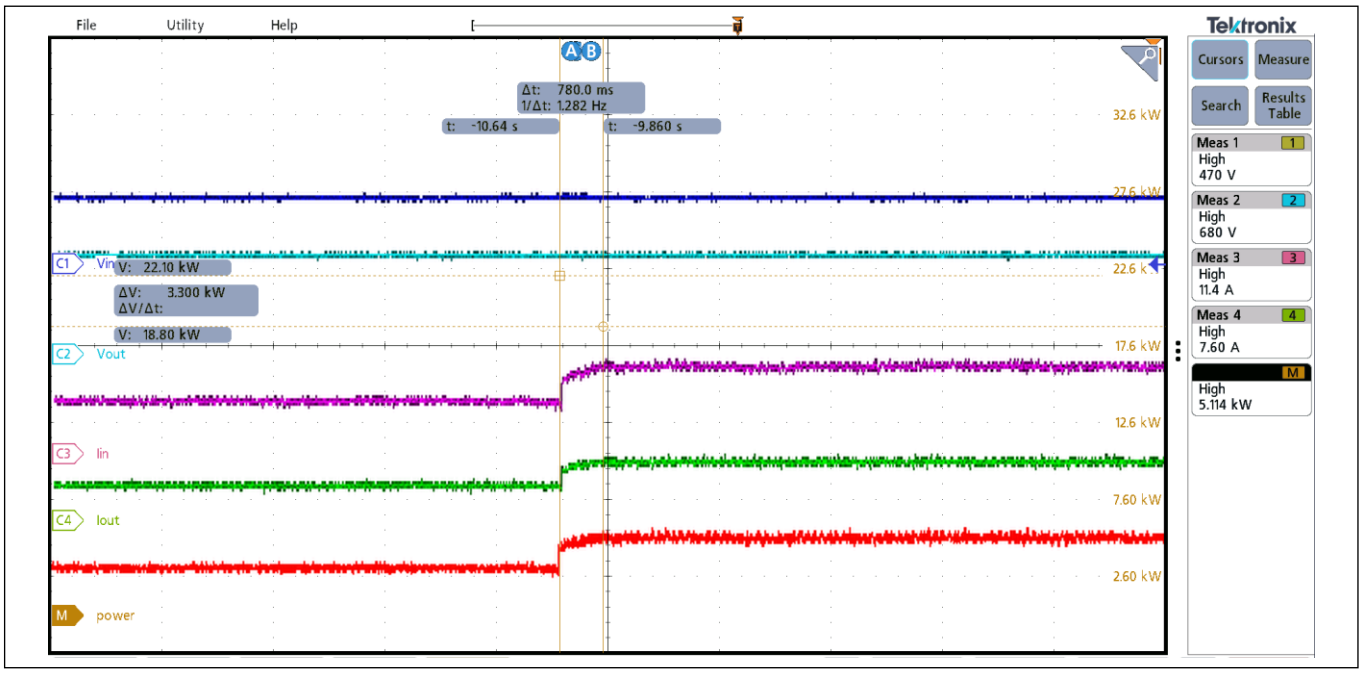


Figure 83 **650 V output voltage, 600 W/m² to 1000 W/m² light intensity, 25°C**

The efficiency result of the 650 V output voltage, light intensity changes from 600 W/m² to 1000 W/m², and 25°C is shown in Figure 844.

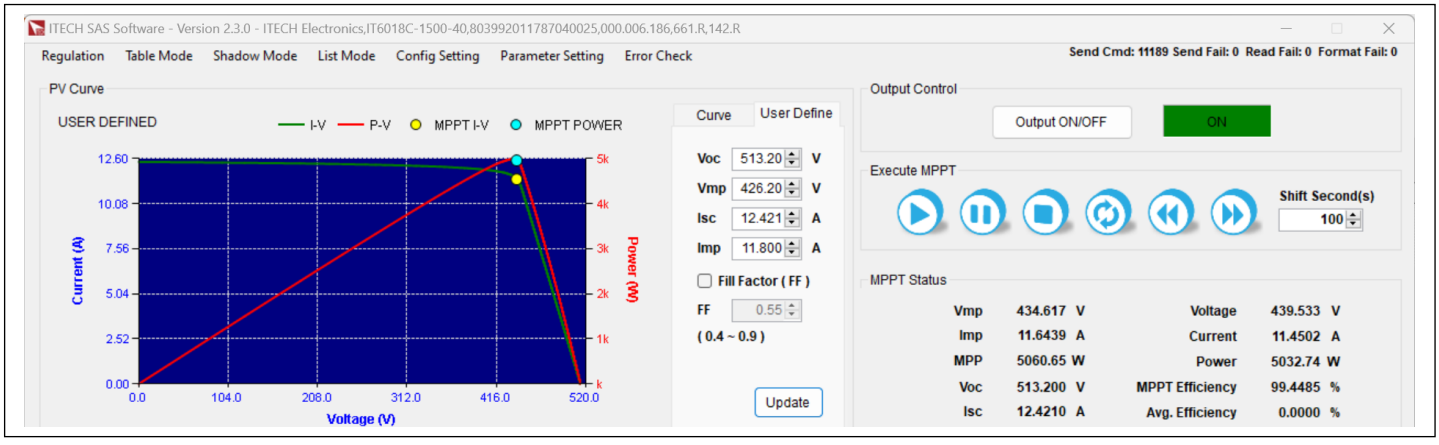


Figure 84 **Efficiency result of 650 V output voltage, 600 W/m² to 1000 W/m² light intensity, 25°C**

5.2.4 Single-current control

Table 13 Test specification

Input voltage	350 V
Output voltage	700 V
Output current	4.45 Amp
Inductor current ref	7.5 Amp
Output power	3.115 kW
Legend	Ch1: Vgk, Ch2: Channel 1 output voltage, Ch3: Inductor current

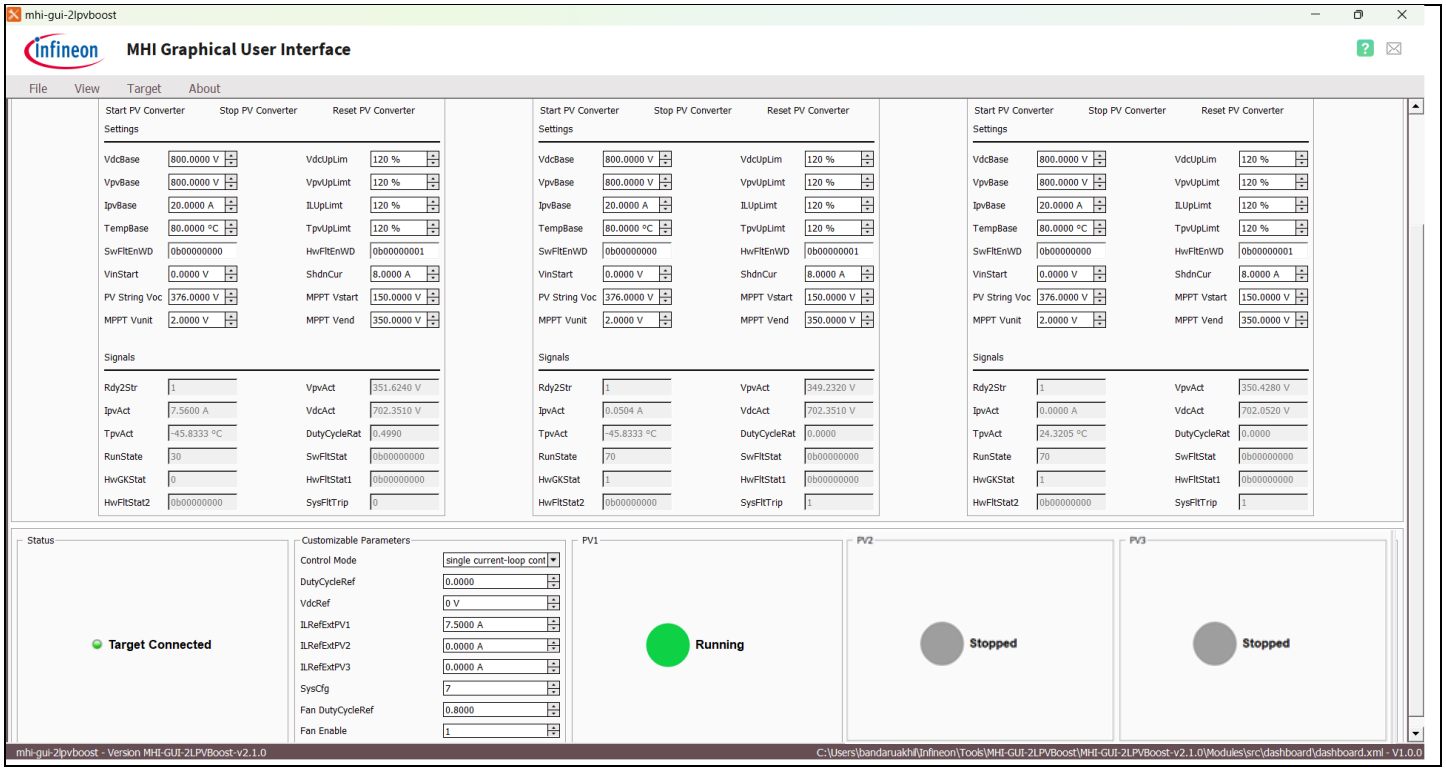


Figure 85 **GUI for the single-current loop**

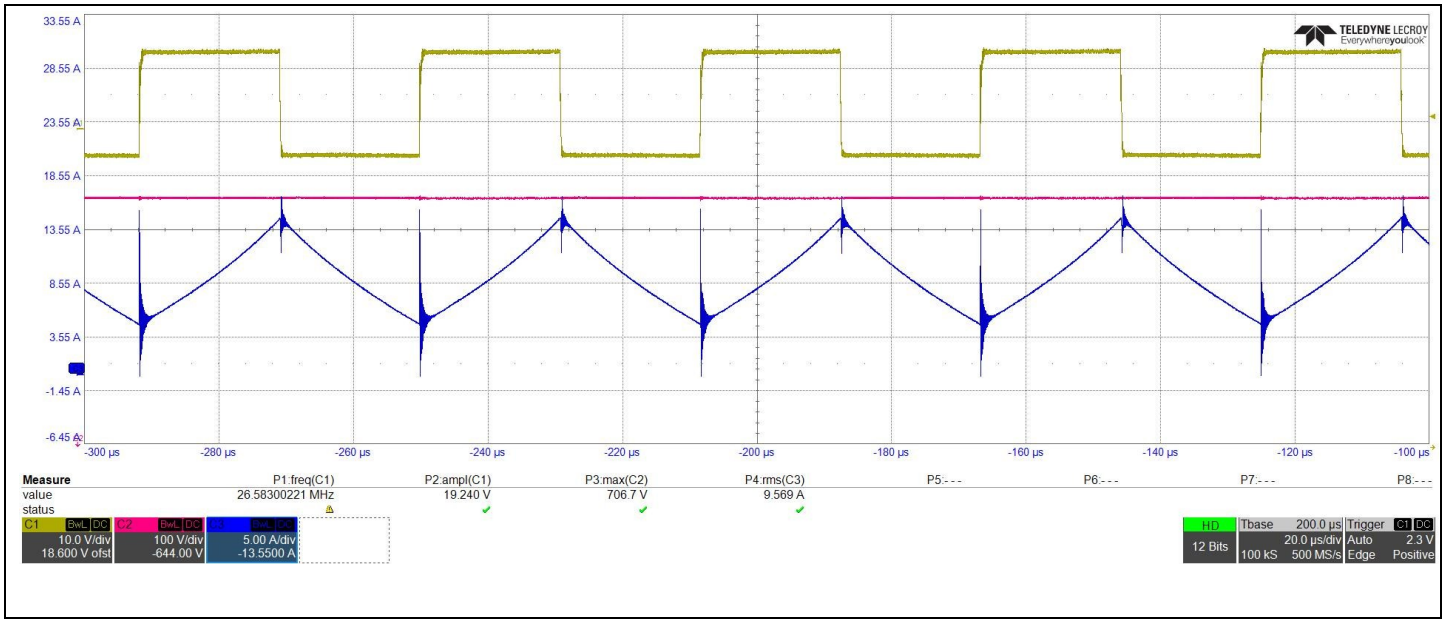


Figure 86 **Waveforms for the single-current loop**

5.2.5 Interleaved boost operation

Table 14 Test specification

Input voltage	400 V
Output voltage	800 V
Frequency	24 kHz
Output power	15 kW
Legend	Ch1: Inductor current 1, Ch2: Inductor current 2, Ch3: Inductor current 3, Ch4: V_{gk} of channel 1

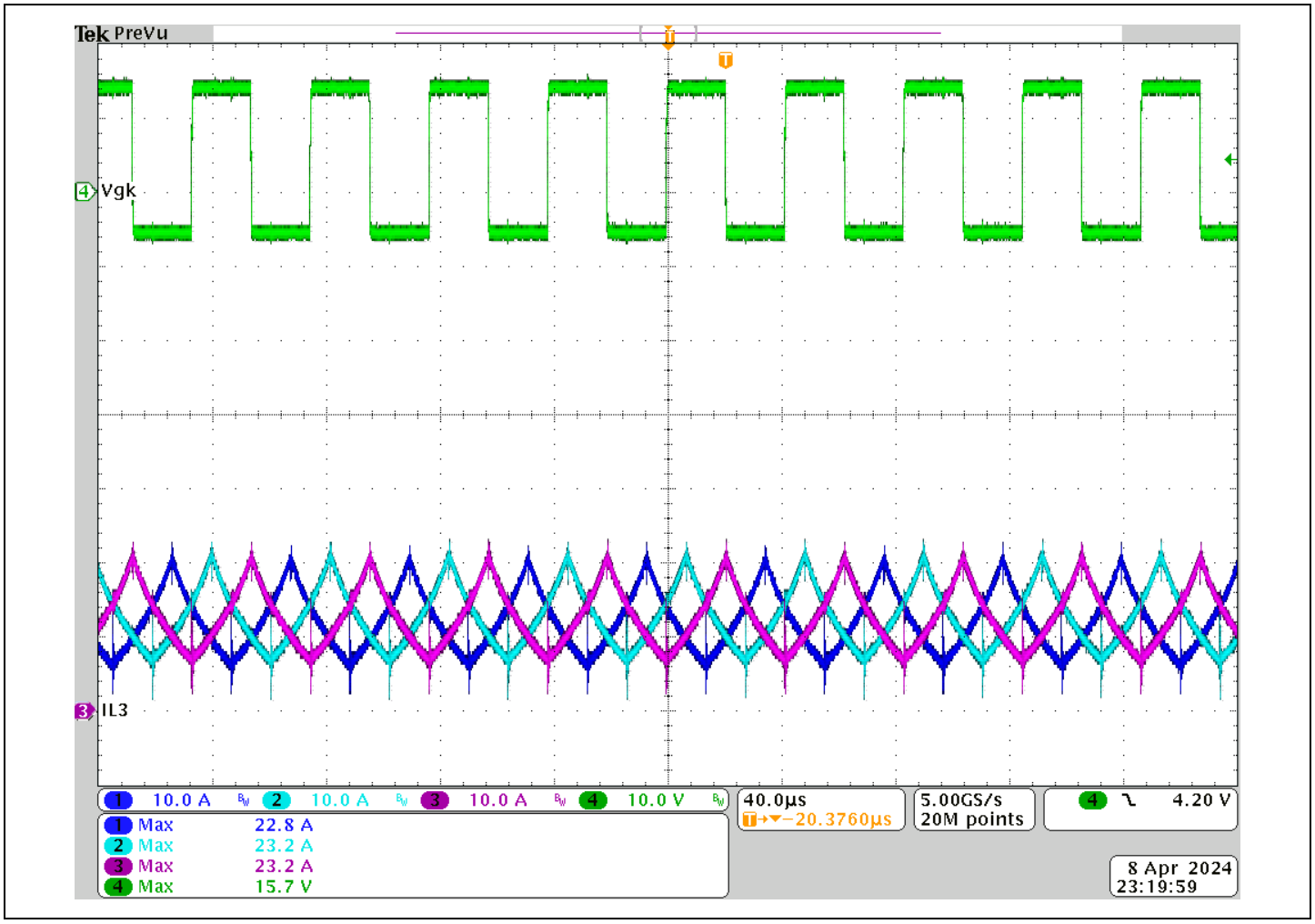


Figure 87 **Interleaved operation**

5.2.6 DC-link voltage ripple

Table 15 Test specification

Input voltage	400 V
Output voltage	800 V
Frequency	24 kHz
Output power	15 kW
Legend	Ch1: Inductor current, Ch3: V_{gk}, Ch4: DC-link voltage

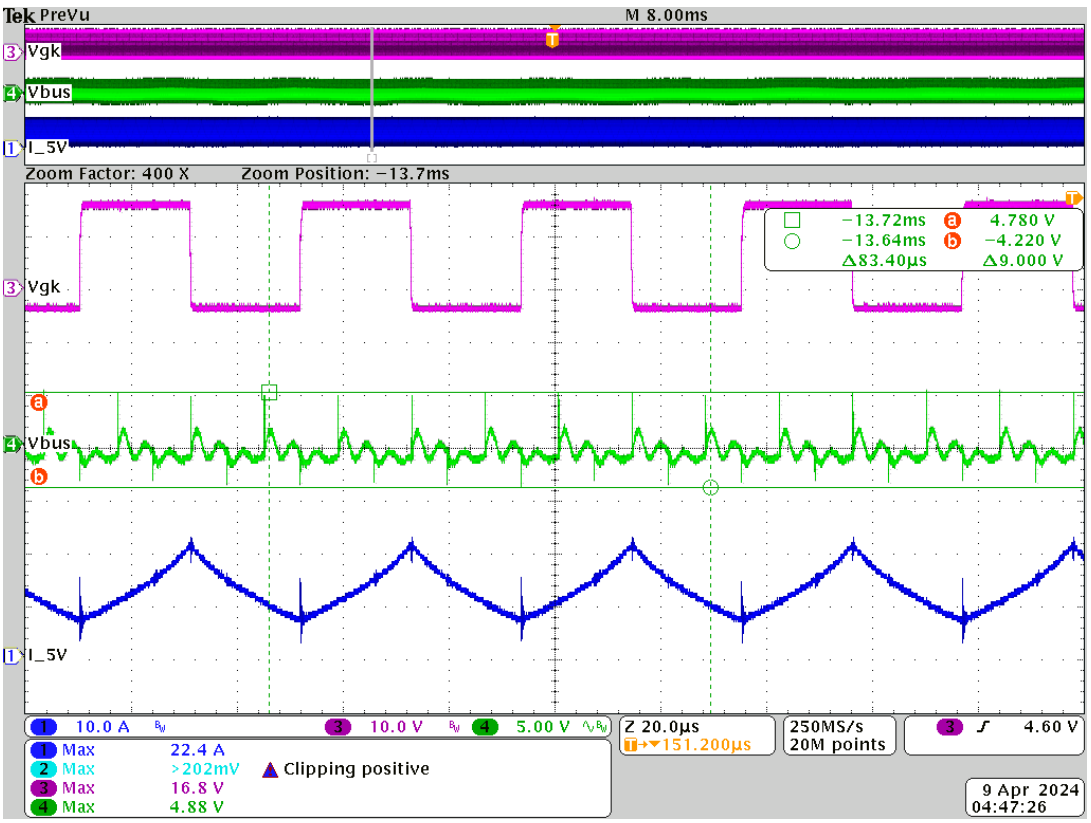


Figure 88 **DC-link voltage ripple**

5.2.7 Soft turn-off

The aim is to validate the soft turn-off function enabled by using the two-level slew rate control gate driver. When a gate-kill condition occurs (the gate-kill signal becomes low) the gate driver should shift to a higher value for the gate resistor, resulting in a soft turn-off.

Legend: Ch3: V_{gk}, Ch4: Gate-kill signal

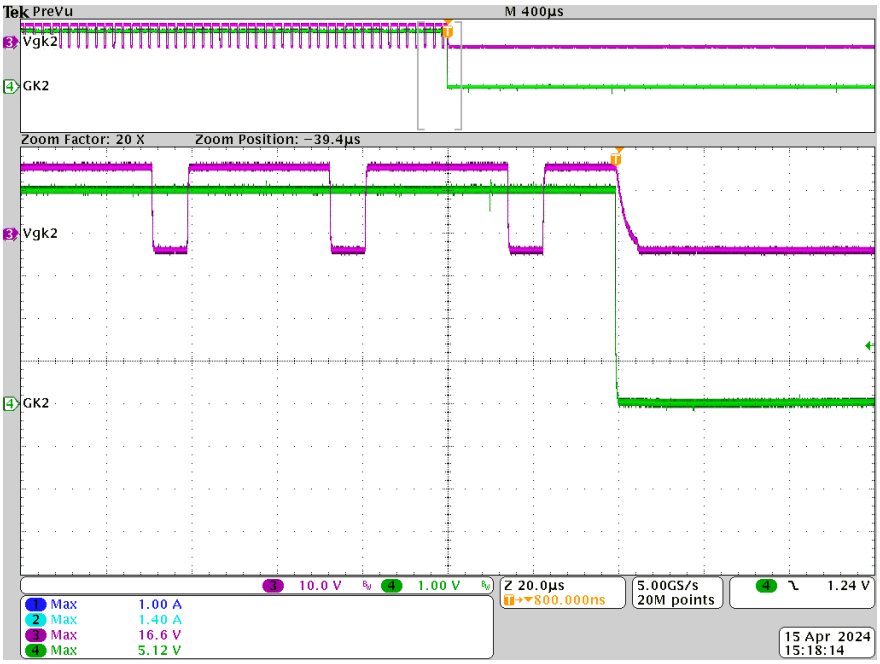


Figure 89 **Soft turn-off**

Legend: Ch1: INF, Ch2: IN, Ch3: V_{gk}

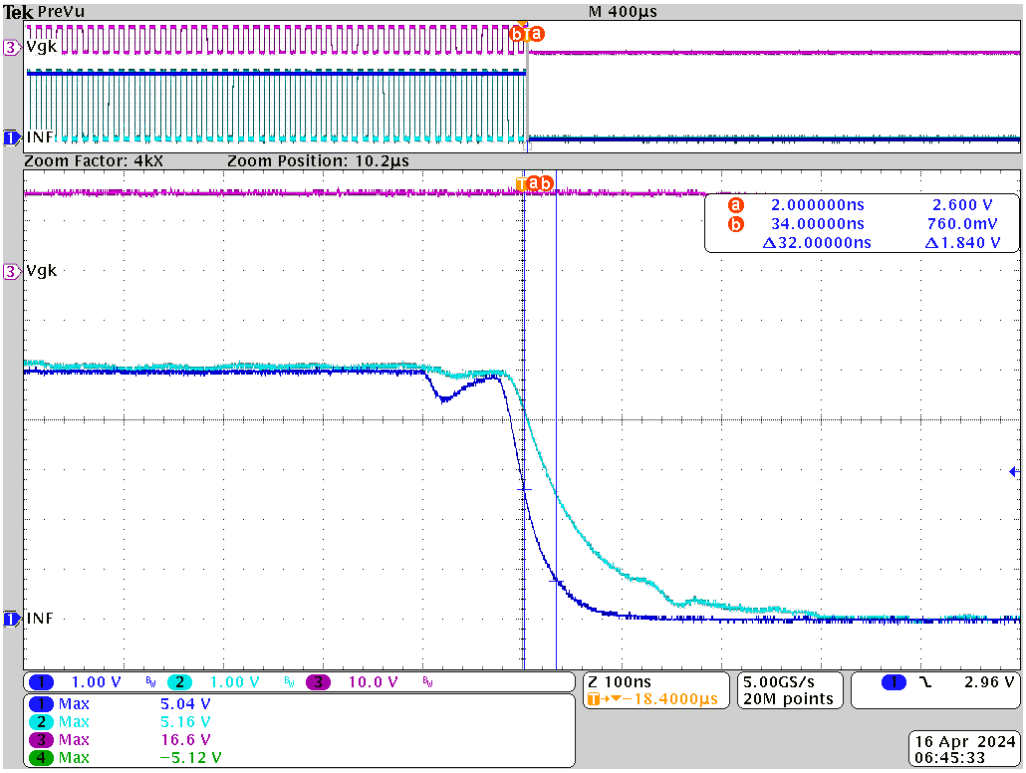


Figure 90 **IN and INF timing**

5.2.8 Inductor overcurrent protection

Table 16 Test specification

Specification	OCD1 programmed to 52 A
Input voltage	10 V
Duty cycle	0.9
Conclusion	The soft turn-off is activated when OCP occurring. (Due to the large duty-cycle, the soft turn-off can be easily triggered)
Legend	Ch2: Inductor current, Ch3: V_{gk}, Ch4: V_{ce}

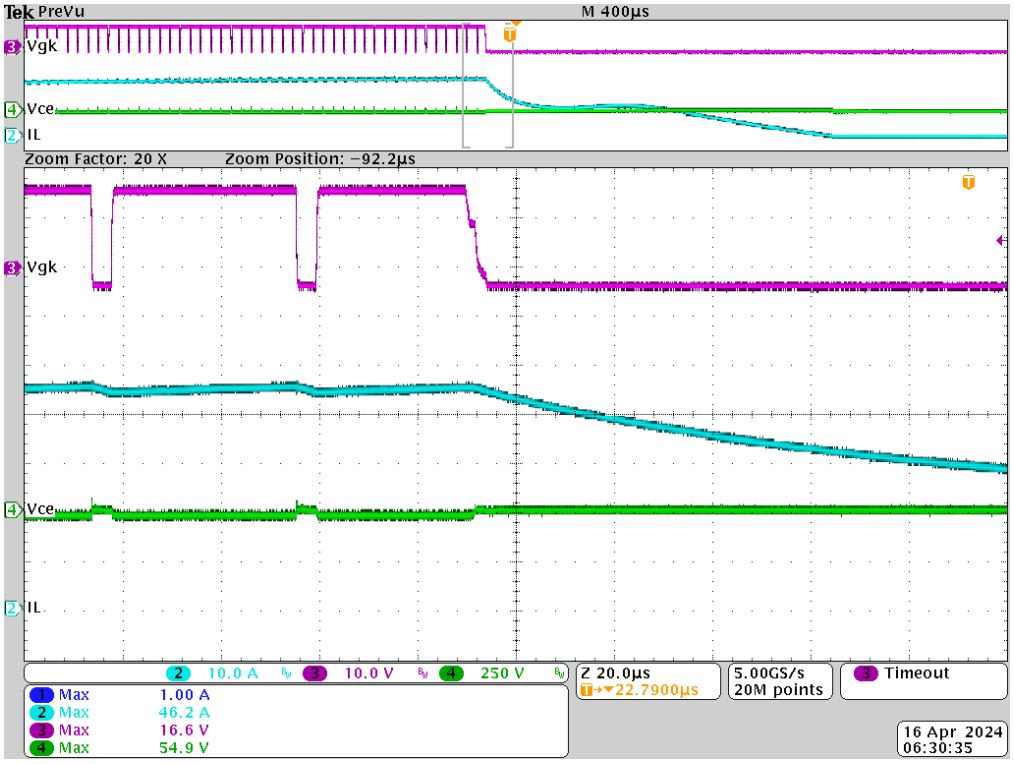


Figure 91 **OCP for channel 1**

5.2.9 Input overvoltage protection

Table 17 Test specification

Specification	The input OVP threshold is set to 883 V
Input voltage	890 V
Duty cycle	0.05
Output resistance	1000 V/5 A
Conclusion	OVP for channel 1: 875 V (Note: due to the small duty-cycle, the soft turn-off may not be easily triggered)
Legend	Ch2: Inductor current, Ch3: Vgk, Ch4: V_{in}

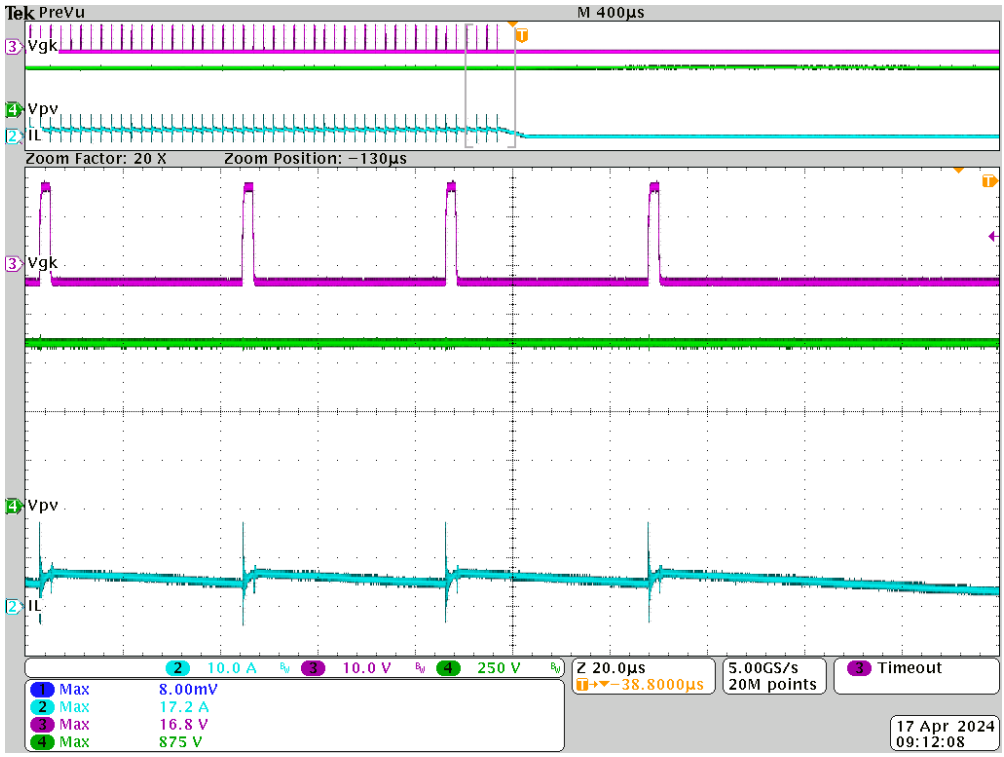


Figure 92 **OVP for channel 1**

5.2.10 DC-link overvoltage protection

Table 18 Test specification

Specification	The DC-link OVP threshold is set to 992 V
Input voltage	890 V
Duty cycle	0.1
Output resistance	1000 V/5 A
Conclusion	OVP for channel 1: 985 V
Legend	Ch2: Inductor current, Ch3: V_{gk}, Ch4: $V_{DC\text{-}link}$

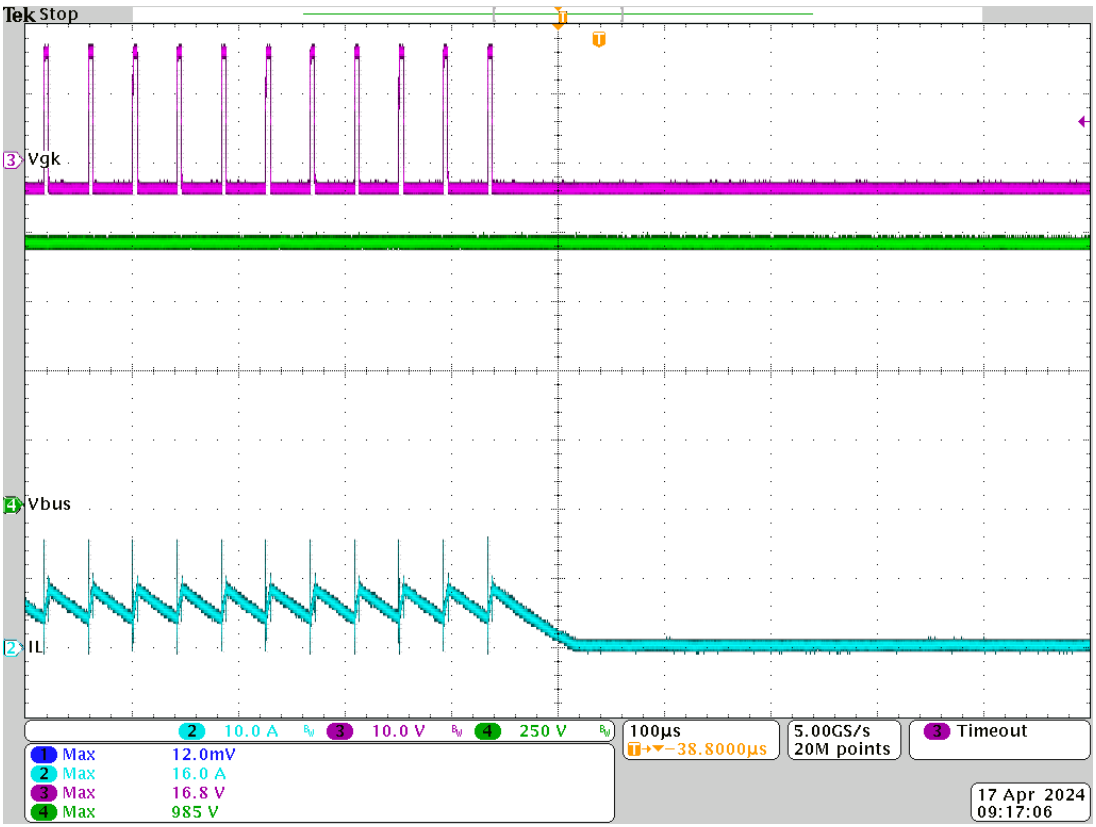


Figure 93 **DC-link OVP for channel 1**

5.2.11 Efficiency measurement

Table 19 Power semiconductors efficiency measurement

Specification	Efficiency measurement using the Zimmer LMG 670 power analyzer
Condition	Duty cycle = 0.5, V_o = 650 V, Loading = 10,20,30,50,75 and 100% Measurements are taken after the boost inductor (power semiconductor losses) for only one channel

Loading	Efficiency
10% load	98.1%
20% load	98.4%
30% load	98.6%
50% load	98.8%
75% load	98.8%
100% load	98.7%

5.2.12 24 V – 5 V auxiliary power supply

Table 20 Test specification

Specification	Output voltage, ripple, and current measurement
Input voltage for Aux power supply	24 V
Input voltage	400 V
Output voltage	800 V
Output power	15 kW
Legend	Ch1: Io, Ch2: Vo

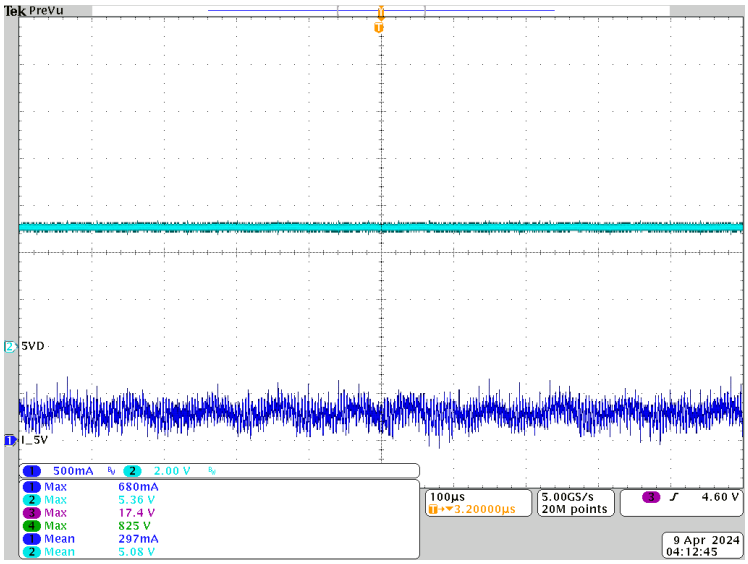


Figure 94 **Output voltage and current of the auxiliary power supply**

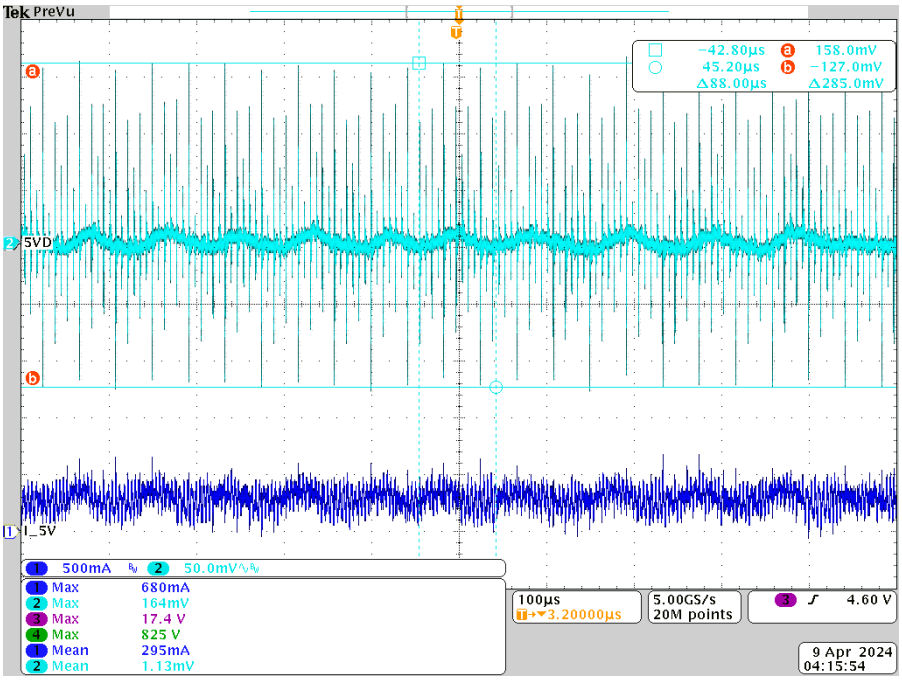


Figure 95 **Voltage ripple and noise of the auxiliary power supply**

6 Board layout

6.1 REF-15KW2LBOOST power conversion main board

Table 21 Mechanical data

Dimensions	260.01 mm x 190 mm
No. of layers	4
Copper thickness	140 µm
Weight	4.5 kg

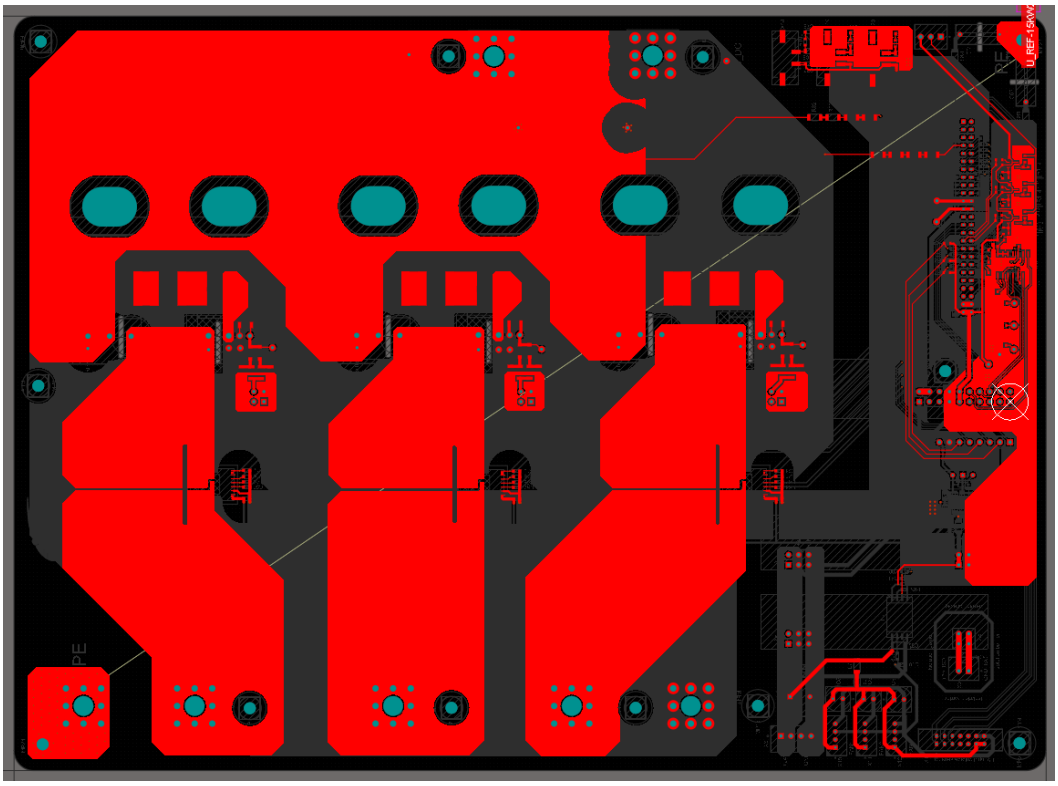


Figure 96 **Layer 1**

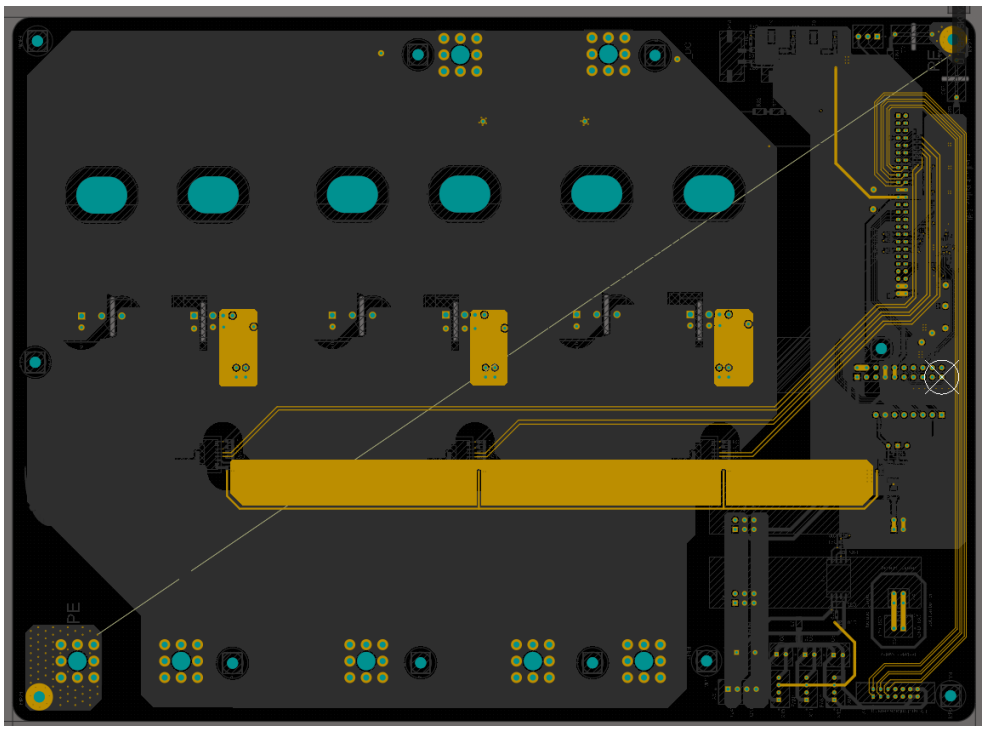


Figure 97 **Layer 2**

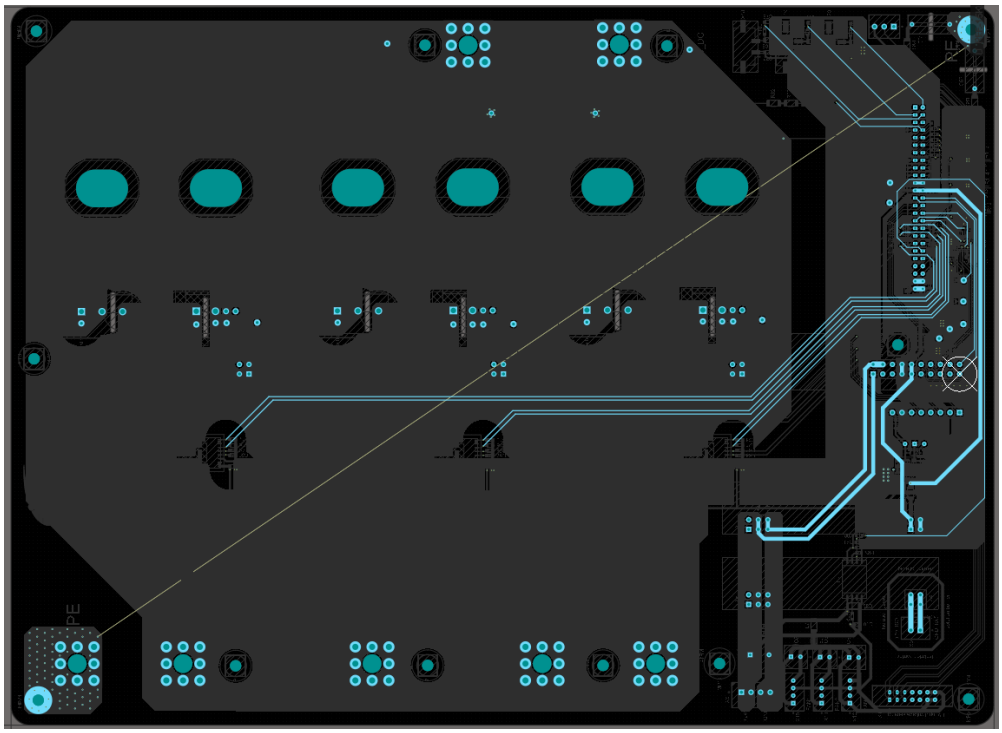


Figure 98 **Layer 3**

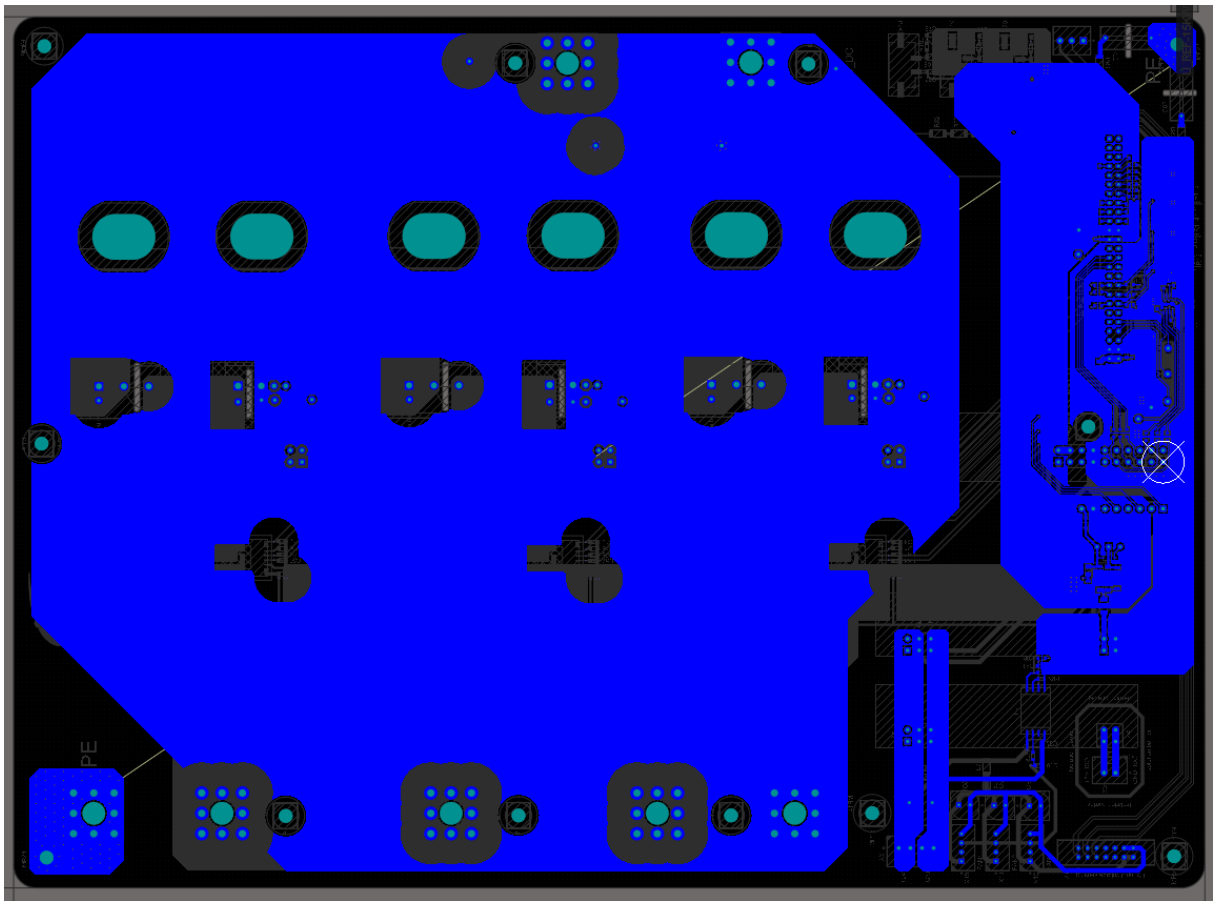


Figure 99 **Layer 4**

6.2 ISODRV-3240C3P15N05-1

Table 22 ISODRV-3240C3P15N05-1 Mechanical data

Dimensions	210 mm x 40 mm
No. of layers	2
Copper thickness	70 µm

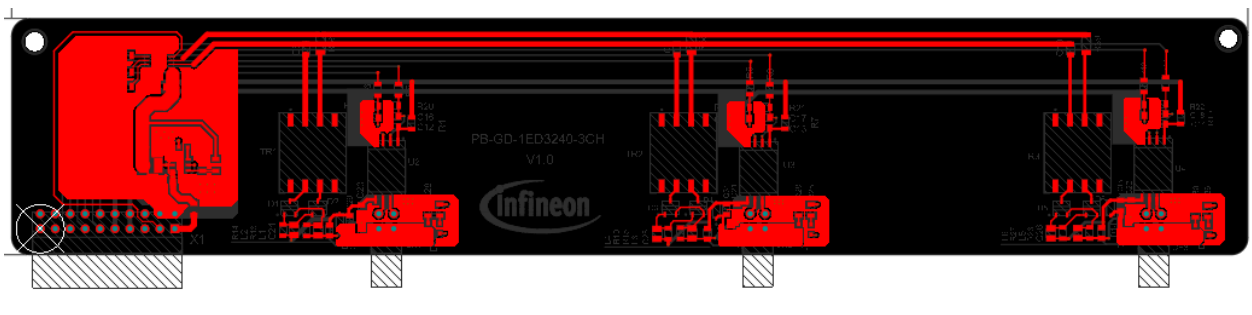


Figure 100 **Layer 1**

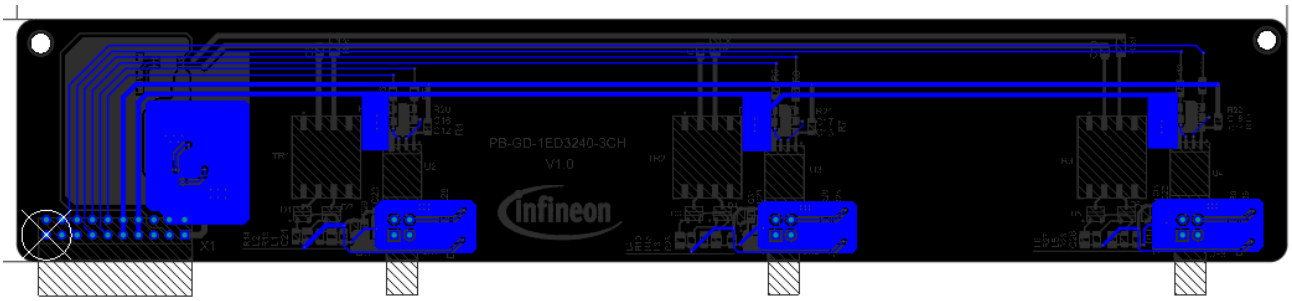


Figure 101 **Layer 2**

6.3 PB-APS-24V-5V ISO

Table 23 Mechanical data

Dimensions	57.1 mm x 27.1 mm
Number of layers	8
Copper thickness	70 µm

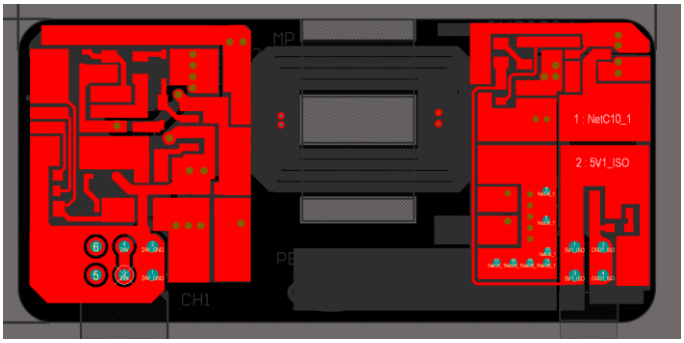


Figure 102 **Layer 1**

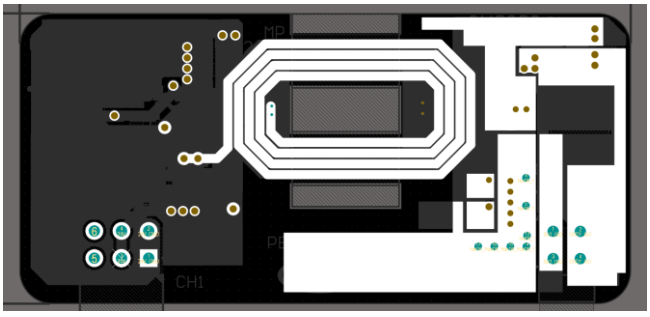


Figure 103 **Layer 2**

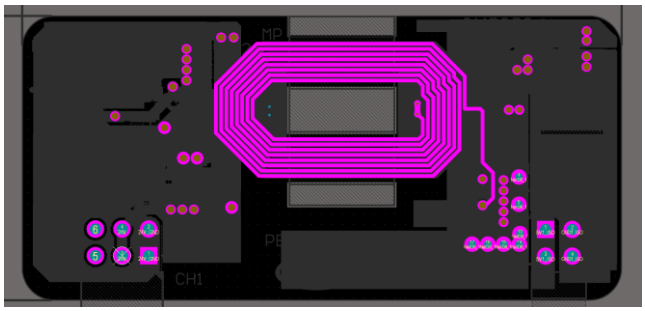


Figure 104 **Layer 3**

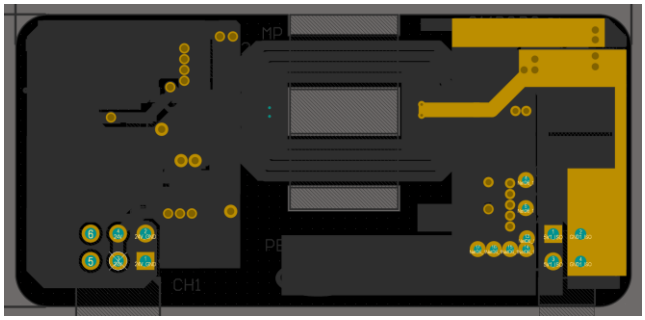


Figure 105 **Layer 4**

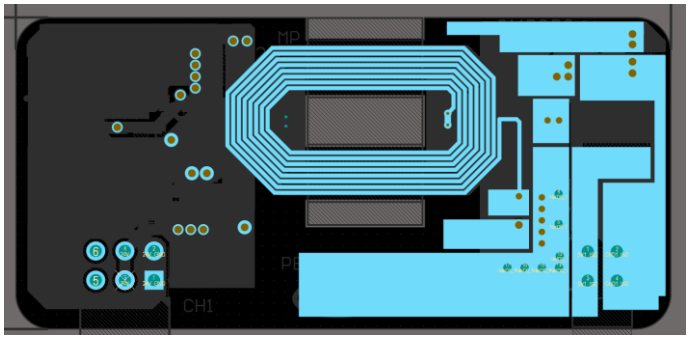


Figure 106 **Layer 5**

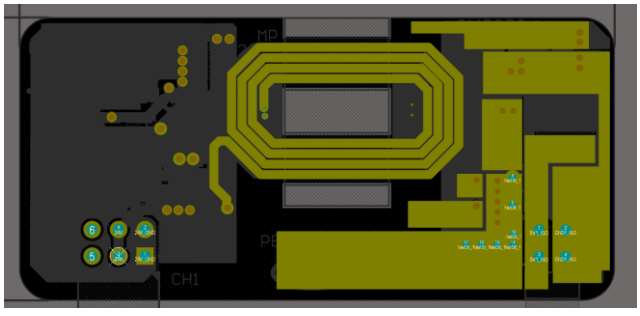


Figure 107 **Layer 6**

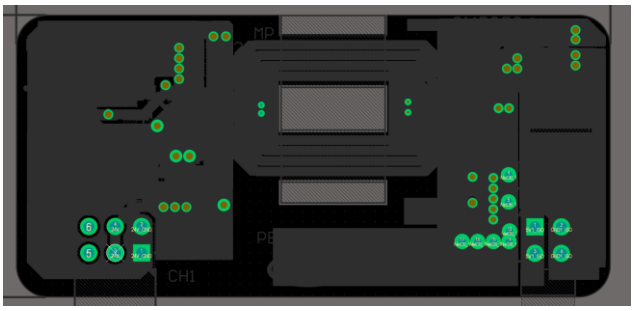


Figure 108 **Layer 7**

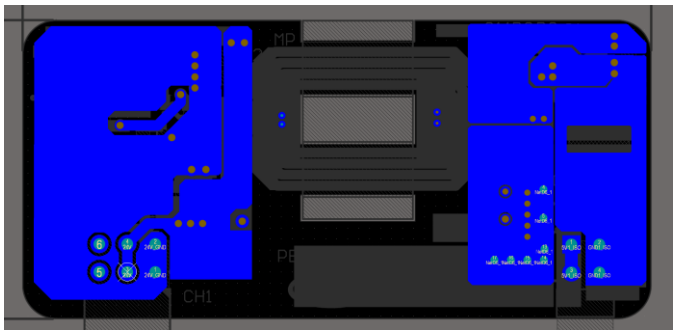


Figure 109 **Layer 8**

6.4 REF-15KW2LBOOST-Filter

Table 24 Mechanical data

Dimensions	230 mm x 220 mm
Number of layers	4
Copper thickness	35 µm
Weight	2.5 kg

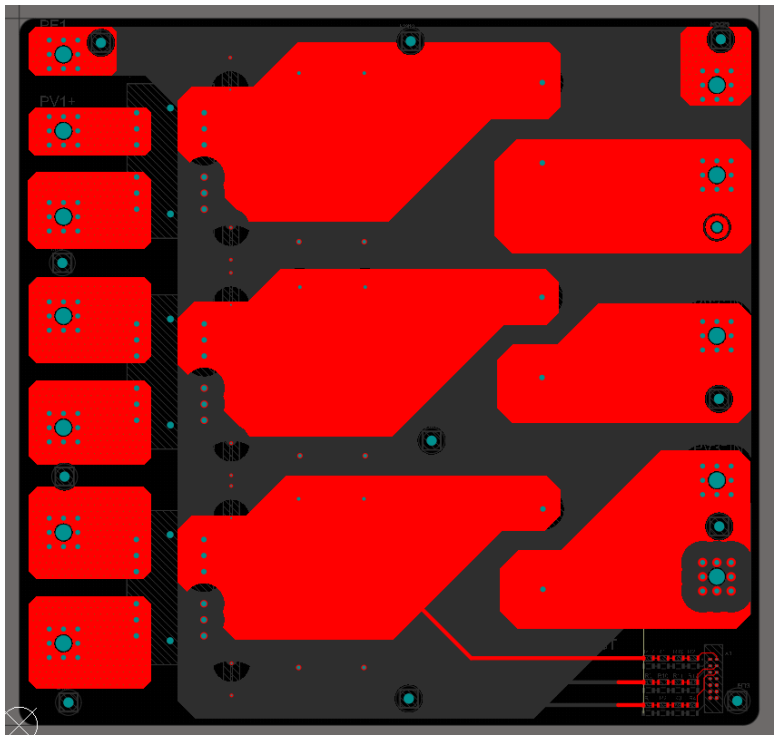


Figure 110 **Layer 1**

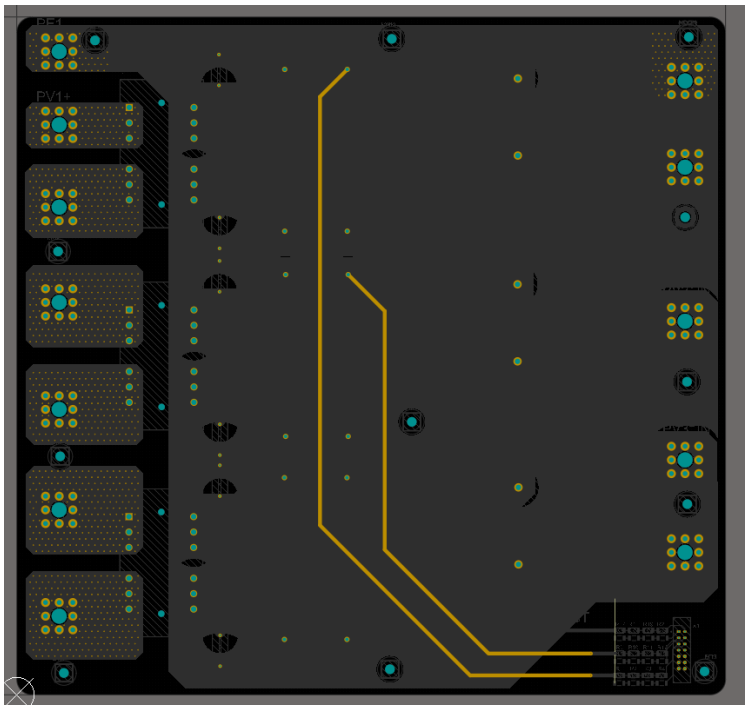


Figure 111 **Layer 2**

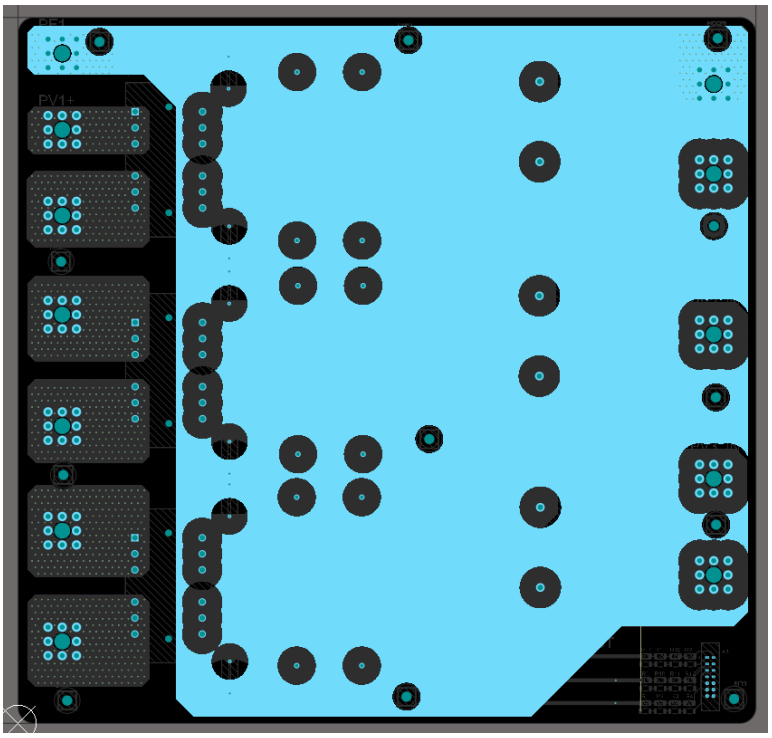


Figure 112 **Layer 3**

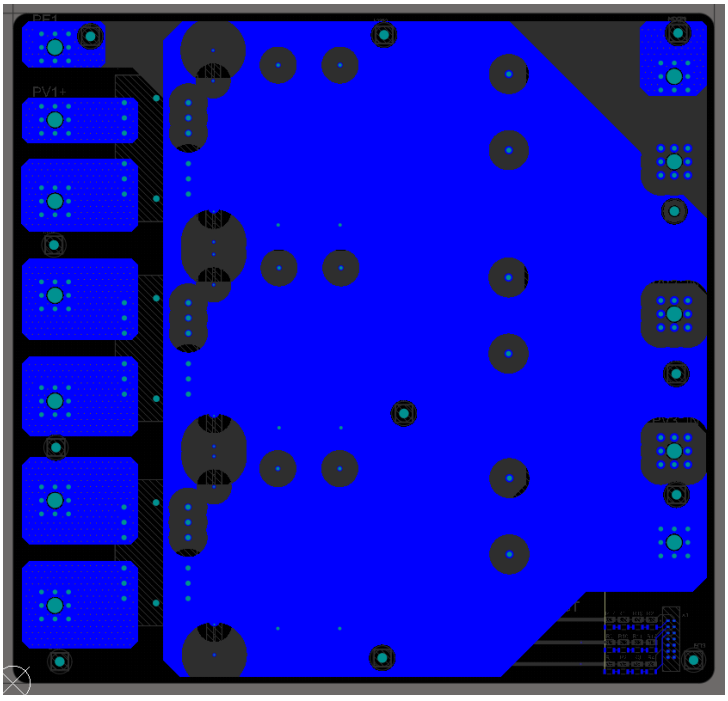


Figure 113 **Layer 4**

6.5 PB-CAPTANK-1.1KV

Table 25 Mechanical data

Dimensions	280 mm x 170 mm
Number of layers	4
Copper thickness	35 µm
Weight	1.7 kg

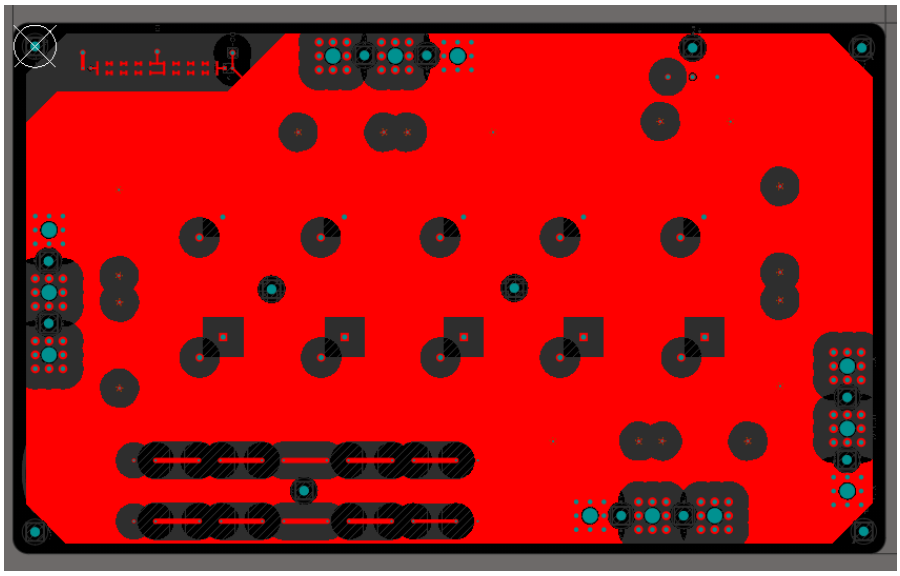


Figure 114 **Layer 1**

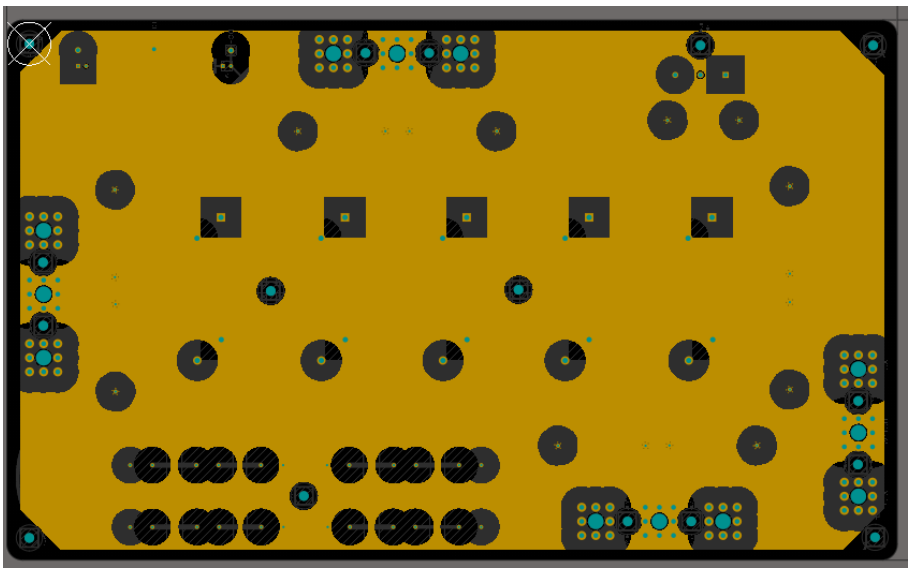


Figure 115 **Layer 2**

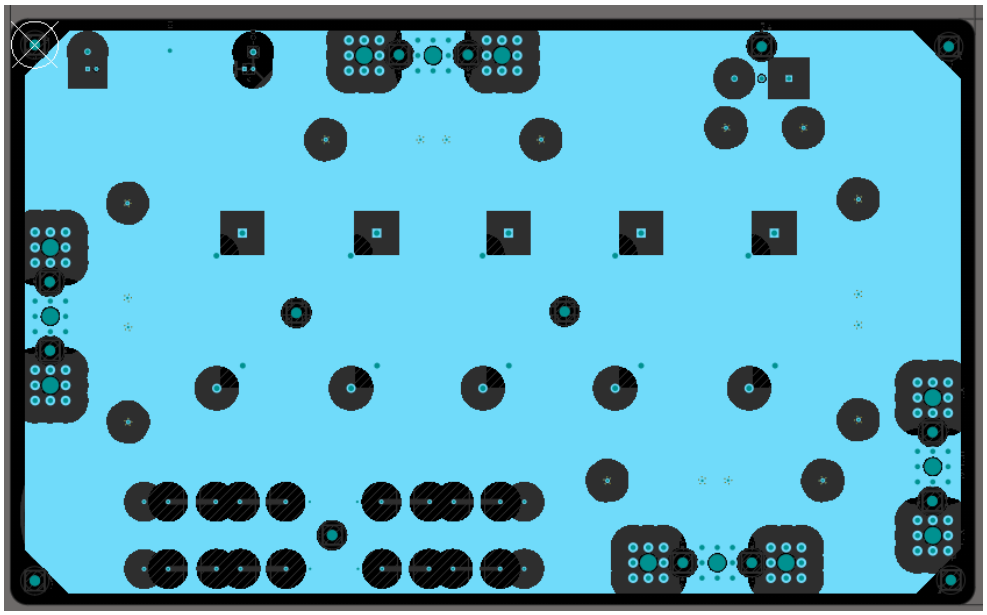


Figure 116 **Layer 3**

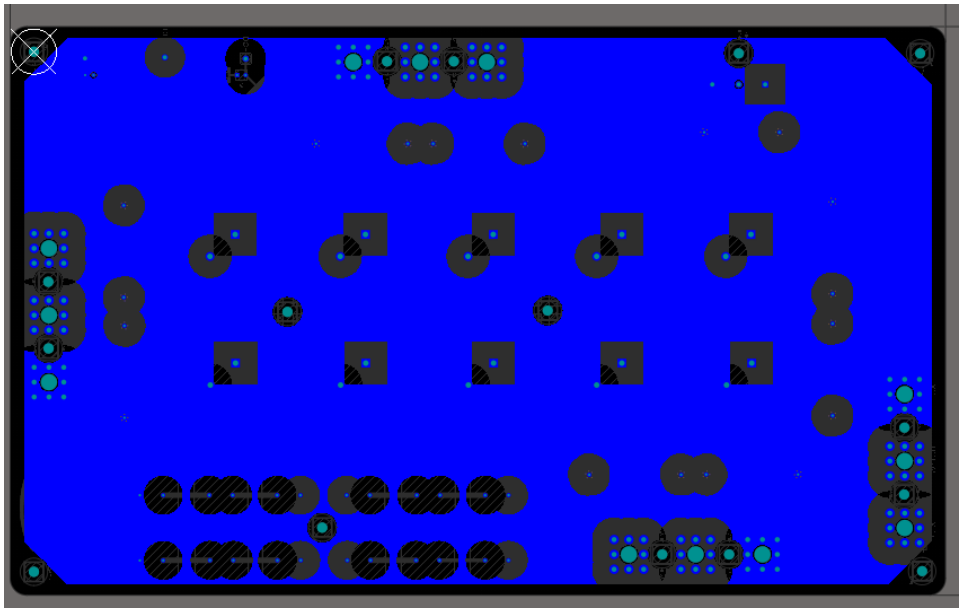


Figure 117 **Layer 4**

7 Bill of materials

Table 8 lists the key materials.

Table 26 BOM

Part	Description
IKZA40N120CH7	1200 V, 40 A IGBT with anti-parallel diode in a TO-247 4-pin package
IDW20G120C5	1200 V Silicon carbide Schottky diode in a TO-247-2 package
1ED3240MC12H	10 A, 5.7 kV (rms) single-channel isolated gate driver with two-level slew-rate control, UL 1577 and VDE 0884-11 certified
TLI4971-A120T5-U-E0001	High precision coreless current sensor for industrial applications
2EP130R	Full-bridge transformer driver
IRS27952	Half-bridge high-voltage controller IC
IRF7351	60 V dual N-channel HEXFET power MOSFET in an SO-8 package
TLE42744GS V33	3.3 V LDO

Revision history

Document version	Date of release	Description of changes
V.1.0	2024-07-18	Initial release
V.1.1	2025-11-18	Updated converter control design, operation and test results

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