10 kW 3-level NPC2 inverter reference design with CoolSiC™ in a top-side cooled QDPAK package

REF-10KW3LNPC2Q

About this document

Scope and purpose

This user guide describes the NPC2 inverter reference design REF-10KW3LNPC2Q with its main features, key data, pin assignments, mechanical dimensions, and electrical interfaces.

Intended audience

This user guide is meant for engineers and technical specialists working on solar photovoltaic and energy storage solutions and similar domains. The concept of this power conversion reference design is modular so that the hardware can also be reused for various other power converter applications and use cases.

Reference design

This reference design is not a qualified and certified commercial product. The hardware does not necessarily meet any safety, EMI, or quality standard (for example, UL, CE) requirements.

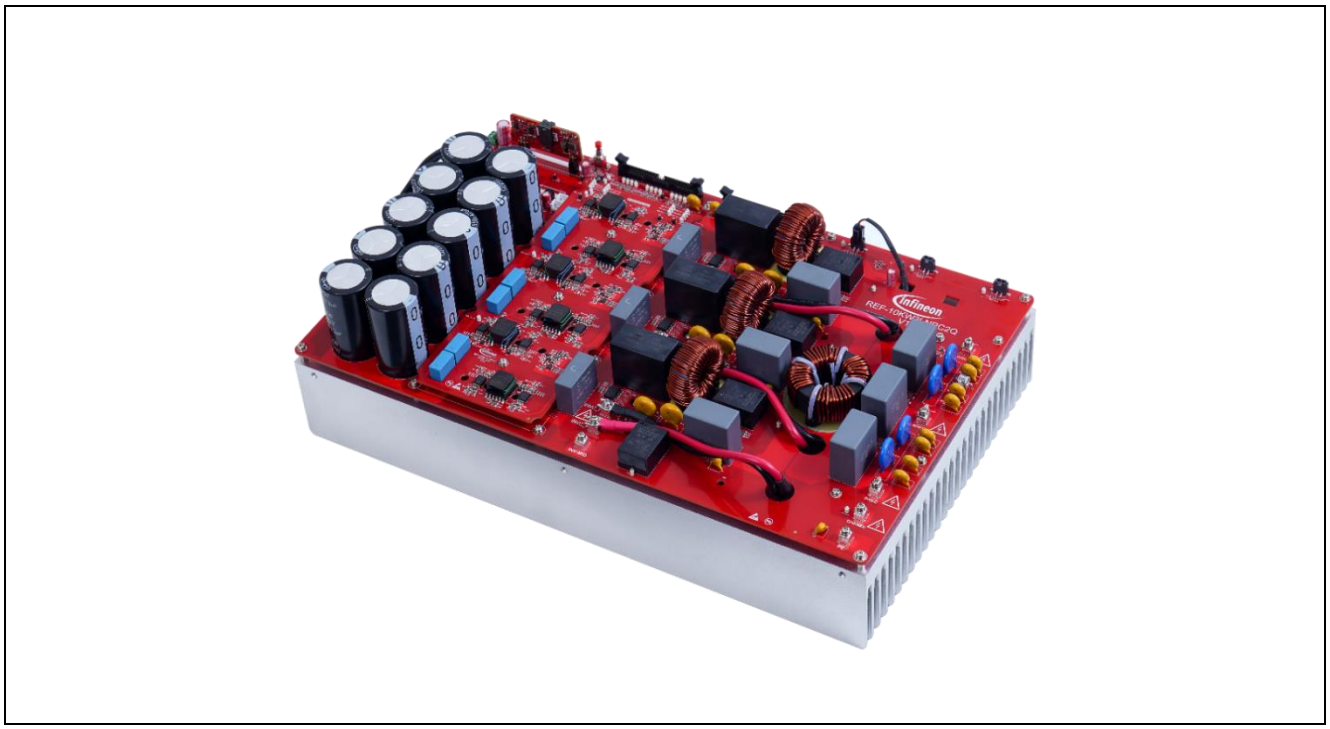

Figure 1 **Power conversion board REF-10KW3LNPC2Q**

Note: *PCB and auxiliary circuits are NOT optimized for final customer design. Please* read the “Important notice” and the “Safety precautions” sections in this document.

Important notice

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems

Table 1 Safety precautions

	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning**: *controller board must be connected to the main power board before powering the DC bus.*
	**Warning:** *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with power electronics should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

Table of contents

1 The power conversion board at a glance

1.1 Introduction

REF-10KW3LNPC2Q is a three-phase, three-level NPC2 inverter and comes as an integrated kit that includes different boards to help users build and operate an NPC2 inverter power stage. The kit includes:

- REF-10KW3LNPC2Q_MB: The NPC2 inverter power stage motherboard that integrates EMI filters and DC-link capacitors
- REF-10KW3LNPC2Q_GDB: A gate driver board with a three-phase drive, and four-channel per phase for each leg of the NPC2 type
- PB-APS-24V-5V ISO: An isolated auxiliary power supply

Users can also get an XMC7200-based control board separately. This board comes with signal-conditioning circuits, a power conversion software, and a GUI that enables the users to operate the inverter either in open-loop, V/F mode, or P/Q mode configurations.

The XMC7200 control board is available under the name REF-CLBXMC7PEC.

1.2 Top-level specifications

Table 2 Specifications

Parameter	Conditions	Value			Unit
		min.	typ.	max.	
Input (DC)					
Max. DC link voltage		–	–	1000	Volt
Operational DC link voltage	DC voltage	–	660	850	Volt
Output					
Grid connection		3Φ	–		
Rated AC output power	Ta = 45°C; derating above 45°C up to 60°C	–	–	10000	Watt
Maximum output power / rated apparent power	Ta = 45°C; derating above 45°C up to 60°C	–	11000	12000	Watt
Rated AC output current	Vout = 380V & Ta = 45°C	–	–	15.2	Amp
Rated AC output current	Vout = 400V & Ta = 45°C	–	–	14.5	Amp
Maximum AC output current	Vout = 380V & Ta = 45°C	–	–	18.2	Amp
Rated AC output voltage	3 / N / PE,	220 / 380 & 230 / 400			Volt
Grid frequency range		50	–	60	Hz
power factor			0.8	1.0	-
Maximum total harmonic distortion		< 3	–	–	%
Gate driver / controller data					
Input voltage for gate driver power supply		–	24	–	Volt

Input power supply	Gate driver primary, sensing and processing circuit	–	5	–	Volt
Switching frequency	Control algorithm: SVPWM	–	–	48	kHz
Protection					
Over-current protection	Peak, it should adjustable	30	–	36	APeak
Overvoltage protection	for DC bus	–	890	–	Volt
Over-temperature protection (Ambient)	Required, via ambient temperature measurement (PCB)		60		°C
Over-temperature protection (Case)	Required, via power device case temperature measurement		100		°C
General data					
Operating temperature	above 45 °C current derating	-25	–	60	°C
Cooling		Natural convection			–

Note: The default configuration for the DC-bus overvoltage protection on the XMC7200 control card, REF-CLBXMC7PEC, is set to 890 V. If this card is used for operating the NPC2 power conversion board, any voltage exceeding this threshold will trigger the overvoltage protection mechanism.

1.3 Key design building blocks

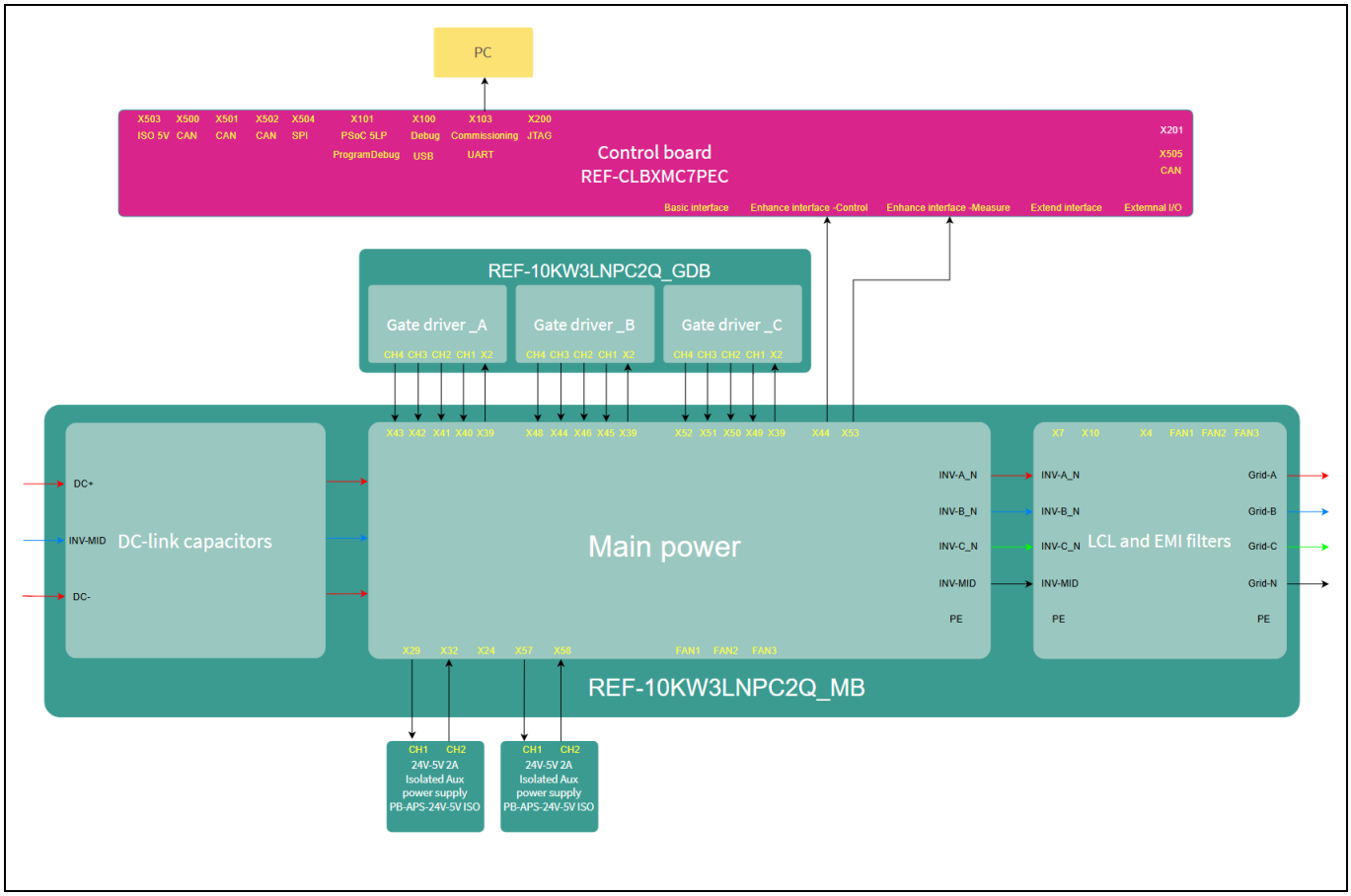


Figure 2 **Functional block diagram for NPC2 inverter**

Figure 2 shows how the different boards are connected to construct the NPC2 inverter. The main power board with integrated DC-link capacitors, power switches, sensing and LCL and EMI filters is in the center. A three-phase gate driver board is mounted on the top of the power board. An isolated power supply subsidiary card is also mounted on the top of the power board to provide an isolated 5 V rail.

Figures 3, 4, and 5 show these components individually – REF-10KW3LNPC2Q_MB, REF-10KW3LNPC2Q_GDB, and PB-APS-24V-5V ISO.

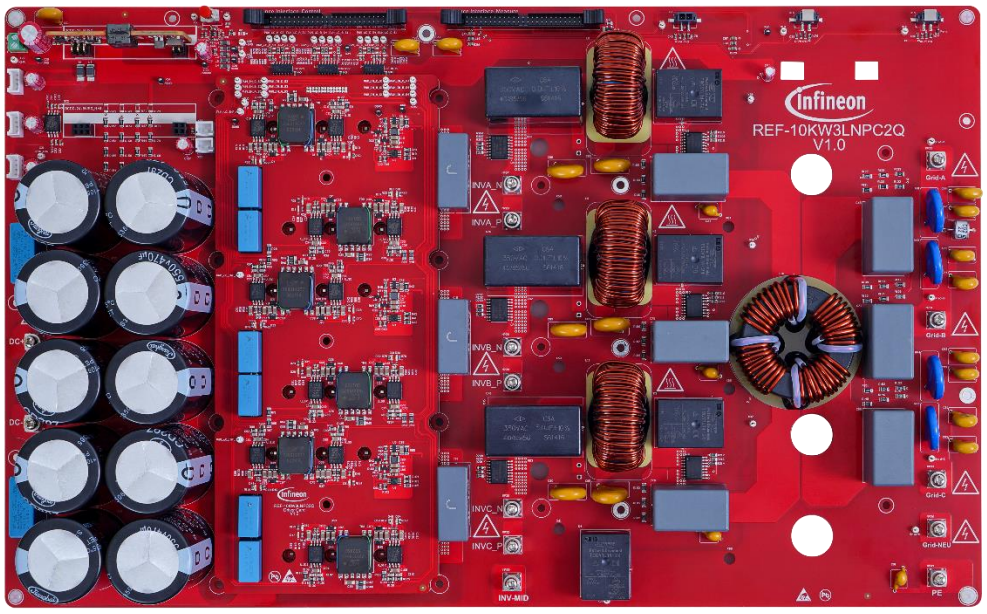


Figure 3 **Main Power Stage**

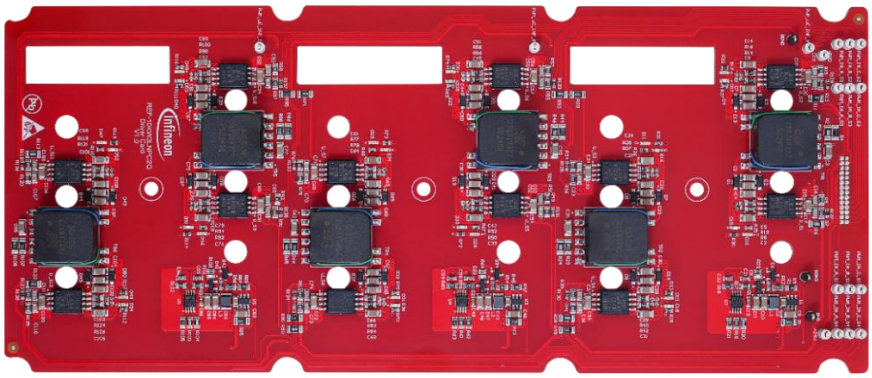


Figure 4 **Gate Driver Card**

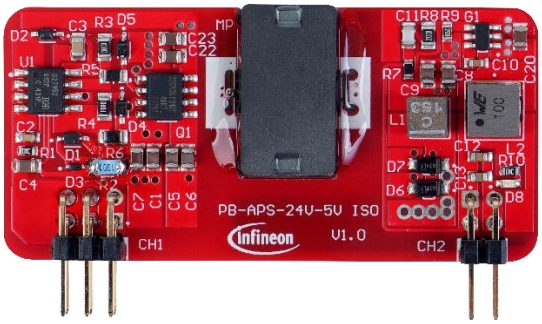


Figure 5 **24V-5V Isolated Auxiliary Power Supply Card**

1.4 Preferred components

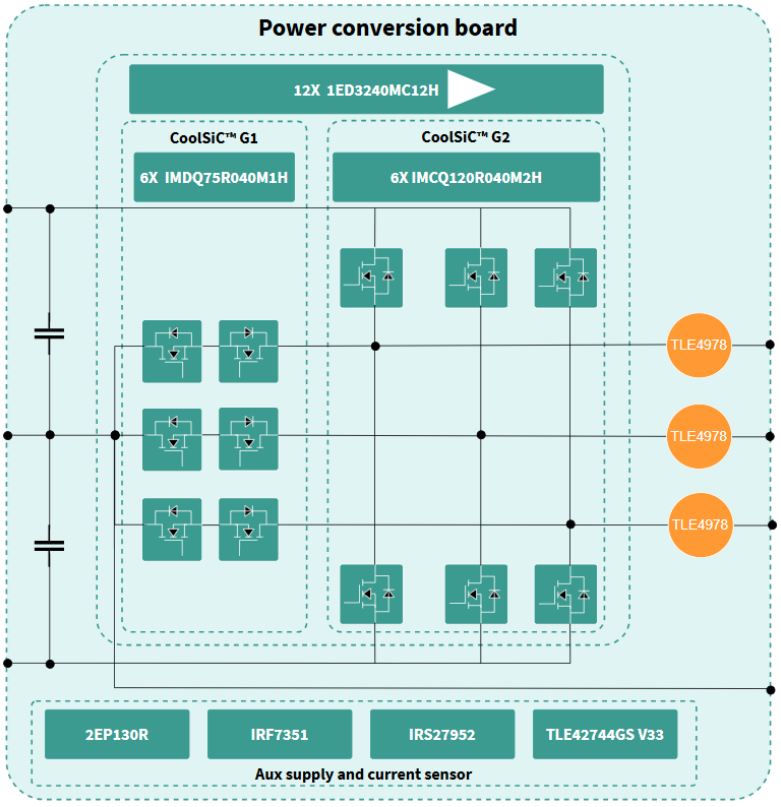


Figure 6 **Key Infineon components in 10kW NPC2 Power Conversion Board**

Note: Figure 6 shows the main Infineon products offered in the 10 kW NPC2 inverter reference design.

- Power semiconductors:
  - 1200 V CoolSiC MOSFET in Q-DPAK: IMCQ120R040M2H
  - 750 V CoolSiC MOSFET in Q-DPAK: IMDQ75R040M1H
- Gate driver:
  - Single channel isolated gate driver with 2-level slew rate control: 1ED3240MC12H

- Current sensor:
    - XENSIV™ magnetic current sensor: TLE4978-R050W5-O-S0010
- Auxiliary power supply:
    - 2EP130R: Full-bridge transformer driver
    - IRS27952: Half-bridge controller IC
    - IRF7351: 60 V dual N-channel HEXFET power MOSFET

2 Functional description of the board

This chapter lists the features available for the 10 kW NPC2 inverter reference design.

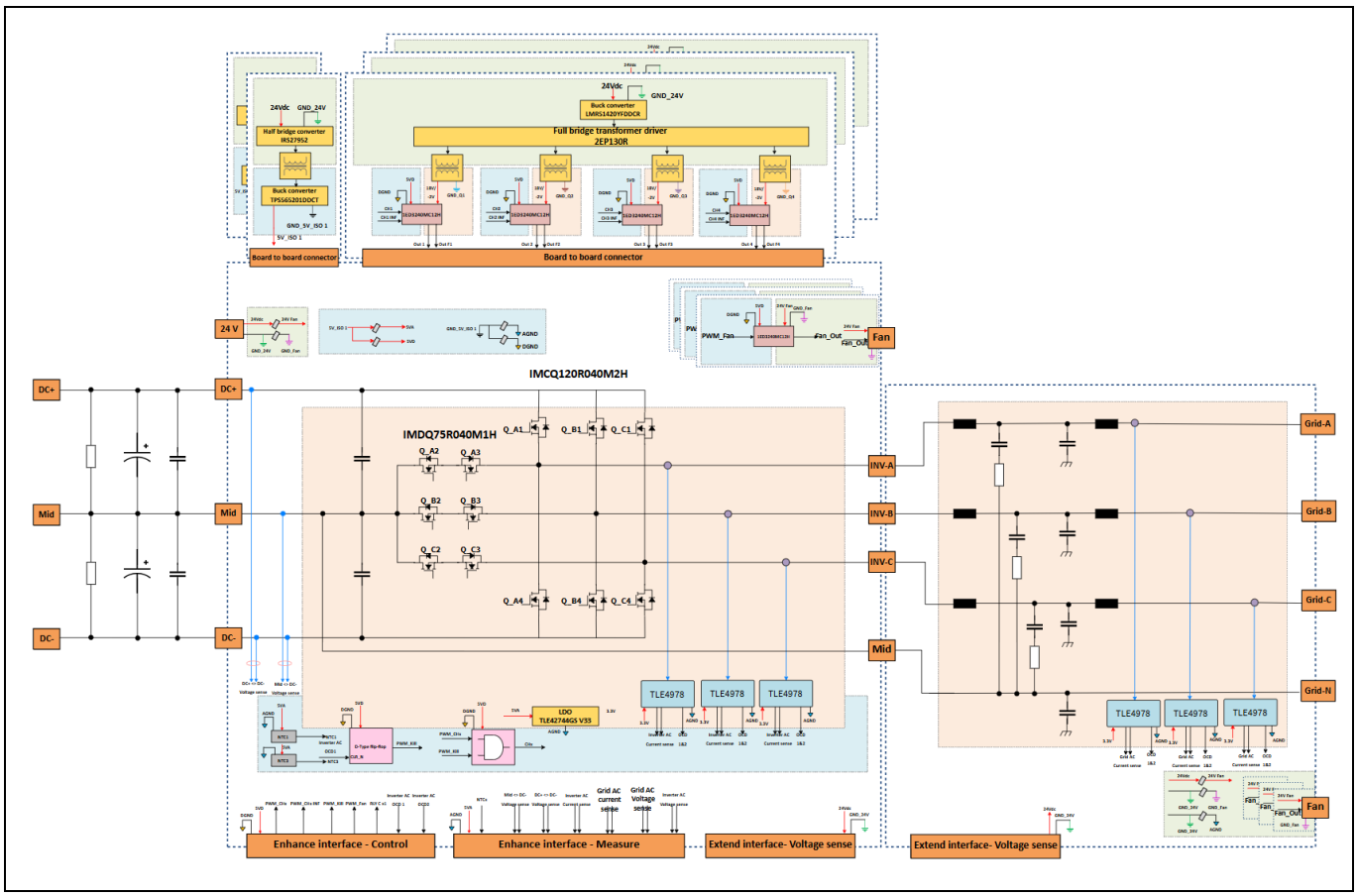


Figure 7 **Block diagram of REF-10KW3LNPC2Q**

2.1 Description of the functional blocks

2.1.1 Switching devices

The inverter stage is realized using the CoolSiC™ MOSFET in the Q-DPAK products IMCQ120R040M2H and IMDQ75R040M1H.

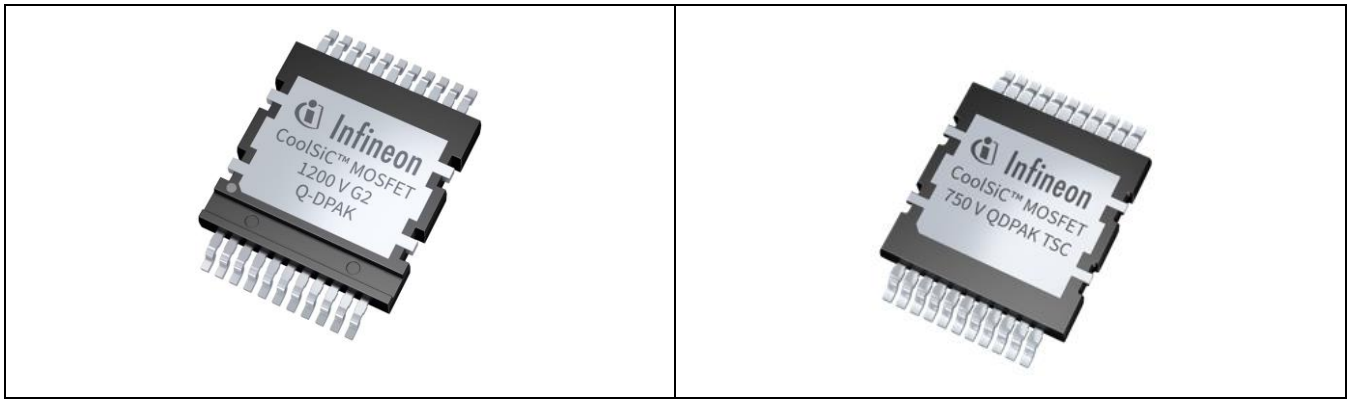


Figure 8 **IMCQ120R040M2H and IMDQ75R040M1H**

IMCQ120R040M2H belongs to the CoolSiC™ G2 family and IMDQ75R040M1H belongs to the CoolSiC™ G1 family.

They come in the innovative top-side cooled Q-DPAK package that is specifically designed for a wide use in industrial applications. Top-side cooled (TSC) Q-DPAK power packages are a promising solution to improve thermal and electrical performance. These packages also help increase power density and reduce manufacturing effort.

2.1.2 Gate driver

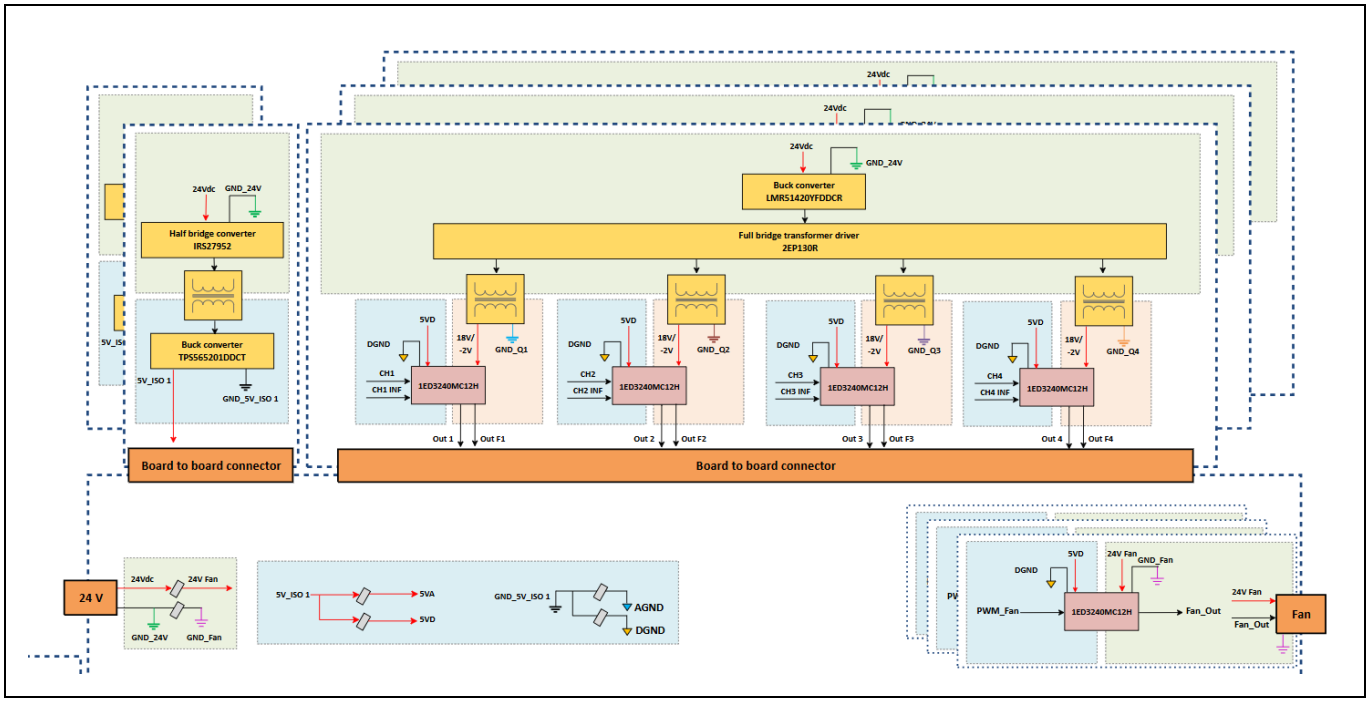


Figure 9 **Functional block diagram of the gate driver card**

The gate driver board contains a three-phase drive, and four output channels per phase for each leg of the NPC2 type. The gate driver used on this board is 1ED3240MC12H.

Figure 10 **1ED3240MC12H**

1ED3240MC12H belongs to the EiceDRIVER™ 2L-SRC Compact 1ED32xx family and is a single-channel, isolated gate driver with a two-level slew-rate control (2L-SRC). It features a typical 10 A sinking and sourcing peak output current in a DSO-8 wide-body package with a large creepage distance (> 8 mm) for IGBTs, MOSFETs, and SiC MOSFETs. Two separate outputs help in controlling two independent gate resistances for both turn-on and turn-off, thus enabling the two-level slew-rate control. The driver can operate over a wide range of supply voltage, both unipolar and bipolar.

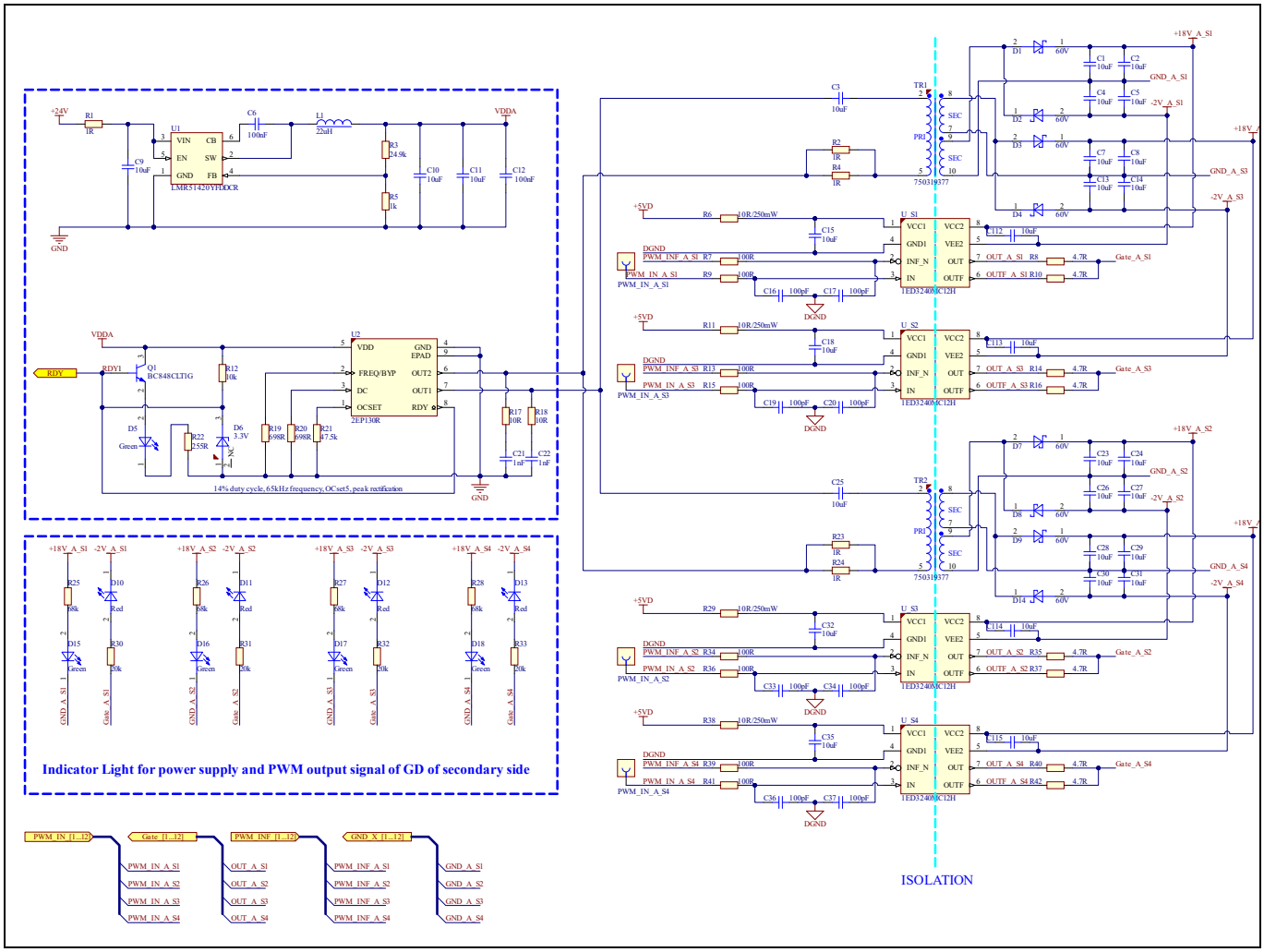


Figure 11 **Gate driver card schematic for one phase (A, B, and C phases are all the same)**

The 24 V voltage and PWM signals come from the power board and are used as an input to the gate driver board. The 24 V is then stepped down and used as an input to the 2EP130R full-bridge transformer driver. A transformer is then used to provide functional isolation. 18 V and -2 V voltages are generated on the rectifier side to be used as the positive and negative voltage for driving the SiC MOSFETs on the power board. The gate resistors are located on the power board.

2.1.3 Internal power supplies

Users must provide an external 24 V voltage to the power board, and the gate driver card is powered by the power board. The 24V voltage is fed to a power supply card that generates an isolated voltage of 5 V. The isolated 5 V is fed to the primary side of the gate driver. The 24 V is fed to the gate driver card that generates the isolated 18 V/-2 V needed to drive the SiC MOSFETs.

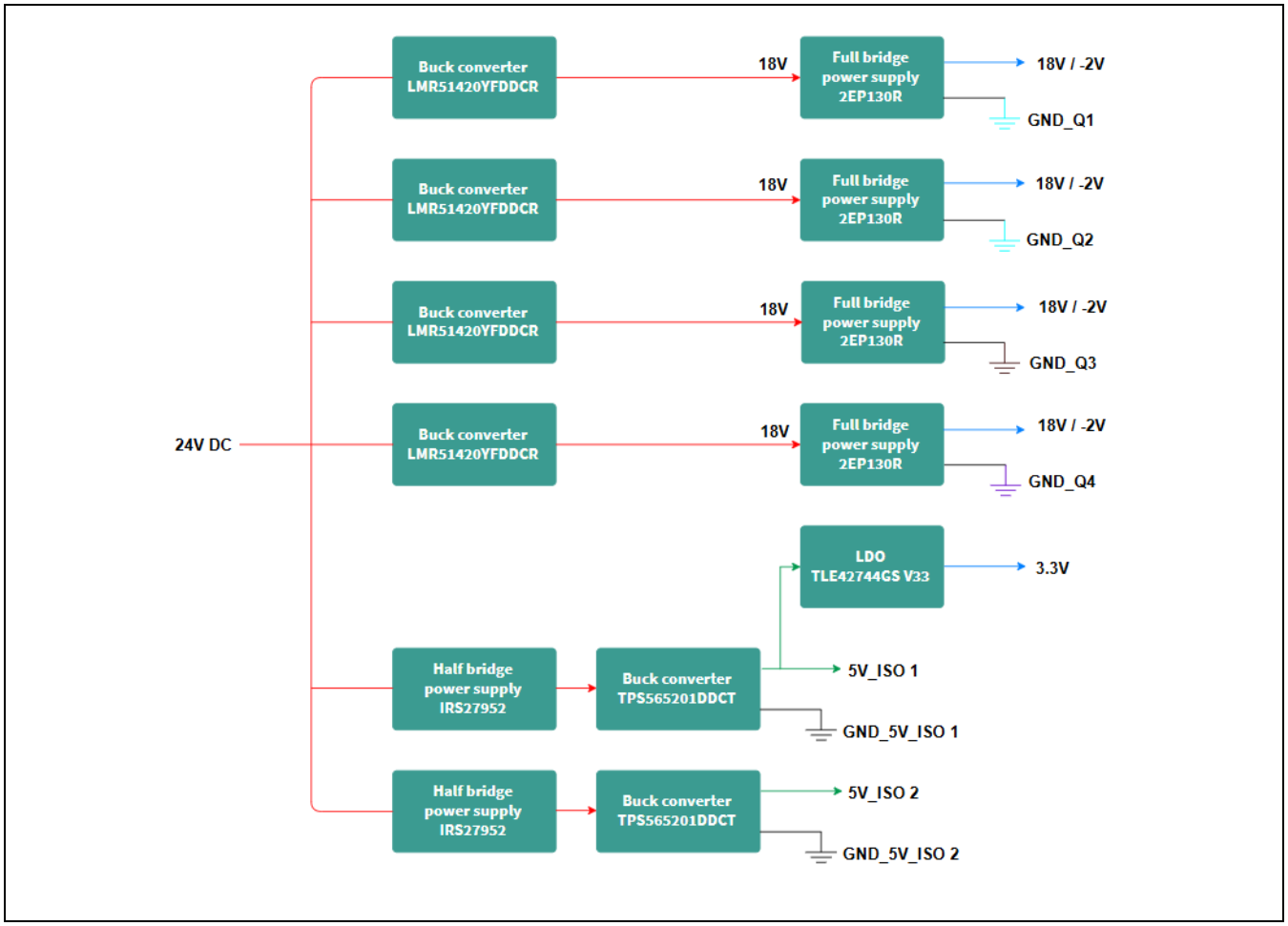


Figure 12 **Auxiliary power supply tree**

Table 3 Specifications of the power supply card

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	21.6	24	26.4	V_{dc}
Input current		0.5		A
Output voltage	4.75	5	5.25	V_{dc}
Output current			2	A
Switching frequency		226		kHz
Half-bridge IC used	IRS27952			-

The specifications of the power supply card are listed in Table 3.

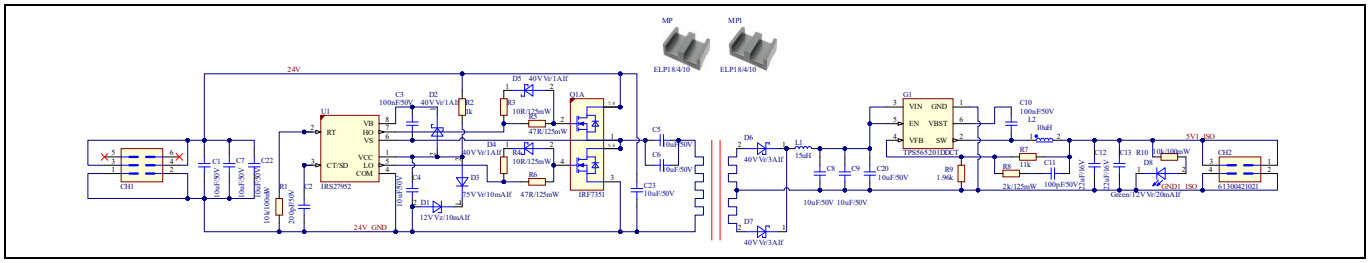


Figure 13 **Schematics of the power supply card**

2.1.4 Sensing and protection

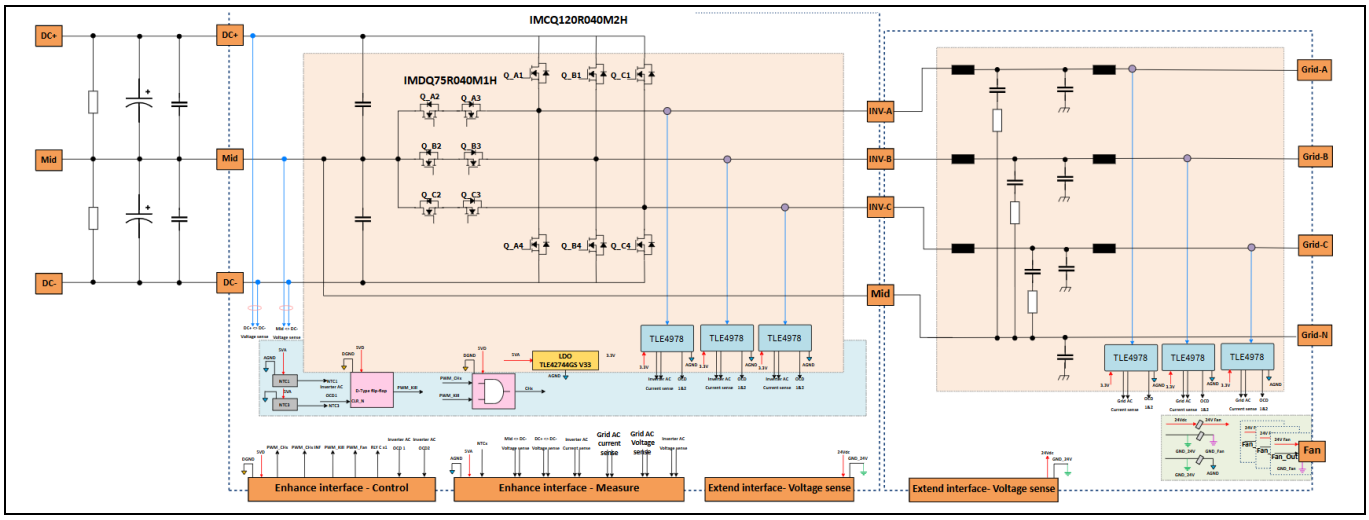


Figure 14 **Functional block diagram of the measurement signals on the power board**

As shown in Figure 14, this is a functional block diagram of the sampling and protection section, which includes current sense, voltage sense, temperature sense, and connectors.

2.1.4.1 Current sense

The inductor currents are measured using the TLE4978-R050W5-O-S0010 current sensor.

TLE4978-R050W5-O-S0010 is a new highly accurate, high-bandwidth coreless current sensor IC from Infineon. It is based on the Hall effect and coil-current sensing with user-configurable overcurrent detection (OCD) and zero crossing detection (ZCD) features. Infineon's well established and robust magnetic sensing technology enables accurate and highly linear measurement of currents with full-scale current of up to ±50 A.

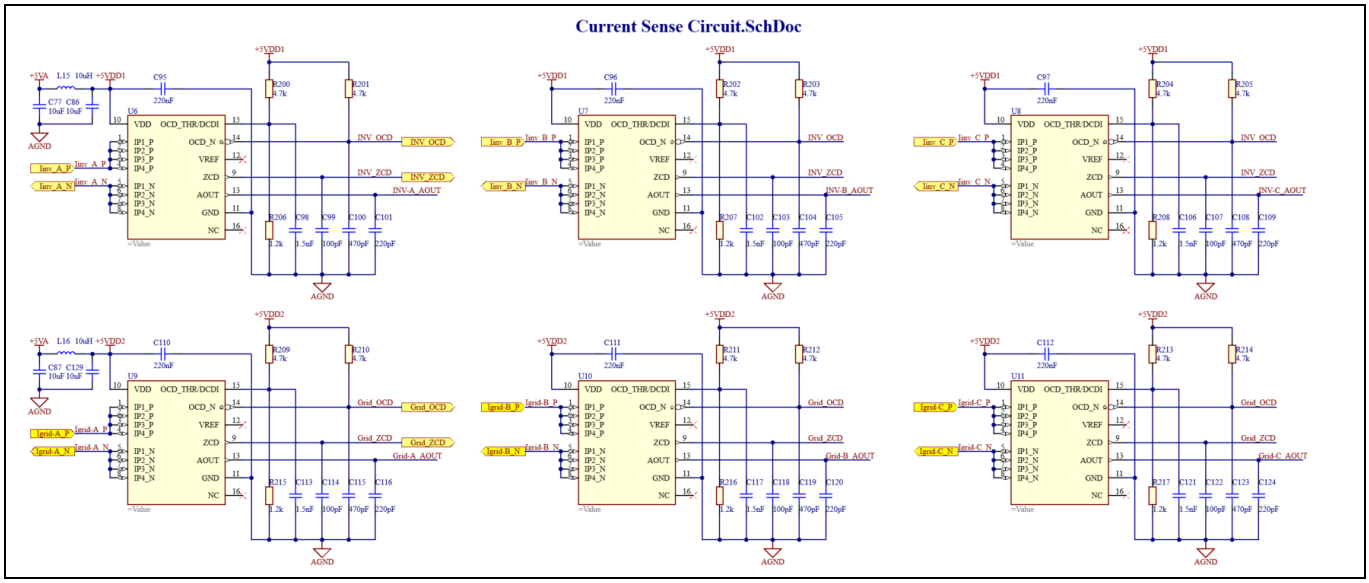


Figure 15 **Current sense circuit**

2.1.4.2 Voltage sense

The DC-link voltages are measured on the power board.

WARNING: The controller board must be connected to the main power board before the power board is switched on. Failure to do so can lead to a hazardous situation.

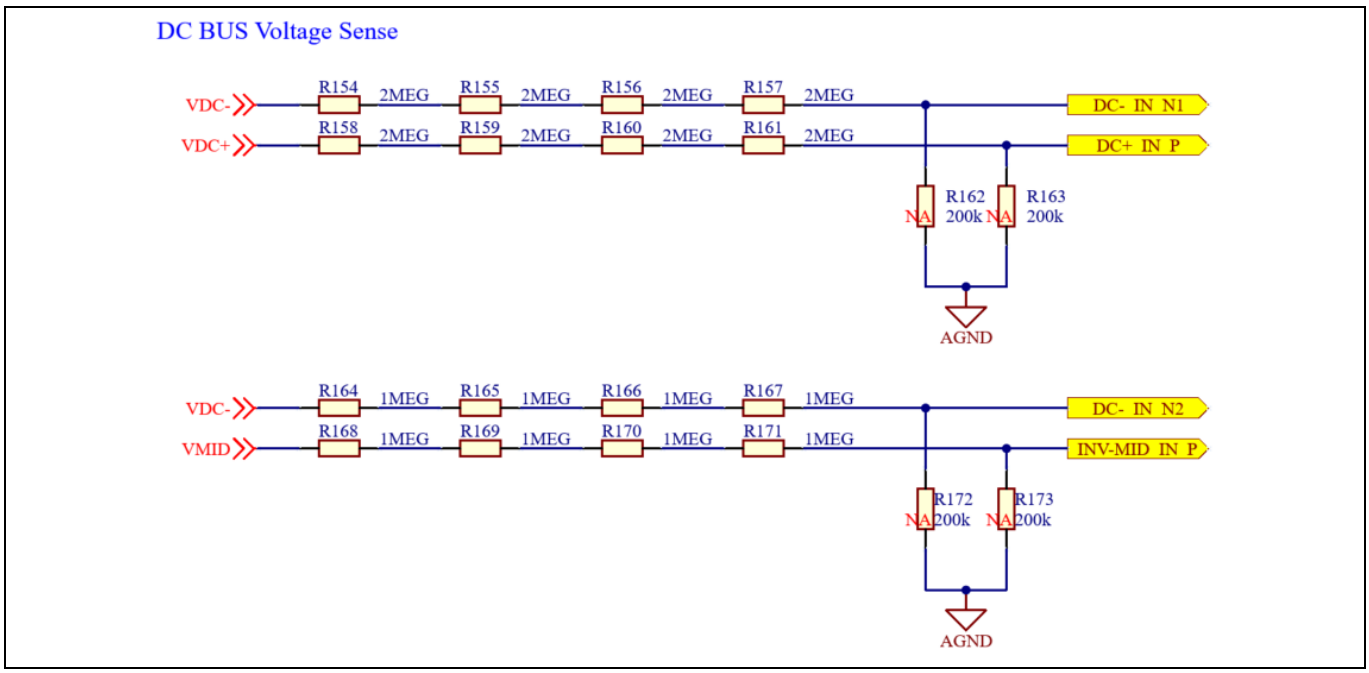


Figure 16 **DC-bus voltage sense**

2.1.4.3 Temperature sense

Three temperature measurements are provided on the power board using NTCs. The NTCs can be connected to the heat sink to measure the temperature and feed it back to the connector that is connected to a control board.

Two NTC thermistors are used for temperature monitoring: NTC3 measures the temperature of the heatsink, while NTC1 monitors the ambient temperature. If the ambient temperature rises above the predefined threshold, forced cooling and power derating will be activated. Additionally, the system will shut down if the heatsink temperature reaches 100°C.

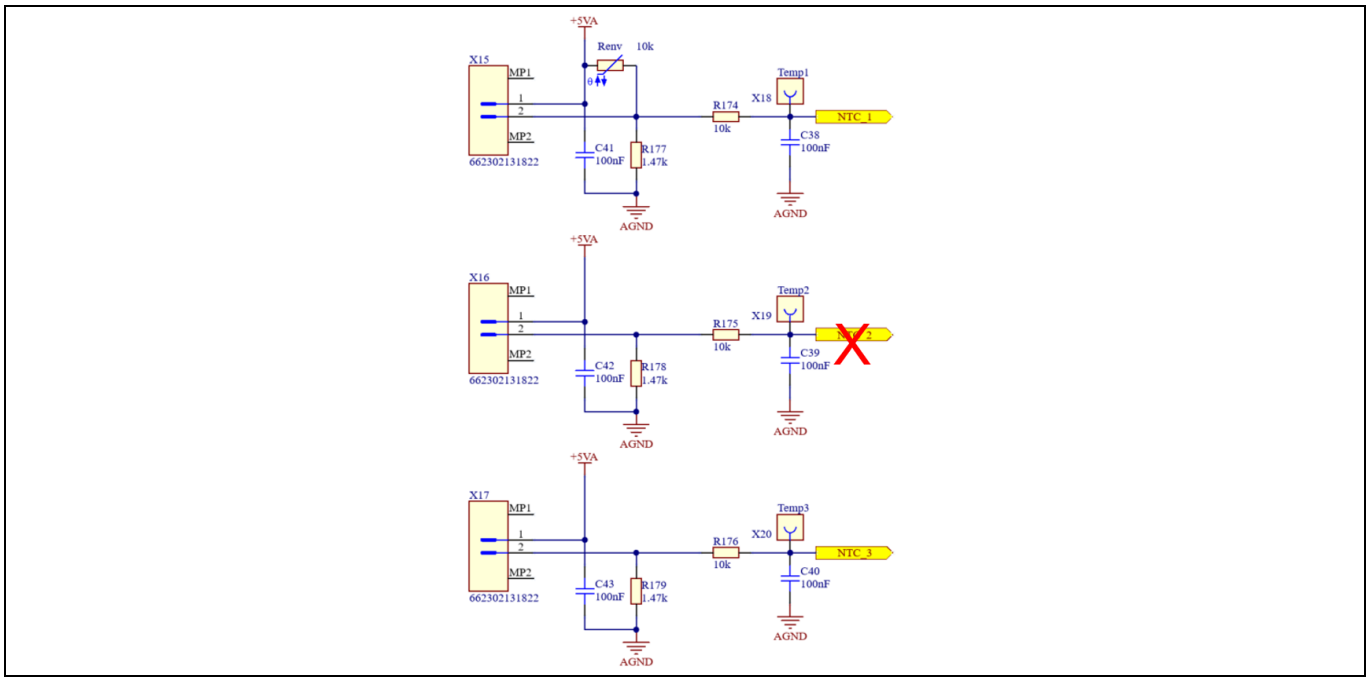


Figure 17 **Temperature sensing circuit**

2.1.4.4 Fault and latch circuit

Fault and latch circuits are provided to disable the PWMs in the case of a fault event. Figure 70 shows the fault and latch circuit.

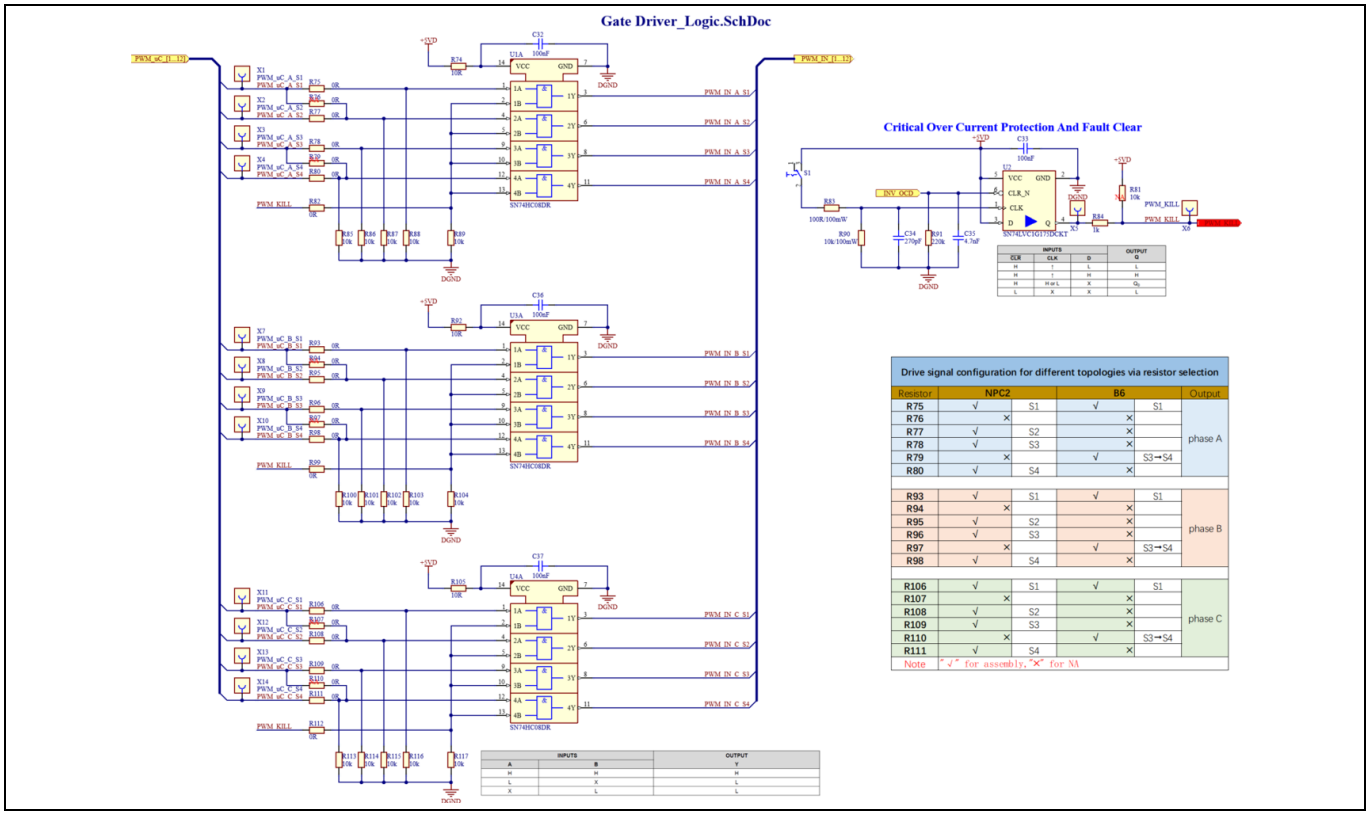


Figure 18 **Fault and latch circuit**

2.1.5 Fan control schematic

Additional fan control circuits are provided in case forced air cooling is required during evaluation.

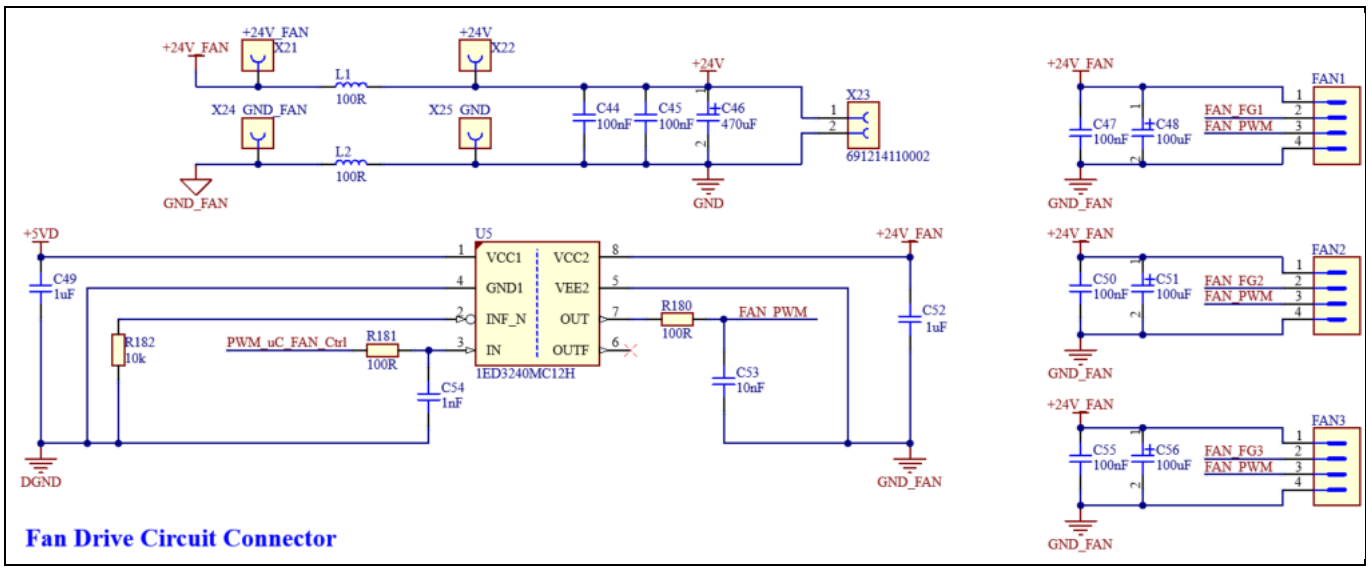


Figure 19 **Fan control circuits**

2.1.6 Connectors

2.1.6.1 Enhanced interface_control

Connector X44 contains all the signals related to the PWMs, faults, and relay control.

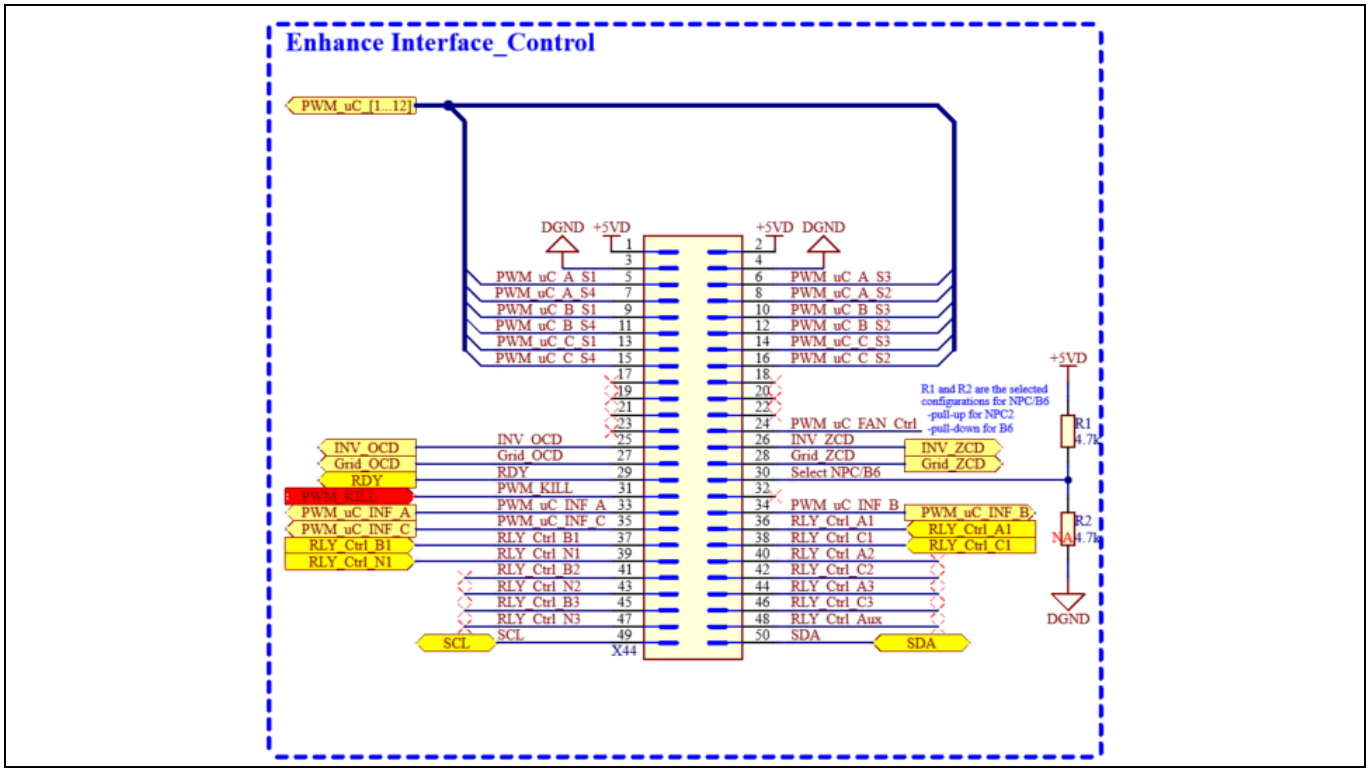


Figure 20 **Enhanced interface_control**

Table 4 Extended interface-voltage sense

Basic interface		
Pin	**Signal**	**Description**
1	+5VD	Digital power
2	+5VD	Digital power
3	DGND	Digital power
4	DGND	Digital power
5	PWM_uC_A_S1	Phase A T1 PWM
6	PWM_uC_A_S3	Phase A T3 PWM
7	PWM_uC_A_S4	Phase A T4 PWM
8	PWM_uC_A_S2	Phase A T2 PWM
9	PWM_uC_B_S1	Phase B T1 PWM
10	PWM_uC_B_S3	Phase B T3 PWM
11	PWM_uC_B_S4	Phase B T4 PWM
12	PWM_uC_B_S2	Phase B T2 PWM
13	PWM_uC_C_S1	Phase C T1 PWM
14	PWM_uC_C_S3	Phase C T3 PWM
15	PWM_uC_C_S4	Phase C T4 PWM
16	PWM_uC_C_S2	Phase C T2 PWM
17	NC	NC
18	NC	NC

19	NC	NC
20	NC	NC
21	NC	NC
22	NC	NC
23	NC	NC
24	PWM_uC_FAN_CTRL	NPC2 FAN control
25	INV_OCD	Inverter side Over Current Protection
27	Grid_OCD	Grid-side Over Current Protection
30	Select NPC/B6	Selection of a different topology
31	PWM_KILL	PWM kill
32	NC	NC
33	PWM_uC_INF_A	Phase A gate driver control
34	PWM_uC_INF_B	Phase B gate driver control
35	PWM_uC_INF_C	Phase C gate driver control
36	RLY_Ctrl_A1	Grid phase A relay control
37	RLY_Ctrl_B1	Grid phase B relay control
38	RLY_Ctrl_C1	Grid phase C relay control
39	RLY_Ctrl_N1	Grid phase N relay control
40	RLY_Ctrl_A2	Bypass phase A relay control
41	RLY_Ctrl_B2	Bypass phase B relay control
42	RLY_Ctrl_C2	Bypass phase C relay control
43	RLY_Ctrl_N2	Bypass phase N relay control
44	RLY_Ctrl_A3	Inverter phase A relay control
45	RLY_Ctrl_B3	Inverter phase B relay control
46	RLY_Ctrl_C3	Inverter phase C relay control
47	RLY_Ctrl_N3	Inverter phase N relay control
48	RLY_Ctrl_AUX	Pre-charge relay control
49	SCL	Gate driver config (if required)
50	SDA	Gate driver config (if required)

2.1.6.2 Enhanced Interface_measure

All the measurement signals are fed to the control board using the X53 connector located on the power board.

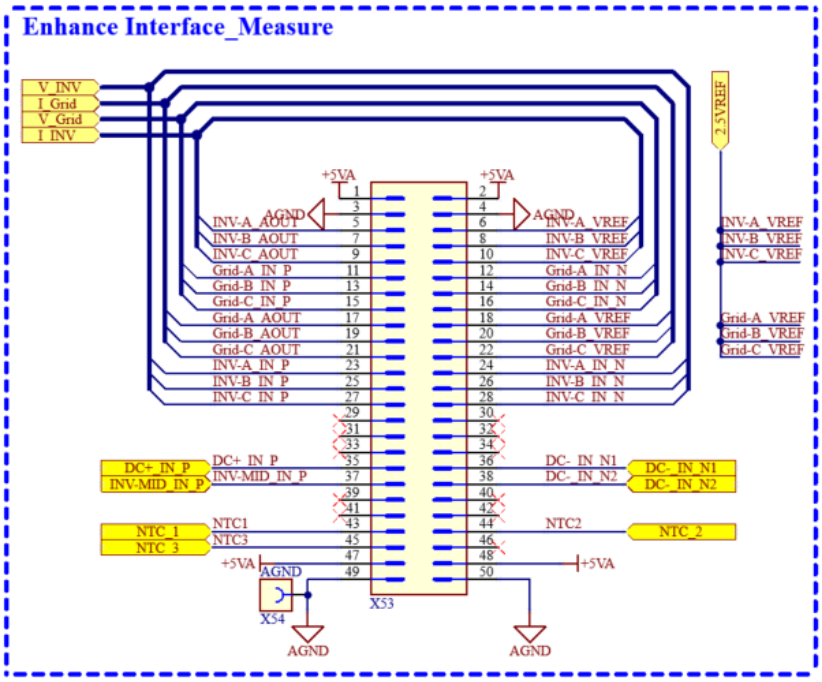


Figure 21 **Enhanced Interface_measure**

Table 5 Enhanced interface_measure

Basic interface		
Pin	**Signal**	**Description**
1	+5 VA	Analog power
2	+5 VA	Analog power
3	AGND	Analog power
4	AGND	Analog power
5	INV-A_AOUT	Inverter phase A current P
6	Grid-A_VREF	Grid phase A current N
7	INV-B_AOUT	Inverter phase B current P
8	Grid-A_VREF	Grid phase A current N
9	INV-C_AOUT	Inverter phase C current P
10	Grid-A_VREF	Grid phase A current N
11	Grid-A_IN_P	Grid phase A voltage P
12	Grid-A_IN_N	Grid phase A voltage N
13	Grid-B_IN_P	Grid phase B voltage P
14	Grid-B_IN_N	Grid phase B voltage N
15	Grid-C_IN_P	Grid phase C voltage P
16	Grid-C_IN_N	Grid phase C voltage N
17	Grid-A_AOUT	Grid phase A current P
18	Grid-A_VREF	Grid phase A current N
19	Grid-B _AOUT	Grid phase B current P

20	Grid-A_VREF	Grid phase A current N
21	Grid-C_AOUT	Grid phase C current P
22	Grid-A_VREF	Grid phase A current N
23	INV-A_IN_P	Inverter phase A voltage P
24	INV-A_IN_N	Inverter phase A voltage N
25	INV-B_IN_P	Inverter phase B voltage P
26	INV-B_IN_N	Inverter phase B voltage N
27	INV-C_IN_P	Inverter phase C voltage P
28	INV-C_IN_N	Inverter phase C voltage N
29	NC	NC
30	NC	NC
31	NC	NC
32	NC	NC
33	NC	NC
34	NC	NC
35	DC+_IN_P	Bus+ voltage P
36	DC-_IN_N1	Bus+ voltage N
37	INV-MID_IN_P	Bus- voltage P
38	DC-_IN_N2	Bus- voltage N
39	NC	NC
40	NC	NC
41	NC	NC
42	NC	NC
43	NTC1	NTC1
44	NTC2	NTC2
45	NTC3	NTC3
46	NC	NC
47	+5 VA	Analog power
48	+5 VA	Analog power
49	AGND	Analog power
50	AGND	Analog power

3 Converter control design

3.1 Converter topology and its switching strategy

3.1.1 Introduction to the NPC2 inverter

REF-10KW3LNPC2Q consists of three legs connected in parallel, each arm containing two SiC MOSFETs, and two clamping diodes. A key feature is the neutral point (NP) – a central node between the DC-link capacitors that serves as a reference voltage for clamping. The circuit diagram for the NPC2 inverter is shown in Figure 22. Parasitic circuits of the inductor and capacitor have been ignored, and the switch and diode have been assumed to be the ideal devices for further mathematical analysis.

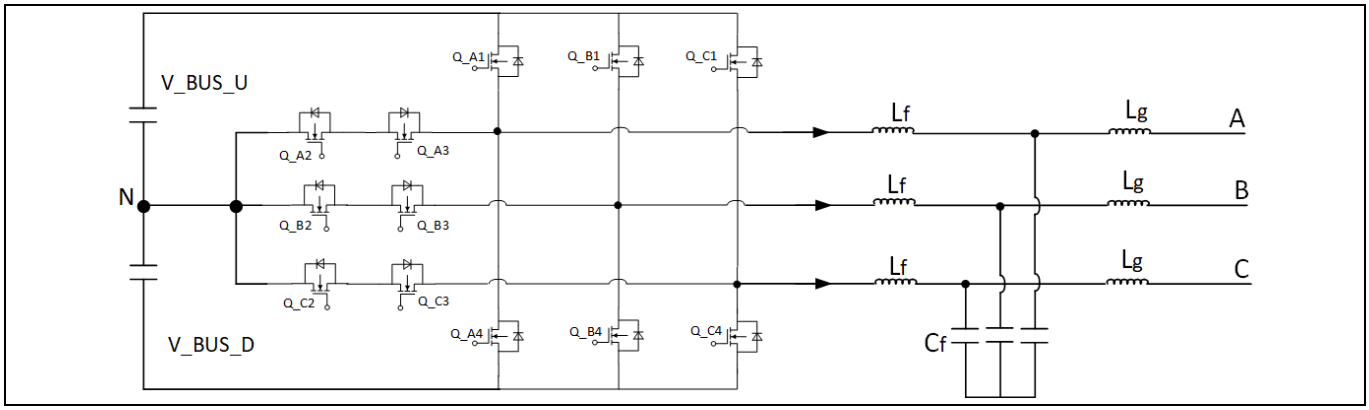


Figure 22 **Circuit diagram of an NPC2 inverter**

3.1.2 NPC2 switching strategy

For an NPC2 three-level topology, the entire sinusoidal period can be divided into positive and negative AC cycles. In the positive AC cycle, the Q1 switch works complementarily with the Q3 switch in each switching cycle. The Q2 switch is always ON and the Q4 is always OFF.

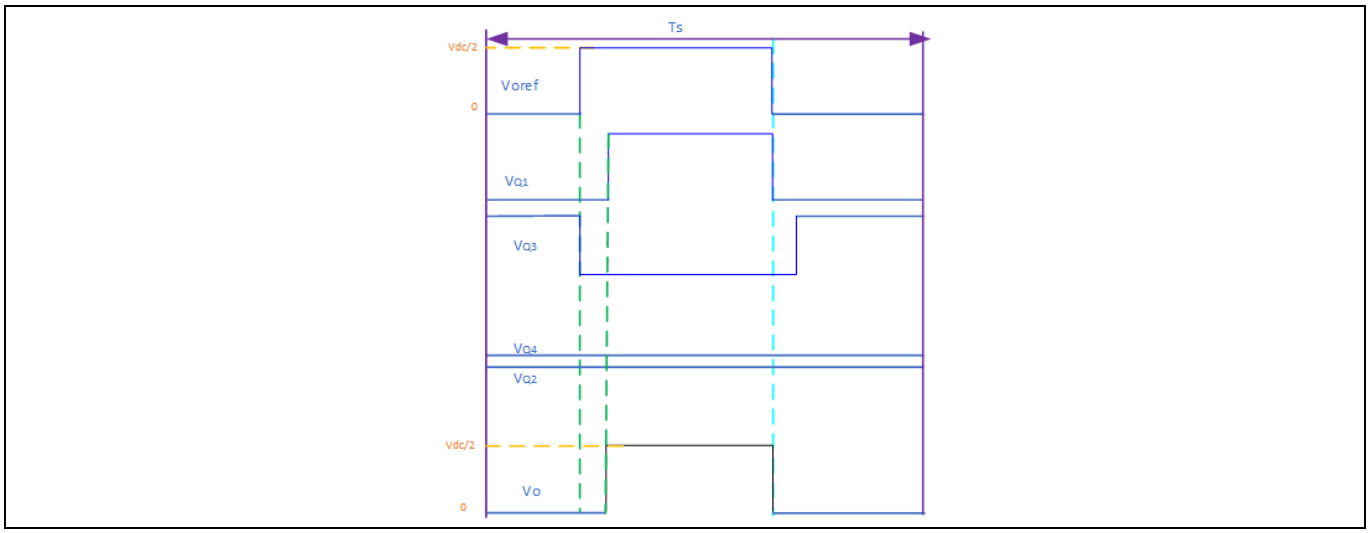


Figure 23 **The positive cycle**

The current flow in the positive AC cycle is shown in Figure 24.

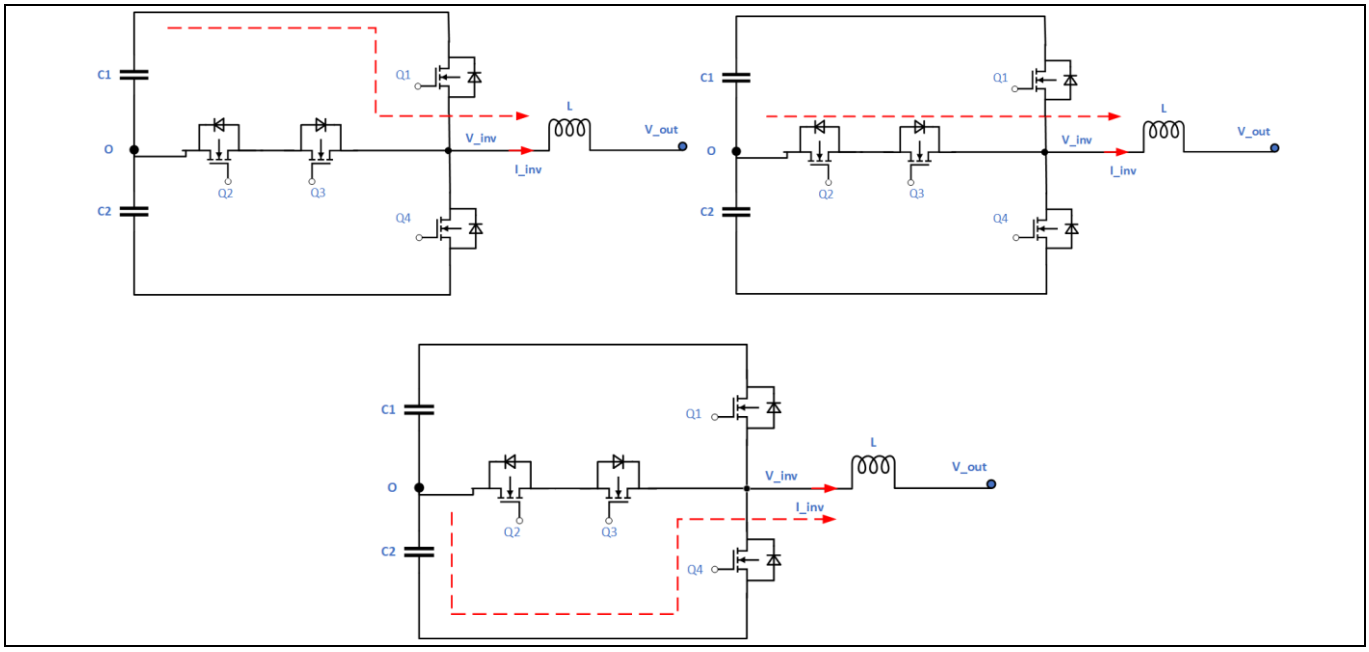


Figure 24 **Current flow in the positive AC cycle**

In the negative AC cycle, the Q4 switch works complementarily with Q2 in each switching cycle. The Q3 switch is always ON and Q1 is always OFF.

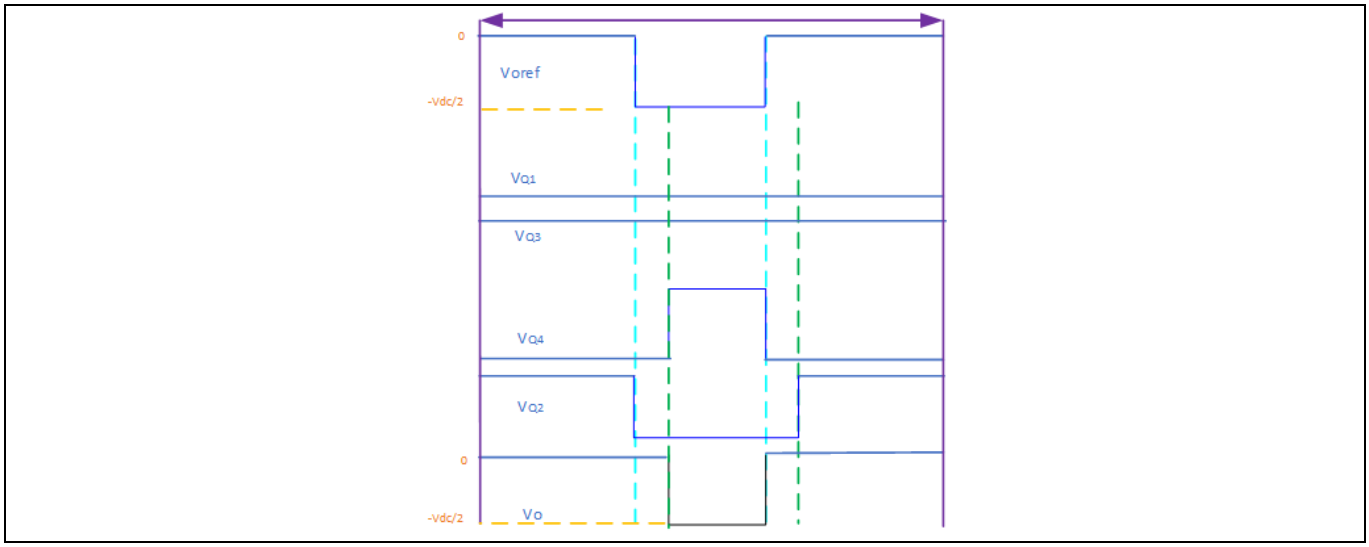


Figure 25 **The negative cycle**

The current flow in a negative AC cycle is shown in Figure 26.

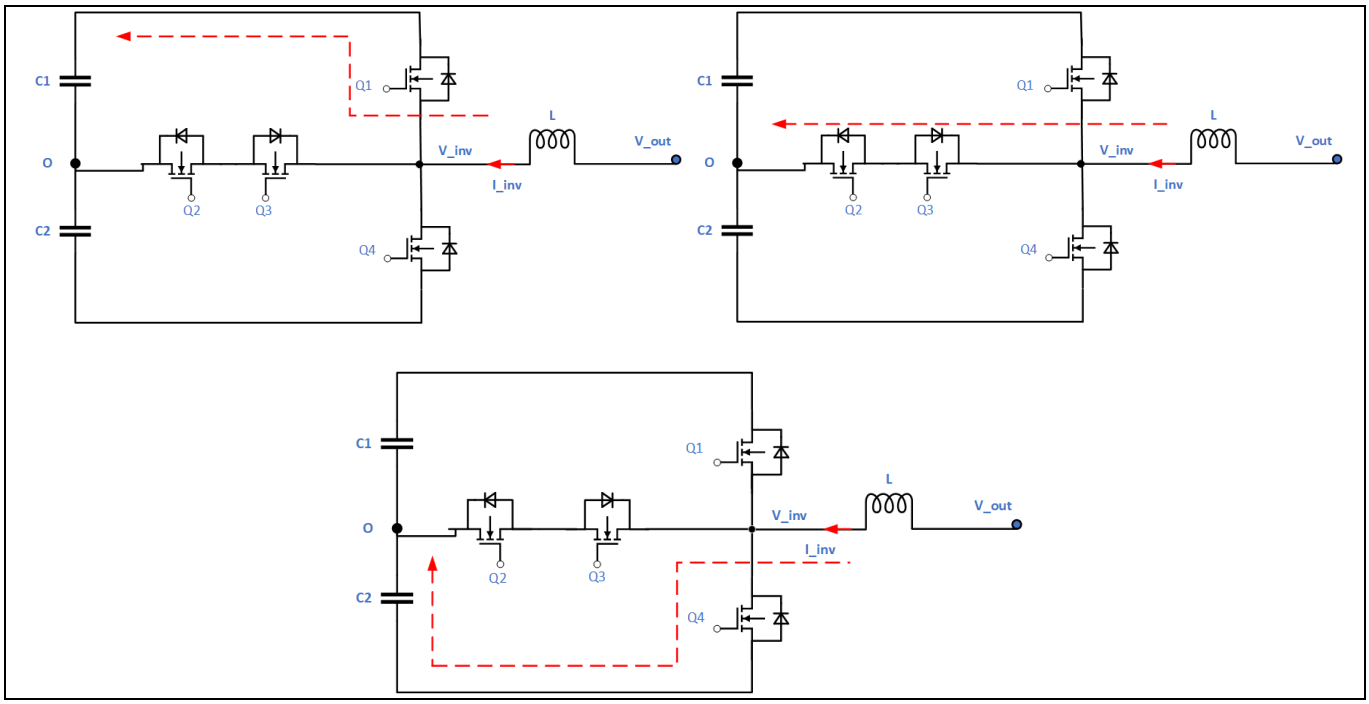


Figure 26 **Current flow in the negative AC cycle**

Figure 27 shows how the pulse-width modulation (PWM) signals look like when deriving the switching sequences described in the previous section. Sinusoidal PWM is used. Uref (orange) is the PWM reference signal for generating the switching sequence for Q1 to Q4. Uref13 (green) is the PWM reference signal for generating the switching sequence for Q1 to Q3 during the positive AC cycle. Uref42 (red) is the PWM reference signal for generating the switching sequence for Q4 to Q2 during the negative AC cycle.

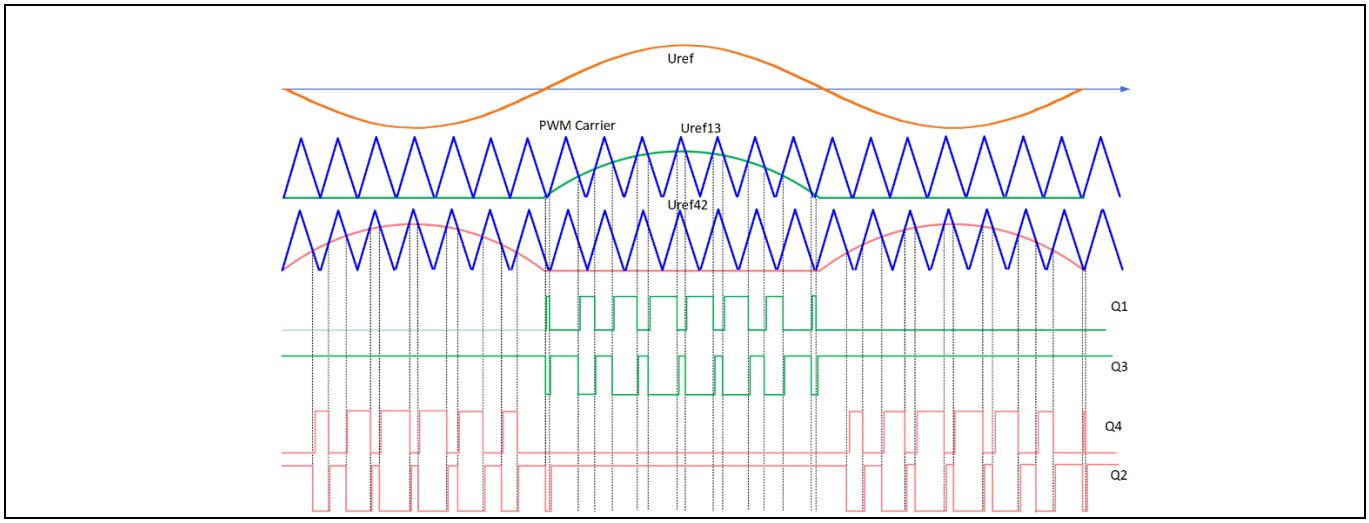


Figure 27 **Switching sequence**

3.2 Control mode and control loop design

3.2.1 Introduction to the control mode

Figure 28 demonstrates the basic control diagram of an NPC2 inverter. It consists of outer loop control, current control loop (based on dq axis), and neutral voltage control. The outer loop control supports both V/F control mode and P/Q control mode, the V/F control mode which operates under grid off condition, and the P/Q control mode operates under grid-tied condition. The outer loop control will choose the corresponding control loop accroding to the control mode setting on GUI. These control blocks allocate resources in different tasks based on priorities.

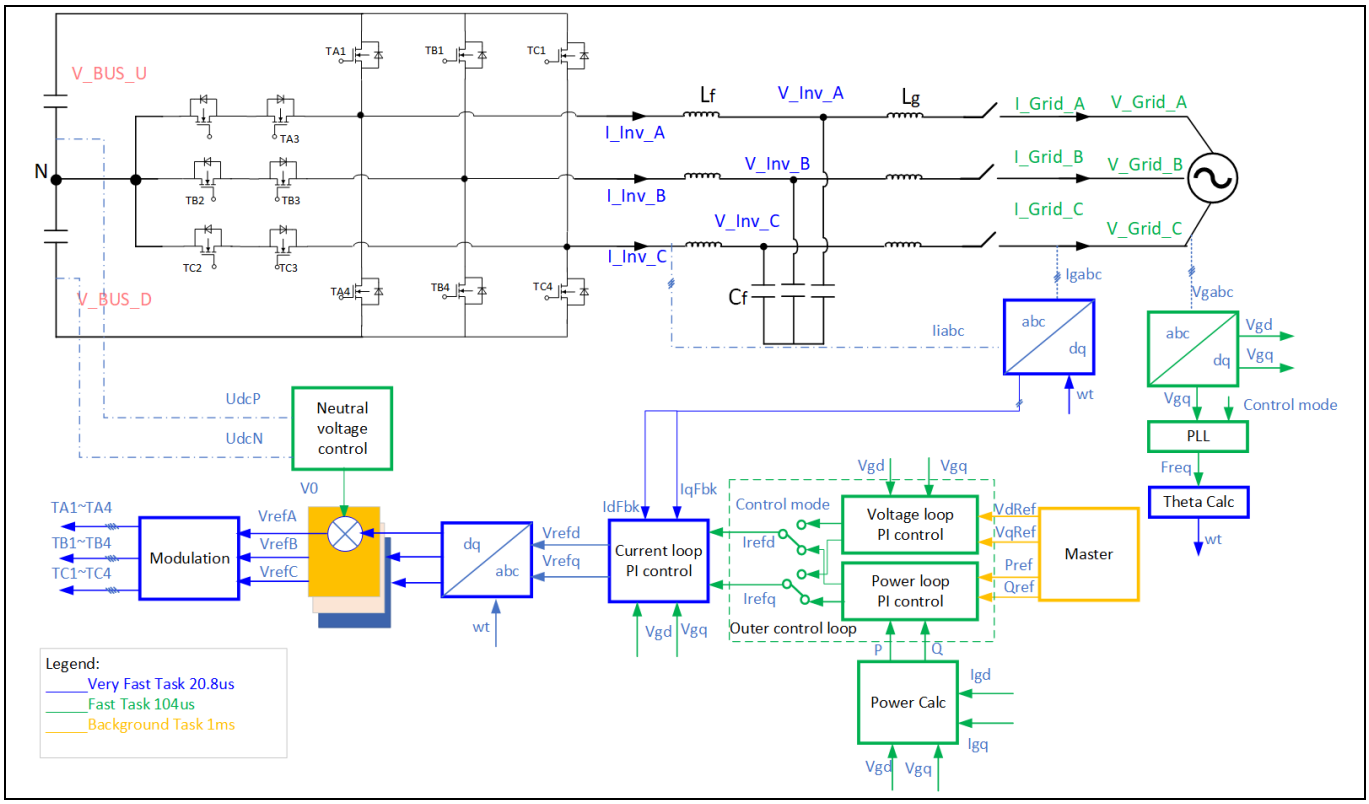


Figure 28 **REF-10KW3LNPC2Q application overview**

Figure 29 shows the features and specification of the application.

Features		Specifications	
Open loop ctrl	SPWM	**Pout**	10 kW(12kW max)
P/Q ctrl	Minimum pulse limit	**Vin**	650~ 950 Vdc
V/F Ctrl	DC balance ctrl	**SW frequency**	48 kHz
protection	UART communication	**Vout**	400 VL-L / 50 Hz

Figure 29 **Features and specifications of REF-10KW3LNPC2Q**

The open loop control of this three-level NPC2 inverter is based on the SPWM scheme. Users can adjust the V_{out} by changing the modulation index. An appropriate DC voltage should be set to avoid overmodulation. In an

NPC2 inverter topology, the DC balance control is a non-negotiable feature that ensures a stable DC-link operation and balanced output voltages. Meanwhile, the application uses UART communication to realize the protection. A detailed explanation of the algorithm of every inverter control loop is provided in the next section.

3.2.2 Control loop and algorithm

3.2.2.1 Three-phase inverter mathematical model

Figure 30 shows a three-phase three-level inverter circuit model.

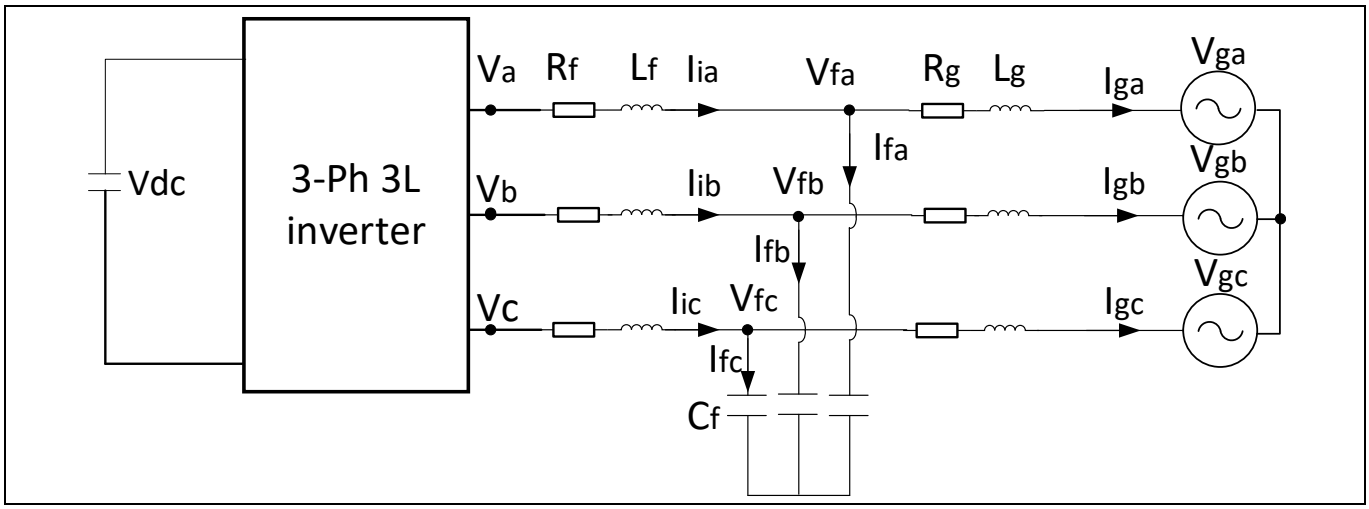


Figure 30 **The NPC2 inverter circuit model**

The mathematical model of the inverter can be obtained according to both Kirchoff's voltage law (KVL) and Kirchoff's current law (KCL) laws at the same time. This is because L_g has little impact on the capacitor's voltage and only the value of LC filter value is considered in the mathematical model:

$$\begin{cases} \frac{dV_{fk}}{dt} = -\frac{1}{C_f} I_{gk} + \frac{1}{C_f} I_{ik} \\ \frac{dI_{ik}}{dt} = -\frac{R_f}{L_f} I_{ik} - \frac{1}{L_f} V_{fk} + \frac{1}{L_f} V_k \end{cases} \quad k = a, b \tag{1}$$

We can get the mathematical model of the node near the grid side, same according to KVL and KCL law:

$$\begin{cases} \frac{dV_{fk}}{dt} = -\frac{1}{C_f} I_{gk} + \frac{1}{C_f} I_{ik} \\ \frac{dI_{gk}}{dt} = -\frac{R_g}{L_g} I_{gk} - \frac{1}{L_g} V_{gk} + \frac{1}{L_g} V_{fk} \end{cases} \quad k = a, b, c \tag{2}$$

It is convenient to design a controller based on the dq rotating reference frame at grid frequency speed, with the d axis aligned to the grid voltage vector.

The mathematical model of the inverter based on dq rotating reference frame and Laplace transform is as follows:

$$\begin{bmatrix} sV_{fd} \\ sV_{fq} \end{bmatrix} = \begin{bmatrix} 0 & \omega_0 \\ -\omega_0 & 0 \end{bmatrix} \begin{bmatrix} V_{fd} \\ V_{fq} \end{bmatrix} - \frac{1}{C_f} \begin{bmatrix} I_{gd} \\ I_{gq} \end{bmatrix} + \frac{1}{C_f} \begin{bmatrix} I_{id} \\ I_{iq} \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} sI_{id} \\ sI_{iq} \end{bmatrix} = \begin{bmatrix} 0 & \omega_0 \\ -\omega_0 & 0 \end{bmatrix} \begin{bmatrix} I_{id} \\ I_{iq} \end{bmatrix} - \frac{1}{L_f} \begin{bmatrix} V_{fd} \\ V_{fq} \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} V_d \\ V_q \end{bmatrix} - \frac{R_f}{L_f} \begin{bmatrix} I_{id} \\ I_{iq} \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} sI_{gd} \\ sI_{gq} \end{bmatrix} = \begin{bmatrix} 0 & \omega_0 \\ -\omega_0 & 0 \end{bmatrix} \begin{bmatrix} I_{gd} \\ I_{gq} \end{bmatrix} - \frac{1}{L_g} \begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix} + \frac{1}{L_g} \begin{bmatrix} V_{fd} \\ V_{fq} \end{bmatrix} - \frac{R_g}{L_g} \begin{bmatrix} I_{gd} \\ I_{gq} \end{bmatrix} \quad (5)$$

Figure 31 shows a graphical representation of this mathematical model.

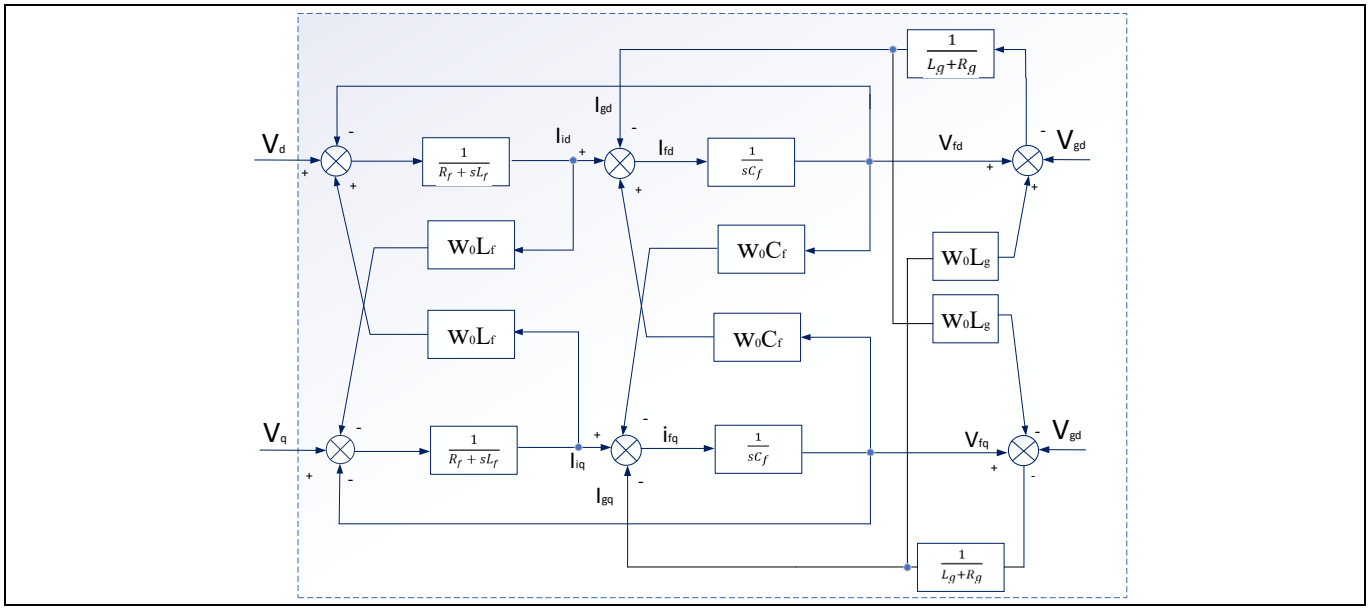


Figure 31 **Graphical representation of the mathematical model**

3.2.2.2 Current loop design

Figure 32 shows the current loop control diagram. Two feedforward elements have been added to remove additional sources of disturbances and errors in the model. This control diagram is suitable for both grid-off and grid-tied control mode.

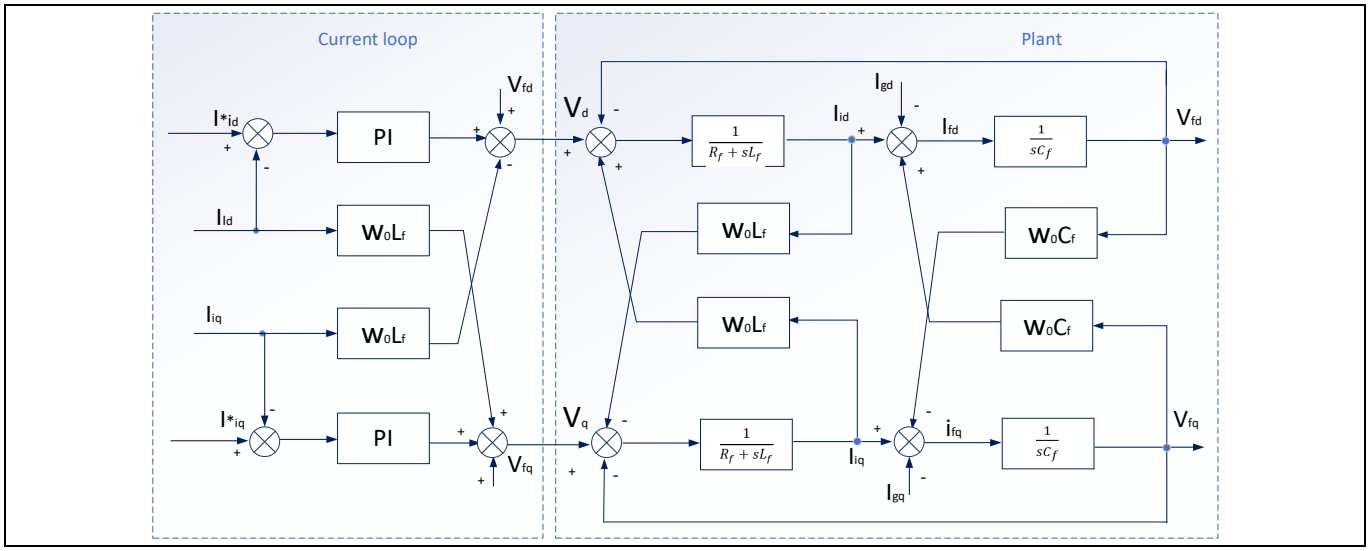


Figure 32 **Current loop control diagram**

To get better performance, the current controller can be designed into a type 1 system. Figure 33 shows its typical structure.

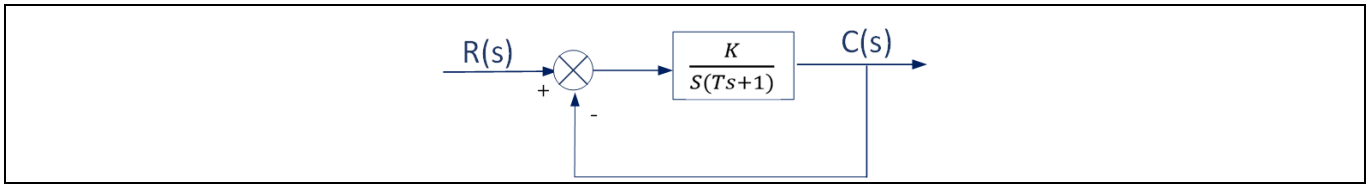


Figure 33 **A typical type 1 system**

The d axis should be picked to design the current controller. Figure 34 shows the entire control diagram, and it is the same for the q axis.

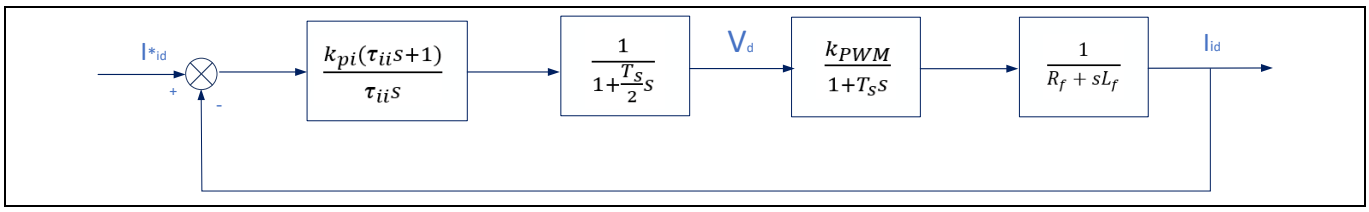


Figure 34 **The entire current control diagram**

If the two first-order blocks are integrated, the final control loop looks like Figure 35.

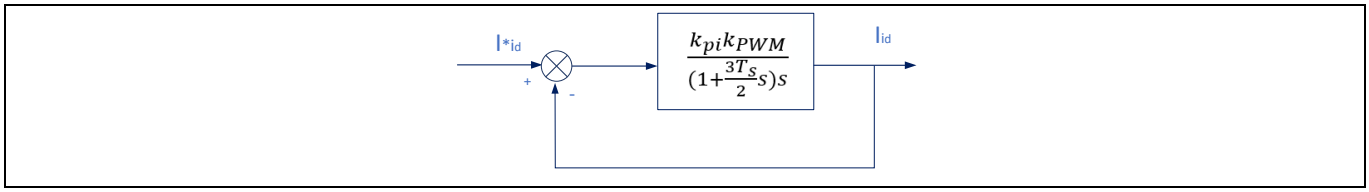


Figure 35 **Offsetting control diagram**

Based on the model above, the type 1 system coefficient can be set to 0.707. The corresponding current PI controller coefficient is then:

$$\frac{1}{2}\sqrt{\frac{1}{\frac{3k_{pi}k_{PWM}T_s}{2L_f}}} = 0.707 \tag{6}$$

$$\begin{cases} k_{pi} = \frac{L_f}{R_f} \\ \tau_{ii} = \frac{L_f}{3k_{PWM}T_s} \end{cases} \tag{7}$$

After calculating the parameter, the frequency response can be drawn in MATLAB. Figure 36 shows the corresponding bode diagram.

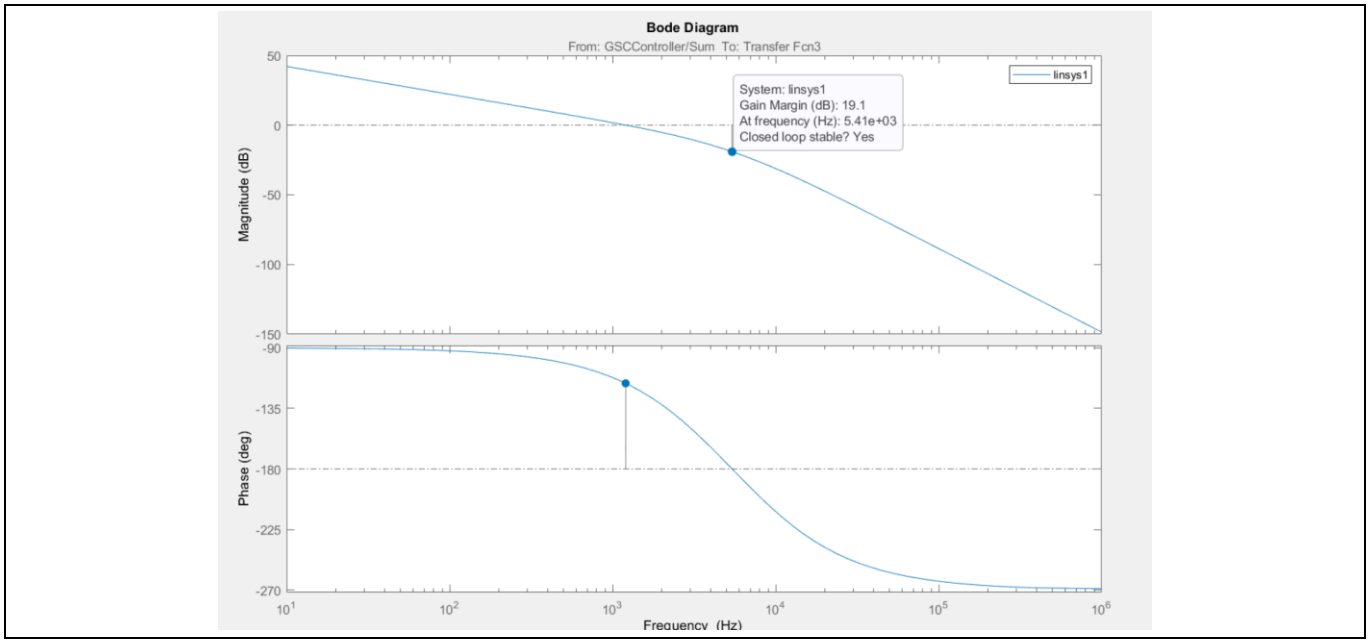


Figure 36 **Frequency response of the current control loop diagram**

3.2.2.3 Voltage loop design

The double loop control diagram is shown in Figure 37, include the current loop and the AC voltage loop. This control diagram is suitable for the grid-off control mode.

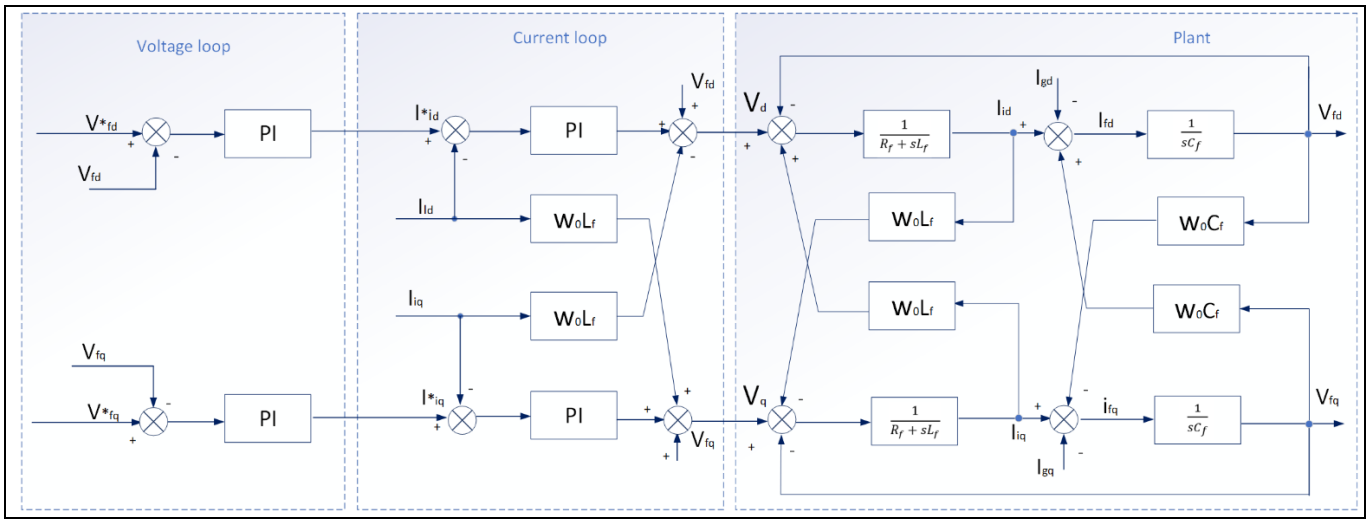


Figure 37 **Double control loop diagram**

To get better performance, the voltage controller can be designed into a type 2 system. Figure 38 shows the typical structure.

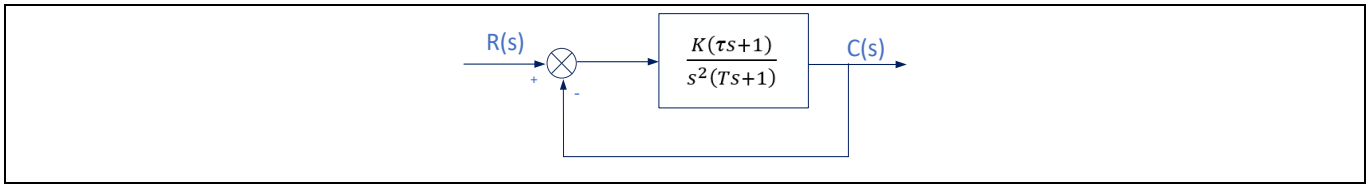


Figure 38 **A typical type 2 system**

The d axis should be picked to design the voltage controller. Figure 39 shows the entire control diagram, and it is the same for the q axis.

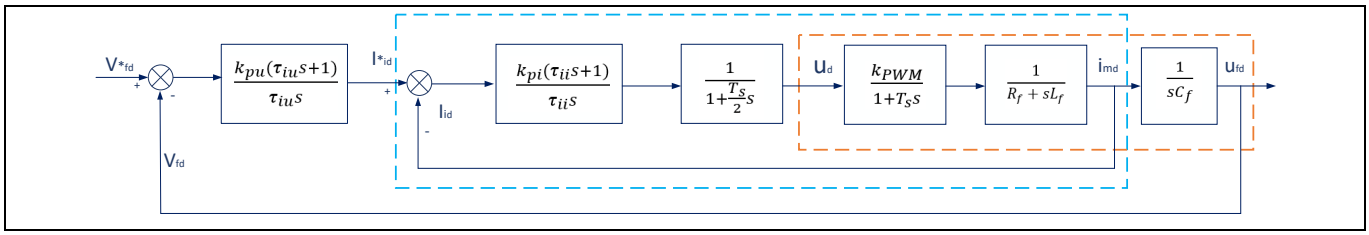


Figure 39 **The entire voltage control diagram**

As the current controller is already designed, the two first-order blocks can be integrated together. The corresponding control loop changes.

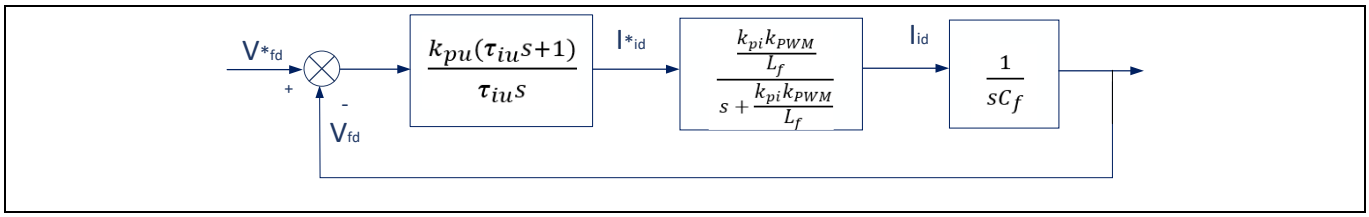


Figure 40 **Integrate control diagram**

To become a type 2 system, some offsetting should be added to the control loop.

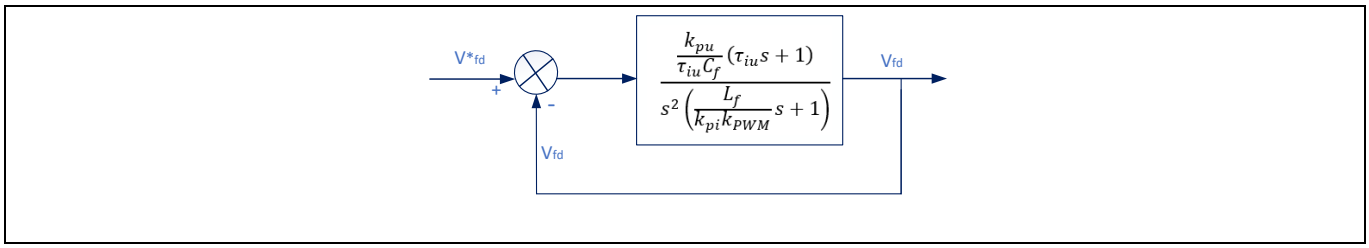


Figure 41 **Offsetting control diagram**

If h and T are set to type 2 system coefficient, the corresponding coefficients of the voltage PI controller can be obtained by:

$$\tau = hT \tag{8}$$

$$k = \omega_1\omega_c = \omega_1^2\frac{h+1}{2} = \left(\frac{1}{hT}\right)^2\frac{h+1}{2} = \frac{1}{2h^2T^2} \tag{9}$$

$$\tau_{iu} = h\frac{L_f}{k_{pi}k_{PWM}} \tag{10}$$

$$k_{pu} = \frac{(h+1)C_f\tau_{iu}}{2h^2\left(\frac{L_f}{k_{pi}k_{PWM}}\right)^2} \tag{11}$$

After calculating the parameter, the frequency response can be drawn in MATLAB. Figure 42 shows the corresponding bode diagram.

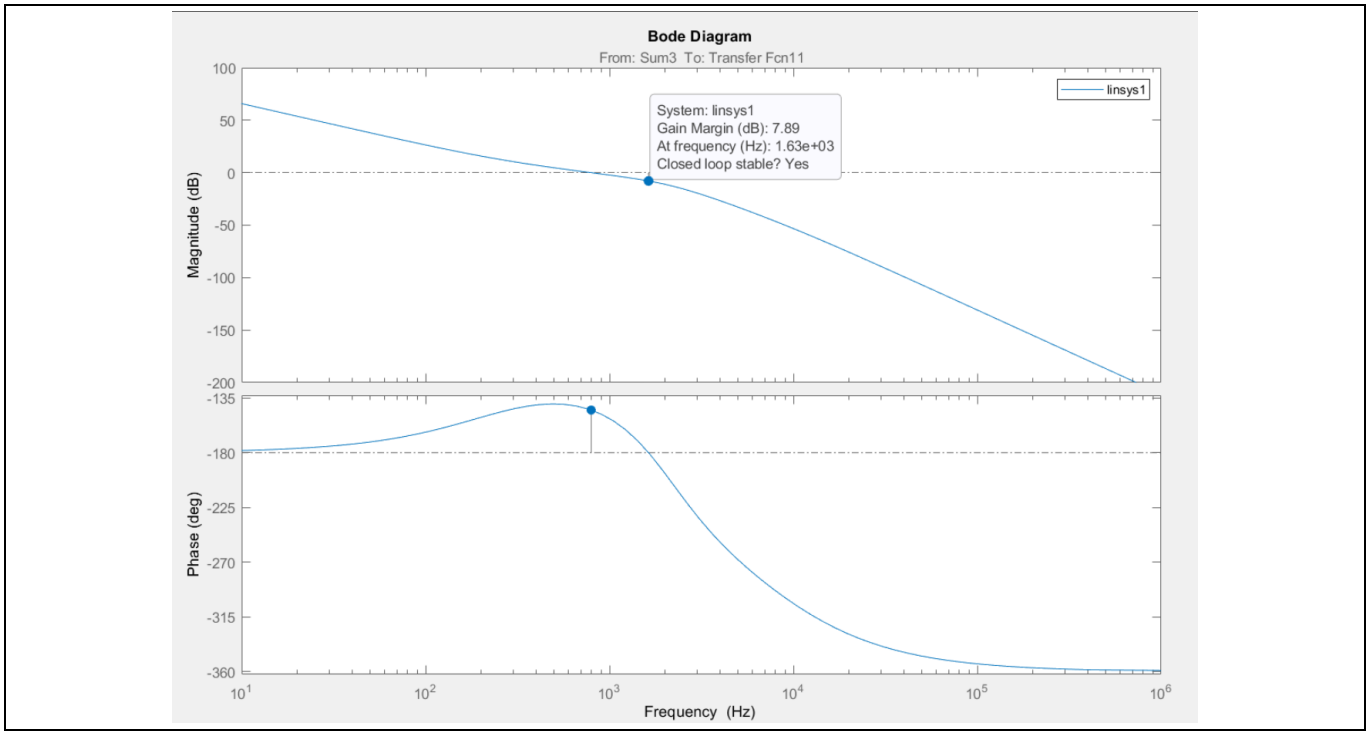


Figure 42 **Frequency response**

3.2.2.4 Power loop design

The double loop control diagram is shown in Figure 43, include the current loop and the AC power loop. This control diagram is suitable for the grid-tied control mode.

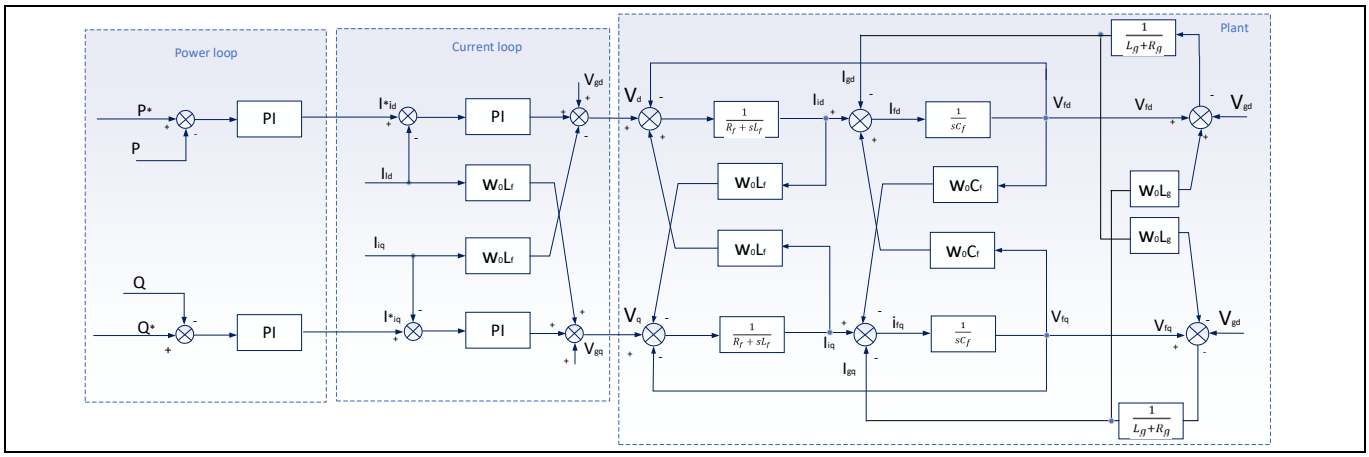


Figure 43 **Power loop and current loop diagram**

To get better performance, the voltage controller can be designed into a type 2 system. Refer to Figure 38 for the typical type 2 system structure.

The d axis should be picked to design the AC power controller. Figure 44 shows the entire control diagram, and it is the same for the q axis.

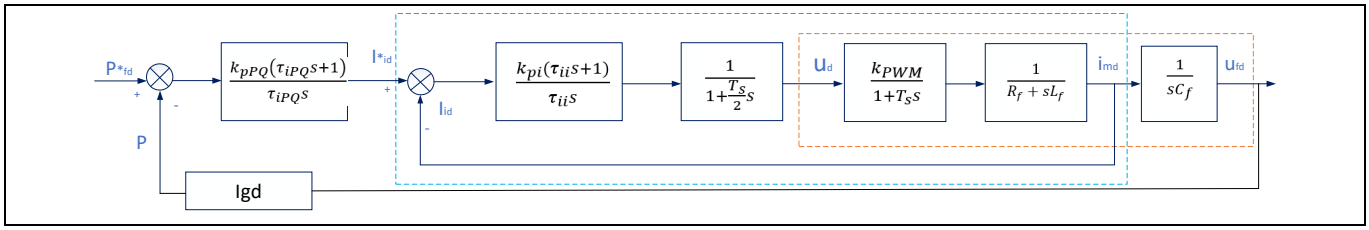


Figure 44 **The entire power control diagram**

As the current controller is already designed, the two first-order blocks can be integrated together. The corresponding control loop changes.

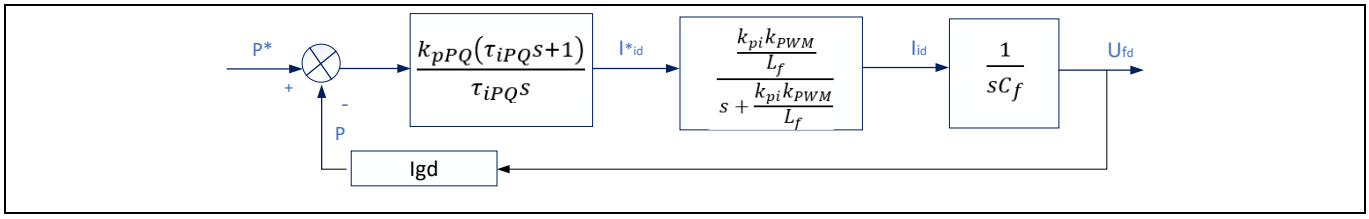


Figure 45 **Integrate control diagram**

Integrate the two first-order blocks together. If h and T are set to type 2 system coefficient, the corresponding coefficients of the power PI controller can be obtained by

$$\tau = hT \tag{12}$$

$$k = \omega_1 \omega_c = \omega_1^2 \frac{h+1}{2} = \left(\frac{1}{hT}\right)^2 \frac{h+1}{2} = \frac{1}{2h^2T^2} \tag{13}$$

$$\tau_{iPQ} = h\frac{L_f}{k_{pi}k_{PWM}} \tag{14}$$

$$k_{pPQ} = \frac{(h+1)C_f\tau_{iPQ}}{2h^2\left(\frac{L_f}{k_{pi}k_{PWM}}\right)^2} \tag{15}$$

3.3 Introducing the functional architecture and task

3.3.1 Functional architecture of the control software

Figure 46 shows the entire GTI application model.

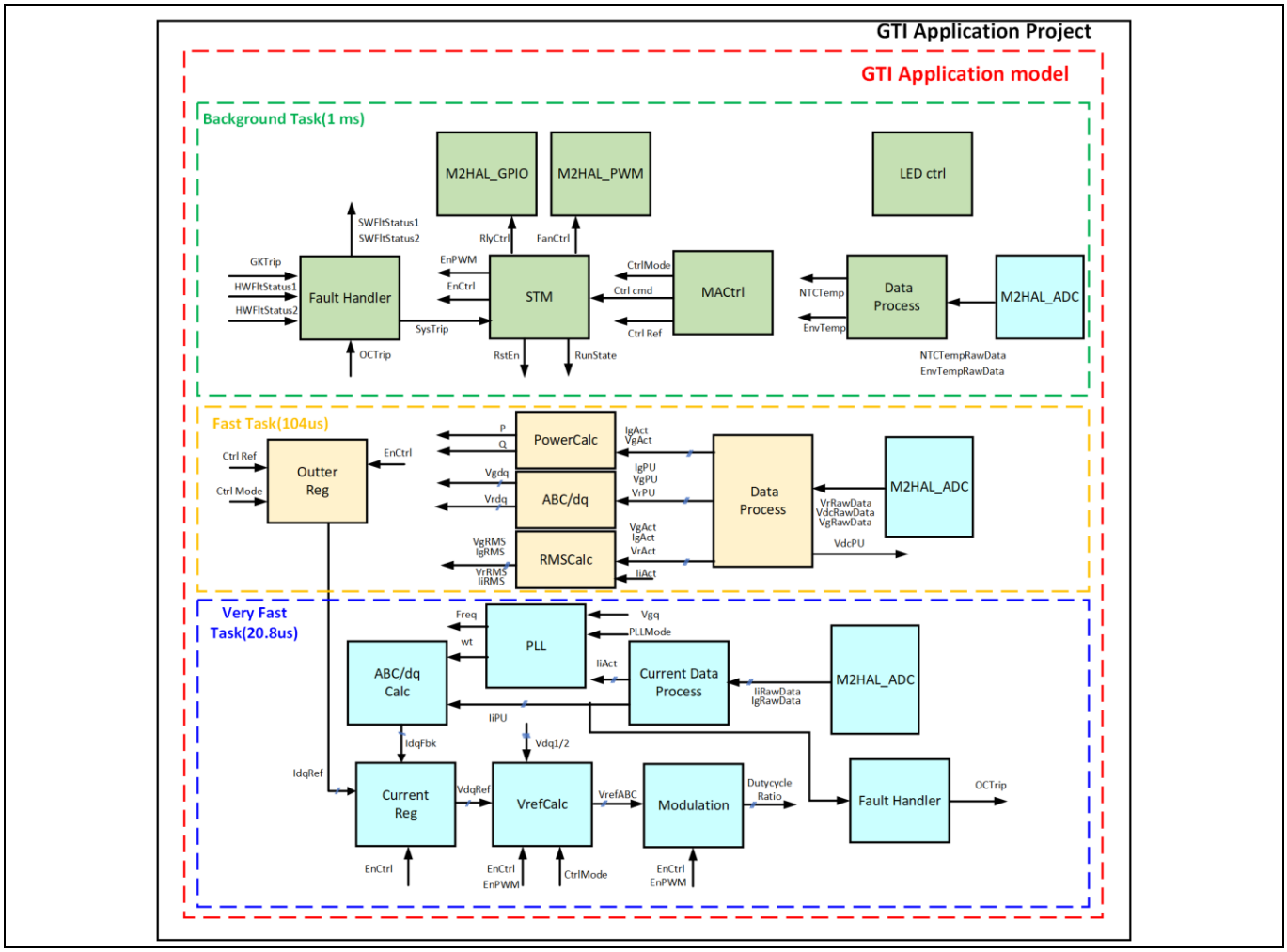


Figure 46 **Functional/Task architecture**

The entire software platform consists of four tasks: Very fast task, fast task, background task, and PWM kill task. The following sections describe these tasks in detail.

3.3.1.1 Very fast task

This task model includes PWMOut, VeryFastAlg, and ADCGet_VF blocks. The PWMOut and ADCGet_VF blocks are the interface to the ADC/PWM peripherals. The core functions and algorithms are all in the VeryFastAlg block.

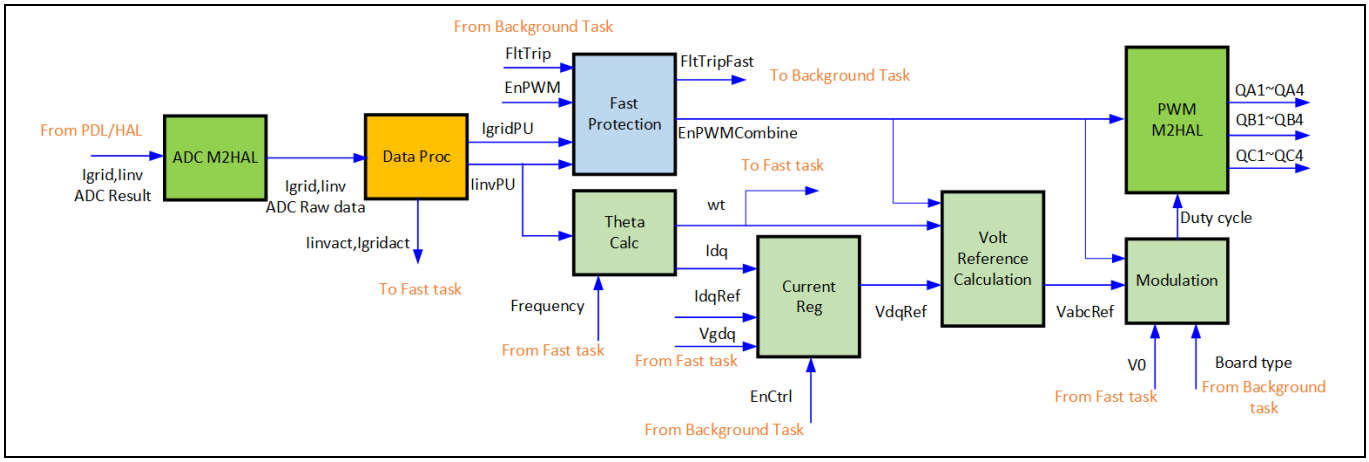


Figure 47 **Very fast task description**

The VeryFastAlg block consists of the following:

- DataProcFast: To calculate the actual value and per unit value of the inverter/grid current from the raw ADC data.
- CurrProtection: To implement the inverter/grid overcurrent protection according to maximum absolute value of the three-phase per unit current value. At the same time combine the slow fault trip, PWM enable, and local overcurrent trip signal together to determine the final PWM enable signal
- ThetaCalc: To calculate the angle, Sine, and cosine values according to the AC frequency, and calculate the current component of the d/q axis
- CurrReg: To implement the current control loop on the d/q axis. The input is current reference/feedback, voltage feedforward, and controller enable signal. The output is voltage control signal
- VabcRefCalc: To calculate the voltage control signal on the abc axis from the d/q axis of the CurrReg. When the PWM enable signal is high, choose the VrefCalcActFun block or the VrefCalcRstFcn block, otherwise the output equals 0
- Modulation: To calculate the voltage control signal on the abc axis from the d/q axis of the CurrReg/modulation index. When the PWM enable signal is high, the block chooses the ModuActFun block, otherwise choose the ModuRstFun block

3.3.1.2 Fast task

There are two blocks included in this fast task model: ADCGet_Fast and FastAlg. The ADCGet_Fast block is the interface to ADC peripherals. The core functions and algorithms are all in the FastAlg block.

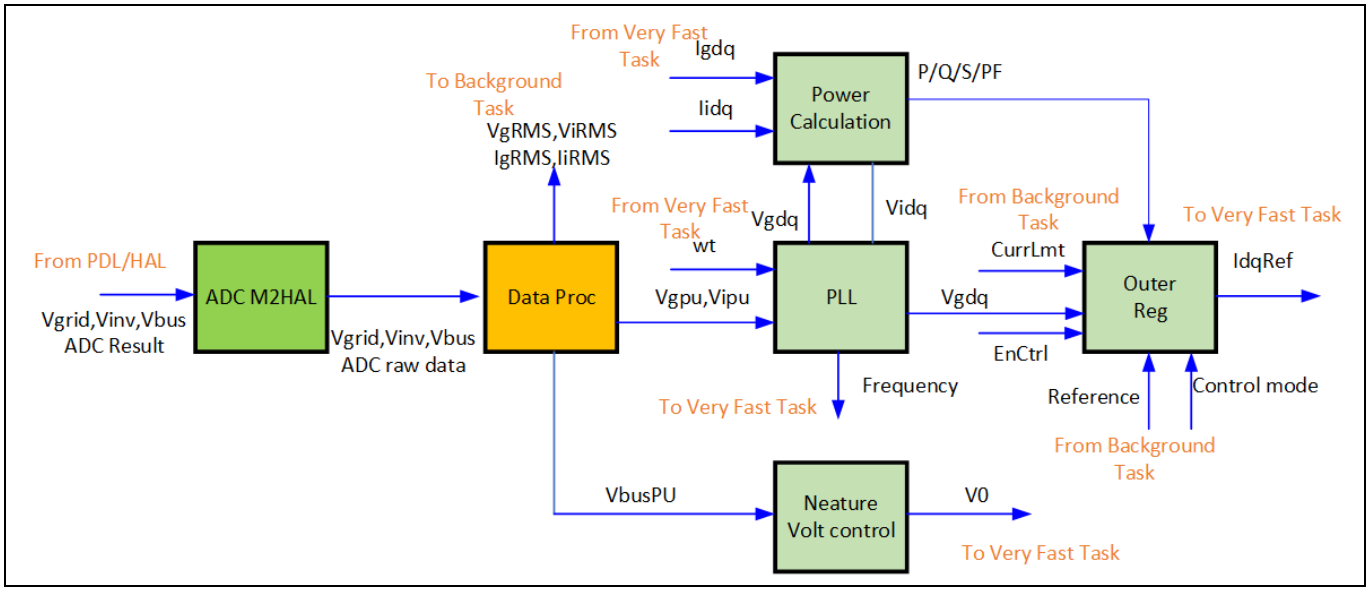


Figure 48 **Fast task description**

The FastAlg block contains five function blocks:

- DataProc: To calculate the actual value and per unit value of AC/DC voltage from the raw ADC data and calculate the root mean square (RMS) value of the AC current/voltage from the actual value
- Neutral voltage control: For balancing the DC-bus voltage
- PLL: To implement the AC voltage coordinate transformation, AC frequency calculation, and grid synchronization control
- OuterReg: To implement the outer loop controller, support V/F, P/Q and grid synchronize controller, include PI controller, control reference ramp control, and controller selection

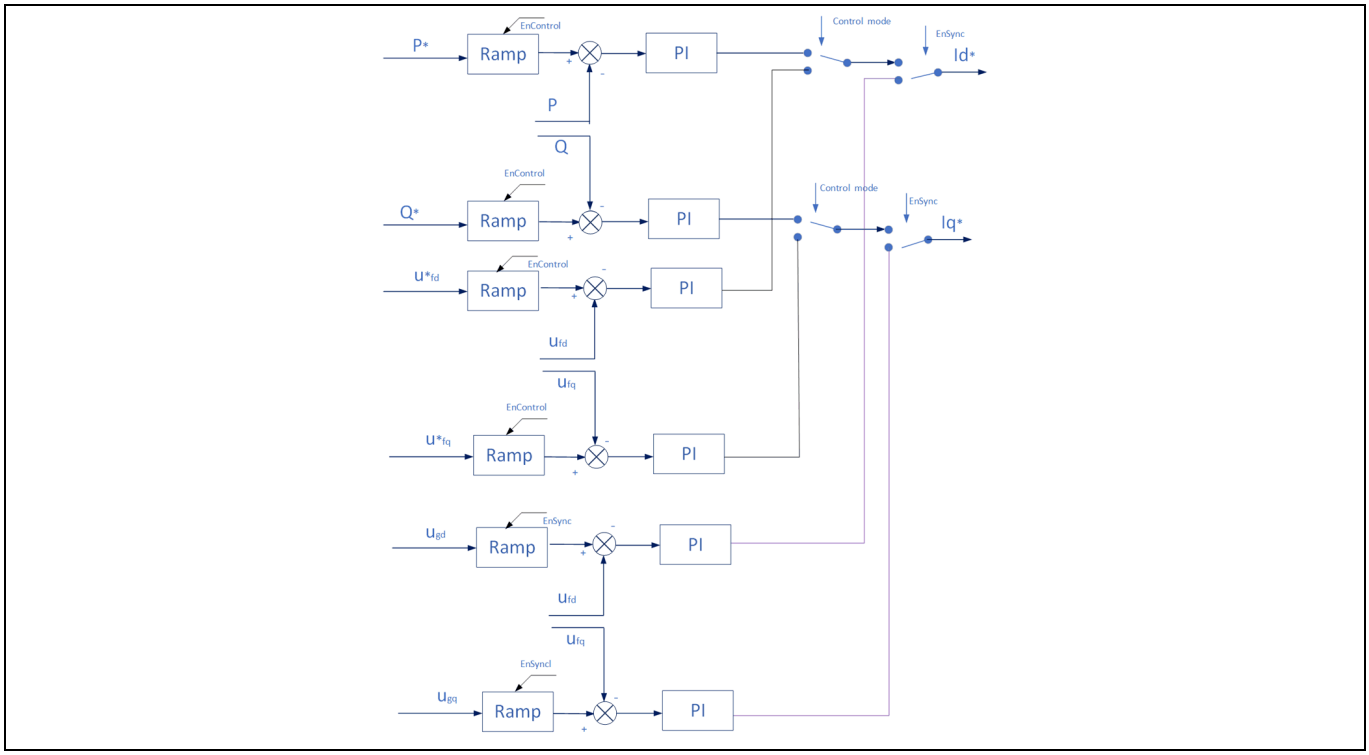


Figure 49 **OuterReg diagram**

- PowerCalc: To calculate the active power, reactive power, apparent power, and power factor of the grid side and inverter side

3.3.1.3 Background task

There are five blocks included in this fast task model: HWFltGet, MACtrl, BckGrdAlg, IOCtrl, and ADCGet_BG. The HWFltGet, MACtrl, IOCtrl, ADCGet_BG blocks are the interfaces to the ADC/PWM/IO peripherals. The core functions and algorithms are all in the BckGrdAlg block.

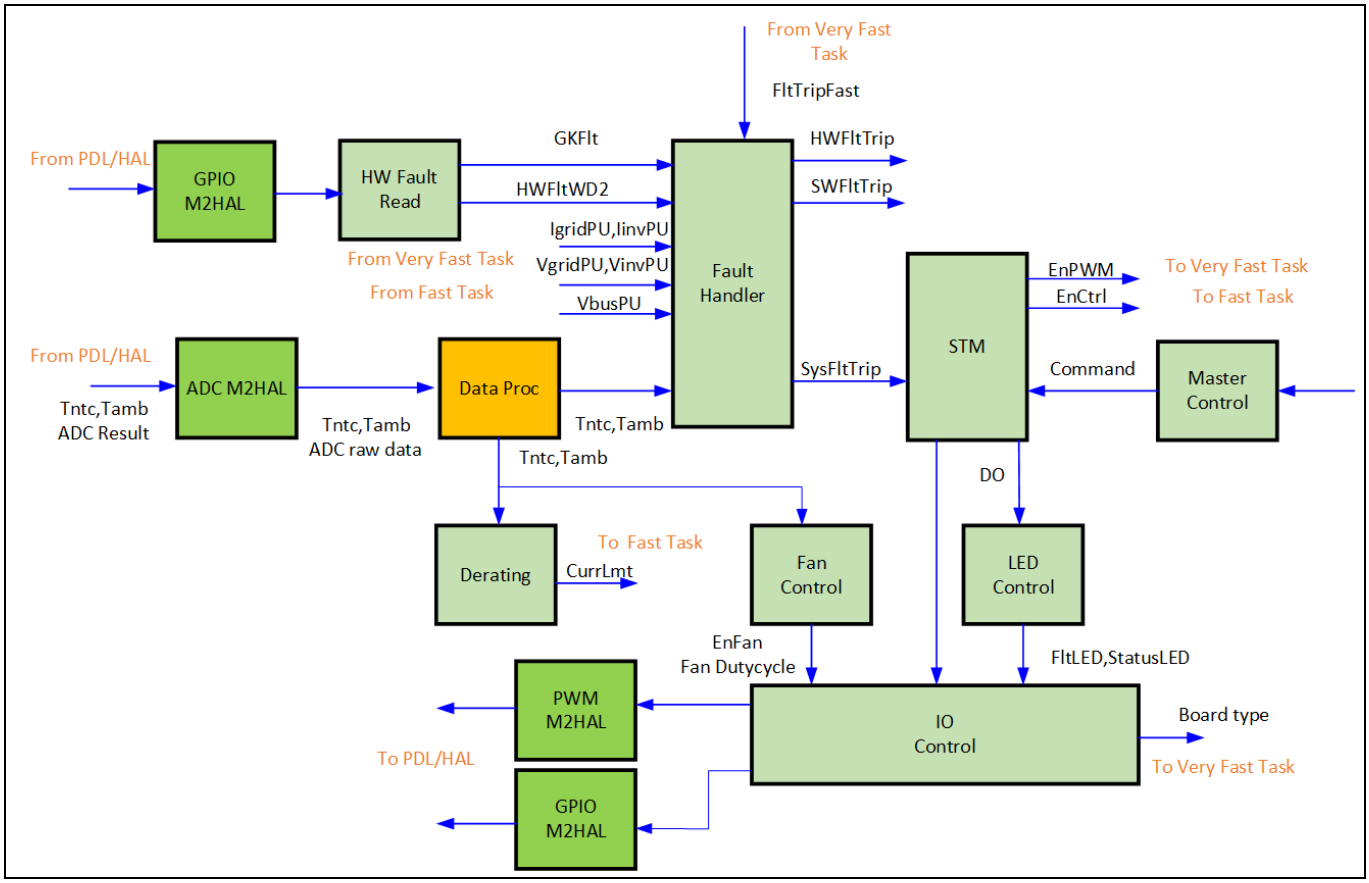


Figure 50 **Background task description**

The BckGrdAlg block contains six function blocks:

- DataProcSL: To calculate temperature
- FltHdl: To detect software and hardware fault
- STM: To control system state machine
- Derating: To derate the system power
- FanCtrl: To control the system fan
- LEDCtrl: To control the system LED

3.3.1.4 State machine

Figure 51 shows the state machine transition condition.

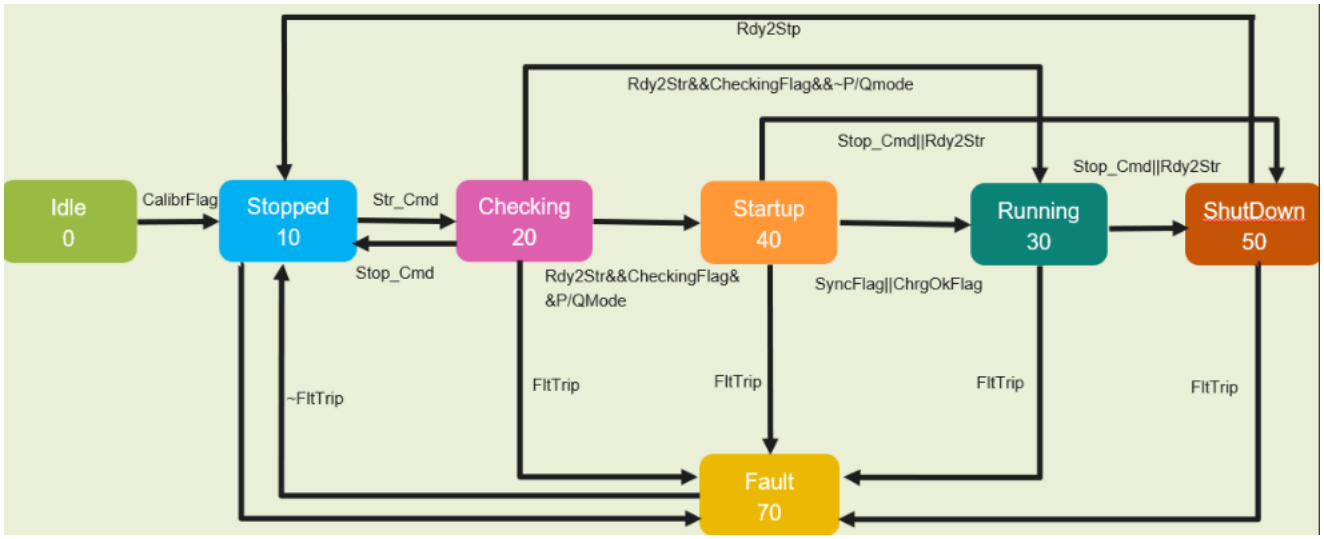


Figure 51 **State machine**

Table 6 Definition of a state machine

State	Value	Description	Control loop	Gating	Comments
IDLE	0	Initial state, calibrating ADC	Disable	Block	
STOPPED	10	Converter not running	Disable	Block	
CHECKING	20	Checking readiness, making sure the relay is closed	Disable	Block	
STARTUP	40	Execute start up sequence, e.g., synchronous	Enable	Allow/Block	Depends on the control mode
RUNNING	30	Converter running	Enable	Allow	
SHUTDOWN	50	Execute shutdown sequence, e.g., Ramp-down	Enable	Allow	
FAULT	70	Converter is in a fault state	Disable	Block	

3.3.1.5 PWM kill task

This task is triggered by a gate kill (GK) signal. It disables the PWM output and reads the hardware fault word1 when the GK signal changes from high to low.

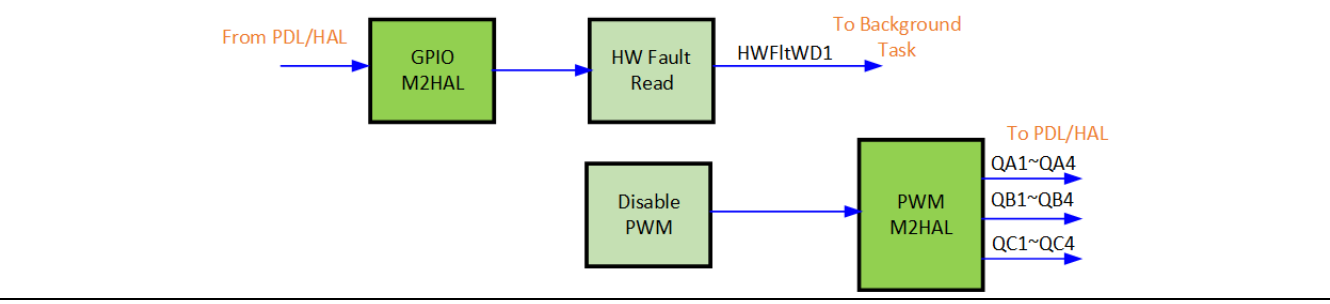


Figure 52 **PWM kill task description**

3.3.2 Deloyment and scheduling of the execution tasks

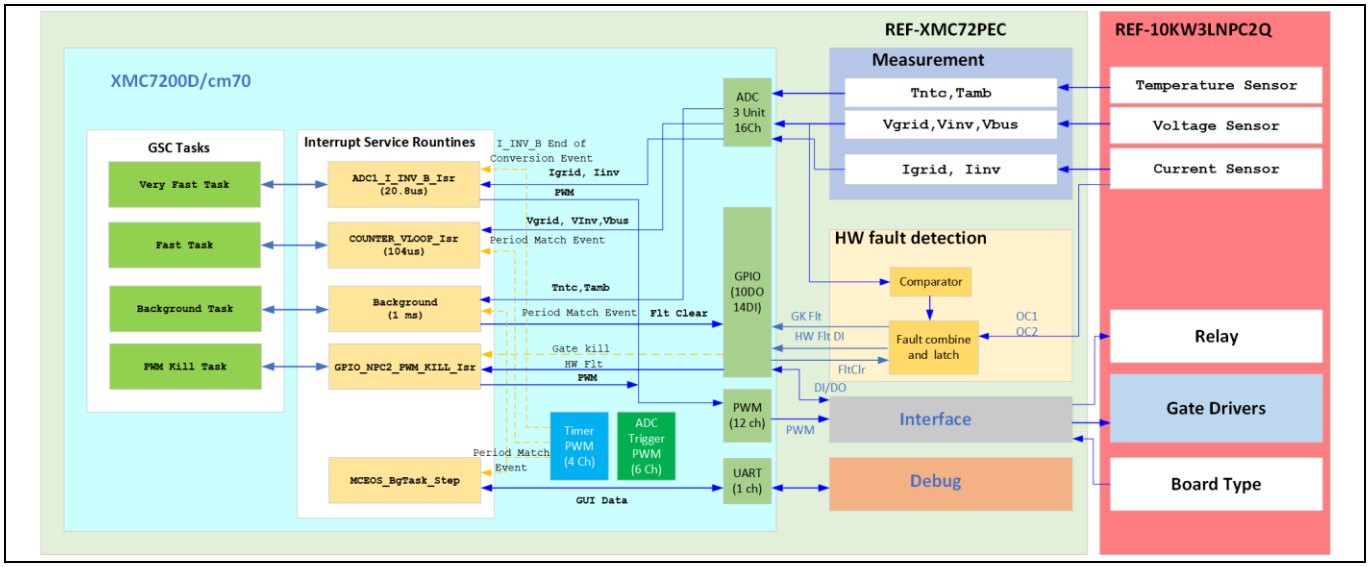


Figure 53 **The hardware and software interface**

Table 7 shows how the execution tasks scheduled with the hardware timmer and ISR (Interrupt Service Routine) are triggered.

Table 7 NPC2Q task

Functionalities	Execution task	ISR timer
Master control	Background task	Background timer
State machine	Background task	Background timer
Fault handler	Background task	Background timer
Fan control	Background task	Background timer
LED control	Background task	Background timer
Derating	Background task	Background timer
Outer loop control	Fast task	COUNTER_ VLOOP timer
Neutral voltage control	Fast task	COUNTER_ VLOOP timer
PLL	Fast task	COUNTER_ VLOOP timer
Power calculation	Fast task	COUNTER_ VLOOP timer
Current protection	Very Fast task	ADC_I_INV timer
Current control loop	Very Fast task	ADC_I_INV timer
Modulation	Very Fast task	ADC_I_INV timer

4 Operation

The 10 kW NPC2 inverter has been tested using the XMC7200-based power control board reference design – REF-CLBXMC7PEC. This reference design can be purchased separately.

The NPC2 inverter was operated in different control modes.

4.1 Introducing the graphical user interface (GUI)

Install the MHI Graphical User Interface available at Infineon Developer Center. Figure 54 shows the GUI of the grid-tied inverter (GTI):

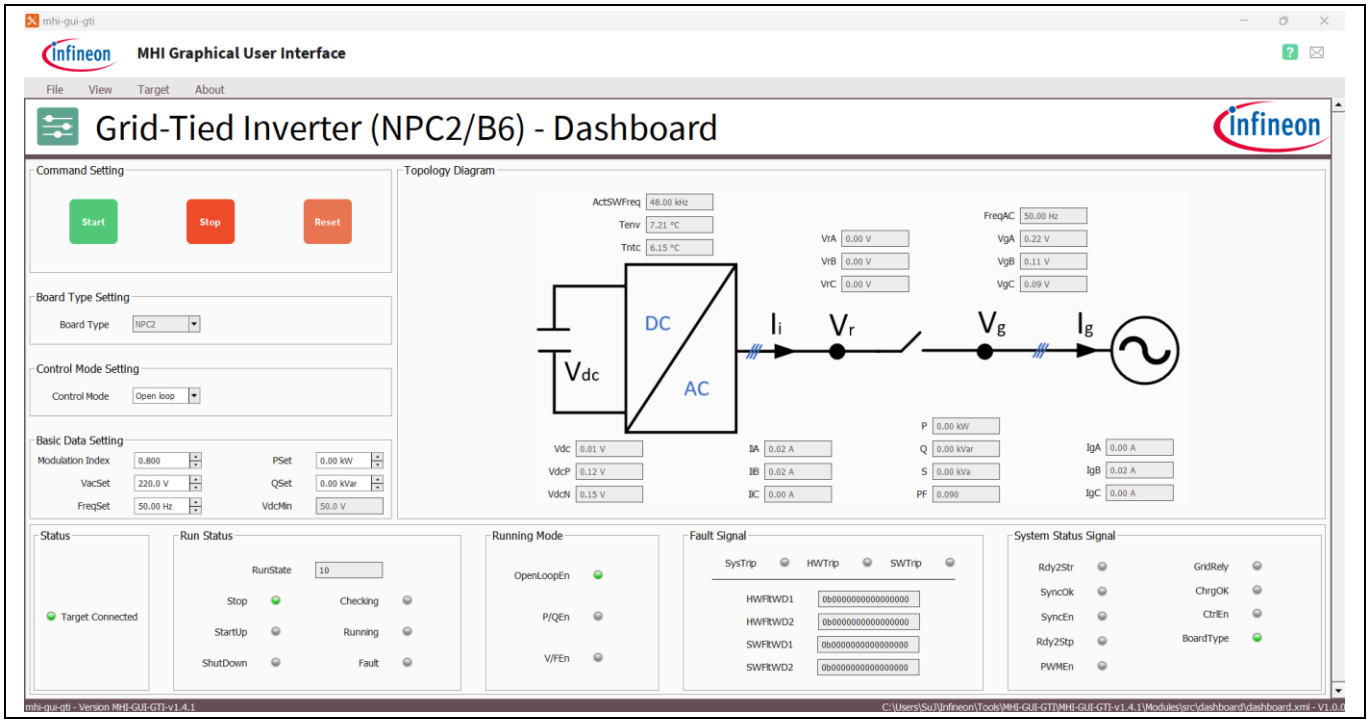


Figure 54 **GTI GUI**

The following sections explain the different functionalities of the GUI.

4.1.1 Target panel

The target panel is used to flash the firmware to the target and connect to the hardware.

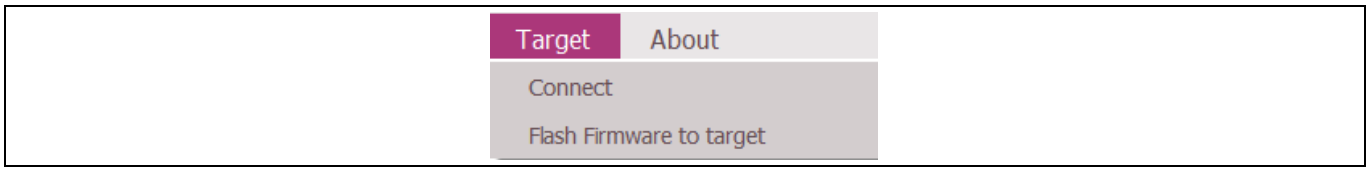


Figure 55 **Target panel**

4.1.2 Settinngs

Settings options can be used to apply changes to the firmware. These parameters take effect immediately after the values are set. Users can use the arrow buttons to change the values or can enter them directly into the input field.

4.1.2.1 Command setting

These buttons are used to set the converter in the loop mode, to stop the converter, or to reset the converter's fault state respectively. The Reset button can be used after a fault has cleared. Before beginning the evaluation, users must click the Reset button.

Figure 56 **Command setting**

4.1.2.2 Board type setting

The board type must be set to NPC2.

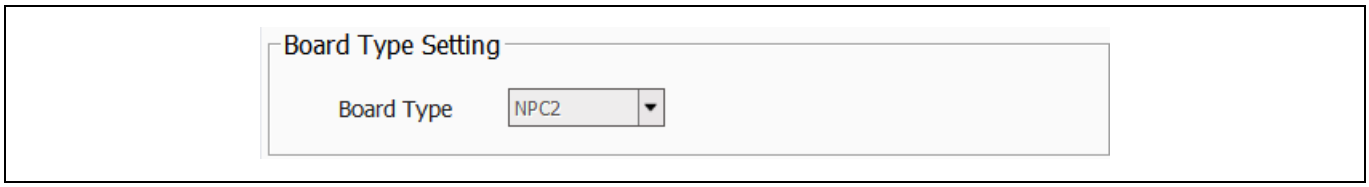


Figure 57 **Board type setting**

4.1.2.3 Control mode setting

The control mode must be set to Open loop, P/Q, or V/F.

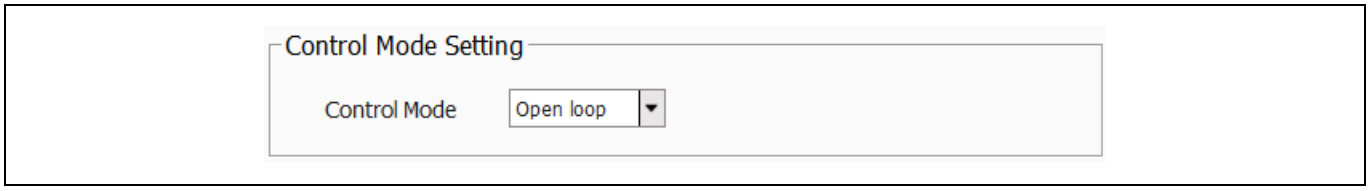


Figure 58 **Control mode setting**

4.1.2.4 Basic data setting

The relevant basic data can be set based on the descriptions provided in Section 4.1.4.

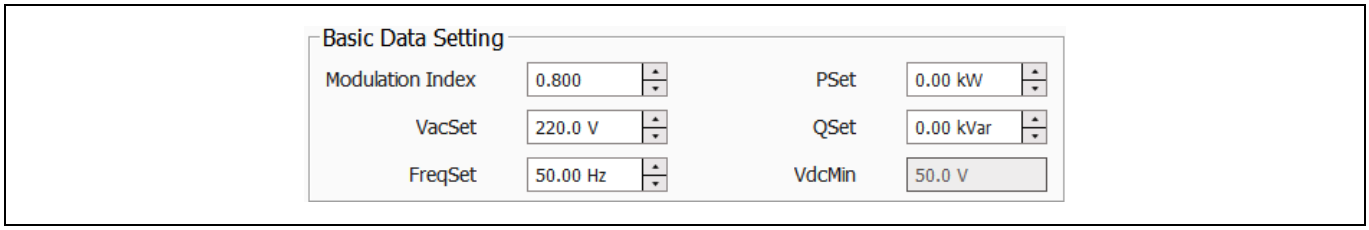


Figure 59 **Basic data setting**

4.1.3 Inverter status

The following sections describe the signals that indicate the current state of the inverter.

4.1.3.1 GTI topology diagram

The top right of the GUI window contains the GTI topology diagram that displays several signals. These signals are “read only”.

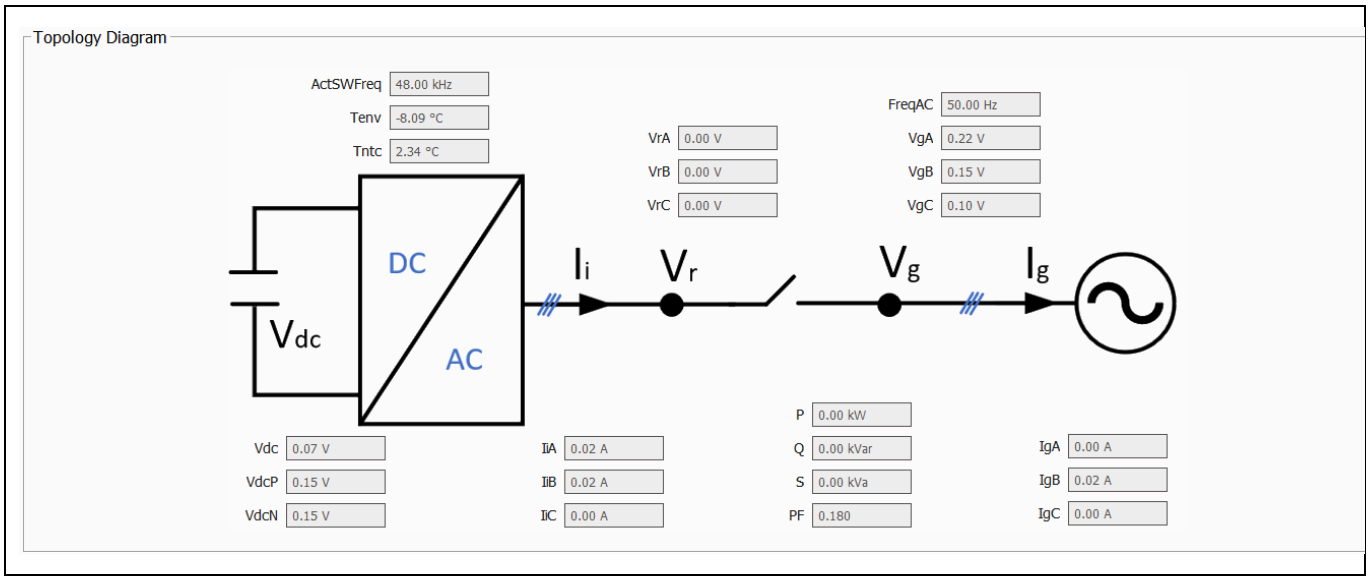


Figure 60 **GTI topology diagram**

4.1.3.2 Status

The bottom left of the GUI window shows the connection status. It indicates the present connection status to the target. It can be used to detect if there is any active connection to the target or not. The red LED sign means that the target is not connected while the green LED means a connection is active.

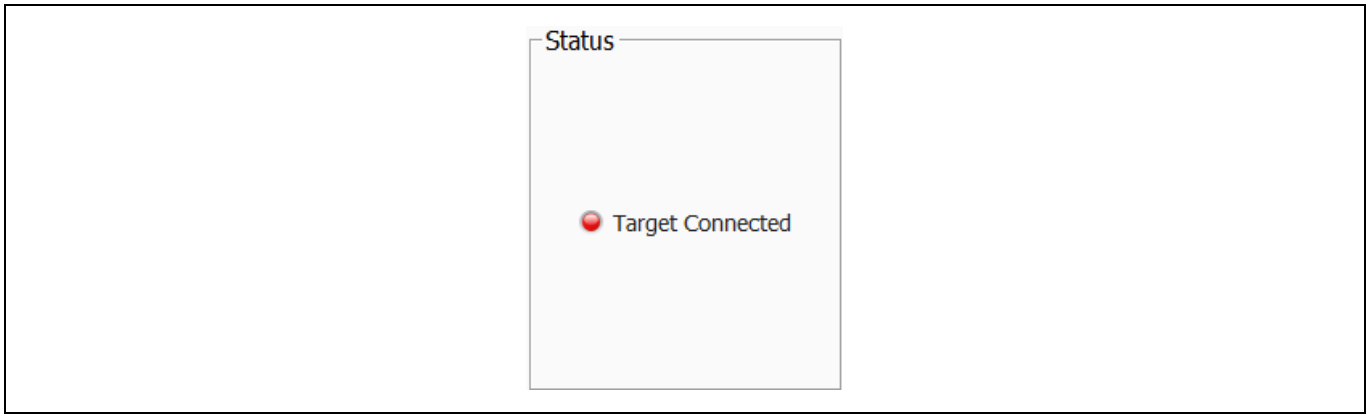


Figure 61 **Status**

4.1.3.3 Run status

The run status section reflects the state of the GTI inverter. A gray LED indicates that the state is not active. A green LED indicates that the state is active.

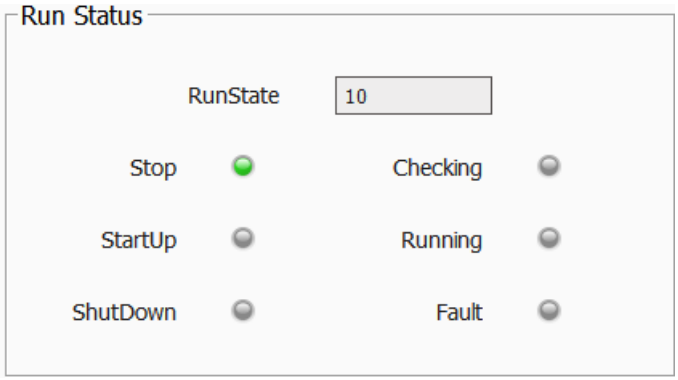


Figure 62 **Run status**

4.1.3.4 Running mode

This section displays the selected running mode.

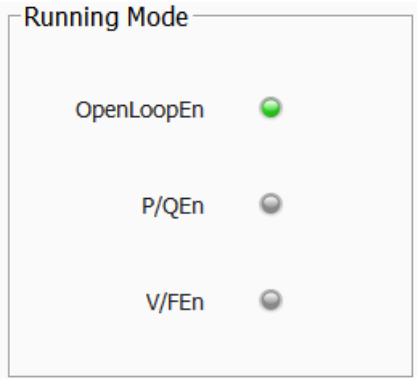


Figure 63 **Running mode**

4.1.3.5 Fault signal

This section displays the fault signals. A grey LED indicates that the fault is not active. A red LED indicates the fault is active. HWFltWD1, HWFltWD2, SWFltWD1, and SWFltWD2 are displayed in binary values. Their detailed description is provided in Section 4.1.4.

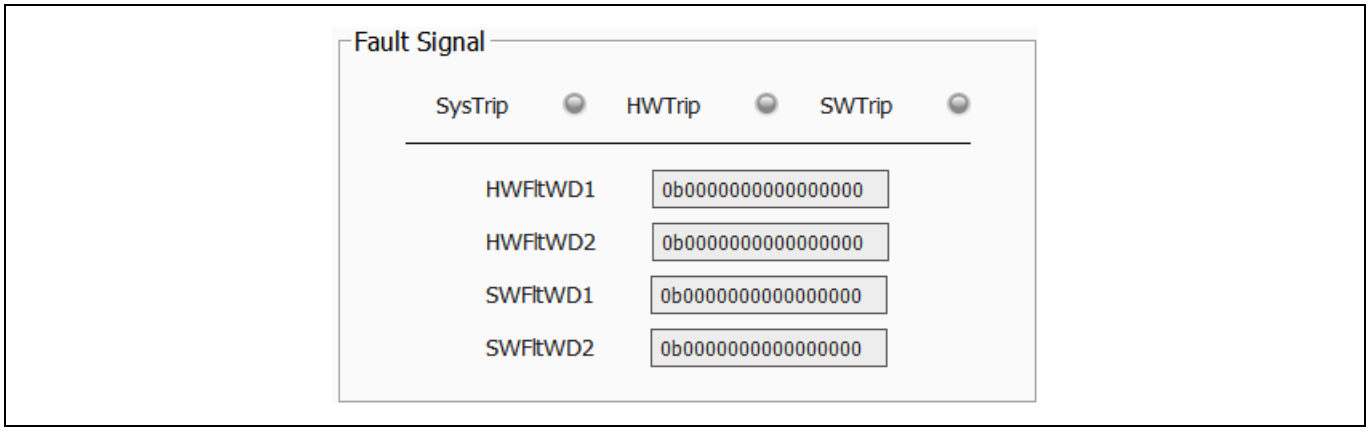


Figure 64 **Fault signal**

4.1.3.6 System status signal

This section displays the system status signals. A detailed description is provided in Section 4.1.4.

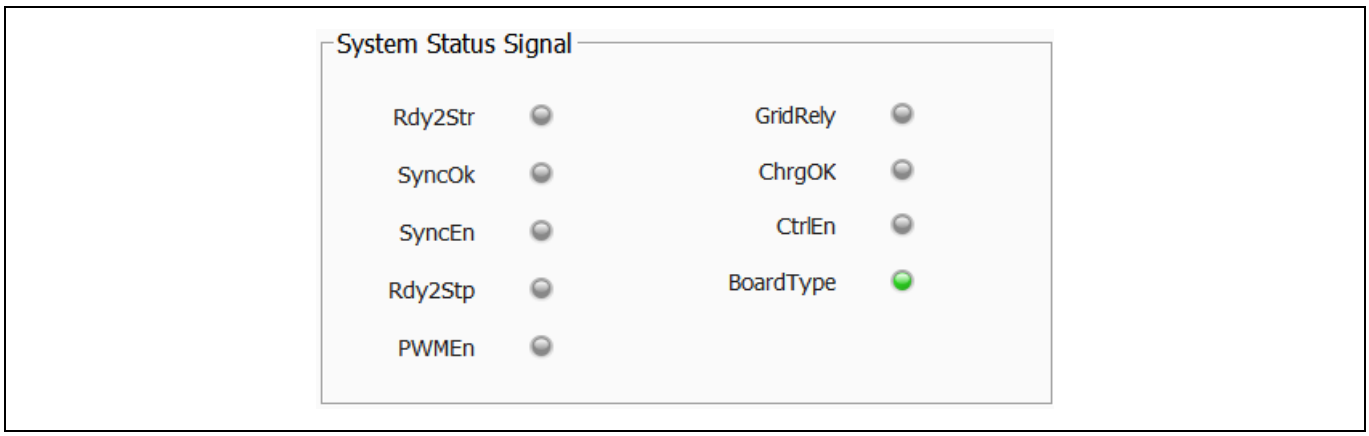


Figure 65 **System status signal**

4.1.4 GUI parameters

Table 8 GUI parameters

No.	Name	Min	Max	Default Values	Step	Unit	Description	Comment
	Settings (Setpoints)							
1	Start	n/a	n/a	n/a	n/a	n/a	Start the converter	
2	Stop	n/a	n/a	n/a	n/a	n/a	Stop the converter	
3	Reset	n/a	n/a	n/a	n/a	n/a	Reset the fault words/status	This is a button
4	Board Type	n/a	n/a	n/a	n/a	n/a	0 represents B6 1 represents NPC2	Combo box
5	Control Mode	n/a	n/a	n/a	n/a	n/a	Grid-tied inverter control mode. 0 represents Open loop, 3 represents P/Q,	Combo box

							5 represents V/F	
6	Modulation Index	0	1	0.8	0.1	n/a	Output modulation index setting, only for open-loop control mode	
7	PSet	-12	12	0	1	kW	Output active power setting, only for P/Q control mode	
8	QSet	-12	12	0	1	kVar	Output reactive power setting, only for P/Q control mode	
9	VacSet	10	400	220	1	V	Output AC phase voltage amplitude setting, only for V/F control mode	
10	FreSet	40	65	50	1	Hz	Output AC voltage frequency setting, only for open loop and V/F control mode	
11	VdcMin	50	1200	n/a	n/a	V	Minimum required DC voltage	
	Signals							
1	ActSWFreq	0	100	n/a	n/a	kHz	The actual switch frequency from firmware	
2	Tenv	-50	200	n/a	n/a	℃	The temperature of environment	
3	Tntc	-50	200	n/a	n/a	℃	The temperature of IGBT	
4	Vdc	0	1200	n/a	n/a	V	Actual value of DC voltage	
5	VdcP	0	1200	n/a	n/a	V	Actual value of DC positive voltage	
6	VdcN	0	1200	n/a	n/a	V	Actual value of DC negative voltage	
7	VrA	0	500	n/a	n/a	V	RMS value of phase A inverter voltage	
8	VrB	0	500	n/a	n/a	V	RMS value of phase B inverter voltage	
9	VrC	0	500	n/a	n/a	V	RMS value of phase C inverter voltage	
10	IiA	0	100	n/a	n/a	A	RMS value of phase A inverter current	
11	IiB	0	100	n/a	n/a	A	RMS value of phase B inverter current	
12	IiC	0	100	n/a	n/a	A	RMS value of phase C inverter current	
13	FreqAC	40	65	n/a	n/a	Hz		

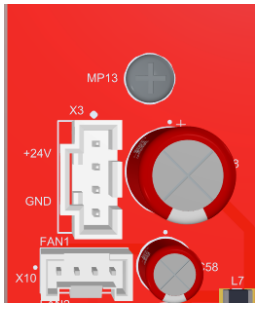
14	VgA	0	500	n/a	n/a	V	RMS value of phase A grid voltage	
15	VgB	0	500	n/a	n/a	V	RMS value of phase B grid voltage	
16	VgC	0	500	n/a	n/a	V	RMS value of phase C grid voltage	
17	P	-100	100	n/a	n/a	kW	Active power of grid side	
18	Q	-100	100	n/a	n/a	kVar	Reactive power of grid side	
19	S	-100	100	n/a	n/a	kVA	Apparent power of grid side	
20	PF	-1	1	n/a	n/a	n/a	Power factor of grid side	
21	IgA	0	100	n/a	n/a	A	RMS value of phase A grid current	
22	IgB	0	100	n/a	n/a	A	RMS value of phase B grid current	
23	IgC	0	100	n/a	n/a	A	RMS value of phase C grid current	
	Status							
1	Target connected	n/a	n/a	n/a	n/a	n/a	Connection Status	LED
2	Runstate	0	255	n/a	n/a	n/a	States of the GTI converter: 10: Stopped state 20: Checking state 30: Running state 40: Startup state 50: Shutdown state 70: Fault state	Every state can be displayed via LEDs, green means 1, gray means 0.
3	OpenLoopEn	0	1	n/a	n/a	n/a	Open-loop control enable status	LED
4	P/QEn	0	1	n/a	n/a	n/a	P/Q control enable status	LED
5	V/FEn	0	1	n/a	n/a	n/a	V/F control enable	LED
6	SysTrip	0	1	n/a	n/a	n/a	Converter system fault-trip signal	LED
7	HWTrip	0	1	n/a	n/a	n/a	Converter hardware fault-trip signal	LED
8	SWTrip	0	1	n/a	n/a	n/a	Converter software fault-trip signal	LED
9	HWFItWD1	0	65535	n/a	n/a	n/a	Converter hardware fault word1	Display in binary
10	HWFItWD2	0	65535	n/a	n/a	n/a	Converter hardware fault word2	Display in binary
11	SWFItWD1	0	65535	n/a	n/a	n/a	Converter software fault word1	Display in binary

12	SWFItWD2	0	65535	n/a	n/a	n/a	Converter software fault word2	Display in binary
13	Rdy2Str	0	1	n/a	n/a	n/a	Converter ready to start status	LED
14	SyncOk	0	1	n/a	n/a	n/a	Converter synchronize OK status	LED
15	SyncEn	0	1	n/a	n/a	n/a	Converter synchronize enable status	LED
16	Rdy2Stp	0	1	n/a	n/a	n/a	Converter ready to stop status	LED
17	PWMEn	0	1	n/a	n/a	n/a	Converter PWM-enable signal	LED
18	GridRely	0	1	n/a	n/a	n/a	Converter grid relay-control signal	LED
19	ChrgOK	0	1	n/a	n/a	n/a	Converter DC charge-OK status	LED
20	CtrEn	0	1	n/a	n/a	n/a	Converter controller-enable signal	LED
21	BoardType	0	1	n/a	n/a	n/a	The actual power board type: 1 means NPC2 0 means B6	LED, from the power board

4.1.5 Establishing a connection

Steps to establish a connection between the PC and the control board

1. Ensure that the NPC2 board and the control board are connected as described in the section on bench setup. The signal cables from the power board provide power to the control board. No external power supply is required for the control board.
2. Connect a DC power supply to the power board. Refer to Table 3 for the specification of power supply card.



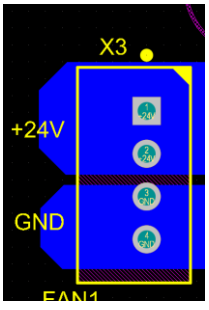


Figure 66 **24 V connector**

3. In the COM port setting in the GUI, choose the COM port to which the control board is connected. This can be checked in the device manager.
4. Click Open COM.

5. If everything is set correctly, the values will appear in the GUI.
6. After the bench setup is done, click Start to evaluate the hardware.

4.2 Flashing the firmware

Steps to flash the firmware

1. Shut down the power stage to put it into safe state.
2. Connect 24 V to the control board.
3. Add three jumper headers as shown in Figure 67.
4. Connect the debug port of the control board to the PC with a USB cable.

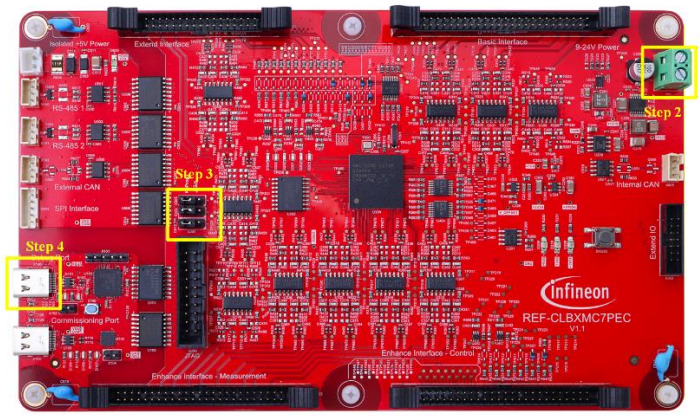


Figure 67 **REF-CLBXMC7PEC debug configuration**

5. Start the MHI-GUI GTI application.

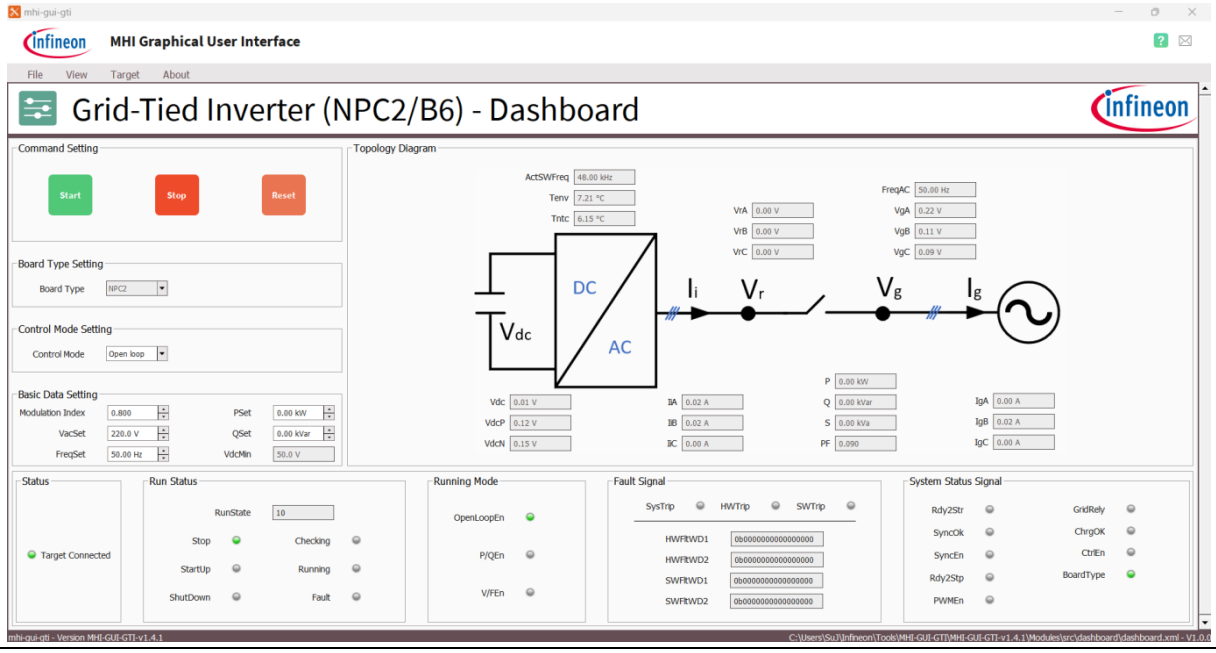


Figure 68 **MHI-GTI GUI**

6. Click Flash Firmware to target and wait until the tool flashes the firmware to the target. A message will appear after the operation is complete. Please note, this operation needs to be done only once.

Figure 69 **Flashing the firmware**

7. Click Connect, then click Connect to server.
8. Choose the COM port (defined in the device manager) and click connect.
9. Click Close to close the window.

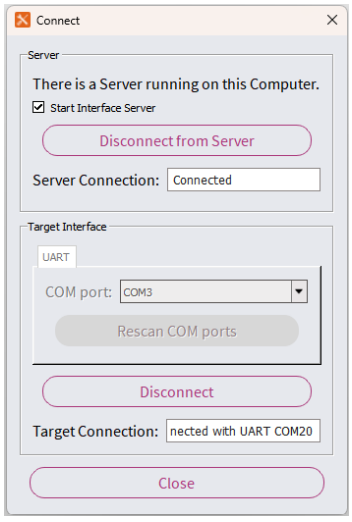


Figure 70 **Connecting to the target**

10. Disconnect the external 24 V power supply.

4.3 Test bench set up

The following equipment is required to begin testing:

- REF-10KW3LNPC2 power board
- REF-CLBXMC7PEC control card with the NPC2 firmware
- GTI GUI
- Resistive load: 3-phase star connected
- DC power source

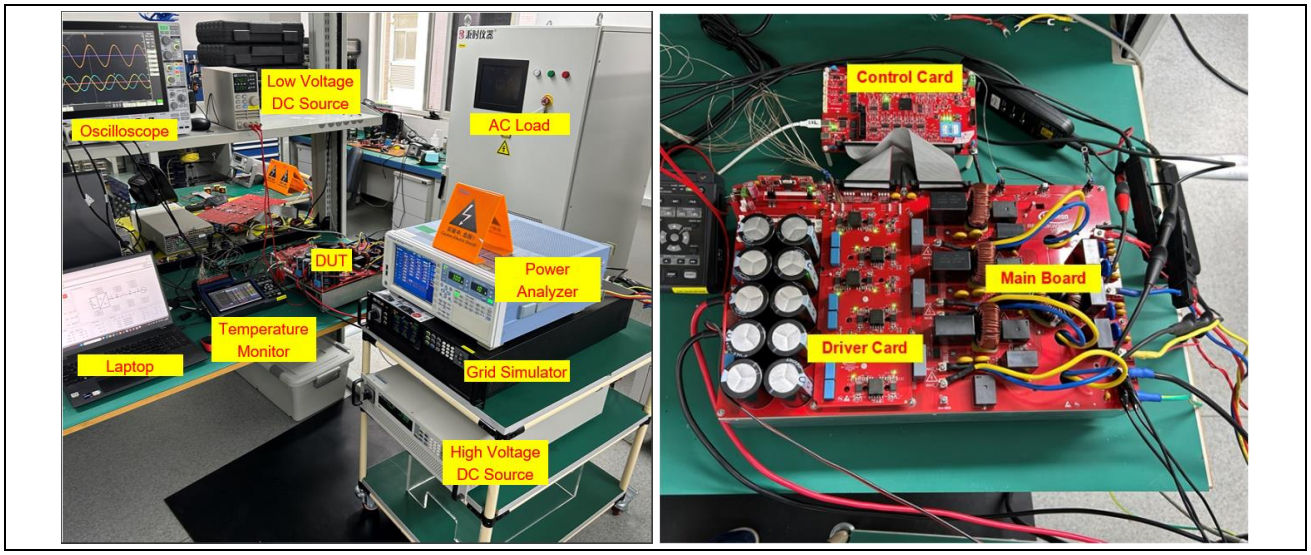


Figure 71 **Test bench setup**

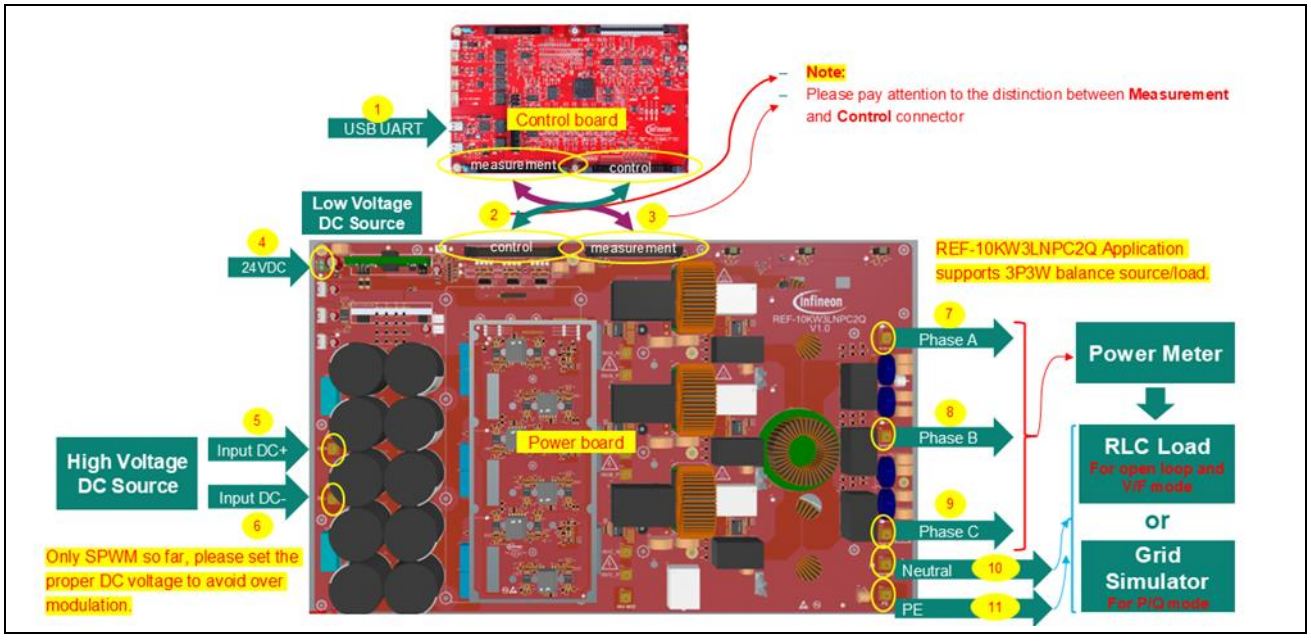


Figure 72 **Detail description for test bench setup**

Figure 71 shows a possible test bench setup for your reference, here are the steps to set up the test bench:

1. Complete the hardware connection according to Figure 72 and follow the steps 1 to 11 as depicted. Note the distinction between the measurement and the control connector.
2. Power on the external 24 V_{dc}.
3. Set up parameters of the system using the GTI GUI.
4. Power on the high-voltage DC source.
5. Run the system.

4.4 Operating in the open-loop control mode

To operate the NPC2 inverter in the open-loop mode, set the Control mode to ‘Open loop’. Do not operate the inverter outside the specified voltages, current, and frequencies in the open-loop mode. The inverter has been

tested only for the specifications listed in Table 2. Performance outside these specifications is not guaranteed. The firmware offers the possibility of increasing the DC-link voltage gradually, monitor it, and then decide to use it if required.

Steps to operate in the open-loop control mode are as follows:

1. Set the control mode to Open loop.
2. Adjust the Modulation index (MI) in the GUI. Set the modulation index value according to the DC bus and the output voltage values. For example, if the DC bus is 750 V and the V_{ac} is 220 Vrms, the MI will be 0.87.
3. Click Start to start the operation.
4. Provide the required supply and load to the converter.
5. Adjust the MI value accordingly.
6. Click Stop to stop the converter.

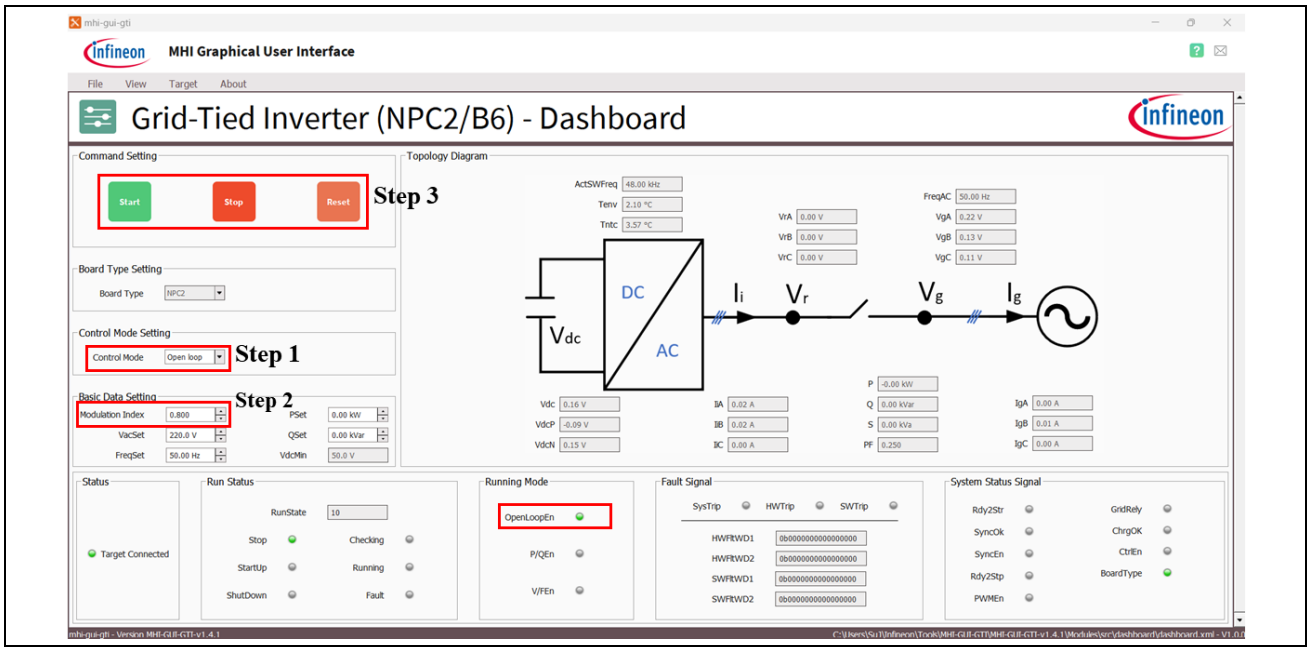


Figure 73 **Operating in the open-loop control mode**

The minimum DC voltage is 50 V. Set the DC source voltage between 50 V and 950 V and ensure that the inverter is in the Rdy2str state before clicking Stop. Then you can do the testing. Otherwise, please check the DC voltage, the board type, and reset the system.

4.5 Operating in the V/F control mode

To operate the NPC2 inverter in the V/F control mode, set the Control mode to 'V/F'. Ensure that the AC-output terminals are connected to the AC load and the DC-input terminals are connected to the DC source.

Steps to operate in the V/F control mode are as follows:

1. Set the control mode to V/F.
2. Set the AC output voltage and frequency. For example, set VacSet to 220 V_{rms} and FreqSet to 50 Hz.

3. Click Start to start the operation.
4. Provide the supply and load required to the converter.
5. Adjust the VacSet and FreqSet value accordingly.
6. Click Stop to stop the converter.

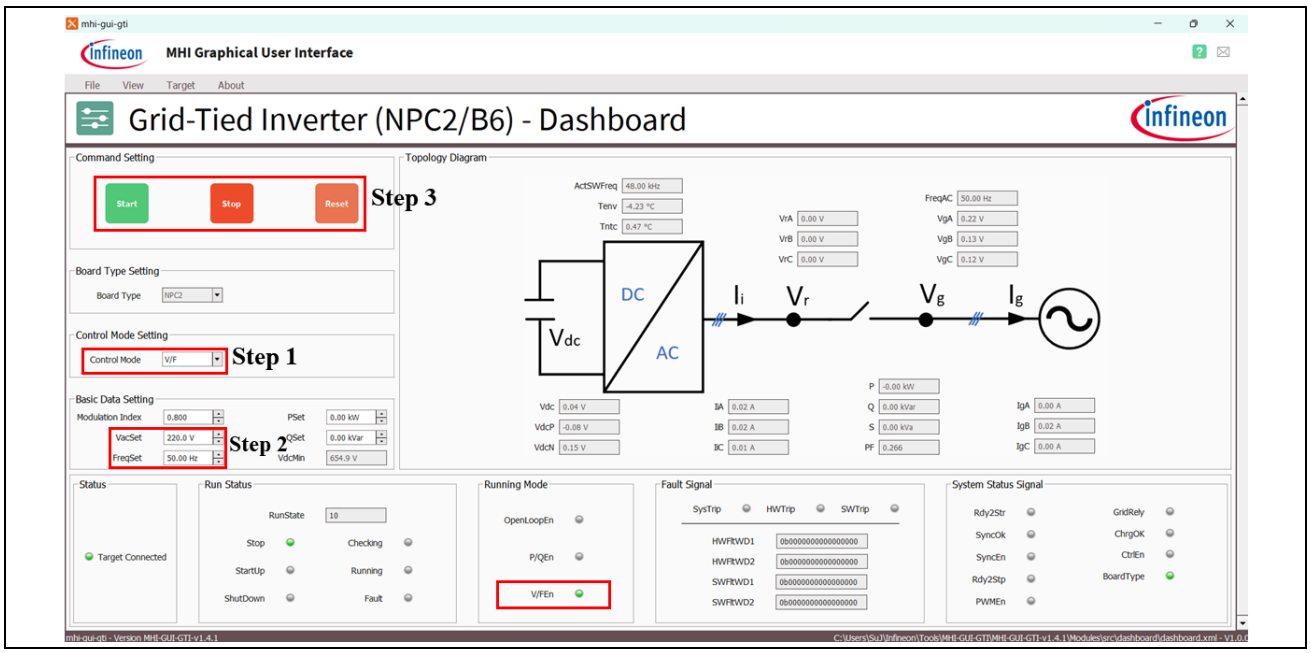


Figure 74 **Operating in the V/F control mode**

1. *Note: The maximum power limit is 12 kVA. If the output power is more than 1.2 pu and lasts for 60 seconds, it can trigger the overload fault.*
2. *According to the B/S, the PF is between 1~±0.8. Please be careful when setting the AC load.*

4.6 Operating in the P/Q control mode

To operate the NPC2 inverter in the P/Q control mode, set the Control mode to 'P/Q'. Ensure that the AC-output terminals are connected to the grid simulator and the DC-input terminals are connected to the DC source.

Steps to operate in the P/Q control mode are as follows:

1. Set the control mode to P/Q.
2. Set the active power (PSet) or reactive power (QSet).
3. Click Start to start the operation.
4. Provide the supply and load required to the converter.
5. Adjust the PSet and QSet value accordingly.
6. Click Stop to stop the converter.

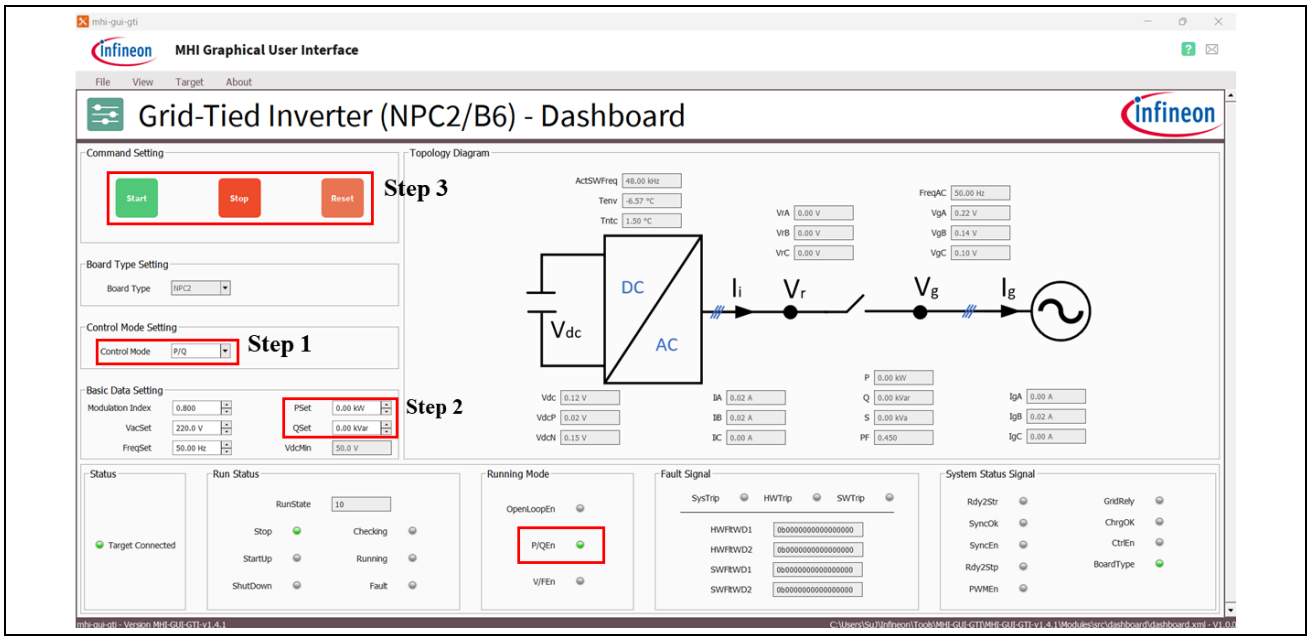


Figure 75 **Operating in the P/Q control mode**

The output power rating in the Topology diagram depends on the PSet. The value of PSet can be positive or negative. A positive value means that the converter is in the inverter mode, a negative value means that the converter is in the rectification mode.

4.7 Safe power down

The safe power down procedure for a 10 kW NPC2 inverter platform is crucial to prevent electrical hazards, protect components from damage, and ensure operational reliability. The safe power down sequence must adapt to the differences in the control modes to ensure safety and protect the component.

For the open-loop and V/F control modes, follow these steps:

1. Click Stop to stop the converter.
2. Stop the output of AC load.
3. Turn off the high-voltage DC source.
4. Turn off the external 24 V_{dc}.

For the P/Q control mode, follow these steps:

1. Click Stop in the GUI to stop the converter.
2. Turn off the grid simulator.
3. Turn off the high-voltage DC source.
4. Turn off the external 24 V_{dc}.

5 Performance and test results

5.1 Open-loop test results

5.1.1 Overcurrent protection

The output current was increased until the overcurrent protection reacted. GK tripped when the peak current reached 38 A.

Legend: CH1: IA, CH2: IB, CH4: IC, CH3: VGS-A-S3, CH7: VGS-A-S1, CH8: GK

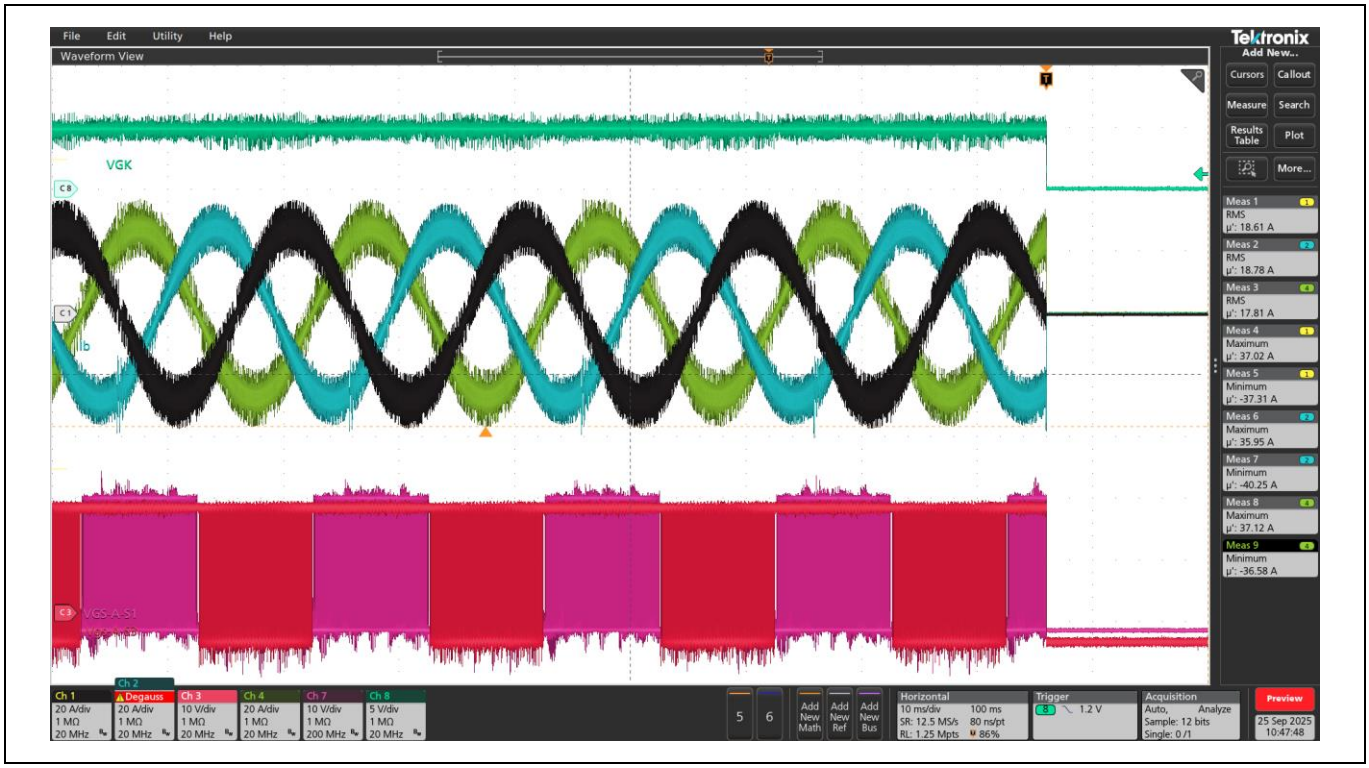


Figure 76 **Overcurrent protection**

5.1.2 Overvoltage protection

The bus voltage was increased until the overvoltage protection reacted. GK1 tripped when the bus voltage reached 890V.

Legend: CH3: VGS-A-S1, CH7: VGS-A-S3, CH8: GK, CH6: VBUS

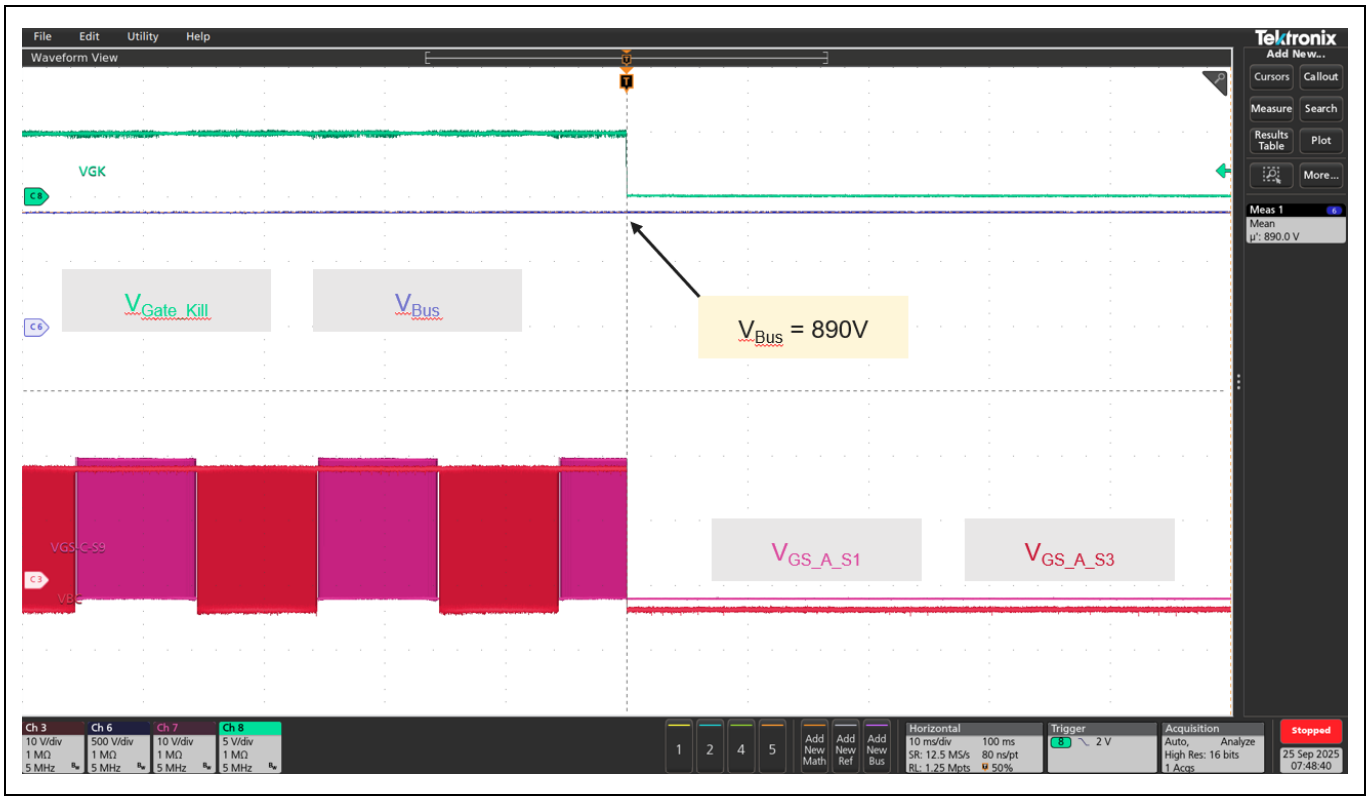


Figure 77 **Overvoltage protection**

5.1.3 Overtemperature protection

5.1.3.1 Overtemperature protection – T_c

The case temperature T_c was increased until the overtemperature protection reacted. All of the V_{gs} values were pulled down when T_c was 100.32℃ and V_{ntc} was 1.488 V.

Legend: CH1: Vntc, CH3: VGS-A-S4, CH6: VGS-A-S1, CH8: VGK

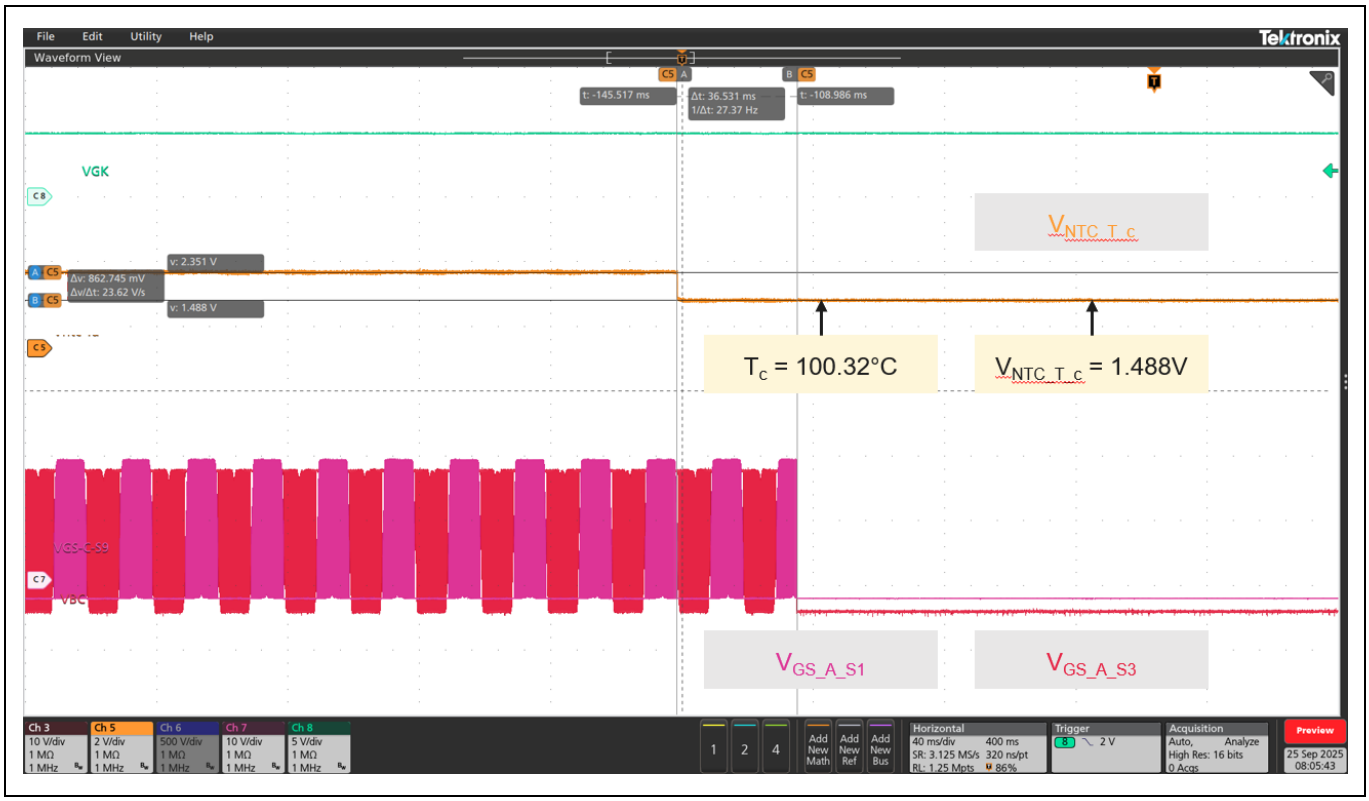


Figure 78 **Overtemperature protection-T_c**

5.1.3.2 Overtemperature protection – T_a

The ambient temperature T_a was increased until the overtemperature protection reacted. All of the V_{gs} were pulled down when T_a was 62.23°C and V_{ntc} was 2.77 V.

Legend: CH1: Vntc, CH3: VGS-A-S4, CH6: VGS-A-S1, CH8: VGK

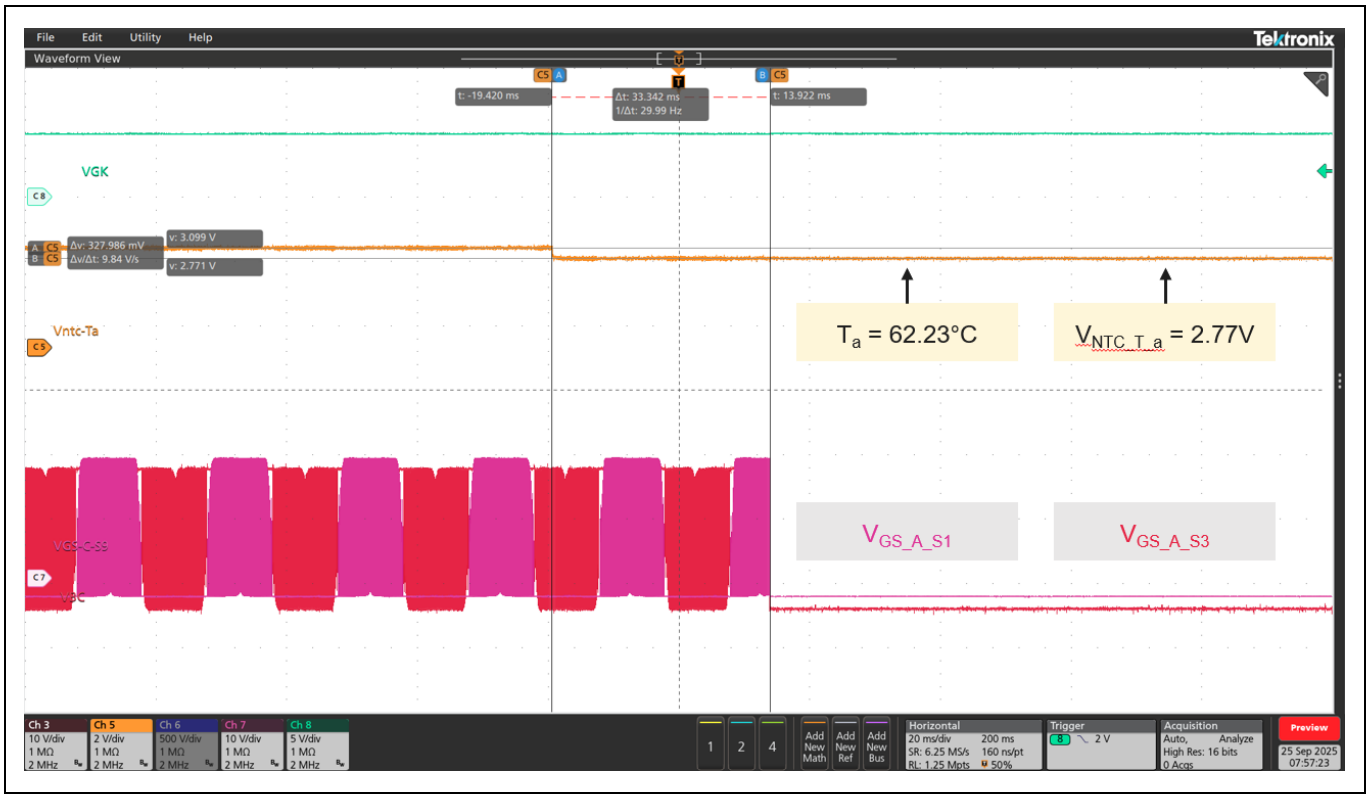


Figure 79 **Overtemperature protection – Ta**

5.2 Closed-loop test results

5.2.1 Output AC voltage against different DC input voltages (V/F & P/Q)

The design was tested with three different input DC voltages – 660 V, 750 V, and 850 V; and two control modes – V/F and P/Q. The output line-to-line rms voltage was kept at around 400 V at 10 kW power.

Table 9 DC input voltage range

Input voltage	660, 750, and 850 V_{dc}
PWM	SPWM, 48 kHz
Output power	10 kW, V_{out} = 400 $V_{l\text{-}l\ rms}$/50 Hz

Table 10 V/F mode test data

Control mode	Input voltage (V_{dc})	Input power (kW)	Output voltage ($V_{l\text{-}l\ rms}$)			Output current (A_{rms})			Waveform
			V_{ab}	V_{bc}	V_{ca}	I_a	I_b	I_c	
V/F	660	10	398.8	399.3	398.6	14.37	14.29	14.36	Figure 80
V/F	750	10	399.0	399.2	398.6	14.36	14.28	14.35	Figure 81
V/F	850	10	399.1	399.0	398.6	14.37	14.28	14.34	Figure 82
Legend	CH1: Vl-l ab, CH2: Vl-l bc, CH3: Vl-l ca, CH4: Ib, CH5: Ia, CH7: Ic, CH6: Vbus								

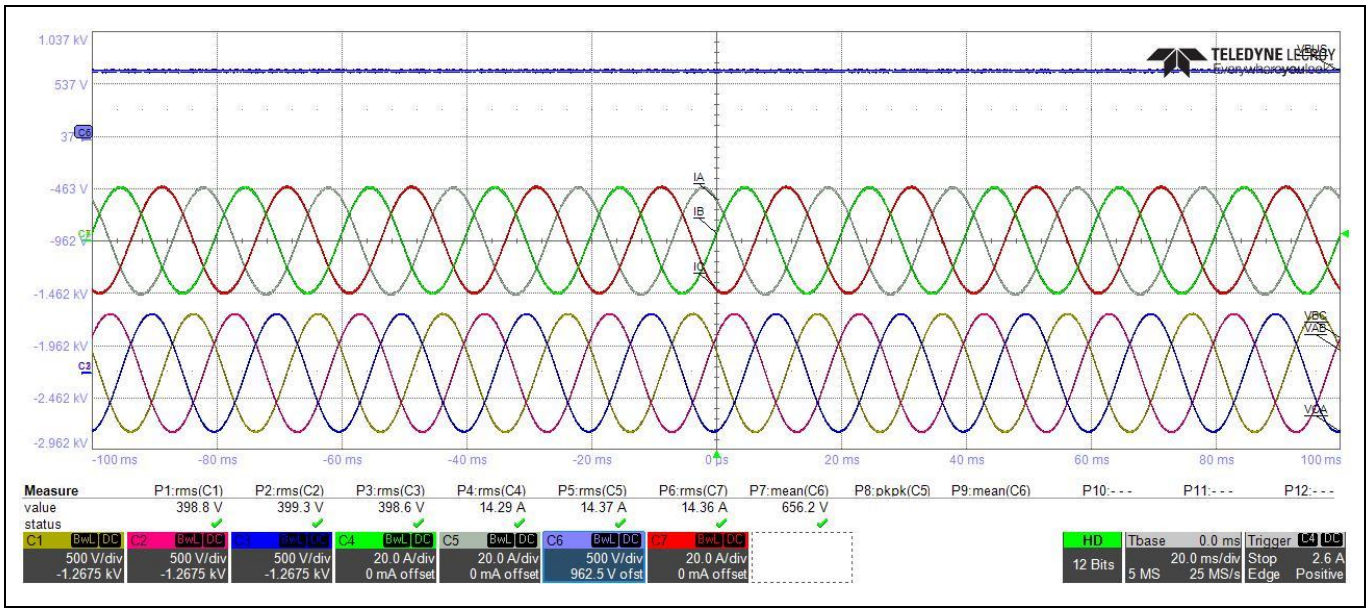


Figure 80 **660 V_{dc} in V/F mode**

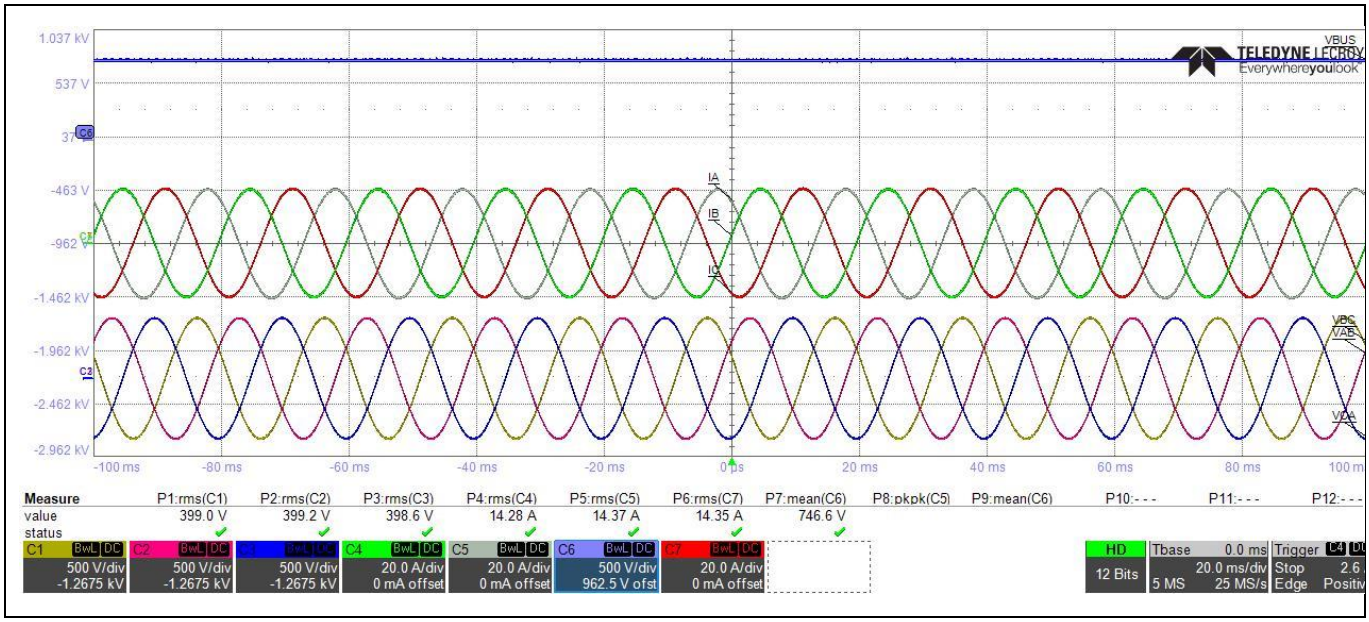


Figure 81 **750 V_{dc} in V/F mode**

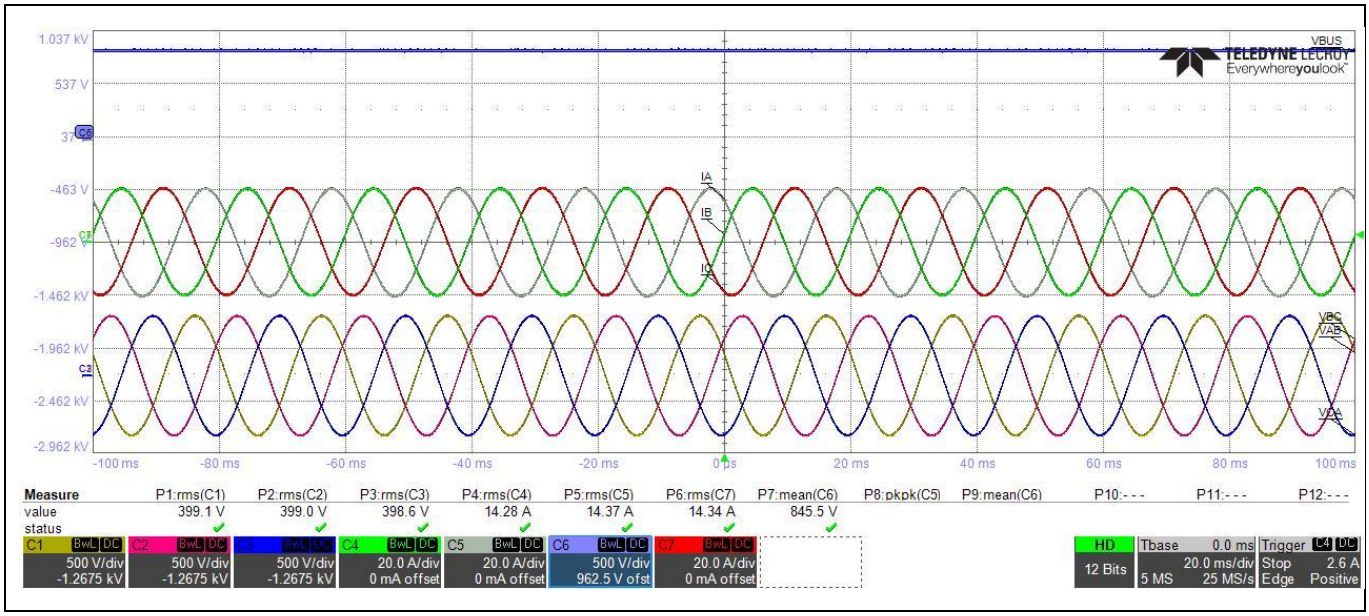


Figure 82 **850 V_{dc} in V/F mode**

Table 11 P/Q mode test data

Control mode	Input voltage (V_{dc})	Input Power (kW)	Output Voltage ($V_{l\text{-}l\ rms}$)			Output Current (A_{rms})			Waveform
			V_{ab}	V_{bc}	V_{ca}	I_a	I_b	I_c	
P/Q	660	10	398.7	398.1	397.5	14.63	14.60	14.64	Figure 83
P/Q	750	10	398.6	398.2	397.7	14.66	14.62	14.64	Figure 84
P/Q	850	10	398.8	398.1	397.6	14.67	14.63	14.63	Figure 85
Legend	CH1: Vl-l ab, CH2: Vl-l bc, CH3: Vl-l ca, CH4: Ib , CH5: Ia, CH7: Ic, CH6: Vbus								

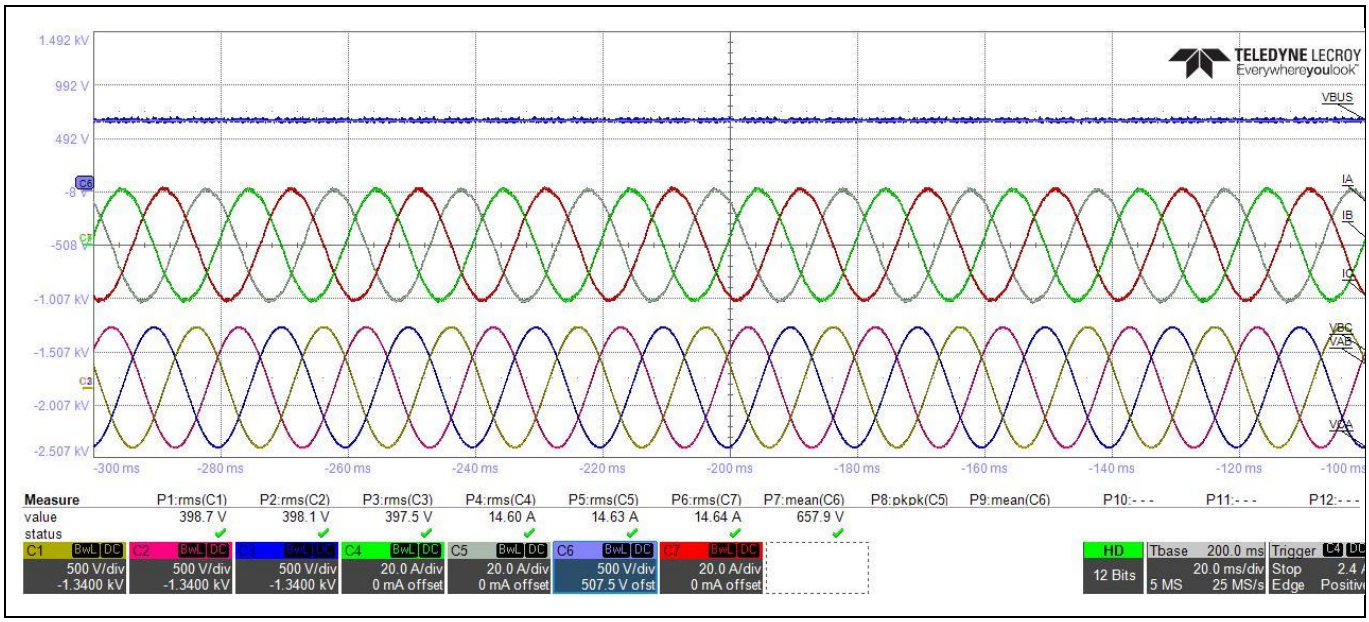


Figure 83 **660 V_{dc} in P/Q mode**

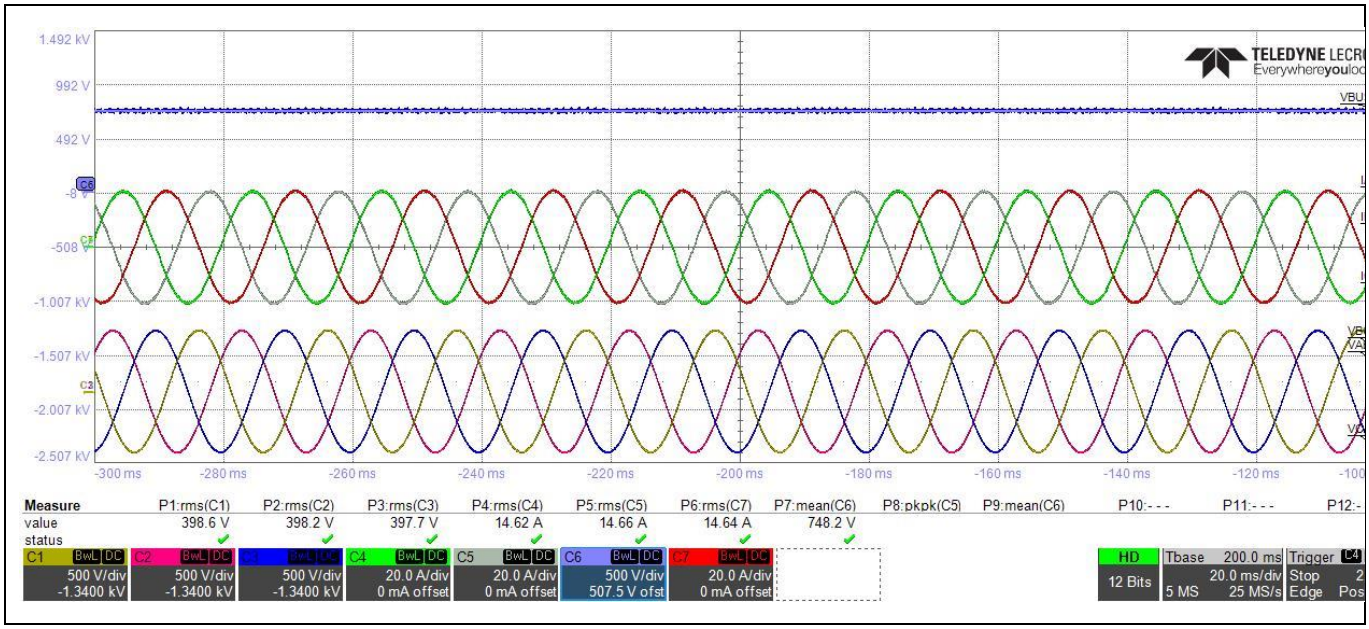


Figure 84 **750 V_{dc} in P/Q mode**

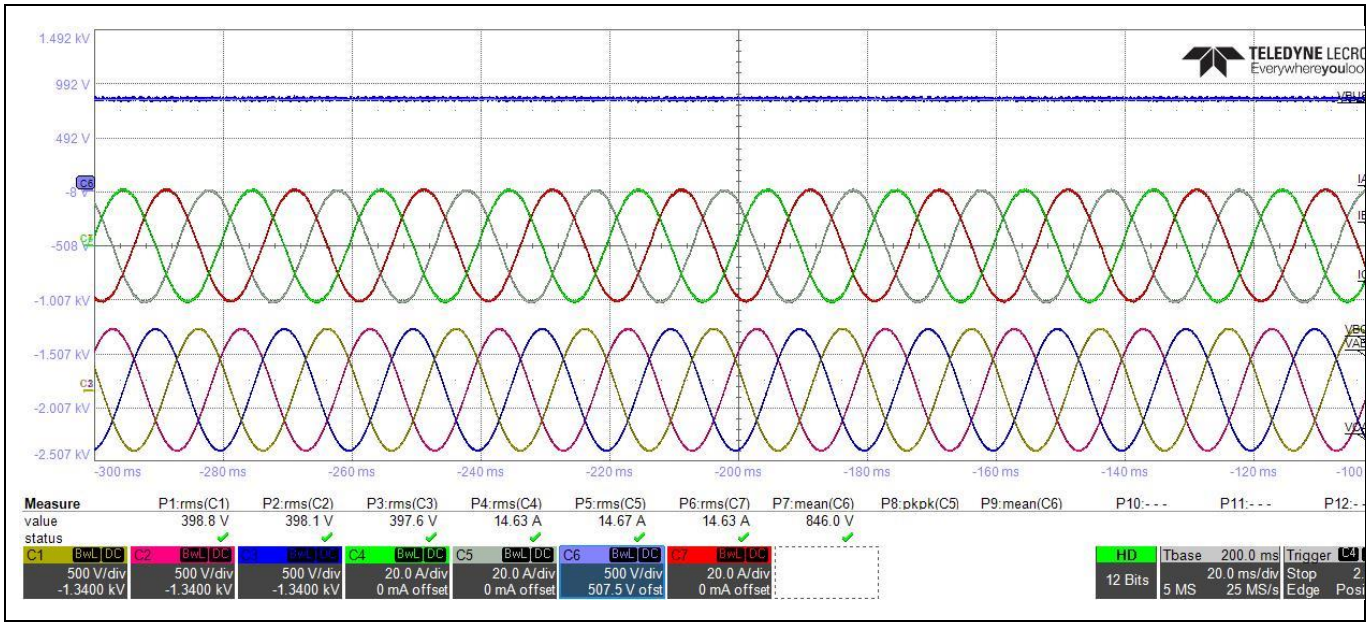


Figure 85 **850 V_{dc} in P/Q mode**

5.2.2 Output current ripple and voltage ripple

The design was tested with an input DC voltage of 750 V and two control modes – V/F and P/Q. The output line-to-line voltage and output current were measured before the LCL filter at 10 kW power.

Table 12 P/Q mode test data

Input voltage	750 V_{dc}
PWM	SPWM, 48 kHz
Output power	10 kW, V_{out} = 400 $V_{l\text{-}l\ rms}$, 50 Hz
Output voltage ripple V_{ab} ($V_{l\text{-}l\ rms}$)	398 V
Output current ripple I_b (A_{rms})	2.14 A
Waveform	Figure 86 & 87

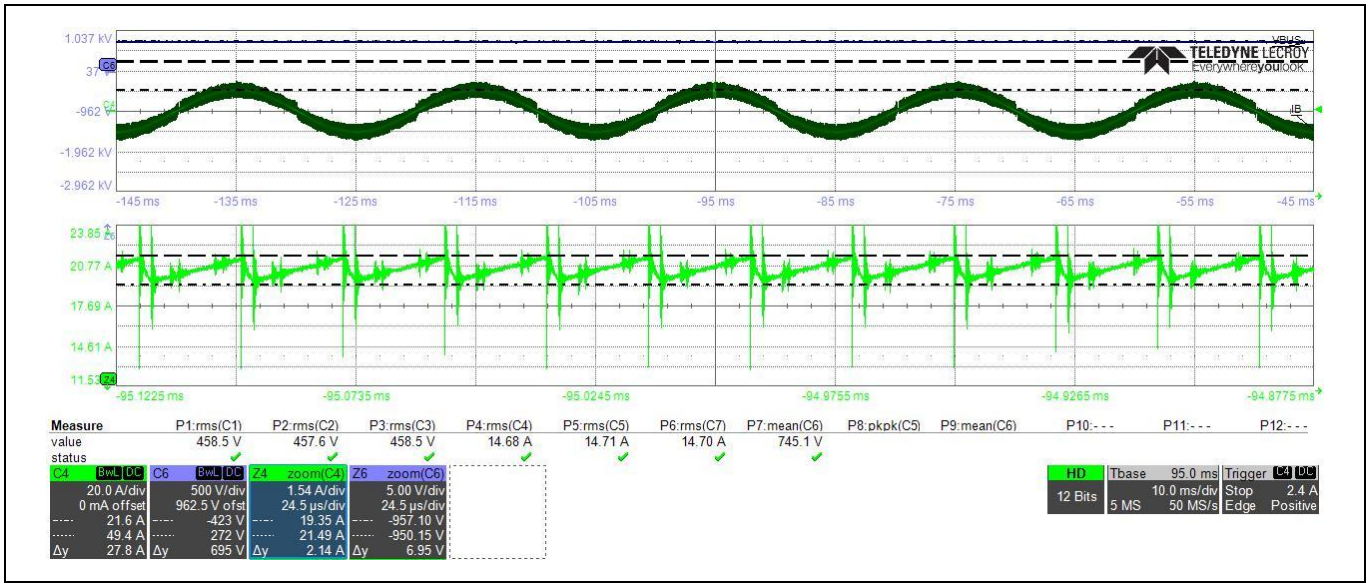


Figure 86 **Output current ripple in P/Q mode**

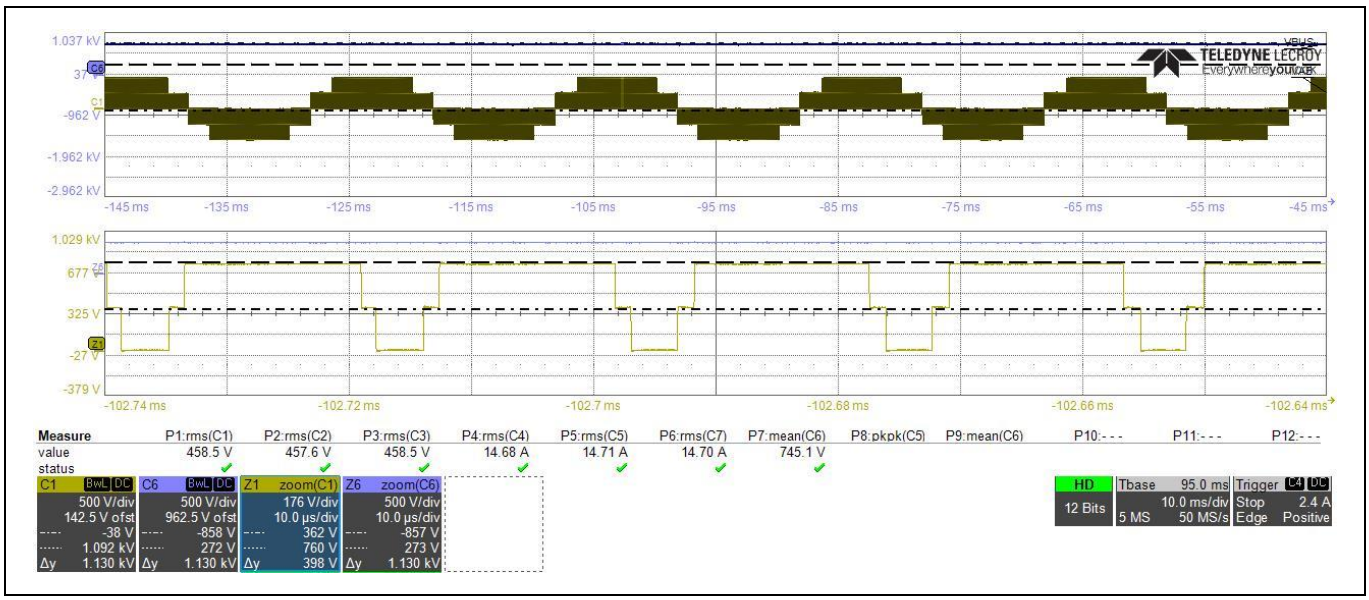


Figure 87 **Output voltage ripple in P/Q mode**

Table 13 V/F mode test data

Input voltage	750 V_{dc}
PWM	SPWM, 48 kHz
Output power	10 kW, V_{out} = 400 $V_{l\text{-}l\ rms}$, 50 Hz
Output voltage ripple V_{ab} ($V_{l\text{-}l\ rms}$)	390 V
Output current ripple I_b (A_{rms})	2.29 A
Waveform	Figure 88 & 89

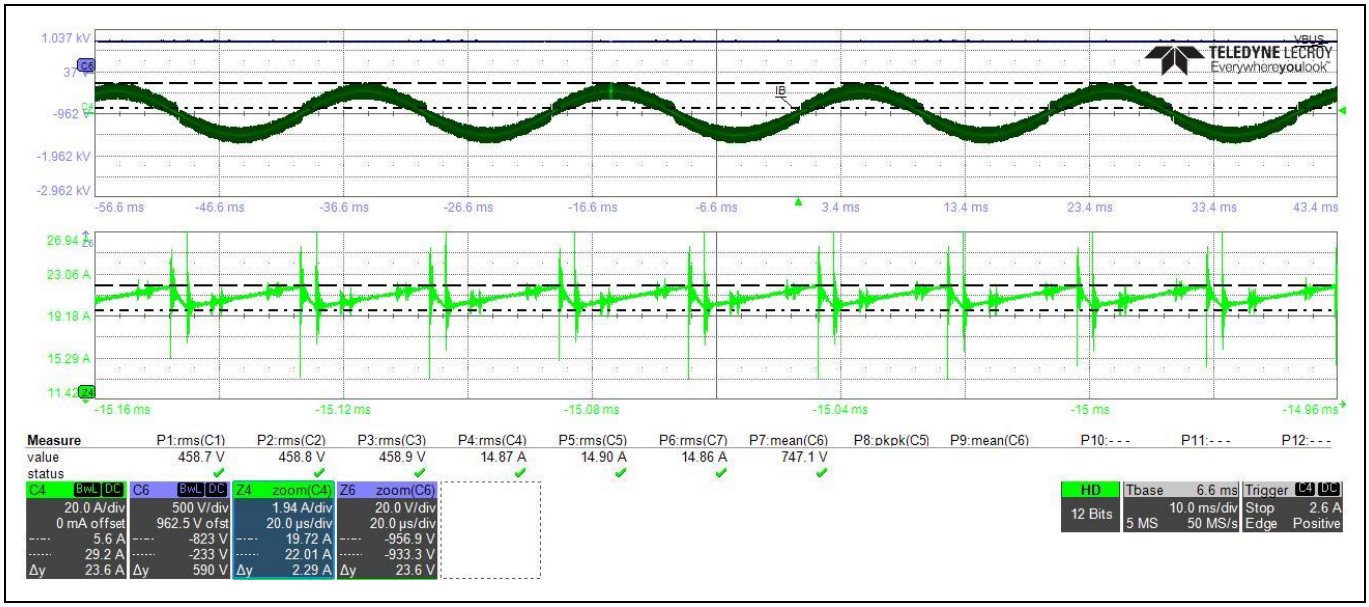


Figure 88 **Output current ripple in V/F mode**

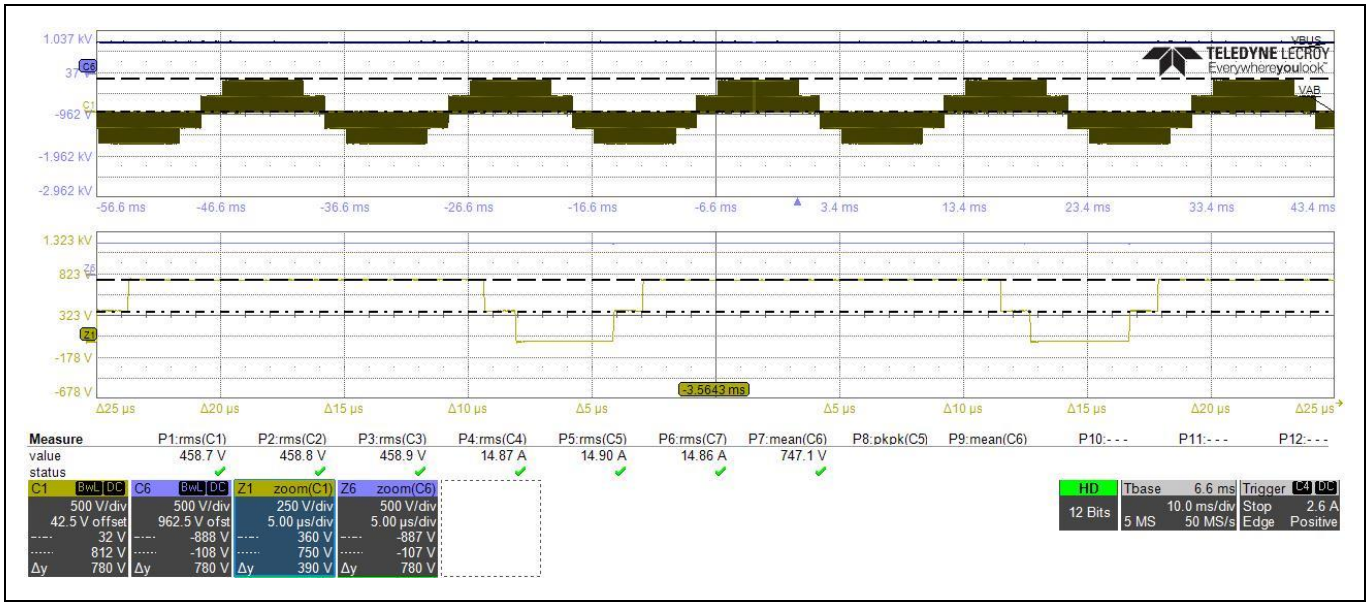


Figure 89 **Output voltage ripple in V/F mode**

5.2.3 Power derating at higher ambient temperature

When the ambient temperature T_a reaches 43.86°C, the output power starts getting derated.

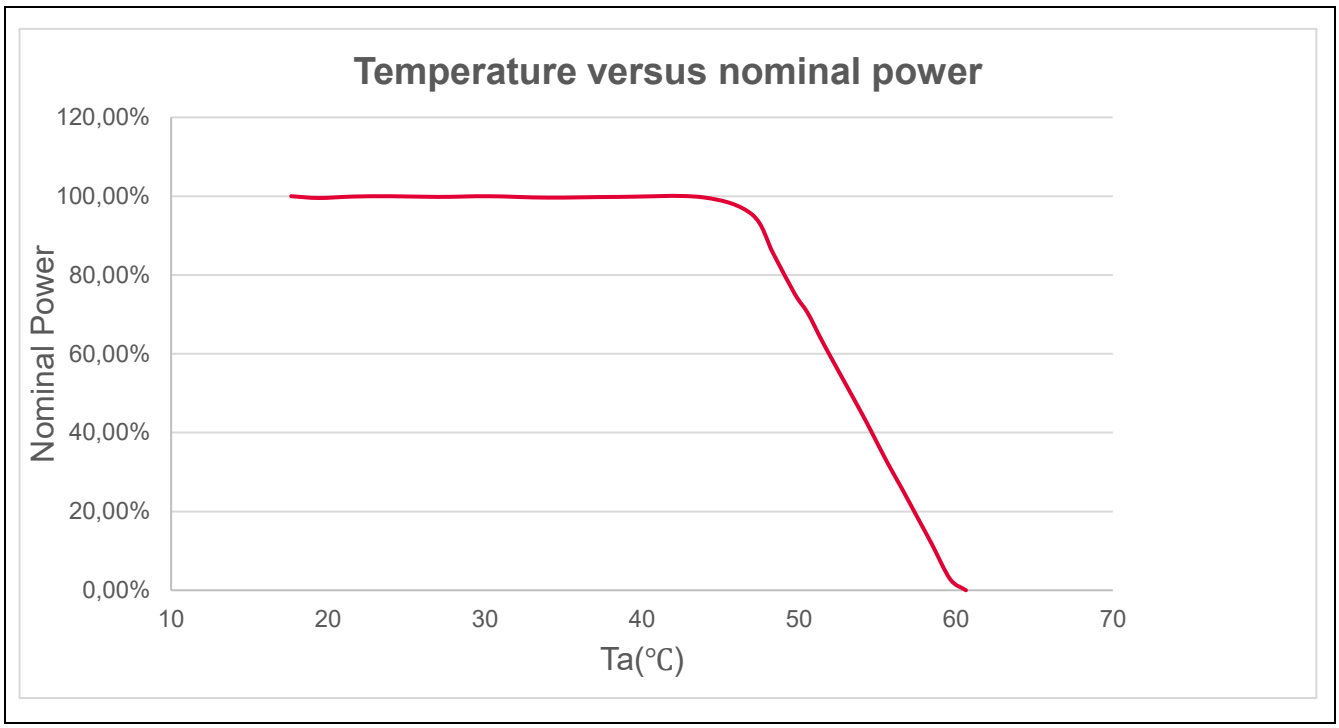


Figure 90 **Power derating curve with ambient temperature**

5.2.4 Measuring the DC voltage

The design was tested to evaluate the balancing performance of the DC bus voltage with 750 V input DC voltage and two control modes – V/F and P/Q – at 10 kW power.

Table 14 P/Q mode test data

Input voltage	750 V_{dc}
PWM	SPWM, 48 kHz
Output power	10 kW, V_{out} = 400 $V_{l\text{-}l\ rms}$, 50 Hz
Half-bus voltage VDC+	371.8 V
Half-bus voltage VDC-	375.4 V
Waveform	Figure 91

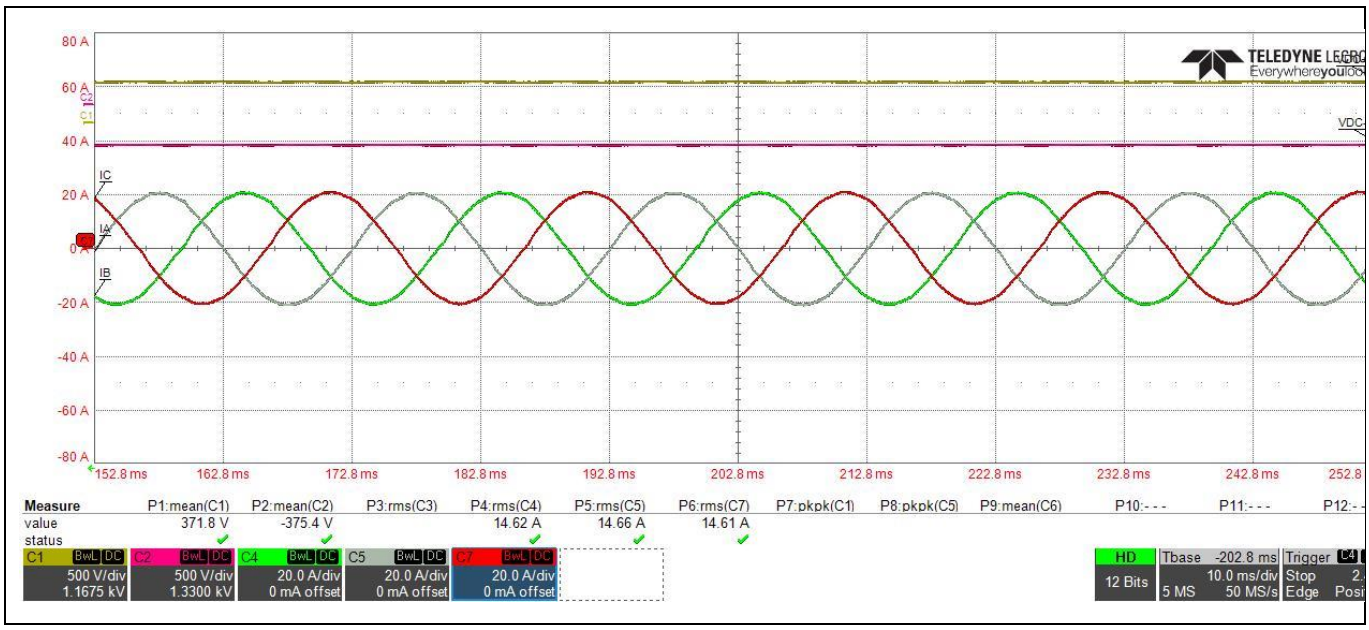


Figure 91 **DC voltage measurement in P/Q mode**

Table 15 V/F mode test data

Input voltage	750 V_{dc}
PWM	SPWM, 48 kHz
Output power	10 kW, V_{out} = 400 $V_{l\text{-}l\ rms}$, 50 Hz
Half-bus voltage VDC+	375.0 V
Half-bus voltage VDC-	374.8 V
Waveform	Figure 92

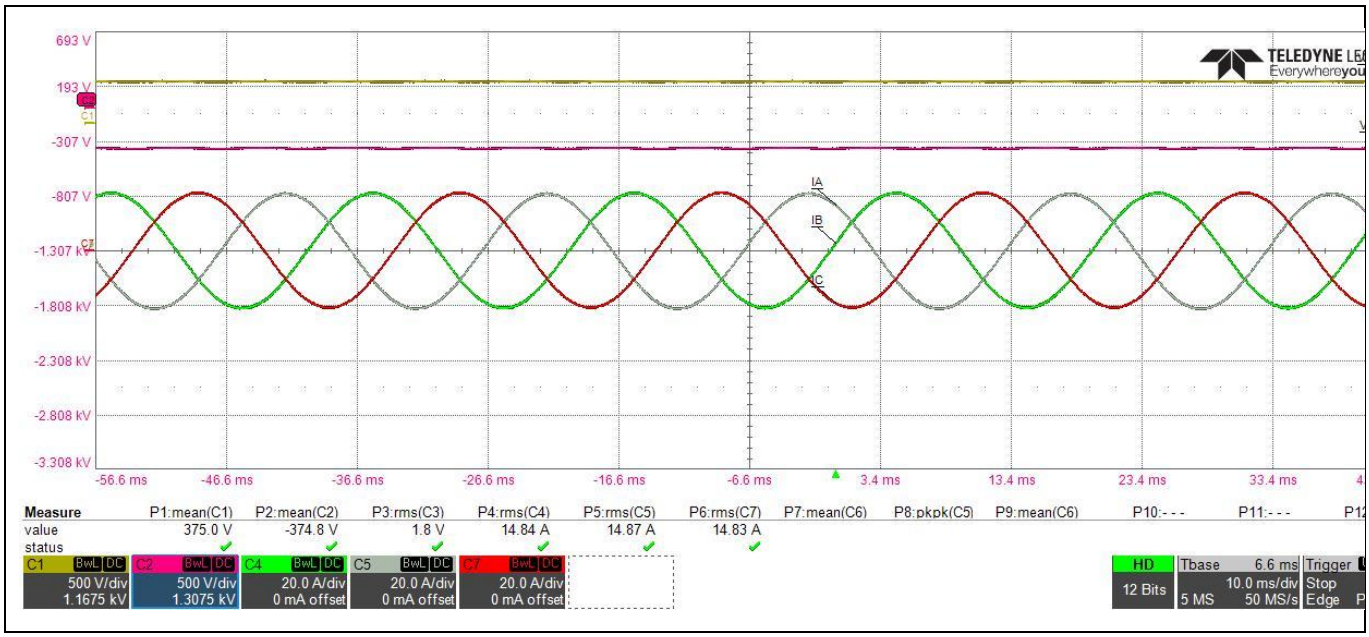


Figure 92 **DC voltage measurement in V/F mode**

5.2.5 Synchronizing the grid

At startup, VNAB gradually follows the grid voltage and eventually reaches a matching waveform.

Legend: CH1: VAB, CH2: VBC, CH3: VCA, CH4: IB, CH5: IC, CH6: VNAB, CH7: IC

Table 16 Test Conditions

Input voltage	750 V_{dc}
Control mode	P/Q mode
PWM	SPWM, 48 kHz
Output power	10 kW, V_{out} = 400 $V_{l\text{-}l\ rms}$/50 Hz

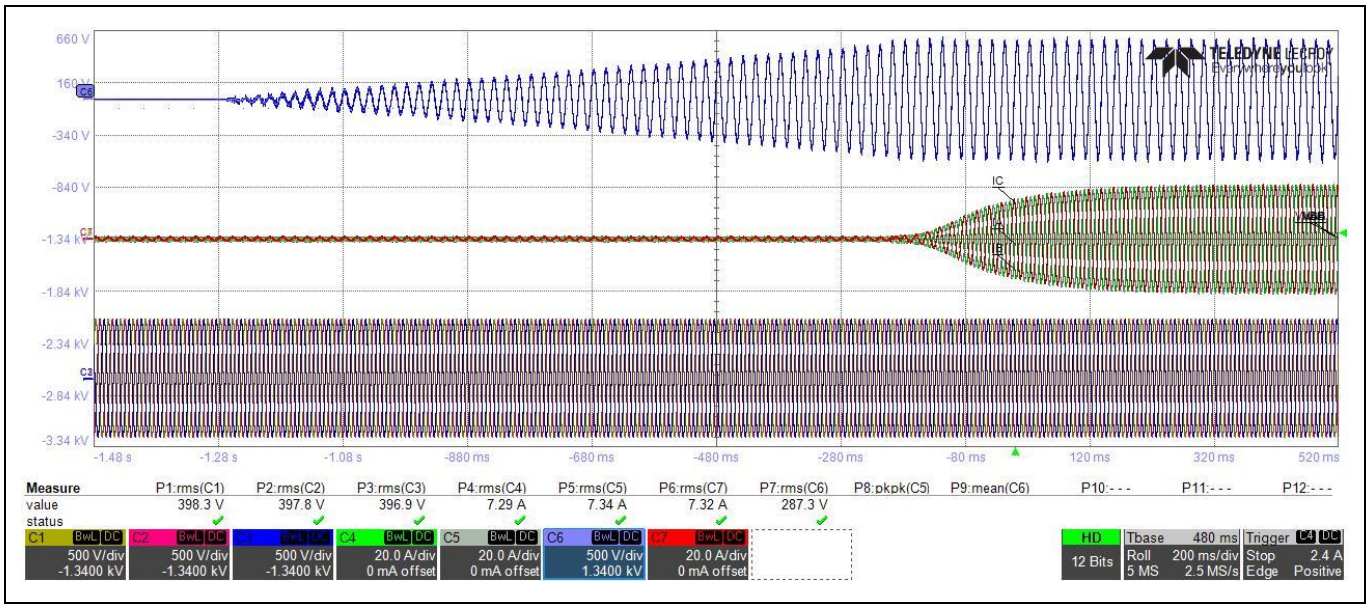


Figure 93 **Grid synchronization in P/Q mode**

5.2.6 Grid undervoltage protection

The grid undervoltage protection is triggered if the grid voltage drops to 64.7% (258 V/399 V) of the rated value and all the V_{gs} values are pulled down.

Legend: CH1: PWM-IN-A-S4, CH2: VBC, CH3: VAB, CH5: VCA, CH6: PWM-IN-A-S1

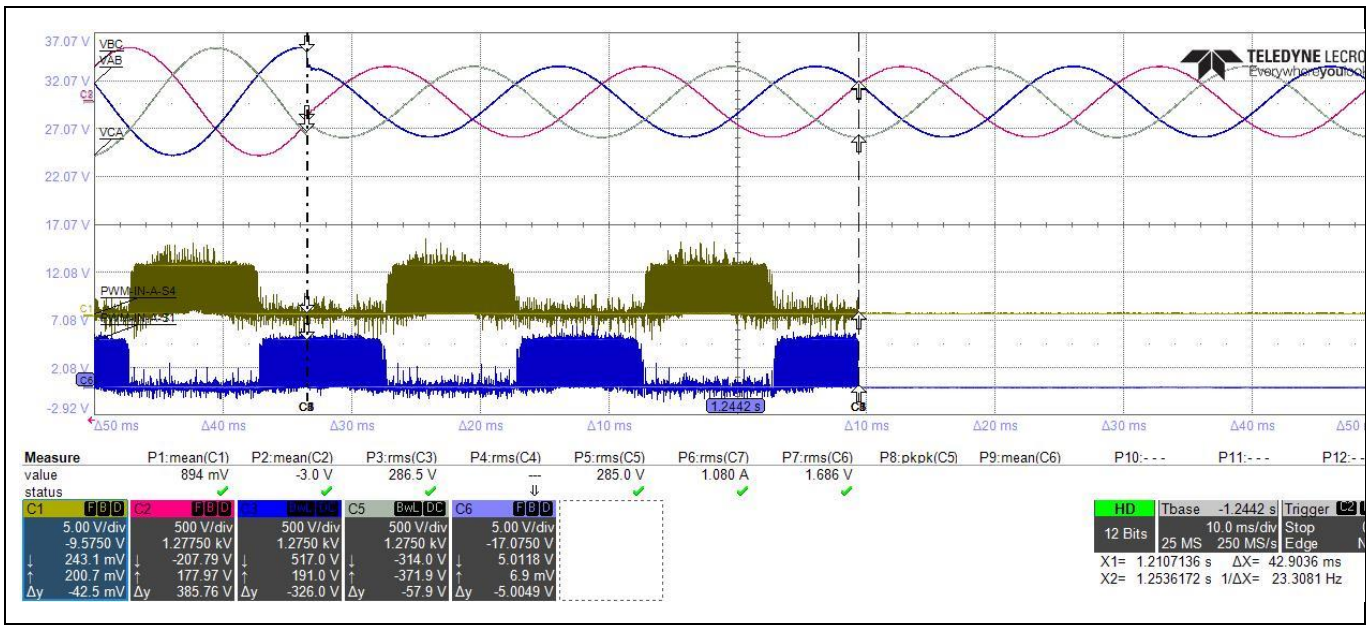


Figure 94 **Grid undervoltage protection**

5.2.7 Measuring the Total Harmonic Distortion

Table 17 THD measurement of power semiconductors in V/F mode

Specification	Measuring THD using the Yokogawa WT1800 precision power analyzer		
Control mode	V/F mode		
PWM	SPWM, 48 kHz		
Output power	10 kW, V_{out} = 400 $V_{l\text{-}l\ rms}$/50 Hz		
THD	**Uthd1**	**Ithd1**	**Pthd1**
V_{dc} = 660 V	0.408%	0.419%	0.002%
V_{dc} = 750 V	0.313%	0.330%	0.001%
V_{dc} = 850 V	0.360%	0.369%	0.001%

Table 18 THD measurement of power semiconductors in P/Q mode

Specification	Measuring THD using the Yokogawa WT1800 precision power analyzer		
Control mode	P/Q mode		
PWM	SPWM, 48 kHz		
Output power	10 kW, V_{out} = 400 $V_{l\text{-}l\ rms}$/50 Hz		
THD	**Uthd1**	**Ithd1**	**Pthd1**
V_{dc} = 660 V	0.141%	1.263%	0.000%
V_{dc} = 750 V	0.119%	1.068%	0.000%
V_{dc} = 850 V	0.132%	1.108%	0.000%

5.2.8 Efficiency measurement

Table 19 Efficiency measurement of power semiconductors in V/F mode

Specification	Measuring efficiency using the Yokogawa WT1800 precision power analyzer
Condition	V_{dc} = 660 V, V_{out} = 400 $V_{l\text{-}l\ rms}$/50 Hz, V/F mode Measurements are taken after the LCL filter (power losses with filter)

Operation	Efficiency
1.2 kW	98.775%
2.4 kW	99.165%
3.0 kW	99.208%
4.2 kW	99.296%
5.4 kW	99.264%
6.0 kW	99.233%
7.2 kW	99.178%
8.4 kW	99.107%
9.0 kW	99.068%
10.2 kW	98.978%

Table 20 Power semiconductors efficiency measurement in V/F mode

Specification	Measuring efficiency using the Yokogawa WT1800 precision power analyzer
Condition	V_{dc} = 750 V, V_{out} = 400 $V_{l\text{-}l\ rms}$/50 Hz, V/F mode Measurements are taken after the LCL filter (power losses with filter)

Operation	Efficiency
1.2 kW	98.348%
2.4 kW	98.900%
3.0 kW	98.991%
4.2 kW	99.121%
5.4 kW	99.110%
6.0 kW	99.092%
7.2 kW	99.041%
8.4 kW	98.971%
9.0 kW	98.930%
10.2 kW	98.847%

Table 21 Power semiconductors efficiency measurement in V/F mode

Specification	Measuring efficiency using the Yokogawa WT1800 precision power analyzer
Condition	V_{dc} = 850 V, V_{out} = 400 $V_{l\text{-}l\ rms}$/50 Hz, V/F mode Measurements are taken after the LCL filter (power losses with filter)

Operation	Efficiency
1.2 kW	97.867%
2.4 kW	98.641%
3.0 kW	98.775%
4.2 kW	98.886%
5.4 kW	98.955%
6.0 kW	98.940%
7.2 kW	98.896%
8.4 kW	98.830%
9.0 kW	98.787%
10.2 kW	98.702%

Table 22 Power semiconductors efficiency measurement in P/Q mode

Specification	Measuring efficiency using the Yokogawa WT1800 precision power analyzer
Condition	V_{dc} = 660 V, V_{out} = 400 $V_{l\text{-}l\ rms}$/50 Hz, P/Q mode Measurements are taken after the LCL filter (power losses with filter)

Operation	Efficiency
1.0 kW	98.481%
2.0 kW	99.051%
3.0 kW	99.210%
4.0 kW	99.303%
5.0 kW	99.297%
6.0 kW	99.262%
7.0 kW	99.223%
8.0 kW	99.185%
9.0 kW	99.127%
10.0 kW	99.070%

Table 23 Power semiconductors efficiency measurement in P/Q mode

Specification	Measuring efficiency using the Yokogawa WT1800 precision power analyzer
Condition	V_{dc} = 750 V, V_{out} = 400 $V_{l\text{-}l\ rms}$/50 Hz, P/Q mode Measurements are taken after the LCL filter (power losses with filter)

Operation	Efficiency
1.0 kW	97.969%
2.0 kW	98.724%
3.0 kW	99.036%
4.0 kW	99.108%
5.0 kW	99.171%
6.0 kW	99.147%
7.0 kW	99.098%
8.0 kW	99.044%
9.0 kW	98.987%
10.0 kW	98.921%

Table 24 Power semiconductors efficiency measurement in P/Q mode

Specification	Measuring efficiency using the Yokogawa WT1800 precision power analyzer
Condition	V_{dc} = 850 V, V_{out} = 400 $V_{l\text{-}l\ rms}$/50 Hz, P/Q mode Measurements are taken after the LCL filter (power losses with filter)

Operation	Efficiency
1.0 kW	97.366%
2.0 kW	98.402%
3.0 kW	98.743%
4.0 kW	98.861%
5.0 kW	98.962%
6.0 kW	98.956%
7.0 kW	98.928%
8.0 kW	98.889%
9.0 kW	98.839%
10.0 kW	98.780%

6 Board layout

6.1 REF-10KW3LNPC2Q_MB

Table 25 Mechanical data

Dimensions	420 mm x 260 mm
No. of layers	4
Copper thickness	70 µm
Weight	8.7 kg

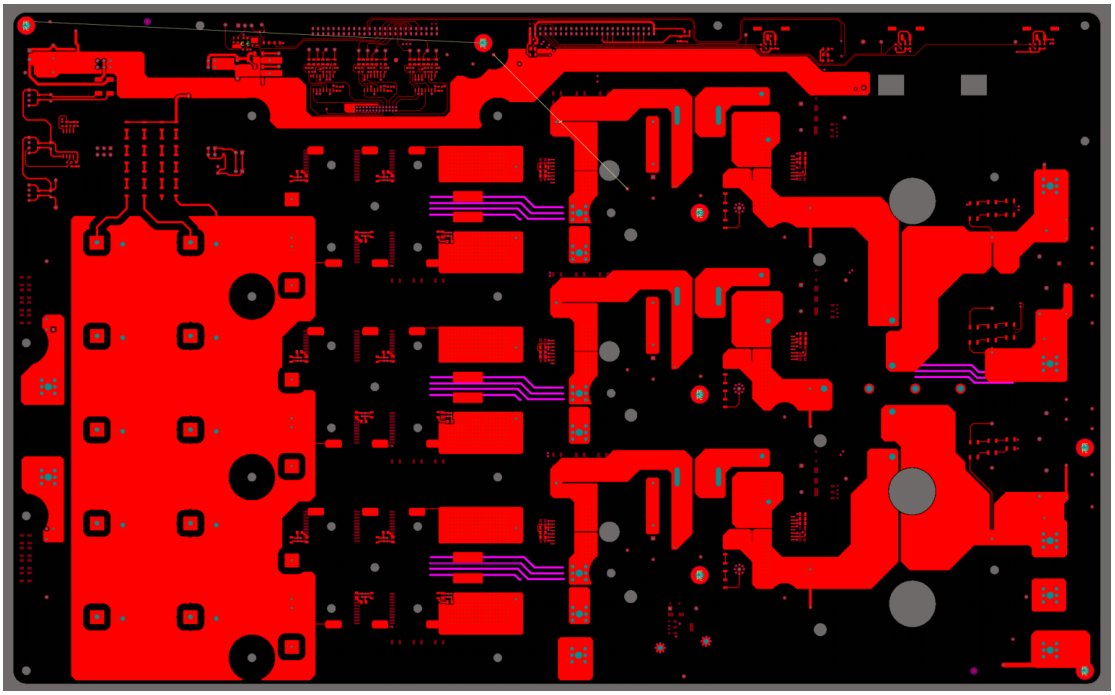


Figure 95 **Layer 1**

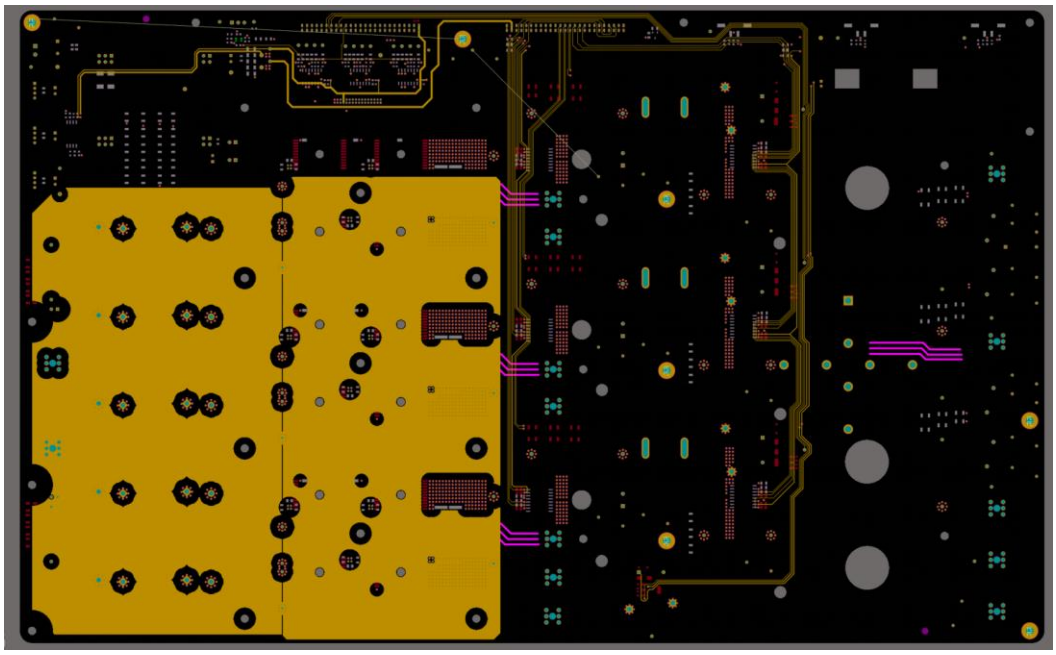


Figure 96 **Layer 2**

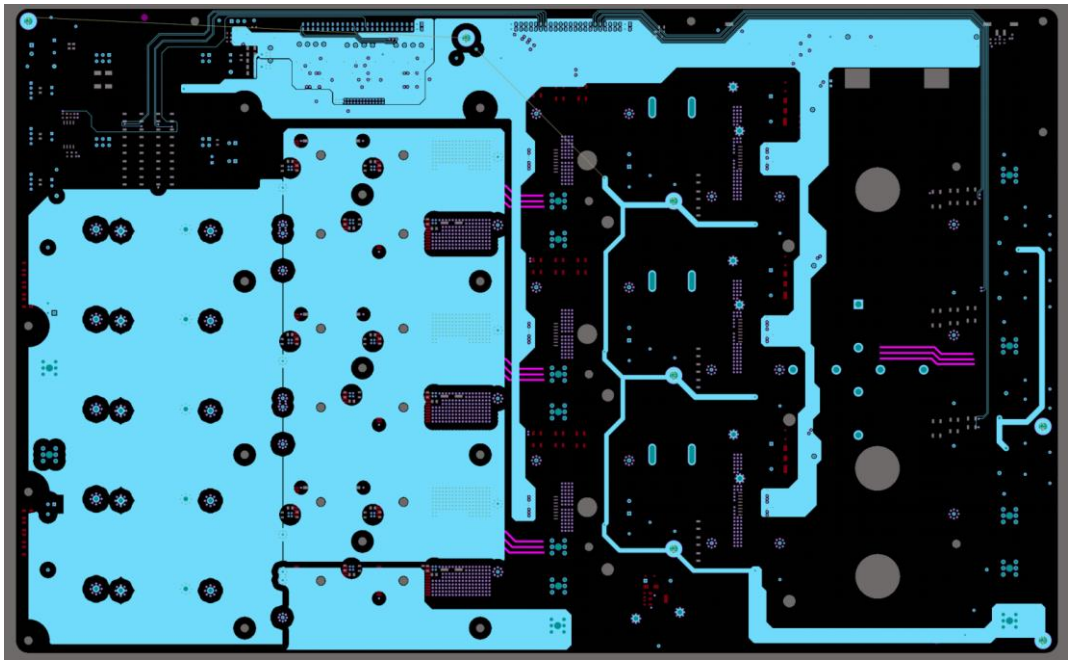


Figure 97 **Layer 3**

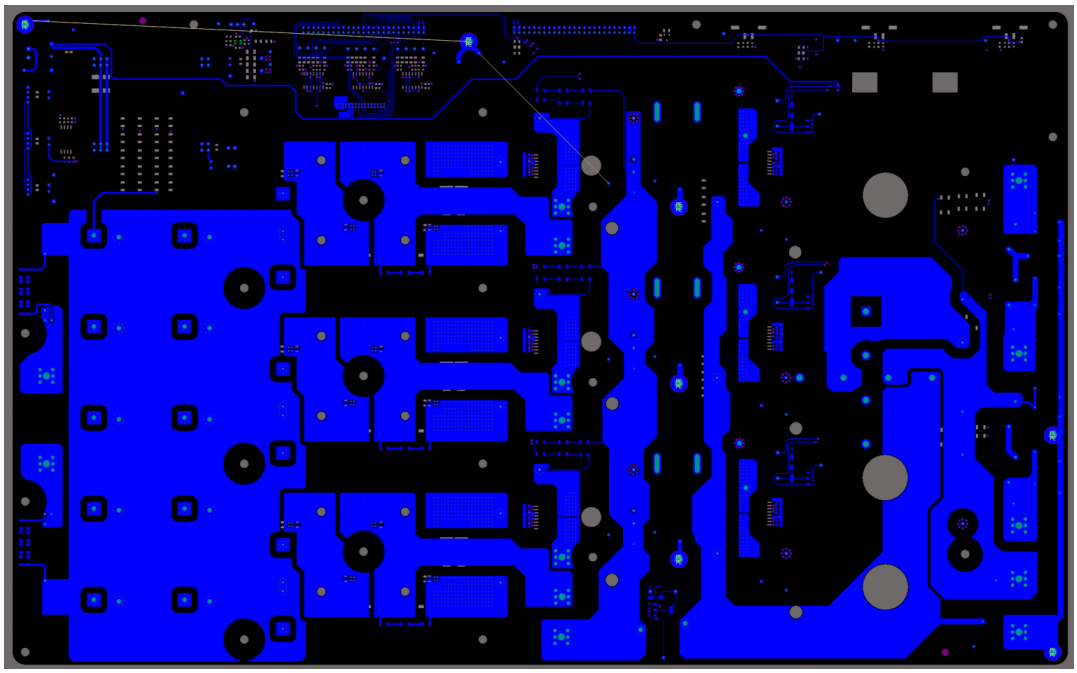


Figure 98 **Layer 4**

6.2 REF-10KW3LNPC2Q_GDB

Table 26 Mechanical data

Dimensions	222 mm x 95 mm
No. of layers	2
Copper thickness	35 µm
Weight	0.2 kg

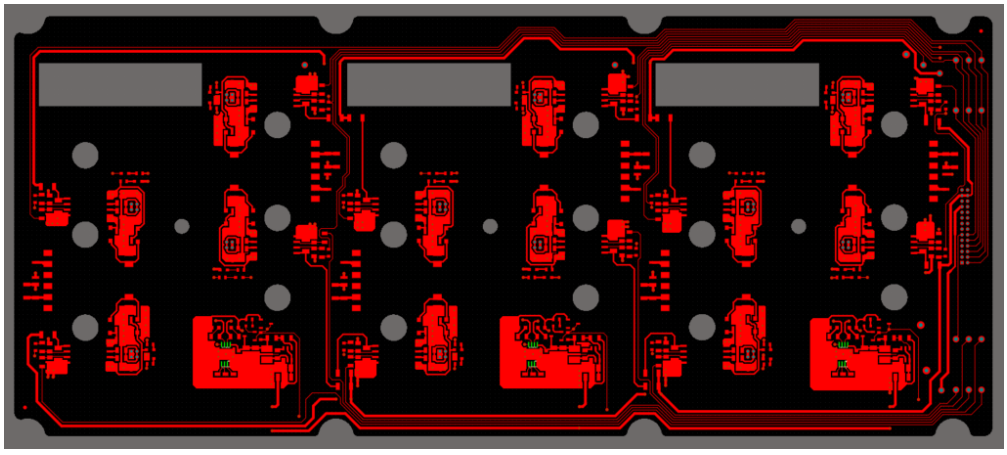


Figure 99 **Layer 1**

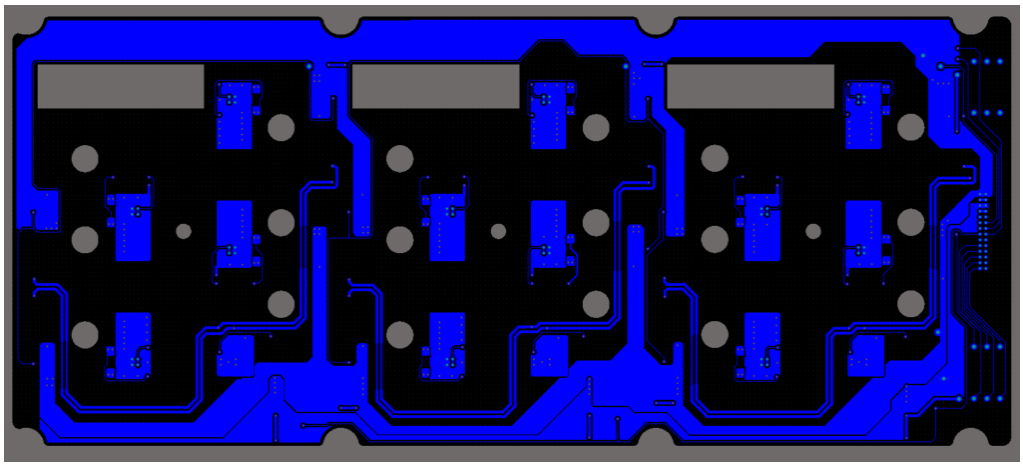


Figure 100 **Layer 2**

6.3 PB-APS-24V-5V ISO

Table 27 Mechanical data

Dimensions	57.1 mm x 27.1 mm
No. of layers	8
Copper thickness	105 µm

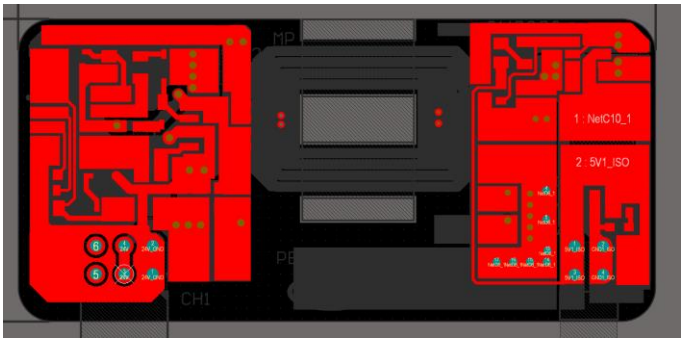


Figure 101 **Layer 1**

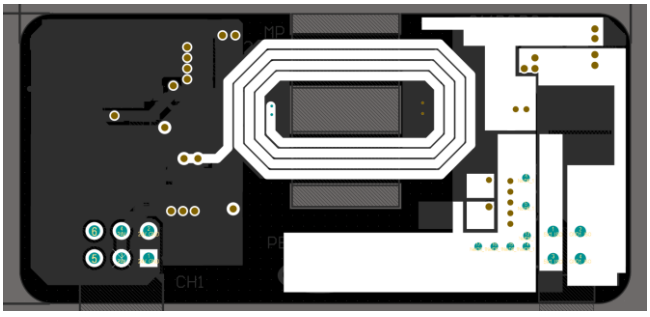


Figure 102 **Layer 2**

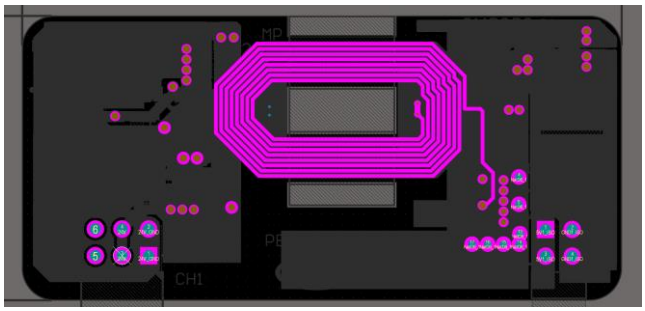


Figure 103 **Layer 3**

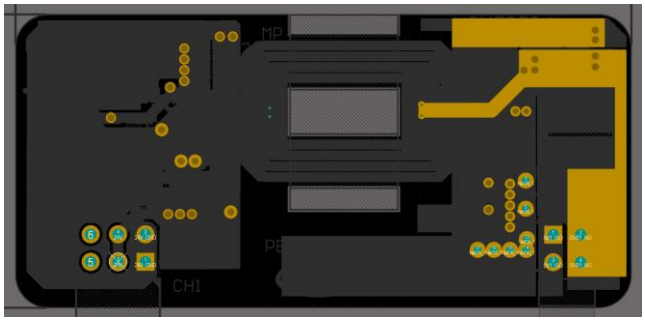


Figure 104 **Layer 4**

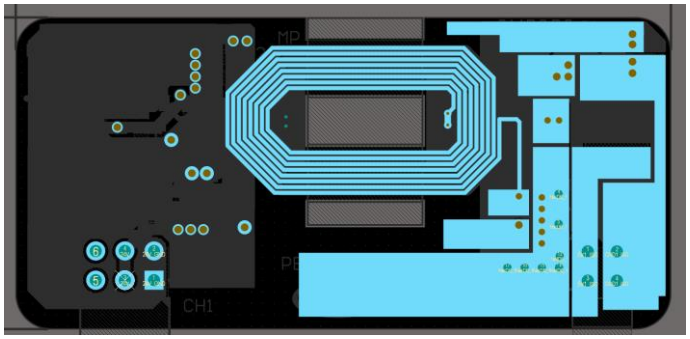


Figure 105 **Layer 5**

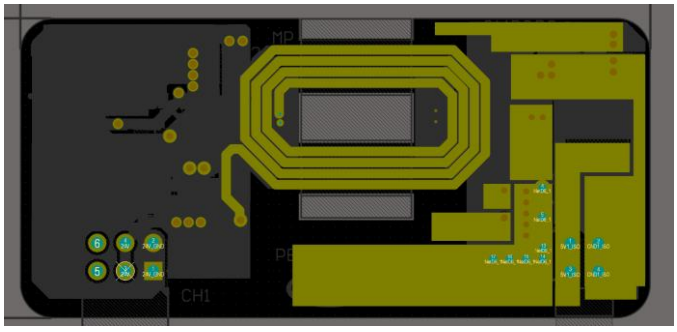


Figure 106 **Layer 6**

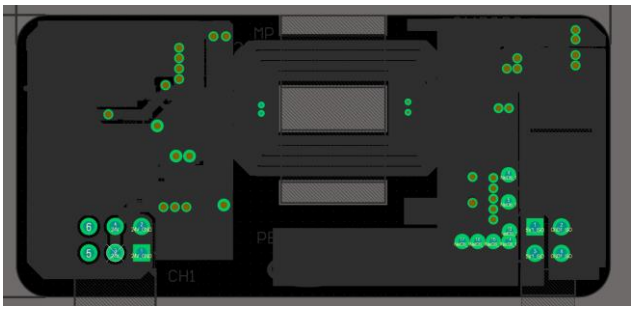


Figure 107 **Layer 7**

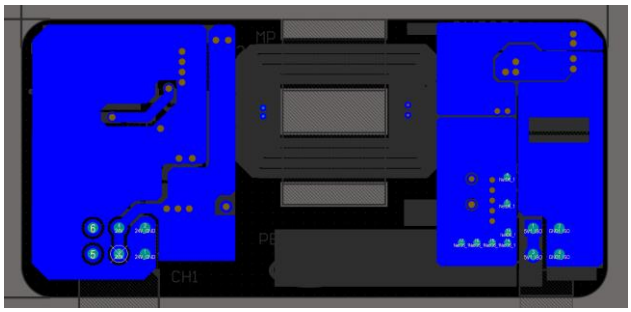


Figure 108 **Layer 8**

7 Bill of materials

Table 28 lists the key materials.

Table 28 BOM

Part	Description
IMCQ120R040M2H	1200 V, 56 A CoolSiC™ MOSFET in top-side cooled Q-DPAK package
IMDQ75R040M1H	750 V, 47 A CoolSiC™ MOSFET in top-side cooled Q-DPAK package
1ED3240MC12H	10 A, 5.7 kV (rms) single-channel isolated gate driver with two-level slew-rate control, UL 1577 and VDE 0884-11 certified
TLE4978-R050W5-O-S0010	High-precision, coreless current sensor for industrial applications
2EP130R	Full-bridge transformer driver
IRS27952	Half-bridge, high-voltage controller IC
IRF7351	60 V dual N-channel HEXFET power MOSFET in an SO-8 package
TLE42744GS V33	3.3 V Low Dropout Regulator

Revision history

Document revision	Date	Description of changes
V.1.0	2025-12-10	Initial release

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Document Reference Number

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Safety & Operating Instructions:
Customer shall check the Evaluation Board for any physical damage which may have occurred during transport. If customer detects any damages or defects in the Evaluation Board, customer shall not connect the Evaluation Board to a power source. Customer shall contact Infineon for further support. If customer observes unusual operating behavior during the evaluation process, customer shall immediately shut off the power supply to the Evaluation Board and consult Infineon for support.
Customer shall not touch the Evaluation Board during operation and keep a safe distance.
Customer shall not touch the Evaluation Board after disconnecting the power supply, several components may still store electrical voltage and can discharge through physical contact. Several parts, like heat sinks and transformers, may still be very hot. Allow the components to cool before touching or servicing.
The electrical installation must be completed in accordance with the appropriate safety requirements.