EVAL-FP50R12W2T7M5

Evaluation board design for EasyPIM™ 2B for general-purpose drives

About this document

Scope and purpose

This user guide provides an overview of the evaluation board design, EVAL-FP50R12W2T7M5, including its main features, key data, pin assignments, measurements results, and performance data. EVAL-FP50R12W2T7M5 is intended for general-purposes drives powered by EasyPIM™ 2B modules such as FP50R12W2T7 that features TRENCHSTOP™ IGBT7.

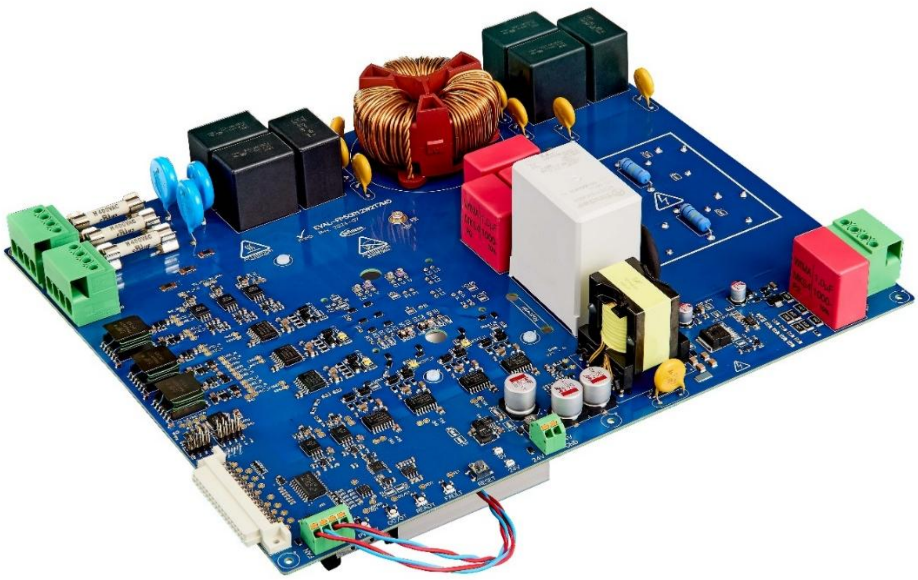
EVAL-FP50R12W2T7M5 includes the gate driver 1ED3321MC12N to switch the B6 topology properly. The driver circuitry of the evaluation board provides precise DESAT-detection and Miller clamping. In addition to general-purpose drives control, the evaluation board offers high-voltage sensing, phase-current sensing, temperature sensing, and protection measures. The evaluation board helps investigate the module's behavior with double-pulse testing (DPT) and system tests.

Intended audience

This user guide is intended for all technical specialists working on high-voltage traction inverters and also for those interested in understanding how Infineon products such as TRENCHSTOP™ IGBT7 and EiceDRIVER™ work under application conditions. The evaluation board's aim is to investigate the module's behavior within double pulse testing (DPT) and system tests.

Evaluation board

EVAL-FP50R12W2T7M5 comes with a pressed-in module and is mounted on to a heat sink. The thermal-interface material (TIM) is already applied. Please store the evaluation board under suitable ambient conditions to ensure proper functionality.



Note: Boards do not necessarily meet safety, EMI, and quality standards (for example UL, CE) requirements.

About this product group

Target applications

- Motor drives
- Auxiliary inverters
- Air conditioning

Product family

This evaluation board is equipped with a power module of the EasyPIM™ 2B product family. The EasyPIM™ 2B power module is designed for 1200 V, 50 A three-phase input rectifier power integrated modules (PIM). It comprises TRENCHSTOP™ IGBT7, an NTC, a preapplied TIM, and PressFIT contact technology. Especially, the EasyPIM™ 2B offers low V_{CEsat} and can operate in overload conditions of up to 175°C.

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Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

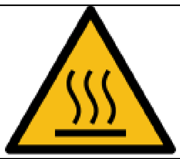
	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high-voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning**: *The evaluation contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the drive system, wait 5 minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by an oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation may become hot during testing. Hence, necessary precautions are required while handling the evaluation board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 The evaluation board at a glance

This user guide provides information about Infineon's EVAL-FP50R12W2T7M5 for EasyPIM™ 2B modules for three-phase input converters with TRENCHSTOP™ IGBT7 and emitter controlled 7 (EC 7) diodes (see Figure 1). This evaluation board is equipped with 1ED3321MC12N – the latest driver from the EiceDRIVER™ family that provides proper switching behavior and offers additional features such as short-circuit protection (DESAT). The isolated internal power supply for the gate driver is implemented with the flyback topology. The flyback topology is realized with the ICE5QSBG flyback controller, the 2EP130R transformer driver, and a transformer from Würth. Advantageously, the evaluation board is then independently supplied without any additional external power supply and can be operated autonomously from the HV grid. The evaluation board provides itself with the utilized 5 V generation through the TLF50211EL IC and is able to proceed with adjustable gate driver voltages (15.3 V/-10.5 V, +15.7 V/-9.1 V, 12.3 V/-6 V. 13.7 V/-6.6 V). Additionally, the evaluation board offers inbuilt temperature sensing, current sensing, and high-voltage sensing features to provide system measurements.

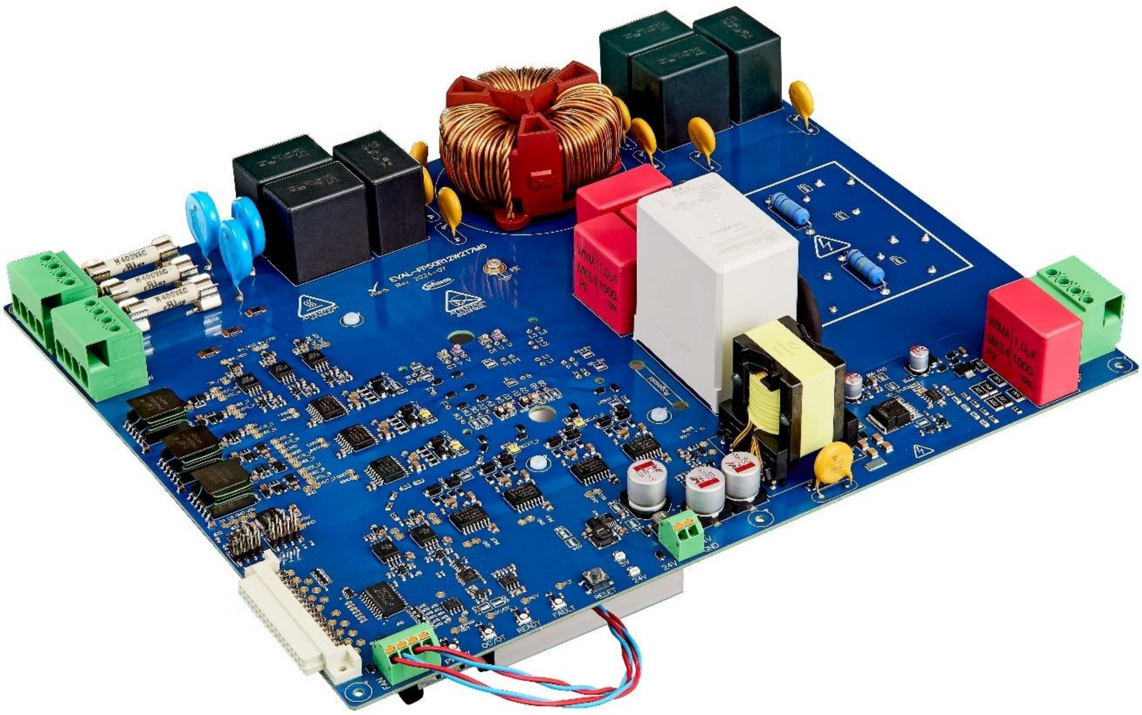


Figure 1 **EVAL-FP50R12W2T7M5: Evaluation board picture**

1.1 Scope of supply

The evaluation board EVAL-FP50R12W2T7M5, which includes

- A gate driver board
- A heat sink
- The power module FP50R12W2T7 with preapplied TIM [1]

1.2 Block diagram

Figure 2 presents a block diagram of the evaluation board's general functionality and the interaction between its key components. The emphasis is on an abstract representation of the evaluation board's operation.

Basically, the evaluation board can be divided into the power conversion part, and the logical supplying part. The power conversion part starts with a general power supply from the grid side via the -J1 connector. The input stage is supported by fuses, varistors, and an EMI filter. The B6 diodes, integrated within the power module, rectify the AC voltage to the associated voltage to generate the applied DC voltage. This voltage is then inverted via the B6 inverter to drive the external motor via the -J3 connector. The DC voltage is buffered by the DC link and is measured by voltage sensing for status information. The motor phase currents are measured through shunt measurements.

The evaluation board's logic part can be supplied in two ways – either by the flyback topology via high voltage or by an external auxiliary supply. The flyback topology is implemented by the quasi-resonant controller ICE5QSBG and the single-channel, low-side gate driver IC 1ED44171N01B to drive the transformer. The rectified power supply is then used to supply all the logical circuits on the evaluation board and additionally the cooling fans. The evaluation board can also be driven by an external power supply connected to -J4.

The gate driver power supply provides the benefit of adjustable voltage levels via the jumpers -J6 and -J7. The power supply is realized by Infineon's voltage regulator TLE 4284 together with Infineon's EiceDRIVER™ transformer driver 2EP130R. Each phase, consisting of a high-side and a low-side driver, is supplied by an independent circuitry.

The driver itself is driven by external PWM signals based on 5 V. These signals are connected via the drive card connector J8. J8 also includes system information signals such as phase current, high-voltage status, and temperature sensing. The evaluation board's operation is enabled via the "Enable" signal on the driver card.

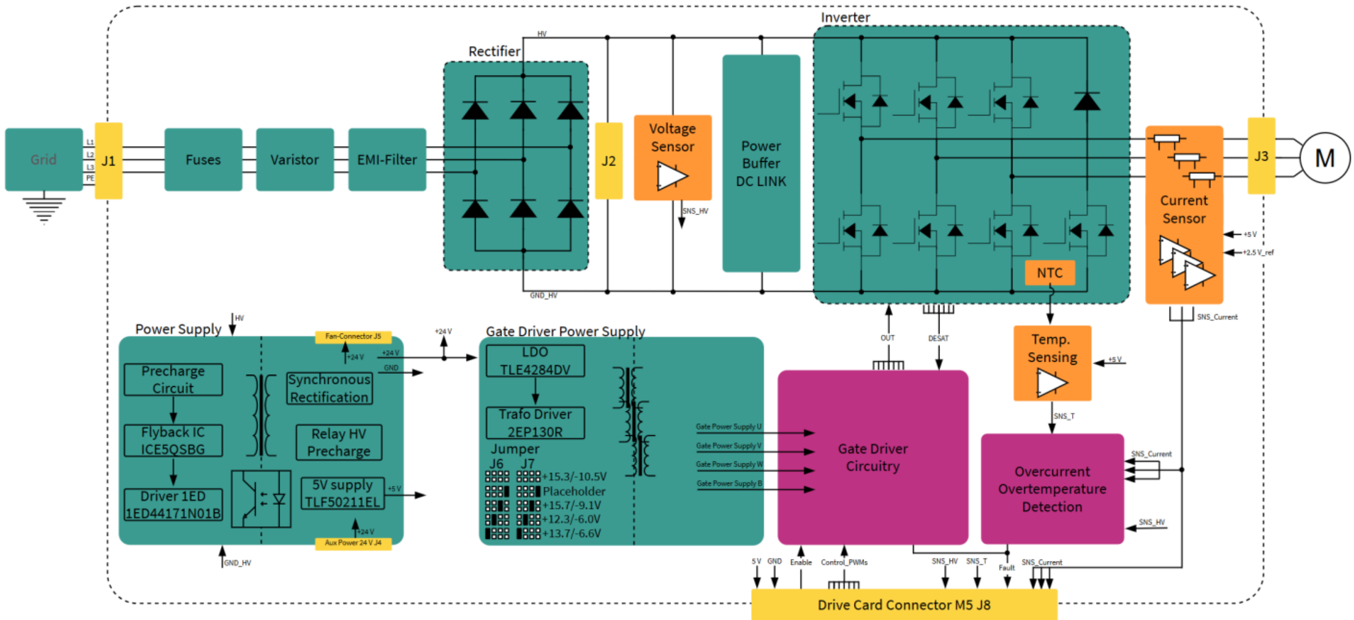


Figure 2 **EVAL-FP50R12W2T7M5: Block diagram**

1.3 Main features of the evaluation board

- EasyPIM™ power module with TRENCHSTOP™ IGBT7 and preapplied TIM
- Passive rectification, three-phase inverter, drive control, and measurements are integrated in one design
- Reinforced, isolated DC-link, phase-current, and NTC temperature measurements
- Independent power supply via flyback topology using Infineon's controller IC (ICE5QSBG)
- Auxiliary power supply for debugging
- Short circuit protection based on DESAT detection
- Overtemperature and overcurrent detection with monitoring on the interface
- PWM signals and system information communicated via an M5 connector
- Compact design with reinforced isolated gate driver and reinforced isolated internal power supply
- Wide range of use in terms of switching frequency, current, and voltage
- Multiple test points on the evaluation board provide a wide range of measurement and debugging options
- Wide range of evaluation opportunities on the EasyPIM™ 2B modules with various gate voltages
- Heat sink and thermals designed according to the power module's heat generation

1.4 Parameters and technical data of EVAL-FP50R12W2T7M5

Table 1 Kit parameters

Parameter	Unit	Min. value	Nominal value	Max. value
Input				
Three-phase input voltage at $f = 50$ Hz	V_{rms}	360	400	480
Current at $f = 50$ Hz	A_{rms}	0	-	32
Operational Parameters				
DC-link voltage (rectified)	V	300	540	690
Switching frequency	kHz	2	8	16
General auxiliary supply voltage	V	-5%	24	+5%
Analog circuit supply/signal level	V	-2%	5	+2%
Driver supply	V	-8 V ±5%	-	16 ±5%
Current measurement range	A	-60	-	60
Current analog output	mV/A	-	42	-
DC bus voltage measurement range	V	0	-	1000
Voltage analog output	mV/V	-	5	-
Voltage range for temperature measurement	V	2.0 at 0°C	88 m at 125°C	33 m at 175°C
Ambient temperature	°C	0	25	40
Output				
Power (3 phases)	kW	-	-	11
Current per leg at f_{nom}	A_{rms}	-	-	26
Current per leg at f_{max}	A_{rms}	-	-	15
Frequency	f		50	60

2 System and functional description

This chapter provides an overview of the functionalities of the evaluation board with a focus on the gate driver circuitries and the sub-schematics of the evaluation board. Figure 3 and Figure 4 show the evaluation board from the top side and from the front side. The sub-circuitries are highlighted in red boxes with yellow font to demarcate the system's sub-functionalities. The evaluation board is equipped with numerous test points to assist users investigate the evaluation board's behavior. The various-sub circuitries are explained in section 2.1.

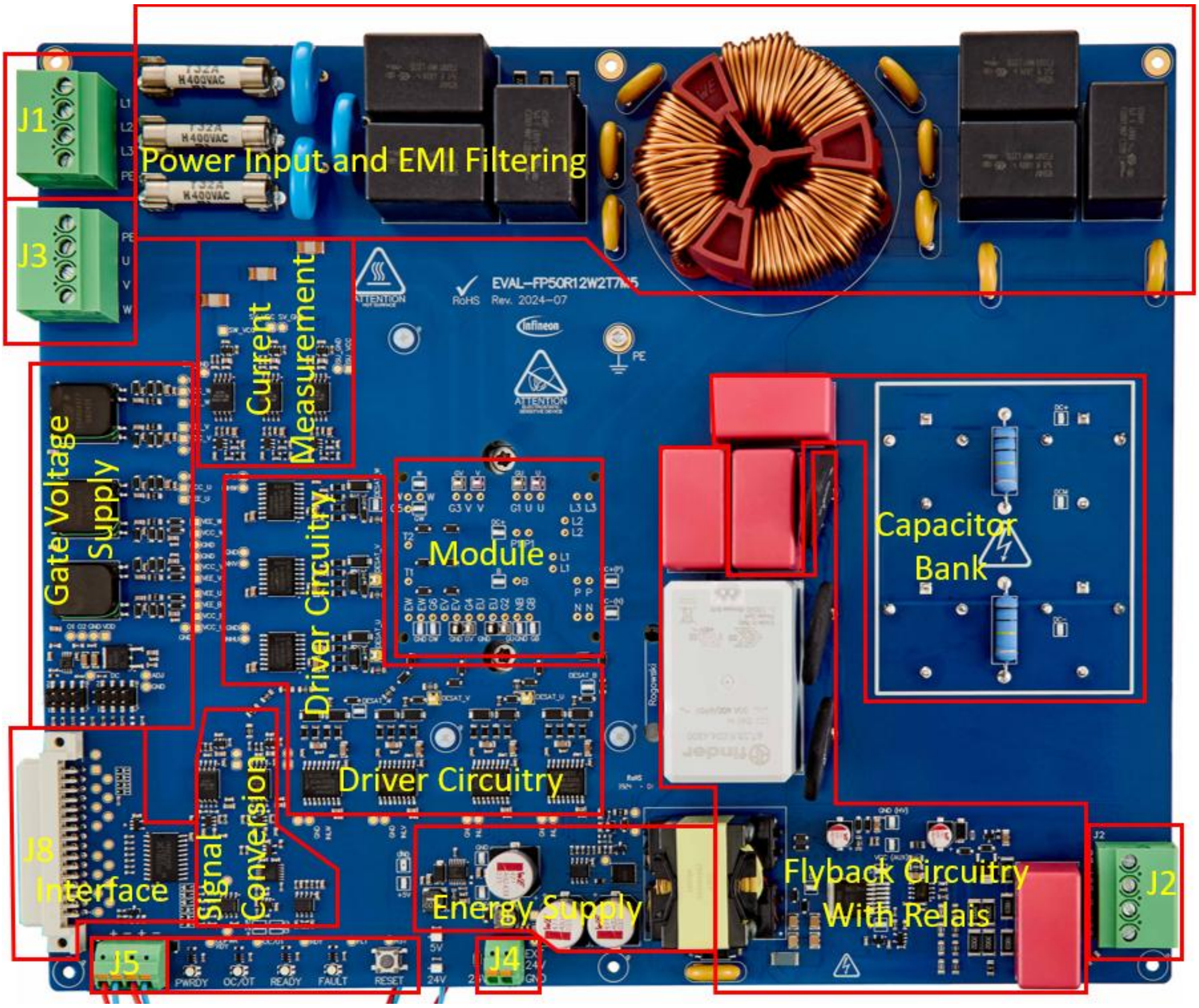


Figure 3 **EVAL-FP50R12W2T7M5: Top side**

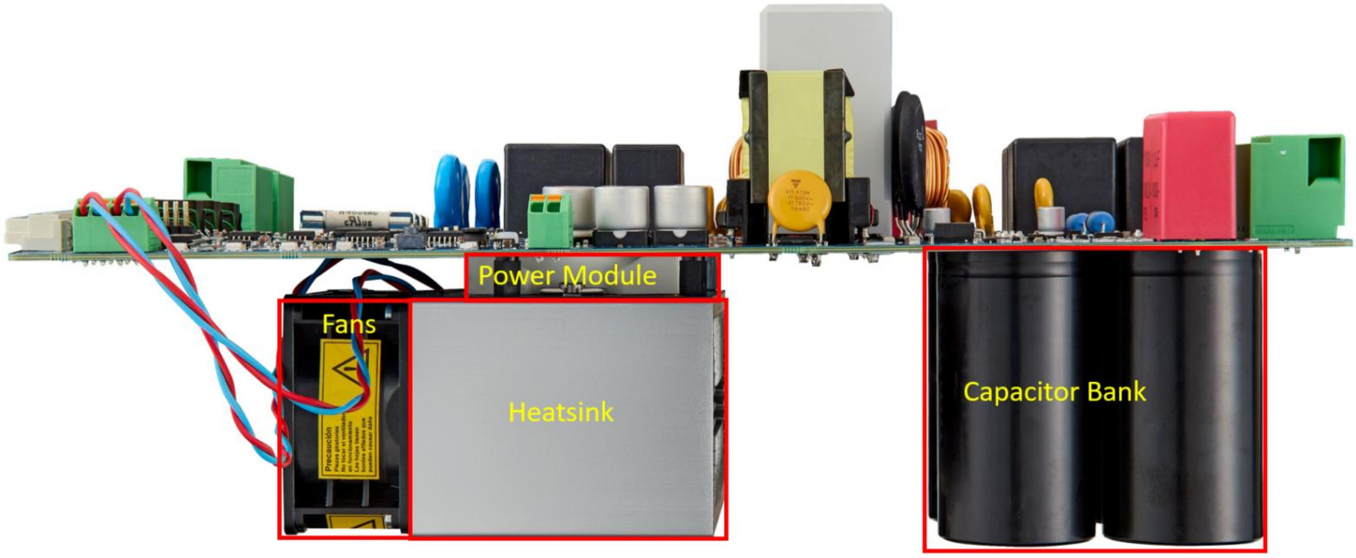


Figure 4 **EVAL- FP50R12W2T7M5: Front side**

Table 2 lists the evaluation board's power connectors. These connectors are highlighted in Figure 3.

Table 2 Power connector, auxiliary power supply and fan

PIN	Label	Function
-J1 1	L1	Power input L1
-J1 2	L2	Power input L2
-J1 3	L3	Power input L3
-J1 4	PE	PE
-J2 1	+VBUS_HV	Input output DC
-J2 2	B	Brake
-J2 3	+VBUS_HV	Input output DC
-J2 4	GND_HV	DC ground
-J3 1	PE	PE
-J3 2	U	Power output U
-J3 3	V	Power output V
-J3 4	W	Power output W
-J4 1	+24V_LV	Aux. power 24 V
-J4 2	GND_LV	Aux. GND
-J5 1	+24V_LV	Fan 1, 24 V
-J5 2	GND_LV	Fan 1, GND
-J5 3	+24V_LV	Fan 2, 24 V
-J5 4	GND_LV	Fan 2, GND

2.1 Hierarchical overview of the system

This section provides an overview of the hierarchical design of the complete system. The various sub-circuitries are emphasized in the images and are explained in detail in the next sections.

2.1.1 Power input stage	**2.1.2 Power output stage**	**2.1.3 Control interface**
2.1.4 Gate drivers	**2.1.5 Power management**	**2.1.6 Measurements**
	Auxiliary supply	Current sensing
	Gate driver	Temperature and voltage sensing
		Current and temperature control

The input stage is fed by the connector -J1, which is essentially the main three-phase AC input of the evaluation board. This AC input is rectified within the block of power input stage. The rectified voltage is available for both, the system's power management and the power output stage. Optionally, the evaluation board can be operated without the AC input. In this case, an external DC voltage can be applied to the connector -J2. Here, it must be noted that the rectifying part of the power module is inactive. Simultaneously, the inverted output voltage can be applied from the output connector -J3. To control the output stage, the IGBTs, six for the inverter and one for the brake chopper, are controlled by reinforced isolated gate drivers. The evaluation board is also equipped with an isolated, independent power management and internal system measurements. The gate driver's PWMs are routed from an external drive card to the gate drivers via the control interface which is equipped with the M5 connector (-J8). Additionally, the monitoring and status signals between the evaluation board and drive card are exchanged.

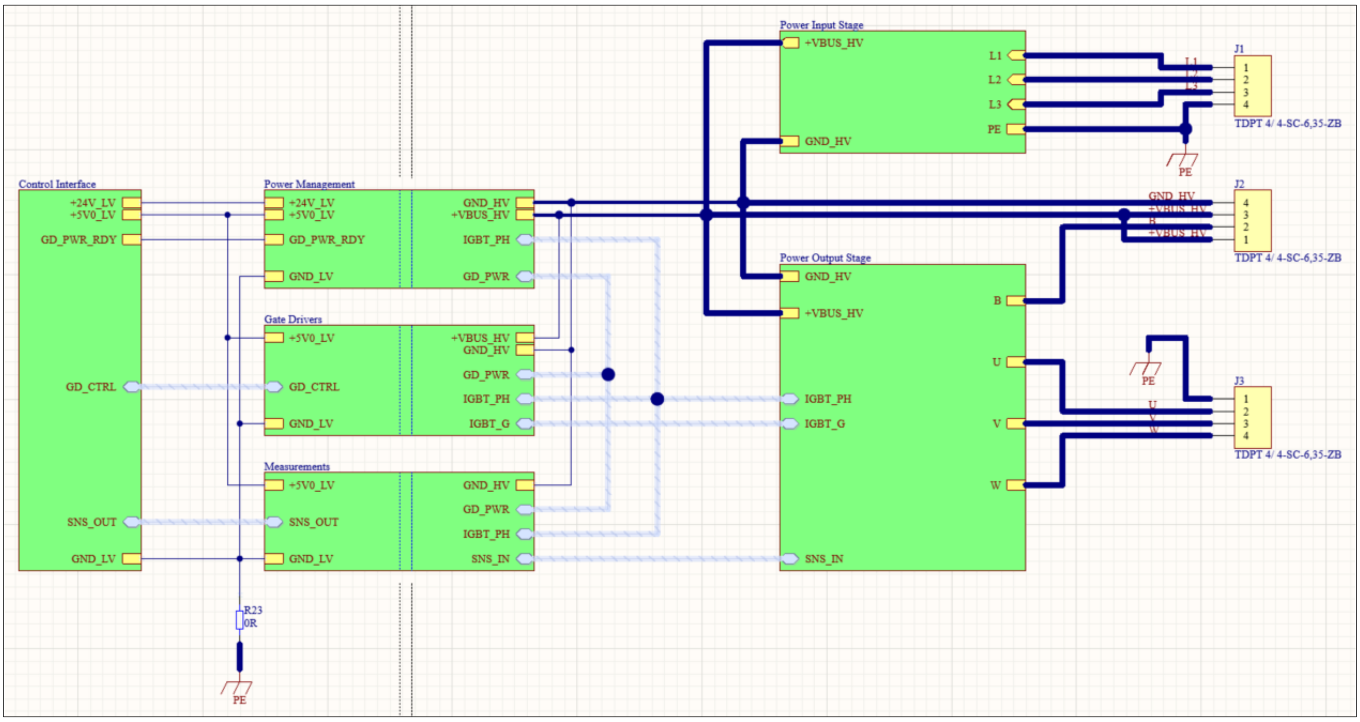


Figure 5 **EVAL-FP50R12W2T7M5: Hierarchical overview**

Caution: The precharge circuit is located between the output of the diode rectifier stage and the DC bus. Due to this, it will only operate when the evaluation board is tied to a grid. If the evaluation board is supplied directly with *a DC voltage at the DC bus, the precharge circuitry will not operate as intended because the DC bus interface connector is located after the precharge. In this case, the DC voltage should be slowly ramped up from the power supply used.*

2.1.1 Power input stage

This section shows the power input stage (see Figure 6). It is divided into the power input with melting fuses for overcurrent protection, the EMI filter, rectification via the power module's rectifier diodes, and the precharge circuitry with Y-capacitors. At the test points, -TP1 and -TP2, the rectified voltage can be measured during operation. The precharge circuitry ensures limited charging currents during the initial power-up of the system. After the evaluation board has powered up, the precharge circuit coil closes and continuous power supply to the evaluation board is enabled. The filtering itself (see Figure 7) is realized by a selection of X-capacitors and Y-capacitors as well as some inductivities. The EMI circuitry reduces high-frequency electromagnetic interferences in the evaluation board during operation enhancing its performance.

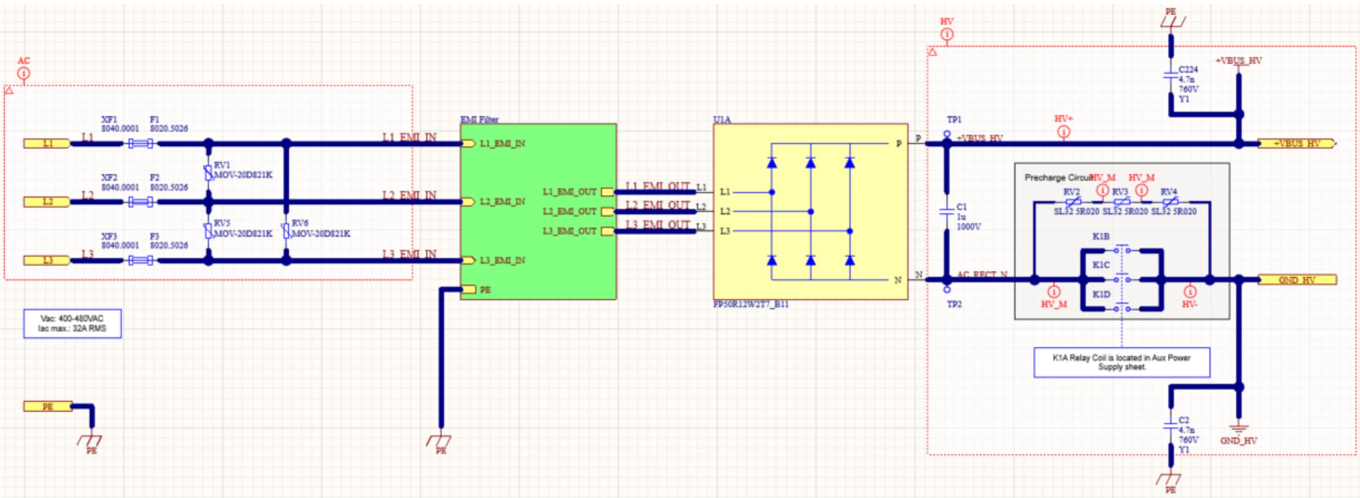


Figure 6 **EVAL-FP50R12W2T7M5: The power input stage**

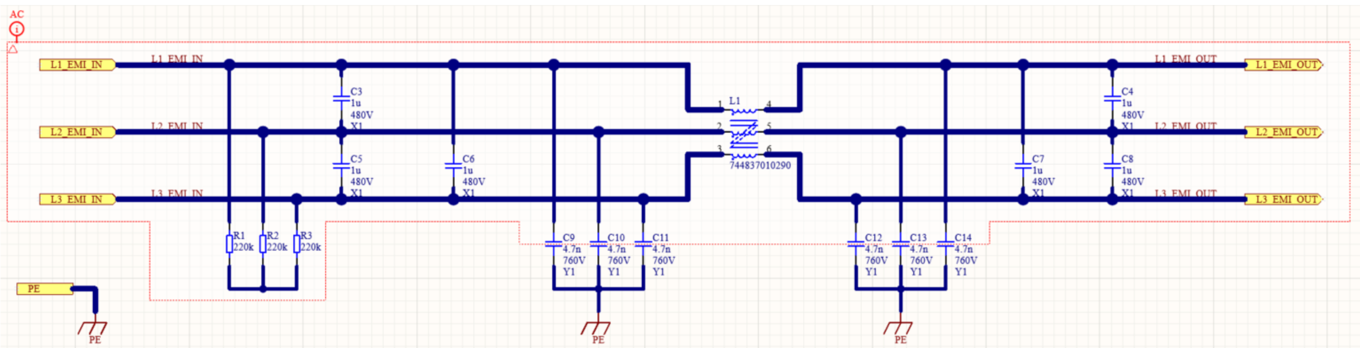


Figure 7 **EVAL-FP50R12W2T7M5: EMI filtering**

2.1.2 Power output stage

The power output circuitry can be divided into the DC-link capacitor bank, the high-voltage DC sensor, the module's B6 inverter including the brake chopper IGBT, and phase-current measurement at the output of the evaluation board. The capacitor bank is realized by four electrolytic capacitors, where two of them (in series) are connected in parallel to the other two (-C15, -C16, -C20, -C21). Additionally, the two capacitors (-C18, -C19) with smaller capacitance are placed closer to the module to enable proper energy supply in the module. The voltage in the DC link is then measured by a series connection of high-resistance resistors where one of them is applied as a shunt resistor (-R13). The voltage across this resistor and the temperature voltage signal of the module's integrated NTC is then passed to the measurement monitoring circuitry. The B6 inverter IGBTs and the brake chopper IGBT are driven by gate signals from the gate driver stage. The phase currents are measured using shunt resistors (-Rs1, -Rs2, -Rs3) and the corresponding voltage signals are passed to the measurement monitoring circuitry.

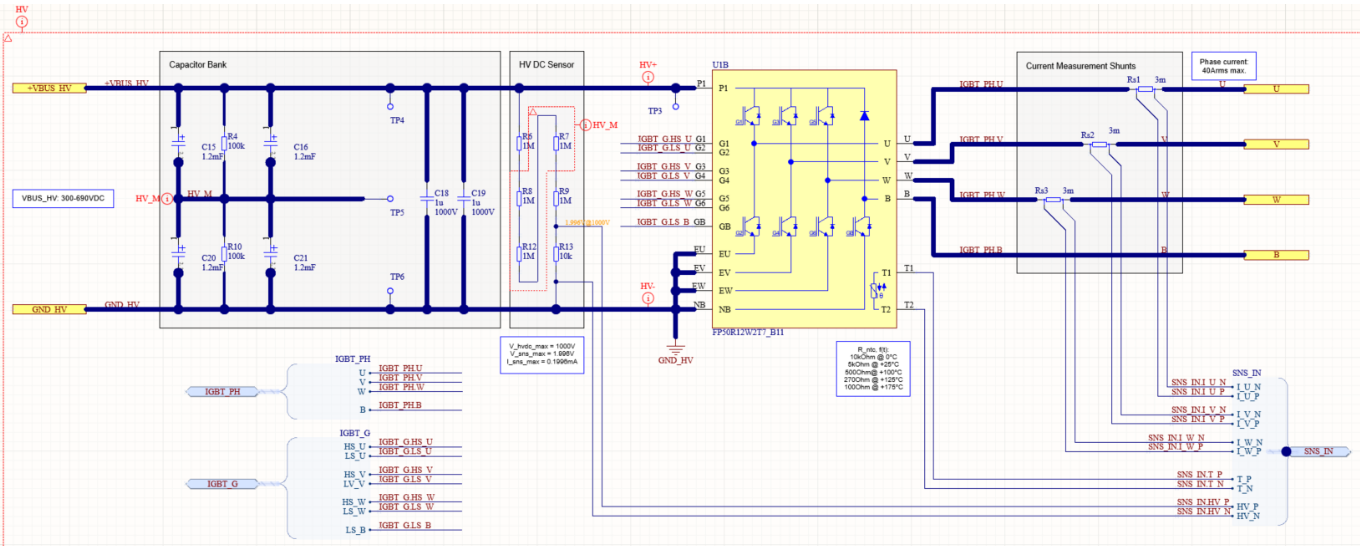


Figure 8 **EVAL-FP50R12W2T7M5: The power output stage**

2.1.3 Control interface

The control interface focuses mainly on exchanging signals between the evaluation board and the external driver card on the M5 connector (-J8). The main task is to pass the PWM signals from the external drive card to the driver stage of the evaluation board. Status and monitoring signals are also exchanged between the external driver card and the evaluation board. The M5 connector's pin assignment is listed in Table 3. Additionally, the digital status signals are preprocessed to ensure proper communication (-U35, -U37) and are indicated by corresponding LEDs (-D92, -D93, -D94, -D95).

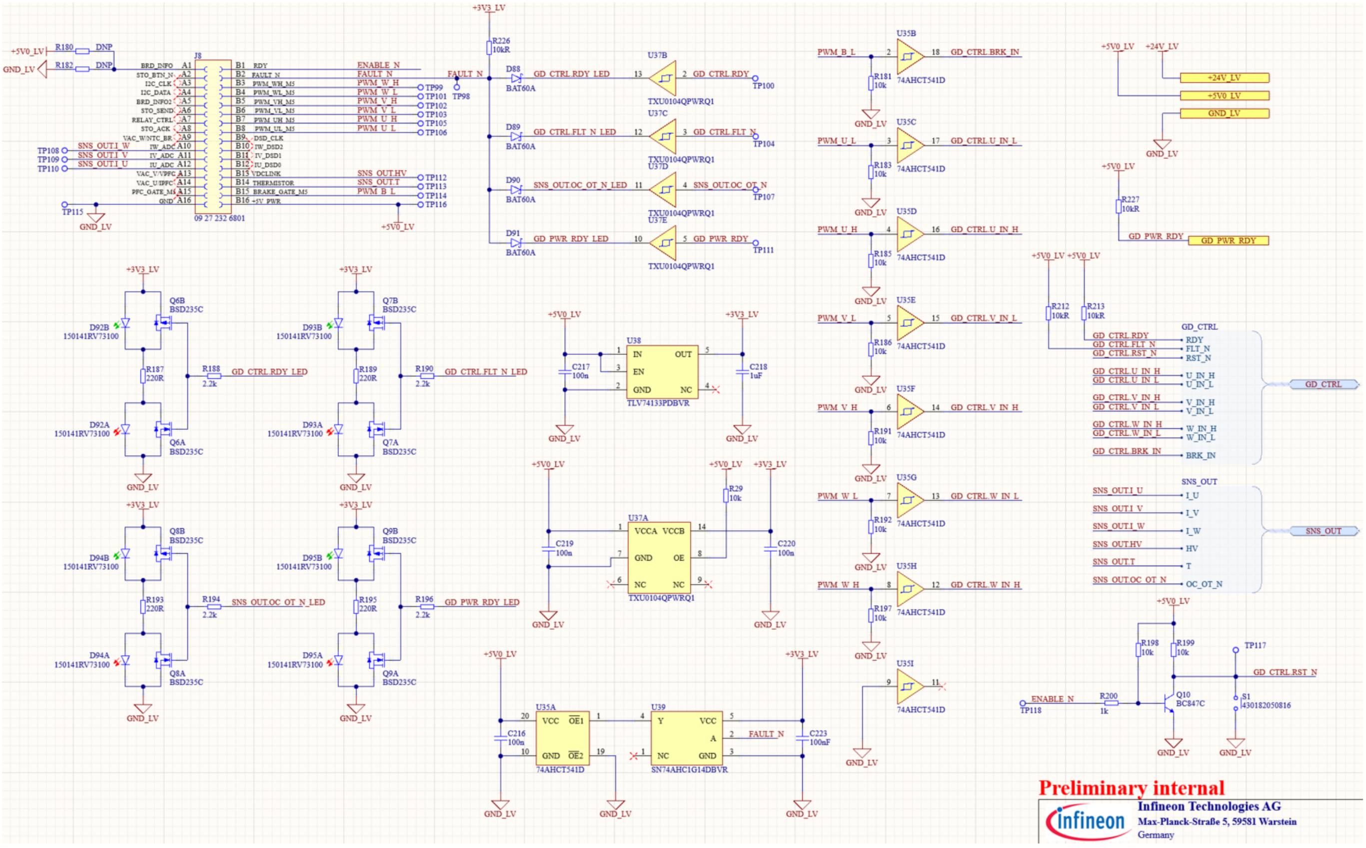


Figure 9 **EVAL-FP50R12W2T7M5: The control interface**

Table 3 Control interface: M5 connector (-J8)

PIN	Label	Function
-J8 A1	BRD_INFO	n.a.
-J8 A2	STO_BTN_N	n.a.
-J8 A3	I2C_CLK	n.a.
-J8 A4	I2C_DATA	n.a.
-J8 A5	BRD_INFO2	n.a.
-J8 A6	STO_SEND	n.a.
-J8 A7	RELAY_CTRL	n.a.
-J8 A8	STO_ACK	n.a.
-J8 A9	VAC_W/NTC_BR	n.a.
-J8 A10	IW_ADC	SNS_OUT.I_W
-J8 A11	IV_ADC	SNS_OUT.I_V
-J8 A12	IU_ADC	SNS_OUT.I_U
-J8 A13	VAC_V/VPFC	n.a.
-J8 A14	VAC_U/IPFC	n.a.
-J8 A15	PFC_GATE_M5	n.a.
-J8 A16	GND	GND_LV
-J8 B1	RDY	ENABLE_N
-J8 B2	FAULT_N	FAULT_N
-J8 B3	PWM_WH_M5	PWM phase W high-side
-J8 B4	PWM_WL_M5	PWM phase W low-side
-J8 B5	PWM_VH_M5	PWM phase V high-side
-J8 B6	PWM_VL_M5	PWM phase V low-side
-J8 B7	PWM_UH_M5	PWM phase U high-side
-J8 B8	PWM_UL_M5	PWM phase U low-side
-J8 B9	DSD_CLK	n.a.
-J8 B10	IW_DSD2	n.a.
-J8 B11	IV_DSD1	n.a.
-J8 B12	IU_DSD0	n.a.
-J8 B13	VDCLINK	SNS_OUT.HV
-J8 B14	THERMISTOR	SNS_OUT.T
-J8 B15	BRAKE_GATE_M5	PWM_B_L
-J8 B16	+5V_PWR	+5V0_LV

2.1.4 Gate drivers

The gate driver circuitry is illustrated (example of one phase) in Figure 10. Generally, the gate driver circuitry consists of Infineon's single-channel gate driver (1ED3321MC12N) for each switch. The gate driver is housed in a DSO-16 wide-body package ensuring reinforced insulation according to IEC 60747-17. Each control signal is routed across the evaluation board from the control interface to the associated driver's input (IN_P).

The driver itself is equipped with some status input and outputs. The RDY output signal reports on the correct operation of the device. The /RST input signal either enables or shuts down the driver and provides the possibility of resetting the driver after DESAT events. /FLT is an open-drain output that reports on desaturation faults in the power transistor and if desaturation occurs, /FLT is low.

On the driver's secondary side, the driver is able to switch the power module via OUTH and OUTL. By default, the evaluation board is delivered with two 10 Ω resistors in parallel for both turn-on and turn-off switching of the power module. If the total 5 Ω resistance is not suitable for the system's test setup, it can be adjusted manually. The evaluation board's driver circuitry is also applied to the CLAMP and DESAT functionality.

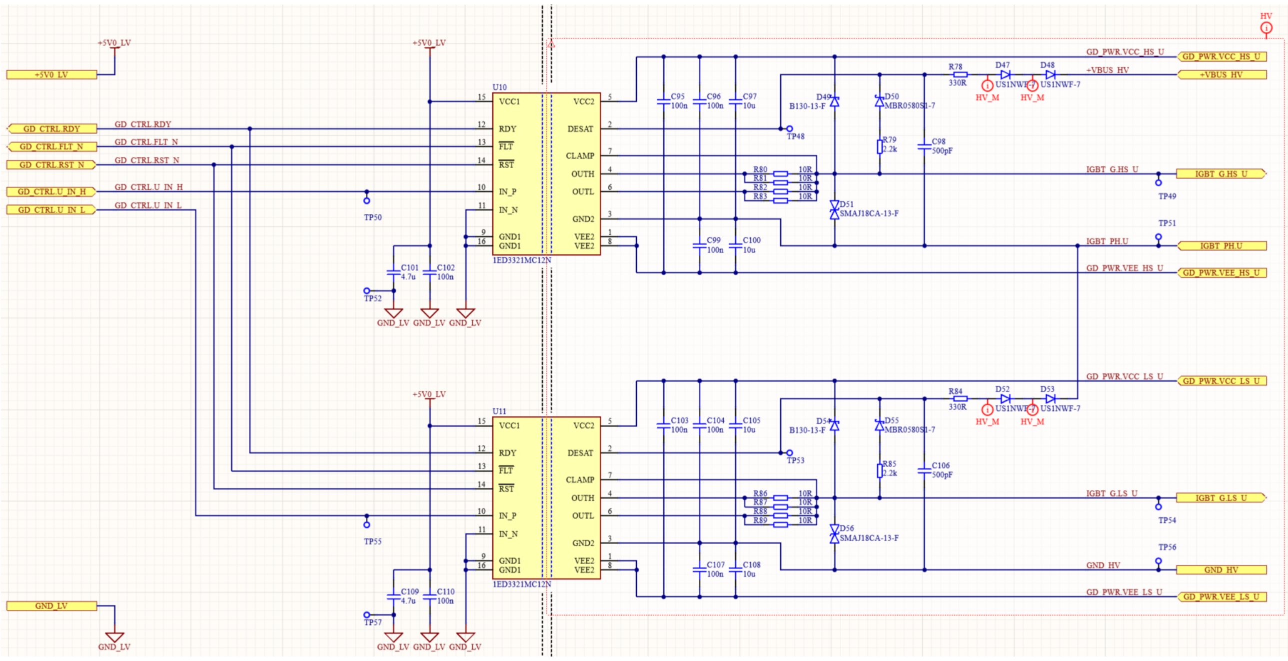


Figure 10 **EVAL-FP50R12W2T7M5: The gate driver circuitry**

2.1.5 Power management

The section explains the circuitries related to power management of the evaluation board. The power supply on the board can be divided into the following sub-circuitries:

- The auxiliary-supply based on a flyback converter topology
- The isolated gate voltage supply for the gate driver

Auxiliary supply

The evaluation board's internal power supply is realized by the isolated flyback topology using Infineon's flyback controller (IC ICE5QSBG) in combination with Infineon's CoolSiC™ MOSFET IMBF170R1K0M1 and the low-side gate driver 1ED44171N01B. Both are implemented on the primary side of the power supply to energize the Würth Electronik transformer. Additionally, the flyback conversion comes with an independent low-dropout voltage regulator. The power supply is controlled by the closed feedback-loop from the secondary side across the optocoupler -U5. Moreover, the precharge circuitry (-Q2 Infineon's IPN95R3K7P7, -Q4 IRLML2060TRPBF) enables voltage-suitable energy supply for the conversion and a snubber circuitry in front of the transformer ensures correct behavior. For more details on flyback control, please refer to ICE5QSBG's data sheet. Energy buffering as well as the feedback loop across the inductance (-L2) and the optocoupler (-U5) are realized on the secondary side. The rippling transformer output is then rectified trough synchronous rectification (-U2).

The circuit also provides fan power supply across the connector -J5 and an auxiliary supply for debugging across the connector -J4. If the system is sufficiently supplied with 24 V, the relais -K1A turns off the precharge circuit for the high-voltage supply. The evaluation board is then fully powered up. The 5 V power supply is implemented by Infineon's buck switching regulator -U7 (TLF50211EL) for the logical circuitries of the evaluation board.

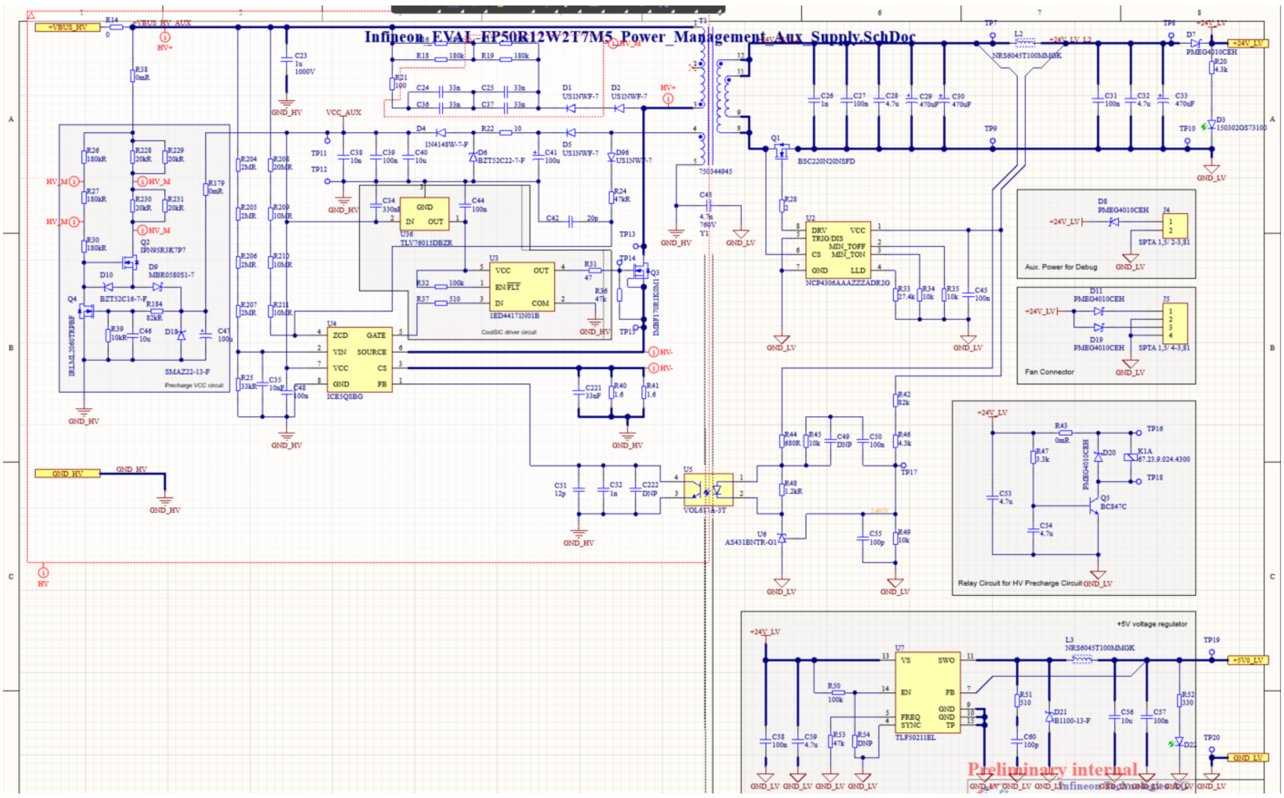


Figure 11 **EVAL-FP50R12W2T7M5: Power management auxiliary supply**

Gate driver

The evaluation board's gate drivers are supplied by a separate isolated power management (see Figure 12). This circuitry comes with Infineon's linear output voltage regulator TLE4284DV (-U8), which provides proper energy supply for the full-bridge transformer driver 2EP130R (-U9). Via jumpers -J6 and -J7, the gate driver's voltage level can be manually adjusted to different levels. The jumper's positioning and its associated gate driver voltage levels can be found in the Figure 2 or in the Table 4 below. The supply voltage is then transferred across three isolated transformers supplying the six gate drivers for the three phases (U, V, W) and the brake driver as well. The power supply should be peak rectified on the secondary side behind the transformer to achieve the target gate driver voltages via suitable Schottky diodes. These voltages are then connected to the gate circuitry.

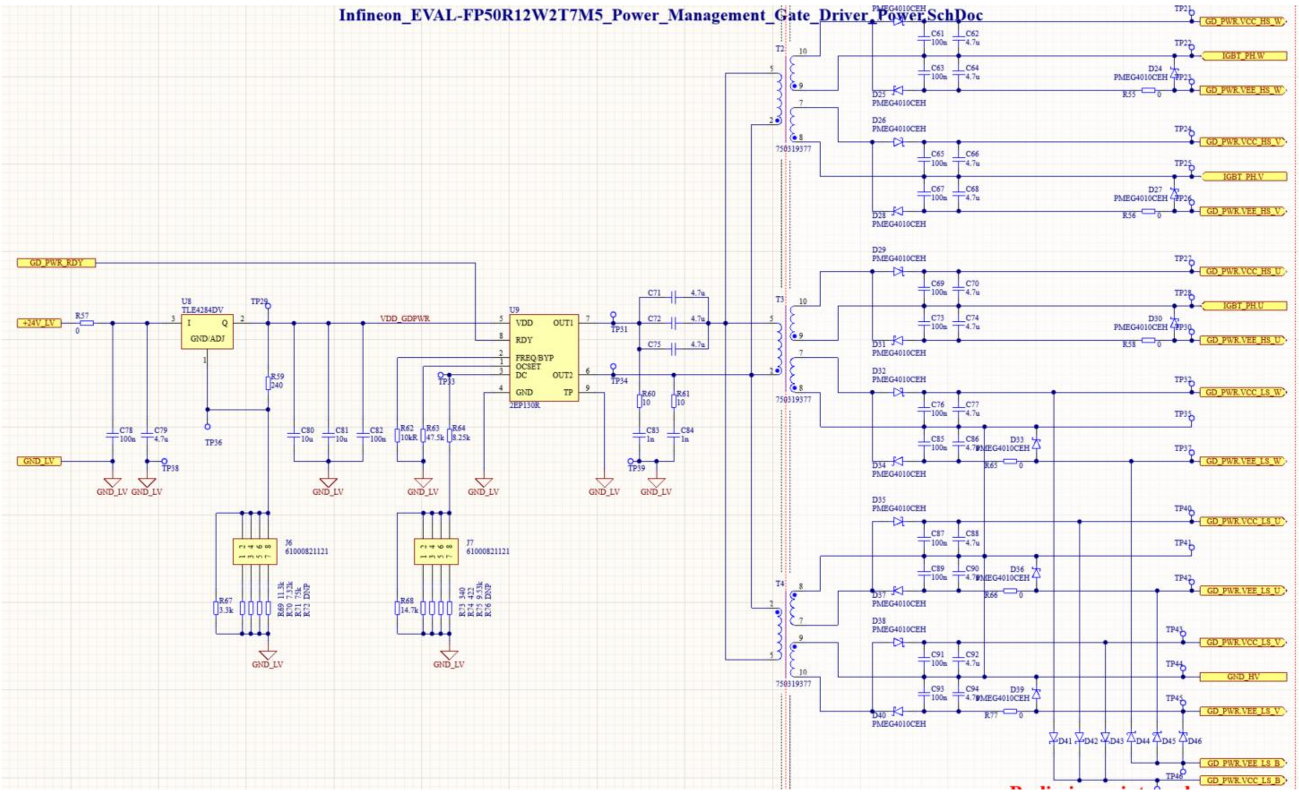


Figure 12 **EVAL-FP50R12W2T7M5: The driver supply rectifier**

Table 4 Jumper positioning for the associated gate driver voltages

Jumper -J6	Jumper -J7	Neg. gate voltage level	Pos. gate voltage level
□□□□ □□□□	□□□□ □□□□	Standard +15.3 V	Standard -10.5 V
□□□█ □□□█	□□□█ □□□█	Placeholder	Placeholder
□□█□ □□█□	□□█□ □□█□	+15.7 V	-9.1 V
□█□□ □█□□	□█□□ □█□□	+12.3 V	-6.0 V
█□□□ █□□□	█□□□ █□□□	+13.7 V	-6.6 V

2.1.6 Measurements

This section explains the sub-circuitries related to the measurements on the evaluation board. The current sensing, temperature and voltage sensing, current and temperature control sub-circuitries can be seen as monitoring blocks on the evaluation board and therefore reflect deeper system representation.

Current sensing

The current sensing is designed by shunt measurements where the reference voltage for zero current is set to a reference voltage of 2.5 V. The current sensor circuitry is generally designed by using a reinforced isolated amplifier with a gain of G_{iso} = 8.2. On the primary side, the circuitry is supplied with 5 V internally by Infineon's voltage regulator TLE4296-2G V50. On the secondary side, the current signal is adjusted to the associated voltage level with a gain of G_{diff} = 1.69. The based calculation is presented as follows:

$$R_{shunt} = 3\ m\Omega, V_{ref} = 2.5\ V, G_{diff} = \frac{16.9\ k\Omega}{10\ k\Omega} = 1.69, G_{iso} = 8.2$$

$$I_{phase,range} = [-50\ A, 50\ A], V_{shunt} = 0.003\ \Omega \cdot I_{phase,range} = [-0.15\ V, 0.15\ V]$$

$$V_{ph,mcu,V} = V_{shunt} \cdot G_{diff} \cdot G_{iso} + V_{ref}$$

In case the representative current signal has to be analyzed or monitored externally, the signal should be transferred again into the corresponding current value.

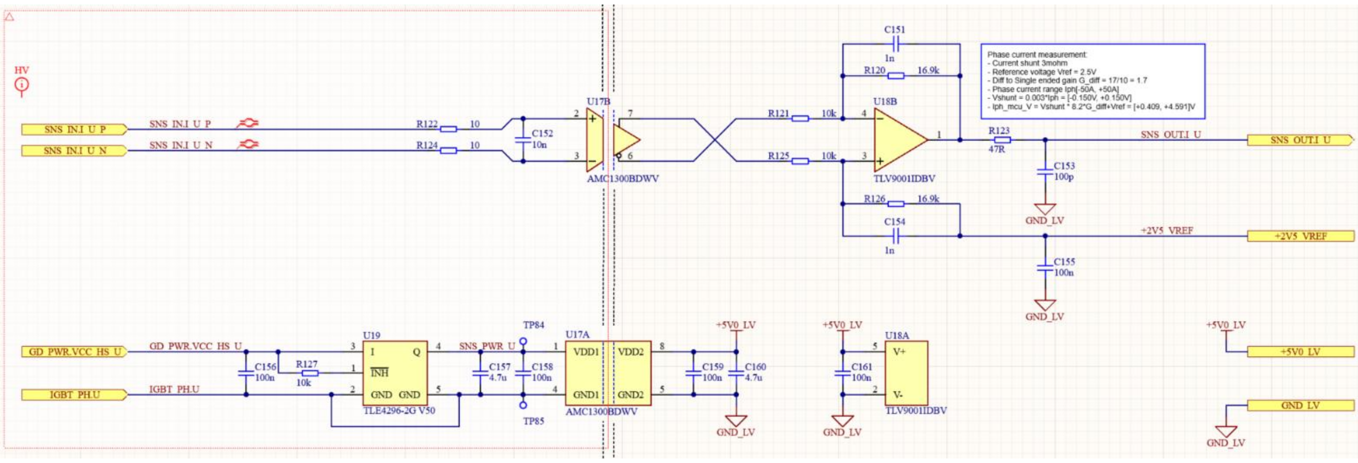


Figure 13 **EVAL-FP50R12W2T7M5: The current sensor circuitry**

Temperature and voltage sensing

Fundamentally, the voltage sensing circuitry (upper part of Figure 14) and the temperature sensing circuitry (lower part of Figure 14) have similar implementation. On the primary side, both circuitries are supplied by Infineon's TLE4296-2G V50. This power supply is applied to the reinforced isolated amplifiers which then transfer the DC-link voltage signal and the module's NTC signal to the secondary side. To convert the signals to the associated voltage levels, the signals are amplified and then routed to the evaluation board's interface output. The following formulas are used to calculate the module's operational temperature at the NTC. The NTC resistance R_{NTC} should be calculated first. This value can then be applied to the formula for deriving the module's NTC temperature T. The R_0, β, and T_0 values can be found in the module's datasheet.

$$V_{temp,dif}[V] = 5V \cdot \frac{R_{NTC}}{R_{NTC} + 15k\Omega}$$

$$V_{mcu}[V] = V_{temp,dif}[V] \cdot \frac{25k}{10k}$$

$$R_{NTC} = R(t) = R_0 \cdot e^{\beta\left(\frac{1}{T} - \frac{1}{T_0}\right)}$$

Table 5 shows some sample results of the calculations

Table 5 Sample results from the module's temperature calculation

T [°C]	R_{NTC} [Ω]	V_{NTC} [V]
0	10 k	2.0
+ 25	5 k	1.25
+ 100	500	0.161
+ 125	270	0.088
+ 175	100	0.033

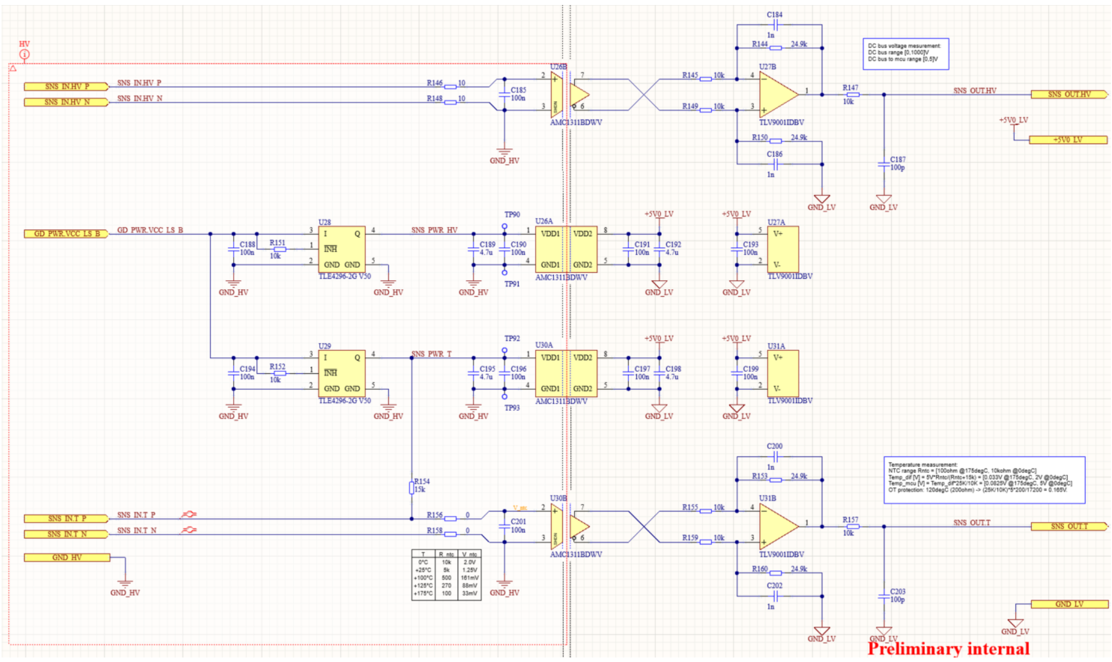


Figure 14 **EVAL-FP50R12W2T7M5: Voltage sensing and temperature sensing circuitry**

Overcurrent and overtemperature detection

The circuitry to detect overcurrent and overtemperature is shown in Figure 15. Basically, the overcurrent and overtemperature detection is based on dual-comparator ICs (-U32, -U33). To create the reference voltage V_{ref} = 2.5 V required for the current sense, the current detection circuitry should have an independent supply of 2.5 V (-U34). Thus, the current signal can be compared with a voltage divider for both positive current values (-U32B) and negative current values (-U32C). Here, the maximum current value of ±55 A, which is reflected by the maximum value of 4.8 V and minimum value of +0.2 V respectively, forces the output to set the overcurrent warning for each phase.

Overtemperature detection has a similar implementation with the threshold value set to 0.165 V. This value reflects an NTC temperature of 120°C and is realized by a voltage divider. If a temperature higher than 120°C is detected, the overtemperature warning is triggered.

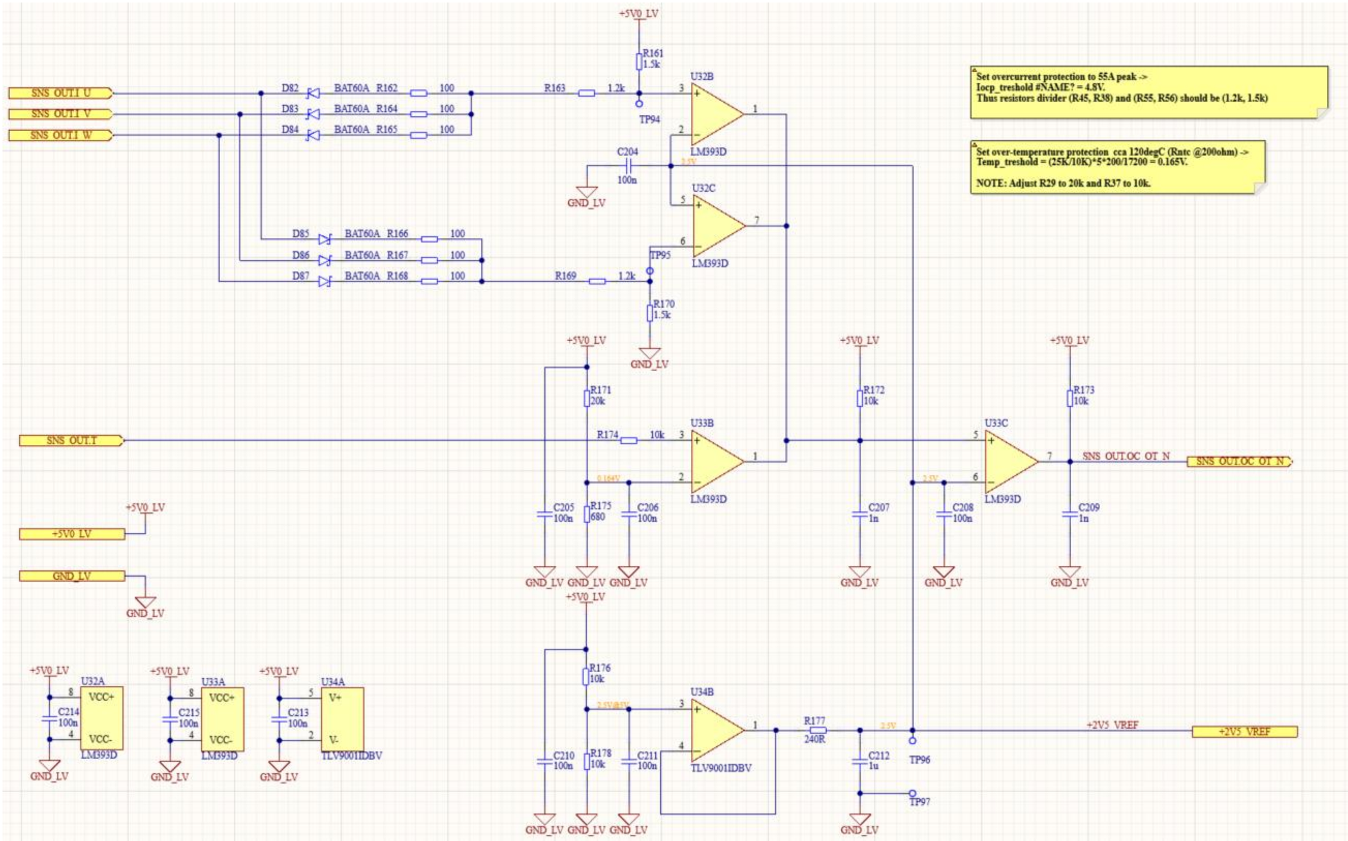


Figure 15 **EVAL-FP50R12W2T7M5: Overcurrent and overtemperature protection**

2.2 Bill of materials

A list of selected main components is provided in Table 6 to give an outline of the assembled components.

Table 6 Bill of materials for EVAL-FFXR12MT7DR

Designator	Component	Description
-C15, -C16, -C20, -C21	B43516B9128MO60	TDK Elco. capacitor, 1.2 mF, 400 V, THT
-C41, -C47	865080545012	Würth Elektronik, capacitor, 100 µF, 35 V
-D3, -D22	150302GS73100	Würth Elektronik, LED WL-SMTW SMT, green
-D92, -D93, -D94, -D95	150141RV73100	Würth Elektronik, LED green/red clear, 3528, SMD
-J6, -J7	61000821121	Würth Elektronik, HEADER SMD, 8 Pos, 2.54MM
-L1	744837010290	Würth Elektronik, 1 mH, 3-line through-hole choke 29 A
-Q1	BSC220N20NSFD	Infineon, OptiMOS™ MOSFET, SuperS08, 52 A [2]
-Q2	IPN95R3K7P7	Infineon, CoolMOS™ P7 SJ, 950 V, SOT223 [3]
-Q3	IMBF170R1K0M1	Infineon, CoolSiC™ 1700 V SiC TO-263-7 [4]
-Q4	IRLML2060	Infineon, 60 V HEXFET Power MOSFET, Micro 3 [5]
-Q6, -Q7, -Q8, -Q9	BSD235C	Infineon, OptiMOS™ 2, small signal transistor [6]
-T1	750344945	Würth Elektronik, transformer, 900 V, 24 V/2 A
-T2, -T3, -T4	750319377	Würth Elektronik, pulse transformers 1.4:1:1
-U1	FP50R12W2T7P_B11	Infineon, EasyPIM™ 2B, 1200 V, 50 A [7]
-U3	1ED44171N01B	Infineon, low-side gate driver, 25 V, 2.6 A [8]
-U4	ICE5QSBG	Infineon, flyback controller, PG-DSO-8 [9]
-U7	TLF50211EL	Infineon, MHz stepdown regulator 500 mA [10]
-U8	TLE4284DV	Infineon, NPN voltage regulator, 1.0 A [11]
-U10, -U11, -U12, -U13, -U14, -U15, -U16	1ED3321MC12N	Infineon, gate driver, 2300 V single-channel isolated, SC-protection, miller clamp [12]
-U19, -U22, -U25, -U28, -U29	TLE4296-2G V50	Infineon, voltage regulator, PG-SCT585, 5 V [13]

2.3 Mechanical data

The mechanical data of the evaluation board is listed in Table 7. This data can be applied to re-manufacture the evaluation board's PCB. The PCB and its components are appropriately selected with respect to the clearance and creepage requirements [2].

Table 7 Mechanical PCB manufacturing data

Description	Value
Number of layers	6
PCB copper thickness – inner layers	70 µm
PCB copper thickness – outer layers	105 µm
PCB insulating material	FR4
Evaluation board length/width/height	~ 300 mm/~ 250 mm/~ 150 mm
PCB thickness/assembled board weight	~ 2 mm/~ 4400 g

2.4 Thermal design

An important aspect of designing the power stage is the dimensioning of the cooling system for removing heat from the power semiconductors. To calculate these values, a combined 1D analytical and simulation approach was applied. Semiconductor losses were calculated via Infineon's IPOSIM tool for different operating conditions within the three-phase PIM module, as listed in Table 8.

Table 8 Operational conditions: Results of thermal simulation

Parameters	OP1 cos(ϕ) = 0.1	OP2 cos(ϕ) = 0.9	OP3 110%
DC-link voltage [V]	600	600	600
Output current [A rms]	25	25	27.5
Switching frequency [kHz]	8	8	8
Modulation index	0.98	0.98	0.98
Power factor cos(ϕ)	0.04	0.9	0.9
Ambient temperature T_a [°C]	20	20	20
Gate resistor $R_{g,on}$, $R_{g,off}$ [Ω]	5.1	5.1	5.1
$P_{switch,IGBT}$ [W]	18.37	20.16	23.71
$P_{con,IGBT}$ [W]	7.45	12.39	14.31
$T_{j,max,IGBT}$ [°C]	126.74	155.4	177.26
$P_{switch,fwd}$ [W]	6.8	7.56	8.93
$P_{con,fwd}$ [W]	6.9	1.99	2.22
$T_{j,max,fwd}$ [°C]	125.39	140.37	159.61
$P_{con,rectifier}$ [W]	0.3	8.19	9.14
$T_{j,max,rectifier}$ [°C]	103.31	139.71	158.15
P_{total} [W]	238.95	301.79	349.81

After calculating the losses of the power module, an analytical approach was taken to determine the appropriate thermal resistances of the heat sink with the following assumptions:

- Maximum ambient temperature: 40°C
- Infineon's TIM 1.0: R_{thJH} =0.938 K/W[1] [3]
- Maximum fixed IGBT junction temperature: 175°C
- Average operating point: OP2 cos(ϕ) = 0.9
- The junction temperature of the IGBT is the hottest point in the setup

The thermal correlations of the system are illustrated with the corresponding boundary value in Figure 16. The approach gave a required thermal resistance of **<u>≤0.35 K/W</u>** for the heat sink [4].

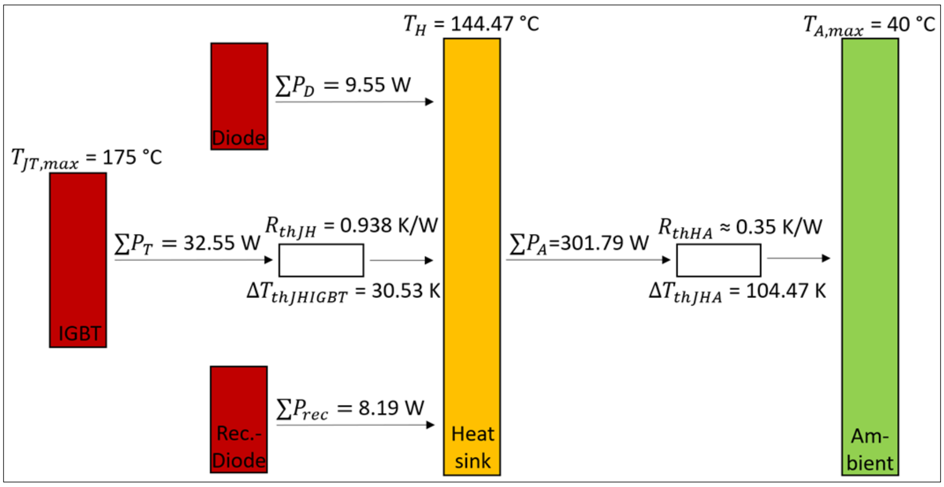


Figure 16 **System's thermal diagram: Calculating the thermal resistance**

Based on the maximum required thermal resistance of the heat sink, the Fischer Elektronik LAM 6 D 75 24 V heat sink was chosen (see Figure 17).

The average thermal resistance of this heat sink is ~0.345 K/W. Its dimensions are 120 mm x 75 mm x 60 mm (fitted with standard 60 mm fans)

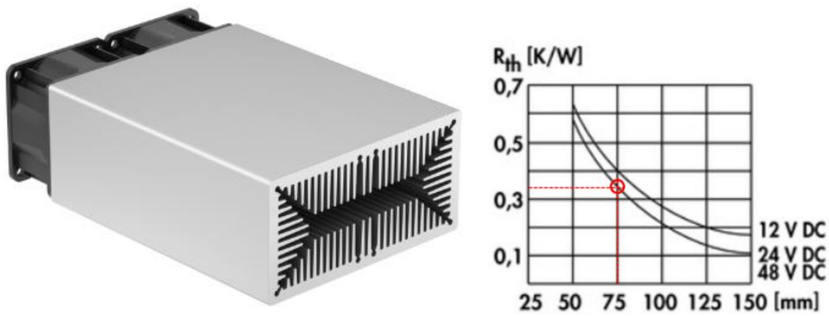


Figure 17 **Fischer Elektronik LAM 6 D 75 24 V heat sink and its thermal resistance**[2]

[1] This value was assumed to be constant and independent of other ambient parameters. In reality, this value can vary depending on the ambient temperature, thickness of coating, degree of the flow (after the face change), and other factors.

[2] *Note: To maintain the evaluation board's power supply, the heat sink's default fan was changed from ebmpapst 614 J/2HHP (P =14.6 W, output = 82 m³/h) to ebmpapst 614 NHH-119 (P =2.9 W, output = 56 m³/h). This setup worked without major performance loss during thermal testing.*

3 System and functional description

Usage of EVAL-FP50R12W2T7M5 must comply with all safety precautions and national accident prevention rules. Please read the disclaimer and safety instructions mentioned in Note: “Important notice”, Note: “Safety precautions”, and Table 1 before operating the evaluation board.

Signals dedicated to high-side driver and low-side driver must have a proper dead time. The recommended minimal dead time value is 2 µs. However, the evaluation board itself does not generate a dead time.

3.1 Installing EVAL-FP50R12W2T7M5

Before operating the evaluation board, please follow these steps:

1. Visually inspect the evaluation board to make sure all its components are assembled and undamaged.
2. Ensure that there are no bent pins.
3. Ensure a proper and straight stand for the evaluation board and use the available spacer to place the system accurately.
4. Connect the evaluation board to the auxiliary supply and check its internal supply voltages. Ensure that the gate drivers are properly supplied.
5. Connect the evaluation board to the interface connector.
6. Ensure that all the required signals are connected properly, the order of status bits is followed correctly, and the control is based on a 5 V supply.
7. Before powering the evaluation board with a high-voltage input, test if the drivers are switching correctly. For this, provide the reference PWM signals and check the drivers' performance on an oscilloscope.
8. To supply power to the system, use an AC power supply that is isolated through an isolation transformer.
9. Use a properly connected and sized motor load.

3.2 Turn-on double-pulse testing

Figure 18 illustrates the typical behavior of the IGBT during a turn-on event in double-pulse tests. The current peaks of the collector current I_C are limited and V_{GE} oscillations of the gate voltage are minimal.

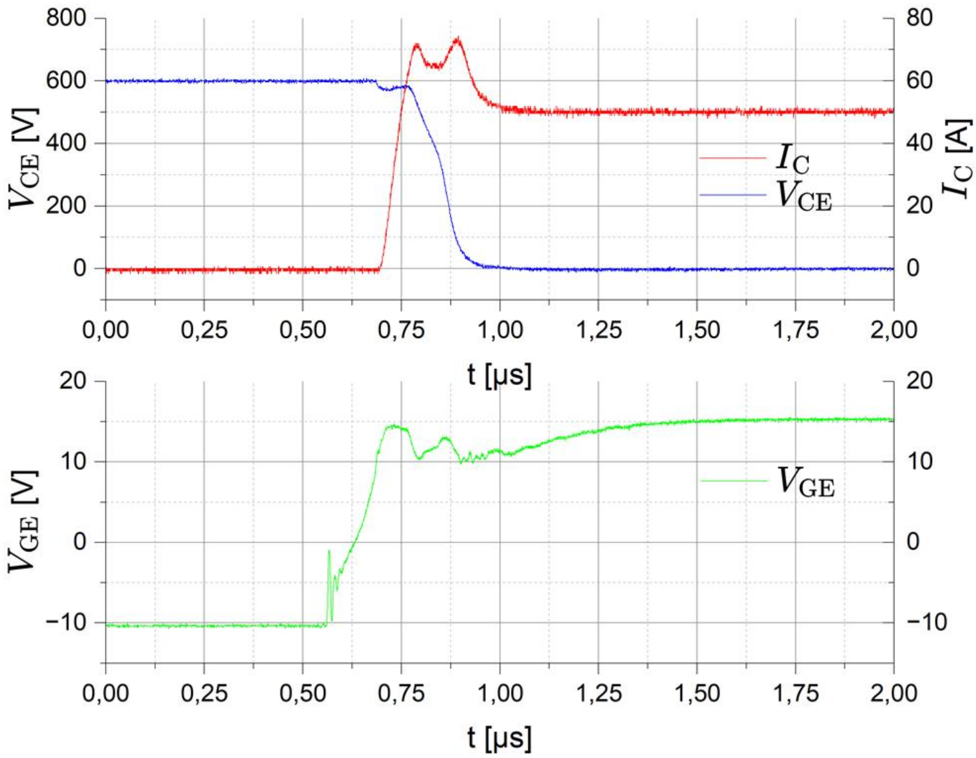


Figure 18 **Turn-on behavior low-side: I_c = 50 A, T_j = 25°C, R_{gon} = 5.1 Ω, U_{zk} = 600 V**

3.3 Turn-off double-pulse testing

Figure 19 illustrates the typical behavior of the IGBT during a turn-off event in double-pulse tests. The overshoot of the collector emitter voltage V_{CE} is limited and V_{GE} oscillations of the gate voltage are minimal.

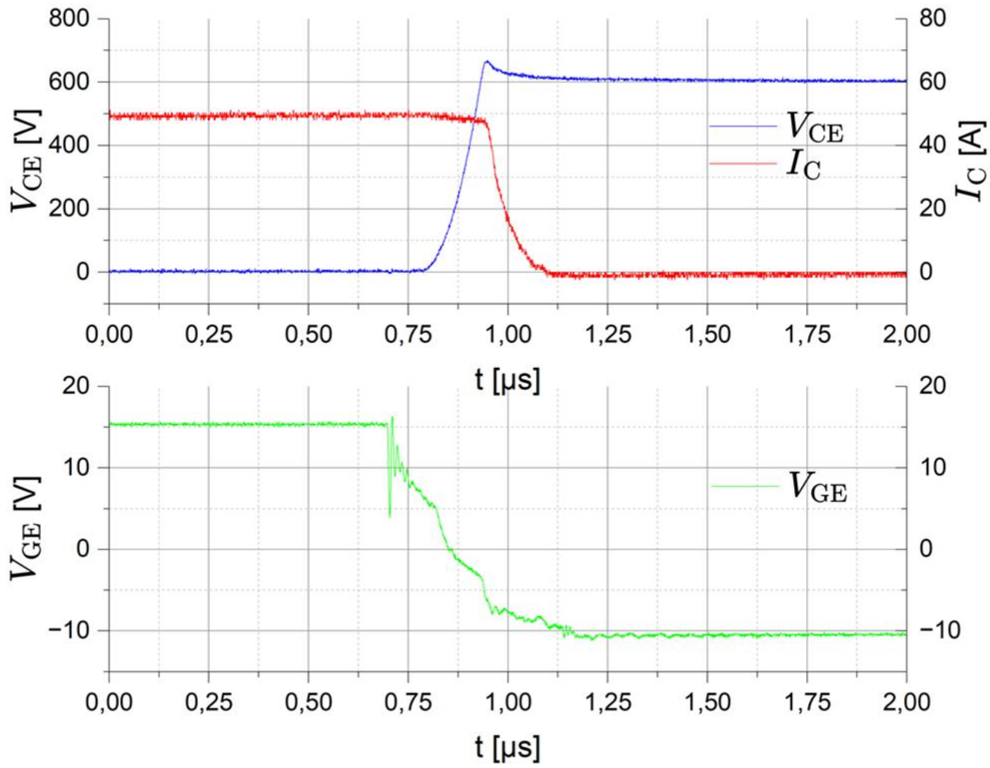


Figure 19 **Turn-off behavior low-side: I_c = 50 A, T_j = 25°C, R_{goff} = 5.1 Ω, U_{zk} = 600 V**

Table 9 Equipment used during the double-pulse tests

Measurement	Equipment	Properties
Oscilloscope	TEK TDS 5054 B/DPO7104-LAN	500 MHz
V_{CE} probe	PMK PHV 642-L |100	1/100
I_C probe	Rogowski CWTUM/1/B	30 MHz, 300 A, 20 mV/A
V_{GE} probe	TEK P6139B	500 MHz, 300 V, 8 pF, 10 MΩ, 1/10

3.4 Thermal investigations OP1 and OP2

The evaluation board EVAL-FP50R12W2T7 with the EasyPIM™ 2B has been tested thermally. The primary goal of the initial measurements was to assess the thermal performance of the evaluation board, with a focus on characterizing the first two operational points (OP1 cos(ϕ) = 0.1 and OP2 cos(ϕ) = 0.9). The EasyPIM™ 2B power module is equipped with two fiber optic temperature sensors – one dedicated to measure the chip temperature and the other to monitor the diode temperature. The setup is also equipped with a modified heat sink that includes thermocouples under the IGBT and the diode to measure the temperature drop.

To observe the temperature around the module housing and heat sink, a thermocouple was applied between the power module's spring clamps and the heat sink. The first investigations were carried out with the phase change material TIM 1.0 [3]. Afterwards, Infineon's TIM 1.0 was compared to the latest TIM 2.0. [5]

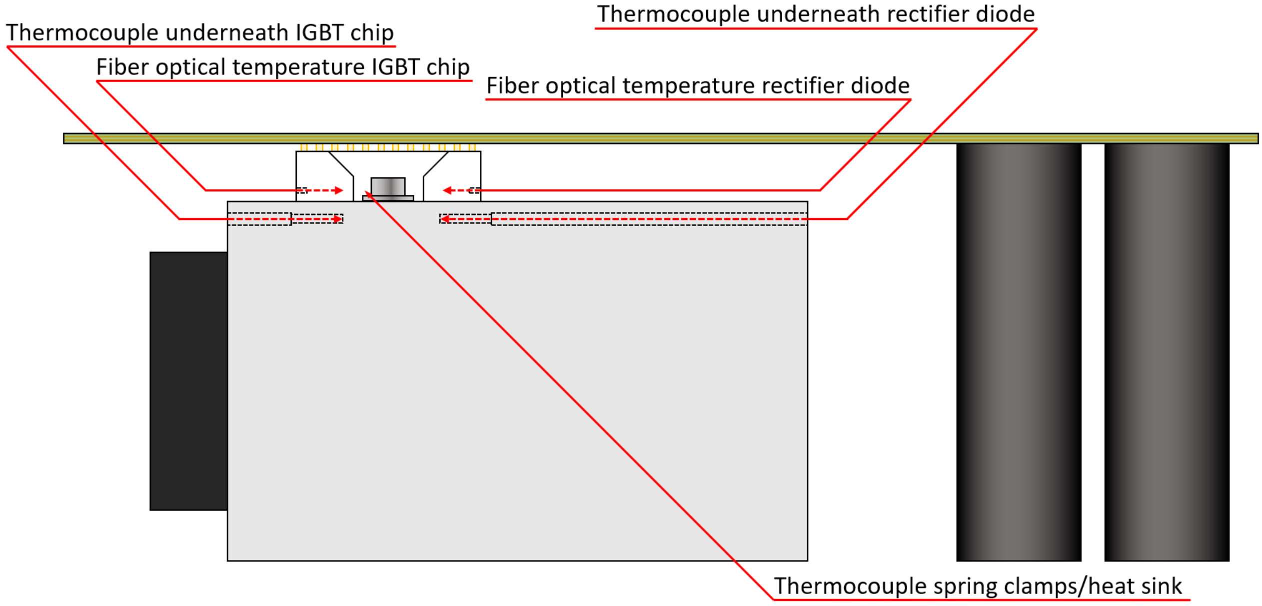


Figure 20 **Thermal investigations: Measurement setup**

3.4.1 Thermal investigation: OP1 with cos(ϕ) = 0.1

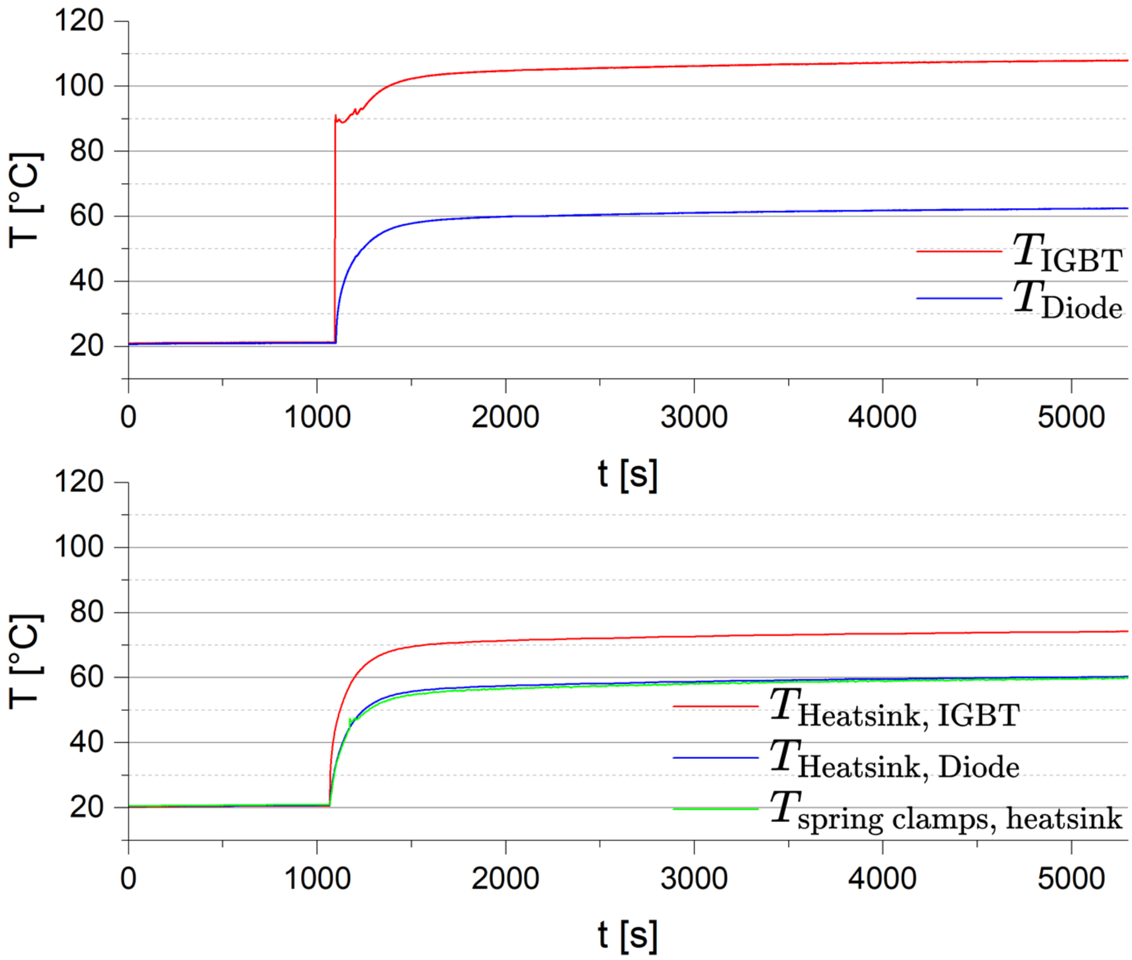


Figure 21 **Thermal investigation: OP1 with cos(ϕ) = 0.1**

Figure 21 shows the different temperature progressions for the operation condition OP1 (see Table 8). While the IGBT chip reached a maximum temperature of approximately 108°C in the stationary state, the temperature of the rectifier diode only rose to 63°C. This highlights the power losses of the predominant IGBT compared to the power losses of the rectifier diode when the evaluation board is operated at cos(ϕ) = 0.1. The temperature of the heat sink under the IGBT increased up to 76°C and of the one below the rectifier diode reached up to 61°C.

The short-term buckling at the beginning of the curve indicates the phase change of the TIM. As a result, the $R_{th,jh}$ between the module and the heat sink reduces.

3.4.2 Thermal investigation: OP2 with cos(ϕ) = 0.9

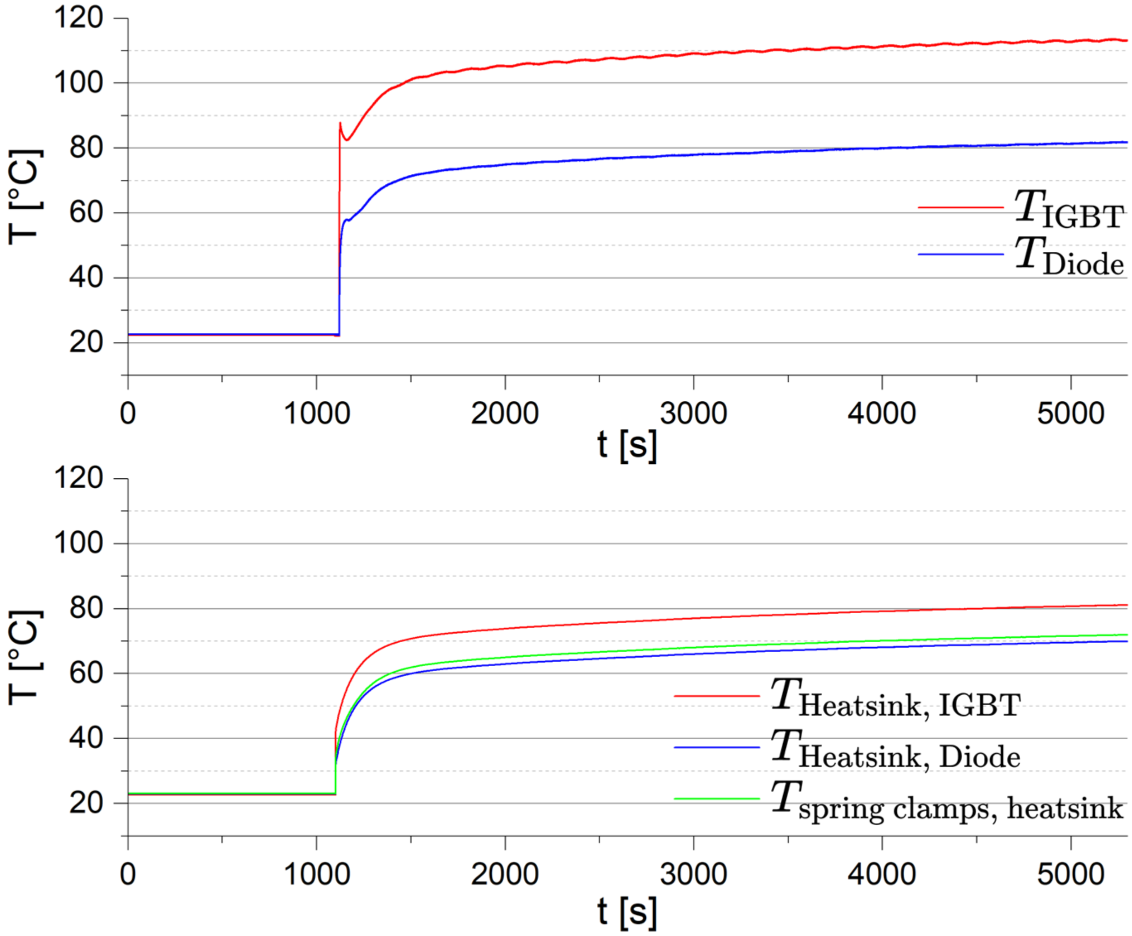


Figure 22 **Thermal investigation: OP2 with cos(ϕ) = 0.9**

The same measurement setup was repeated with OP2 and TIM was reapplied. In this case, the IGBT temperature rose to approximately 116°C while the rectifier diode's temperature increased to 84°C. The temperature of the heat sink under the IGBT reached 83°C and of the one below the rectifier diode reached up to 73°C during steady state.
According to simulation results (see Table 8), the power losses of the inverter switch (IGBT including the free-wheeling diode) with approximately 36 W remained almost unchanged between OP1 and OP2, although the IGBT losses increased slightly. However, because the conductive power losses of the free-wheeling diode also reduced at the same time, a comparable total power loss of the IGBT was obtained in both conditions.
On the other hand, the losses in the rectifier diode increased significantly from OP1 to OP2. As a result, the temperature across the entire system increased.

3.5 Comparison between TIM 1.0 and TIM 2.0

EVAL-FP50R12W2T7M5 has also been used to investigate and compare the thermal performances of TIM 1.0 and TIM 2.0. Initially, the measurement setup was built similar to the one discussed in section 3.4 (see Figure 20). Two measurements were run with different TIMs applied for OP2.

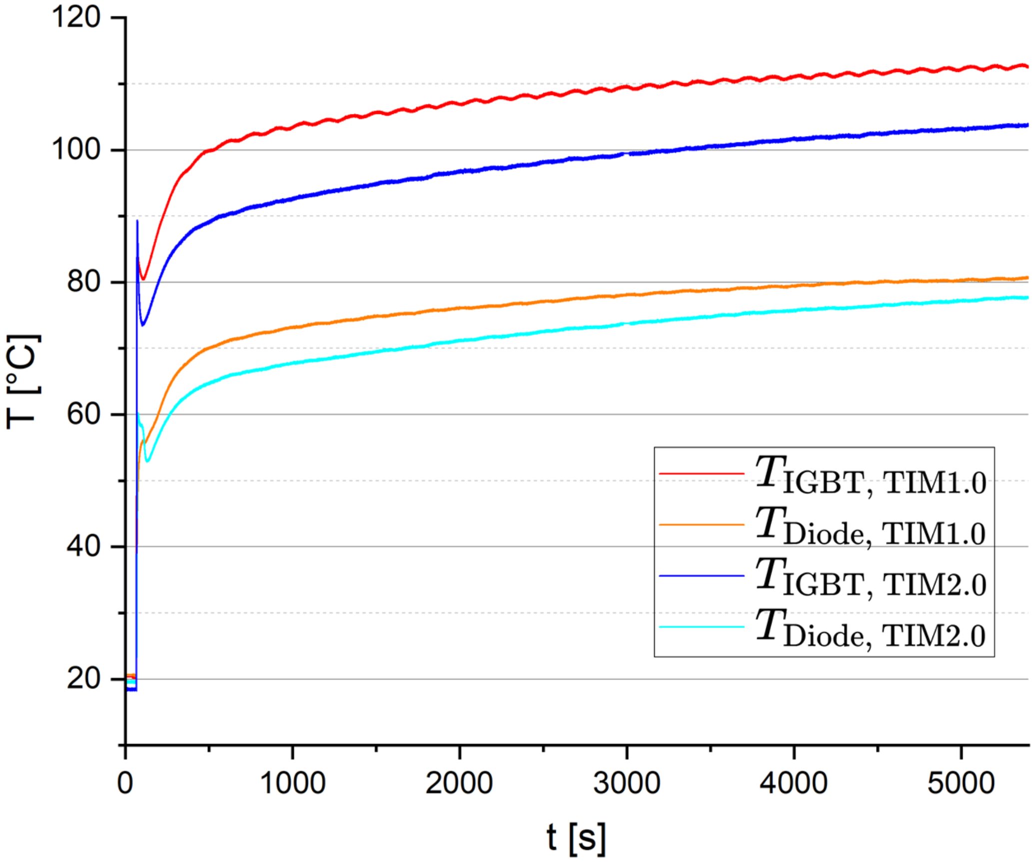


Figure 23 **Thermal investigations with OP2: TIM 1.0 versus TIM 2.0**

Fundamentally, it was observed that the phase-change of both TIM 1.0 and 2.0 took place during the turn-on event of the power module. In both the cases, the IGBT chip heated more than the rectifier diode, but the steady-state temperatures decreased with TIM 2.0.

In general, both TIM 1.0 and 2.0 showed different thermal management behavior, for example, their unique phase-change temperature and their different R_{th}.

4 References

[1] I. T. AG, AN2019-06 Modules with applied Thermal Interface Material (TIM), 81726 Munich, Germany , 2010.

[2] I. T. AG, BSC220N20NSFD MOSFET OptiMOSTM3 Power-Transistor, 200 V, 81726 München, Germany, 2018.

[3] I. T. AG, IPN95R3K7P7 MOSFET 950V CoolMOS(TM) P7 SJ Power Device, 81726 München, Germany, 2018.

[4] I. T. AG, IMBF170R1K0M1 CoolSiC™ 1700 V SiC Trench MOSFET, 81726 München, Germany, 2025.

[5] I. Rectifier, IRLML2060TRPbF HEXFET Power MOSFET, El Segundo, California 90245, USA: Infineon Technologies AG, 2012.

[6] I. T. AG, BSD235C OptiMOS™ 2 + OptiMOS™-P 2 Small Signal Transistor, 2015.

[7] I. T. AG, FP50R12W2T7_B11 EasyPIM™ module with TRENCHSTOP™IGBT7 and emitter controlled 7 diode and PressFIT / NTC, 81726 Munich, Germany, 2025.

[8] I. T. AG, 1ED44171N01B Single-channel low-side gate driver IC, 81726 Munich, Germany, 2022.

[9] I. T. AG, ICE5QSBG Quasi-Resonant Controller, 81726 Munich, Germany, 2020.

[10] I. T. AG, TLF50211EL 2.2 MHz Step-Down Regulator 500 mA, 5 V, low quiescent current, 81726 Munich, Germany, 2018.

[11] I. T. AG, Voltage Regulator TLE 4284, 81726 Munich, Germany, 2007.

[12] I. T. AG, EiceDRIVER™ 1ED332xMC12N Enhanced (1ED-F3), 81726 Munich, Germany, 2024.

[13] I. T. AG, TLE4296-2G V50, 81726 Munich, Germany, 2023.

[14] E. STANDARD, Insulation coordination for equipment within low-voltage supply systems - Part 1: Principles, requirements and tests, Brussels: CEN_CENELEC, 4/12/2020.

[15] I. T. AG, AN 2012-07 Modules with preapplied thermal interface, 81726 Munich, Germany , 2017.

[16] I. Rectifier, Application Note AN-1057 Heat sink Characteristics.

[17] I. T. AG, AN-2025-03 Pre-Applied phase change Thermal Interface Material 2.0, 81726 Munich, Germany , 2025.

Revision history

Document revision	Date	Description of changes
1.0	2025-10-27	Initial version
1.1	2025-11-17	Adjustments

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