CIPOS™ Prime AMM12SxxLB1Z: Evaluation board with dual channel gate drivers

Evaluation board for switching tests

About this document

Scope and purpose

This document outlines the evaluation board featuring the CIPOS™ Prime AMM12SxxLB1Z molded module together with EiceDRIVER™ dual-channel gate drivers. The board is designed for switching tests that tune the gate driving circuit to the requirements of the user.

The design features a low voltage (LV) inout domain and a high voltage (HV) domain. These are separated by a galvanic isolation barrier. The HV domain can handle voltages up to 840 V, matching the application use cases for HV automotive.

Intended audience

This document is intended for skilled technical staff. The technical staff must be sufficiently qualified to identify and control any hazard that arises from usage of an evaluation board connected to high voltage.

About this product group

Target applications

- On-board charger (OBC)
- Automotive HV DC-DC converter
- Power conversion AC-DC, DC-AC

Product family

- CIPOS™ Prime molded module
- EiceDRIVER™ isolated gate drivers

Evaluation board

This board is for use during the design-in process for evaluating and measuring characteristic curves, and for checking datasheet specifications.

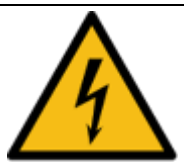
Note: PCB and auxiliary circuits are NOT optimized for final customer design. Boards do not necessarily meet the safety, EMI, and quality standard (for example UL, CE) requirements.

Evaluation board for switching tests
Safety precautions

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems

Table 1 Safety precautions

	**Warning:** The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high-voltage differential probes must be used. Failure to do so may result in personal injury or death.
	**Warning**: The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.
	**Caution:** The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.
	**Caution:** The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing, or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.
	**Caution:** The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.

Evaluation board for switching tests

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1 The board at a glance

The Eval-AMM12SSxxLB1Z-2EDR3147XQE board is designed to evaluate the 2EDR3147XQE EiceDRIVER™ dual-channel isolated gate driver ICs that drive the CIPOS™ Prime AMM12SxxLB1Z module from Infineon Technologies. The CIPOS™ Prime AMM12SxxLB1Z is a molded module in a B6 configuration. It comes with a 1200 V SiC MOSFET in different sizes ranging from nominal $R_{ds,on}$ of 18mΩ to 62mΩ.

The outer dimensions of the board are 140 x 142 mm and its thickness is 1.6 mm.

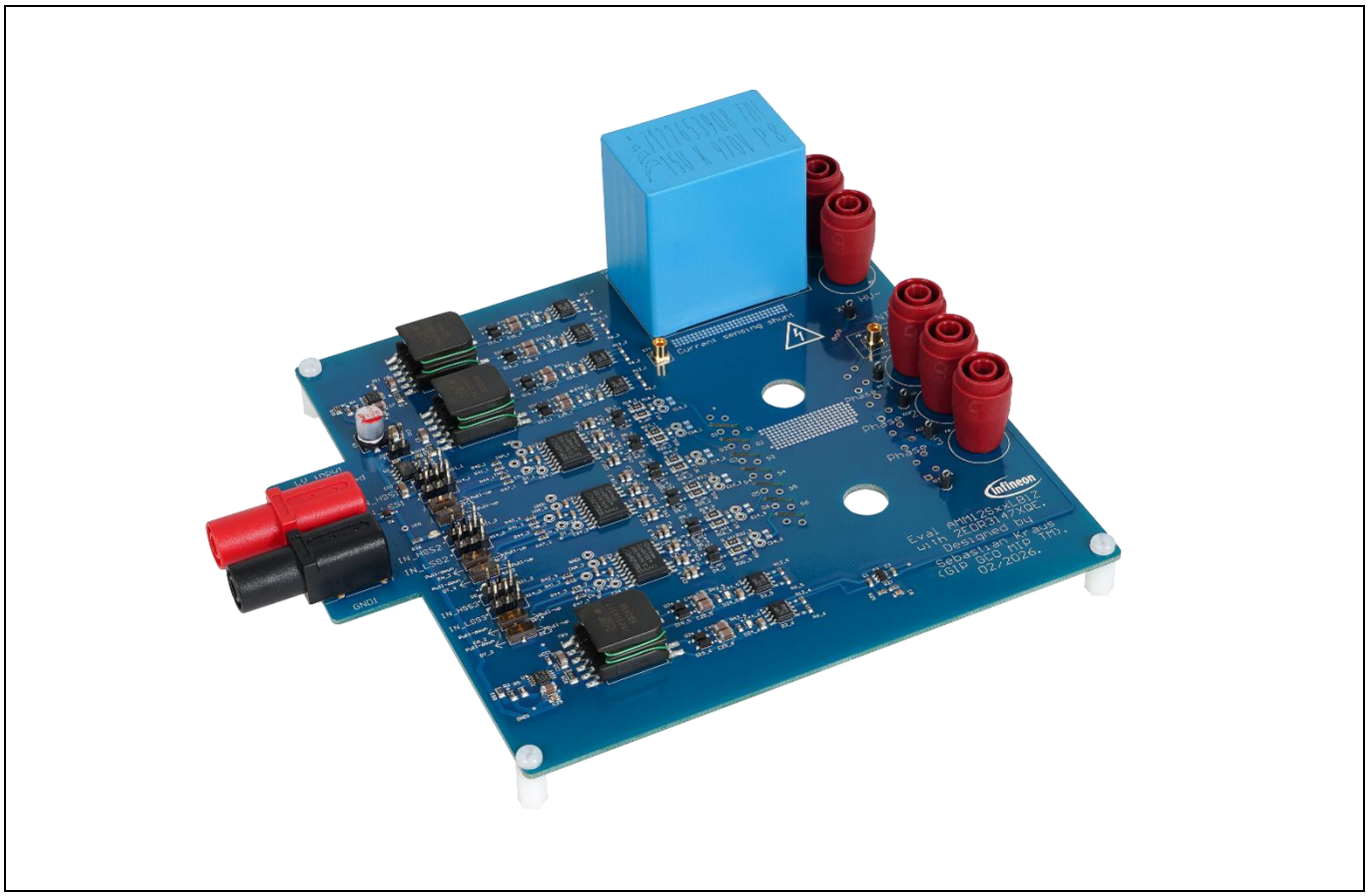


Figure 1 The Eval-AMM12SxxLB1Z-2EDR3147XQE evaluation board

1.1 Scope of supply

The delivery contains:

- The Eval-AMM12SxxLB1Z-2EDR evaluation board

Note: The evaluation board does not come with a CIPOS™ Prime module already assembled. Users can order the device of interest together with the evaluation board. Please also note that only modules following the nomenclature AMM12SxxLB1Z are compatible with the evaluation board. This nomenclature describes a module in a 6-pack configuration with xx being a placeholder indicating the nominal $R_{ds,on}$ (in mΩ) of the SiC MOSFET used.

1.2 Block diagram

Figure 2 shows the block diagram of the Eval-AMM12SxxLB1Z-2EDR evaluation board.

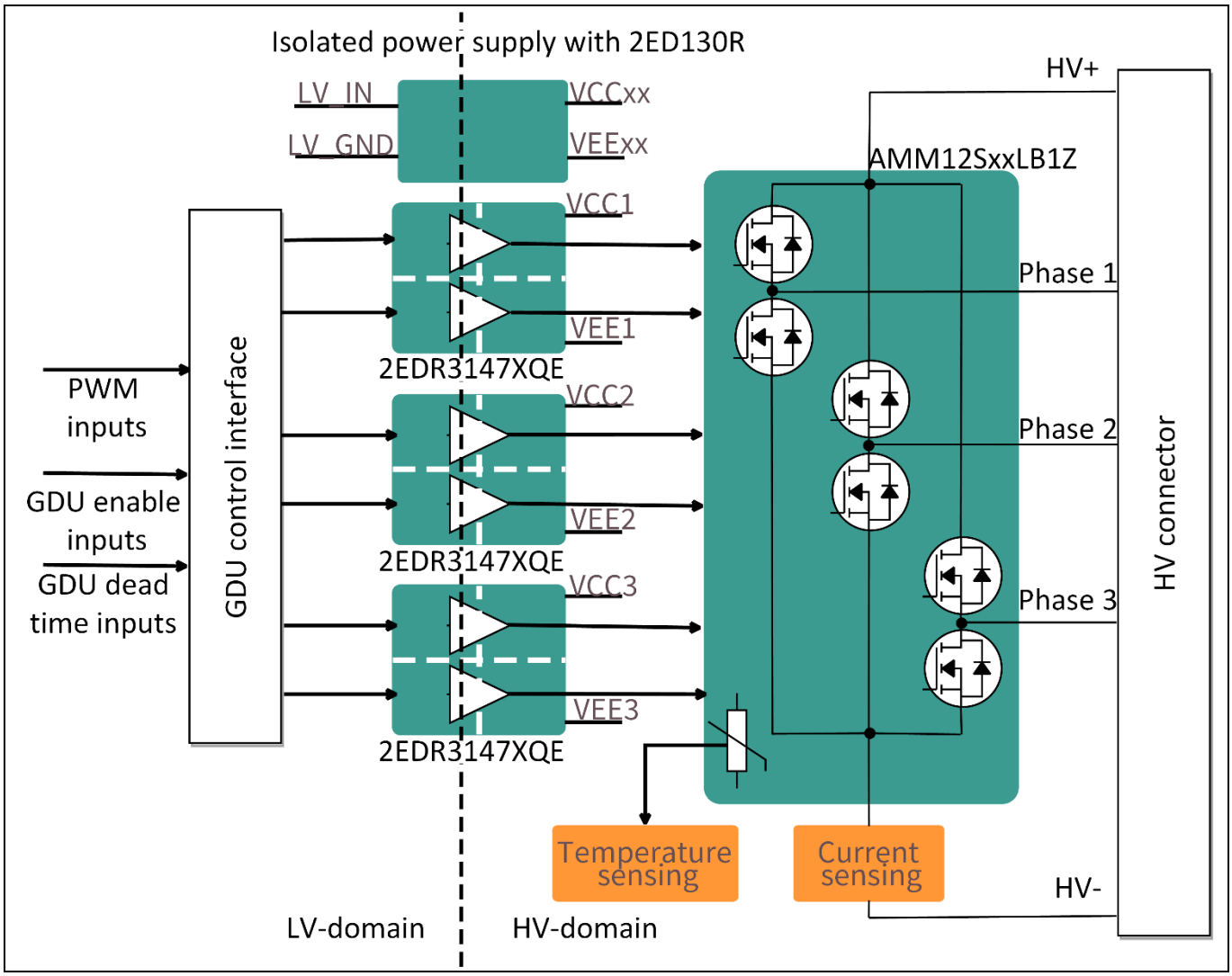


Figure 2 Eval_AMM12SxxLB1Z_2EDR block diagram

1.3 Main features

The Eval_AMM12SxxLB1Z_2EDR is an evaluation board for the CIPOS™ Prime molded module AMM12SxxLB1Z in combination with Infineon EiceDRIVER™ dual-channel gate drivers.

CIPOS™ Prime AMM12SxxLB1Z

- Molded module in a 6-pack configuration qualified for automotive applications compliant with AEC-Q101/200 and AQG 324
- Insulated package with a high performance AlN DCB substrate
- Maximum operating junction temperature T_j of 175°C
- Infineon's 2nd generation 1200 V SiC technology
- Exceptionally low switching losses

EiceDRIVER™ 2EDR3147XQE

- Dual-channel isolated gate driver
- Galvanically isolated coreless transformer gate driver
- Product validated according to AEC-Q100
- Absolute maximum supply voltage of 35 V

1.4 Board parameters and technical data

2 comprises the most important technical parameters of the board and their maximum values.

Table 2 Board parameters and ratings

Parameter	Symbol	Conditions	Value	Unit
Input-side supply voltage	VIN	Referenced to GND1	-0.3…20	V
Input-side control voltage	VCC1	Referenced to GND1	-0.3…7	V
Positive input for low-side gate driver	IN_LS_xx	Referenced to GND1	-0.3…7	V
Positive input for high-side gate driver	IN_HS_xx	Referenced to GND1	-0.3…7	V
Gate driver enable input	ENxx	Referenced to GND1	-0.3…7	V
Gate driver dead-time input	DTxx	Referenced to GND1	-0.3…7	V
Ready output for power supply	RDYxx	Ready state of the on-board power supply	-0.3…7	V
Output-side positive supply voltages	VCC2_xx	Referenced to GND2	0…20	V
Output-side negative supply voltages	VEE2_xx	Referenced to GND2	-10…0	V
DC-link voltage	VDC	Applied between HV+ and HV_GND. Limited by component ratings and design clearances	-0.2…840	V
Half-bridge mid-point connection	Phase_xx	Applied between Phase xx and HV_GND	-0.2…840	V
Switching frequency	f_{sw}	Maximum switching frequency for continuous operation. Power dissipation should be considered	100	kHz
Peak phase current	$I_{out,peak}$	Maximum pulse current in the double-pulse test	100	A
Storage temperature	T_{stg}	Storage temperature of the board	-40…125	°C
Junction temperature	T_j	Maximum junction temperature of AMM12SxxLB during operation	-40…175	°C

2 System and functional description

2.1 Getting started

EVAL_AMM12SxxLB1Z_2EDR is optimized for use with both 5 V and 3.3 V input-side supply voltage, VCC1. The board also has a linear power supply circuit that generates the 5 V or 3.3 V required for VCC1. However, it is important to note that the threshold values for the primary-side input signals are independent of the VCC1 supply voltage.

Using the board with the onboard isolated power supply for output-side supply voltages of high-side and low-side gate drivers is recommended. For a nominal input voltage, VIN, of 15 V at the LV domain, the isolated power supply provides a bipolar +18 V/-2.9 V voltage on the HV domain for both the high-side and the low-side gate drivers.

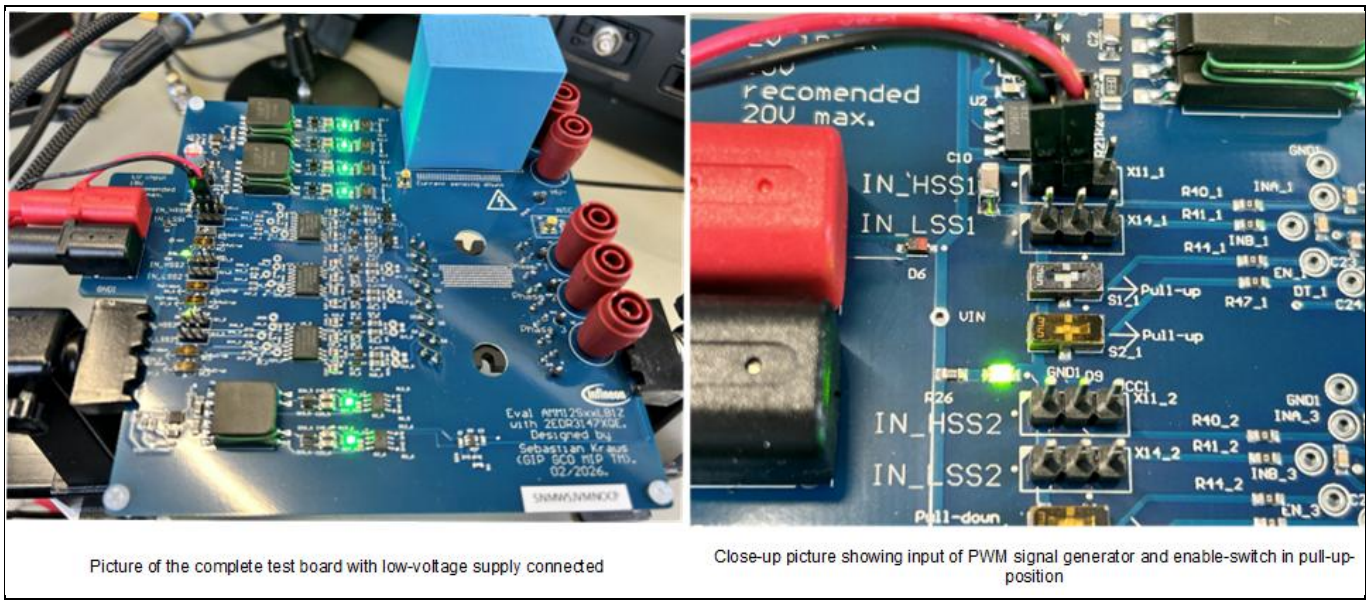
2.1.1 Prerequisites

- A low-voltage power supply for the input side on the low-voltage domain, capable of supplying >15 V and 100 mA. Connect between X1 (VIN) and X3 (GND1)
- Suitable function generator for generating a double-pulse signal. Using BNC-to-square-pin cables is recommended to inject the control signals in the evaluation board
- A high-voltage power supply for providing DC-link voltage on the high-voltage domain. Connect between X2 (HV+) and X7 (HV_GND)
- A suitable inductive load for testing the double pulse
- One AMM12SxxLB1Z device soldered to the respective footprint on the board. Users can choose the part

2.2 Power-up sequence of the board

To set up the board for double-pulse testing, follow these steps:

1. Connect the low-voltage supply to the banana jacks on the input domain of the board as shown in Fig. 3 (a).
2. Connect the positive terminal of the supply voltage to connector X1 and the ground of the supply voltage to connector X3 on the board. The recommended value of the supply voltage is 15 V and the maximum value is 20 V. The expected current consumption of the low-voltage power supply is around 75 mA.
3. All LEDs on the board should be green, indicating proper operation.
4. Connect the PWM input generator to the board as shown below in Fig. 3 (b). For example, connect the signal to the connector X14_1_2 for the high-side switch of phase 1, and connect the ground of the signal generator to connector X14_1_1.
5. Enable the gate driver of the phases that will be switched. To do this, set the slider S1_xx to position 1, that is to the right-hand side following the orientation in Figure 3. The slider S2_xx can be left in the central position.
6. Connect the high-voltage power supply that will provide the DC-link voltage during the double-pulse test. Connect the positive terminal of the high voltage to connector X2 on the board and the negative terminal of the high voltage to connector X7. Do not turn on the high-voltage power supply before taking the necessary protective measures.
7. Connect the inductive load for the double-pulse test. Connect one terminal of the load to either one of the phases, connectors X4, X5, or X6, on the board and depending on the target double-pulse configuration, connect the other terminal to either connector X2 (DC+) or connector X7 (DC-).
8. Connect the measurement instruments. Recommendations are given in section 2.3.
9. Turn on the high-voltage supply.



0Evaluation board with low-voltage supply and PWM input

2.3 Double-pulse operation: The recommended measurement setup

The measurement instruments and setup described in this section are only recommendations. Users can use their preferred instruments and setups.

A typical double-pulse test involves measuring the signals given in Table 3. An example of how to connect a differential probe to the board for measuring the gate-source voltage is shown in Fig. 4.

Table 3 Double-pulse signals and measurement instruments

Signal	Description	Measurement instrument
V_{DS}	Drain-source voltage of the active switch	HV passive probe, e.g., PMK PHV 1000 Differential probe, e.g., PMK BumbleBee®
i_s	Switched current, source current of the active switch	Current measurement shunt with PMK FireFly®, Rogowski coil PEM CWT Ultramini series
V_{GS}	Gate-source voltage of the active switch	Optically isolated differential probe, e.g., PMK FireFly®
$V_{GS,fw}$	Gate-source voltage of the freewheeling switch	Optically isolated differential probe, e.g., PMK FireFly®

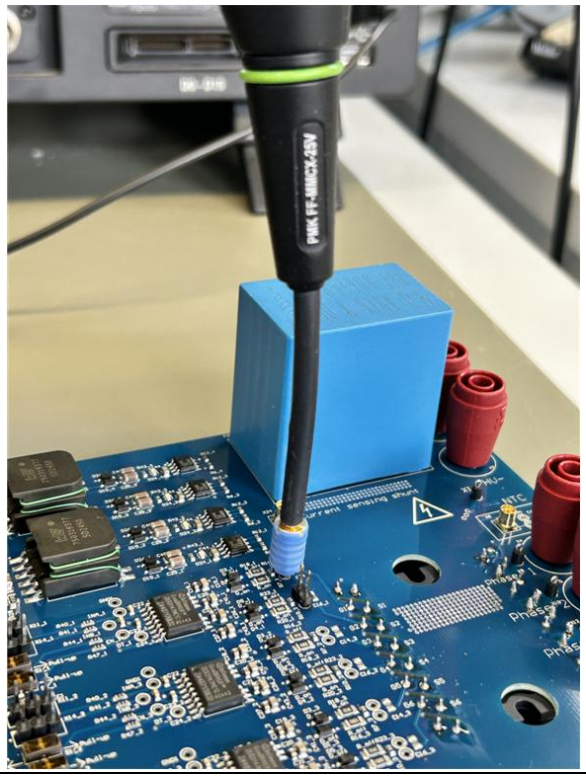


Figure 3 Example for connecting a differential probe to the gate-source test points

2.4 Modifying the gate driver's supply voltage

The isolated gate driver supply is generated from the low-voltage input, V_{IN}, by the 2EP130R transformer driver and the secondary-side rectifier stages. The negative rail, V_{EE}, is set by the open-loop, transformer-driver operating point. The positive rail, V_{CC}, is additionally regulated on each secondary side by the TLS805B1SJV adjustable LDO. The calculator file can be used to estimate the resulting V_{CC} and V_{EE} values before changing the component values. Ensure that V_{IN} does not exceed 20 V.

2.4.1 Modifying V_{EE}

V_{EE} is generated directly by the open-loop isolated supply. It is therefore influenced by the low-voltage input supply, V_{IN}, and by the configured duty cycle of 2EP130R. For the peak-rectified topology used on this board, the ideal negative rail can be estimated using [2]:

$$V_{EE} = 2 \cdot V_{IN} \cdot (-D) / TTR + V_F$$

Equation 1 Calculating V_{EE}

Here, D is the duty cycle at OUT1, TTR is the transformer turns ratio, and V_F is the rectifier-diode, forward-voltage assumption. Increasing V_{IN} makes V_{EE} more negative, and decreasing V_{IN} makes V_{EE} less negative. V_{IN} must remain within the allowed board input range and must not exceed 20 V.

Alternatively, V_{EE} can be modified by changing the duty-cycle set resistor connected from the DC pin of 2EP130R to GND. The duty cycle is selected in discrete 1% steps – from 10% to 50% – using the E96 resistor values listed for the 2EP1xxR family [2]. A larger duty cycle makes V_{EE} more negative, while a smaller duty cycle makes V_{EE} less negative. For the nominal board configuration, R4 and R5 are 698 Ω, which gives D = 14% and results in V_{EE} = −2.6 V at V_{IN} = 15 V or V_{EE} = −3.2 V at V_{IN} = 18 V approximately, when TTR = 1.4:1 and V_F = 0.4 V.

2.4.2 Modifying V_{CC}

The positive gate driver rail V_{CC} is regulated on each secondary side by the TLS805B1SJV adjustable LDO. The output voltage is set by the resistor-divider from the regulator output Q to ADJ and from ADJ to GND. On this board, R6_x is the lower resistor R2 and is fitted with 10 kΩ. R12_x is the upper resistor R1 and is fitted with 140 kΩ for the default setting of 18 V.

The regulated V_{CC} value can be calculated using the following equation:

$$V_{CC} = (R1 + R2) / R2 \cdot 1.2\ V$$

Equation 2 Calculating the regulated V_{cc}

With R2 = 10 kΩ, use R1 = 115 kΩ to set V_{CC} to 15 V, and use R1 = 140 kΩ to set V_{CC} to 18 V. The 18 V option is the default configuration. It matches the nominal, isolated supply setting used for the SiC MOSFET double-pulse testing. Use the 15 V option when a lower positive gate-drive voltage is required by the device under test (DUT) or by the test plan.

Before selecting a regulated V_{CC} setting, ensure that the raw positive rail generated by the transformer-driver remains high enough for the LDO to regulate under the intended load condition. If V_{IN} or the duty cycle is changed to modify V_{EE}, recalculate the raw V_{CC} margin as well, because both rails are generated by the same isolated supply.

2.5 Monitoring temperature

CIPOS™ Prime features an integrated resistor with a negative temperature coefficient (NTC) for measuring temperature. The evaluation board provides external circuitry for convenient read-out of the temperature shown in Fig. 9. The voltage regulator, G3, provides a stable 5 V reference from the isolated, gate driver supply voltage on the secondary side. This 5 V reference is connected to the first output terminal of the NTC resistor through a 4.7 kΩ resistor. The second terminal of the NTC resistor is connected to the ground of the 5 V reference. The voltage proportional to the temperature can be measured either at connector X8 or between test points TP1 and TP2 conveniently. The complete look-up table that shows the relationship between the temperature in °C, the nominal resistance of the NTC in kΩ, and the measured voltage in V is available in Appendix A.

3 System design

3.1 Schematics

This section contains the schematics of the evaluation board.

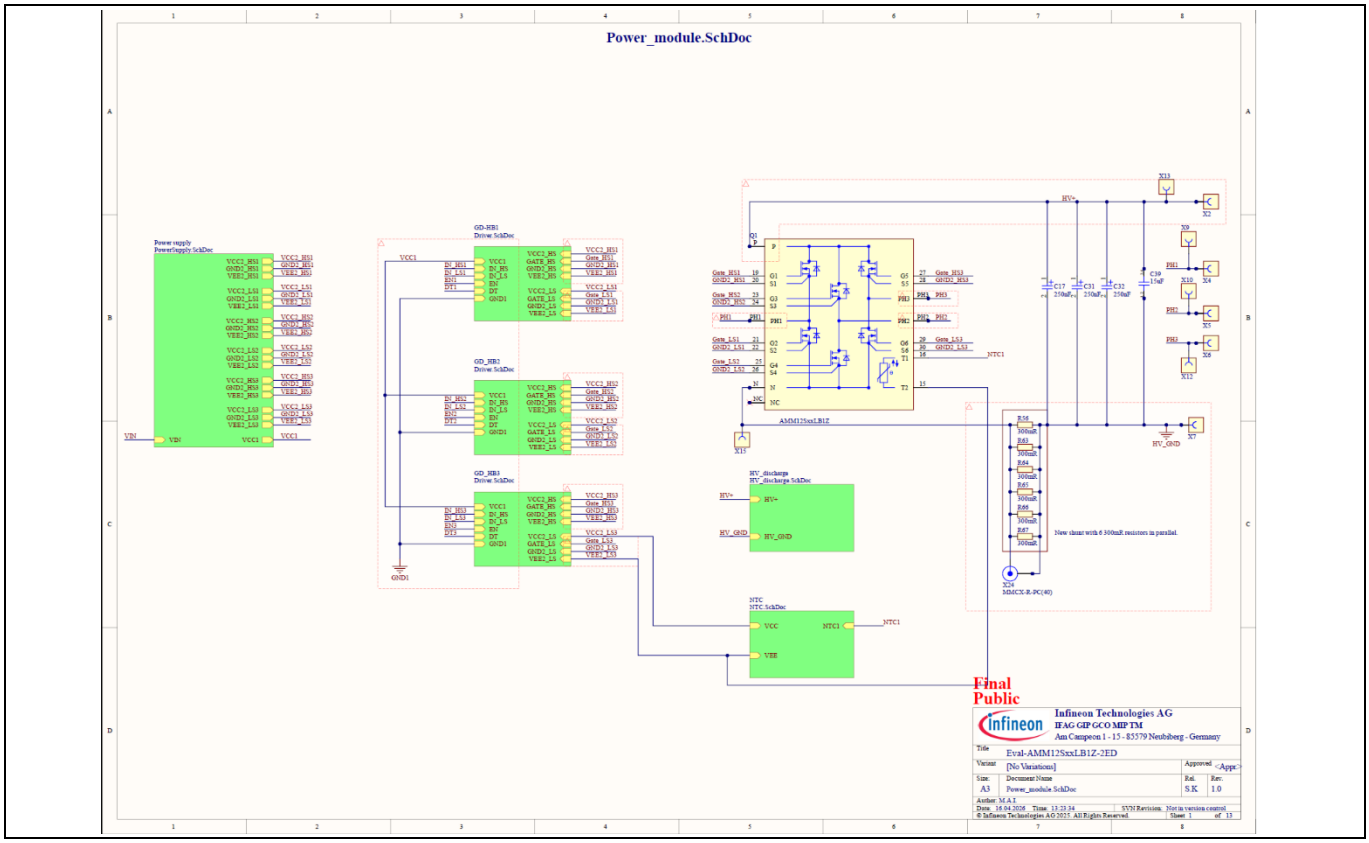


Figure 4 Schematic main sheet

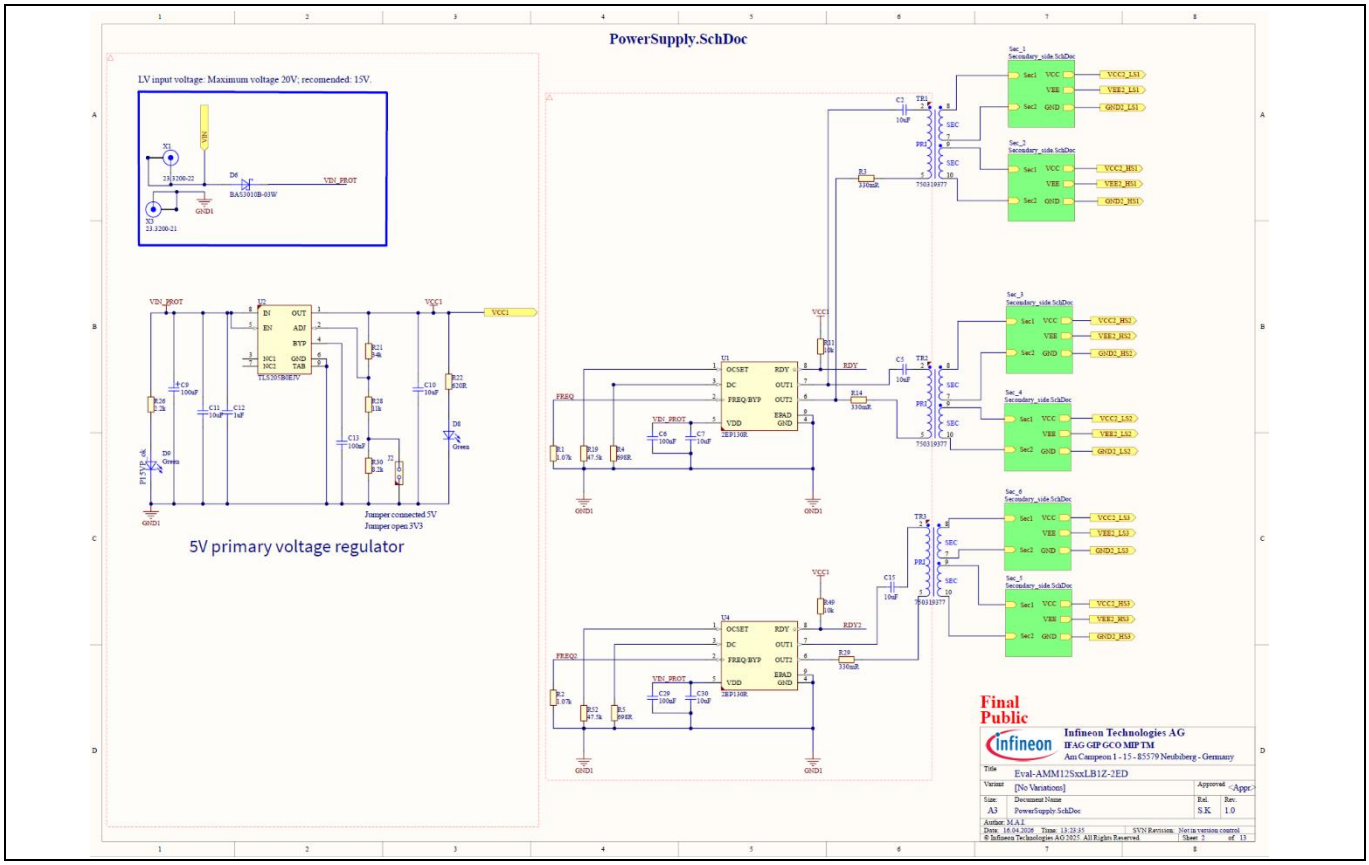


Figure 5 Schematic of the input side and power supply

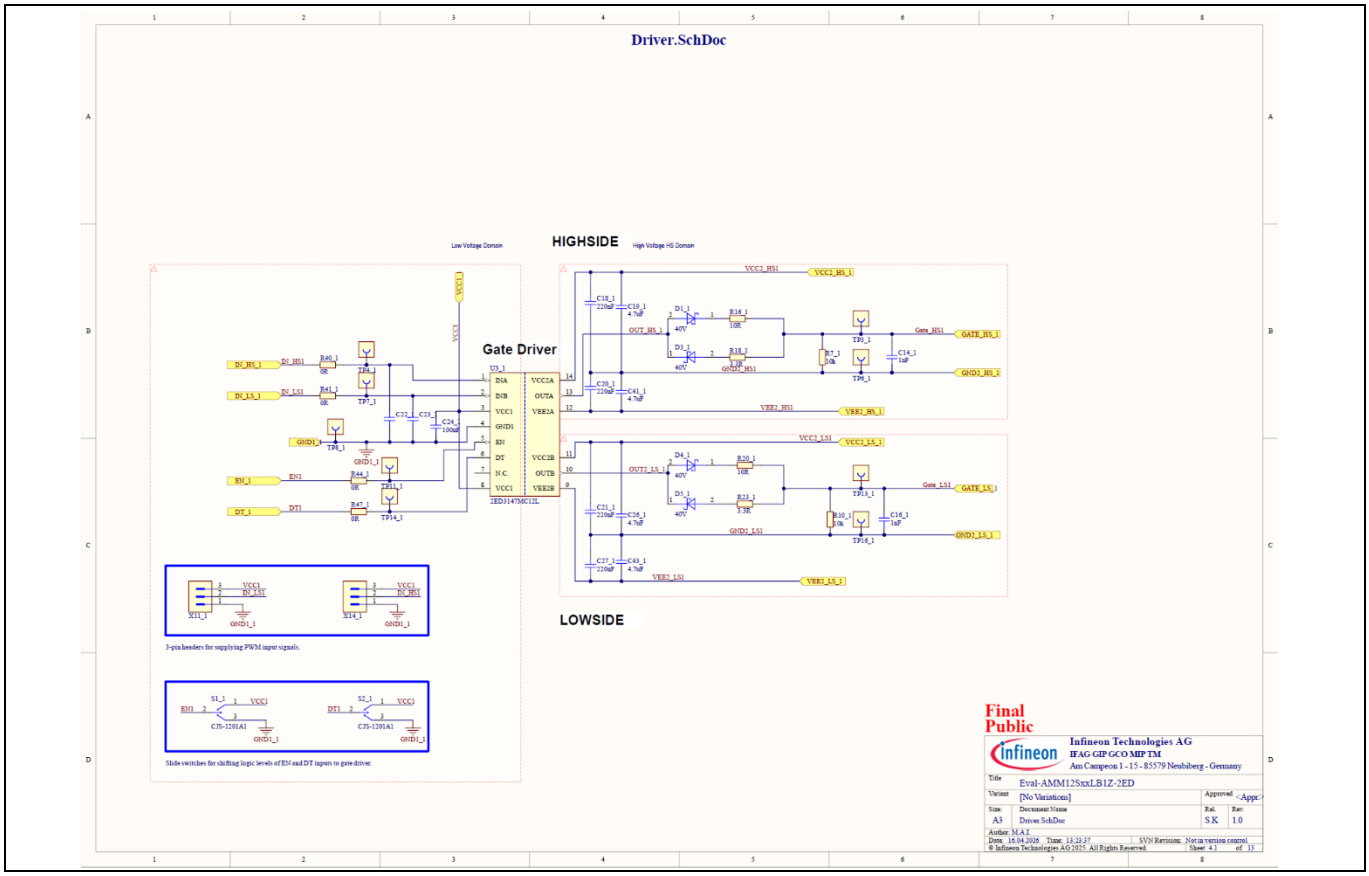


Figure 6 The gate driver schematic

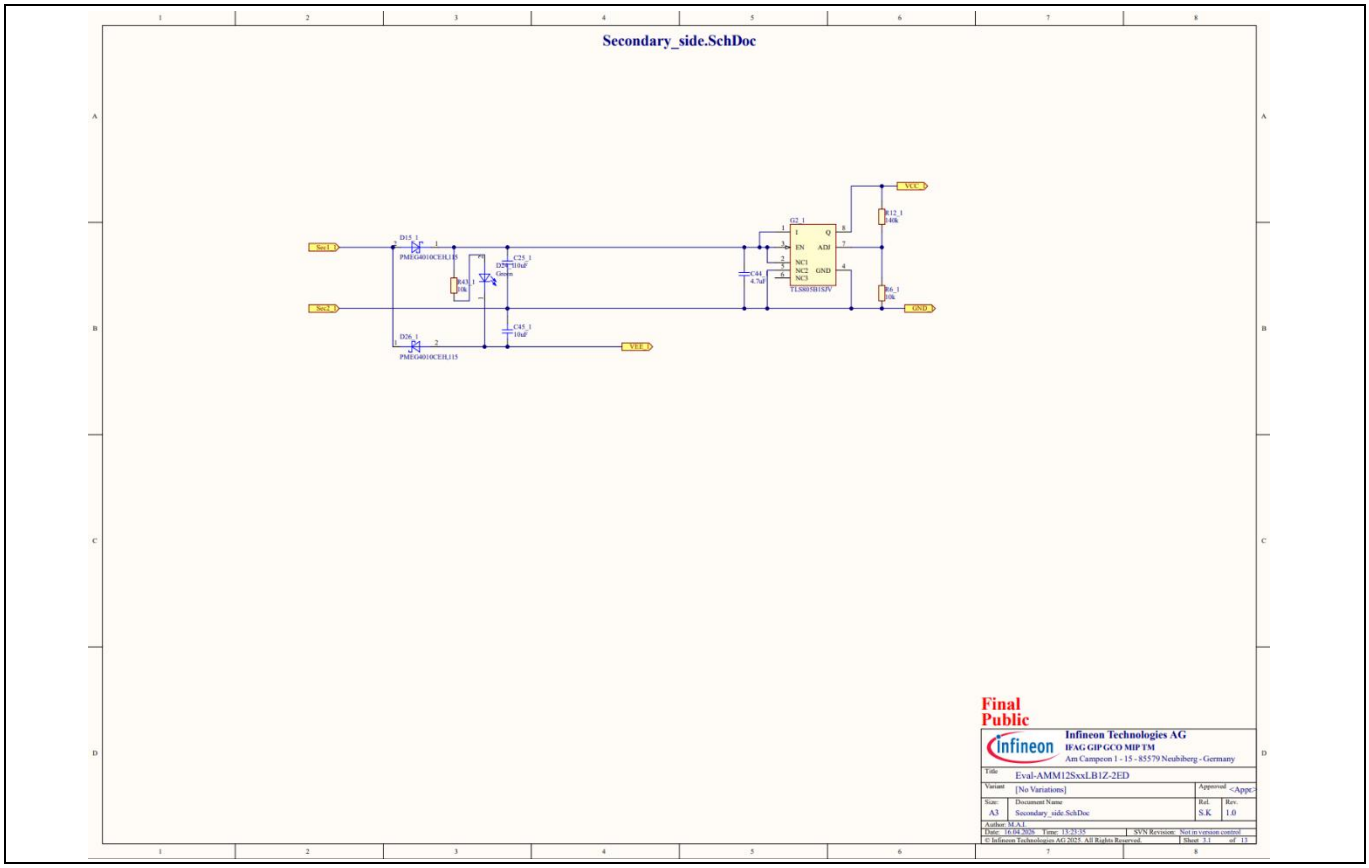


Figure 7 The secondary-side schematic of the transformer

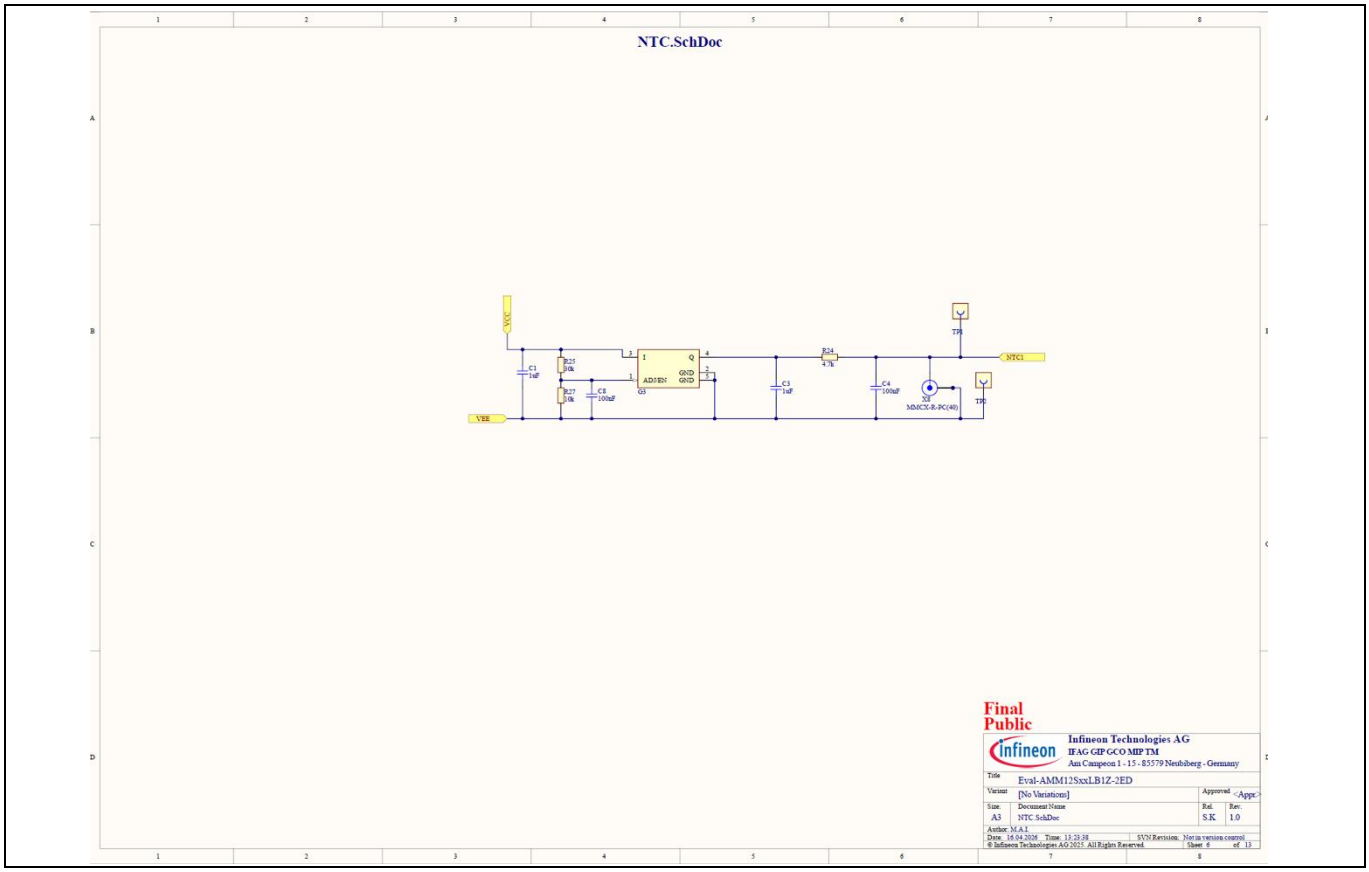


Figure 8 The NTC schematic

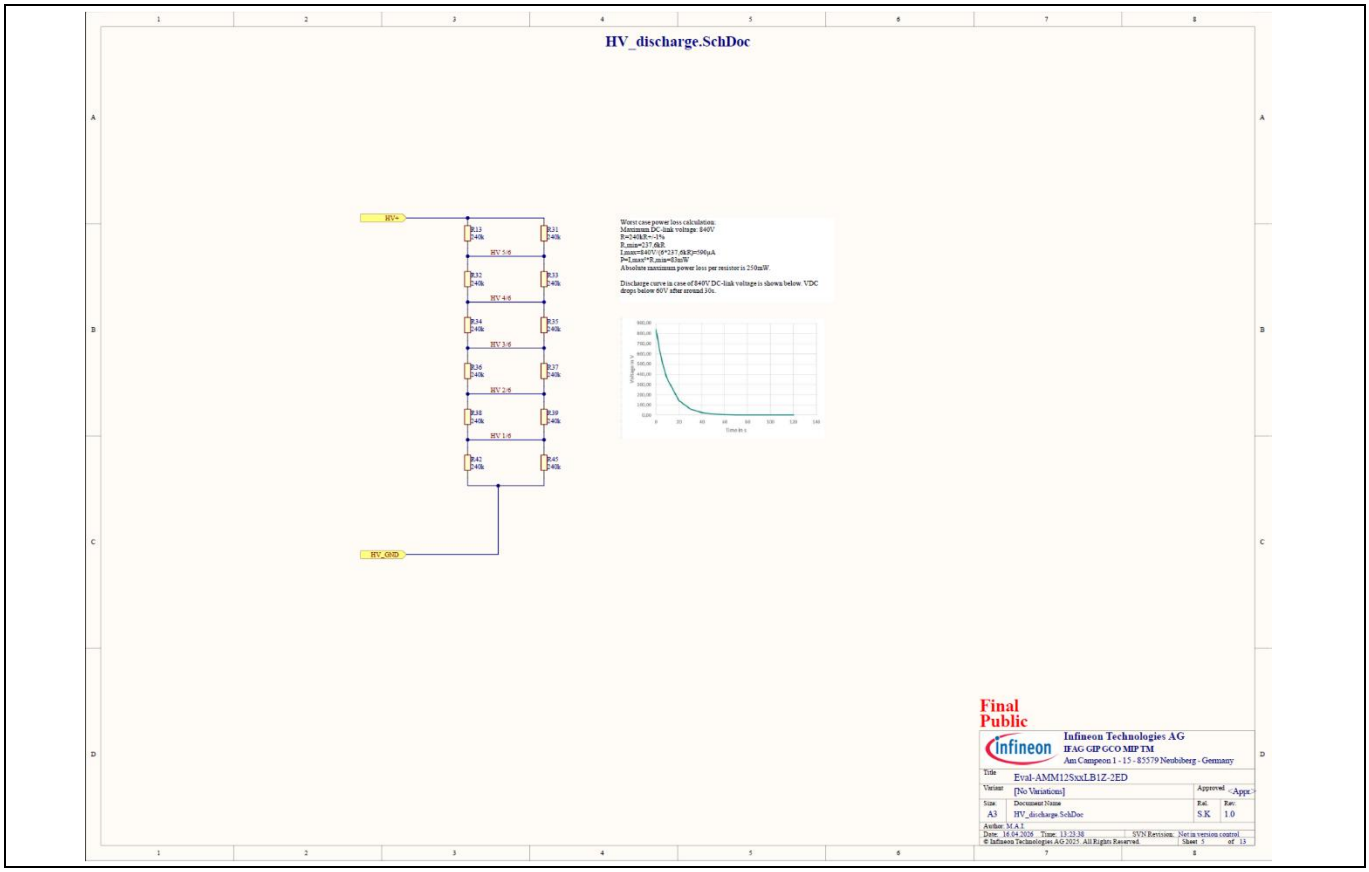


Figure 9 The HV discharge schematics

3.2 Layout

The evaluation board EVAL_AMM12SxxLB1Z_2EDR uses a four-layer PCB with 35 µm thick copper layer. This section contains images of the top and bottom layers as well as the copper layers.

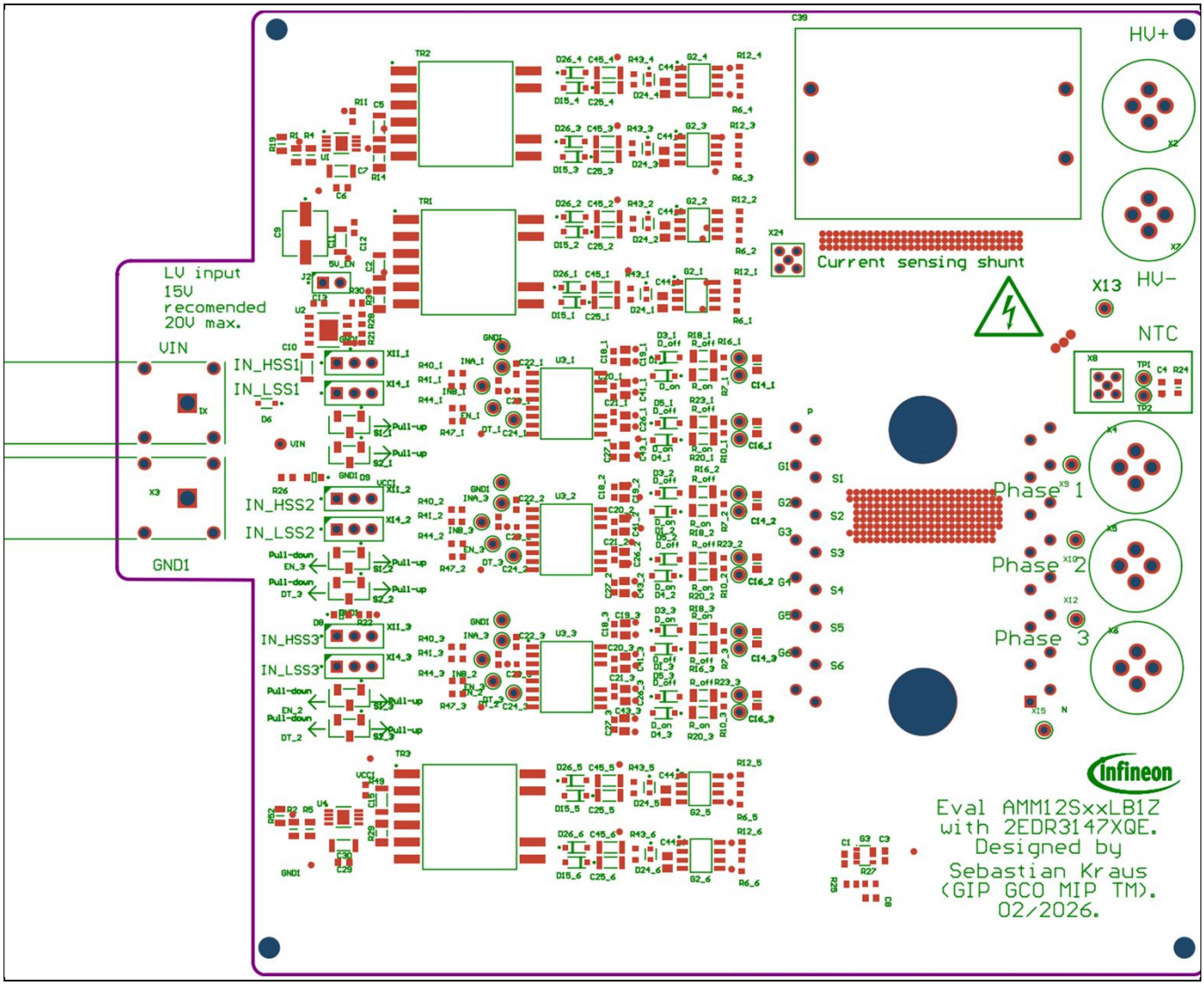


Figure 10 Top layer of the PCB

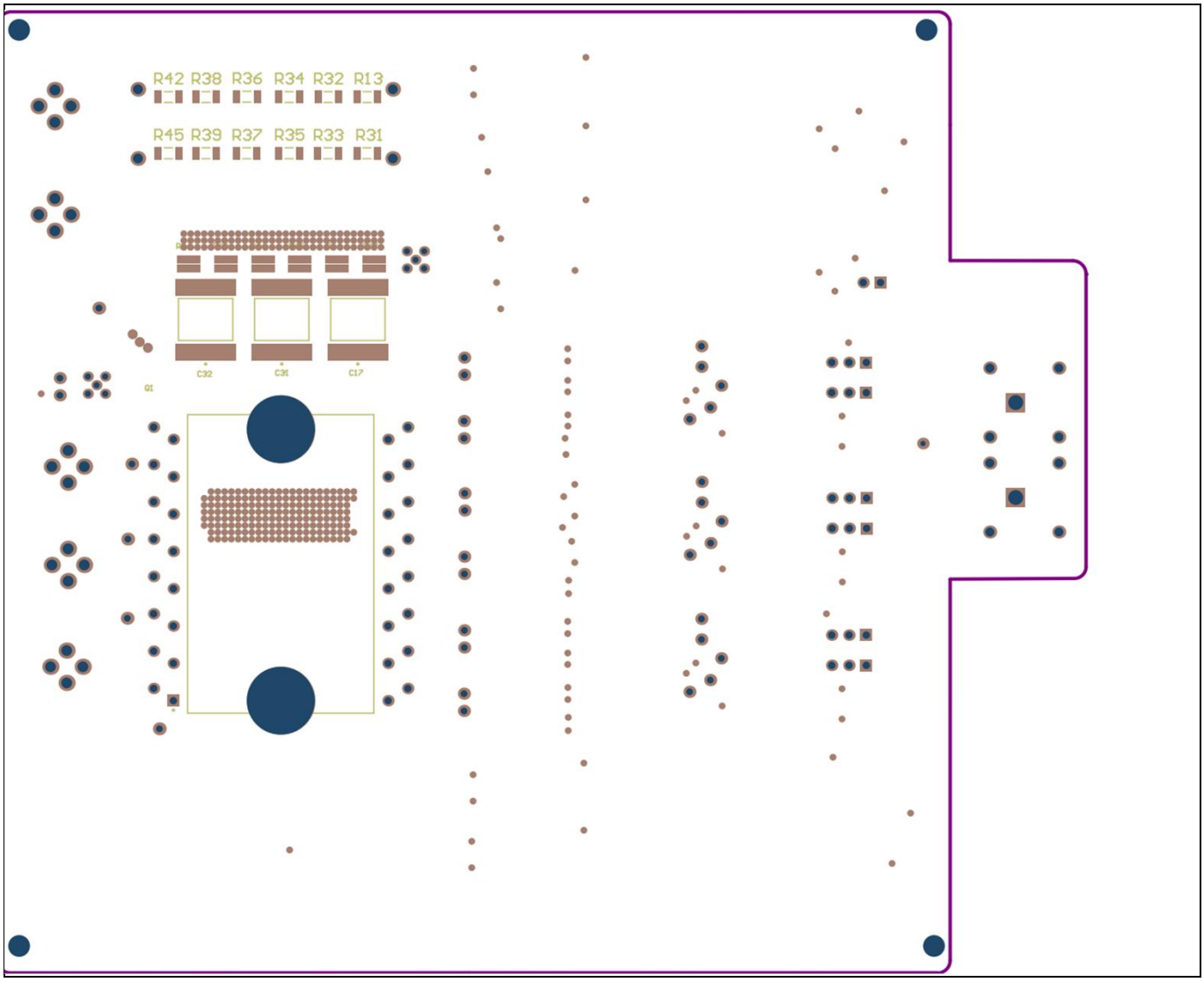


Figure 11 Bottom layer of the PCB

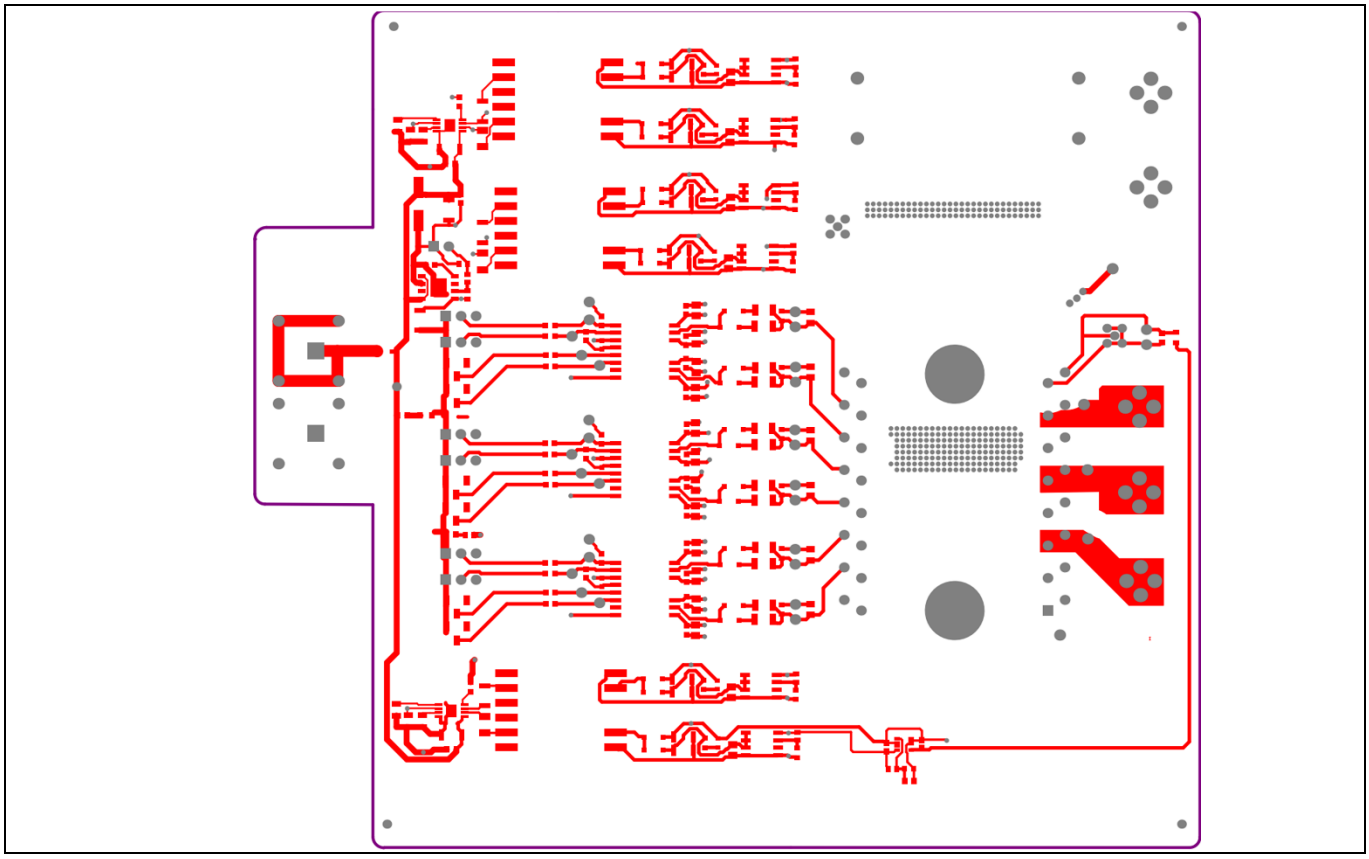


Figure 12 Top copper layer of the PCB

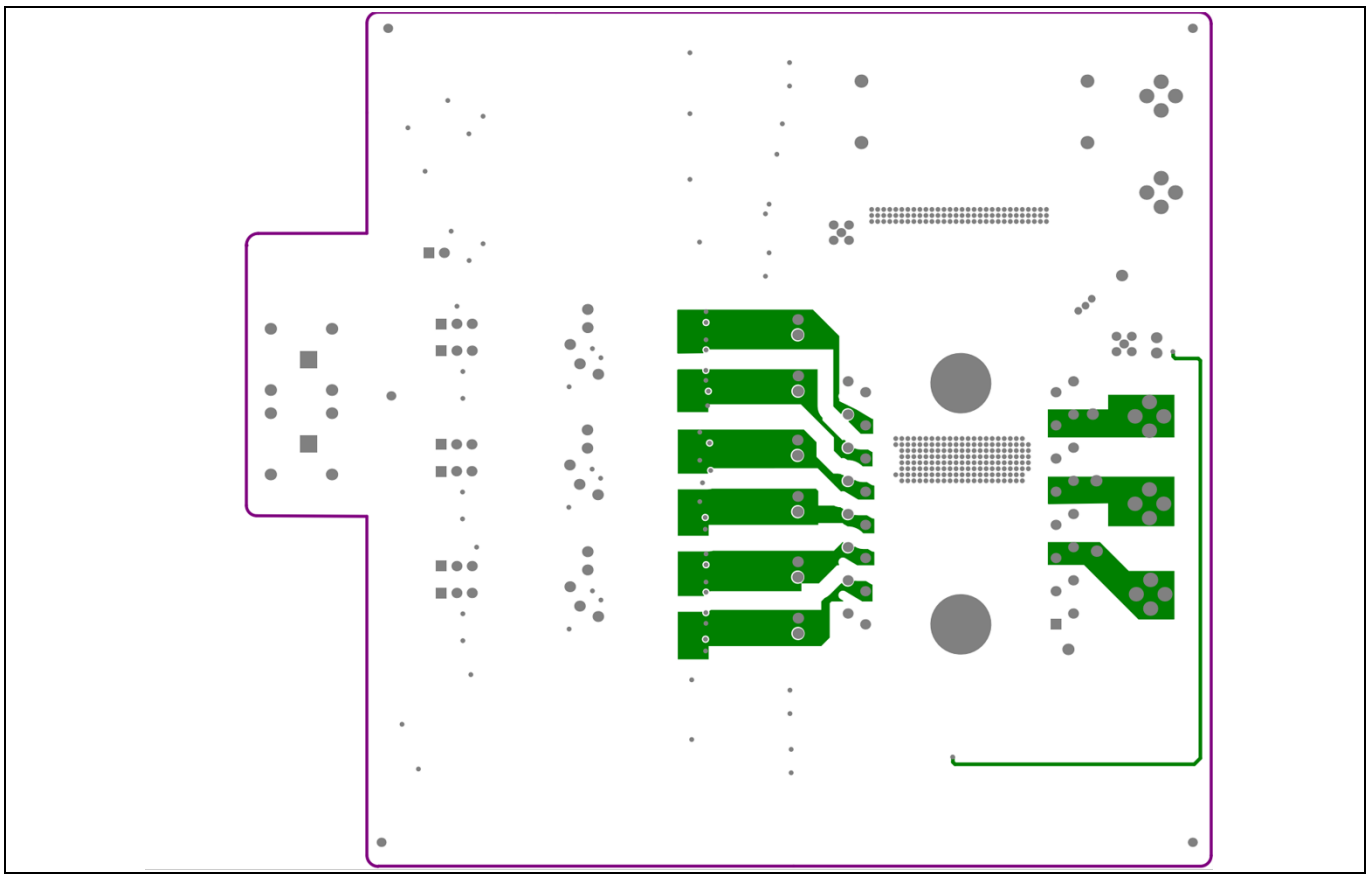


Figure 13 Inner copper layer 1 of the PCB

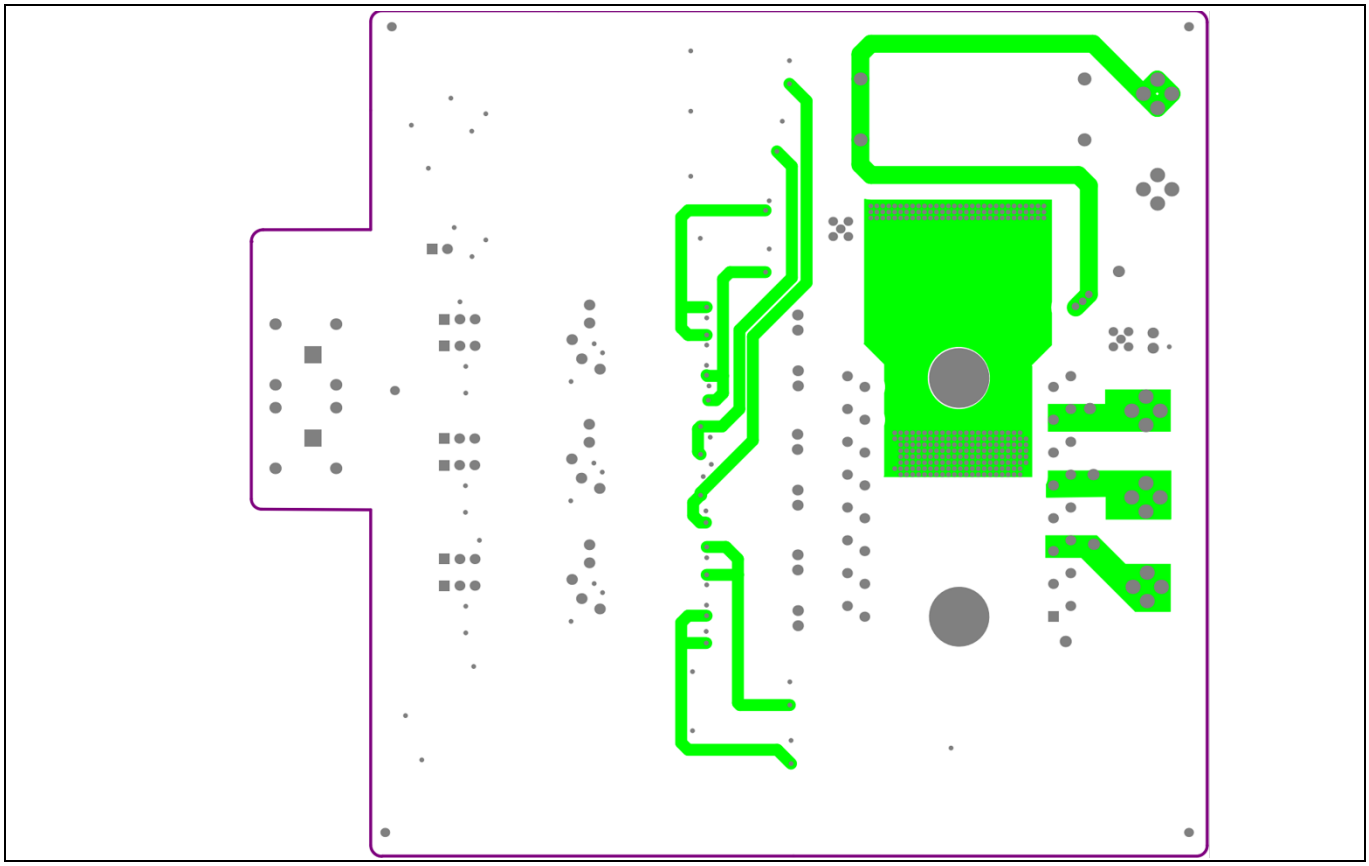


Figure 14 Inner copper layer 2 of the PCB

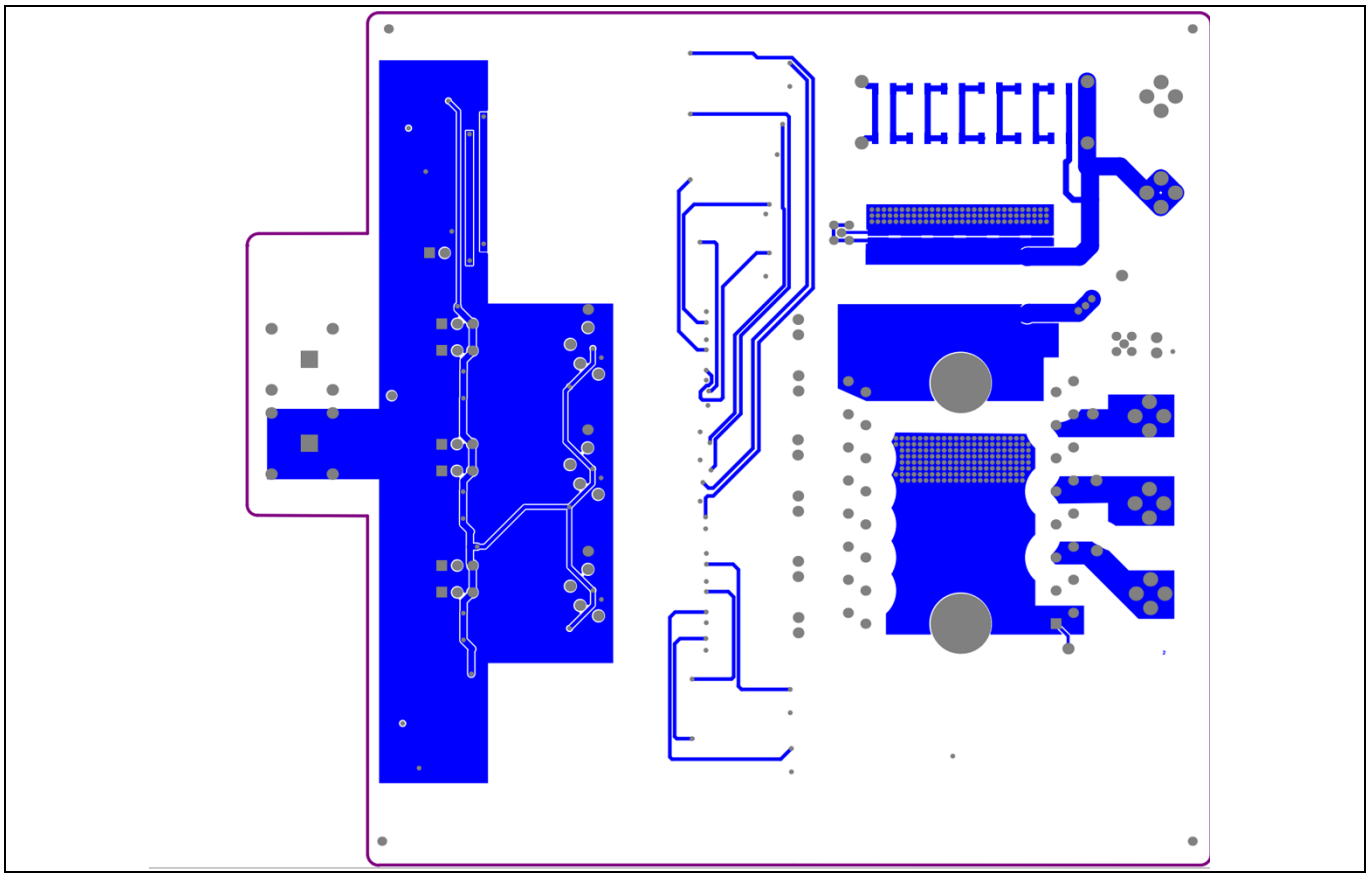


Figure 15 Bottom copper layer of the PCB

3.3 Bill of materials

The complete bill of materials is available in the download section of Infineon's website. Login credentials are required to access and download the information.

Table 4 Bill of materials

Designator	Quantity	Description	Manufacturer	Manufacturer P/N
C1, C3	2	1 uF	TDK Corporation	C1608X7R1E105K080AB
C2, C5, C7, C10, C11, C15, C25_1, C25_2, C25_3, C25_4, C25_5, C25_6, C30, C45_1, C45_2, C45_3, C45_4, C45_5, C45_6	19	10 uF	TDK Corporation, Würth Elektronik	C3216X7R1H106K160AC, 885012208069
C4, C6, C8, C29	4	100 nF	MuRata, AVX	GRM188R71E104KA01, 06035C104K4Z2A
C9	1	100 uF	Würth Elektronik	865090445008
C12	1	1 uF	Würth Elektronik	885012106022
C13	1	100 nF	Würth Elektronik	885012206120
C14_1, C14_2, C14_3, C16_1, C16_2, C16_3	6	1 nF	MuRata	GRM216R71H102MA01
C17, C31, C32	3	250 nF	TDK Corporation	B58031I9254M062
C18_1, C18_2, C18_3, C20_1, C20_2, C20_3, C21_1, C21_2, C21_3, C27_1, C27_2, C27_3	12	220 nF	MuRata	GCJ188R91H224KA01D
C19_1, C19_2, C19_3, C26_1, C26_2, C26_3, C41_1, C41_2, C41_3, C43_1, C43_2, C43_3, C44_1, C44_2, C44_3, C44_4, C44_5, C44_6	18	4.7 uF	TDK Corporation	C2012X7R1H475K125AC
C22_1, C22_2, C22_3, C23_1, C23_2, C23_3	6	1 nF	Würth Elektronik	885012206059
C24_1, C24_2, C24_3	3	100 nF	Würth Elektronik	885012206095
C39	1	15 uF	TDK Corporation	B32776H0156K000
D1_1, D1_2, D1_3, D3_1, D3_2, D3_3, D4_1, D4_2, D4_3, D5_1, D5_2, D5_3	12	40 V	Nexperia	PMEG4010CEH,115
D6	1	BAS3010B-03W	Infineon Technologies	BAS3010B-03W
D8, D9	2	Green	Würth Elektronik	150080VS75000
D15_1, D15_2, D15_3, D15_4, D15_5, D15_6,	12	PMEG4010CEH,115	Nexperia	PMEG4010CEH,115

Designator	Quantity	Description	Manufacturer	Manufacturer P/N
D26_1, D26_2, D26_3, D26_4, D26_5, D26_6				
D24_1, D24_2, D24_3, D24_4, D24_5, D24_6	6	Green	Kingbright Electronic Co.	APHD1608LCGCK
G2_1, G2_2, G2_3, G2_4, G2_5, G2_6	6	TLS805B1SJV	Infineon Technologies	TLS805B1SJV
G3	1	TLE4250-2G	Infineon Technologies	TLE4250-2G
J2	1	61300211121	Würth Elektronik	61300211121
R1, R2	2	1.07 k	Vishay	CRCW08051K07FK
R3, R14, R29	3	330 mR	Bourns	CRM1206-FX-R330 E LF
R4, R5	2	698 R	Vishay	CRCW0805698RFK
R6_1, R6_2, R6_3, R6_4, R6_5, R6_6, R7_1, R7_2, R7_3, R10_1, R10_2, R10_3, R27, R43_1, R43_2, R43_3, R43_4, R43_5, R43_6	19	10 k	Yageo, Panasonic	RC0603FR-0710KL, ERJUP3F1002V
R12_1, R12_2, R12_3, R12_4, R12_5, R12_6	6	140 k	Vishay	CRCW0603140KFK
R13, R31, R32, R33, R34, R35, R36, R37, R38, R39, R42, R45	12	240 k	Vishay	CRCW1206240KFK
R16_1, R16_2, R16_3, R20_1, R20_2, R20_3	6	10 R	Stackpole Electronics	RMCF1206FT10R0
R18_1, R18_2, R18_3, R23_1, R23_2, R23_3	6	3.3 R	Vishay	CRCW12063R30FK
R19, R52	2	47.5 k	Vishay	CRCW080547K5FK
R21	1	34 k	Vishay	CRCW060334K0FK
R22	1	620 R	Vishay	CRCW0603620RFK
R24	1	4.7 k	Panasonic	ERJ-PB3B4701V
R25	1	30 k	Vishay	CRCW060330K0FK
R26	1	2.2 k	Vishay	TNPW06032K20BE
R28	1	11 k	Vishay	CRCW060311K0FK
R30	1	8.2 k	Vishay	CRCW06038K20FK
R40_1, R40_2, R40_3, R41_1, R41_2, R41_3, R44_1, R44_2, R44_3, R47_1, R47_2, R47_3	12	0 R	Bourns	CR0603-J/-000ELF
R56, R63, R64, R65, R66, R67	6	300 mR	Panasonic	ERJ-B2BFR30V

Designator	Quantity	Description	Manufacturer	Manufacturer P/N
S1_1, S1_2, S1_3, S2_1, S2_2, S2_3	6	CJS-1201A1	NIDEC COPAL ELECTRONICS, Inc.	CJS-1201A1
TR1, TR2, TR3	3	750319377	Wurth Elektronik	750319377
U1, U4	2	2EP130R	Infineon Technologies	2EP130R
U2	1	TLS205B0EJV	Infineon Technologies	TLS205B0EJV
U3_1, U3_2, U3_3	3	2ED3147MC12L	Infineon Technologies	2ED3147MC12L
X1	1	23.3200-22	Multi-Contact	23.3200-22
X2, X4, X5, X6, X7	5	CT3151V1-2	Cal Test Electronics	CT3151V1-2
X3	1	23.3200-21	Multi-Contact	23.3200-21
X8, X24	2	MMCX-R-PC(40)	Hirose Connectors	MMCX-R-PC(40)
X9, X10, X12, X13, X15	5	20-2137	Vero Technologies	20-2137
X11_1, X11_2, X11_3, X14_1, X14_2, X14_3	6	HTSW-103-07-G-S	Samtec Inc.	HTSW-103-07-G-S

3.4 Connector details

This section provides general information on the connectors of EVAL_AMM12S_2EDR.

Table 5 lists the connectors that provide input power to the high-voltage domain and the connections for a three-phase inductive load.

Table 5 High-voltage connectors

Pin	Symbol	Function
X7	HV_GND	DC-link ground connection
X4	PH1	Half-bridge midpoint connection phase 1
X5	PH2	Half-bridge midpoint connection phase 2
X6	PH3	Half-bridge midpoint connection phase 3
X2	HV+	DC-link positive voltage connection

Table 6 lists the connectors that provide input power for the low-voltage domain and the inputs for PWM signals to all the six switches.

Table 6 Input-side connectors

Pin	Symbol	Function
X1	VIN	LV domain input voltage
X3	GND1	LV domain electrical ground
X11_1_2	IN_LS1	PWM input signal low-side switch phase 1
X14_1_2	IN_HS1	PWM input signal high-side switch phase 1
X11_2_2	IN_LS2	PWM input signal low-side switch phase 2
X14_2_2	IN_HS2	PWM input signal high-side switch phase21

Pin	Symbol	Function
X11_3_2	IN_LS3	PWM input signal low-side switch phase 3
X14_3_2	IN_HS3	PWM input signal high-side switch phase 3

4 System performance

4.1 Test points

Table 7 summarizes the test points on the board.

Table 7 Test points

Test point	Symbol	Signal measured	Ground reference for test point
TP1	NTC1	NTC terminal 1	
TP2	VEE	NTC terminal 2	
TP3_1	Gate HS1	Gate voltage HSS phase 1	GND2_HS1
TP3_2	Gate HS2	Gate voltage HSS phase 2	GND2_HS2
TP3_3	Gate HS3	Gate voltage HSS phase 3	GND2_HS3
TP4_1	IN_HS1	PWM input signal HSS phase 1	GND1
TP4_2	IN_HS2	PWM input signal HSS phase 2	GND1
TP4_3	IN_HS3	PWM input signal HSS phase 3	GND1
TP6_1	GND2_HS1	Kelvin source HS phase 1	GND2_HS1
TP6_2	GND2_HS2	Kelvin source HS phase 2	GND2_HS2
TP6_3	GND2_HS3	Kelvin source HS phase 3	GND2_HS3
TP7_1	IN_LS1	PWM input signal LSS phase 1	GND1
TP7_2	IN_LS2	PWM input signal LSS phase 2	GND1
TP7_3	IN_LS3	PWM input signal LSS phase 3	GND1
TP11_1	EN_1	Enable signal for gate driver phase 1	GND1
TP11_2	EN_2	Enable signal for gate driver phase 2	GND1
TP11_3	EN_3	Enable signal for gate driver phase 3	GND1
TP13_1	Gate LS1	Gate voltage LSS phase 1	
TP13_2	Gate LS2	Gate voltage LSS phase 2	
TP13_3	Gate LS3	Gate voltage LSS phase 3	
TP14_1	DT1	Dead time control gate driver phase 1	GND1
TP14_2	DT2	Dead time control gate driver phase 2	GND1
TP14_3	DT3	Dead time control gate driver phase 3	GND1
TP16_1	GND2_LS1	Kelvin source LS phase 1	
TP16_2	GND2_LS2	Kelvin source LS phase 2	
TP16_3	GND2_LS3	Kelvin source LS phase 3	

Test results

System performance

The following measurements were performed with AMM12S25LB1Z at V_{DC} = 800 V, I_{load} = 40 A at 25°C room temperature. The DUT in this example is the low-side switch of phase U. The load for the double-pulse test was a 581 µH air core inductor with 35 pF parasitic inductance. The gate driver settings were the default ones of the board at V_{DD} = 15 V.

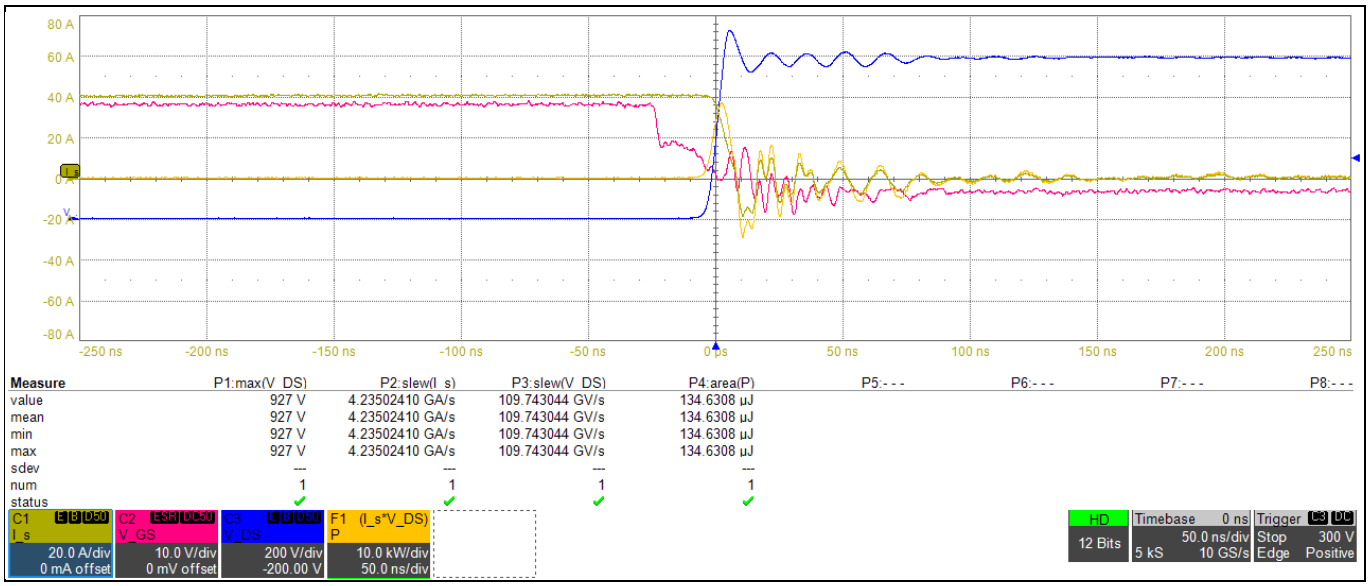


Figure 16 Turn-off-process with AMM12S25LB1Z at V_{DC} = 800 V , I_{load} = 40 A, and 25°C room temperature

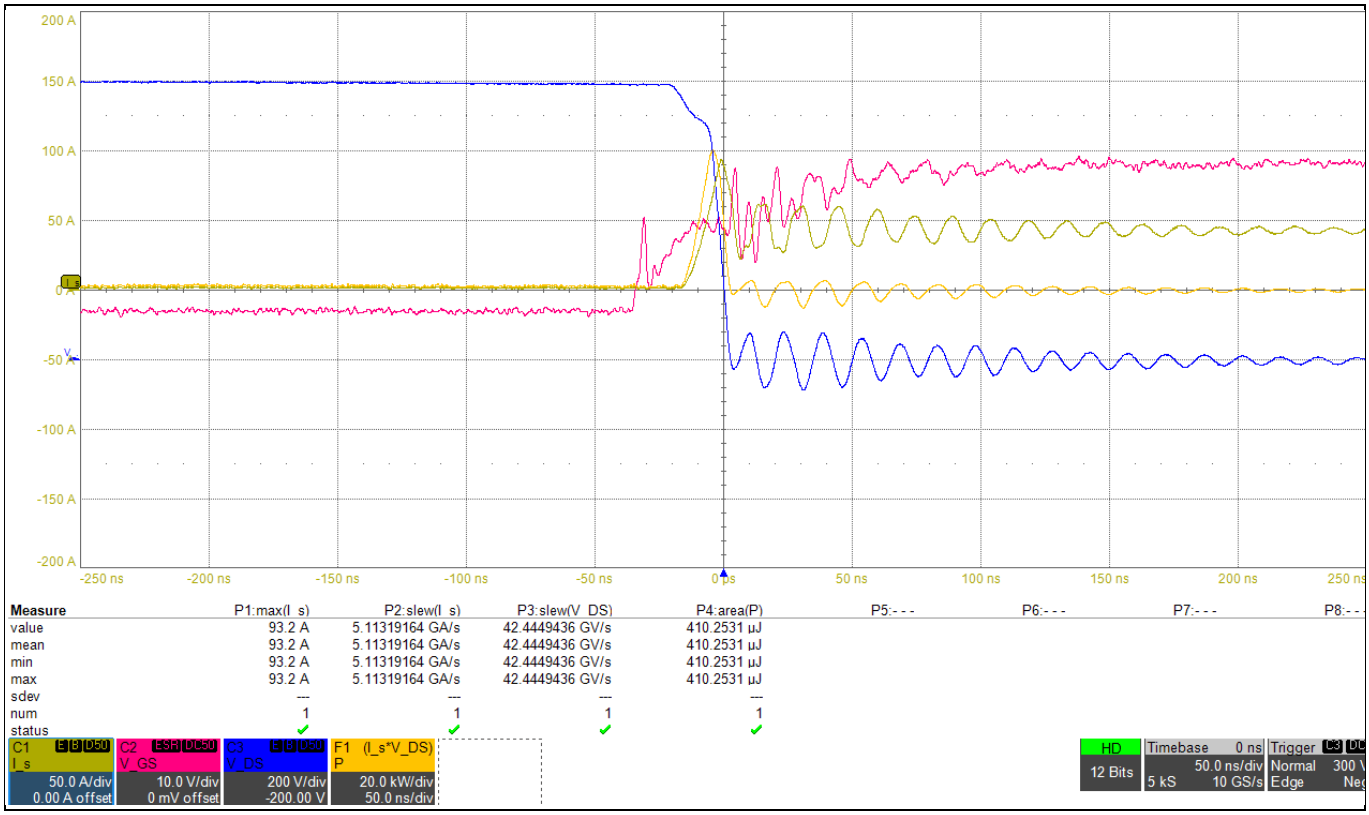


Figure 17 Turn-on-process with AMM12S25LB1Z at V_{DC} = 800 V , I_{load} = 40 A, and 25°C room temperature

The captured signals with the respective measurement instruments are summarized in Table 8.

Table 8 Captured signals from the sample measurement with AMM12S25LB1Z

Signal	Oscilloscope channel	Measurement instrument
Source current low side I_s	1	PMK FireFly® optically isolated probe with 1:25 attenuation on 50 mΩ shunt
Gate-source voltage low side V_GS	2	PMK BumbleBee® HV differential probe with 1:50 attenuation
Drain-source voltage low side V_DS	3	PMK BumbleBee® HV differential probe with 1:500 attenuation
Power loss LS V_DS*I_s	F1	Math functions in the oscilloscope

The oscilloscope used for this measurement was a HDO 6104A-MS 4-channel instrument from Teledyne LeCroy. The deskew of channels 1 and 3 was compensated using the 067-0405-02 test kit from Tektronix.

5 Related resources

- CIPOS™ product family: Link to webpage
- EiceDRIVER™ product family: Link to webpage
- Application design guide for 2EP130R transformer driver: Link
- Infineon developer community

Appendices

A NTC raw data and corresponding voltage

Table 9 NTC raw data: Temperature, nominal resistance, and output voltage

Temperature (°C)	R_{NTC} (kΩ)	V_{out} (V)
-40	307.6	4.925
-39	289.2	4.920
-38	272	4.915
-37	255.9	4.910
-36	240.9	4.904
-35	226.8	4.898
-34	213.6	4.892
-33	201.3	4.886
-32	189.7	4.879
-31	178.8	4.872
-30	168.7	4.864
-29	159.1	4.857
-28	150.1	4.848
-27	141.7	4.839
-26	133.8	4.830
-25	126.4	4.821
-24	119.4	4.811
-23	112.9	4.800
-22	106.7	4.789
-21	100.9	4.777
-20	95.45	4.765
-19	90.17	4.752
-18	85.21	4.739
-17	80.55	4.724
-16	76.18	4.709
-15	72.06	4.694
-14	68.2	4.678
-13	64.56	4.661
-12	61.13	4.643
-11	57.91	4.625
-10	54.88	4.606
-9	52.02	4.586

-8	49.33	4.565
-7	46.79	4.544
-6	44.39	4.521
-5	42.13	4.498
-4	40	4.474
-3	37,99	4,450
-2	36,09	4,424
-1	34,29	4,397
0	32,59	4,370
1	30,98	4,341
2	29,45	4,312
3	28,01	4,282
4	26,65	4,250
5	25,36	4,218
6	24,14	4,185
7	22,99	4,151
8	21,9	4,117
9	20,86	4,081
10	19,88	4,044
11	18,96	4,007
12	18,08	3,968
13	17,25	3,929
14	16,45	3,889
15	15,71	3,849
16	14,99	3,807
17	14,32	3,764
18	13,68	3,721
19	13,07	3,678
20	12,49	3,633
21	11,94	3,588
22	11,42	3,542
23	10,92	3,496
24	10,45	3,449
25	10	3,401
26	9,572	3,353
27	9,165	3,305
28	8,777	3,256
29	8,408	3,207
30	8,056	3,158
31	7,721	3,108

32	7,401	3,058
33	7,097	3,008
34	6,806	2,958
35	6,529	2,907
36	6,264	2,857
37	6,012	2,806
38	5,771	2,756
39	5,541	2,705
40	5,321	2,655
41	5,111	2,605
42	4,911	2,555
43	4,719	2,505
44	4,536	2,456
45	4,361	2,406
46	4,193	2,357
47	4,033	2,309
48	3,879	2,261
49	3,732	2,213
50	3,592	2,166
51	3,458	2,119
52	3,330	2,073
53	3,207	2,028
54	3,089	1,983
55	2,976	1,939
56	2,868	1,895
57	2,765	1,852
58	2,665	1,809
59	2,570	1,768
60	2,479	1,727
61	2,391	1,686
62	2,307	1,646
63	2,226	1,607
64	2,148	1,568
65	2,074	1,531
66	2,002	1,494
67	1,934	1,458
68	1,868	1,422
69	1,804	1,387
70	1,743	1,353
71	1,685	1,319

72	1,628	1,286
73	1,574	1,254
74	1,522	1,223
75	1,472	1,192
76	1,424	1,163
77	1,377	1,133
78	1,333	1,105
79	1,290	1,077
80	1,248	1,049
81	1,208	1,022
82	1,170	0,997
83	1,133	0,971
84	1,098	0,947
85	1,064	0,923
86	1,031	0,899
87	0,9991	0,877
88	0,9684	0,854
89	0,9389	0,833
90	0,9104	0,811
91	0,8829	0,791
92	0,8563	0,771
93	0,8307	0,751
94	0,806	0,732
95	0,7821	0,713
96	0,759	0,695
97	0,7368	0,678
98	0,7153	0,660
99	0,6945	0,644
100	0,6744	0,627
101	0,6551	0,612
102	0,6364	0,596
103	0,6183	0,581
104	0,6009	0,567
105	0,584	0,553
106	0,5676	0,539
107	0,5518	0,525
108	0,5365	0,512
109	0,5217	0,500
110	0,5074	0,487
111	0,4935	0,475

112	0,4801	0,463
113	0,4671	0,452
114	0,4546	0,441
115	0,4424	0,430
116	0,4306	0,420
117	0,4191	0,409
118	0,4081	0,399
119	0,3973	0,390
120	0,3869	0,380
121	0,3769	0,371
122	0,3671	0,362
123	0,3577	0,354
124	0,3485	0,345
125	0,3396	0,337
126	0,331	0,329
127	0,3226	0,321
128	0,3145	0,314
129	0,3067	0,306
130	0,299	0,299
131	0,2916	0,292
132	0,2844	0,285
133	0,2774	0,279
134	0,2706	0,272
135	0,264	0,266
136	0,2576	0,260
137	0,2514	0,254
138	0,2454	0,248
139	0,2395	0,242
140	0,2338	0,237
141	0,2282	0,232
142	0,2228	0,226
143	0,2176	0,221
144	0,2125	0,216
145	0,2076	0,212
146	0,2028	0,207
147	0,1981	0,202
148	0,1935	0,198
149	0,1891	0,193
150	0,1848	0,189
151	0,1806	0,185

152	0,1765	0,181
153	0,1725	0,177
154	0,1687	0,173
155	0,1649	0,169
156	0,1612	0,166
157	0,1577	0,162
158	0,1542	0,159
159	0,1508	0,155
160	0,1475	0,152
161	0,1443	0,149
162	0,1412	0,146
163	0,1382	0,143
164	0,1352	0,140
165	0,1323	0,137
166	0,1295	0,134
167	0,1267	0,131
168	0,1241	0,129
169	0,1214	0,126
170	0,1189	0,123
171	0,1164	0,121
172	0,114	0,118
173	0,1116	0,116
174	0,1093	0,114
175	0,1071	0,111

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[2] Infineon Technologies AG: EiceDRIVER™ Power 2EP1xxR family datasheet, Full-bridge transformer driver for IGBT and SiC MOSFET gate driver supply, document version v1.00, 2024-08-31, www.infineon.com

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