# Application Note AN-1092

## Understanding HVIC Datasheet Specifications

*By Satyavrat Laud*

Table of Contents

**Page**

1. **Introduction** ..... 2

2.1 **Datasheet Description and Key Features** ..... 2

2.2 **Product Summary** ..... 3

2.3 **Absolute Maximum Ratings** ..... 3

2.4 **Recommended Operating Conditions** ..... 5

2.5 **Dynamic Electrical Characteristics** ..... 5

2.6 **Static Electrical Characteristics** ..... 7

2.7 **Functional Block Diagram** ..... 10

2.8 **Lead Definitions** ..... 10

2.9 **Lead Assignments** ..... 11

2.10 **Figures/Graphs** ..... 12

3. **Notes/Tips** ..... 12

4. **Conclusions** ..... 13

This application note provides a detailed explanation of the contents of typical International Rectifier HVIC (high voltage IC) datasheets. The goal is to convey the underlying significance of the key specifications and information contained therein.

**1. *Introduction***:

International Rectifier (IR) gate driver IC datasheets contain a wealth of information for the circuit designer/user. However, often this information is very brief and to the point (as is the case with most technical specifications). The aim of this application note is to better understand the IR gate driver IC datasheets and the technical specifications listed therein. This will facilitate the first time users as well as experienced circuit designers in their applications. The IRS2110/IRS2113 datasheet is used as the basis in the following discussion, unless mentioned otherwise. In the sections 2.1 to 2.10 that follow, each part of the datasheet is discussed in the same order of succession as per the IRS2110/IRS2113 datasheet.

**2.1 *Datasheet Description and Key Features:***

As with all other IR product datasheets, each product datasheet has an identification number and a revision number on the top of the first page. It also lists the type of driver, whether a single channel (for driving a single MOSFET/IGBT), or dual channel (such as a high and low side driver, or a half bridge driver). For example, the IRS2110/IRS2113 datasheet describes it as a high and low side driver, built using a latch immune CMOS, proprietary, monolithic technology. As such, these drivers may be used to drive two independent MOSFETs/IGBTs (hereafter denoted as 'switches'), one on the high side and the other on the low side, or may be configured as a half bridge driver.

The key features of the driver IC are provided on the first page of the datasheet. For example, the IRS2110/IRS2113, has a floating channel which provides gate drive for the high side switch. As such, the $V_S$ pin can float above the HV return (the COM) by +500V for the IRS2110, or +600 V for the IRS2113. Other features are as follows:

- The gate drive supply range is quite wide (10 V to 20 V), unlike many other competitors' MOS gate drivers, which typically provide lower voltage levels.

- The two independent undervoltage lockout features sense the $V_{CC}$, and the floating channel supply $V_{BS}$, and shut down both channels, or the high side channel, in the event of undervoltage conditions, protecting the switches being driven, and the IC itself.
- The input signal compatibility (down to 3.3 V CMOS logic) allows for easy interfacing with controllers such as microprocessors and DSPs.
- All input pins have Schmitt triggers providing better noise immunity.
- The propagation delays are matched.
- A high pulse current buffer stage, to minimize any possible cross-conduction (between the high and low side switches).

**2.2 *Product Summary***:

The Product Summary section is a brief summary of the key IC specifications. These specifications may include: the maximum offset voltage, the output current ratings (maximum sourcing and sinking currents, Io+/-), the output voltage (at HO and LO pins), the propagation delay times, delay matching timings, etc. Also, there is a typical connection diagram that shows the input and output pins of the IC, and how it is to be used as a driver. For example, the IRS2110 may be used in the half bridge (HB) driver configuration, or could be used to drive two independent switches, depending on the application requirements.

**2.3 *Absolute Maximum Ratings*:**

These are absolute sustained maximum limits for a given specification, beyond which damage to the device may occur. For some of the specifications, there is also an absolute minimum limit (primarily due to presence of a negative voltage diode clamp). These ratings are described as follows (for this section we will continue to use the IRS2110 & IRS2113 datasheet specifications):

- *$V_B$ - High side floating supply voltage*: The maximum voltage at the $V_B$ pin, with respect to the COM, is 520 V for the IRS2110, and 620 V for the IRS2113. There is also a minimum voltage of – 0.3 V at this pin.

- *$V_S$ – High side floating supply offset voltage*: The maximum swing allowable at the $V_S$ pin, with respect to $V_B$, is between $V_B$ + 0.3 V (maximum), and $V_B$ – 20 V (minimum).
- *$V_{HO}$ - High side floating output voltage*: The maximum voltage allowable at the HO pin is equal to $V_B$ + 0.3 V, and the minimum is $V_S$ – 0.3 V.
- *$V_{CC}$ - Low side fixed supply voltage*: The maximum supply voltage allowable at the $V_{CC}$ pin, which provides the biasing power supply for the low side channel and the input side circuitry, is 20 V (internally clamped) for the IRS2110/IRS2113, and the minimum is – 0.3 V.
- *$V_{LO}$ – Low side output voltage*: The voltage available at the LO pin is allowed to swing between $V_{CC}$ + 0.3 V (maximum), and – 0.3 V with respect to COM (minimum).
- *$V_{DD}$ - Logic supply voltage*: This is the supply voltage providing biasing to the input side circuit of the IC, and is referenced to the $V_{SS}$ pin. The maximum allowable voltage at this pin is $V_{SS}$ + 20 V (internally clamped), and the minimum is – 0.3 V.
- *$V_{SS}$ - Logic offset supply voltage*: The $V_{SS}$ pin provides the reference for the input signals, and the biasing supplies. The maximum swing allowable at this pin is up to $V_{CC}$ + 0.3 V, and the minimum is $V_{CC}$ – 20 V.
- *$V_{IN}$ - Logic input voltage*: The voltage level at the input pins ($H_{IN}$, $L_{IN}$, and SD), referenced to $V_{SS}$, can swing between a maximum of $V_{DD}$ + 0.3 V, and a minimum of $V_{SS}$ – 0.3 V.
- *$dV_S/dt$ – Allowable offset supply voltage transient*: The maximum rate at which the voltage at the $V_S$ pin can change is 50 V/ns. This high degree of tolerance makes the IC robust, and ensures excellent device performance in demanding applications such as motor drives, switching power supplies, etc. The $dV_S/dt$ capability is measured as per the test set up shown in Fig. 2 of the datasheet.
- *$P_D$ – Package power dissipation at $T_A \leq +25$ ° C*: This is the maximum amount of power that can be safely dissipated by the IC, at a given ambient temperature. For the 14 lead DIP package this is 1.6 W, and for the 16 lead SOIC package it is 1.25 W.

- $R_{THJA}$ - *Thermal resistance, junction to ambient*: The maximum thermal resistance of the package to the flow of heat from the junction to the ambient is 75 ° C/W for the 14 lead DIP package, and 100 °C/W for the 16 lead SOIC package. This specification is characterized with the device mounted on a 2 oz. copper pad of surface area 1 sq inch, on a FR-4 board.
- $T_J$ *–Junction temperature*: The maximum temperature of the junction (silicon) inside the package is 150 °C. For safe device operation, the allowable maximum $T_J$ must never be exceeded.
- $T_S$ *– Storage temperature*: The temperature, at which the device may be safely stored, when not being used, is 150 °C (maximum), and – 55 °C (minimum). These limits must never be exceeded.
- $T_L$ *– Lead temperature (soldering, 10 seconds)*: The maximum temperature the device may be safely subjected to during soldering, is 300 °C for up to 10 s.

All supplies (i.e., $V_B$, $V_{CC}$, and $V_{DD}$) are fully tested at 25 V; an internal 20 V clamp exist for each supply.

**2.4 *Recommended Operating Conditions*:** These are the operating conditions for the key specifications as listed in the previous section, under which the device is **recommended** to be operated. The device input/output signals, and supply and offset voltage ratings are tested for a 15 V bias ($V_{CC}$ = 15 V) condition, and for a given ambient temperature ($T_A$ = 25 °C). Typically, the recommended operating conditions define limits for device operation under steady state conditions. The absolute maximum and minimum limits discussed earlier, provide the limits for worst case conditions, such as transients.

**2.5 *Dynamic Electrical Characteristics*:**

These specifications relate to timing information. These are discussed as follows:

- $t_{ON}$ - *Turn-on propagation delay*: This is the time taken for the output voltage at HO (or LO) to reach to 10% of its maximum possible value, when the input has reached 50% of its maximum possible value. It essentially reflects the delay between the time when a signal is applied at the input (HIN, or LIN), to the time the output starts going high (at HO or LO).

- $t_{OFF}$ - *Turn-off propagation delay*: This is the time taken for the output voltage at HO (or LO) to reach to 90% of its maximum possible value, when the input has reached 50% of its maximum possible value. It essentially reflects the delay between the time when a signal is applied at the input (HIN, or LIN), to the time the output starts going low (at HO or LO).
- $t_{SD}$ - *Shutdown propagation delay*: This is the time taken for the outputs (at HO and LO) to decrease to 90% of their maximum values, when the signal at the shutdown input (SD pin) has reached 50% of its maximum value.
- $t_r$ - *Turn-on rise time*: This is the time taken for the outputs (HO and LO) to reach 90% of their maximum values, for given test conditions. The shorter the rise time, the faster is the IC response.
- $t_f$ - *Turn-off fall time*: This is the time taken for the outputs (HO and LO) to reach 90% of their maximum values, for given test conditions. Again, the shorter the fall time, the faster is the IC response.
- *MT – Delay matching, HS and LS turn-on/off* : This is the time difference between the LO and HO outputs, when each output has reached 10% of it's maximum (during turn-on), or when each output has decreased to 90% of it's maximum (during turn-off), assuming that HIN and HIN are simultaneously applied. The shorter the delay matching time, the better the circuit performance.

The timing information can be more easily understood by referring to the timing diagrams (reproduced from the IRS2110/IRS2113 datasheet available on the IR website at www.irf.com):

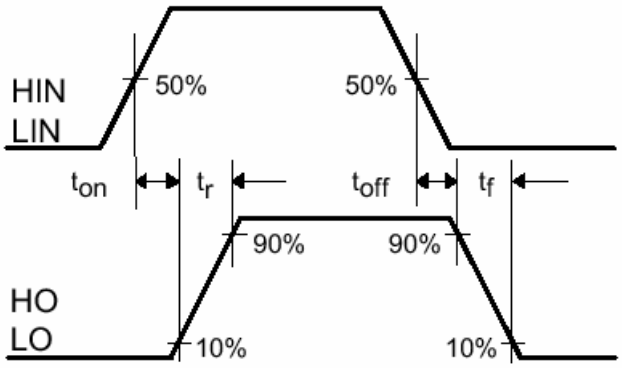


**Fig. 1: Switching Time Waveforms Definition.**

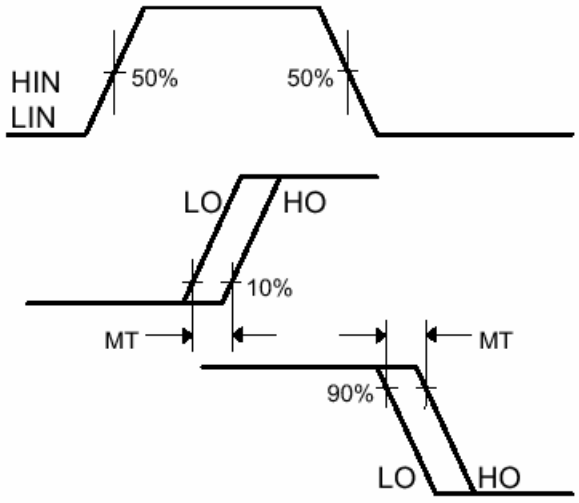


**Fig. 2: Delay Matching Waveforms definition.**

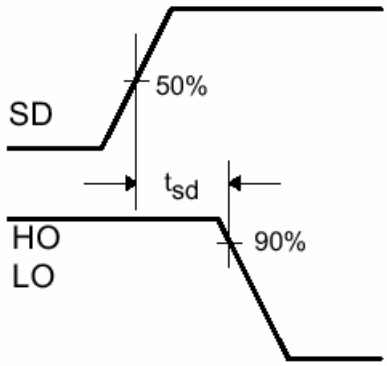


**Fig. 3: Shutdown Waveforms definition.**

**2.6** ***Static Electrical Characteristics***:

These specifications relate to the operating requirements for specific parameters such as the input and output, for given bias ($V_{CC}$, $V_{BS}$, and $V_{DD}$), and ambient temperature ($T_A$ = 25 °C ) conditions.

- $V_{IH}$ - *Logic "1" input voltage*: This is the minimum voltage level, which if made available at the input pins (HIN, LIN), causes the respective outputs (HO, LO) to go high. The outputs will remain high as long as this minimum voltage is present. In case of the SD pin, if this minimum voltage level is present at that pin, both the outputs are forced low (the SD pin disables the device).
- $V_{IL}$ - *Logic "0" input voltage*: This is the maximum voltage level, which if available at the input pins (HIN, LIN), causes the respective outputs (HO and LO) to go low. The output will remain low as long as the voltage at the respective input pin(s) is below this voltage. In case of the SD pin, if the voltage level is below this level, the outputs are not affected.
- $V_{OH}$ - *High level output voltage*, $V_{BIAS} - V_O$: This is the maximum voltage drop that may occur on the output side circuitry of the IC, such that at no load ($I_O$ = 0 A), when the output is in the HIGH state, the voltage at that output pin would be the bias supply, minus this drop.

- $V_{OL}$ - *Low level output voltage, $V_O$*: This is the maximum voltage drop that may occur on the output side circuitry of the IC, such that at $I_O$ = 20 mA, when the output is in the LOW state, the voltage at that output pin would be the COM (or $V_S$ for the high side channel), plus this drop.
- $I_{LK}$ - *Offset supply leakage current*: This is the maximum leakage current that can flow through the output circuit on the high side of the IC, when the $V_B$ and $V_S$ pins are tied together, and $V_B$, $V_{CC}$, $V_{DD}$ are biased at 15 V and $V_{SS}$ = COM. It essentially reflects the leakage from the high side circuitry to the COM in the IC.
- $I_{QBS}$ - *Quiescent $V_{BS}$ supply current*: This is the maximum DC current that may be consumed from the high side supply ($V_{BS}$), when the outputs are either high or low state.
- $I_{QCC}$ - *Quiescent $V_{CC}$ supply current*: This is the maximum DC current that may be consumed from the bias supply ($V_{CC}$), when the inputs are either high or low state.
- $I_{QDD}$ - *Quiescent $V_{DD}$ supply current*: This is the maximum DC current that may be consumed from the logic power supply ($V_{DD}$), when the inputs are either high or low state.
- $I_{IN+}$ - *Logic "1" input bias current*: This is the maximum DC current that may be sourced to the input pin(s), when that input pin(s) is pulled high ($V_{IN}$ = $V_{DD}$). The positive current reference implies that this current flows into the input pin(s).
- $I_{IN-}$ - *Logic "0" input bias current*: This is the maximum DC current that may be sunk at the input pin(s), when that input pin is pulled low ($V_{IN}$ = 0 V). The negative current reference implies that this current flows out of the input pin(s).
- $V_{BSUV+}$ - *$V_{BS}$ supply under voltage positive going threshold*: When the $V_{BS}$ supply voltage rises above this threshold level, the UVLO (under voltage lockout feature) is disabled.
- $V_{BSUV-}$ - *$V_{BS}$ supply under voltage negative going threshold*: When the $V_{BS}$ supply voltage falls below this threshold level, the UVLO is enabled.
- $V_{CCUV+}$ - *$V_{CC}$ supply under voltage positive going threshold*: When the $V_{CC}$ supply voltage rises above this threshold level, the UVLO is disabled.

- *$V_{CCUV-}$ - $V_{CC}$ supply under voltage negative going threshold*: When the $V_{CC}$ supply voltage falls below this threshold level, the UVLO is enabled.
- *$I_{O+}$ - Output high short circuit pulsed current*: This is the peak current that can flow out of the output pin(s), for a given pulse duration, when the respective input pin is high, and the output pin is shorted to the COM. This represents the peak capacity of the IC to supply the gate charge of the driven switch.
- *$I_{O-}$ - Output low short circuit pulsed current*: This is the peak current that can flow into the output pin(s), for a given pulse duration, when the respective input pin is low, and the output pin is fully biased with respect to the COM. This represents the peak capacity of the IC to discharge the gate charge of the driven switch.

**Note:** The UVLO protection feature on the $V_{BS}$ supply, and that on the $V_{CC}$ are separate, and operate differently. The UVLO on the $V_{BS}$ is cycle by cycle type. The output (HO) is latched off when the $V_{BS}$ goes below the set threshold and resets itself with the next cycle (requires a fresh edge on the HIN). The UVLO on the $V_{CC}$ is real-time, and as long as the $V_{CC}$ is below the specified threshold, LO, and HO remain off (such as after the initial power on condition). Once the $V_{CC}$ goes above the UVLO threshold, the LO will follow LIN (does not need a fresh edge at LIN). The HO however would require a fresh edge at HIN. Also, the UVLO threshold levels on the $V_{CC}$ and $V_{BS}$ are absolute (do not change with the applied $V_{CC}$ or $V_{BS}$).

**2.7 *Functional Block Diagram***:

This shows in block diagram format, the internal functional structure of the IC, such as the level shift circuits, the under voltage detect for both high and low side supplies, the pull down resistors on the input pins etc.

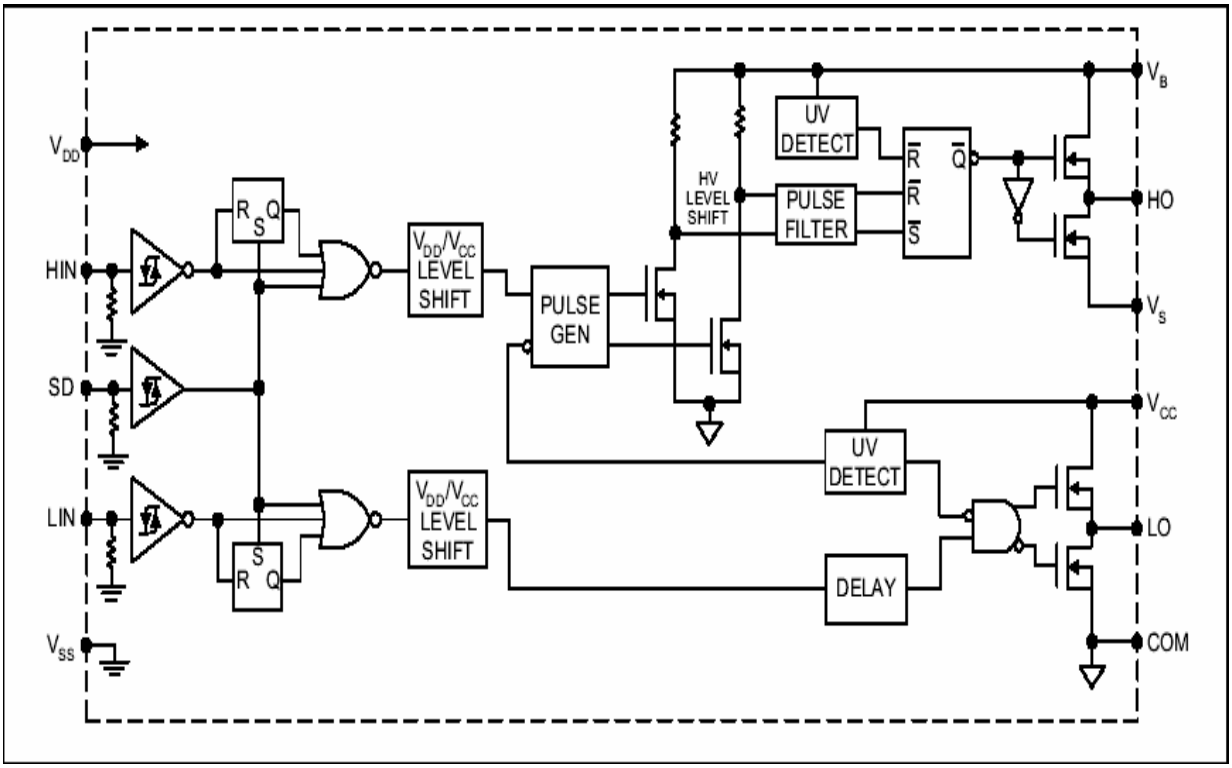


**Fig. 4: Functional Block Diagram (for IRS2110/IRS2113)**

**2.8** ***Lead Definitions***:

This section provides a description for each of the IC pins (except those that are not connected).The definitions are detailed as follows:

- $V_{DD}$ - *Logic supply voltage*: This is the supply voltage providing biasing to the input side circuit of the IC (such as the HIN, LIN, and SD signals).
- *HIN – Logic input for high side gate driver output (HO), in phase*: This is the input pin at which the input PWM signal to control the high side output (HO), is to be applied. The HO is in phase with the HIN for the IRS2110/IRS2113.
- *SD – Logic input for shutdown*: This is the input pin at which an active high signal can be applied, which will disable the IC outputs (shut down HO and LO).
- *LIN – Logic input for low side gate driver output (HO), in phase*: This is the input pin at which the input PWM signal to control the low side output (LO), is to be applied. The LO is in phase with the LIN for the IRS2110/IRS2113.

- *$V_{SS}$ - Logic offset supply voltage*: This is the reference for the input signals, and biasing supplies. This is normally tied to the input side ground (signal ground).
- *$V_B$ – High side floating supply*: This is the floating supply voltage pin. This voltage provides the high side supply ($V_{BS}$). The bootstrap capacitor $C_B$ is connected across the $V_B$ and $V_S$ pins as shown in typical connection diagram.
- *HO – High side gate drive output*: This is the output pin at which the PWM signal to control the high side switch is available.
- *$V_S$ – High side floating supply offset voltage*: This is the floating reference voltage for the high side supply ($V_B$). $V_S$ swings between the COM (when HIN is low, and $L_{IN}$ is high), and the high voltage rail (when the $H_{IN}$ is high, and $L_{IN}$ is low).
- *$V_{CC}$ - Low side fixed supply voltage*: This is the ground referenced voltage at the $V_{CC}$ pin, which provides the biasing power supply for the low side channel, and also the input side circuitry.
- *LO – Low side gate drive output*: This is the output pin at which the PWM signal to control the low side switch is available.
- *COM – Low side return*: This is the reference pin for the output side circuits, and for the $V_{CC}$. Typically the COM is electrically very close to the $V_{SS}$ in potential. The potential difference between the $V_{SS}$ and COM should not exceed 5 V, for proper device operation.

**2.9 *Lead Assignments***:

These figures show the pin out of the IC, with pin numbering. The pin outs for the 14 lead DIP, and the 16 lead SOIC versions are shown.

**2.10 *Figures/Graphs***:

The figures in the datasheet provide detailed characterization of various specifications such as the variation of turn-on time with temperature, shutdown time with respect to $V_{DD}$ supply voltage, junction temperature with respect to switching frequency, etc. Most figures show the variation of the maximum and typical values of the given specification. This helps the designer to utilize the IC to its full potential.

**3. *Notes/Tips*:**

In this section, we discuss aspects of the IC operation that may not be apparent, or obvious from the datasheet:

1. The internal pull down resistors at the input pins, are weak pull downs (typically 50 kΩ to 1 MΩ range). As such, external strong pull downs can be used in electrically noisy environments.
2. Typically, the operating frequency range for the IRS2110/IRS2113 is from a few tens of Hz, up to about 100 kHz (frequencies up to 250 kHz may be possible, based on the maximum allowable power dissipation not being exceeded).
3. The static and dynamic electrical characteristics are measured/characterized for $V_{BIAS}$ voltages (such as $V_{CC}$, $V_{BS}$, and $V_{DD}$) set to 15 V. At lower voltages (such as 10 V or 12 V), the timings such as $t_r$, $t_f$, and $t_{SD}$ times would be slower (as shown in the figures on the datasheet).
4. The threshold levels for the input voltages at $H_{IN}$, $L_{IN}$, and SD scale according to the input side bias supply (the $V_{DD}$). For example, as the datasheet specification for $V_{IH}$ = 9.5 V (min) is characterized for $V_{DD}$ = 15 V, if a specific design uses a $V_{DD}$ = 12 V, then $V_{IH}$ = (12 V/15 V) * 9.5 V = 7.6 V (min) in that application.
5. The $V_{DD}$ should be the same as the input logic level. For example, if the input logic level is TTL, 5 V logic, the $V_{DD}$ should also be 5 V.
6. IC start-up procedure: For applications such as MOSFET/IGBT half-bridges, and using the typical connection diagram (shown on the datasheet), the standard start-up procedure for the IC is as:
    - Ensure that the correct bootstrap capacitor and diode components have been selected as per design tip DT 98-2.
    - Ensure that the $V_{CC}$ and $V_{DD}$ voltages are available, and within specifications.
    - Enable the high voltage supply (the DC bus).
    - Apply the input signal to LIN. Accordingly, the LO will go high (after the $t_{ON}$ and $t_r$ times).
    - When the low side switch turns on, the bootstrap capacitor can charge to almost $V_{CC}$ (minus the [bootstrap diode drop + drop across the low side

switch/load]), within a given time duration (based on its capacitance and the charging path impedance). In most cases, 100 µs to 200 µs should suffice for this purpose.

- When the bootstrap capacitor is fully charged, the PWM signals may be applied as per the required logic.

**4. *Conclusions***:

In this Application Note, the major specifications as listed on the gate driver IC datasheet have been discussed, with particular reference to the IRS2110/IRS2113 gate driver IC. The subtleties underlying the specifications are highlighted. Finally, a few notes/tips are presented, which would be useful to the first time users of this IC. For details on applications using IR gate driver ICs, consult AN-978, and other application notes listed at: http://www.irf.com/technical-info/appnotes.htm.