CoolSiC™ MOSFET M2 in Easy modules

About this document

Scope and purpose

The benefits of wide-bandgap silicon carbide (SiC) semiconductors arise from their higher breakthrough electric field, larger thermal conductivity, higher electron-saturation velocity, and lower intrinsic carrier concentration compared to silicon (Si). Based on these SiC material advantages, SiC MOSFETs are an attractive switching transistor for high-power applications, such as solar inverters, energy storage systems, and offboard and onboard electric vehicles (EV) chargers.

This application note introduces a new generation of products that leverage advancements in SiC MOSFET technology, innovative packaging, and improved interconnection techniques. Different applications require different features – Infineon's latest CoolSiC™ MOSFET M2 with .XT interconnection technology and new housing in the EasyC series will cover them all.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems

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1 Infineon's SiC Trench CoolSiC™ MOSFET M2 – key features

The new CoolSiC™ MOSFET M2 offers major improvements over its predecessor, the CoolSiC™ MOSFET M1H, inboth hard-switching and soft-switching topologies for a wide range of applications, such as EV charging, energy storage systems, solar inverters, and other high-frequency switching applications. The key features of the CoolSiC™ MOSFET M2 are:

- **Improved chip performance:**

  Due to an optimized channel and cell design, the latest chip technology of the CoolSiC™ MOSFET M2 enables a ~25% better $R_{DS(on)}$ x A at nominal current over the entire T_{vj} range.

- **Enlarged gate-source voltage window:**

  The CoolSiC™ MOSFET M2 with extended gate-source voltage specifications offers higher flexibility:

  - Recommended gate-source voltage window from 15 V to 18 V and from 0 V to -5 V
  - Extended maximum gate-source voltage from -10 V to +25 V to cover overshoots and undershoots

- **Increased maximum virtual junction temperature:**

  The CoolSiC™ MOSFET M2 enables continuous operation at a temperature of $T_{vj\,op}$ = 175°C and up to $T_{vj\,over}$ = 200°C under overload conditions.

- **Enlarged reverse bias safe operating area (RBSOA):**

  The repetitive peak drain current has been increased to 2.5 times the nominal current to provide an additional buffer in applications that require high current overload.

- **Longer lifetime:**

  The CoolSiC™ MOSFET M2 comes with an improved module assembly and the .XT (e**x**tended life**t**ime) interconnection technology. It offers over 20 times better power cycling capability at T_{vjmax} of 175°C, ΔT_{vj} of 100K and $t_{cyc} \leq 3s$ than standard interconnection technology for best long-term performance.

The vertical structure of the new CoolSiC™ MOSFET M2 with an optimized channel and cell design is shown in Figure 1. More general information regarding CoolSiC™ MOSFET essentials are shown in [11].

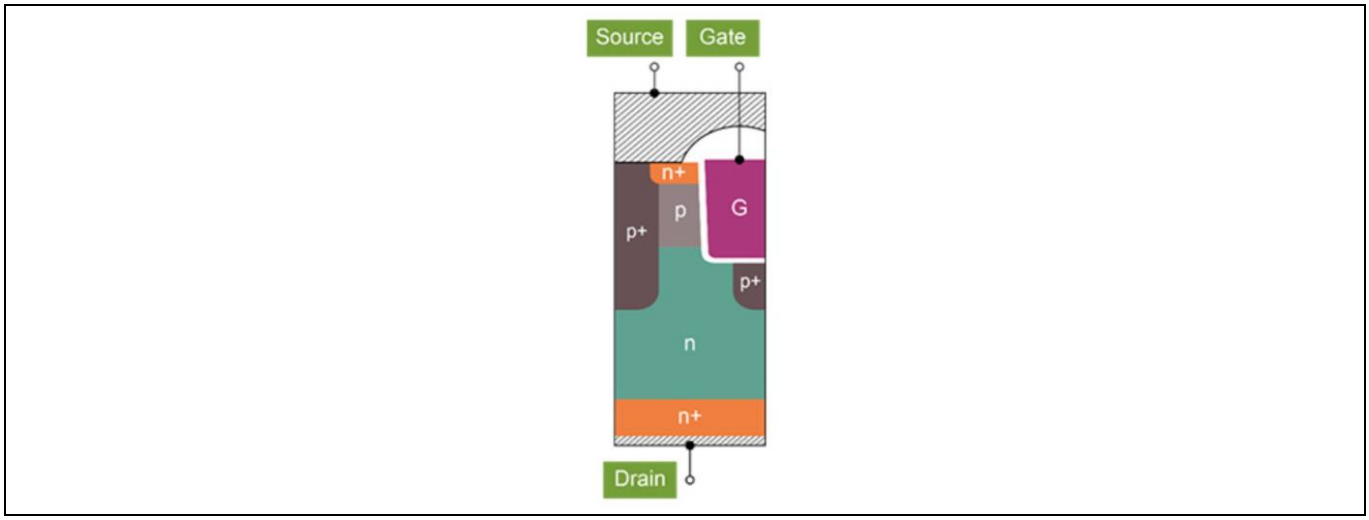

Figure 1 **The vertical trench cell structure of the CoolSiC™ MOSFET M2.**

Infineon's SiC Trench CoolSiC™ MOSFET M2 – key features

Besides innovation in the chip technology of the CoolSiC™ MOSFET M2, Infineon also provides an upgrade on the package technology that enables flexibility and low-inductive designs. The extended product range covers the Easy 1C and Easy 2C modules, shown in Figure 2. The EasyC series is currently available in the industry grade version. It's automotive grade version, that complies to the AQG324 qualifications and requirements, will be available soon. More detailed information of the newest package technology is shown in chapter 5.

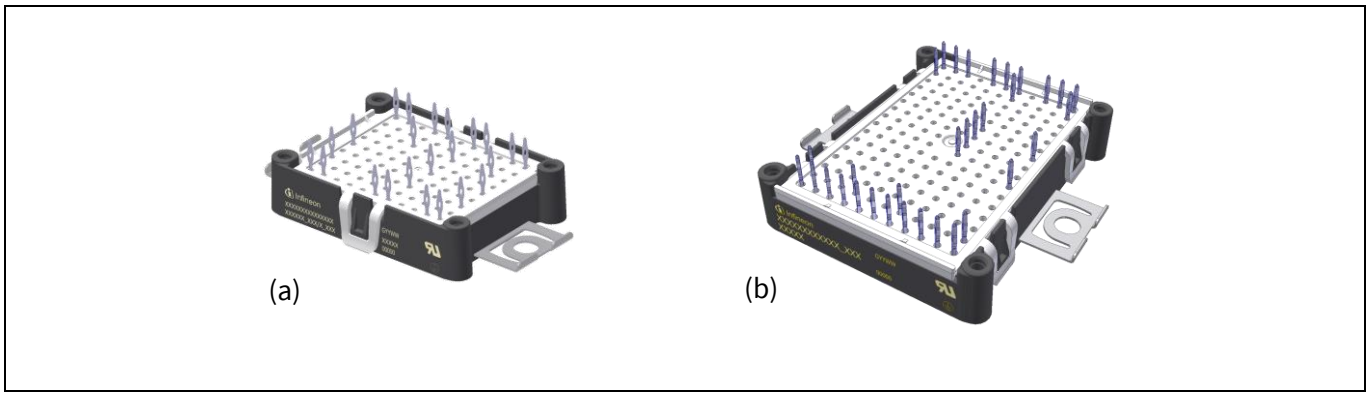

Figure 2 **Module solutions using CoolSiC™ MOSFET M2 (a) Easy 1C, (b) Easy 2C.**

The CoolSiC™ MOSFET M2 in the Easy module family works with a wide range of different topologies to meet individual application requirements. Figure 3 shows the nomenclature legend for the new CoolSiC™ MOSFET M2 portfolio.

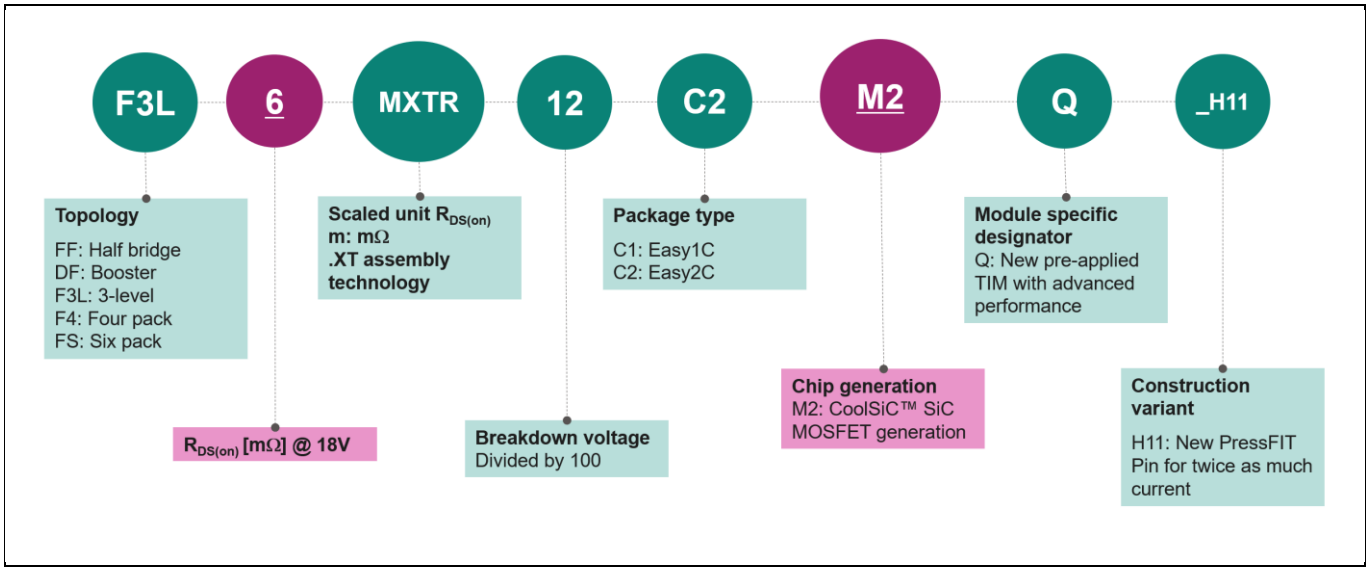

Figure 3 **CoolSiC™ MOSFET M2 nomenclature legend.**

2 Device characteristics

The CoolSiC™ MOSFET technologies can be used in a wide range of applications, which have different and specific requirements. The new CoolSiC™ MOSFET M2 technology offers a more flexible gate-source voltage range than the previous CoolSiC™ MOSFET M1H. It can simplify the design-in process and help optimize the technology to the highest level for each application.

To select the right gate source voltage, many trade-offs need to be considered. The criteria listed below give an overview of some of the most important parameters that will be affected by the chosen gate-source voltage:

- Performance:
  - On-state resistance, $R_{DS(on)}$
  - I-V characteristics of the body diode
  - Dynamic switching behavior
- Driver stage:
  - Gate charge: Output power rating of the driver
  - Complexity of the driver stage: Unipolar versus bipolar power supply
- Parasitic turn-on
- Failure In Time (FIT) rates

This chapter explains the impact of the gate-source voltage on the abovementioned individual parameters. The information in this chapter was developed using specific part numbers but the general behavior is also applicable to other packages or chips using the CoolSiC™ MOSFET M2 technology.

2.1 Datasheet definitions of the gate-source voltage

One of the advantages of the CoolSiC™ MOSFET M2 technology is that the devices can be operated within a flexible gate-source voltage range. The wide gate-drive voltage window for the positive and negative voltage provides the flexibility to choose the best operating point for an application, depending on the individual use case.

It is important to establish a clear distinction between the maximum static gate-source voltages, the maximum dynamic gate-source voltages, and the recommended on-state and off-state gate voltages.

The maximum static gate-source voltage ratings, which correspond to the steady-state operating condition, are bound by an upper limit of +20 V and a lower limit of -7 V. As it is a maximum rated value, it is essential to ensure that these limits are not exceeded, except under transient dynamic conditions, which is discussed in detail below.

Device characteristics

Table 3 Maximum rated values

Parameter	Symbol	Note or test condition	Values	Unit
Gate-source voltage, max. transient voltage	V_{GS}	D<0.01	-10/25	V
Gate-source voltage, max. static voltage	V_{GS}		-7/20	V

Table 4 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
On-state gate voltage	$V_{GS(on)}$		15 ... 18	V
Off-state gate voltage	$V_{GS(off)}$		0 ... -5	V

Figure 4 **Datasheet values for the gate-source voltage in CoolSiC™ MOSFET M2.**

The maximum dynamic gate-source voltages describe the transient voltage peak during the turn-on and turn-off events. The dynamic gate-source voltages can reach maximum peak voltages of +25 V and -10 V for a duty cycle of less than 1%. This is the maximum rated value and must not be exceeded.

A duty cycle is defined as the entire time period as well as the time when the gate-source voltage exceeds the maximum static gate-source voltages. Figure 5 shows a sample gate-source voltage waveform. For simplicity, the envelope (green dotted line in Figure 5) can be used to extract the timeframes t_1 and t_2. Equation (1) shows how to calculate the duty cycle.

$$D = \frac{t1}{T} = < 1\%\,; \qquad D = \frac{t2}{T} = < 1\% \tag{1}$$

In addition to the maximum rated values, driving the devices in a certain voltage range is recommended. The on-state voltage range is between + 15 to + 18 V and the off-state gate voltage range is between 0 to -5 V. Depending on individual requirements in the respective application, the $V_{GS(on)}$ and $V_{GS(off)}$ levels must be defined carefully.

The characteristic values specified in the CoolSiC™ MOSFET M2 datasheet are $V_{GS(on)}$ = + 18 V and $V_{GS(off)}$ = - 3 V. This is a good trade-off between the performance and lifetime for many applications [1].

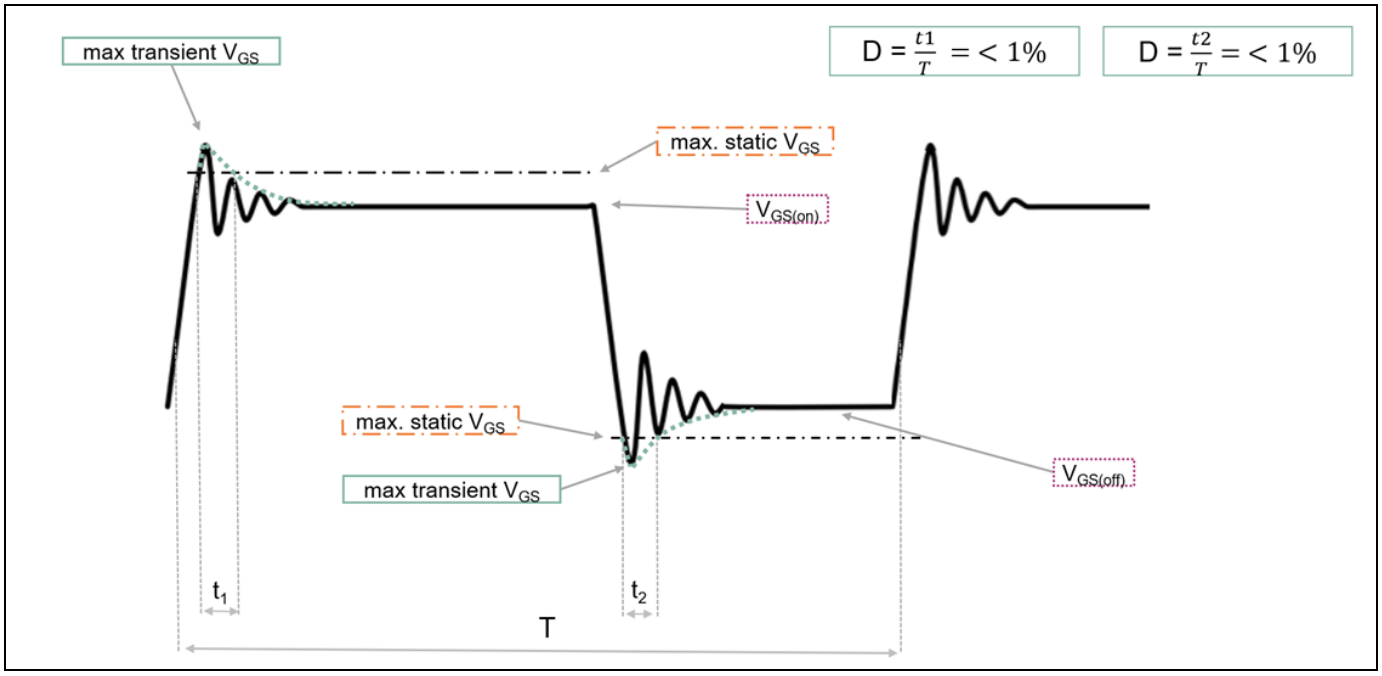

Figure 5 **Schematic gate-source voltage waveform.**

2.2 Device characteristics of CoolSiC™ MOSFET M2

This section describes the impact of the gate-source voltage on several key parameters of the CoolSiC™ MOSFET M2.

2.2.1 On-state resistance $R_{DS(on)}$ versus V_{GS}

As described in the previous section, driving the devices with an on-state voltage of +15 to +18 V and an off-state voltage of 0 to -5 V is recommended. Transient peak voltages during a switching event can reach up to +25 V and -10 V with a duty cycle of 1%. Thus, the typical on-resistance of a device is determined at $V_{GS(on)}$ = +18 V and +15 V in the respective datasheets.

The choice of the on-state gate voltage has an impact on the static performance of the device. The $R_{DS(on)}$ at room temperature as well as the temperature dependency differs among different on-state gate voltages [1].

The I-V curves or output characteristics of a MOSFET are measured in pulse mode for different junction temperatures, such as 25°C, 125°C, and 175°C. Figure 6 shows the drain current as a function of the drain-source voltage, V_{DS}, with an on-state gate-source voltages $V_{GS(on)}$ of 18V.

The dark green lines in Figure 6 show the characteristics of the CoolSiC™ MOSFET M2 compared to that of the previous CoolSiC™ MOSFET M1H (light green lines) with the same chip size. The solid curves are typical results at 25°C, and the dashed curves are those at higher junction temperature of 125°C and 175°C.

Device characteristics

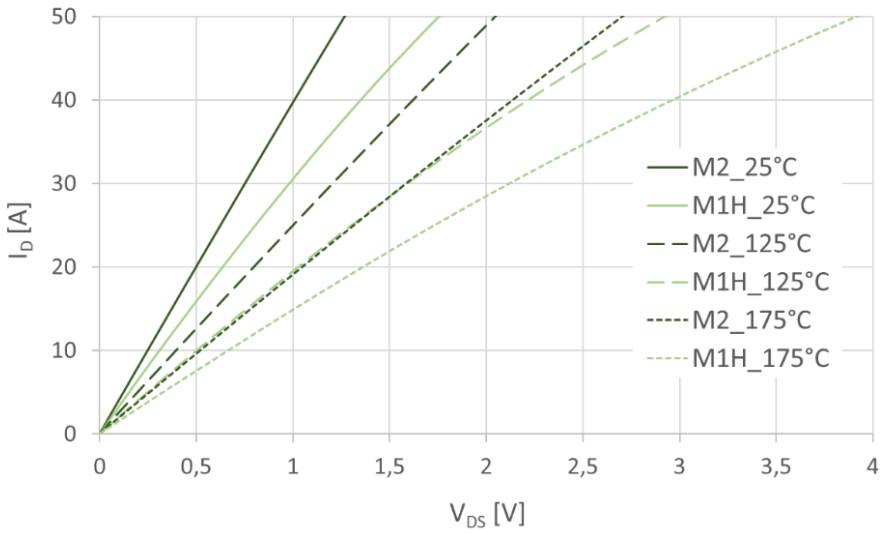

Figure 6 **Typical output characteristics for the M2 compared to the previous M1H technology with the same chip size. V_{GS} = 18 V at T_j = 25°C, 125°C, and 175°C.**

Due to the optimized pitch design of the new CoolSiC™ MOSFET M2, the chip shows a higher saturation current than the CoolSiC™ MOSFET M1H, as shown in Figure 6. A reduced pitch leads to a higher density of trenches per-unit area, resulting in a wider channel width. This, in turn, accommodates a larger number of current-carrying elements. Consequently, the transconductance becomes more pronounced, causing the curve to exhibit a steeper slope. As a result, the improvement in the CoolSiC™ MOSFET M2 are even more pronounced at currents above nominal, leading to a fully linear behavior in the relevant current regime. Due to this, the contribution of M2 in channel resistance (R_{ch}) is less.

The total $R_{DS(on)}$ resistance is determined by the sum of the following single resistances:

- The channel resistance (R_{ch})
- The resistance of the junction field-effect transistor (R_{JFET})
- The epitaxial layer resistance of the drift region (R_{epi})
- The resistance of the highly doped SiC substrate (R_{Sub})

The MOSFET's channel resistance has a negative temperature characteristic due to the behavior of the interface states, while the drift region and intrinsic JFET have positive temperature characteristics. Due to the advantageous channel orientation along the preferred crystal plane with a low density of interface defects, the total $R_{DS(on)}$ of CoolSiC™ MOSFET M2 is not dominated by the MOSFET's channel resistance. Thus, the total $R_{DS(on)}$ is predominantly influenced by the drift region, so, at $V_{GS(on)}$ of 18V, the total $R_{DS(on)}$ exhibits a positive temperature coefficient in the complete temperature range. This behavior is beneficial for balancing current distribution in parallel devices [1], [11].

The MOSFET's channel resistance depends on the applied positive on-state gate voltage. The higher the on-state gate voltage the lower the $R_{DS(on)}$.

The on-state resistance, $R_{DS(on)}$, of CoolSiC™ MOSFET M2 as a function of junction temperature T_{vj} is shown in Figure 7 (a). At a rated current of I_{DS} = 25 A, the $R_{DS(on)}$ = 24.9 mΩ at T_j = 25°C, and $V_{GS(on)}$ = +18 V; at T_j = 25°C and $V_{GS(on)}$ = +15 V, the $R_{DS(on)}$ = 30 mΩ.

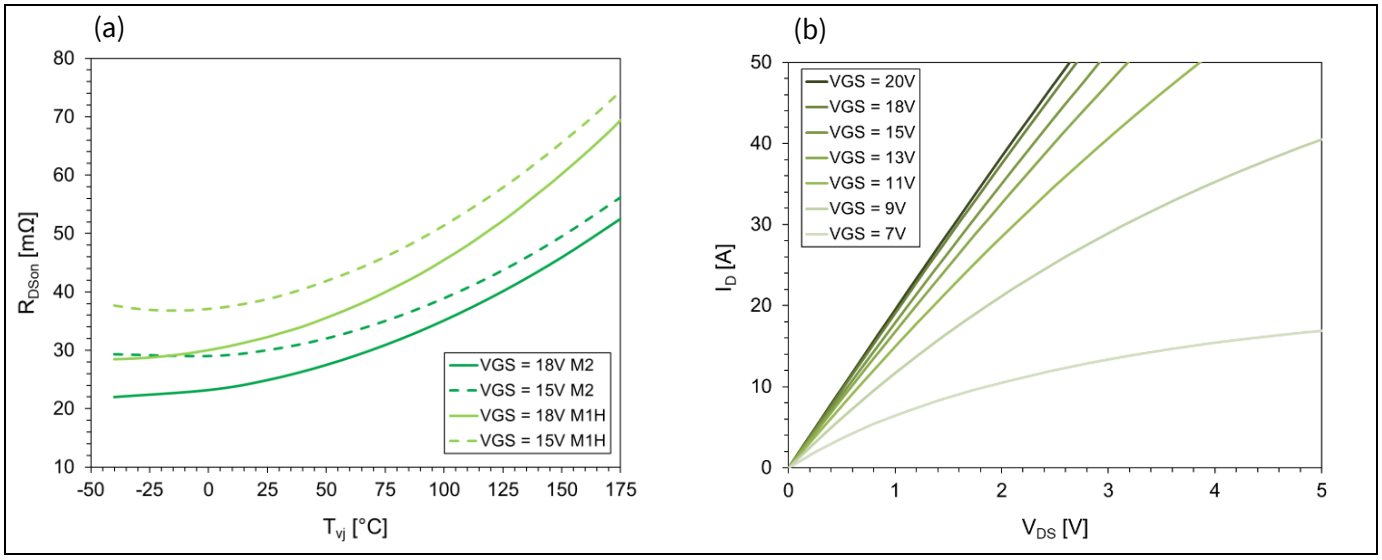

Figure 7 **(a) Typical on-resistance vs. junction temperature for M1H and M2 technologies. I_{DS} = 25 A, V_{GS} = 18 V and 15 V; (b) Typical output characteristics, V_{GS} = +7 to +20 V, with T_j = 175°C.**

Similar to the CoolSiC™ MOSFET M1H, it can be observed that the temperature dependence of the CoolSiC™ MOSFET M2 at $V_{GS(on)}$ = +18 V is more pronounced than for $V_{GS(on)}$ = +15 V. This is because at different on-state gate voltages the contribution of the MOSFET's channel resistance is lesser and the resistance of the epitaxial layer is more dominant [1], [11]. Furthermore, M2 shows a significant improvement in $R_{DS(on)}$ over the entire specified temperature range compared to its predecessor, M1H.

As the SiC MOSFET is a voltage-controlled device, it turns on gradually with increasing gate-source voltage. Due of the higher saturation current in M2, the right curves of Figure 7 are almost linear up to drain currents of about 50 A, even for gate-source voltages as low as 11 V. For higher drain currents or lower gate-source voltages, the current slope decreases significantly with increasing V_{DS}. This behavior is a consequence of the built-in junction field-effect transistor (JFET), which is formed by the deep p+ wells. As the p+ wells are linked to the source, the junction channel of the JFET is controlled by the drain-source voltage drop. Hence, the JFET channel narrows down with increasing V_{DS} [1], [11].

2.2.2 Body diode and synchronous rectification

The choice of the off-state gate voltage also has an impact on the performance of the body diode.
The CoolSiC™ MOSFET M2 integrates an intrinsic body diode with p-n junction behavior. As shown in Figure 8, the SiC devices with intrinsic bipolar body diode have a relatively high forward voltage V_{SD} (about 4.2 V at 25 A, V_{GS}= -3 V, T_j = 25°C) compared to silicon devices. The forward voltage drop changes with a negative gate voltage. At 0 V, the forward voltage is lower than at -5 V. The forward voltage, V_{SD}, has a negative temperature coefficient (about 3.9 V at 25 A, V_{GS}= -3 V, T_j = 175°C), and the temperature dependency is almost similar for gate voltages between 0 and -5 V.

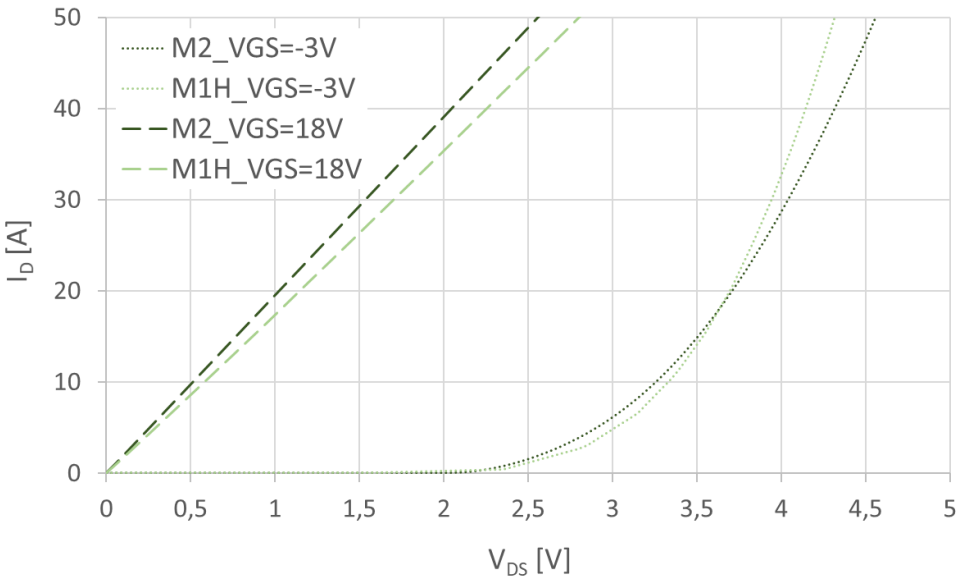

Figure 8 **Comparison between the third quadrant operation of CoolSiC™ MOSFET M2 and M1H chip at V_{GS} = 18 V and -3 V at T_{vj} = 175°C [3].**

Since the voltage drop is quite high, using the body diode to conduct current for long periods of time is not effective. The continuous current rating given in the datasheet is a theoretical value calculated based on T_H, T_{vjmax}, and conduction losses. When high currents are continuously applied through the body diode's path, it can result in an asymmetrical current distribution if chips are paralleled. This can potentially lead to a thermal runaway due to the negative temperature coefficient. However, operating at these current levels during typical deadtimes causes no issues.

Fortunately, the CoolSiC™ MOSFET M2 can conduct reverse current from the source to the drain through the channel if a positive bias is applied to the gate.

This mode of operation is called synchronous rectification (or third quadrant operation) and achieved by a positive on-state gate voltage of typically +15 to +18 V on the gate. As shown in Figure 8, the synchronous rectification mode is highly recommended for limiting conduction losses. Similar to the forward direction of the MOSFET, +18 V shows lower V_{SD} than +15 V [1].

Applying synchronous rectification has the additional benefit that the positive temperature coefficient of the MOSFET in reverse direction will support current sharing in case of paralleling. More details are provided in [1], [2] or [11].

2.2.3 Parasitic turn-on

Many applications that use the CoolSiC™ MOSFET M2 modules try to minimize switching losses by accepting steep transients in voltage and current. Therefore, the immunity of the device against parasitic turn-on is paramount. The CoolSiC™ MOSFET M2 shows a comparable behavior to the CoolSiC™ MOSFET M1H. Comprehensive details can be found in [1].

2.2.4 Gate-charge and gate-driver output power rating

The total gate charge, Q_G, is defined as the charge from the origin (e.g., $V_{GS(off)}$ = - 3 V) to the point on the curve where the driving voltage equals the actual gate-to-source voltage of the device (e.g., $V_{GS(on)}$ = 18 V). Thus, the choice of the on-state and off-state gate voltage has an impact on the share of the gate charge required when a lower voltage range is used for driving. As already mentioned, reducing the pitch increases the number of trenches, therefore the gate charge, Q_G, of M2 is higher for the same active area as compared to M1H. Figure 9 shows the gate-charge characteristic at I_{DS} = 25 A for both M2 and M1H technologies. As can be seen, M2 has an approximately 20% higher Q_G of 0.089 µC at $V_{GS(on)}$ = 18 V. This higher gate charge is attributed to the improvement of $R_{DS(on)}$. When considering the scaled gate charge for the same $R_{DS(on)}$ (scale from 24.9 mΩ of M2 to 32.3 mΩ of M1H), it can be seen that at the same $R_{DS(on)}$, Q_G is lower.

This means the required output power (P_{GD}) for the gate driver can be derived depending on the applied gate-source voltage. This increase in Q_G must be considered when selecting the appropriate gate driver and driving power.

- $P_{GD} = f_{sw} \times Q'_G \times \Delta V_{GS}$
- f_{sw} = Switching frequency of the SiC MOSFET
- Q'_G = Gate charge, reading taken from a diagram for the voltage range actually used
- $\Delta V_{GS} = |V_{GS(on)}| + |V_{GS(off)}|$ (steady state values)

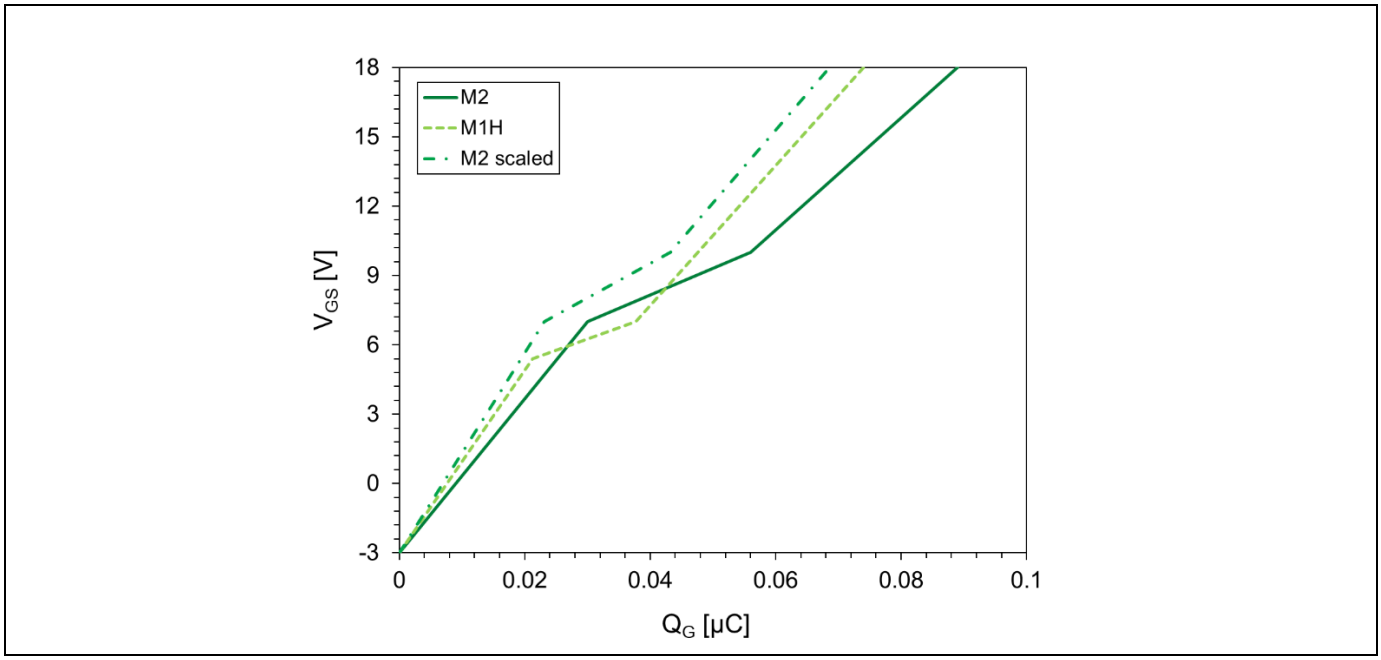

Figure 9 **Typical gate charge values for M2 compared to M1H for $V_{GS} = f(Q_G)$, I_{DS} = 25 A, V_{DS} = 800 V, and T_{vj} =25°C; turn-on pulse.**

2.2.5 FIT rates versus V_{gs} and lifetime

The bathtub curve, which is shown in Figure 10, is widely used to describe the FIT rates. The bathtub curve can be divided into three parts:

- The first part with a decreasing failure rate, also known as early failure. Screening processes in the production lines sort out the weak devices and exclude them from the field
- The second part shows a constant, flat failure rate. For SiC MOSFETs, this area is mainly defined by gate oxide failures and cosmic ray effects
- In the third and last part, an increasing failure rate can be observed. This section is also known as the wear out (intrinsic material failures like bond wire lift off, solder degradation or DCB degradation)

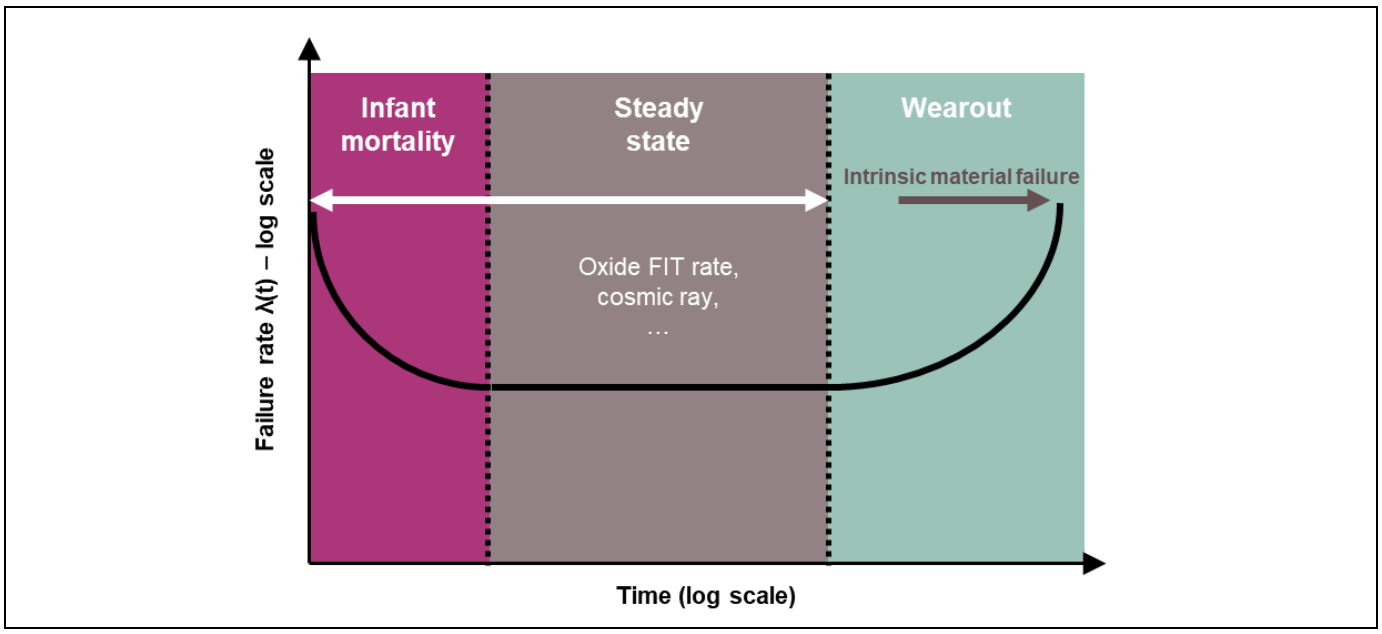

Figure 10 **A typical bathtub curve.**

For on-state operation, a larger gate-source voltage window of V_{GS} = +15 to +18 V for the CoolSiC™ M2 products is recommended. For off-state operation, a V_{GS} of 0 to -5 V is recommended. The trade-off between a longer lifetime and performance is well balanced at this operating voltage. Exceeding the gate voltage range specified in the absolute maximum ratings can lead to immediate device destruction, or cause early degradation for sure. However, operating within the recommended range, gate voltages up to 18 V is recommended, resulting in a reduction in on-resistance. In cases where a negative gate voltage is required, the specific voltage level depends on the intended switching speed and the proximity of the driver to the die, with CoolSiC™ MOSFET M2 typically requiring a small negative voltage of -2 to -4 V, even under high switching speeds and unfavorable conditions.

In general, Infineon devices could be driven with gate-source voltages higher than 18 V. However, this reduces the lifetime of the gate oxide because the gate-oxide stress rises, accelerating the aging of the device. The failure rates also increase if gate-source voltages higher than 18 V are used.

For operating conditions that deviate from Infineon recommendations, please consult your Infineon contact for impact on lifetimes and FIT rates [1].

3 Dynamic behavior – switching performance

An external gate resistance impacts the switching speed critically and must be chosen carefully. Constraints on V_{DS} and V_{GS} under different operating conditions should be kept in mind for both active and passive switches. Exceeding these limits can cause irreversible drift in the electrical parameters or accelerate degradation, leading to a shorter lifetime. Higher external gate resistance also means slower switching speed and higher switching losses. This necessitates the identification of a sweet spot that balances both switching speed and reliability [1], [11].

With a low-inductive design, the drain-source voltage overshoot (passive switch during turn-on and active switch during turn-off) can be reduced significantly. Both E_{on} and E_{off} can be reduced by reducing the DC-link inductance or selecting a smaller R_G. For the M1H technology, an approximately 40% improvement in E_{tot} was achieved by reducing the stray inductance of the setup from 38 nH to 15 nH. More details are provided in [1]. All Easy C-series modules equipped with CoolSiC™ MOSFET M2 are characterized standardly with a low stray inductance setup with 15 nH.

A gate driver that aligns with the recommendations outlined in [8] and [9], and features minimal gate-loop inductance is advantageous in fast switching applications. This strategic design approach not only enhances the overall performance but also helps mitigate switching-related challenges.

Double-pulse testing (DPT) can be used to evaluate the switching performance of the CoolSiC™ MOSFET M2 under various dead time conditions. In [12] you can find more detailed information of DPT and the related challenges.

This chapter discusses the impact of dead time on switching energy losses and how this information is presented in the module datasheets.

3.1 Dead time definition

Dead time refers to the brief period, typically in the range of 100 to 1000 nanoseconds (ns), when both the high-side and low-side switches are turned off simultaneously. This interval is necessary to prevent the shoot-through currents and ensure a reliable, damage-free design. Infineon defines dead time as the time between the on and off pulse-width modulation (PWM) signals, as explained in Figure 11. To set an appropriate dead time, any additional gate driver and delays in switch reaction should be considered [1].

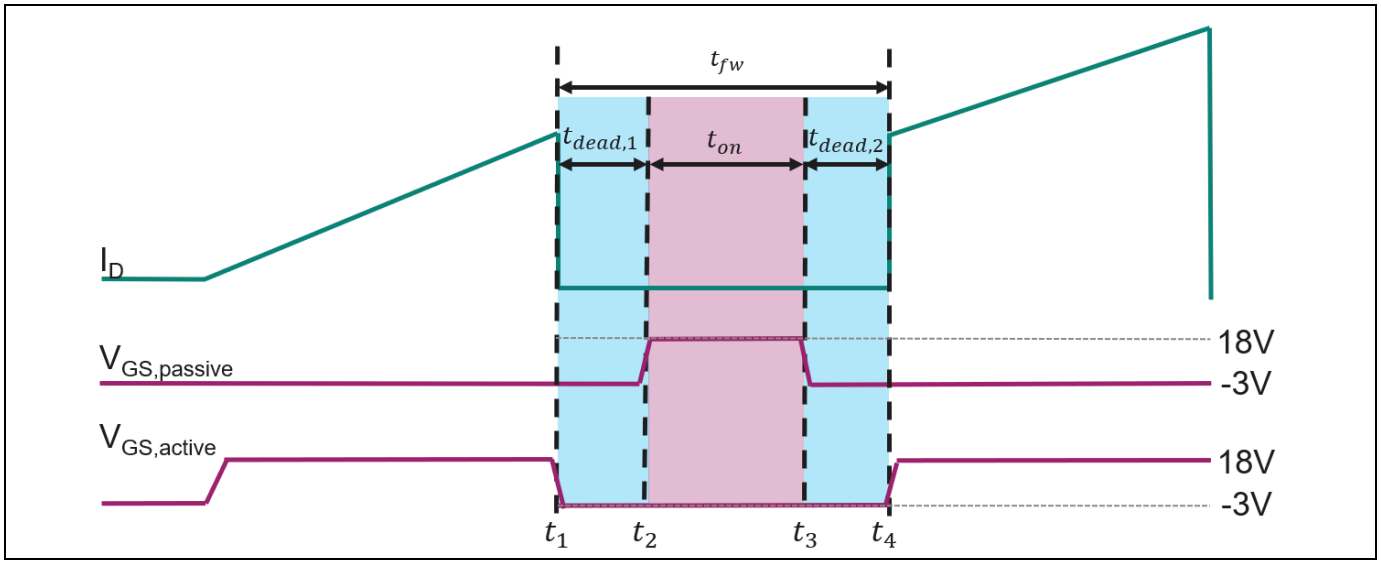

Figure 11 **Definition of dead time.**

Dynamic behavior – switching performance

During dead time, the body diode conducts the load current and the stored charge accumulates in the body diode. When the voltage direction changes, a high dv/dt is applied to the body diode, causing a high di/dt and consequently, a voltage overshoot. Thus, optimizing the dead time is important.
The dead time should be long enough to mitigate the risk of short circuits but short enough to minimize the voltage peak, V_{rmax}, which is caused by the body diode's reverse recovery during turn-on. Whenever possible, the t_{dead} value should be lowered so that the device does not reach its equilibrium stage, thus minimizing Q_{rr}. This in turn decreases the turn-on energy loss, E_{on}, and the recovery loss, E_{rec} [10].

3.2 Switching behavior at different dead times

Reducing the pitch has a minimal impact on the capacitances, such as C_{oss}, C_{iss}, and C_{rss}, resulting in a similar overall switching behavior between M1H and M2 devices. The devices were operated within the specified voltage limits given in the datasheet, whichwas achieved by carefully adjusting the external R_G based on specific load conditions, system stray inductance, and dead time.

Figure 12 depicts the typical switching behavior of a half-bridge module featuring CoolSiC™ MOSFET M2 (with three dies in parallel per leg), under the following measurement conditions:

- V_{DD} of 800 V
- I_D of 75 A
- V_{GS} of -3 V/+18 V

The figure presents a direct comparison between the switching behavior at two different dead times – 1000 ns and 100 ns. The measurements were taken at T_{vj} = 25°C and 175°C, with an identical external R_G in both cases.

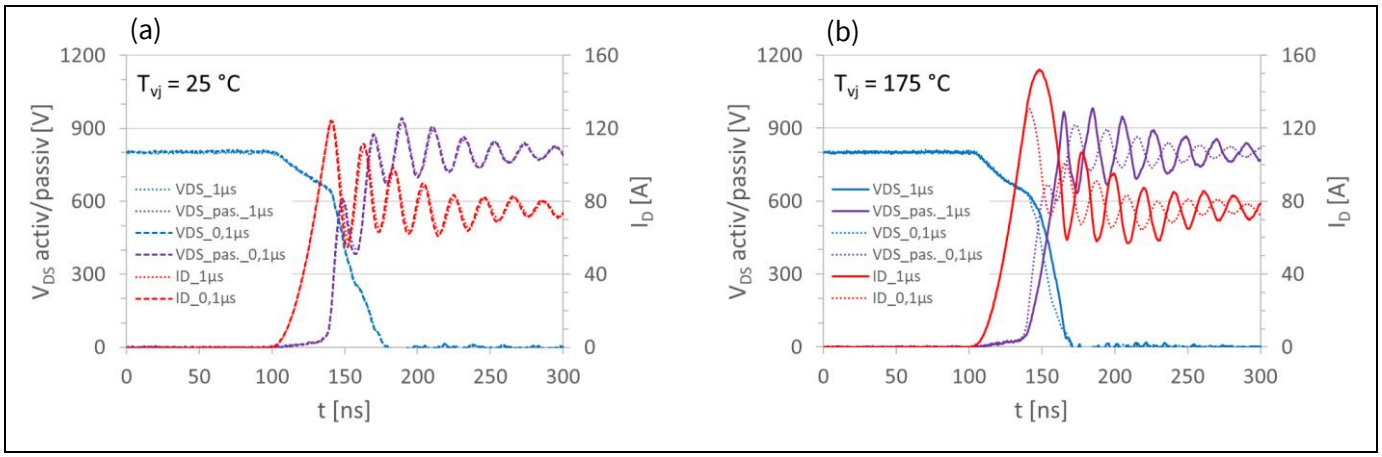

Figure 12 **Comparison between the switching behavior at two different dead times and temperatures for a half-bridge CoolSiC™ MOSFET M2 module [3].**

For a dead time of 100 ns at T_{vj} of 175°C (as seen in Figure 12 (b)), the overvoltage peak for $V_{DS\_pas.}$ of the passive switch decreases by over 50 V. This effect is negligible at a T_{vj} of 25°C due to the reduced bipolar charge in the body diode.

The results indicate that the dead time has a significant impact on the usability of an application. It facilitates faster switching while concurrently reducing switching losses at application relevant temperatures. The impact of dead time on switching losses at higher temperatures is shown in Figure 13.

Dynamic behavior – switching performance

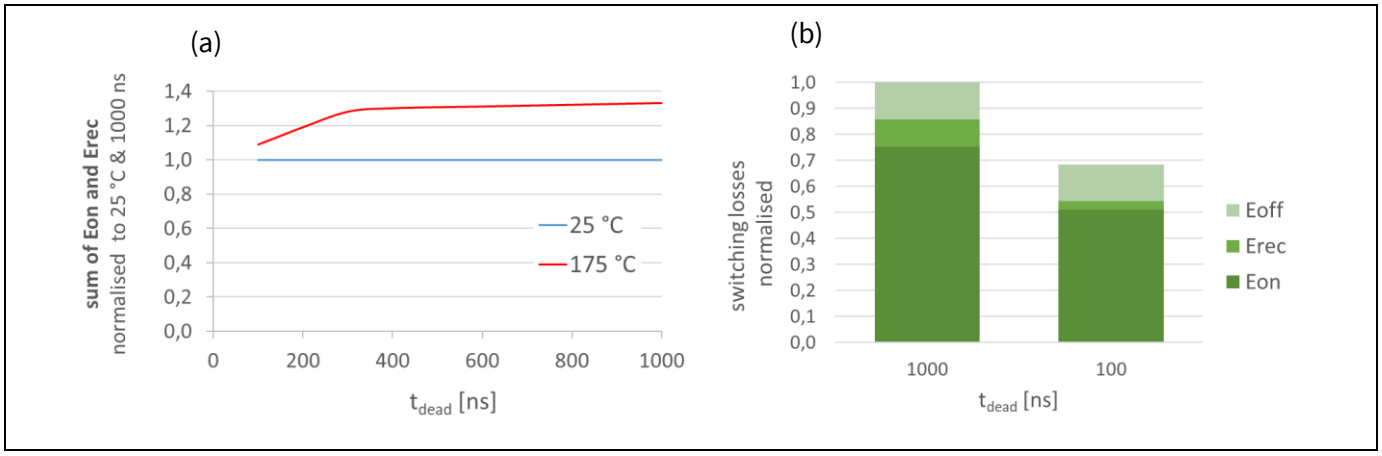

Figure 13 **Influence of the dead time duration on switching losses at Tvj = 175°C. (a) switching loss changes over different dead time durations. (b) switching losses changes over a dead time of 1000 ns and 100 ns with an optimized $R_{Gon,o}$ [3].**

Figure 13 provides a general illustration of the influence of dead time on switching losses. Notably, at 25°C, the losses remain unaffected by dead time, whereas at 175°C, a significant reduction in losses is observed for shorter dead times. A further comparison is presented in Figure 13 (b), which compares the switching losses at dead times of 1000 ns and 100ns at a T_{vj} of 175°C. As can be seen, at a dead time of 100 ns, E_{on} decreases by more than 30%, while E_{rec} decreases by over 60%. The performance gain is amplified when R_{Gon} is optimized, as a low dead time minimizes the voltage peak, enabling faster switching. Therefore, at a dead time of 100 ns with an improved R_{Gon}, the total switching losses reduce by over 30% compared to the losses at a dead time of 1000 ns with standard R_{Gon}.

This dependency of switching losses on dead time is included in the datasheets of all modules equipped with the CoolSiC™ MOSFET M2. Additional diagrams are provided to illustrate the normalized switching losses as a function of dead time at nominal current and nominal gate resistance. This information is also included in the tabular section of the product datasheets, where values corresponding to low dead time are marked as “optimized” or with an “o” suffix. Note that the lowest achievable dead time may vary from product to product. Comprehensive details and exemplary diagrams can be found [1].

Even when a low DC-link inductance and a low dead time are implemented, the gate-source voltage can be a limiting factor that restricts the possibility of faster switching if it reaches its maximum limit of 25 V or -10 V. The easiest way to check is by measuring the voltage at the gate-source terminals. However, this does not have a direct relation to the undershoots and overshoots endured by the die. Overshoots and undershoots are influenced by internal inductances of the gate loop, the internal resistance of the SiC MOSFET, and the resistance inherent in the layout design itself. To assess the actual voltage experienced by the die, an approach for post-processing signals is discussed in [10]. For additional guidance on the evaluation, reach out to your Infineon contact person.

4 .XT interconnection technology

Infineon's innovative .XT (**ex**tended life**t**ime) interconnection technology represents a significant breakthrough in mitigating the stress and strain on the SiC dies that can lead to its delamination from the lead frame. One approach for achieving the required lifetime in applications has been to increase the chip size, thereby reducing the temperature and thermal stress. However, this approach is not sustainable, as it can compromise power density and results in higher costs due to the oversized chips.

To overcome these limitations and enhance both the power density and lifespan, Infineon has introduced a more advanced interconnection technology. Modules in the Infineon EasyC series leverage the .XT technology, building upon the proven concepts of IGBT5 PrimePACK™ and the 3.3 kV CoolSiC™ MOSFET XHP2 modules [5]. This innovative approach addresses the challenges associated with the stress and strain on the SiC dies effectively, while delivering improved performance and reliability.

The .XT technology for Easy modules combines high lifetime die attach with a copper frontside interconnection technology. It not only improves the thermal performance but also offers tremendous advancements in power cycling. A principle sketch of the .XT technology is shown in Figure 14.

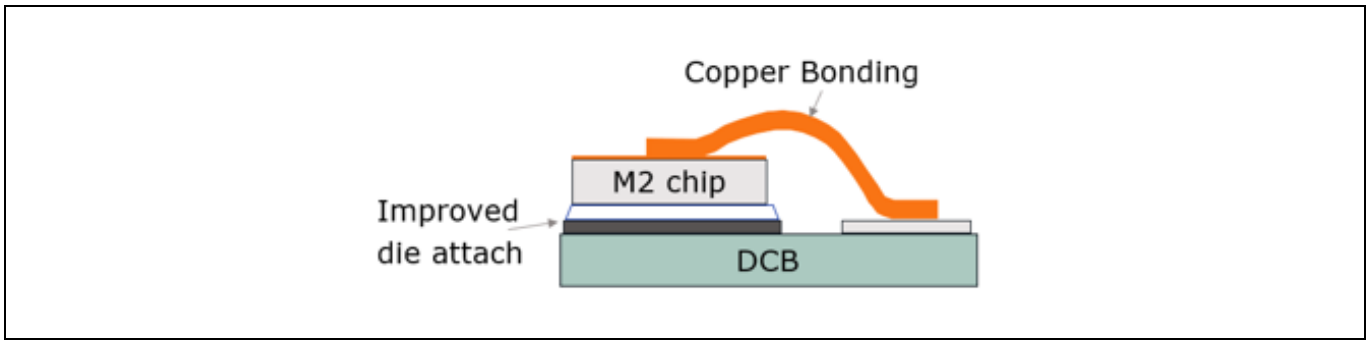

Figure 14 **Infineon .XT interconnection technology.**

The .XT technology employs a high lifetime die attach, which significantly reduces solder voids and minimizes the solder layer thickness. This approach ensures a robust die attachment, enhancing overall reliability. This technology also offers a high tensile strength, which improves power cycling robustness.

With this technology, soldering degradation is no longer the primary weak point in power cycling tests, and the bottleneck shifts to bond lift-off. To address this challenge, a more robust copper bonding process has been introduced, made possible by the copper frontside metallization on the chip. This combination of advanced soldering and bonding techniques improves the power cycling capability substantially, with more than 20x increase in endurance for the same temperature delta (ΔT). These enhancements shift the end-of-life cycle count to levels that are beyond the requirements of current applications, effectively extending the lifespan of the device.

4.1 Power cycling and reliability

The EasyC series featuring the .XT chip interconnection technology is tailored to meet the power cycling demands of applications such as EV charging, energy storage systems, solar inverters, and many others. With a power cycling improvement of over a factor of 20 compared to standard interconnection technologies, the .XT interconnection technology addresses application relevant requirements such as:

- Thermal cycling up to 10 k cycles/year,
- Longer cycle times from 15 minutes up to 1 hour,
- Changing operation modes
- Huge temperature cycles of up to 100 K

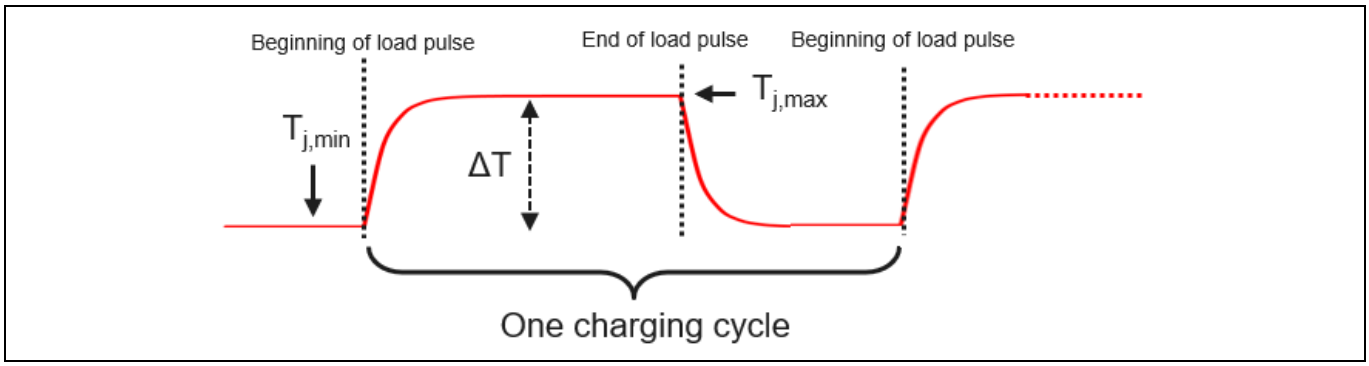

Figure 15 **A typical charging cycle.**

The power cycling capability of SiC devices that utilize traditional interconnection technologies, such as soft solder and aluminum bond wires, is lower than that of silicon (Si) devices in the same current and voltage classes. This disparity is attributed to the distinct material properties of silicon carbide, which differ from those of silicon. As a result, the primary aging mechanism in SiC devices shifts from other factors to the degradation of the chip solder, making it a critical lifetime concern [4].

In [3], a power cycling test was conducted on a densely packed module featuring nine paralleled SiC MOSFETs. The module was subjected to stress conditions such as $T_{vj,max}$ > 175°C and ΔT ≈ 130 K with a 30-second turn-on time. The modules withstood over 90,000 cycles, surpassing the extrapolated specification of traditional interconnection technology by a factor of over 20. Despite the harsh stress conditions, no end-of-life signs were observed in the interconnection layer, as confirmed by both electrical data and analysis. Ultrasonic microscopy images revealed a rounding of the ceramic substrate around the chips. This is consistent with previous findings in baseplate-less modules using the .XT silicon technology, demonstrating the exceptional reliability and durability under extreme conditions offered by the .XT technology.

The results in [3] indicate that the combination of .XT interconnection technology and the latest CoolSiC™ MOSFET M2 technology in the EasyC series can overcome the disadvantages of SiC with respect to power cycling, without compromising other reliability tests. For more detailed information regarding power cycling and reliability, please refer to [3] or the respective Product Qualification Report (PQR).

5 Package technology – the EasyC series

In addition to advancements in the chip technology, Infineon launched a new package family – the EasyC series. While retaining many features and properties of the earlier products in EasyB series, the EasyC series boasts a groundbreaking housing concept, as illustrated in Figure 16, which offers a new approach to package design and functionality.

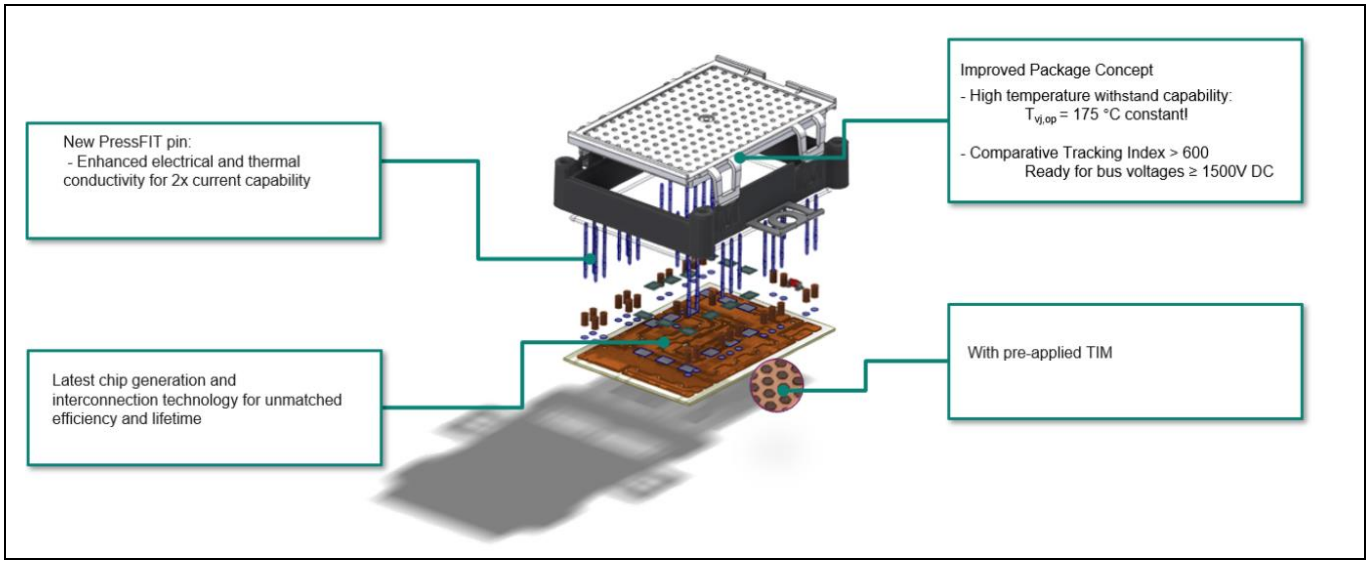

Figure 16 **New features of the EasyC series package family.**

The EasyC series package is designed to be mechanically compatible with the versatile EasyB series, ensuring effortless integration, reduced manufacturing complexities, and enhanced automation capabilities. This compatibility, combined with its ability to support higher power density, flexible layout, and power pin arrangements, makes the EasyC series an ideal platform for cutting-edge technologies such as the CoolSiC™ M2 MOSFET .XT. It enables the development of future designs with, for example, higher voltage classes, unlocking new possibilities for power electronic applications.

5.1 Package concept

A new mechanical concept, featuring a separate frame and lid, enables the use of advanced materials that have a high comparative tracking index (CTI) of over 600, offering more design flexibility. This innovative design also offers more flexibility in pin layout, which minimizes stray inductances, and is well suited for high-voltage applications that have bus voltages of ≥ 1500 V DC.

The clearance and creepage distances for the EasyC series are given in [7].

The EasyC series provides the capability to operate continuously at virtual junction temperatures of up to 175°C under switching conditions, if required. In addition, the package can withstand up to 200°C under overload conditions for a maximum of 100 hours (cumulative), which makes it perfect for mitigating failure events in applications. The datasheet definition is shown in Figure 17.

Temperature under switching conditions	$T_{vj\ op}$		-40		175	°C
Temperature under overload switching conditions	$T_{vj\ over}$	Overload, cumulative max. 100 h			200	°C

Figure 17 **Datasheet definition of temperature under (overload) switching conditions.**

5.2 Pre-applied TIM 2.0

Infineon has introduced a new thermal interface material, TIM 2.0. It is designed to meet the demanding requirements of a wide range of applications. This advanced material boasts of exceptional wetting properties, making it ideal for high-performance applications and providing a significant value-add to customer products. To facilitate easy identification, Infineon has incorporated the letter “Q” into the product names of devices that utilize the TIM 2.0 technology.

TIM 2.0, formerly known as PTM6000HV-SP, is a phase change material (PCM). Its polymer structure undergoes a phase change from solid to soft at temperatures above 45°C. Below the melting temperature of 45°C, it maintains a wax-like consistency. To ensure complete phase change, heat the TIM to above 60°C once after assembly. TIM 2.0 offers several key benefits, including:

- Enhanced thermal performance due to high thermal conductivity of 5.2 W/mK and excellent wetting properties that reduce contact resistance
- High resistance to pump-out, even in vertically mounted power modules
- Proven long-term stability and competitive thermal performance, making it ideal for high power density applications and long device lifetimes
- Increased continuous operating temperature limit of 150°C for TIM 2.0
- Long term stability as perfect match for .XT

More information on the technical properties, reliability, and handling of TIM 2.0 is provided in [6].

5.3 High-current PressFIT pin

The new high-current PressFIT pins from Infineon offer significantly enhanced electrical and thermal performance, doubling the current capability. These advanced pins are designed to alleviate thermal stress on the PCB and improve tolerances, facilitating process automation during press in. Its key features and main benefits are:

- A new material with 3.5 times higher electrical and thermal conductivity to reduce hot spots on PCB
- An innovative “Eye of the needle” press-fit zone design
- An optimized design to reduce the sliding effect into the rivet
- A new pin placing process that ensures higher accuracy
- No changes from PCB specifications for standard PressFIT pin, ensuring seamless integration
- Compatible with all Easy series designs, providing a versatile solution

Comprehensive assembly instructions, and creepage and clearance distances are provided in [7].

6 Application tests

To perform a comparative analysis of the new chip generation, simulations and measurements of a typical setup in an application were conducted.

6.1 Simulation

Typical setup configurations for EV charging were simulated to evaluate the performance of our solutions in the Power Factor Correction (PFC) stage under hard-switching conditions. The analysis focused on solutions with the Easy2 footprint with identical chip sizes, specifically comparing the 11 mΩ M1H product with the 8 mΩ M2 product. Two variants of the M2 were considered, taking into account high (1000 ns) and low (100 ns) dead time.

The M2 EasyC series enables further optimization of the Direct Copper Bonded (DCB) layout and the use of the new pre-applied TIM 2.0. The simulation results, based on dedicated operating conditions of the PFC stage in an EV charger, are shown in Figure 18.

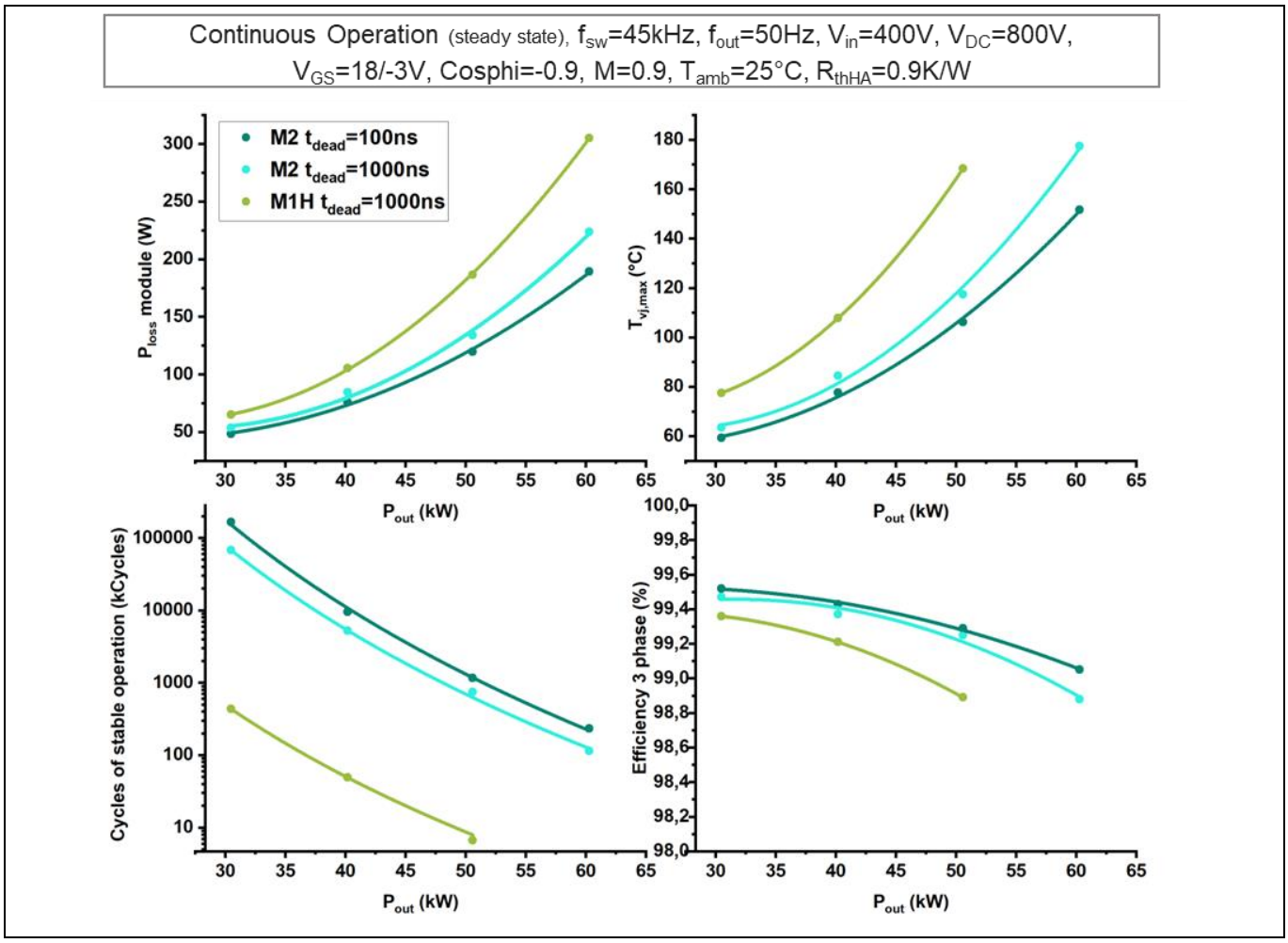

Figure 18 **Simulation results of the PFC stage with typical operating conditions of an EV charger with different power ratings.**

Application tests

The results show a substantial enhancement in performance with the EasyC M2 solution, which successfully delivered 60 kW to 74 kW power without surpassing the junction temperature limits. Notably, this was achieved while maintaining efficiency levels similar to the M1H solution, which was restricted to 50 kW.

The .XT technology integrated into the M2 solution demonstrated a remarkable extension of operational lifetime for EV charging applications. In contrast to the M1H solution, which had a lifespan of just over a year when subjected to 15 fast charging cycles per day, the M2 solution showed the capability of operating for over 18 years under the same conditions. This significant increase in lifespan is a direct result of the advanced technology, as standard SiC technologies with conventional interconnection technology typically require power and junction temperature limitations to achieve comparable lifetimes.

Figure 19 illustrates the potential output power using the same operating conditions as before but applying different cooling conditions. $R_{th,HA}$ represents the heatsink-ambient thermal resistance.

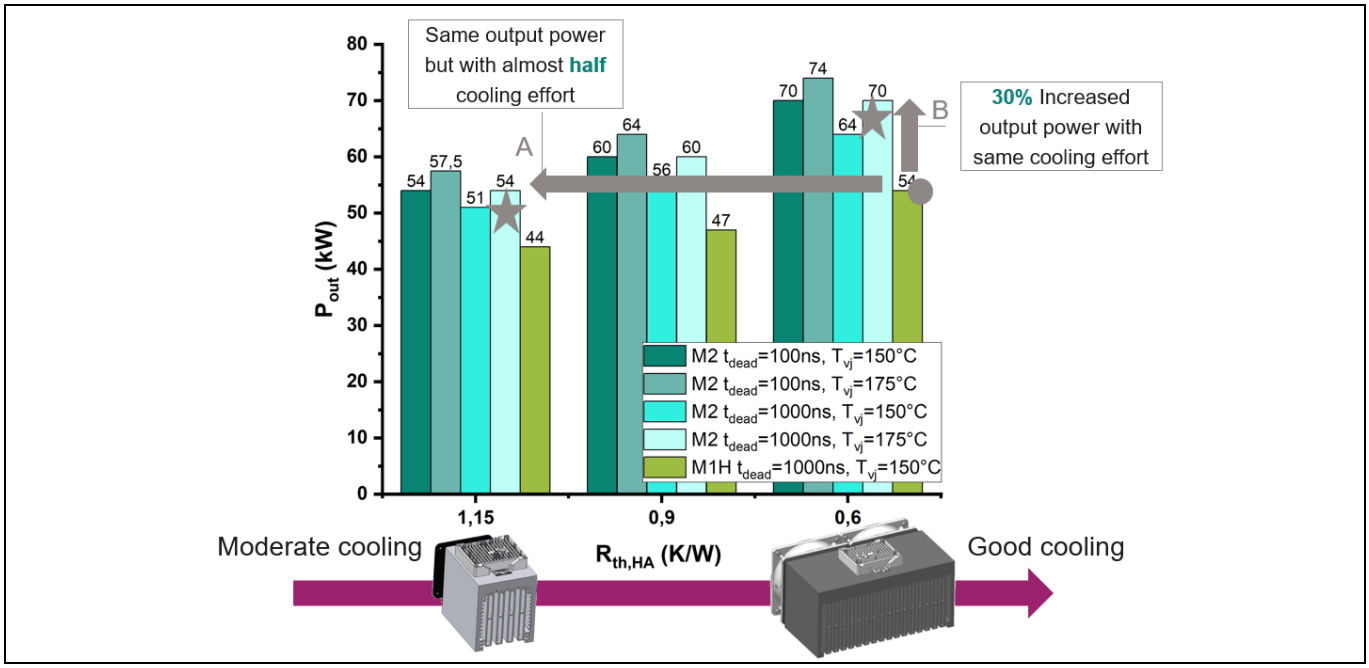

Figure 19 **Simulation results of the PFC stage with different cooling conditions.**

The improvement from M1H to M2 offers several advantages, such as higher power ratings without sacrificing efficiency or lifetime, or the implementation of cost-effective measures such as lower cooling power. The same 54 kW power rating can be achieved with M2 under moderate cooling conditions ($R_{th,HA}$ = 1.15 K/W) compared to M1H that requires good cooling conditions ($R_{th,HA}$ = 0.6 K/W). This is made possible because of reduction in losses and the ability to operate at 175°C continuously with the CoolSiC™ MOSFET M2.

With the CoolSiC™ MOSFET M2, it is possible to increase the output power by 30% while maintaining the same cooling effort, or to achieve the same output power with almost half the cooling effort. In soft-switching DC-DC stages, the performance improvement is even more significant due to the substantial $R_{DS(on)}$ enhancement in M2, which reduces conduction losses. All these advantages eventually lead to enhanced overall efficiency, improved performance, and increased reliability of the devices.

6.2 Measurements

To validate the performance improvements observed in simulations, actual application tests were conducted using a single-chip SixPACK™ as the test vehicle. The tests compared the performance of a 25 mΩ M2 device and a 33 mΩ M1H device under identical operating conditions. The results, as shown in Figure 20, demonstrate a clear improvement in performance for the M2 solution, highlighting the benefits of using the M2 device in real-world applications.

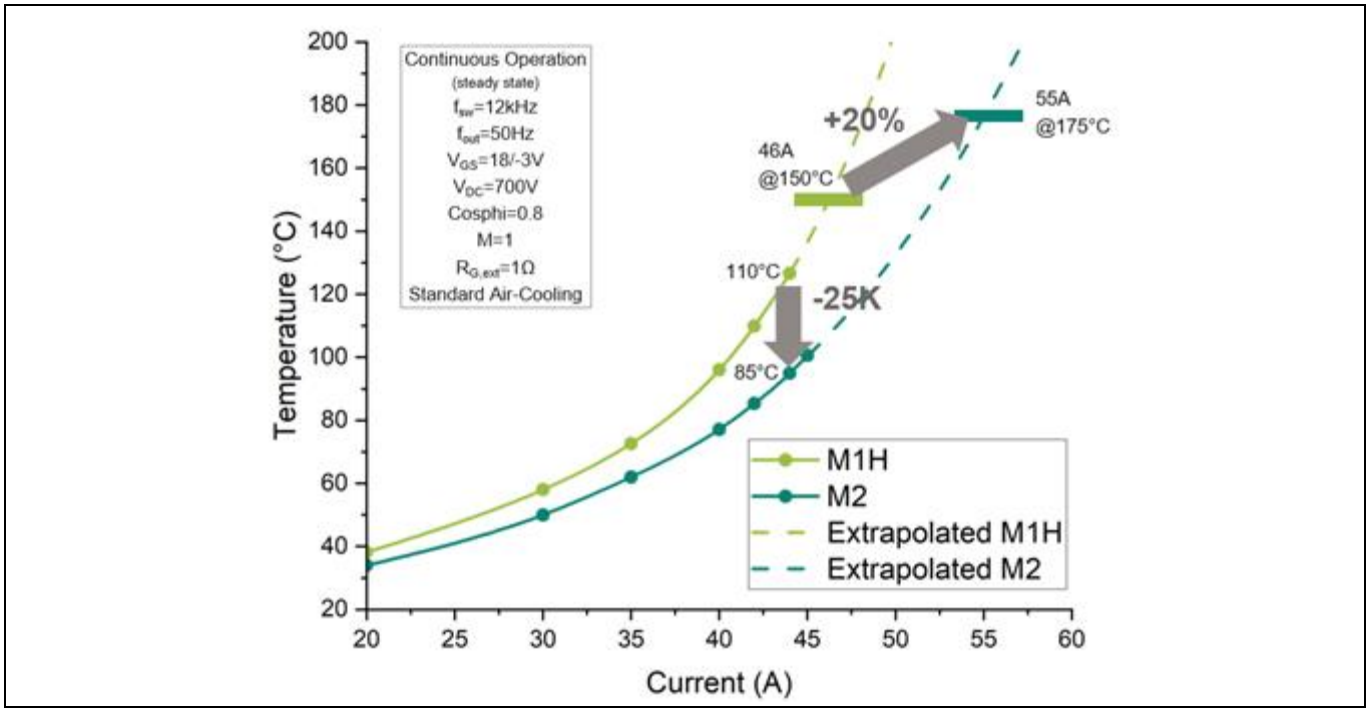

Figure 20 **Application measurement results – temperature versus current**

The M2 device offers two distinct advantages over its predecessor. It can either operate at a 20% higher output power, or maintain the same power rating while reducing the junction temperature by 25 K. Note that these improvements are solely attributed to the new chip and interconnection technology, as the same layout and thermal interface material were used in both samples.

The test results, demonstrate substantial enhancements with the M2 EasyC series solution. This confirms the expected benefits of the M2 technology.

7 Glossary

$R_{DS(on)}$ Resistance at the actual junction temperature, given at the datasheet current, I_{DS}

$V_{GS(th)}$ Voltage between the gate and the source at which the current starts to flow

I_{DSS} Drain-source leakage current at shorted gate-source voltage = 0 V and V_{DSS} = 1200 V

V_{GS} Bias between the gate and the source, corresponds to V_{ge} in an IGBT

I_{DS} Load current flowing between the drain and the source

V_{DS} Bias between the drain and the source, corresponds to V_{ce} in an IGBT

C_{rss} Effective capacitance between the gate and the drain. It is measured at 800 V, which is the typical DC-link voltage in AN application. It is equal to the gate-drain capacitance

C_{gs} Effective capacitance between the source and the gate

C_{iss} Effective capacitance between the gate and the source. It is measured at 800 V, which is the typical DC-link voltage in an application. It is equal to the sum of gate-source capacitance and gate-drain capacitance

C_{gd} Effective capacitance between the drain and the gate

C_{oss} Effective capacitance between the source and the drain. It is measured at 800 V, which is the typical DC-link voltage in an application. It is equal to the sum of gate-drain capacitance and gate-source capacitance

C_{ds} Effective capacitance between the source and the drain

R_{G_int} Effective internal gate resistance, comprising the sum of the resistance of the distributed gate network and additional resistors added to the gate pad

E_{on} Turn-on energy loss, measured according to IEC 60747-8

E_{off} Turn-off energy loss, measured according to IEC 60747-8

E_{tot} Total energy loss, sum of E_{on} and E_{off}

Q_{GD} Typically gate charge needed to pass the Miller plateau

Q_G Total gate charge

$Q_{GS,pl}$ Gate charge required to reach the Miller plateau from the off-state, V_{GS}

R_G Externally applied gate resistance, adds to R_{G_int}

$R_{G(on)}$ Externally applied gate resistance for turn-on

$R_{G(off)}$ Externally applied gate resistance for turn-off

$T_{vj\,op}$ Virtual junction temperature during operation. The term “virtual” refers to a temperature measured by temperature-sensitive electrical parameters as described in the IEC 60747 standards

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Revision history

Document version	Date of release	Description of changes
Revision 1.0	2025-06-02	First release

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Edition 2025-06-02

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN-2025-02

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