CIPOS™ IPM simulation in IPOSIM

Application note

About this document

Scope and purpose

This application note describes the IPM simulation model in Infineon power simulation(IPOSIM).

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

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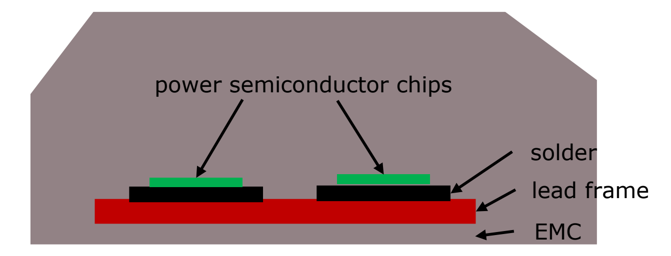
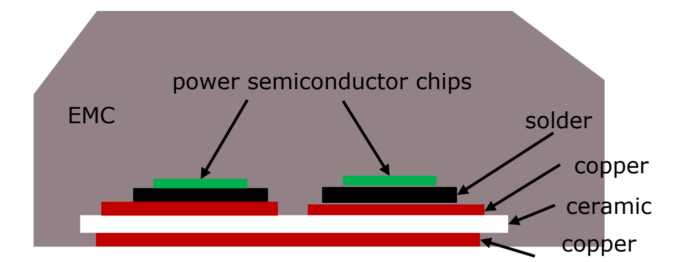
1 Thermal impedance

The internal structure of intelligent power module (IPM)s required to extract thermal impedances is shown in Figure 1. The fully molded package has epoxy molding compounds (EMC) at the top of the power chips and at the bottom of the lead frame, as shown in Figure 1 (a). The heat generated from the power chip is transferred to the heat sink through the solder, leadframe, and EMC. Figure 1 (b) shows a package with direct copper bonding (DCB), in which the heat from the power semiconductor chip is transferred to the heat sink through solder, copper, ceramic, and substrate.

To extract the thermal impedance, the chips should be heated by passing a current through them and then measuring the difference between the chip and the case temperature.



(a) Internal structure of a fully molded package

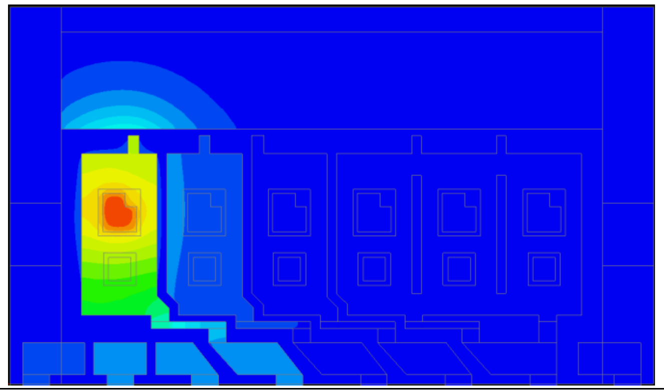


(b) Internal structure of a DCB package

Figure 1 **Internal structure of IPM packages.**

1.1 Single-chip heating

Figure 2 shows the thermal impedance extraction process in the case of single-chip heating. When current is passed through the IGBT or the diode, the temperature of the chips increases due to power losses. The thermal impedance between the junction and the case can then be extracted. These values are given in the datasheet taking into account the worst condition margins.


Single-chip heating (IGBT)

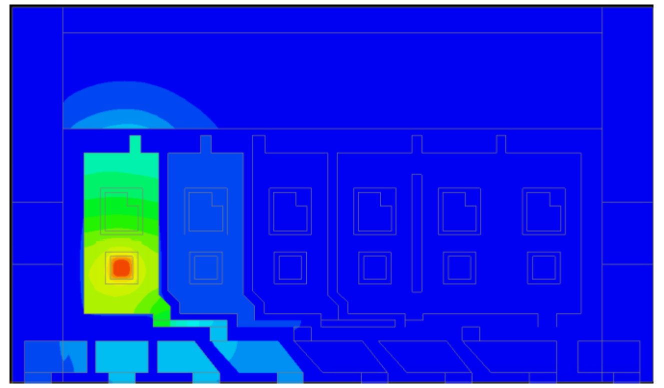

Single-chip heating (diode)

Figure 2 **Simulation of extracting thermal impedance in the case of single-chip heating.**

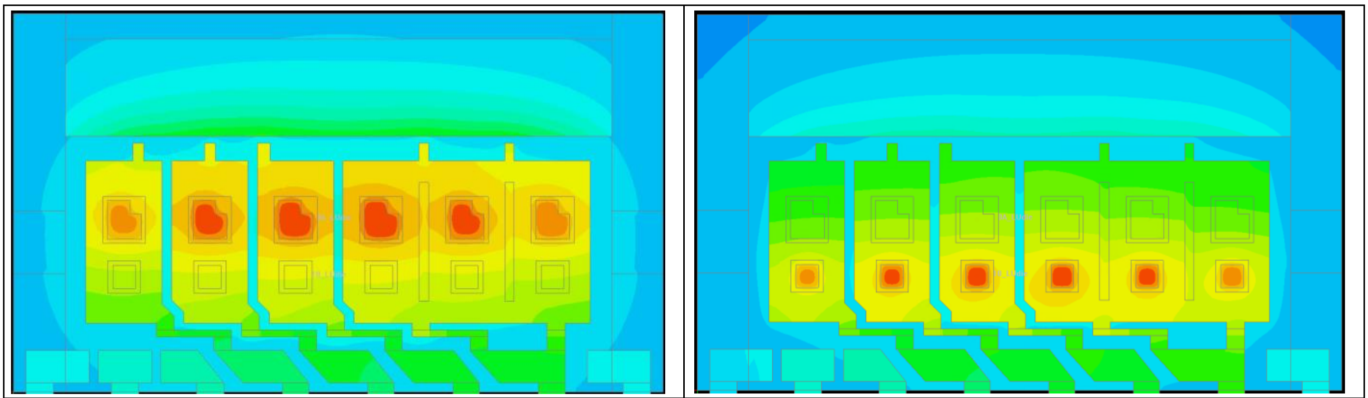
1.2 Multichip self-heating and thermal coupling

Figure 3 shows the process for extracting thermal impedance under multichip self-heating conditions considering the temperature of multiple chips. When all IGBTs are in the ON state, the thermal impedance of the hottest IGBT is extracted (Figure 3(a)). The thermal impedance of the diodes is also extracted in the same way. During operation, thermal interference occurs in all the power chips. This is because multiple power chips are clustered closely in the IPM package. The temperature, resulting from power loss, of all the chips has a thermal effect. The thermal effect between the chips should be considered because all the IGBTs and diodes operate continuously according to the switching cycle in an inverter operation.

As the IGBTs and the antiparallel diodes are close together and operate complementarily, the heat affecting the diode when the IGBT operates or the heat affecting the IGBT when the diode operates must be considered. In this document, this effect is called thermal coupling. To consider this effect in an IPM, the thermal coupling coefficient should be extracted by measuring the IGBT temperature with all the diodes turned ON, as shown in Figure 3(b). Conversely, the thermal coupling coefficient of the diode is extracted by measuring the diode temperature with all the IGBTs turned ON, as shown in Figure 3(a).

The thermal coupling coefficient is extracted in the form of a foster thermal impedance model and is based on the hottest IGBT or diode. The temperature arising due to thermal coupling coefficients is added to the IGBT and diode in the simulation. The thermal impedance modeling is discussed in detail in the next chapter.

As mentioned before, to estimate the actual junction temperature accurately in simulation the values from multichip heating and thermal coupling coefficient should be considered.

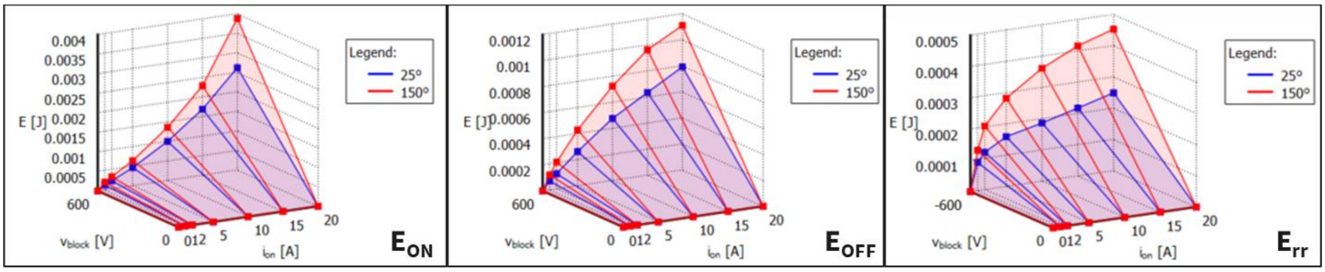


(a) Multichip heating (IGBT)	(b) Multichip heating (diode)

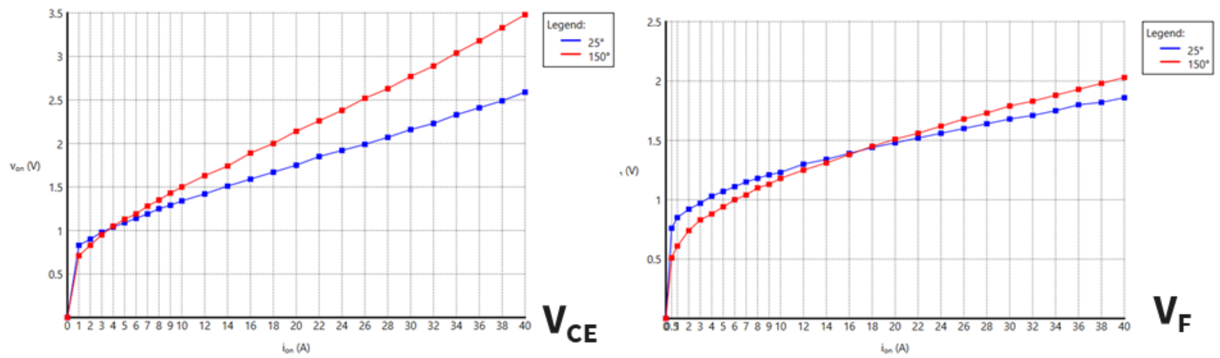
Figure 3 **Simulation of extracting thermal impedance in the case of multichip heating.**

2 IPM simulation modeling

IPOSIM provides simulations for IPMs to obtain power loss and temperature information. To provide data for simulations, switching, conduction, and thermal impedance data modeling is required.



Switching losses of the IGBT and diode in an IPM



Conduction losses of the IGBT and diode in an IPM

Figure 4 Electrical characteristics for modeling IPM simulation.

Figure 4 shows the electrical characteristics of IPMs such as turn-on loss (E_{ON}), turn-off loss (E_{OFF}), diode reverse recovery loss (E_{rr}), and conduction loss. These parameters are required for simulation.

600 V products use 300 V switching characteristics and 1200 V products use 600 V switching characteristics at room temperature (25°C) as well as high temperature (150°C). In the case of conduction losses also, conductive characteristics of the IGBT and diode are required at both room temperature (25°C) and high temperature (150°C).

Figure 5 shows the thermal impedance structure of an IPM. TJ_Q and TJ_D denote the temperature of the IGBT and diode, respectively. The thermal impedances are obtained from multichip heating. Other foster models are thermal coupling coefficients. TJ_D2Q denotes the thermal impedance on the heat generated in the IGBT by the diode and TJ_Q2D denotes the thermal impedance on the heat generated in the diode by the IGBT. After the thermal coupling coefficients are added to TJ_Q and TJ_D, the resultant values show as TJ_IGBT and TJ_Diode in IPOSIM.

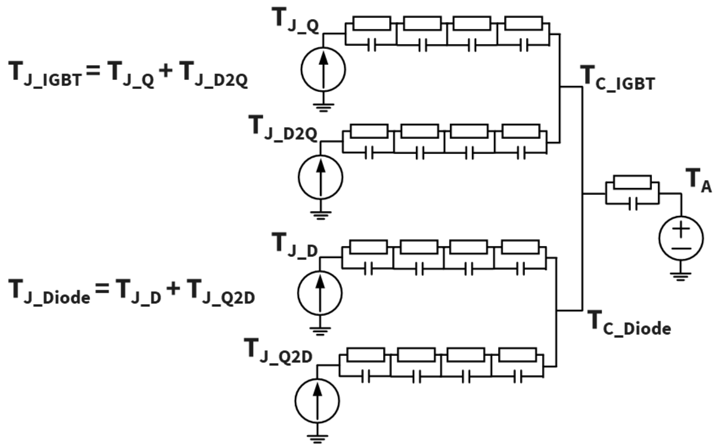


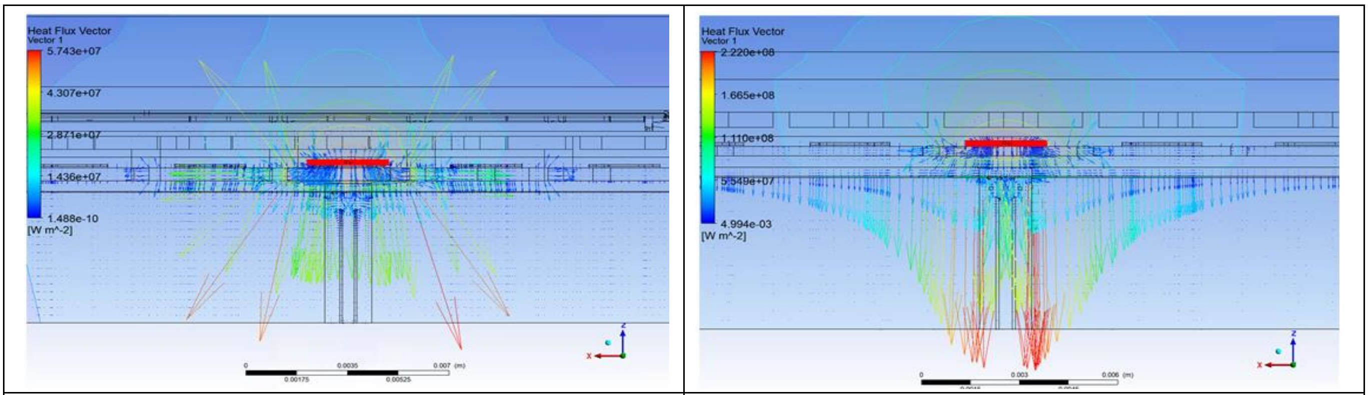
Figure 5 **Thermal impedance structure in simulation.**

3 Difference between a fully molded and a DCB package

Figure 6 shows the heat flux in a fully molded and a DCB IPM package under fixed temperature conditions.

Figure 6 (a) shows the fully molded IPM package. Since the fully molded IPM has low thermal conductivity, the fraction of heat flux of the chips is delivered to the printed circuit board (PCB) and other areas. This means more thermal interaction between adjacent chips in the package when multiple power chips operate together.

Figure 6 (b) shows the heat flux of a DCB IPM package. It has a good heat dissipation path from the power chips to the case. Therefore, most of the heat in the junction of the power chips goes through the copper layer and the thermal interaction between adjacent chips is less than in the fully molded IPM package.



(a) The heat flux in a fully molded IPM package | (b) The heat flux in a DCB IPM package

Figure 6 **Heat flux in IPMs based on the package type.**

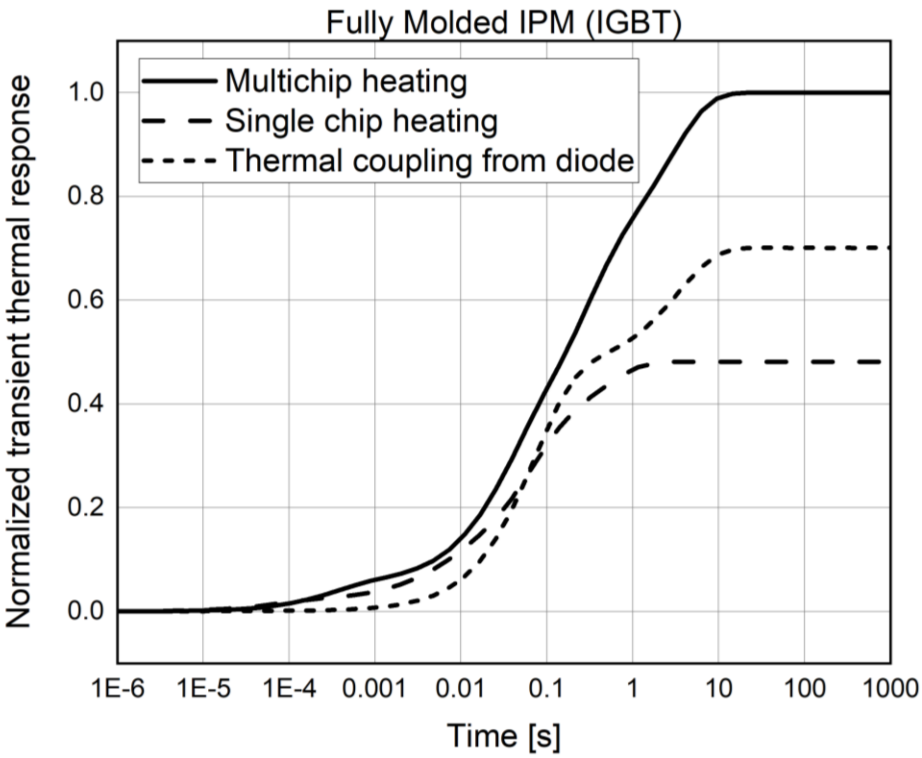
Thermal impedance curves that show the effects of thermal interference and multichip heating are illustrated in Figure 7.

In inverter applications, most of the power loss occurs in the IGBTs and their temperature is higher than that of diodes, so only the IGBT is covered in Figure 7. Figure 7 (a) and (b) show the thermal impedance curves of the fully molded IPM and DCB IPM. the solid line represents multichip heating, the dash line represents singlechip heating, and the short dash line represents the thermal coupling from diode.

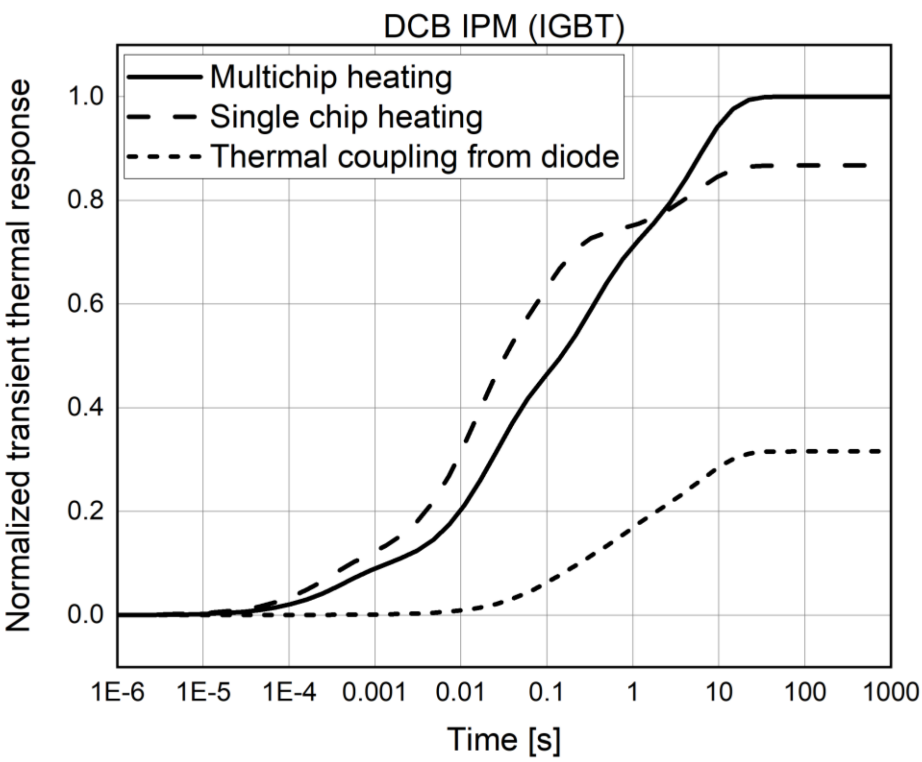
Based on the per unit basis for multichip heating, the fully molded IPM has around 70% thermal coupling and the DCB IPM has around 30% thermal coupling. This means that the fully molded IPM is more affected by thermal coupling than the DCB IPM. Even considering that the power losses of diode are not high in an inverter system, estimating the junction temperature can result in significant errors in the fully molded IPM. The thermal response curve for single-chip heating in a fully molded IPM is about 50% compared to multichip heating. The temperature rise due to multichip heating is significantly higher than in the DCB IPM which has only a 15% gap. This is because the EMC and the copper substrate transfer heat differently.

Based on these results, it is clear that the fully molded IPMs are more affected by thermal coupling. The thermal impedance of multichip heating is much higher than that of a single chip. The effects of multichip heating and thermal coupling are small on the DCB IPMs but affective. Therefore, while operating the IPMs the thermal impedance of multiple chips and the thermal coupling coefficient should be applied to reach closer to the actual junction temperature.

Difference between a fully molded and a DCB package



(a) Transient thermal response to Fully molded IPM



(b) Transient thermal response to DCB IPM

Figure 7 The transient thermal response curves of IPMs.

4 Comparison between simulation and experiment results

Figure 8 shows the setup for measuring temperature. The case (T_C) and ambient (T_A) temperature were measured by a temperature recorder using a thermocouple. The junction temperature of the product (decapsulated) was measured using an infrared camera. The maximum junction temperature could not be measured due to the limited frame of the camera. Therefore, simulation modeling was verified using the average junction temperature of the experiment.

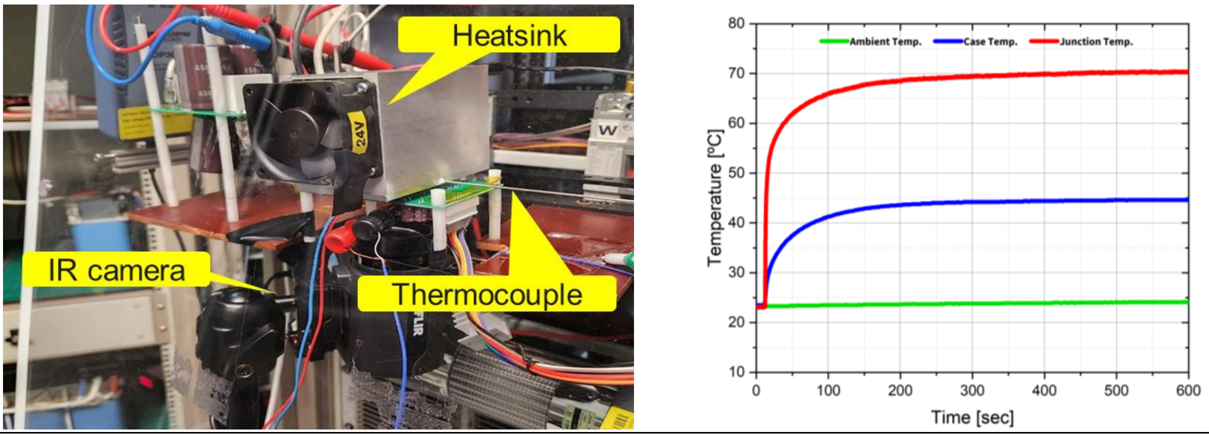


Figure 8 The setup for experiment and measurement result.

Table 1 shows a comparison between the temperature data obtained from simulation and experiment. Multichip heating and thermal coupling were adapted to simulation modeling. The temperature results are based on the operating conditions that are listed as footnotes. As it is difficult to define the thermal impedance of the heat sink for each operating condition, the case temperature from the experiment was used for simulation. The simulations were run under a fixed heat sink temperature.
All simulation results were slightly different from the experiment results because simulation modeling cannot be considered for the same environment as the experiments. There can be several reasons for these differences in the results:

1. The first reason could be the transfer of the fraction of heat flux in other directions rather than the T_c point. A simulation that only considers $R_{th(J-C)}$ and power losses cannot consider the heat flow in the other direction.
2. The second reason could be that as power increases, the thermal coupling becomes higher. Simulation only considers thermal coupling between the IGBT and the diode. However, at higher power, thermal coupling can occur not only between the IGBT and the diode but also between other chips, leading to different simulation results.
3. The third reason could be the experiment setup. As the thickness of the TIM depends on user requirements, measurement point error, etc. can show up as differences.

The third reason could be the experiment setup. When an IPM is attached to the heat sink, the thermal conductivity (TC) can be changed based on the mounting torque force and the thickness of the thermal interface material (TIM). Also, there can be differences between the TC point provided in datasheet and the measurement location, which can lead to differences with the simulation results. Even though the simulation results do not exactly match compared to the experiment, this simulation is sufficient to estimate the actual junction temperature without measurement.

Table 1 Temperature comparison between simulation and experiment results

Package types	Products		Temperature data		
			T_C [°C]	$T_{J(AVG.)}$ [°C]	$T_{J(MAX.)}$ [°C]
Fully molded IPM	IM06B15AC1	Experiment[1]	44.6	70.4	
		Simulation[1]		68.6	72.3
		Experiment[2]	52.9	62.6	
		Simulation[2]		60.8	61.9
	IKCM15L60GA	Experiment[1]	51.8	93.9	
		Simulation[1]		91.5	97.4
		Experiment[2]	68.1	84.8	
		Simulation[2]		80.1	81.7
Copper substrate IPM	IM535-U6D	Experiment[3]	66.8	103.1	
		Simulation[3]		102.1	109.7
		Experiment[4]	81.1	133.3	
		Simulation[4]		127.8	138.3
	IM12B15CC1	Experiment[5]	46.0	60.2	
		Simulation[5]		61.2	64.1
		Experiment[6]	62.5	93.4	
		Simulation[6]		89.5	94.7

1) Operation conditions: V_{DC} = 340 V, F_{SW} = 6 kHz, F_O = 60 Hz, V_{DD} = 15 V, MI = 0.82, PF = 0.9, I_O = 7.07 Arms, SVPWM, forced cooling.
2) Operation conditions: V_{DC} = 310 V, F_{SW} = 15 kHz, F_O = 60 Hz, V_{DD} = 15 V, MI = 0.91, PF = 0.99, I_O = 2 Arms, SVPWM, convection cooling.
3) Operation conditions: V_{DC} = 380 V, F_{SW} = 5 kHz, F_O = 60 Hz, V_{DD} = 15 V, MI = 0.5, PF = 0.78, I_O = 21.2 Arms, SVPWM, forced cooling.
4) Operation conditions: V_{DC} = 380 V, F_{SW} = 5 kHz, F_O = 60 Hz, V_{DD} = 15 V, MI = 0.59, PF = 0.78, I_O = 24.75 Arms, SVPWM, forced cooling.
5) Operation conditions: V_{DC} = 600 V, F_{SW} = 6 kHz, F_O = 60 Hz, V_{DD} = 15 V, MI = 0.46, PF = 0.90, I_O = 7.07 Arms, SVPWM, forced cooling.
6) Operation conditions: V_{DC} = 600 V, F_{SW} = 15 kHz, F_O = 60 Hz, V_{DD} = 15 V, MI = 0.46, PF = 0.90, I_O = 7.07 Arms, SVPWM, forced cooling.

5 Conclusion

This document described the IPM simulation modeling in IPOSIM. Unlike other power modules, IPMs generally have small packages composed of EMC and the power chips are placed close to each other. Therefore, it is necessary to consider not only the temperature rise caused by a single chip, but also the temperature rise caused by the operation of multiple power chips. The fully molded IPM has low thermal conductivity because the fraction of heat flux transfers to other sides. This also leads to challenges in estimating the junction temperature. To overcome these challenges, the thermal impedance value for multichip heating and thermal coupling coefficients should be applied to simulation modeling. Direct copper bonded IPMs with relatively high thermal conductivity should also be applied to improve accuracy.

Table 1 shows temperature data from simulations that use thermal impedance values for multichip self-heating and thermal coupling coefficient, and experiments. The fact that there are only slight differences between the results of simulation and experiments verifies the accuracy of the IPM simulation modeling. IPM modeling in IPOSIM provides a good and quick estimate of how hardware will perform, which is helpful in selecting the appropriate IPM.

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Revision history

Version number	Revision date	Revision description
1.00	2025-12-01	Initial release

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