Understanding and interpreting the CoolSiC™ MOSFET 1200 V datasheet

About this document

Scope and purpose

The purpose of this paper is to help users better understand the datasheet parameters of the CoolSiC™ 1200 V MOSFET to understand the potential and limitations of the device. This document also helps users apply datasheet parameters correctly to the system design.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

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1 Introduction

Compared to silicon (Si) devices, silicon carbide (SiC) MOSFETs have superior properties at high voltage and high power in almost all aspects due to their material advantages, such as:

- Three times larger band gap
- Three times higher thermal conductivity
- Ten times larger critical electric field
- Two times higher saturation velocity

SiC MOSFETs can thus significantly improve the performance of a system. A deeper understanding and right usage of SiC MOSFETs can help enhance device performance and maximize system value propositions.

This document provides detailed information about the parameters and conditions of Infineon CoolSiC™ MOSFET 1200 V given in its datasheet. The aim is to help users maximize performance in actual systems.

Infineon CoolSiC™ MOSFET 1200 V discretes were especially developed for applications such as photovoltaic, energy storage system (ESS), electric vehicle (EV) charging, uninterruptible power supply (UPS), industrial drives, and others. The CoolSiC™ MOSFET 1200 V discretes enable accelerated system design for more cost-optimized, efficient, compact, and reliable solutions.

Note: The terminologies and conditions given in the datasheet follow the IEC 60747-8 and IPC 9592B standards. However, there is one exception that the switching time is measured using inductive load in parallel with a clamp diode which is the same as for the switching energy loss test.

2 General information section of the CoolSiC™ MOSFET 1200 V datasheet

The first page (cover page) of Infineon's datasheet provides brief information about a product. It includes:

① The sales code

② Technology name and description

③ Features of the product

④ Potential applications (or target applications)

⑤ Product validation

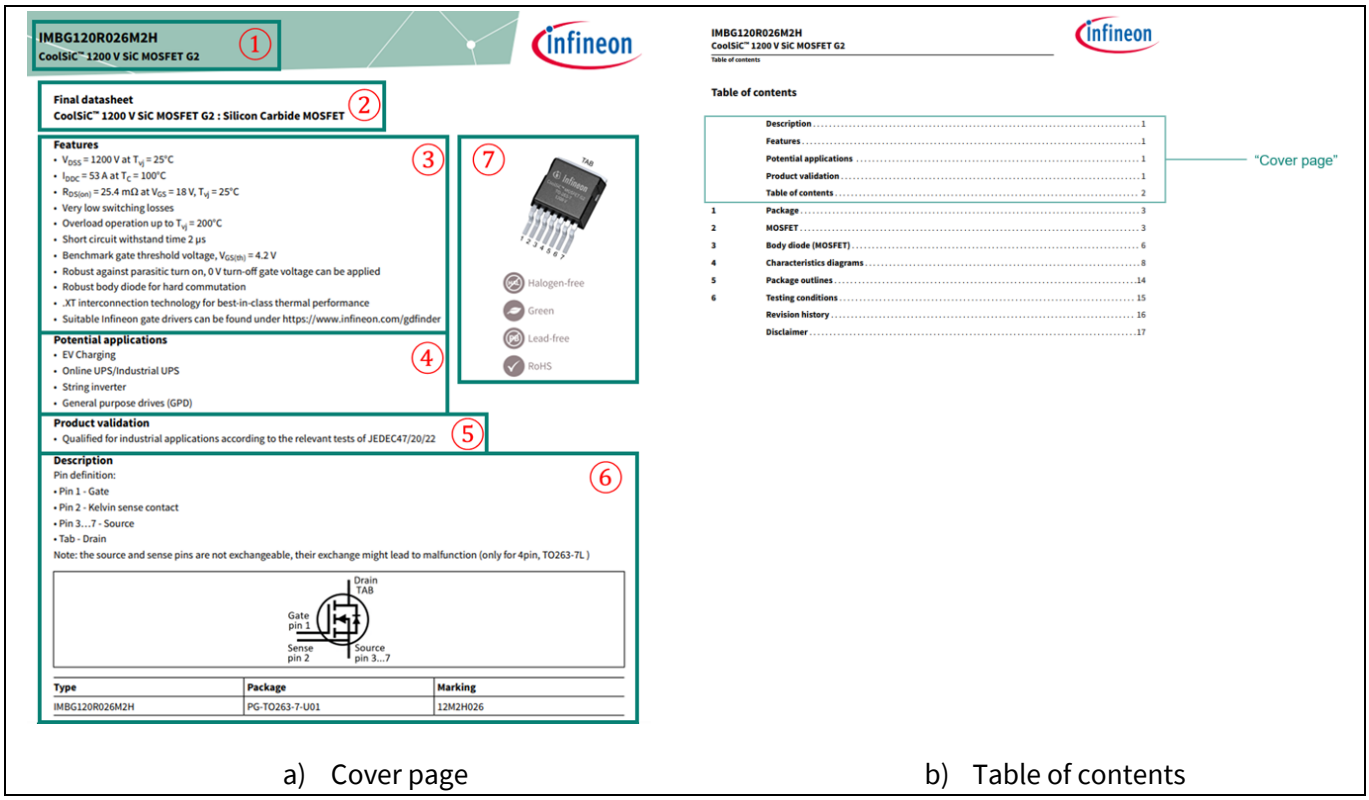
⑥ Symbol, pin description, and marking information

⑦ Image of the package

The table of contents (TOC) lists the main items in the datasheet in order of appearance in the document. The first five items listed in the TOC are on the cover page. After this, the following topic headings are listed in a sequence:

1. Package
2. MOSFET
3. Body diode
4. Characteristics diagrams
5. Package outlines
6. Testing conditions

When the datasheet is revised, the revision history gets updated. The disclaimer appears on the last page.



a) Cover page b) Table of contents

Figure 1 Cover page and table of contents

3 Package information

Chapter 1 of the datasheet provides package relevant information as shown in Figure 2. The first three parameters in the list are storage and assembly-related information, and the last two items in the table are values of thermal resistances – junction-ambient $R_{th(j-a)}$ and junction-case $R_{th(j-c)}$.

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	wave soldering only allowed at leads 1.6 mm (0.063 in.) from case for 10 s			260	°C
Mounting torque	M	M3 screw, Maximum of mounting processes: 3			0.6	Nm
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			0.4	0.52	K/W

Figure 2 Package characteristic values

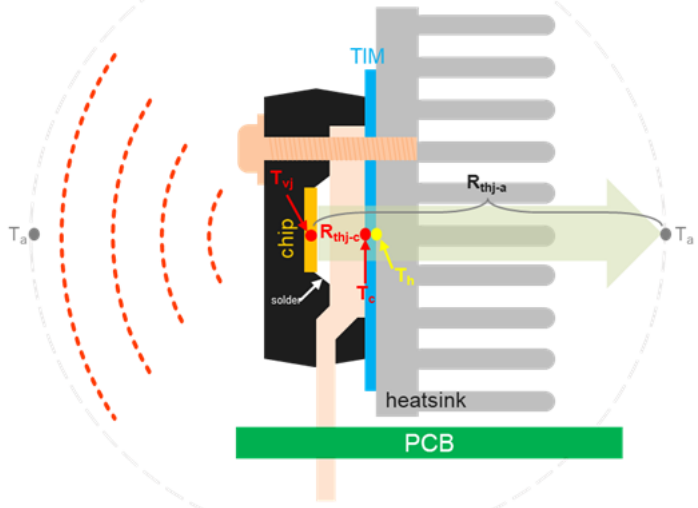


Figure 3 Thermal path of the power semiconductor and thermal resistances, R_{th} definition

The definition of thermal resistances, $R_{th(j-a)}$ and $R_{th(j-c)}$, of power semiconductor devices is often not properly understood. To understand it correctly, look at a practical use case shown in Figure 3. Here a through-hole device is mounted on a heat sink via a thermal interface material (TIM).

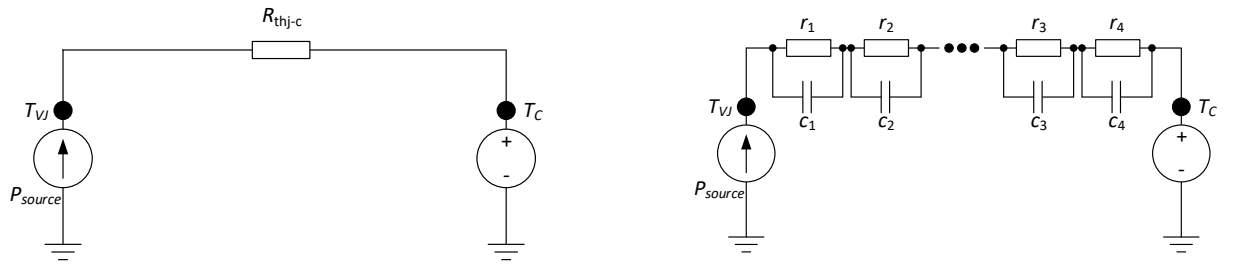
When power is given to the chip inside, heat is generated and the junction temperature increases as a result. This heat dissipates mainly through the direction shown by the green arrow towards a point T_a. A very small part of the heat also radiates from the package's surface and dissipates. Here, T_a refers to the temperature at a fixed imaginary point that is not affected by the device. In the Infineon datasheet, the junction temperature is defined as T_{vj} (virtual junction temperature) because it is not measured. However, it is possible to estimate it through temperature-sensitive electrical parameters (TSEPs), such as $R_{DS(on)}$ and V_F, whose values vary depending on the junction temperature and can be measured almost precisely.

Meanwhile, the surface temperature of the lead frame just under the chip is defined as the case temperature T_c. The thermal resistance between the junction to case is defined as $R_{th(j-c)}$, and between the junction to ambient as $R_{th(j-a)}$.

T_{vj} of a device at steady state can be calculated by an equation similar to Ohm's law if we know how power is consumed by the device (1). For the steady state condition, the thermal chain can be interpreted as the electrical circuit shown in Figure 4. Here the power dissipation $P_{dis.}$ is replaced by the current source I, temperature is replaced by a voltage drop V, and the thermal resistance is replaced by electric resistance R.

$$P_{dis.} = \frac{T_{vj} - T_c}{R_{th(j-c)}} \quad (1)$$

$$T_{vj} = P_{dis.} \times R_{th(j-c)} + T_c \quad (2)$$



a) Steady-state model b) Dynamic-state model (Foster model)

Figure 4 Thermal netwok models

However, at dynamic state conditions, the shorter the time for which power is applied to the chip, the smaller the rise in the junction temperature. Therefore, a more accurate model should be considered. For example, the Foster model shown in Figure 4 (b), which includes multiple thermal capacitances in parallel with multiple thermal resistances in series.

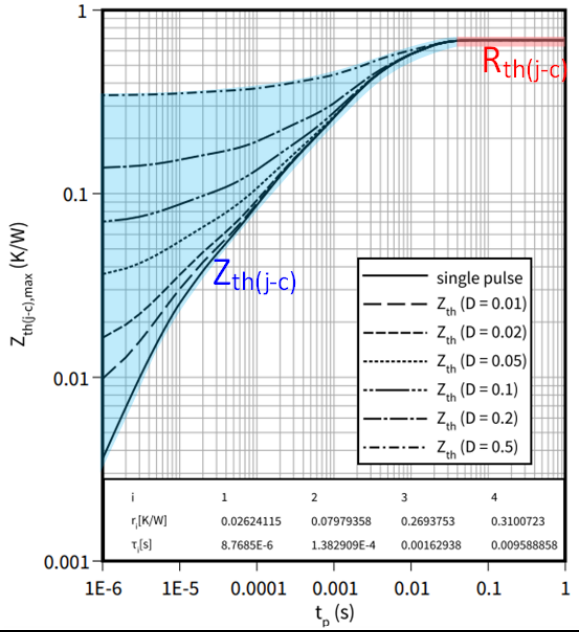


Figure 5 Example of transient thermal impedance

Figure 5 shows the Z_{th} curve derived using the Foster model. Here the saturated value shown on the right is the thermal resistance $R_{th(j-c)}$ for steady state while the variable pulse widths on the left are thermal impedances $Z_{th(j-c)}$.

From the second generation CoolSiC™ MOSFET 1200 V, G2 onwards Infineon provides two maximum virtual junction temperatures, $T_{vj.max}$, and $T_{vj.max\ (over)}$, as shown in Figure 6. Here, $T_{vj.max}$ = 175°C represents the maximum junction temperature for the entire product lifetime under normal operating conditions, and $T_{vj.max\ (over)}$ 200°C is the maximum junction temperature guaranteed under overload conditions for a total cumulative time of 100 hours over the entire life of the device. This limitation is due to the packaging constraints, not the SiC chip itself.

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Virtual junction temperature	T_{vj}		-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[2)]			200	°C

Figure 6 Virtual junction temperatures

4 MOSFET

4.1 Maximum rated values

Chapter 4 of the datasheet provides information related to the performance and characteristics of the MOSFET channel. It shows the maximum rated values that enable safe usage of the device. The device must not be used beyond these values except under two exceptional scenarios – a short circuit, and single and repetitive avalanche modes (E_{AS} and E_{AR}) that do not occur during normal operation.

4.1.1 Drain-source voltage, V_{DSS}

V_{DSS} is the maximum allowed drain to source voltage that can be applied. To guarantee the safety of the device, the operating voltage in applications must not exceed this value. Infineon guarantees V_{DSS} for 25°C ≤ T_{vj} ≤ 200 °C in the datasheet because the drain-source breakdown voltage ($V_{(BR)DSS}$) has been 100% tested at 25°C following a test process with sufficient margin. Like other semiconductor materials, SiC also has a positive temperature coefficient on its breakdown voltage, therefore the actual $V_{(BR)DSS}$ inevitably decreases as T_{vj} decreases. However, considering that its temperature coefficient on the breakdown voltage is very low, and sufficient margin is applied on $V_{(BR)DSS}$ during test at 25°C, the CoolSiC™ MOSFET 1200 V G2 maintains the breakdown voltage above the rated V_{DSS} even at -55°C as shown in Figure 7. However, V_{DSS} at T_{vj} ≥ -55°C is not specified in the datasheet because it is not tested in production.

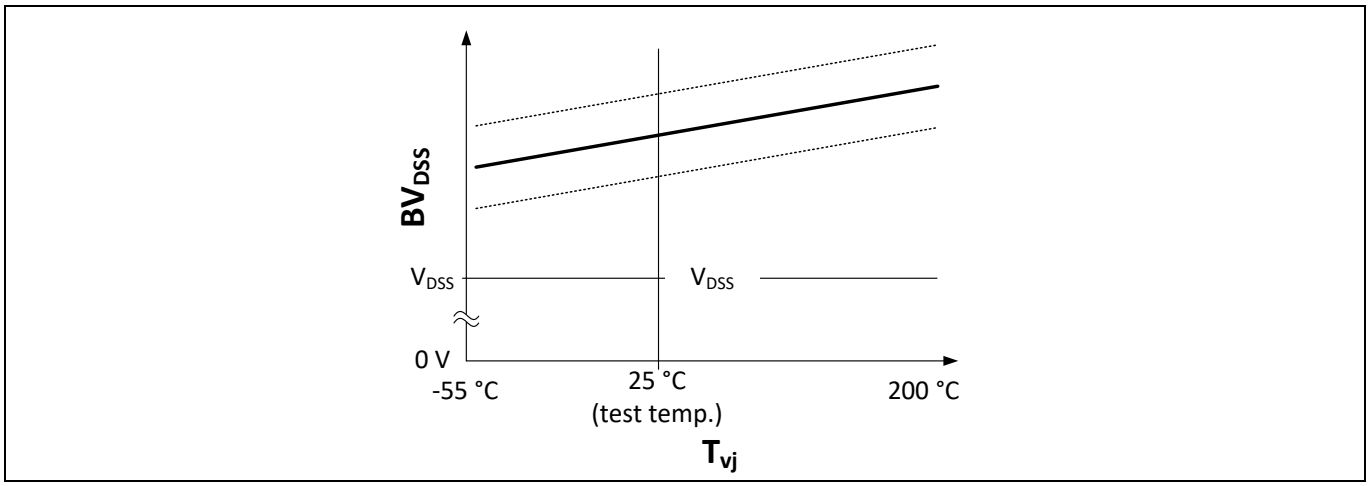


Figure 7 Actual breakdown voltage of the CoolSiC™ MOSFET

4.1.2 Continuous DC drain current, I_{DDC}

I_{DDC} is the maximum DC drain current that a device allows at the case temperature T_c of 25°C and 100°C. As shown in Fig 8, it is limited to the lower values between the calculated maximum power consumption of the device as determined by $R_{DS(on)max}$@ 175°C and $R_{th(j-c)}$, shown in equation (3), or the allowable current density of the bond wires.

$$I_{DDC}@T_c = \sqrt{\frac{T_{vj(\max)} - T_c}{R_{DS(on).max}@175°C \times R_{th(j-c)}}} \quad (3)$$

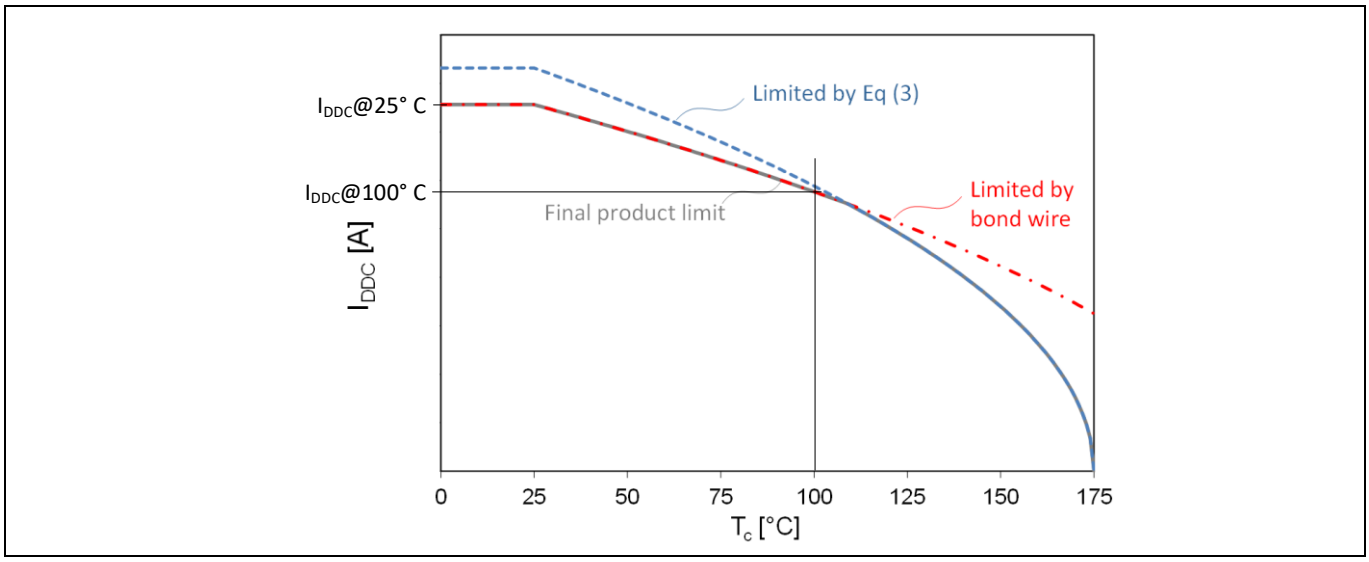


Figure 8 Example of DC drain current, I_{DDC} definition when the value limited by bond wire is less than the limited by chip limit

4.1.3 Peak drain current, I_{DM}

I_{DM} is the value of the allowable peak pulse current guaranteed by the design as long as the junction temperature does not exceed $T_{vj.max}$.

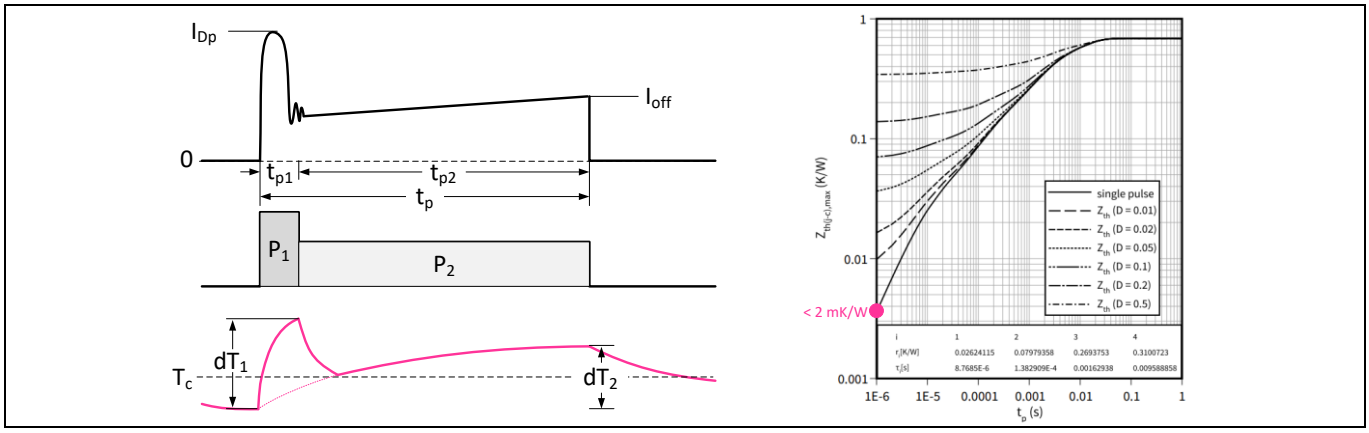


Figure 9 A practical example of I_{DM}

Users can calculate T_{vj} from Equation (2) and define whether the surge current observed in the system can be tolerated. Assuming a switching current that includes a front-stage surge, as shown in Figure 9, two power components can be considered – P_1 caused by the surge and P_2 caused by the normal switching current. In most situations, the duration of the surge is usually very short, less than 1% of the duty cycle (D), and can be considered as a single pulse, but it can also be the whole switching current, I_{off} being the peak switching current. The power dissipation P_1 induced by the surge current can be measured with an oscilloscope (multiplying waveforms of V_{DS} and I_D) and the virtual junction temperature T_{vj} can be estimated. As the junction temperature cannot be measured very accurately, it is recommended that T_{vj} does not exceed 150°C. Assuming that T_c is stabilized at 90°C, the approximate allowable power dissipation of the surge part (D < 1%), shown in Figure 9, can be calculated as 30 kW, even if Z_{thj-c} is considered conservatively.

$$P_1 = \frac{T_{vj} - T_c}{Z_{th(j-c)}} = \frac{(150 - 90)K}{2\ mK/W} = 30\ kW \quad (4)$$

However, it is important to note that increasing the time high current flows also increases D and $Z_{thj\text{-}c}$. This results in a significant excess of $T_{vj,max}$ and I_{Dp} might be restricted to below I_{DM}.

4.1.4 Gate-source voltage, V_{GS}

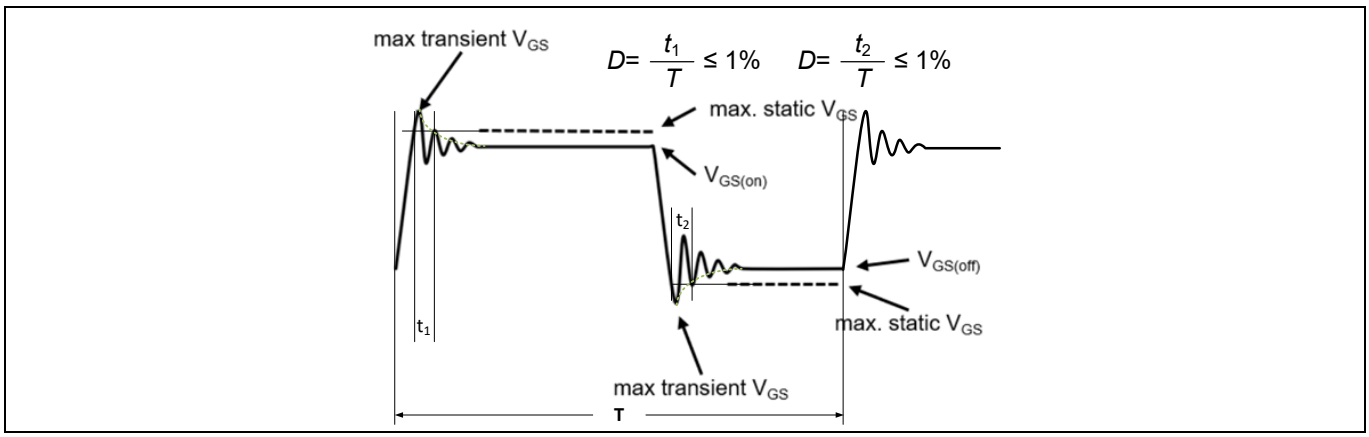


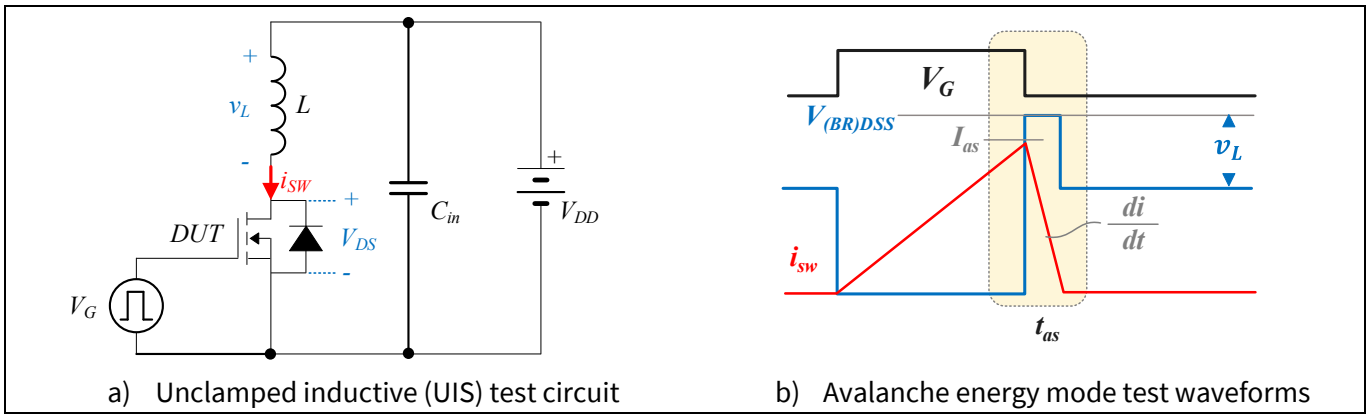
Figure 10 Definition of the gate-source voltage

V_{GS} is the guaranteed range of the gate-source voltages. Definitions of the maximum transient voltage and maximum static voltage are shown in Figure 10. The V_{GS} specification assumes that users apply $V_{GS(on)}$ and $V_{GS(off)}$ to drive the device in compliance with the IPC-9592B standard.

The maximum gate-source voltages describe the transient voltage peak during the turn-on and turn-off events. It can reach maximum peak voltages of +23 V and -10 V for a duty cycle of less than 1% as shown in Figure 10. These are the maximum rated values and must not be exceeded.

4.1.5 Avalanche energy, E_{AS}/E_{AR}

E_{AS} and E_{AR} indicate the maximum amount of energy a device can withstand under a single pulse and under repetitive avalanche breakdown mode, respectively.



a) Unclamped inductive (UIS) test circuit b) Avalanche energy mode test waveforms

Figure 11 Avalanche energy test

In practical applications, when the turn-off transient of a SiC MOSFET is very fast, even a small amount of parasitic inductance in the circuit may induce overvoltage transients exceeding the rated voltage V_{DSS}. Avalanche

ruggedness, E_{AS} and E_{AR}, are determined through an unclamped inductive switching (UIS) characterization test in which the inductive load is not clamped by anything, as shown in Figure 11. Therefore, when a single pulse is applied to the device under test (DUT), it is subjected to the avalanche mode at turn-off and the amount of energy induced can be calculated by:

$$E_{as} = \int_0^{t_{as}} V_{DS} i_{sw}(t) dt = \int_0^{t_{as}} V_{DS} \left(I_{as} - \frac{V_L}{L} t \right) dt$$

$$= \frac{L {I_{as}}^2 V_{DS}}{V_L} - \frac{L {I_{as}}^2 V_{DS}}{2 V_L} \quad (5)$$

If $V_L = V_{(BR)DSS} - V_{DD}$, then,

$$E_{as} = \frac{1}{2} L {I_{as}}^2 \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}} \quad (6)$$

Meanwhile, as the V_{DD} value applied to the E_{AS} test, 50 V is significantly lower than the DC-link voltage value in practical applications, it is not reasonable to directly substitute the value of E_{AS} in the datasheet. However, as the voltage can be corrected using Equation (6), it is possible to evaluate if an avalanche mode occurring unexpectedly in the system is acceptable, as shown in Figure 12.

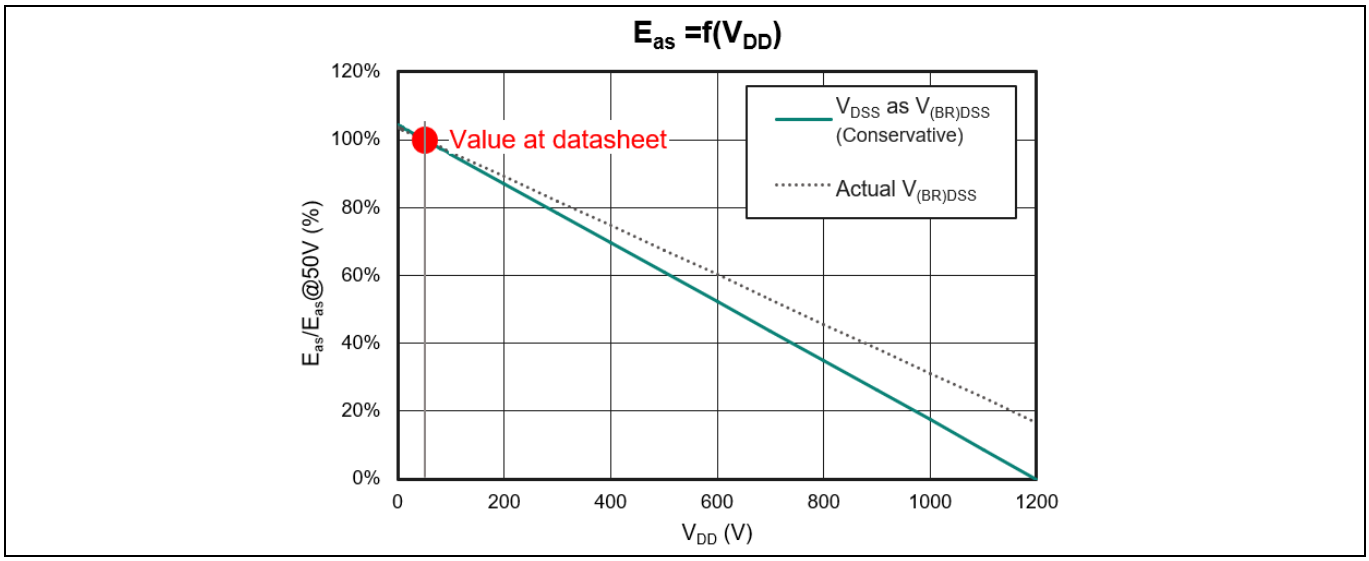


Figure 12 Corrective E_{AS} capability for the DC-link voltage

4.1.6 Short-circuit withstand time, t_{sc}

t_{sc} is the maximum time till which a device is allowed to withstand a short-circuit condition. The CoolSiC™ MOSFET 1200 V G1 has t_{sc} of 3 µs and G2 has a t_{sc} of 2 µs.

4.1.7 Power dissipation, P_{tot}

P_{tot} is the maximum power allowed for devices if T_{vj} does not exceed T_{vjmax} at case temperature (T_c) values of 25°C and 100°C. P_{tot} is measured with $R_{th(j-c)}$, as shown in Figure 2, through the following experiment: The case

temperature T_c of the DUT is fixed by mounting it on an infinite heat sink at 25°C or 100°C. Power dissipation is then triggered by injecting a DC current. P_{tot} can be defined as the power at which the measured T_{vj} reaches the $T_{vj.max}$. Here, T_{vj} can be measured by a temperature coefficient (k-factor: $R_{DS(on)}$ or V_F).

4.2 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

Figure 13 Recommended values

Figure 13 shows the recommended values for $V_{GS(on)}$ and $V_{GS(off)}$. $V_{GS.static}$ and $V_{GS.dynamic}$ have already been described in Section 4.1.4. However, as the voltage applied to the device increases, the stress level of the device gets worse and the failure in time (FIT) rate also increases exponentially. Thus, it is recommended that users use V_{GS} with an appropriate safety margin just like V_{DSS}. IPC-9592B standard suggests that V_{GS} should not exceed 80% of its datasheet value. The CoolSiC™ MOSFET datasheet recommends a $V_{GS(on)}$ of 15 V to 18 V, and a $V_{GS(off)}$ of -5 V to 0 V.

4.3 Characteristic values

This section describes the characteristic values that are not absolute but indicate the performance of the device. The typical values are defined by a characterization test and the minimum and the maximum values are guaranteed by 100% testing at production.

4.3.1 Drain-source on-state resistance, $R_{DS(on)}$

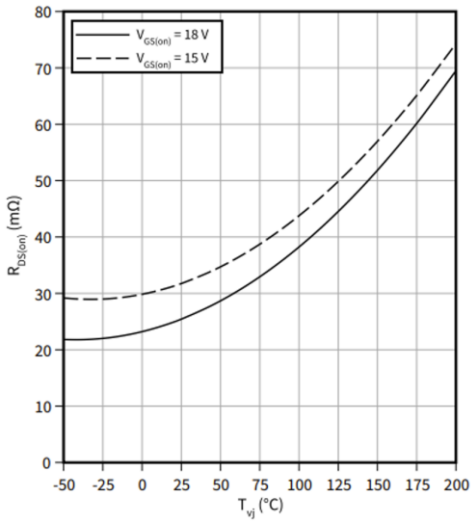


Figure 14 Typical on-state resistance as a function of junction temperature

$R_{DS(on)}$ is the resistance between the drain and source when a MOSFET conducts completely. In most applications, the driving voltage of the SiC MOSFET is usually 18 V, so $R_{DS(on)}$ values at nominal current $I_{D.nom}$, and T_{vj} = 25°C, 150°C, and 175°C are stated respectively in the datasheet. Since the actual junction temperature in practical systems becomes high during operation, from the G2 data sheet, the maximum $R_{DS(on)}$ value at 150°C is provided in the table. For a fair comparison with other products with V_{GS} = 15 V, the $R_{DS(on)}$ at 25°C for V_{GS} = 15 V is also given.

Like silicon devices, the SiC MOSFETs also have a positive temperature coefficient for $R_{DS(on)}$, as shown in Figure 14.

4.3.2 Gate-source threshold voltage, $V_{GS(th)}$

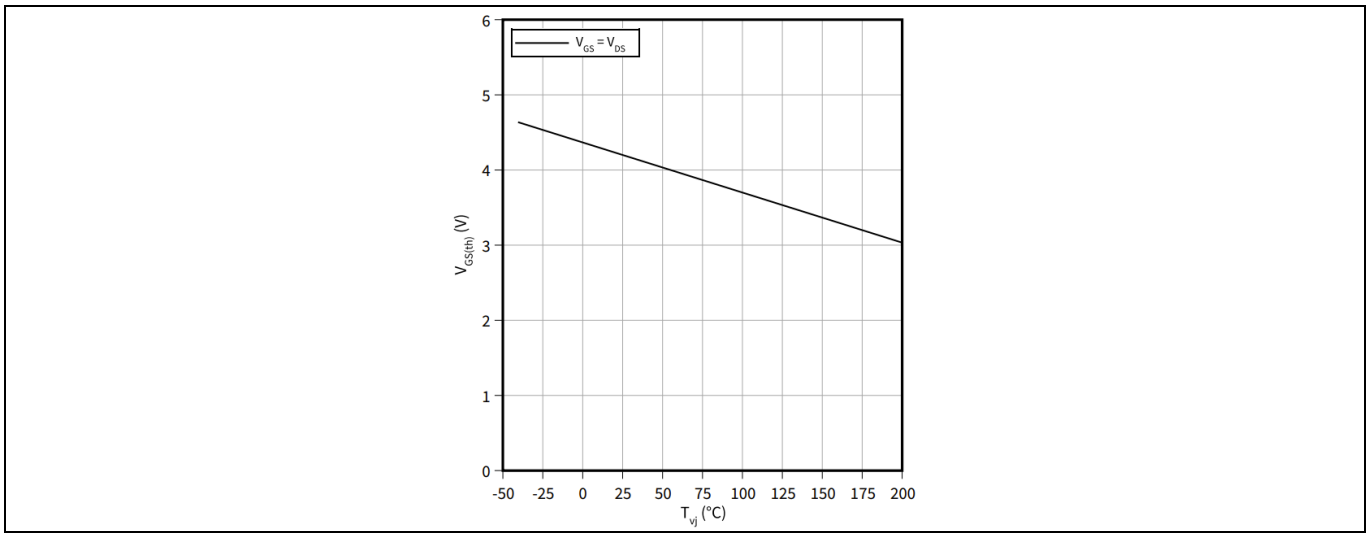


Figure 15 Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)}$ is the gate-source voltage when a drain-source current with a specific current density begins to flow in the MOSFET channel and has a negative temperature dependence, as shown in Figure 15. $V_{GS(th)}$ is an important parameter with respect to parasitic turn-on (PTO), along with the C_{GS}/C_{GD} ratio. Through its high $V_{GS(th)}$ and high C_{GS}/C_{GD} ratio, Infineon's CoolSiC™ MOSFET 1200 V G1 and G2 enable unipolar gate driving, i.e., 0/+18 V, in practical applications.

4.3.3 Zero gate-voltage drain current, I_{DSS}

I_{DSS} is the drain current that flows when the gate-source voltage (V_{GS}) is zero, but it can be simply considered as a drain-source leakage current.

4.3.4 Gate-leakage current, I_{GSS}

I_{GSS} is the gate-leakage current when the maximum (+23 V) and the minimum (-10 V) gate voltages are applied.

4.3.5 Forward transconductance, g_{fs}

g_{fs} is the ratio between the change in output current and the corresponding change in the input voltage of a MOSFET under the given conditions. As shown in Figure 16, the graph of g_{fs} corresponds to the output characteristics.

Forward transconductance is often considered to judge the thermal instability that occurs when V_{GS} is below the crossover point that the channel current I_D starts having a negative temperature coefficient. As shown in Figure 16, when the MOSFET is driven in the area below the crossover point, the channel current I_D increases as the junction temperature increases. This can be a critical problem during a parallel operation. In other words, the higher the V_{GS} voltage, the more advantageous it is in terms of the thermal stability of the MOSFET. For example, V_{GS} = 18 V is more advantageous in parallel operation than V_{GS} = 15 V.

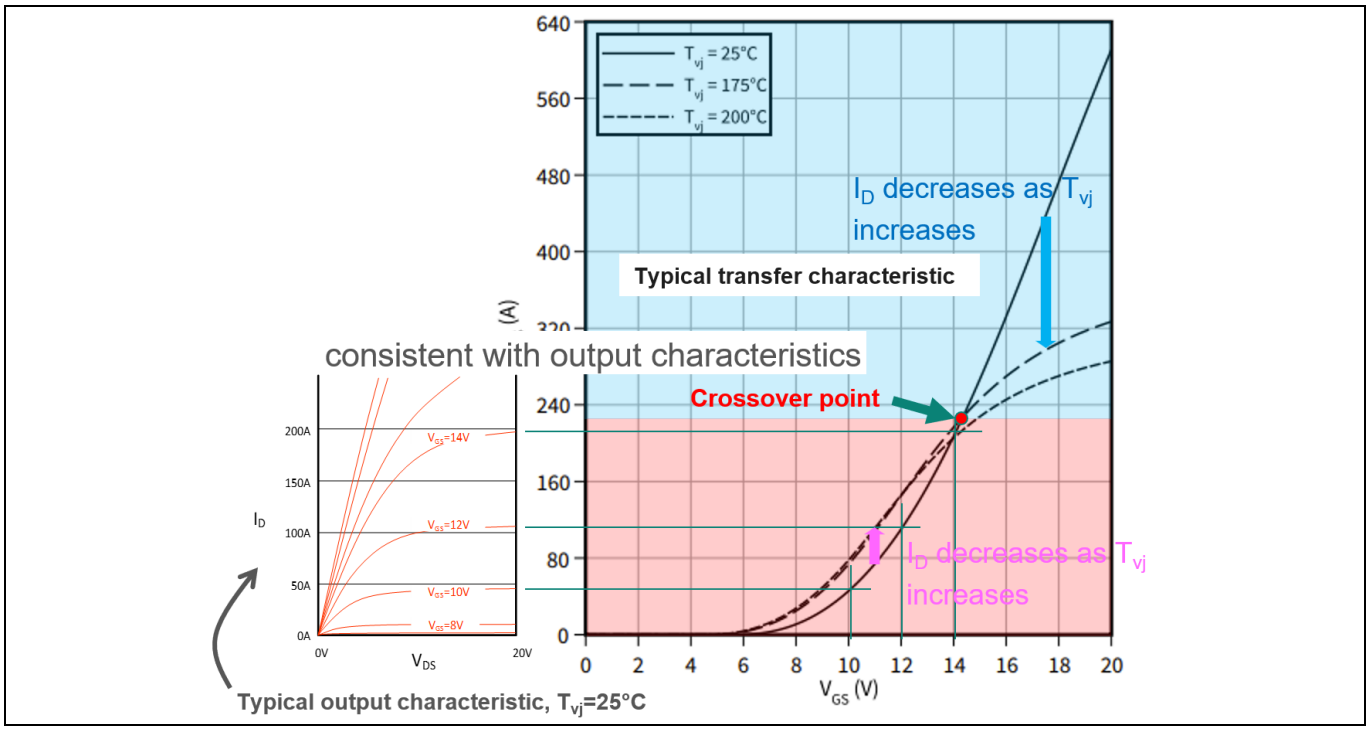


Figure 16 Matching typical transfer characteristics and typical output characteristics at T_{vj} = 25°C

4.3.6 Internal gate resistance, $R_{G,int}$

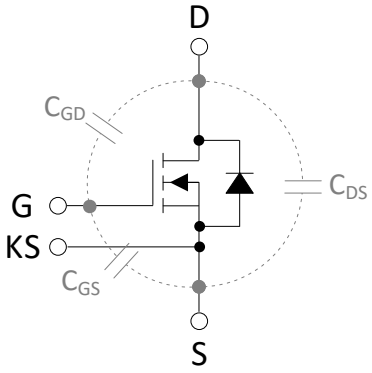
$R_{G,int}$ is the built-in gate resistance of the device which can consist of a dedicated resistor, $R_{G,Poly}$, which is adjustable, and the distributed resistor, $R_{G,Dist}$, which is not adjustable. Adding $R_{G,Poly}$ is especially important for paralleling chips in SiC power module products., Some discrete CoolSiC™ SiC MOSFET 1200V G1, and G2 have only $R_{G,Dist}$ for the fast switching performance, i.e., $R_{g,int}$ is the minimum.

4.3.7 Capacitances

The capacitance of a SiC MOSFET is defined in the same way as that of a conventional Si MOSFET and IGBT.

- Input capacitance, $C_{iss} = C_{GS} + C_{GD}$
- Reverse transfer capacitance, $C_{rss} = C_{GD}$
- Output capacitance, $C_{oss} = C_{DS} + C_{DG}$

As shown in Figure 17, C_{iss} has a relatively constant value with respect to the drain-source voltage, while C_{rss} and C_{oss} vary greatly in value depending on the drain-source voltage.



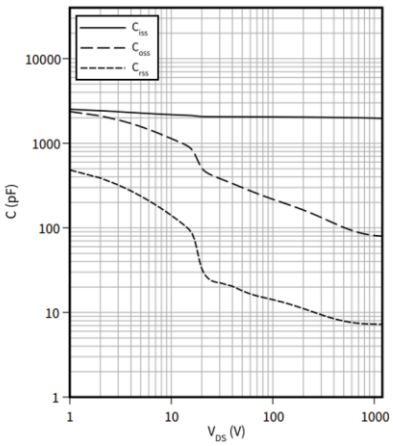


Figure 17 Intrinsic capacitances of a SiC MOSFET

4.3.8 Parameters related to output capacitance

4.3.8.1 C_{oss} stored energy, E_{oss}

E_{oss} is the equivalent energy stored in C_{oss} at a certain value of the drain-source voltage V_{DS}.

4.3.8.2 Output charge, Q_{oss}

Q_{oss} is the charge stored in C_{oss} at a certain value of the drain-source voltage V_{DS}.

Note: *C_{oss} is a factor that depends on the V_{DD} value with junction capacitance. Therefore, unlike typical capacitors, simple equations are not valid.*

$$E_{oss} \neq \frac{1}{2} C_{oss} V_{DS} \tag{7}$$

$$Q_{oss} \neq C_{oss} V_{DS} \tag{8}$$

E_{oss} and Q_{oss} must be calculated by integrating C_{oss} with respect to V_{DS} as follows:

$$E_{oss}@V_{DS} = \int_0^{V_{DS}} vC(v)\,dv \tag{9}$$

$$Q_{oss}@V_{DS} = \int_0^{V_{DS}} C(v)\,dv \tag{10}$$

There are two effective output capacitances, the energy related $C_{o(er)}$ and the time related $C_{o(tr)}$. Both parameters are equivalent capacitances that can be calculated using:

$$C_{o(er)} = \frac{2 * E_{oss}}{{V_{DS}}^2} \tag{11}$$

$$C_{o(tr)} = \frac{Q_{oss}}{V_{DS}} \tag{12}$$

4.3.8.3 When to consider E_{oss} or $C_{o(er)}$

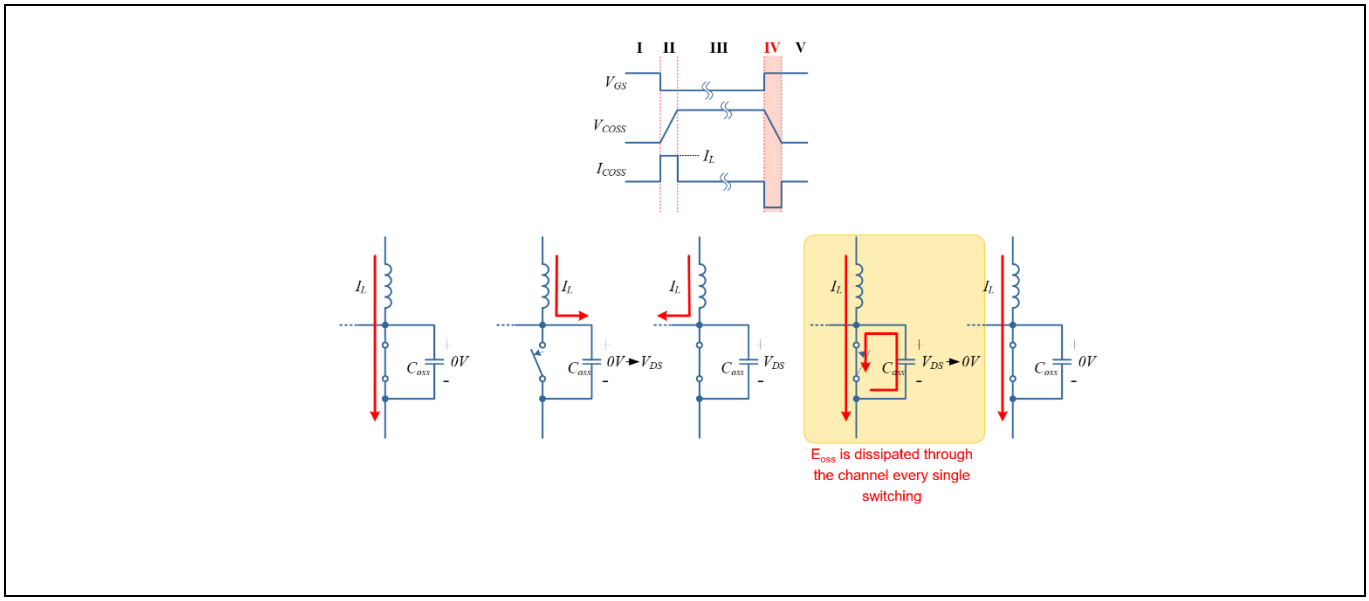


Figure 18 One switching cycle in a hard-switching operation

Although C_{oss} does not affect the switching speed of the device, it results in an intrinsic energy loss, E_{oss}, in hard-switching applications. One switching cycle of the device in a real system is shown in Figure 18. Here in a hard-switching operation, the energy charged to C_{oss} during Mode 3 dissipates through the channel during Mode 4 and the switch turns on again. This causes an extra switching loss during turn-on, i.e., E_{oss}. More importantly, this loss is irrelevant to the switching current and proportional to the switching frequency. In the worst case, this E_{oss} may heat the device significantly even at no load condition and deteriorate the efficiency of the light load system. Therefore, system engineers should pay attention to E_{oss} when selecting a device especially for high switching-frequency operations. $C_{o(er)}$ is only a proportional element of E_{oss}, but for those who prefer it to make direct comparisons with devices from other manufacturers, Infineon has started providing the $C_{o(er)}$ value from the CoolSiC™ MOSFET 1200 V G2 datasheet.

4.3.8.4 When to consider Q_{oss} or $C_{o(tr)}$

In the case of soft-switching applications, the energy charged to C_{oss}, Q_{oss}, during Mode 3 in Figure 18 does not dissipate through the channel. Instead, it is recovered to the DC-link capacitor, or dissipated through the freewheeling path.

In soft-switching applications, C_{oss} is another important aspect for setting the dead time. Figure 19 shows a zoomed-in image of the turn-off switching current in an LLC converter topology. The dead time required for zero voltage switching (ZVS) in the LLC converter must be determined within the time frame of the switching current reaching zero and the resonant current changing its polarity. Under light load conditions, the switching

frequency of the LLC converter becomes very high, and the turn-off current gets low, which highly limits the margin of the dead time. If the switching frequency is designed to be very high despite the large Q_{oss} value of a device, the hard-switching operation during light load is inevitable and the light-load efficiency will deteriorate. Therefore, a device having a small Q_{oss}, such as the CoolSiC™ MOSFET 1200 V, is very useful for high switching-frequency designs. The $C_{o(tr)}$ is proportional to Q_{oss} as given in equation (12), and Infineon has started providing the $C_{o(tr)}$ value from the CoolSiC™ MOSFET 1200 V G2 datasheet.

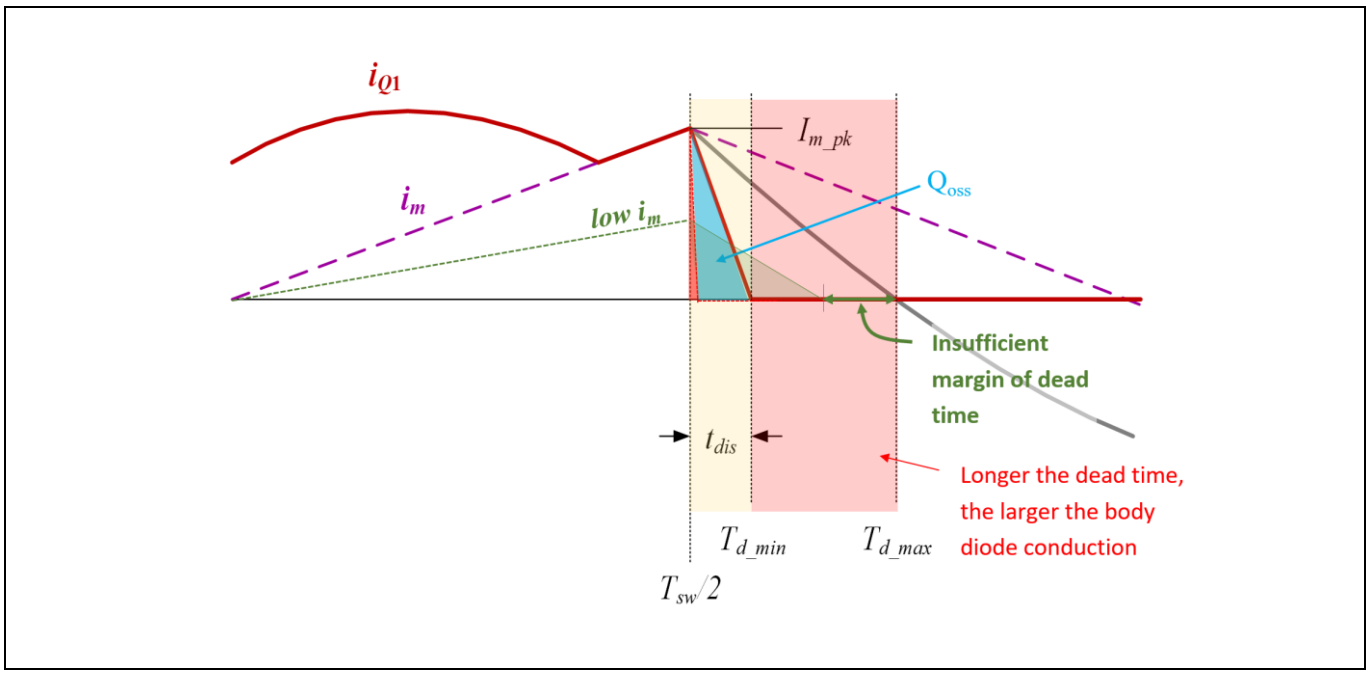


Figure 19 Zoom-in switching current waveform of the LLC converter

On the other hand, the default device simulation models provided on the website are based on double pulse test results under hard switching conditions. Therefore, for more accurate loss simulation in soft switching applications, the E_{oss} should be manually subtracted from the turn off energy loss in the simulation model in case of CoolSiC™ MOSFET 1200 V, G2.

4.3.9 Gate charge

Typical changes in the gate charge required to turn on a SiC MOSFET at any given drain current, gate-source voltage V_{GS} and operating voltage V_{DD}, are:

- Plateau gate charge, $Q_{GS(pl)}$: This is defined as the charge required for V_{GS} to reach the point where V_{DS} starts declining sharply, or the point where the imaginary plateau starts as shown in Figure 20.
- Gate-to-drain charge, Q_{GD}: This is defined as the charge from the beginning to the end of the imaginary plateau shown in Figure 20.
- Total gate charge, Q_G: This is the total charge from $V_{GS} = 0$ to $V_{GS} = V_{GS,static}$ (18 V)

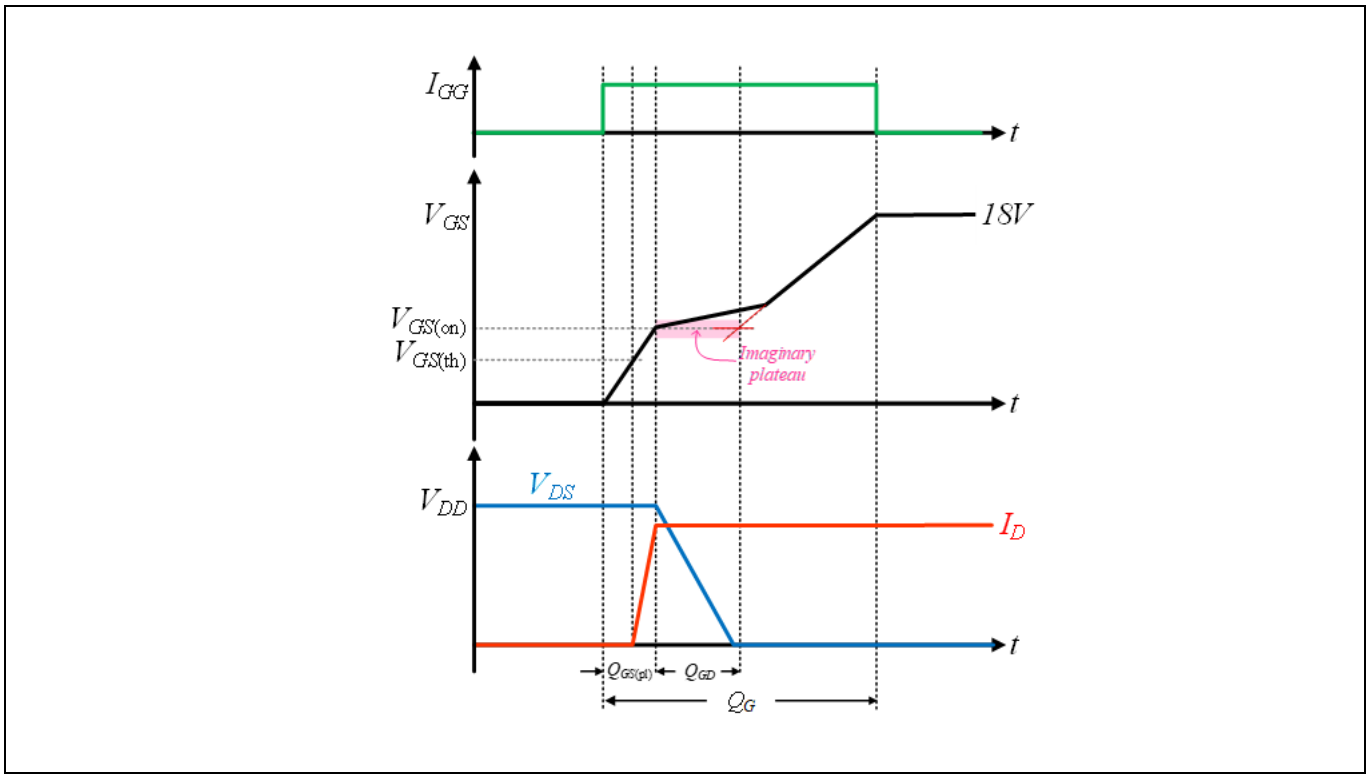


Figure 20 Definition of gate charge

4.3.10 Switching characteristics

The switching characteristics and energy loss data are measured at 25 °C and 175 °C, and the measurement criteria are shown in Figure 21.

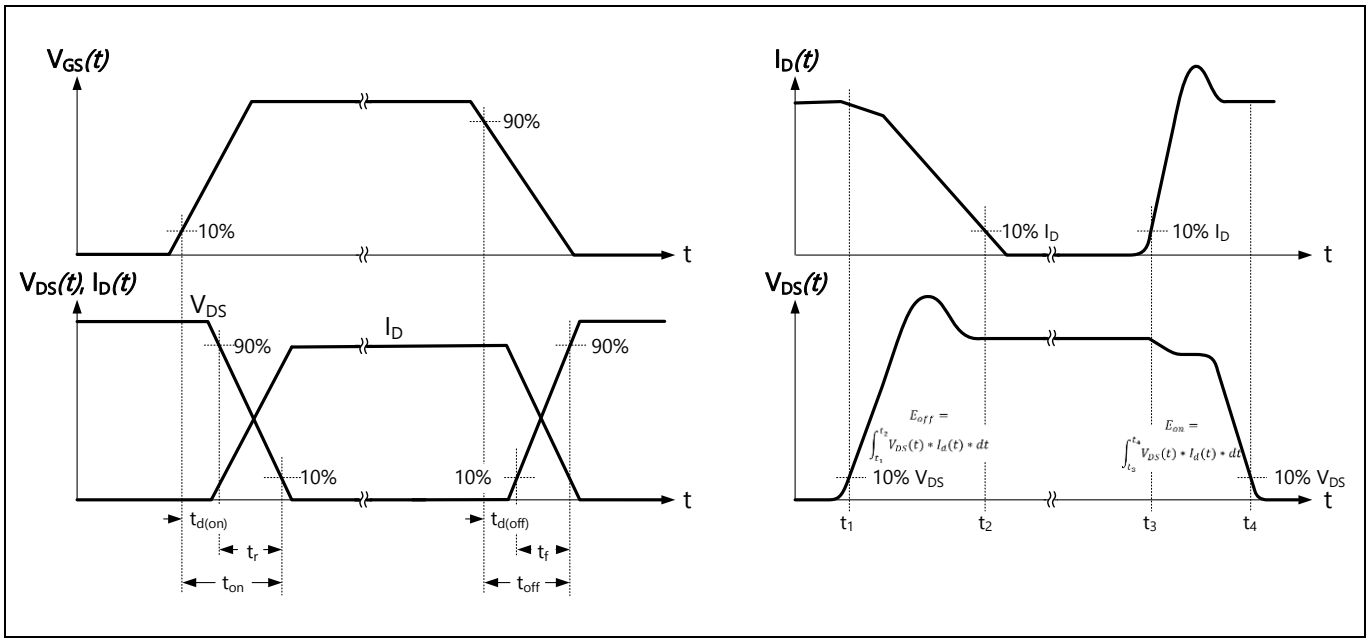


Figure 21 Definition of switching time and switching energy losses

5 Body diode (MOSFET)

5.1 Maximum rated values

Chapter 5 of the datasheet provides information related to the performance and characteristics of the body diode (MOSFET), and lists the maximum rated values that guarantee safe usage of the device. The device must not be used in conditions beyond these values.

5.1.1 Drain-source voltage, V_{DSS}

V_{DSS} of the body diode is the same as that for the MOSFET because the body diode is an intrinsic component of the device.

5.1.2 Continuous reverse DC drain current, I_{SDC}

I_{SDC} is the DC current that the body diode allows at the case temperature, T_c, of 25°C and 100°C. It can be calculated using the following equation. However, it can also be limited by current density of bond wire likewiase I_{DDC} and bipolar degradation in [12].

$$I_{SDC}@T_c = \frac{V_{S\_knee}@T_{vj.max}}{2R_F} + \sqrt{\frac{V_{S\_knee}^2@T_{vj.max}}{4R_F^2@T_{vj.max}} + \frac{T_{vj}-T_c}{R_{thj-c}R_F@T_{vj.max}}} \quad (13)$$

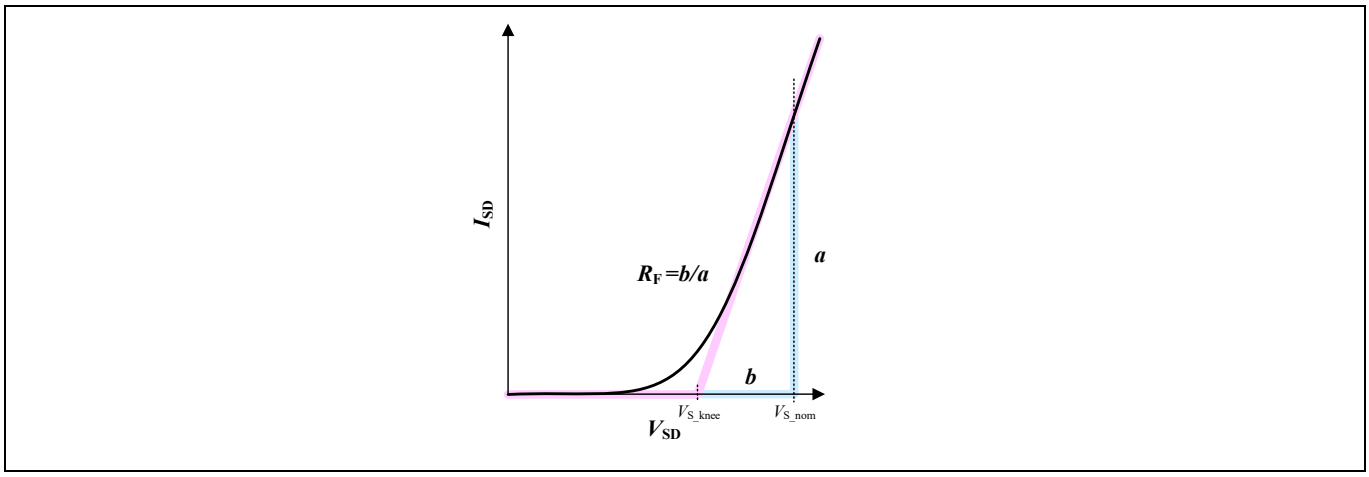


Figure 22 Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

5.1.3 Peak drain current, I_{SM}

I_{SM} is the value of the peak reverse drain current guaranteed by the design as long as the junction temperature does not exceed $T_{vj.max}$.

5.2 Characteristic values

This section describes the characteristic values that are not absolute but indicate the performance of the device. The typical values are defined by a characterization test, and the minimum and maximum values are guaranteed by 100% testing at production.

5.2.1 Drain-source reverse voltage, V_{SD}

V_{SD} is the source-drain voltage drop under the specified conditions at T_{vj} of 25°C, 100°C, and 175°C.

5.2.2 MOSFET forward recovery charge, Q_{fr}

Q_{fr} is the reverse recovery charge of the body diode defined in Figure 23.

$$Q_{fr} = \int_0^{t_{fr}} i_{FR(t)} dt \tag{14}$$

5.2.3 MOSFET peak forward recovery current, I_{frm}

I_{frm} is the permissible peak reverse recovery current of the body diode defined in Figure 23.

5.2.4 MOSFET forward recovery energy, E_{fr}

E_{fr} is the reverse recovery energy of the body diode under the specified conditions at T_{vj} of 25°C and 175°C. For CoolSiC™ MOSFET 1200 V, G2, E_{fr} is included to E_{tot}.

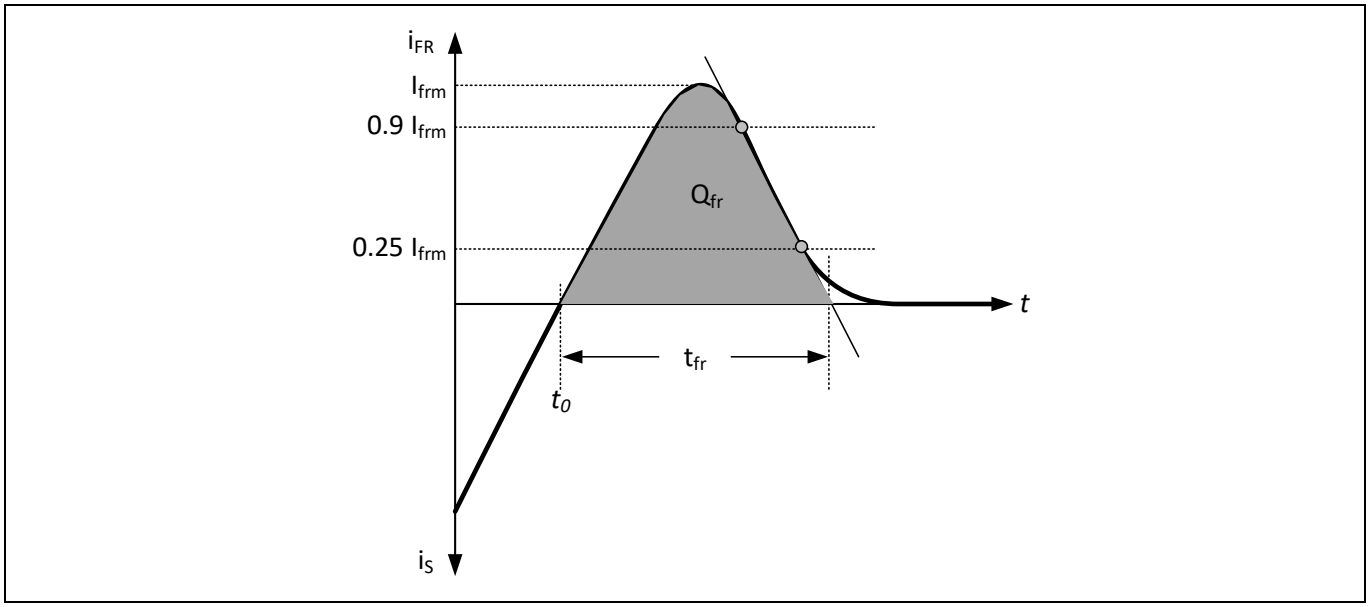


Figure 23 Definition of reverse recovery of MOSFET (following IEC 60747-8)

6 Other graph-related data

6.1 Safe operating area (SOA)

The safe operating area (SOA) defines the range of voltage and current limits guaranteed by the manufacturers for device safety. Operating outside the SOA can lead to the destruction or degradation of the device. The SOA is basically determined by some design parameters and some calculations, but Infineon verifies it through SOA characterization tests and defines it with additional safety margin.

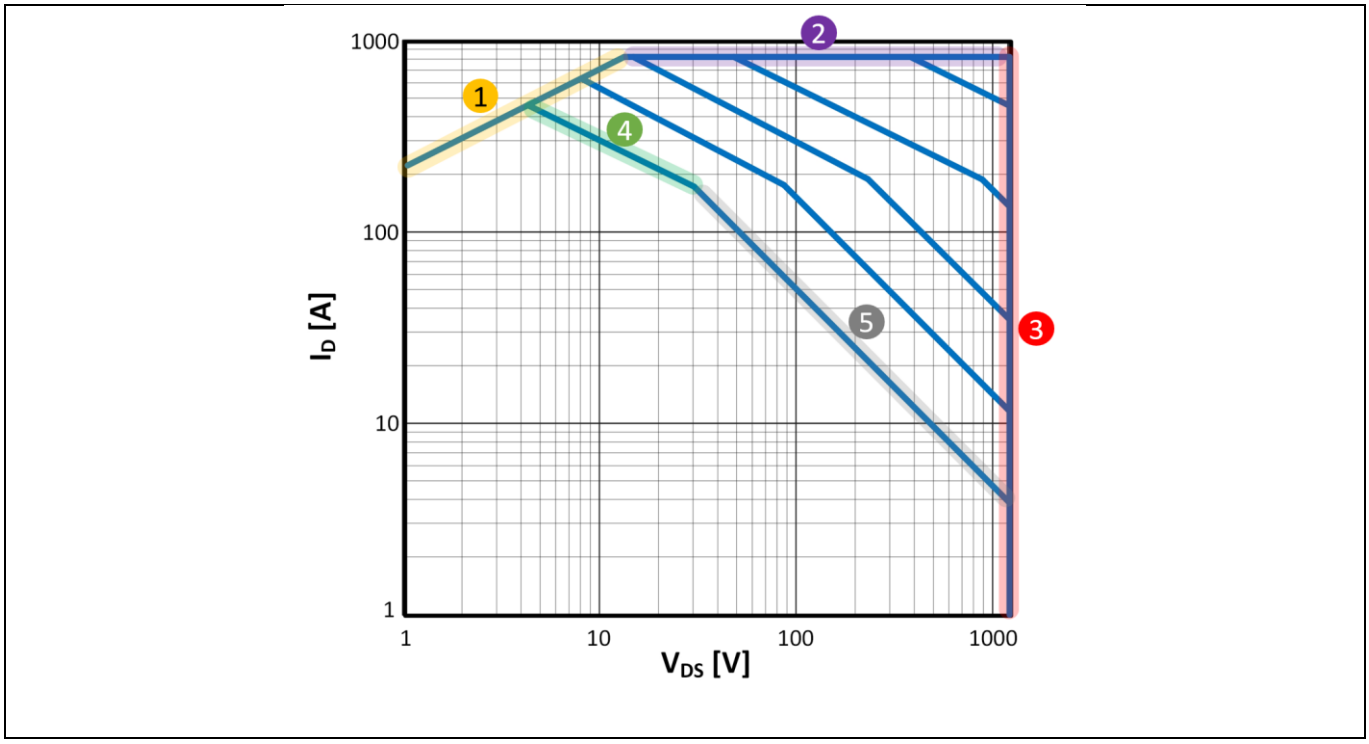


Figure 24 Example of a safe operation area (SOA)

The parameters to determine SOA are:

1. $R_{DS(on)}$
2. Peak drain current
3. Rated drain voltage
4. Power dissipation that the device guarantees
5. The thermal instability limited by local thermal thermal runaway due to negative temperature coefficient of g_{fs} at low gate voltage

1 to 3 are design parameters, while 4 and 5 are based on calculations.

6.1.1 $R_{DS(on)}$ Limit ①

$$I_{D.limit}@V_{DS} = \frac{V_{DS}}{R_{DSon}@V_{GS}=18V\ \&\ T_{vj}=T_{vj.max}} \quad (15)$$

6.1.2 Peak drain current, I_{DM} limit ②

$$I_{D.limit}@V_{DS} = I_{DM} \tag{16}$$

6.1.3 Drain-source voltage, V_{DSS} limit ③

$$V_{DS} = V_{DSS} \tag{17}$$

6.1.4 Power dissipation, P_{tot} limit ④

$$I_{D.limit}@V_{DS} = \frac{T_{vj.max} - 25}{V_{DS} * Z_{thj-c}} \tag{18}$$

6.1.5 Thermal stability limit ⑤

Following the maximum power limit-line ④ reveals a point at which the slope of the limit-line changes. This point indicates the onset of the limit-line for thermal instability. To understand the origin of this limitation, it is necessary to consider the criteria for thermal instability. A SiC MOSFET is a very fast switching device, therefore, the power may be generated faster during switching transitions than the power dissipated over temperature. In such a condition the temperature of the system becomes unstable and the system is not in a thermal equilibrium unlike Eq. (1) and is limited by the power dissipation.

$$P_{gen.} > P_{dis.} \tag{19}$$

$$V_{DS} \frac{\partial I_D}{\partial T_{vj}} > \frac{1}{Z_{thj-c}} \tag{20}$$

Where $\frac{\partial I_D}{\partial T_{vj}}$ is defined as the temperature coefficient.

As $V_{DS} > 0$ and $1/Z_{thj\text{-}c} > 0$, the thermal instability can occur only if the temperature coefficient of the drain-to-source current is positive. The question under what conditions such a positive temperature coefficient can be found is answered by Figure 16 that shows I_{DS} over V_{GS} for various temperatures. The theoretical thermal runaway limit point can be driven by:

$$V_{DS} \cdot Z_{th} \cdot \frac{\partial I_D}{\partial T} = 1 \tag{21}$$

However, as the temperature coefficient is unknown, users cannot calculate the limit easily by the thermal runaway, but the manufacturer can limit it with calculation.

6.1 Dead time effect

When the body diode of a SiC MOSFET starts conducting current, it gradually accumulates plasma until an equilibrium between the carrier generation and recombination is achieved. The diode voltage is initially high but as the plasma concentration increases it decreases to a steady state value. If the set dead time is very short the plasma in the drift region, at the instant when the body diode is turned off, cannot be fully constructed by the

opposite SiC MOSFET that turns on. In such a scenario, the amount of charge that is discharged from the drift region is lesser than that in the case of a longer dead time. Consequently, the reverse recovery current of the body diode reduces leading to a lower recovery energy, E_{fr}. On the other hand, when the bridge leg operates in the commutation mode, the reverse recovery loss of the SiC MOSFET's body diode is added to the turn-on energy, E_{on}, of the opposite switch.

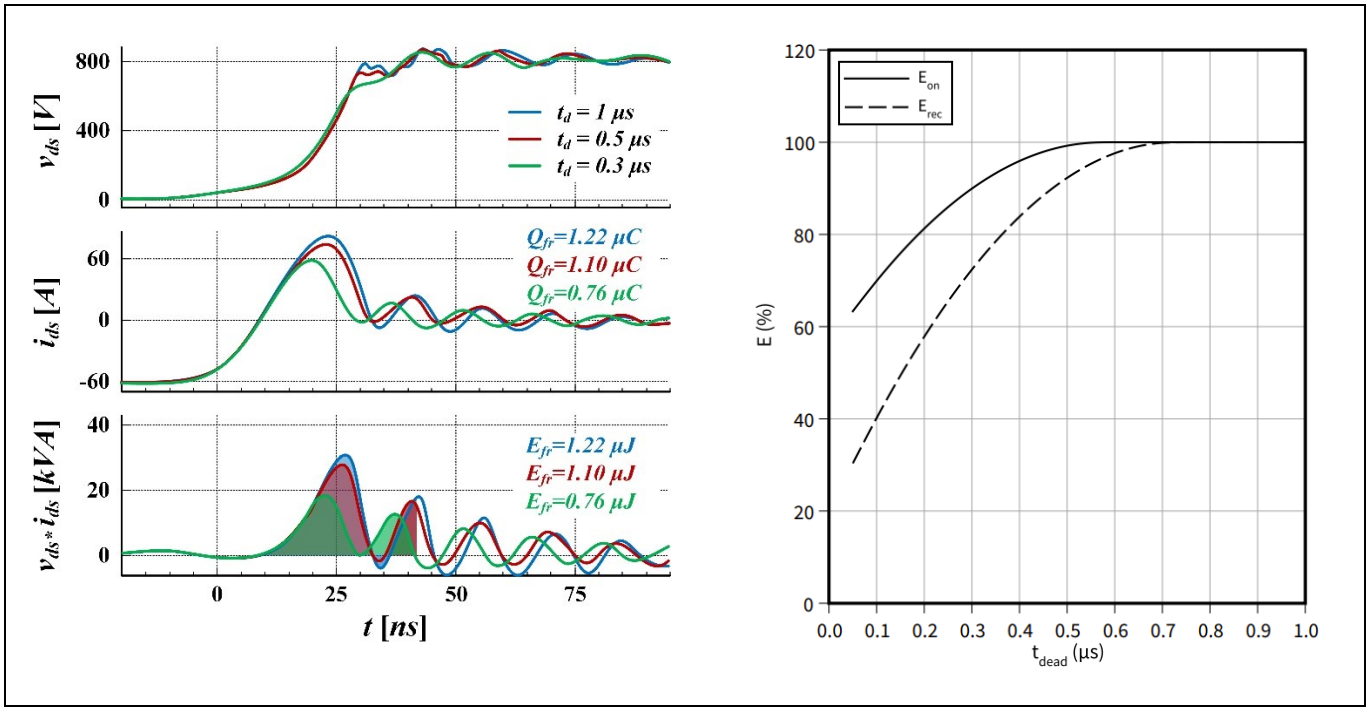


Figure 25 Turn-off waveforms of a SiC MOSFET's body diode for different dead times at 175°C (left), and the typical switching energy as a function of dead time (right)

In Figure 25, the impact of different dead times is illustrated. Compared to 1 *µs*, a significant reduction in reverse recovery charge can be observed for a dead time of 300 *ns*, and a smaller value can be obtained by applying a smaller dead time. Meanwhile, the plasma concentration in the drift region saturates somewhere between 500 *ns* and 1 *µs*. At a dead time ≥ 1 *µs*, no difference is observed in the reverse recovery behavior.
Due to the reduced plasma concentration, a short dead time can significantly reduce the recovery losses, overvoltage, and associated oscillation behavior, which also makes it possible to use lower gate resistance, R_g. System performance can be maximized by minimizing the dead time, but there are practical limitations on how much it can be reduced in a typical application.

6.1.1 Selecting the optimum dead time in hard-switching applications

In hard-switching applications, the dead time relies highly on the device's switching behavior. The simplest approach for predicting the switching speed of a power semiconductor device is to consider the total gate charge Q_g of the device. This is because when the gate voltage reaches the driving voltage level completely, it has been observed that the turn-on process of the device is complete. Conversely, when the gate voltage reaches 0, it means that the device's turn-off process is complete.
The theoretical switching turn-off waveform of a SiC MOSFET is shown in Figure 26. As shown in the figure, the switching turn-off transition is complete when $V_{GS}(t)$ reaches the threshold voltage, $V_{GS(th)}$, level.

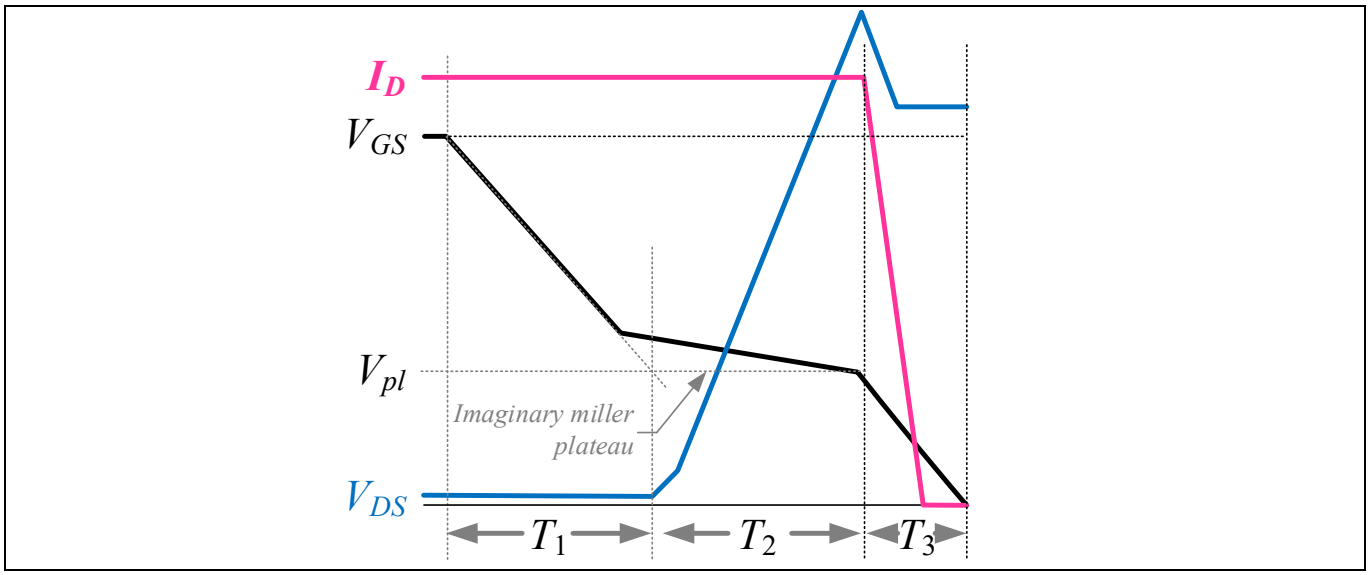


Figure 26 Turn-off behavior of a SiC MOSFET

Therefore, the minimum dead time can be obtained by:

$$DT_{min} \geq k_{dt}(T_1 + T_2 + T_3) \tag{22}$$

Where,

$$T_1 \geq R_{G,tot} \cdot C_{iss} \cdot ln\left(\frac{V_{GS}}{V_{pl}}\right) \tag{23}$$

$$T_2 \geq R_{G,tot} \cdot C_{rss}\left(\frac{V_{DD}}{V_{pl}}\right) \tag{24}$$

and,

$$T_3 \geq R_{G,tot} \cdot C_{iss} \cdot ln\left(\frac{V_{pl}}{V_{th\_low}}\right) \tag{25}$$

Here, $R_{g,tot}$ is the sum of $R_{g,int}$ given in the datasheet and $R_{g,ext}$ is user-applied for system tuning.

$$R_{G,tot} = R_{G,int} + R_{G,\text{ext}} \tag{26}$$

Here k_{dt} is an additional time margin constant considering the propagation delay of the gate driver IC and the parameter distribution of the SiC MOSFET. A value between 1.5 and 2 is appropriate in most cases. Meanwhile, to avoid additional time delay by a limited driving current, the output current capability, I_{Go}, of the driver IC should be:

$$I_{Go,min} \geq \frac{V_{GS}}{R_{g,tot}} \quad (27)$$

Overall, the dead time in real systems can be shorter than what is currently applied. To ensure proper system reliability, the minimum dead time must be confirmed by measuring the switching behavior in the target application.

7 Conclusion

This application note described the contents of the datasheet of the CoolSiC™ MOSFET 1200 V, including its features and the results of a performance characterization. Some general, practical design guidelines were highlighted for designing the CoolSiC™ MOSFET into a power system.

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