

PrimePACK™ power modules FF1800R23IE7 and FF2400RB12IP7 for solar central inverters

About this document

Scope and purpose

The PrimePACK™ power modules FF1800R23IE7 and the FF2400RB12IP7 have been developed for 1500 V DC solar central inverter applications. This application note introduces the 2300 V TRENCHSTOP™ IGBT7 E7 and the emitter-controlled diode EC7. It also provides design hints and recommendations to achieve a low inductive DC link design for a 3-level neutral point clamp topology (NPC2, T-type).

Intended audience

The intended audience for this document is design engineers, technicians, and developers of electronic systems.

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1 Introduction

1.1 Instructions

This application note provides a possible use case and an explanation of the parameters and diagrams given in the datasheet of the 2300 V TRENCHSTOP™ IGBT7 module – FF1800R23IE7, and the 1200 V TRENCHSTOP™ IGBT7 common collector module – FF2400RB12IP7. It includes background information for power electronic system designers and clarifies, in detail, the information given in the datasheet. Both modules come with pre-applied thermal interface material.

The information in this application note is only a reference for implementation of the devices and should not be regarded as a description or warranty of any functionality, condition, or quality of the device.

Recommended reading for more information about IGBTs and their usage:

- AN2011-05 Industrial IGBT Modules Explanation of Technical Information [3]
- AN2009-08 V2.0 Application and Assembly Notes for PrimePACK™ Modules [4]
- Repetitive Short Circuit Behaviour of Trench-/Field-Stop IGBTs [5]
- 2300 V – A new voltage class for Si IGBT and Si FWD [6]
- PrimePACK™ with 2300 V and 1200 V TRENCHSTOP™ IGBT7 enabling 1500 V-DC NPC2 in MW solar central inverter [7]
- IGBT Modules Technologies, Driver and Application [9]

1.2 Chip technology

In both modules, 7th generation IGBT and diode are used. In this generation, the IGBT structure is based on the micropattern trenches cell design (MPT). Details on how this design was implemented can be found in [6].

2 Application of FF1800R23IE7

2.1 Introduction

This application note supplements the existing PrimePACK™ application notes and describes the various possible topologies that use the FF1800R23IE7 module. A couple of configurations are shown in detail including the busbar design. These reference designs are only an example of how the module can be utilized and users must fully test them for application specific requirements before implementing them in an inverter.

2.2 Modules used

The modules used for various designs in this application note are:

- FF1800R23IE7 – 2300 V PrimePACK™ 3+ module built in the dual (half-bridge) configuration
- FF2400RB12IP7 – 1200 V PrimePACK™ 3+ module built in the common collector configuration

2.3 Possible topologies

The FF1800R23IE7 module has been designed to suit solar applications with a DC link voltage of 1500 V. There can be two possible topologies – 2-level and 3-level NPC2.

Advantages of the 2-level topology are well-known and established – low inductive busbar design, simple control and system design. Figure 1 shows the simplified circuitry of one phase of a 2-level topology. Figure 1 (a) shows two half-bridge modules in parallel and Figure 1 (b) shows three half-bridge modules in parallel per phase to increase the current capacity of each inverter phase leg.

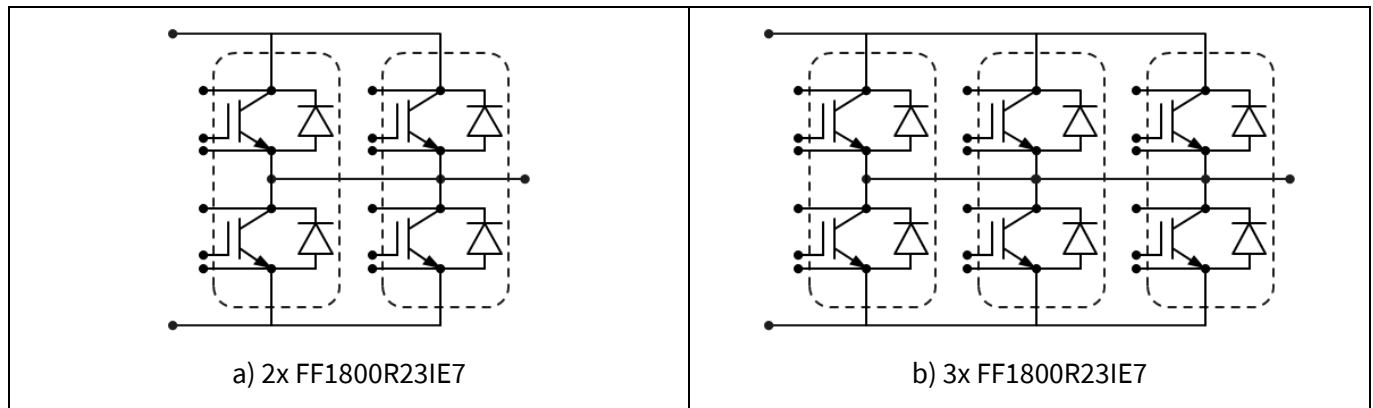


Figure 1 **Possible 2-level topologies with FF1800R23IE7 modules**

Advantages of the 3-level NPC2 topology are lower harmonics and higher efficiency due to reduced losses. This may reduce the output filter's requirements and size. Figure 2 (a) shows a 3-level NPC2 topology using FF1800R23IE7 and FF2400RB12IP7 modules. Figure 2 (b) shows an additional FF1800R23IE7 module being used in parallel to increase the current capacity of each phase leg of the inverter. Sections 3.1 and 3.2 provide implementation details of the designs shown in Figure 2 (a) and Figure 2 (b) respectively.

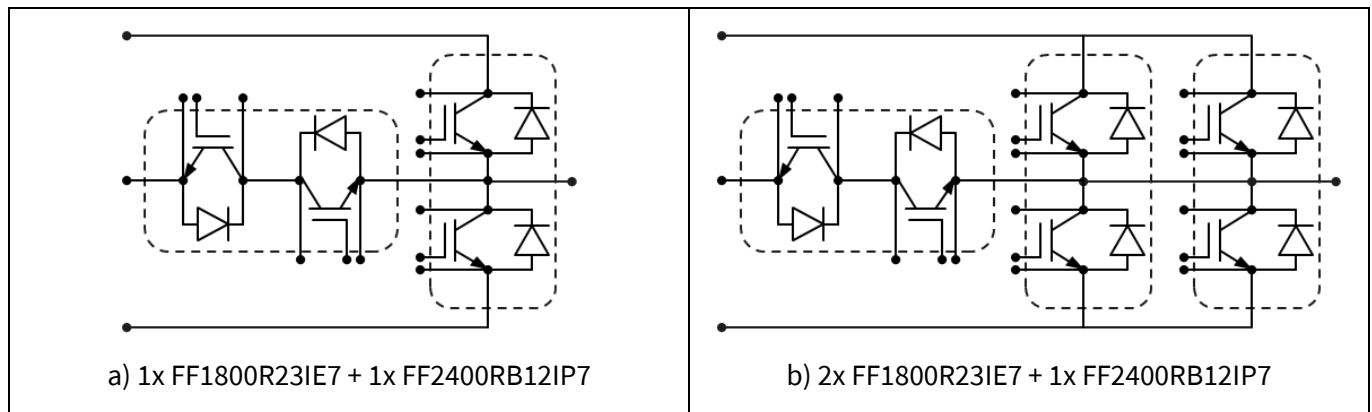


Figure 2 **Possible NPC 2 topologies using FF1800R23IE7 and FF2400RB12IP7 modules**

The choice of topology depends on system requirements. Infineon has modules that can work in either setup, users must verify all implementations before deploying them.

2.4 Gate drive units

The IGBT gate driver has to perform multiple functions from turning the IGBT ON and OFF to protection. Chapter 6 in [9] provides a detailed description of the various functions that the gate driver needs to perform. Additional features of the gate driver depend on the system design.

The main points to consider while designing or choosing a gate driver for the FF1800R23IE7 and FF2400RB12IP7 modules are:

- Turn ON voltage – an ON voltage of +15 V is recommended
- Turn OFF voltage – a negative OFF voltage of at least -7 V is recommended to prevent the risk of parasitic turn ON due to high dv/dt
- Gate resistors – in a voltage-driven gate driver the gate resistors influence the current and voltage slopes during turn ON and turn OFF sequences. Based on system specifications of losses and EMI, the gate resistors have to be appropriately selected. The application note – AN2015-06 Gate resistor for power devices [11] – provides comprehensive information on selecting gate resistors. Also, the datasheets of both modules have useful graphs on loss versus gate resistor and switching time versus gate resistor that can help in selecting gate resistors. It is ideal to select gate resistors within the specified range.

2.5 Overload conditions

2.5.1 Definition of 175°C operation junction temperature

Most IGBT modules are defined for operating at a continuous junction temperature of 150°C. FF1800R23IE7 and FF2400RB12IP7 are designed for overload conditions as well, where they can operate at a junction temperature of up to 175°C for a limited period of time.

An overload condition is defined as a period when the virtual junction temperature of the module exceeds 150°C. In an overload condition, the maximum virtual junction temperature allowed is 175°C. Figure 3 shows a simplified junction temperature profile during overload conditions. The duration of the overload condition must not exceed 1 second. Every time the temperature exceeds 150°C and the duration of overload is less than 1 second it is considered an overload event. The maximum junction temperature of 175°C according to Figure 3 is specified for 1000 events.

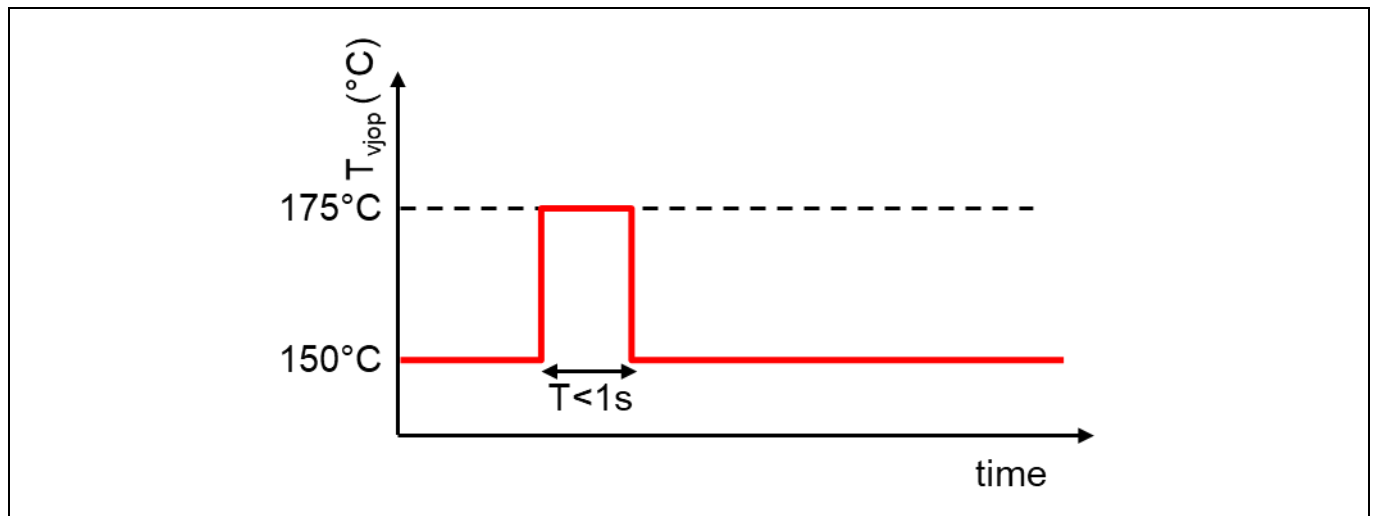


Figure 3 **Overload capability of FF1800R23IE7 and FF2400RB12IP7 modules**

This extended junction specification provides an additional margin to deal with external faults or overload conditions within an application. For example, during a low voltage ride through (LVRT) grid fault event the module can operate at a higher temperature for a short duration without breaking down. With this extra margin, power modules can continue operating at the continuous junction temperature providing a higher nominal current than previous generation modules that were defined for a maximum junction temperature of 150°C.

2.5.2 Simulated example of an overload condition

Figure 4 shows the junction temperature of devices based on simulation of an LVRT fault situation. In this simulation, a 3-phase 2-level inverter was considered with a FF1800R23IE7 module and a Discontinuous Pulse Width Modulation switching strategy. An LVRT condition was triggered 500 seconds after the model was in a steady state condition.

The steady state condition for this simulation was:

- $V_{DC} = 1200\text{ V}$
- $V_{AC} = 600\text{ V}$
- $I_{OUT} = 600\text{ A}$
- Switching frequency = 3 kHz
- Modulation index = 0.78
- Case-to-heatsink thermal resistance = 51.9 K/kW
- Ambient temperature = 30°C

With these conditions the maximum junction temperature at steady state was 150°C, as shown in Figure 4, before the LVRT condition at 500 seconds.

The LVRT condition was triggered at 500 seconds by modifying the output load – the output voltage V_{AC} was reduced to 30 V, the output current I_{OUT} was increased to 720 A (120% of the designed nominal current) for a duration of 50 milliseconds and then reduced to 600 A for a duration of 700 milliseconds. This LVRT sequence is an example of how to simulate the overload condition and not a specific grid code. After this, the LVRT cleared and the inverter returned to a steady state condition with $I_{OUT} = 600\text{ A}$. The junction temperature rose by ~25 K during the LVRT event but did not cross the limit of 175 °C. Additionally, the maximum junction temperature returned to 150°C within 1 second of the start of the LVRT condition. This simulation demonstrates the benefits of the additional margin in this inverter design during grid fault conditions.

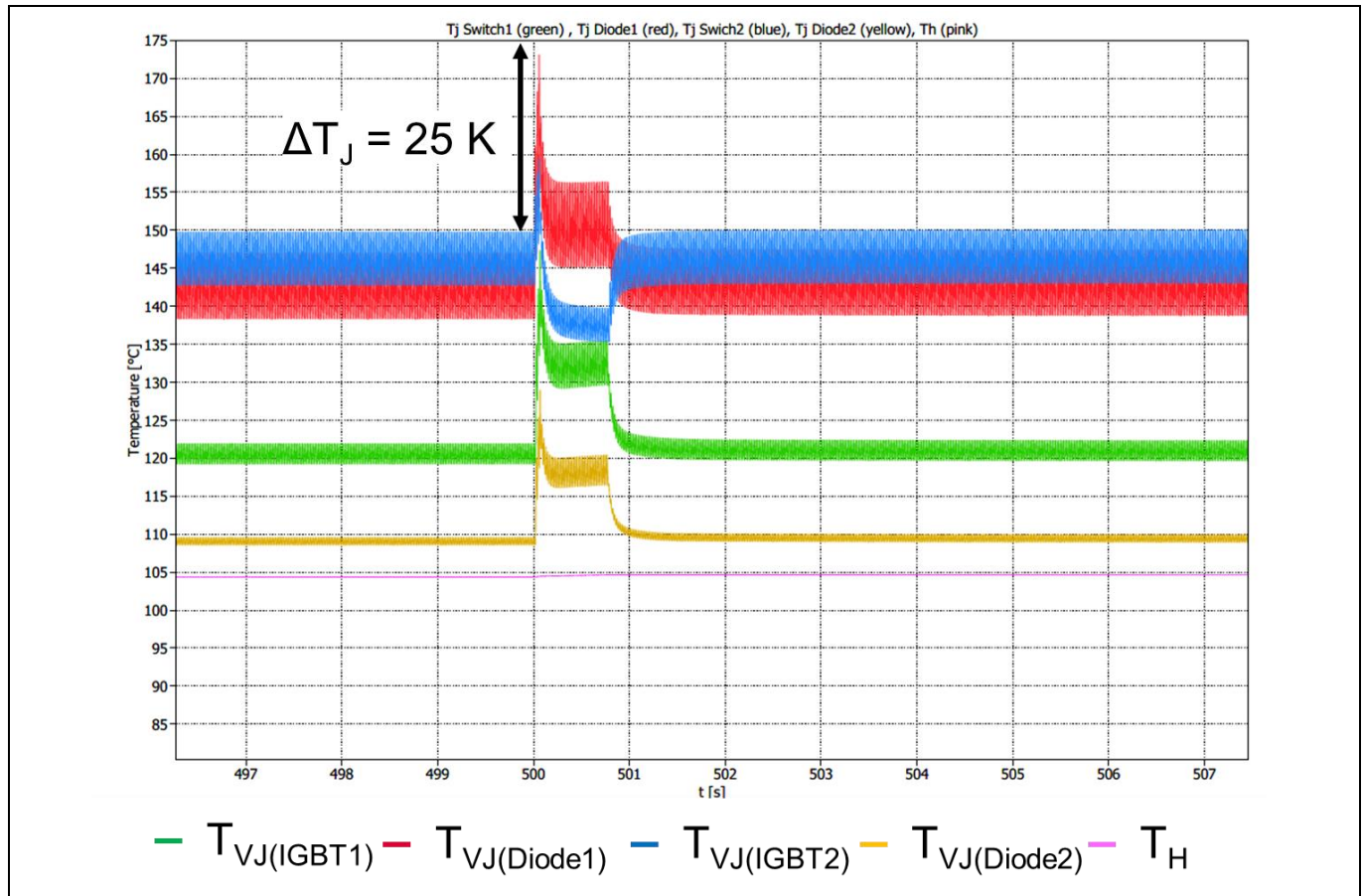


Figure 4 **Simulated junction temperatures of IGBTs during an LVRT event**

2.6 Cosmic radiation

The FF1800R23IE7 module is designed to operate continuously at 1500 V_{DC}. With this blocking voltage, the module provides a typical CR-FIT rate of CR < 100 FIT at 25°C and 0 meters above sea level. This makes the FF1800R23IE7 ideal for all applications operating at the highest possible DC voltage allowed by the low voltage directive. Compared to lower DC voltages, a higher power density for the inverter is possible with higher DC voltage.

2.7 Difference between inverter data and 3-level data

The data sheet of the FF1800R23IE7 module is divided into two sections:

- IGBT and diode for inverter applications
- IGBT and diode for 3-level applications

The difference between the two sections are the conditions at which the modules were tested. The data for the 2-level inverter was used to test the module in a half-bridge configuration and the commutation was done within FF1800R23IE7. The data for the 3-level inverter was used to test the module in an NPC2 configuration and was specified with the common collector module, FF2400RB12IP7, as the neutral point clamp device during commutation.

3 Example designs

Infineon has made two sample design setups using the FF1800R23IE7 and FF2400RB12IP7 modules. The design possibilities presented in this document must be validated by users before implementation. It is recommended that the designs be as symmetrical as possible to ensure that all devices are loaded equally to prevent/reduce any temperature mismatch. In a 3-level design, attention must be paid to the external commutation path and its parasitic inductance with respect to overvoltage of the devices.

3.1 NPC2 with FF1800R23IE7 and FF2400RB12IP7 modules

One design that has been constructed and tested is that of a power stack using one FF1800R23IE7 module and one FF2400RB12IP7 module in an NPC2 configuration. The circuit diagram is shown in Figure 2 (a). The test setup is built for one phase leg. The phase leg has been tested and characterized based on the well-known double-pulse test. Further measurements are available in [7].

For the busbar design, the number of layers has been limited to three to minimize complexity. Figure 5 shows the layers of the busbar layout that have been tested. The first layer shares and connects the individual AC and DC+. Both layers are not rectangular, but rather L-shaped. The second layer is the DC neutral point and the third is the DC layer. With this setup the simulated parasitic inductance (without the DC capacitors) is approximately 26 nH.

For characterization and measurement, the test setup includes DC capacitors and current measurements. These elements along with the mechanical accommodations made to include them in the loop increase the parasitic inductance to 50 nH.

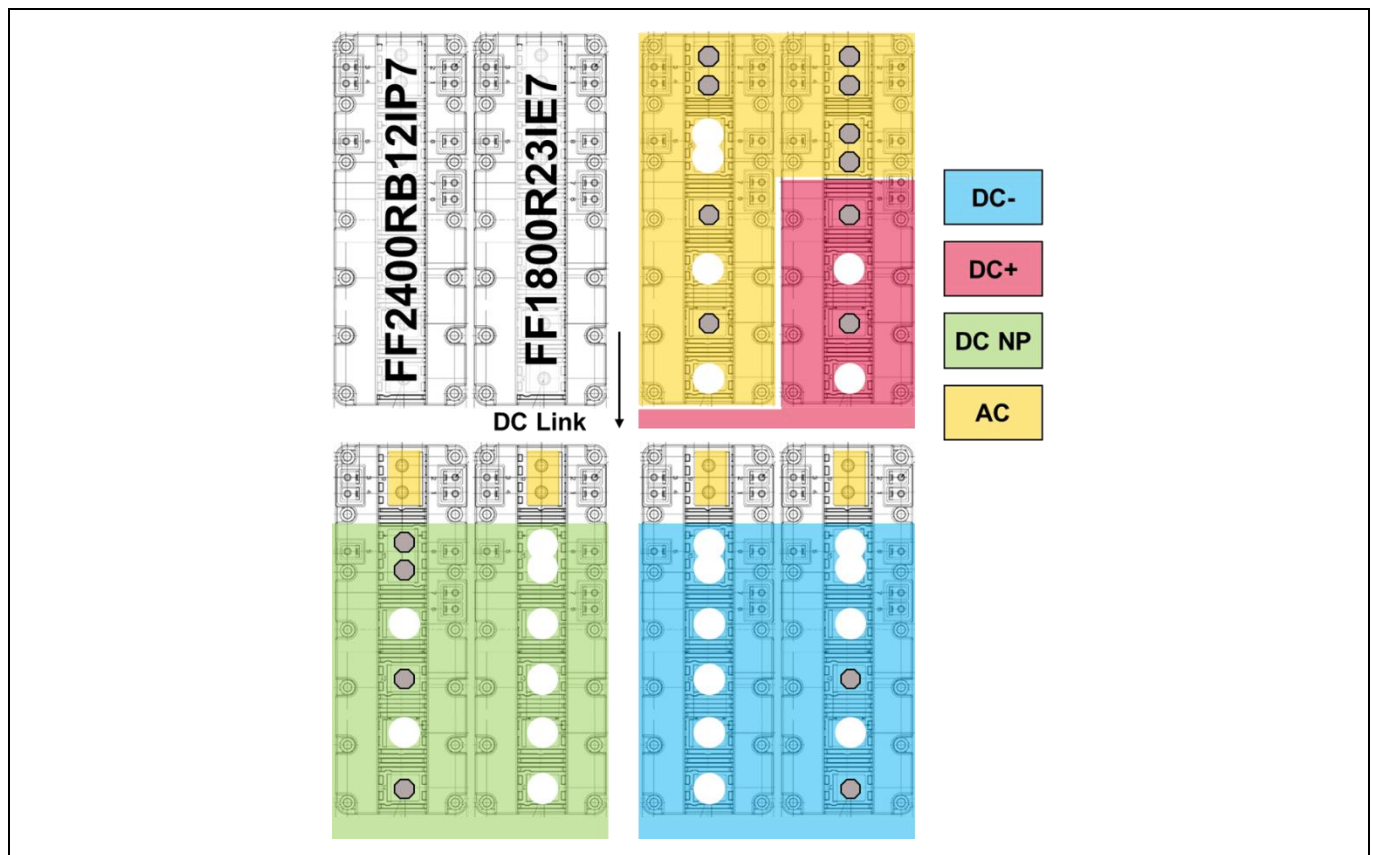


Figure 5 DC link concept: Busbar design

Example designs

3.2 NPC2 with three modules

For increased current and power levels another design has been constructed and tested using two FF1800R23IE7 modules in parallel and one FF2400RB12IP7 module in an NPC2 configuration. The simplified circuit diagram is shown in Figure 2 (b). The test setup is built for one phase leg. The phase leg has been tested and characterized based on the double-pulse test. Further measurements are available in [8]. The simulated parasitic inductance here (without DC capacitors) is approximately 15 nH.

Similar to the previous configuration, during characterization and measurement, the DC capacitors, current measurement, and necessary mechanical accommodations increase the parasitic inductance to approximately 40 nH.

For the busbar design, the number of layers has once again been limited to three to minimize complexity. Figure 6 shows the implementation of this stack design. To maintain a symmetric design, the FF2400RB12IP7 module is placed between the FF1800R23IE7 modules. The capacitors for the DC link are arranged beside the modules. This placement also ensures that the air flow over the module heatsink is not obstructed by the capacitors. It should be noted that the FF2400RB12IP7 module in the NPC2 topology switches at 50 Hz and generates lower losses compared to the FF1800R23IE7 module (for $\cos\phi = 1$).

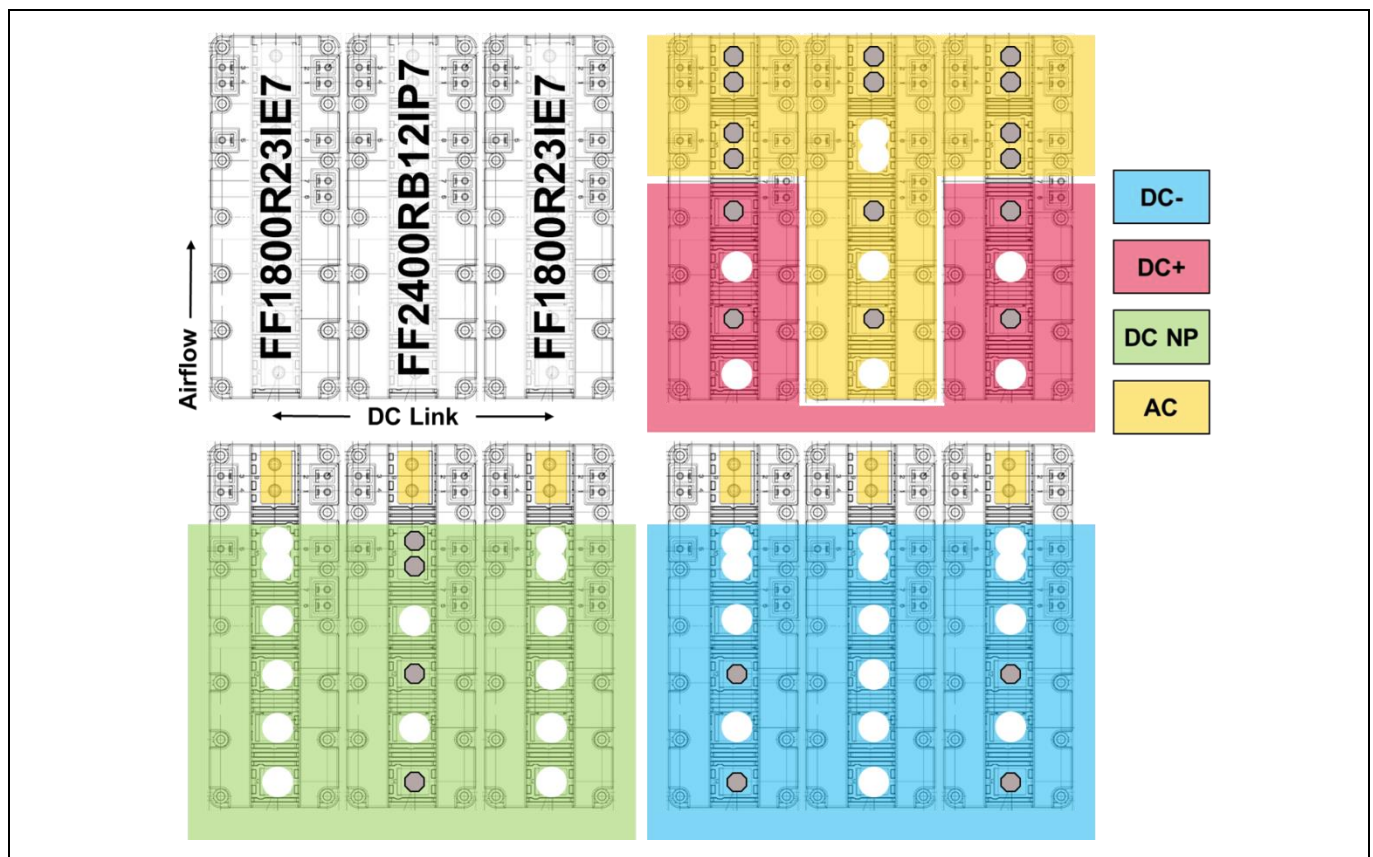


Figure 6 DC link concept: Busbar design

For all selected and proposed setup examples, the application note “AN2009-08 V2.0 Application and Assembly Notes for PrimePACK™ Modules” [4] should be considered.

4 References

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Revision history

Revision history

Document revision	Date	Description of changes
1.00		First version

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