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x8 SPI Device Software Development Guide

Doc. # 002-28659 Rev. **

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1.1 Interface Overview

1.1.1 General Description

The Cypress Semper™ Flash Octal family of products are high-speed CMOS, MirrorBit NOR flash devices that are compliant with the JEDEC JESD251 eXpanded SPI (xSPI) specification. Semper Flash is designed for Functional Safety with development according to ISO 26262 standard to achieve ASIL-B compliance and ASIL-D readiness.

Semper Flash with Octal Interface devices support both the Octal Peripheral Interface (OPI) as well as Legacy x1 Serial Peripheral Interface (SPI). Both interfaces serially transfer transactions reducing the number of interface connection signals. SPI supports SDR whereas OPI supports both SDR and DDR.

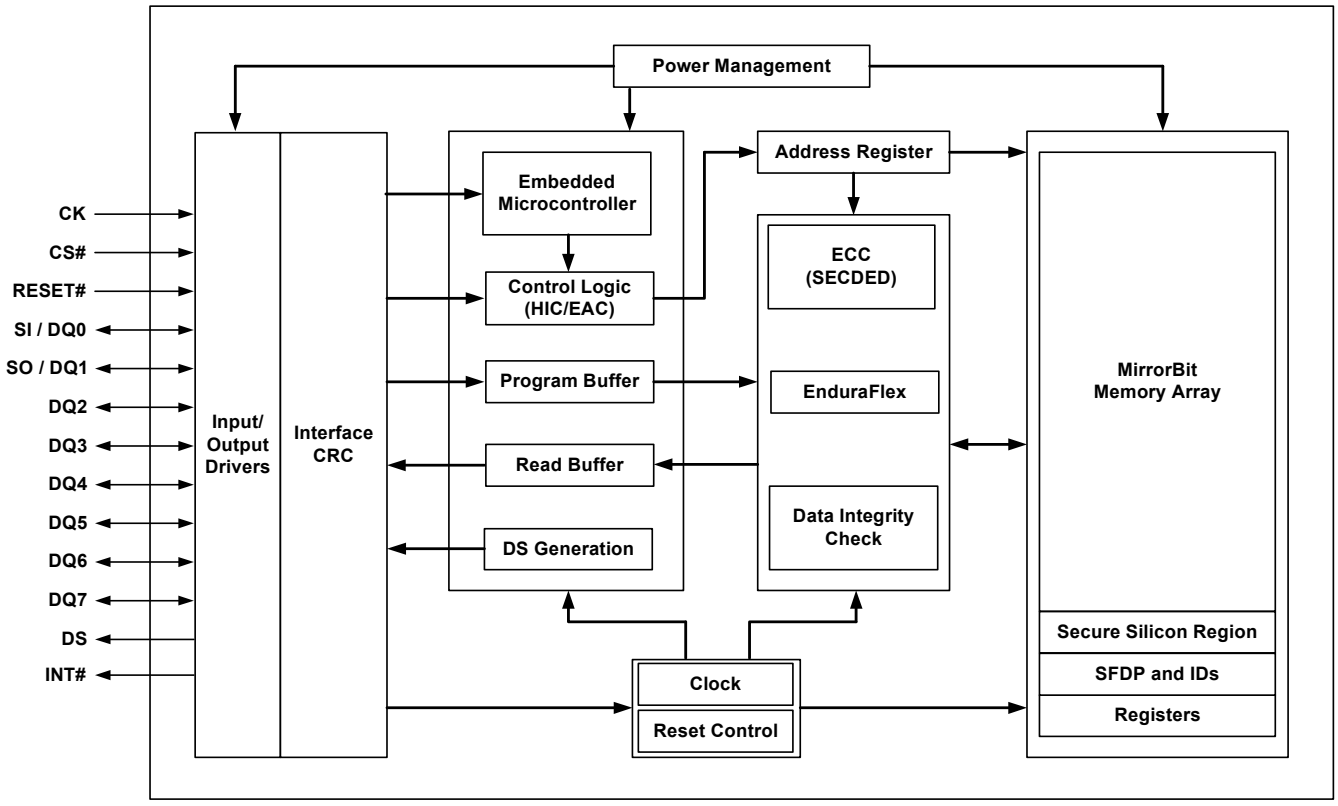
Read operations from the device are burst oriented. Read transactions can be configured to use either a wrapped or linear burst. Wrapped bursts read from a single page whereas linear bursts can read the whole memory array.

The erased state of each memory bit is a logic 1. Programming changes a logic 1 (HIGH) to a logic 0 (LOW). Only an erase operation can change a memory bit from a 0 to a 1. An erase operation must be performed on a complete sector (4 KBs or 256 KBs).

Semper Flash provides a flexible sector architecture. The address space can be configured as either a uniform 256 KB sector array, or a hybrid configuration 1 where thirty-two 4 KB sectors are either grouped at the top or at the bottom while the remaining sectors are all 256 KB, or a hybrid configuration 2 where the thirty-two 4 KB sectors are equally split between the top and the bottom while the remaining sectors are all 256 KB.

The Page Programming Buffer used during a single programming operation is configurable to either 256 bytes or 512 bytes. The 512 byte option provides the highest programming throughput.

Figure 1. Logic Block Diagram



The Semper Flash with Octal Interface family consists of multiple densities with, 1.8V and 3.0V core and I/O voltage options.

The device control logic is subdivided into two parallel operating sections: the Host Interface Controller (HIC) and the Embedded Algorithm Controller (EAC). The HIC monitors signal levels on the device inputs and drives outputs as needed to complete read, program, and write data transfers with the host system. The HIC delivers data from the currently entered address map on read transfers; places write transfer address and data information into the EAC command memory, and notifies the EAC of power transition, and write transfers. The EAC interrogates the command memory, after a program or write transfer, for legal command sequences and performs the related Embedded Algorithms.

Changing the nonvolatile data in the memory array requires a sequence of operations that are part of Embedded Algorithms (EA). The algorithms are managed entirely by the internal EAC. The main algorithms perform programming and erase of the main flash array data. The host system writes command codes to the flash device. The EAC receives the command, performs all the necessary steps to complete the transaction, and provides status information during the progress of an EA.

In addition to the mandatory SPI signals CK, CS#, SI/DQ0, SO/DQ1, and DQ[7:2], the Semper Flash with Octal Interface device also includes RESET#, DS and INT# signals. The RESET# transition from LOW to HIGH returns the device to the default state that occurs after an internal power-on reset (POR). The Data Strobe (DS) is synchronized with the output data during read transactions enabling host system to capture data at high clock frequency operation. The INT# is an open-drain output that can provide an interrupt to the device master to indicate when the device transitions from busy to ready at the end of a program or erase operation or to indicate the detection of an error (ECC) during read.

EnduraFlex™ Architecture provides system designers the ability to customize the NOR Flash endurance and retention for their specific application. The host defines partitions for high endurance or long retention, providing up to 1+ million cycles or 25 years of data retention.

The Semper Flash with Octal Interface device supports error detection and correction by generating an embedded Hamming error correction code during memory array programming. This ECC code is then used for single-bit and double-bit error detection and single-bit correction during read.

The Semper Flash with Octal Interface device has built-in diagnostic features providing the host system with the device status.

- Program and Erase Operation: Reporting of program or erase success, failure and suspend status
- error detection and correction: 1-bit and/or 2-bit error status with address trapping and error count
- Data Integrity Check: Error detection over memory array contents
- Interface CRC: Error detection over device interface
- SafeBoot: Reporting of proper flash device initialization and configuration corruption recovery
- Sector Erase Status: Reporting of erase success or failure status per sector
- Sector Erase Counter: Counts the number of erase cycles per sector

1.1.2 Signal Protocols

1.1.2.1 Semper Flash Octal and SPI Clock Modes

The Semper Flash with Octal interface device can be driven by an embedded microcontroller (bus master) in either of the following two clocking modes:

- **Mode 0** with Clock Polarity LOW at the fall of CS# and staying LOW until it goes HIGH at capture input.
- **Mode 3** with Clock Polarity HIGH at the fall of CS# then going LOW to HIGH at capture input.

For these two modes, data is latched into the device on the rising edge of the CK signal in SDR protocol and both edges of the CK signal in DDR protocol. The output data in SDR protocol is available on the falling edge of the CK clock signal and the output data in DDR protocol is available on the rising edge of the CK clock signal.

The difference between the two modes is the clock polarity when the bus master is in Standby mode and not transferring any data.

Figure 2. SPI SDR Mode Support

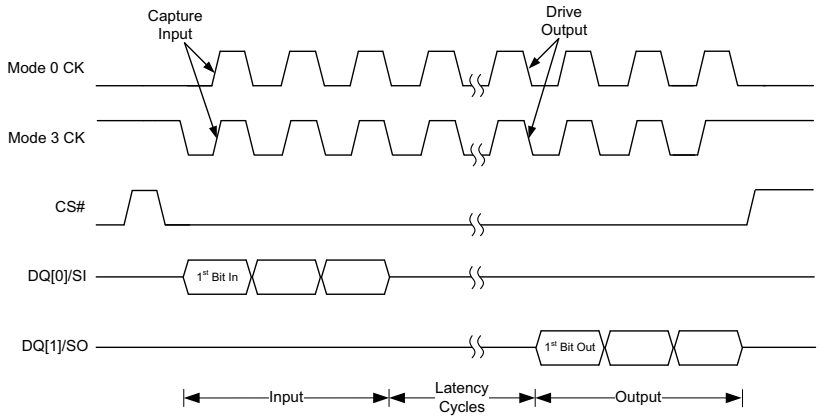
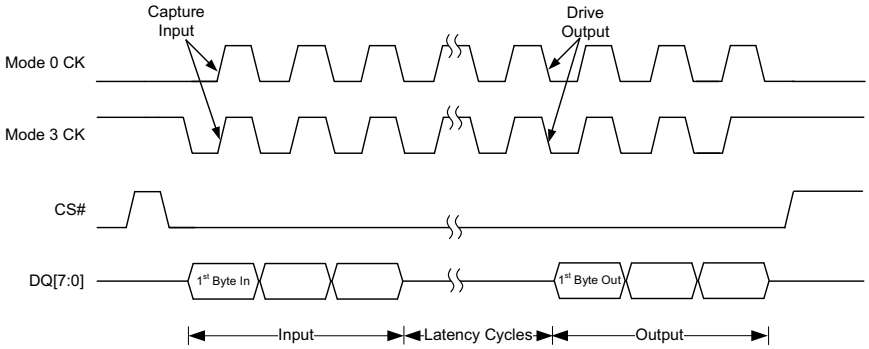
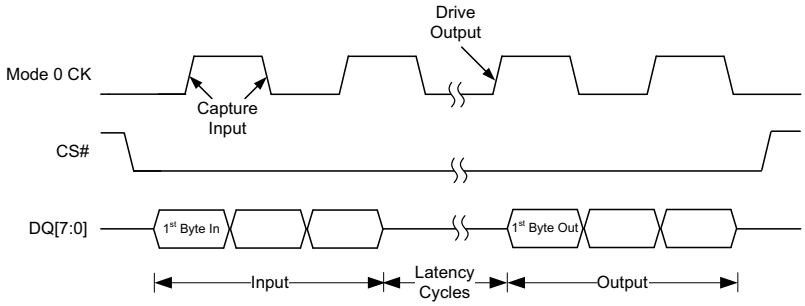


Figure 3. Octal SDR Mode Support



For Semper Flash Octal DDR mode operation, only clock Mode 0 is supported.

Figure 4. Octal DDR Mode Support



1.1.3 Transaction Protocol

Transaction

- During the time that CS# is active (LOW), the clock signal (CK) is toggled while command information is first transferred on the data (DQ) signals followed by address and data from the host to the flash device. The clock continues to toggle during the transfer of read data from the flash device to the host or write data from the host to the flash device. When the host has transferred the desired amount of data, the host drives the CS# inactive (HIGH). The period during which CS# is active is called a transaction on the bus.
- While CS# is inactive, the CK is not required to toggle.
- The command transfer occurs at the beginning of every transaction. The address, latency cycles, and data transfer phases are optional and their presence depends on the protocol mode or command transferred.

Transaction Capture

- CK marks the transfer of each bit or group of bits between the host and memory. Command, address and write data bits transfer occurs on CK rising edge in SDR transactions, or on every CK edge, in DDR transactions.

Protocol Terminology

- The number of DQ signals used during the transaction depends on the current protocol mode or command transferred. The latency cycles do not use the DQ signals for information transfer. The protocol mode options are described by the data rate and the DQ width (number of DQ signals) used during the command, address, and data phases in the following format:

  WR-WR-WR, where:
  - The first WR is the command bit width and rate.
  - The second WR is the address bit width and rate.
  - The third WR is the data bit width and rate.
- The bit width value may be 1, or 8. R has a value of S for SDR or D for DDR. SDR has the same transfer value during the rising and falling edge of a clock cycle. DDR can have different transfer values during the rising and falling edges of each clock.
- Examples:
  - 1S-1S-1S means that the command is 1 bit wide SDR, the address is 1 bit wide SDR, and the data is one bit wide SDR.
  - 8D-8D-8D means that the command, address, and data transfers are always 8 bits wide DDR.

Protocols Definition

- Protocol Modes defined for the Semper Flash Octal Interface:

  1.1S-1S-1S: One DQ signal used during command transfer, address transfer, and data transfer. All phases are SDR.

  2.8S-8S-8S: Eight DQ signals used during command transfer, address transfer, and data transfer. All phases are SDR.

  3.8D-8D-8D: Eight DQ signals used during command transfer, address transfer, and data transfer. All phases are DDR.

1S-1S-1S Protocol

- The 1S-1S-1S mode is the preferred default protocol following Power-On-Reset (POR), but flash devices can be configured to reset into the Octal mode.
- Each transaction begins with an 8-bit (1-byte) command. The command selects the type of information transfer or device operation to be performed.
- This protocol uses SI/DQ[0] to transfer information from host to flash device and SO/DQ[1] to transfer information from flash device to host. On each DQ, information is placed on the DQ line in Most Significant bit (MSb) to Least Significant bit (LSb) order within each byte. Sequential address bytes are transferred in highest order to lowest order sequence. Sequential data bytes are transferred in lowest address to highest address order.
- In 1S-1S-1S, DQ[7:2] are not used for data transfer period. Hence, the DQ[7:2] signals will be high impedance.

8S-8S-8S and 8D-8D-8D Protocols

- Each transaction begins with a 16-bit (two same bytes) command. The command selects the type of information transfer or device operation to be performed.
- Supports 4-byte addressing only.
- This protocol uses DQ[7:0] signals. The LSb of each byte is placed on DQ[0] with each higher order bit on the successively higher numbered DQ signals. Sequential address bytes are transferred in highest order to lowest order sequence. Sequential data bytes in SDR are transferred in lowest address to highest address order. Sequential data bytes in DDR are transferred only in byte pairs (words) where the byte order depends on the order in which the bytes are written or programmed in that protocol mode. Sequential data bytes are transferred in lowest address to highest address order.
- In this protocol, during the period of data transfer in a read transaction, the Data Strobe (DS) signal is driven by the flash device and transitions are synchronized (Edge aligned in DDR and center aligned in SDR protocol) with the DQ signal data transitions. DS is used as an additional output signal with the same timing characteristics as other data outputs but with the guarantee of transitioning with every data bit transferred.

Section 1.1.3.1 Serial Peripheral Interface (SPI, 1S-1S-1S) on page 9 and Section 1.1.3.2 Octal Peripheral Interface (Octal, 8S-8S-8S and 8D-8D-8D) on page 11 show all transaction formats by protocol mode.

1.1.3.1 Serial Peripheral Interface (SPI, 1S-1S-1S)

Figure 5. SPI Transaction with Command Input

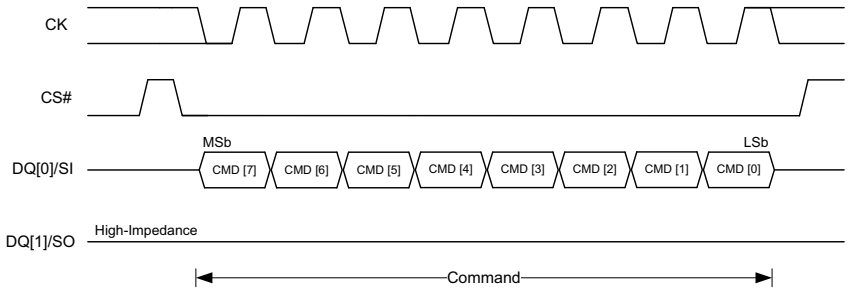


Figure 6. SPI Transaction with Command and Address Input

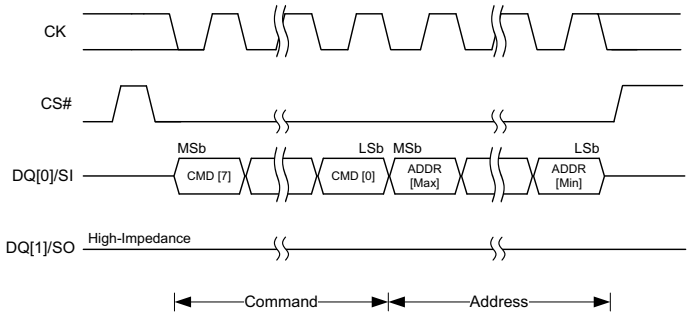


Figure 7. SPI Transaction with Command and Two Input Addresses

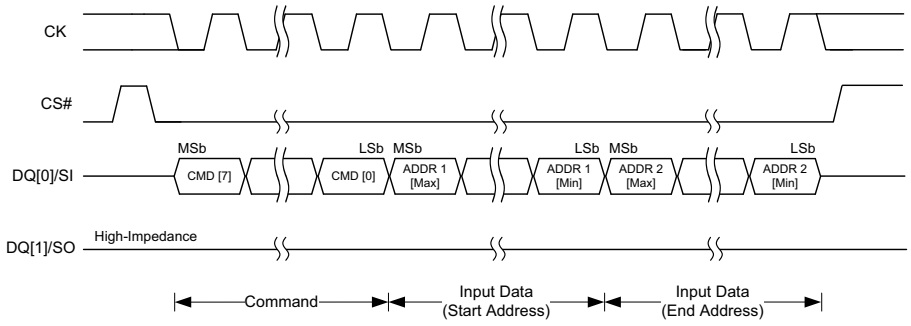


Figure 8. SPI Program Transaction with Command, Address, and Data Input

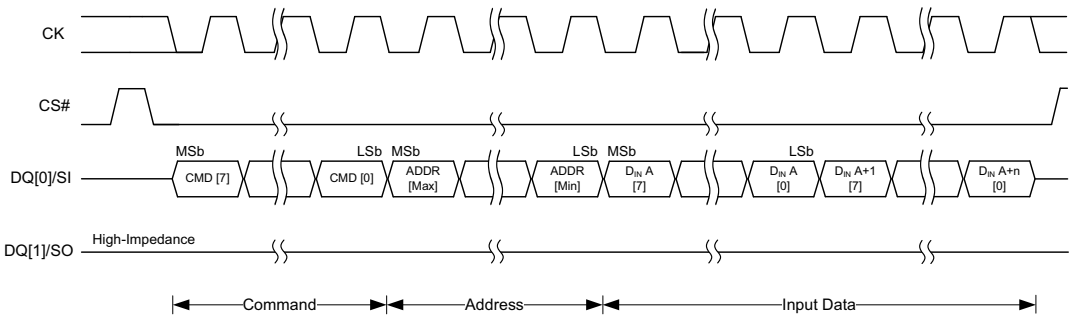


Figure 9. SPI Program Transaction with Command and Data Input

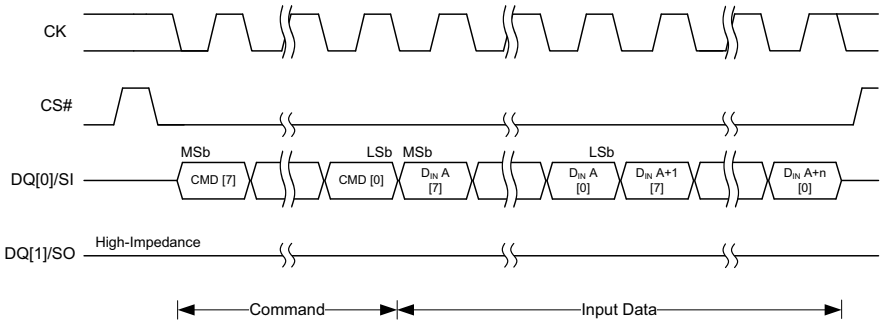


Figure 10. SPI Read Transaction with Command Input (Output Latency)

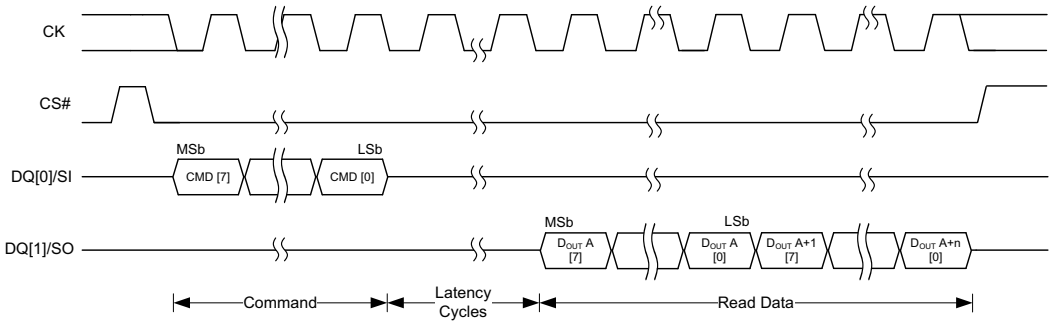


Figure 11. SPI Read Transaction with Command and Address Input (Output Latency)

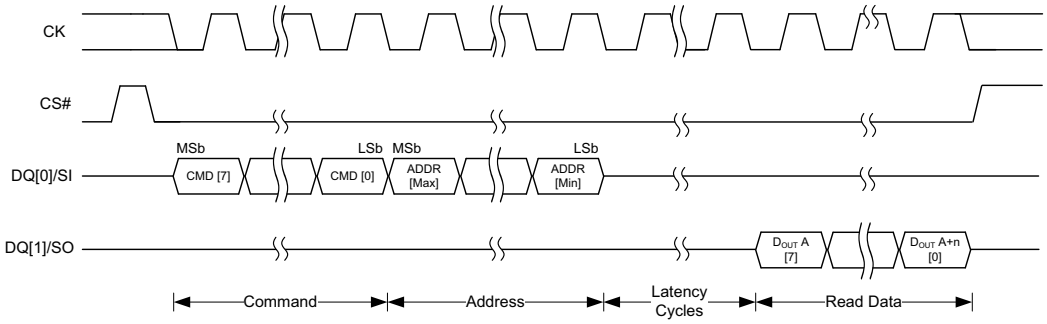


Figure 12. SPI Read Transaction with Command and Address Input (No Output Latency)

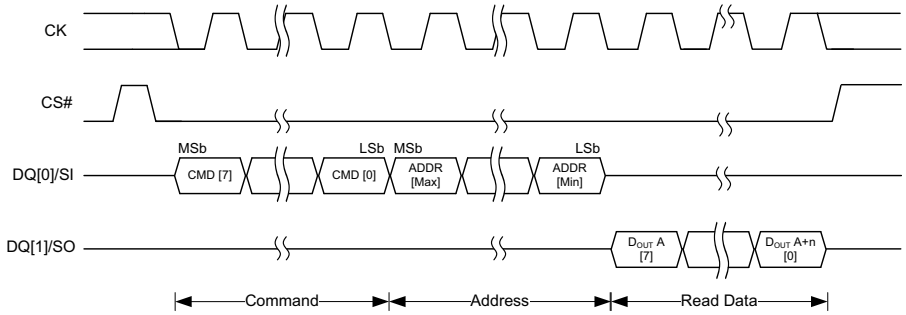
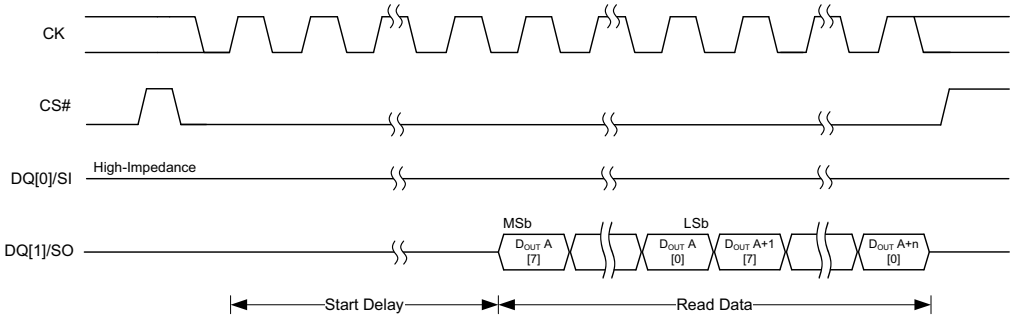


Figure 13. SPI Transaction with Output Data Sequence (AutoBoot)



1.1.3.2 Octal Peripheral Interface (Octal, 8S-8S-8S and 8D-8D-8D)

Figure 14. Octal SDR Transaction with Command Input

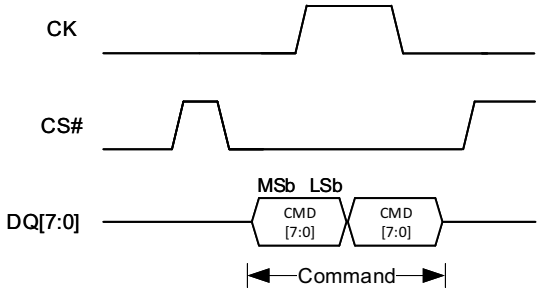


Figure 15. Octal DDR Transaction with Command Input

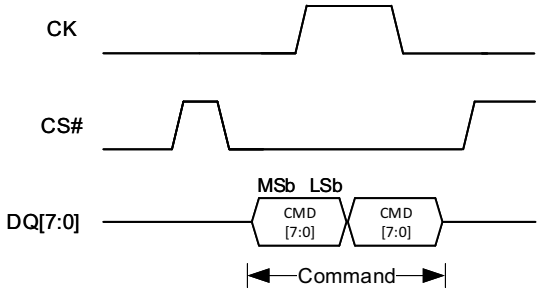


Figure 16. Octal SDR Transaction with Command and Address Input

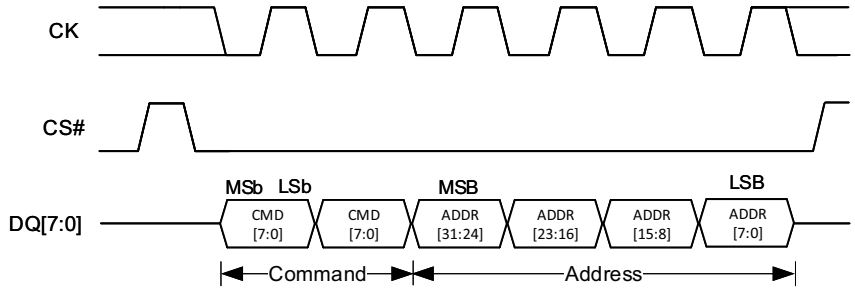


Figure 17. Octal DDR Transaction with Command and Address Input[1]

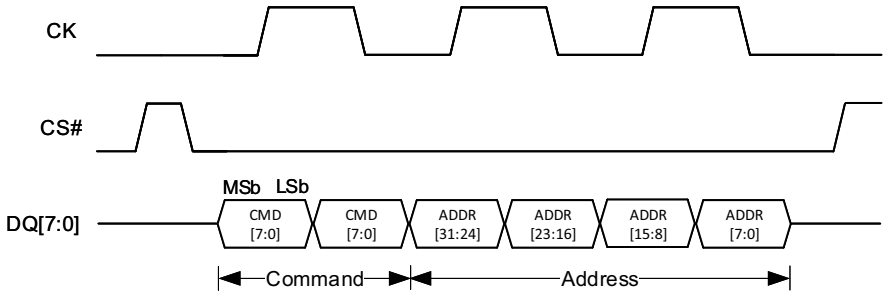


Figure 18. Octal SDR Transaction with Command and Two Input Addresses

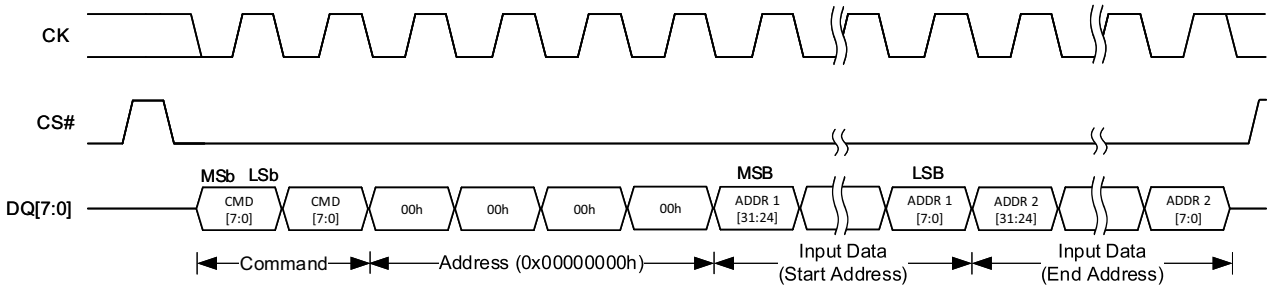
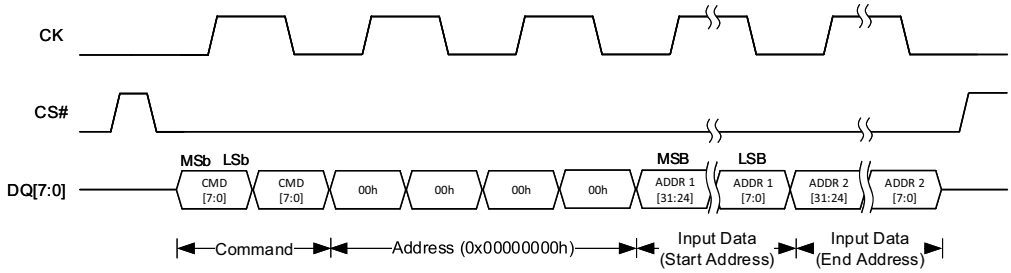


Figure 19. Octal DDR Transaction with Command and Two Input Addresses



Note
1. The LSb of the address always be zero in any Octal DDR transactions with the address input.

Figure 20. Octal SDR Program Transaction with Command, Address, and Data Input

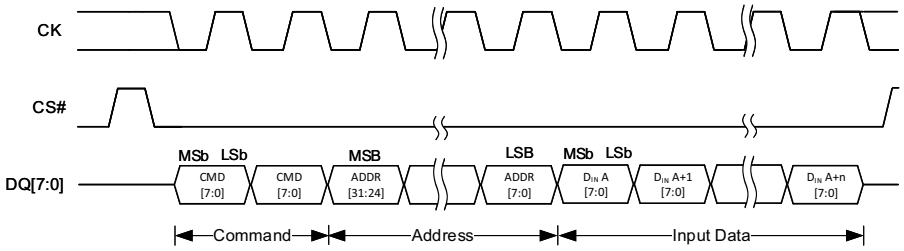


Figure 21. Octal DDR Program Transaction with Command, Address, and Data Input[2]

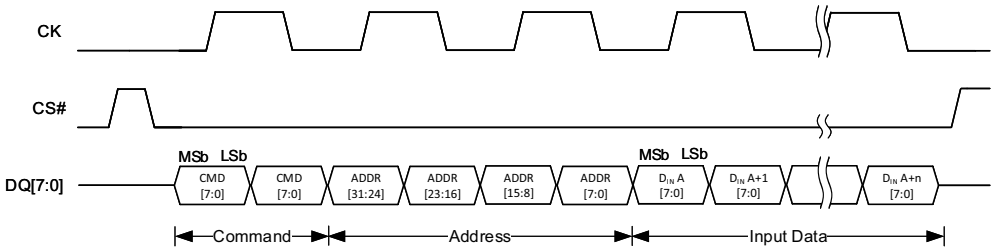


Figure 22. Octal DDR Program Transaction with Command, Address, and Single Byte Data Input[2]

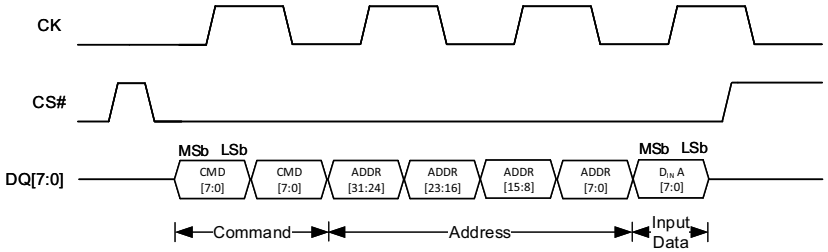
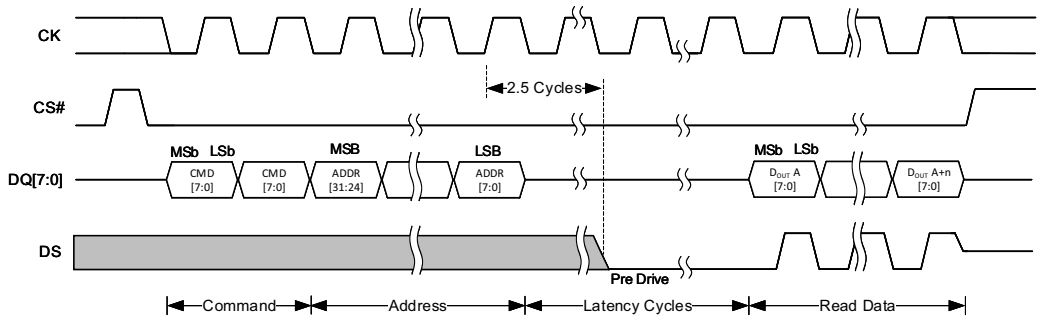


Figure 23. Octal SDR Read Transaction with Command and Address Input (Output Latency)



Note

2. The LSb of the address always be zero in any Octal DDR transactions with the address input.

Figure 24. Octal DDR Read Transaction with Command and Address Input (Output Latency)[3, 4]

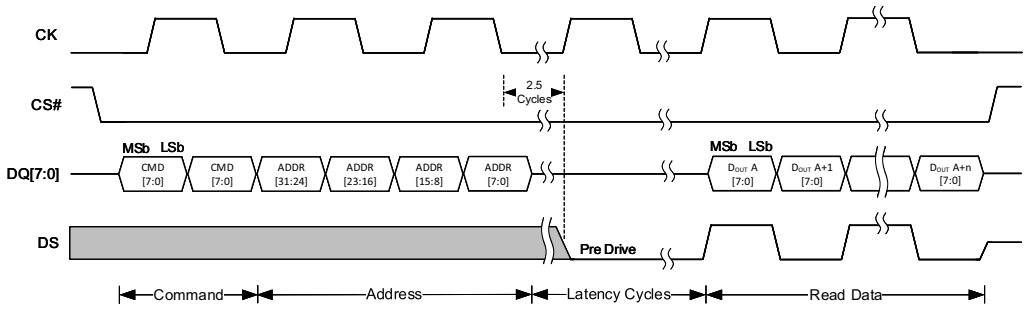


Figure 25. Octal DDR Single Byte Read Transaction with Command and Address Input (Output Latency)[5]

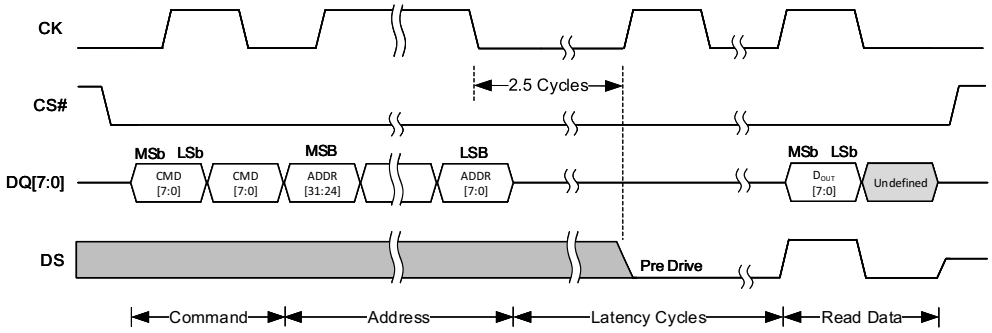
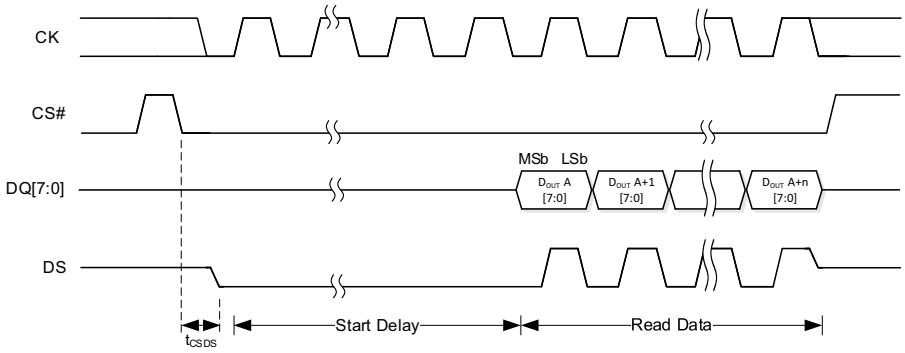
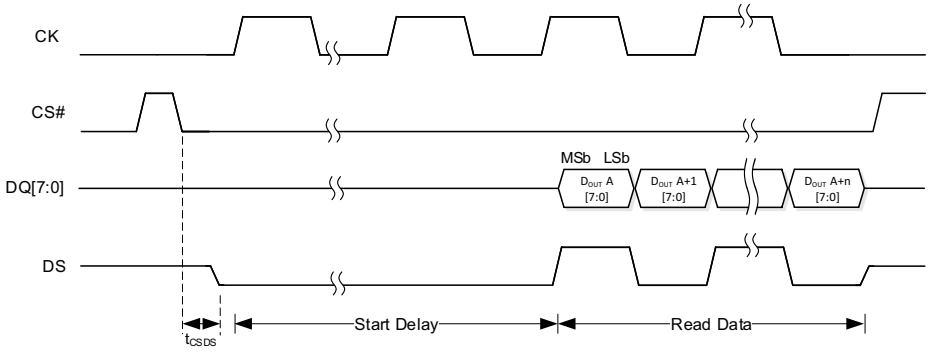


Figure 26. Octal SDR Transaction with Output Data Sequence (AutoBoot)



Notes
3. The LSb of the address always be zero in any Octal DDR transactions with the address input.
4. Read Interface CRC Transaction is supported with Octal DDR only.
5. The LSb of the address always be zero in any Octal DDR transactions with the address input.

Figure 27. Octal DDR Transaction with Output Data Sequence (AutoBoot)



1.1.4 Register Naming Convention

Figure 28. Register Naming Convention

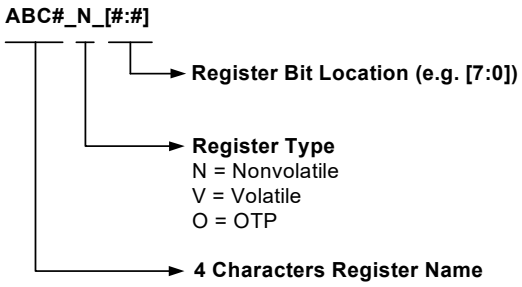
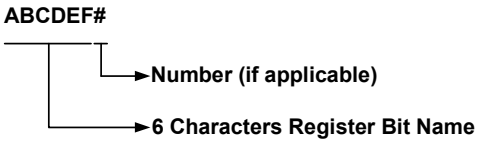
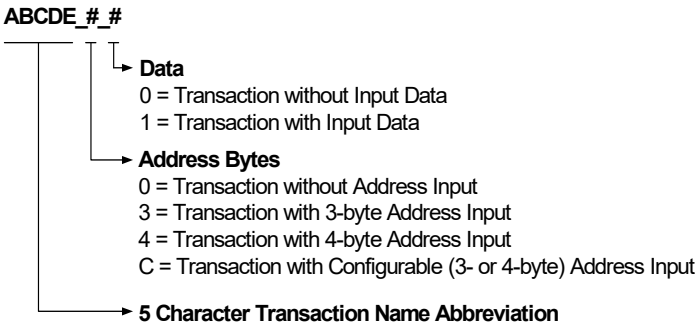


Figure 29. Register Bit Naming Convention



1.1.5 Transaction Naming Convention

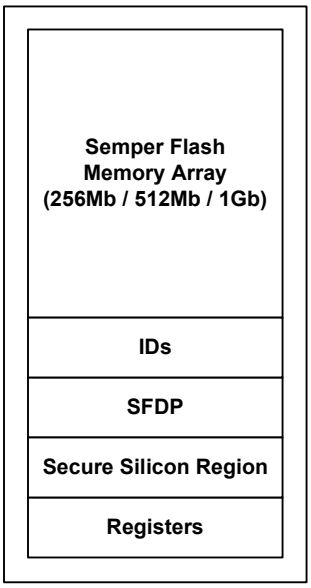
Figure 30. Transaction Naming Convention



1.2 Address Space Maps

The HL-T/HS-T family supports 32-bit (4-Byte) addresses only to enable 256 Mb or 512 Mb or 1 Gb density devices. 4-Byte addresses allow direct addressing of up to 4 GB (32 Gb) address space. Besides Flash memory array, HL-T/HS-T family includes separate address spaces for Manufacturer ID, Device ID, Unique ID, Serial Flash Discoverable Parameters (SFDP), Secure Silicon Region (SSR), and Registers.

Figure 31. HL-T/HS-T Address Space Map Overview



1.2.1 Semper Flash Memory Array

The main flash array is divided into units called physical sectors.

The HL-T/HS-T family sector architecture supports the following options:

- 256 Mb, 512 Mb, 1 Gb supports 256 KB Uniform sector options
- 256 Mb, 512 Mb, 1 Gb Hybrid sector options
  - Physical set of thirty-two 4 KB sectors and one 128 KB sector at the top or bottom of address space with all remaining sectors of 256 KB
  - Physical set of sixteen 4 KB sectors and one 192 KB sector at both the top and bottom of the address space with all remaining sectors of 256 KB

The combination of the sector architecture selection bits in Configuration Register-1 and Configuration Register-3 support the different sector architecture options of the HL-T/HS-T family. See Section 1.3 Registers on page 21 for more information.

Table 1. 256 KB Uniform Sector Address Map[6]

Sector Size (KB)	S28HL01GT and S28HS01GT			S28HL512T and S28HS512T			S28HL256T and S28HS256T		
	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)
256	512	SA00	00000000h-0003FFFFh	256	SA00	00000000h-0003FFFFh	128	SA00	00000000h-0003FFFFh
		:	:		:	:		:	:
		SA511	07FC0000h-07FFFFFFh		SA255	03FC0000h-03FFFFFFh		SA127	01FC0000h-01FFFFFFh

Note
6. Configuration: CFR3N[3] = 1.

Table 2. Bottom Hybrid Configuration 1 Thirty-two 4 KB Sectors and 256 KB Uniform Sectors Address Map[7]

Sector Size (KB)	S28HL01GT and S28HS01GT			S28HL512T and S28HS512T			S28HL256T and S28HS256T		
	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)
4	32	SA00	00000000h-00000FFFh	32	SA00	00000000h-00000FFFh	32	SA00	00000000h-00000FFFh
		:	:		:	:		:	:
		SA31	0001F000h-0001FFFFh		SA31	0001F000h-0001FFFFh		SA31	0001F000h-0001FFFFh
128	1	SA32	00020000h-0003FFFFh	1	SA32	00020000h-0003FFFFh	1	SA32	00020000h-0003FFFFh
256	511	SA33	00040000h-0007FFFFh	255	SA33	00040000h-0007FFFFh	127	SA33	00040000h-0007FFFFh
		:	:		:	:		:	:
		SA543	07FC0000h-07FFFFFFh		SA287	03FC0000h-03FFFFFFh		SA159	01FC0000h-01FFFFFFh

Note
7. Configuration: CFR3N[3] = 0, CFR1N[6] = 0, CFR1N[2] = 0.

Table 3. Top Hybrid Configuration 1 Thirty-two 4 KB Sectors and 256 KB Uniform Sectors Address Map[8]

Sector Size (KB)	S28HL01GT and S28HS01GT			S28HL512T and S28HS512T			S28HL256T and S28HS256T		
	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)
256	511	SA00	00000000h-0003FFFFh	255	SA00	00000000h-0003FFFFh	127	SA00	00000000h-0003FFFFh
		:	:		:	:		:	:
		SA510	07F80000h-07FBFFFFh		SA254	03F80000h-03FBFFFFh		SA126	01F80000h-01FBFFFFh
128	1	SA511	07FC0000h-07FDFFFFh	1	SA255	03FC0000h-03FDFFFFh	1	SA127	01FC0000h-01FDFFFFh
4	32	SA512	07FE0000h-07FE0FFFh	32	SA256	03FE0000h-03FE0FFFh	32	SA128	01FE0000h-01FE0FFFh
		:	:		:	:		:	:
		SA543	07FFF000h-07FFFFFFh		SA287	03FFF000h-03FFFFFFh		SA159	01FFF000h-01FFFFFFh

Note
8. Configuration: CFR3N[3] = 0, CFR1N[6] = 0, CFR1N[2] = 1.

Table 4. Hybrid Configuration 2 Bottom Sixteen and Top Sixteen 4 KB Sectors Address Map[9]

Sector Size (KB)	S28HL01GT and S28HS01GT			S28HL512T and S28HS512T			S28HL256T and S28HS256T		
	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)	Sector Count	Sector Range	Byte Address Range (Sector Starting Address - Sector Ending Address)	Sector Count	Sector Range	
4	16	SA00	00000000h-00000FFFh	16	SA00	00000000h-00000FFFh	16	SA00	00000000h-00000FFFh
		:	:		:	:		:	:
		SA15	0000F000h-0000FFFFh		SA15	0000F000h-0000FFFFh		SA15	0000F000h-0000FFFFh
192	1	SA16	00010000h-0003FFFFh	1	SA16	00010000h-0003FFFFh	1	SA16	00010000h-0003FFFFh
256	510	SA17	00040000h-0007FFFFh	254	SA17	00040000h-0007FFFFh	126	SA17	00040000h-0007FFFFh
		:	:		:	:		:	:
		SA526	07F80000h-07FBFFFFh		SA270	03F80000h-03FBFFFFh		SA142	01F80000h-01FBFFFFh
192	1	SA527	07FC0000h-07FEFFFFh	1	SA271	03FC0000h-03FEFFFFh	1	SA143	01FC0000h-01FEFFFFh
4	16	SA528	07FF0000h-07FF0FFFh	16	SA272	03FF0000h-03FF0FFFh	16	SA144	01FF0000h-01FF0FFFh
		:	:		:	:		:	:
		SA543	07FFF000h-07FFFFFFh		SA287	03FFF000h-03FFFFFFh		SA159	01FFF000h-01FFFFFFh

Note
9. Configuration: CFR3N[3] = 0, CFR1N[6] = 1.

These are condensed tables that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 4 KB sectors have the pattern xxxxx000h-xxxxxFFFh. All 256 KB sectors have the pattern xxx00000h-xxx3FFFFh, xxx40000h-xxx7FFFFh, xx80000h-xxxCFFFFh, or xxD0000h-xxxFFFFFh.

1.2.2 ID Address Space

This particular region of the memory is assigned to manufacturer, device, and unique identification:

- The manufacturer identification is assigned by JEDEC.
- The device identification is assigned by Cypress.
- A 64-bit unique number is located in 8 bytes of the Unique Device ID address space. This Unique ID can be used as a software readable serial number that is unique for each device.

There is no address space defined for these IDs as they can be read by providing the respective transactions only. The transactions do not need the address to read these IDs. The data in this address space is read-only data.

1.2.3 JEDEC JESD216 Serial Flash Discoverable Parameters (SFDP) Space

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of this serial flash device in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features. The SFDP address space has a header starting at address zero that identifies the SFDP data structure and provides a pointer to each parameter. The SFDP address space is programmed by Cypress and read-only for the host system.

Table 5. SFDP Overview Address Map

Byte Address	Description
0000h	Location zero within JEDEC JESD216C SFDP space - start of SFDP header
,,,	Remainder of SFDP header followed by undefined space
0100h	Start of SFDP parameter tables The SFDP parameter table data starting at 0100h
...	Remainder of SFDP parameter tables followed by either more parameters or undefined space

1.2.4 Secure Silicon Region (SSR) Address Space

Each HS/L-T family memory device has a 1024-byte Secure Silicon Region which is OTP address space. This address space is separate from the main flash array. The SSR area is divided into 32 individually lockable, 32-byte aligned and length regions.

In the 32-byte region starting at address zero:

- The sixteen lowest bytes contain a 128-bit random number. The random number cannot be written to, erased or programmed and any attempts will return an PRGERR flag.
- The next four bytes are used to provide one bit per secure region (32 bits in total) to permanently protect once set to “0” from writing, erasing or programming.
- All other bytes are reserved.

The remaining regions are erased when shipped from Cypress, and are available for programming of additional permanent data.

Table 6. SSR Address Map

Region	Byte Address Range	Contents	Initial Delivery State
Region 0	000h	LSB of Cypress Programmed Random Number	Cypress Programmed Random Number
	...	...	
	00Fh	MSB of Cypress Programmed Random Number	
	010h to 013h	Region Locking Bits Byte 10h [bit 0] locks region 0 from programming when = 0 ... Byte 13h [bit 7] locks region 31 from programming when = 0	All Bytes = FFh
	014h to 01Fh	Reserved for Future Use (RFU)	
Region 1	020h to 03Fh	Available for User Programming	
Region 2	040h to 05Fh		
...	...		
Region 31	3E0h to 3FFh		

1.2.5 Registers

Registers are small groups of memory cells used to configure how the HS/L-T family memory device operates, or to report the status of device operations. The registers are accessed by specific commands and addresses. Table 7 shows the address map for every available register in this flash memory device.

Table 7. Register Address Map

Function	Register Type	Register Name	Volatile Component Address (hex)	Nonvolatile Component Address (hex)
Device Status	Status Register 1	STR1N[7:0], STR1V[7:0]	0x00800000	0x00000000
	Status Register 2	STR2V[7:0]	0x00800001	N/A
Device Configuration	Configuration Register 1	CFR1N[7:0], CFR1V[7:0]	0x00800002	0x00000002
	Configuration Register 2	CFR2N[7:0], CFR2V[7:0]	0x00800003	0x00000003
	Configuration Register 3	CFR3N[7:0], CFR3V[7:0]	0x00800004	0x00000004
	Configuration Register 4	CFR4N[7:0], CFR4V[7:0]	0x00800005	0x00000005
	Configuration Register 5	CFR5N[7:0], CFR5V[7:0]	0x00800006	0x00000006
Interface CRC	Interface CRC Enable Register	ICEV[7:0]	0x00800008	N/A
EnduraFlex Architecture	EnduraFlex Architecture Selection Register 0 [1:0]	EFX0O[7:0]	N/A	0x00000050
	EnduraFlex Architecture Selection Register 1 [7:0]	EFX1O[7:0]		0x00000052
	EnduraFlex Architecture Selection Register 1 [10:8]	EFX1O[10:8]		0x00000053
	EnduraFlex Architecture Selection Register 2 [7:0]	EFX2O[7:0]		0x00000054
	EnduraFlex Architecture Selection Register 2 [10:8]	EFX2O[10:8]		0x00000055
	EnduraFlex Architecture Selection Register 3 [7:0]	EFX3O[7:0]		0x00000056
	EnduraFlex Architecture Selection Register 3 [10:8]	EFX3O[10:8]		0x00000057
	EnduraFlex Architecture Selection Register 4 [7:0]	EFX4O[7:0]		0x00000058
	EnduraFlex Architecture Selection Register 4 [10:8]	EFX4O[10:8]		0x00000059
Interrupt Pin	Interrupt Configuration Register	INCV[7:0]	0x00800068	N/A
	Interrupt Status Register	INSV[7:0]	0x00800067	
Error Correction	ECC Status Register	ESCV[7:0]	0x00800089	
	ECC Error Detection Count Register [7:0]	ECTV[7:0]	0x0080008A	
	ECC Error Detection Count Register [15:8]	ECTV[15:8]	0x0080008B	
	ECC Address Trap Register [7:0]	EATV[7:0]	0x0080008E	
	ECC Address Trap Register [15:8]	EATV[15:8]	0x0080008F	
	ECC Address Trap Register [23:16]	EATV[23:16]	0x00800040	
	ECC Address Trap Register [31:24]	EATV[31:24]	0x00800041	
AutoBoot	AutoBoot Register [7:0]	ATBN[7:0]	N/A	0x00000042
	AutoBoot Register [15:8]	ATBN[15:8]		0x00000043
	AutoBoot Register [23:16]	ATBN[23:16]		0x00000044
	AutoBoot Register [31:24]	ATBN[31:24]		0x00000045
Erase Count	Sector Erase Count Register [7:0]	SECV[7:0]	0x00800091	N/A
	Sector Erase Count Register [15:8]	SECV[15:8]	0x00800092	
	Sector Erase Count Register [23:16]	SECV[23:16]	0x00800093	
Data Integrity Check	Data Integrity Check CRC Register [7:0]	DCRV[7:0]	0x00800095	
	Data Integrity Check CRC Register [15:8]	DCRV[15:8]	0x00800096	
	Data Integrity Check CRC Register [23:16]	DCRV[23:16]	0x00800097	
	Data Integrity Check CRC Register [31:24]	DCRV[31:24]	0x00800098	

Table 7. Register Address Map (Continued)

Function	Register Type	Register Name	Volatile Component Address (hex)	Nonvolatile Component Address (hex)
Protection and Security	Advanced Sector Protection Register [7:0]	ASPO[7:0]	N/A	0x00000030
	Advanced Sector Protection Register [15:8]	ASPO[15:8]		0x00000031
	ASP PPB Lock Register (Persistent Protection Block)	PPLV[7:0]	0x0080009B	N/A
	ASP Password Register [7:0]	PWDO[7:0]	N/A	0x00000020
	ASP Password Register [15:8]	PWDO[15:8]		0x00000021
	ASP Password Register [23:16]	PWDO[23:16]		0x00000022
	ASP Password Register [31:24]	PWDO[31:24]		0x00000023
	ASP Password Register [39:32]	PWDO[39:32]		0x00000024
	ASP Password Register [47:40]	PWDO[47:40]		0x00000025
	ASP Password Register [55:48]	PWDO[55:48]		0x00000026
	ASP Password Register [63:56]	PWDO[63:56]		0x00000027

1.3 Registers

Registers are small groups of storage cells used to configure as well as report the status of the device operations. HL-T/HS-T family of devices use separate nonvolatile and volatile storage groups to implement the different register bit types for legacy compatibility as well as new functionality. Each register is organized as a group of volatile bits with associated nonvolatile bits (if permanence is required). During power-up, hardware reset or software reset, the data in the nonvolatile bits of the register is transferred to the volatile bits to provide the default state of the volatile bits. When writing new data to nonvolatile bits of the register, the volatile bits are also updated with the new data. However, when writing new data to the volatile register bits the nonvolatile bits retain the old data. The register structure is shown in Figure 32.

Figure 32. Register Structure

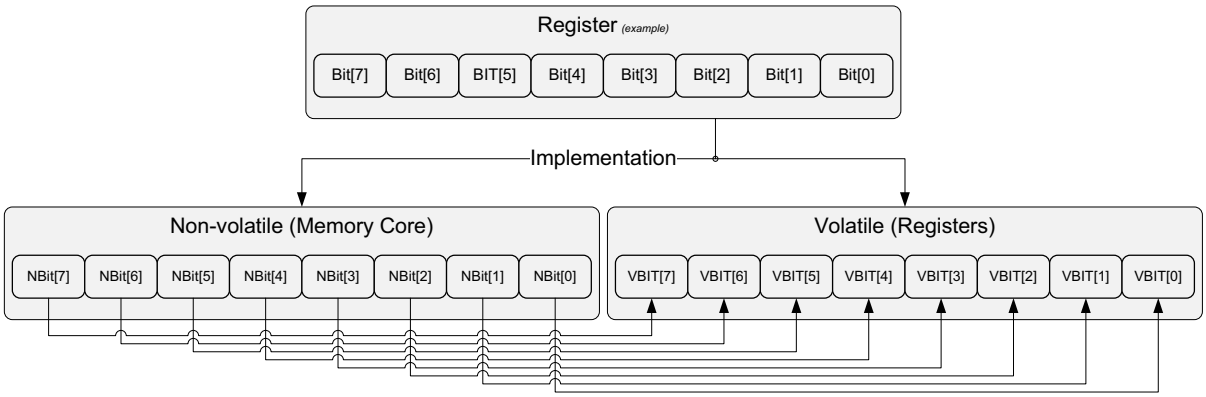
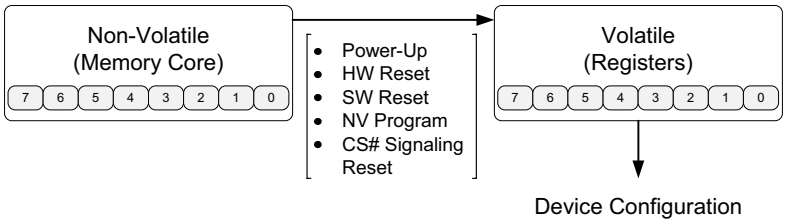


Figure 33. Data Movement Within Register Components



1.3.1 Register Naming Convention

Table 8. Register Bit Description Convention

Bit Number	Name	Function	Read/Write	Factory Default (binary)	Description
REGNAME#T[x] T = N, V, O Descending Order	–	–	Possible Options: N/A - Not Applicable R - Readable Only R/W - Readable and Writable R/1 - Readable and OTP	Possible Options: 0 1	Format: Description of the Configuration bit 0 = Option ‘0’ selection of the Bit 1 = Option '1' selection of the Bit Dependency: Is this Bit part of a function which requires multiple bits for implementation?

1.3.2 Status Register 1 (STR1x)

Status Register 1 contains both status and control bits. The functionality of supported Status Register 1 type is described in Table 9.

Table 9. Status Register 1[10]

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
STR1N[7] STR1V[7]	RESRVD	Reserved for Future Use	N->R V->R	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
STR1V[6]	PRGERR	Programming Error Status Flag	V -> R	0	Description: The PRGERR bit indicates program operation success or failure. When the PRGERR bit is set to a '1', it indicates that there was an error in the last programming operation. PRGERR bit is also set when a program operation is attempted within a protected memory region. When PRGERR is set, it can only be cleared with the Clear Program and Erase Failure Flags (CLPEF_0_0) transaction or a hardware/software reset. **Note** The device will only go to standby mode once the PRGERR flag is cleared. Selection Options: 0 = Last programming operation was successful 1 = Last programming operation was unsuccessful Dependency: N/A
STR1V[5]	ERSERR	Erasing Error Status Flag	V -> R	0	Description: The ERSERR bit indicates erase operation success or failure. When the ERSERR bit is set to a '1', it indicates that there was an error in the last erasing operation. ERSERR bit is also set when a erase operation is attempted within a protected memory sector. When ERSERR is set, it can only be cleared with the Clear Program and Erase Failure Flags (CLPEF_0_0) transaction or a hardware/software reset. **Note** The device will only go to standby mode once the ERSERR flag is cleared. Selection Options: 0 = Last erase operation was successful 1 = Last erase operation was unsuccessful Dependency: N/A
STR1N[4:2] STR1V[4:2]	LBPROT[2:0]	Legacy Block Protection based Memory Array size selection	If PLPROT = 0 N -> R/W V -> R/W If PLPROT = 1 N -> R V -> R	000	Description: The LBPROT[2:0] bits define the memory array size to be protected against program and erase transactions. Based on the LBPROT[2:0] configuration, either top 1/64, 1/4, 1/2, etc. or bottom 1/64, 1/4, 1/2, etc., or up to the entire array is protected. **Note** If PLPROT bit - Permanent Locking selection of Legacy Block Protection and 4 KB Sector Architecture (CFR1x[4]) is set to a '1', the LBPROT[2:0] bits cannot be erased or programmed. Selection Options: 000 = Protection is disabled 001 = 1/64th of the (top/bottom) array protection is enabled 010 = 1/32nd of the (top/bottom) array protection is enabled ….. 111 = All sectors are protected Dependency: TBPROT (CFR1x[5])
STR1V[1]	WRPGEN	Write/Program Enable Status Flag	V -> R	0	Description: The WRPGEN bit must be set to '1' to enable all program, erase or register write operations - it provides protection against inadvertent changes to memory or register values. The Write Enable (WRENB_0_0) transaction set the WRPGEN bit to '1' to allow program, erase or write transactions to execute. The Write Disable (WRDIS_0_0) transaction resets WRPGEN to a '0' to prevent all program, erase, and write transactions from execution. The WRPGEN bit is cleared to '0' at the end of any successful program, erase or register write operation. After a power down / power up sequence or a hardware/software reset, the Deep Power Down WRPGEN bit is cleared to '0'. Selection Options: 0 = Program, erase or register write is disabled 1 = Program, erase or register write is enabled Dependency: N/A

Note
10. STR1x value during POR, Hardware Reset, Software Reset, DPD Exit, and CS# Signaling Reset is not valid.

Table 9. Status Register 1[10] (Continued)

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
STR1V[0]	RDYBSY	Device Ready/Busy Status Flag	V -> R	0	Description: The RDYBSY bit indicates whether the device is performing an embedded operation or is in standby mode ready to receive new transactions. **Note** The PRGERR and ERSERR status bits are updated while RDYBSY is set. If PRGERR or ERSERR are set, the RDYBSY bit will remain set indicating the device is busy and unable to receive new transactions. A Clear Program and Erase Failure Flags (CLPEF_0_0) transaction must be executed to return the device to standby mode. Selection Options: 0 = Device is in standby mode ready to receive new operation transactions 1 = Device is busy and unable to receive new operation transactions Dependency: N/A

Note
10. STR1x value during POR, Hardware Reset, Software Reset, DPD Exit, and CS# Signaling Reset is not valid.

Table 10. PRGERR Summary

Error Flag	Symbol	Conditions
Program Error	PRGERR	Bits cannot be programmed '1' to '0'
		Trying to program in a protected region
		If ASP0[2] or ASP0[1] is 0, any nonvolatile register write attempting to change the value of CFR1N[6:2]/CFR1V[6:2]
		After the Password Protection Mode is selected and ASP Password Register update transaction executed
		SafeBoot Failure
		Configuration Failure

Table 11. ERSERR Summary

Error Flag	Symbol	Conditions
Erase Error	ERSERR	Sector Device Erase - All bits cannot be erased to '1's
		Trying to erase a protected region
		Register Erase - All bits cannot be erased to '1's during Erase portion of Register Write
		SafeBoot Failure

1.3.3 Status Register 2 (STR2x)

Status Register 2 provides device status on operations. The functionality of supported Status Register 2 type is described in Table 12.

Table 12. Status Register 2[11]

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
STR2V[7:5]	RESRVD	Reserved for Future Use	V -> R	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
STR2V[4]	DICRCS	Memory Array Data Integrity Cyclic Redundancy Check Suspend Status Flag	V -> R	0	Description: The DICRCS bit is used to determine when the device is in Memory Array Data Integrity Cyclic Redundancy Check suspend mode. Selection Options: 0 = Memory Array Data Integrity Cyclic Redundancy Check is not in suspend mode 1 = Memory Array Data Integrity Cyclic Redundancy Check is in suspend mode Dependency: N/A
STR2V[3]	DICRCA	Memory Array Data Integrity Cyclic Redundancy Check Abort Status Flag	V -> R	0	Description: The DICRCA bit indicates that the Memory Array Data Integrity CRC calculation operation was aborted. The abort condition is based on ending address (ENDADD) and starting address (STRADD) relationship. If ENDADD < STRADD + 3, then DICRCA will be set and the device will return to the Standby state. DICRCA flag gets cleared at the next Data Integrity CRC calculation operation when ENDADD ≥ STRADD + 3. Selection Options: 0 = Memory Array Data Integrity CRC calculation Is not aborted 1 = Memory Array Data Integrity CRC calculation is aborted Dependency: N/A
STR2V[2]	SESTAT	Sector Erase Success/Failure Status Flag	V -> R	0	Description: The SESTAT bit indicates whether the erase operation on the sector completed successfully. Evaluate Erase Status transaction (EVERS_4_0) must be executed prior to reading SESTAT bit which specifies the sector address. Selection Options: 1 = Addressed sector (EVERS_4_0) was erased successfully 0 = Addressed sector (EVERS_4_0) was not erased successfully Dependency: N/A
STR2V[1]	ERASES	Erase operation Suspend Status Flag	V -> R	0	Description: The ERASES bit is used to indicate if the Erase operation is suspended. Selection Options: 0 = Erase operation is not in suspend mode 1 = Erase operation is in suspend mode Dependency: N/A
STR2V[0]	PROGMS	Program operation Suspend Status Flag	V -> R	0	Description: The PROGMS bit is used to indicate if the Program operation is suspended. Selection Options: 0 = Program operation is not in suspend mode 1 = Program operation is in suspend mode Dependency: N/A

Note

11. STR2x value during POR, Hardware Reset, Software Reset, DPD Exit, and CS# Signaling Reset is not valid. STR2x bits are valid only when STR1V[0] / RDYBSY = 0.

1.3.4 Configuration Register 1 (CFR1x)

Configuration Register 1 controls interface and data protection functions.

Table 13. Configuration Register 1

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
CFR1N[7] CFR1V[7]	RESRVD	Reserved for Future Use	N -> R/W V -> R/W	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
CFR1N[6] CFR1V[6]	SP4KBS	Split 4 KB Sectors selection between top and bottom address space	If PLPROT = 0 N -> R/W V -> R If PLPROT = 1 N -> R V -> R	0	Description: The SP4KBS bit selects whether the 4 KB sectors are grouped together or evenly split between High and LOW address ranges. Selection Options: 0 = 4 KB Sectors are grouped together 1 = 4 KB Sectors are split between High and Low Addresses Dependency: TB4KBS(CFR1N[2])
CFR1N[5] CFR1V[5]	TBPROT	Top or Bottom Protection selection for Legacy Protection Mode	If PLPROT = 0 N -> R/W V -> R If PLPROT = 1 N -> R V -> R	0	Description: The TBPROT bit selects the reference point of the Legacy Block Protection bits (LBPROT[2:0]) in the Status Register on whether the protection starts from the top or starts from the bottom of the address range. The bit also selects a memory address range (lowest or highest) to remain readable is available for reading during Read Password Protection mode even before a successful Password entry is completed. Selection Options: 0 = Legacy Protection is applicable in the top half of the address range 1 = Legacy Protection is applicable in the bottom half of the address range Dependency: LBPROT[2:0] (STR1x[3:1])
CFR1N[4] CFR1V[4]	PLPROT	Permanent Locking selection of Legacy Block Protection and 4 KB Sector Architecture	N -> R/1 V -> R	0	Description: The PLPROT bit permanently protects the Legacy Block Protection and 4 KB Sector location. It thereby permanently protects the memory array protection scheme and sector architecture. **Note** PLPROT protects LBPROT[2:0], SP4KBS, TBPROT, and TB4KBS bits from program and erase, and it is recommended to configure these bits before configuring the PLPROT bit. Selection Options: 0 = Legacy Block Protection and 4 KB Sector Location are not protected 1 = Legacy Block Protection and 4 KB Sector Location are protected Dependency: N/A
CFR1N[3] CFR1V[3]	RESRVD	Reserved for Future Use	N -> R/W V -> R/W	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
CFR1N[2] CFR1V[2]	TB4KBS	Top or Bottom Address Range selection for 4 KB Sector Block	If PLPROT = 0 N -> R/W V -> R If PLPROT = 1 N -> R V -> R	0	Description: The TB4KBP bit defines the logical address location of the 4 KB sector block. The 4 KB sector block replaces the fitting portion of the highest or lowest address sector. Selection Options: 0 = 4 KB Sector Block is in the bottom of the memory address space 1 = 4 KB Sector Block is in the top of the memory address space Dependency: SP4KBS (CFR1x[6])
CFR1N[1] CFR1V[1]	RESRVD	Reserved for Future Use	N -> R/W V -> R/W	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
CFR1N[0] CFR1V[0]	TLPROT	Temporary Locking selection of Legacy Block Protection and Sector Architecture	N -> R V -> R/W	0	Description: The TLPROT bit temporarily protects the Legacy Block Protection and 4 KB Sector location. Upon power-up or a hardware reset, TLPROT is set to its default state. When selected, it protects the memory array protection scheme and sector architecture from any changes. **Note** TLPROT protects LBPROT[2:0], SP4KBS, TBPROT, and TB4KBS bits from program and erase. Selection Options: 0 = Legacy Block Protection and 4 KB Sector Location are not protected 1 = Legacy Block Protection and 4 KB Sector Location are temporarily protected Dependency: N/A

Table 14. 4 KB Parameter Sector Location Selection

SP4KBS	TB4KBS	4 KB Location
0	0	4 KB physical sectors at bottom (Low address)
0	1	4 KB physical sectors at top, (High address)
1	X	4 KB Parameter sectors are split between top (High Address) and bottom (Low Address)

Table 15. PLPROT and TLPROT Protection

PLPROT	TLPROT	Array Protection and 4K Sector
0	0	Unprotected (Unlocked)
1	X	TBPROT, LBPROTx, SP4KBS, TB4KBS - Permanently Protected (Locked)
0	1	TBPROT, LBPROTx, SP4KBS, TB4KBS - Protected (Locked) till next Power-down

1.3.5 Configuration Register 2 (CFR2x)

Configuration Register 2 controls memory read latency and address byte length selection.

Table 16. Configuration Register 2

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
CFR2N[7] CFR2V[7]	ADRBYT	Address Byte Length selection between 3 or 4 bytes for Instructions	N -> R/W V -> R/W	0	Description: The ADRBYT bit controls the expected address length for all instructions that require address and is selectable between 3 Bytes or 4 Bytes. Selection Options: 0 = Instructions will use 3 Bytes for address 1 = Instructions will use 4 Bytes for address Dependency: N/A
CFR2N[6:4] CFR2V[6:4]	RESRVD	Reserved for Future Use	N -> R/W V -> R/W	0000	These bits are Reserved for future use. This bit must always be written/loaded to its default state.
CFR2N[3:0] CFR2V[3:0]	MEMLAT[3:0]	Memory Array Read Latency selection - Dummy cycles required for initial data access	N -> R/W V -> R/W	1000	Description: The MEMLAT[3:0] bits control the read latency (dummy cycles) delay in all variable latency memory array and nonvolatile register read transactions. MEMLAT selection allows the user to adjust the read latency during normal operation based on different operating frequencies. Selection Options: 0000 = 0/5 Latency Cycles Selection based on transaction opcodes ….. 1111 = 15/28 Latency Cycles Selection based on transaction opcodes Dependency: N/A

Table 17. Latency Code (Cycles) Versus Frequency[12, 13, 15]

Latency Code	Number of Cycles (1-1-1 / 8-8-8)	SDR SPI Read Transactions (MHz) (1S-1S-1S)	SDR Octal Read Transactions (MHz) (8S-8S-8S)	DDR Octal Read Transactions (MHz) (8D-8D-8D)
		RDAY2_C_0 RDSSR_4_0 RDARG_C_0[14] RDECC_4_0 RDPPB_4_0	RDAY1_4_0 RDSSR_4_0 RDARG_4_0[14] RDECC_4_0 RDPPB_4_0	RDAY2_4_0 RDSSR_4_0 RDARG_4_0[14] RDECC_4_0 RDPPB_4_0
0000	0 / 5	50	50	42
0001	1 / 6	68	64	57
0010	2 / 8	81	92	85
0011	3 / 10	93	121	107
0100	4 / 12	106	150	121
0101	5 / 14	118	166 (HL-T) / 178 (HS-T)	135
0110	6 / 16	131	200	150
0111	7 / 18	143	200	164
1000	8 / 20	156	200	166 (HL-T) / 178 (HS-T)
1001	9 / 22	166	200	192
1010	10 / 23	166	200	200
1011	11 / 24	166	200	200
1100	12 / 25	166	200	200
1101	13 / 26	166	200	200
1110	14 / 27	166	200	200
1111	15 / 28	166	200	200

Notes

12. When using the ECC error reporting mechanisms, the read output data must be at least 2 bytes for correct ECC reporting.
13. CK frequency > 200 MHz SDR, or > 200 MHz DDR is not supported by HS-T family of devices and CK frequency > 166 MHz SDR, or > 166 MHz DDR is not supported by HL-T family of devices.
14. RDARG_C_0 and RDARG_4_0 uses these latency cycles for reading nonvolatile registers.
15. RSFDP_3_0 always have a dummy cycle of eight and the maximum frequencies for different interfaces related to eight dummy cycles.

1.3.6 Configuration Register 3 (CFR3x)

Configuration Register 3 controls transaction behavior.

Table 18. Configuration Register 3

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
CFR3N[7:6] CFR3V[7:6]	VRGLAT[1:0]	Volatile Register Read Latency selection - Dummy cycles required for initial data access	N -> R/W V -> R/W	00	Description: The VRGLAT[1:0] bits control the read latency (dummy cycles) delay in all variable latency register read transactions. VRGLAT[1:0] selection allows the user to adjust the read latency during normal operation based on different operating frequencies. Selection Options: 00 = 0/0/32 Latency Cycles Selection based on transaction opcodes ..... 11 = 2/2/32 Latency Cycles Selection based on transaction opcodes Dependency: N/A
CFR3N[5] CFR3V[5]	BLKCHK	Blank Check selection during Erase operation for better endurance	N -> R/W V -> R/W	0	Description: When this feature is enabled an erase transaction first evaluates the erase status of the sector. If the sector is found to erased, the erase operation is aborted. In other words, the erase operation is only executed if programmed bits are found in the sector. Disabling BLKCHK executes an erase operation unconditionally. Selection Options: 0 = Blank Check is disabled before executing an erase operation 1 = Blank Check evaluation is enabled before executing an erase operation Dependency: N/A
CFR3N[4] CFR3V[4]	PGMBUF	Program Buffer Size selection	N -> R/W V -> R/W	0	Description: The PGMBUF bit selects the Programming Buffer size which is used for page programming. Program buffer size affects the device programming time. **Note** If programming data exceeds the program buffer size, data gets wrapped. Selection Options: 0 = 256 Byte Write Buffer Size 1 = 512 Byte Write Buffer Size Dependency: N/A
CFR3N[3] CFR3V[3]	UNHYSA	Uniform or Hybrid Sector Architecture selection	N -> R/W V -> R	0	Description: The UNHYSA bit selects between uniform (all 256 KB sectors) or hybrid (4 KB sectors and 256 KB sectors) sector architecture. If hybrid sector architecture is selected, 4 KB sector block is made part of the main Flash array address map. The 4 KB sector block can overlay at either the highest or the lowest address range of the device. If uniform sector architecture is selected, 4 KB sector block is removed from the address map and all sectors are of uniform size. **Note** Hybrid sector architecture also enables 4 KB Sector Erase transaction (20h). Otherwise, 4 KB Sector Erase transaction, if issued, is ignored by the device. Selection Options: 0 = Hybrid Sector Architecture (combination of 4 KB sectors and 256 KB sectors) 1 = Uniform Sector Architecture (all 256 KB sectors) Dependency: ST4KBP(CFR1N[6]), TB4KBP(CFR1N[2])
CFR3N[2] CFR3V[2]	RESRVD	Reserved for Future Use	N -> R/W V -> R/W	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
CFR3N[1] CFR3V[1]	RESRVD	Reserved for Future Use	N -> R/W V -> R/W	0	
CFR3N[0] CFR3V[0]	RESRVD	Reserved for Future Use	N -> R/W V -> R/W	0	

Table 19. Register Latency Code (Cycles) Versus Frequency[17, 19]

Latency Code	SDR SPI Register Transaction Latency Dummy Cycles (1S-1S-1S)[16]			SDR Octal Register Transactions Latency Dummy Cycle (8S-8S-8S)		DDR Octal Register Transactions Latency Dummy Cycle (8D-8D-D8)	
	Frequency	RDARG_C_0[18] RDDYB_4_0	RDPLB_0_0 RDIDN_0_0 RDSR1_0_0 RDSR2_0_0	Frequency	RDARG_4_0[18] RDPLB_0_0 RDDYB_4_0 RDIDN_0_0 RDSR1_0_0 RDSR2_0_0	Frequency	RDARG_4_0[18] RDPLB_0_0 RDDYB_4_0 RDIDN_0_0 RDSR1_0_0 RDSR2_0_0
00	50 MHz	0	0	50 MHz	3	25 MHz	3
01	133 MHz	1	0	133 MHz	4	66 MHz	4
10	133 MHz	1	1	166 MHz	5	166 MHz (HL-T) / 200 MHz (HS-T)	5
11	166 MHz	2	2	200 MHz	6	200 MHz	6

Notes
16. CK frequency > 166 MHz SDR, is not supported.
17. RDUID_4_0 alway has 32 cycles of latency. Maximum frequency under SDR SPI is 166 MHz, under HS-T SDR/DDR Octal is 200 MHz and under HL-T SDR/DDR Octal is 166 MHz.
18. RDARG_C_0 and RDARG_4_0 uses these dummy cycles for reading volatile registers.
19. RDCRC_4_0 alway has 8 cycles of latency. Maximum frequency under SDR SPI is 166 MHz, under HS-T SDR/DDR Octal is 200 MHz and under HL-T SDR/DDR Octal is 166 MHz

1.3.7 Configuration Register 4 (CFR4x)

Configuration Register 4 controls the main Flash array read transactions burst wrap behavior and output driver impedance.

Table 20. Configuration Register 4

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
CFR4N[7:5] CFR4V[7:5]	IOIMPD[2:0]	I/O Driver Output Impedance selection	N -> R/W V -> R/W	101	Description: The IOIMPD[2:0] bits select the IO driver output impedance (drive strength). The output impedance configuration bits adjust the drive strength during normal device operation to meet system signal integrity requirements. Selection Options: 000 = 45Ω 001 = 120Ω 010 = 90Ω 011 = 60Ω 100 = 45Ω 101 = 30Ω (Factory Default) 110 = 20Ω 111 = 15Ω Dependency: N/A
CFR4N[4] CFR4V[4]	RBSTWP	Read Burst Wrap Enable selection	N -> R/W V -> R/W	0	Description: The RBSTWP bit selects the read burst wrap feature. It allows the device to enter and exit burst wrapped read mode during normal operation. The wrap length is selected by RBSTWL[1:0] bits. Selection Options: 0 = Read Wrapped Burst disabled 1 = Read Wrapped Burst enabled Dependency: RBSTWL[1:0] (CFR4x[1:0])
CFR4N[3] CFR4V[3]	ECC12S	Error Correction Code (ECC) 1-bit or 1-bit/2-bit error correction selection	N -> R/W V -> R/W	1	Description: The ECC12S bit selects between 1-bit ECC error detection/ correction or both 1-bit ECC error detection and correction and 2-bit ECC error detection. This configuration option affects Address Trap Register and ECC Counter Register functionalities as well. The host needs to erase and reprogram the data in the Semper Flash memory upon ECC configuration change (1-bit correction to 1-bit correction and 2-bit detection or vice versa). Selection Options: 0 = 1-bit ECC Error Detection/Correction 1 = 1-bit ECC Error Detection/Correction and 2-bit ECC error detection Dependency: N/A

Table 20. Configuration Register 4 (Continued)

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
CFR4N[2] CFR4V[2]	DPDPOR	Deep Power Down power saving mode entry selection upon POR	N -> R/W V -> R	0	Description: The DPDPOR bit selects if the device will be in either Deep Power Down (DPD) mode or the Standby mode after the completion of POR. If enabled, DPDPOR configures the device to start in DPD mode to reduce current consumption until the device is needed. If the device is in DPD, a pulse on CS# or a Hardware reset will return the device to Standby mode. Selection Options: 0 = Standby mode is entered upon the completion of POR 1 = Deep Power Down Power mode is entered upon the completion of POR Dependency: N/A
CFR4N[1:0] CFR4V[1:0]	RBSTWL[1:0]	Read Burst Wrap Length selection	N -> R/W V -> R/W	00	Description: The RBSTWL[1:0] bits select the read burst wrap length and alignment during normal operation. It selects the fixed length/aligned group of 8-, 16-, 32-, or 64-bytes. Selection Options: 00 = 8 Bytes Wrap length 01 = 16 Bytes Wrap length 10 = 32 Bytes Wrap length 11 = 64 Bytes Wrap length Dependency: RBSTWP (CFR4x[4])

Table 21. Output Data Wrap Sequence

Wrap Boundary (Bytes)	Start Address (Hex)	Address Sequence (Hex)
Sequential	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18.
8	XXXXXX00	00, 01, 02, 03, 04, 05, 06, 07, 00, 01, 02.
8	XXXXXX07	07, 00, 01, 02, 03, 04, 05, 06, 07, 00, 01.
16	XXXXXX02	02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03.
16	XXXXXX0C	0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E.
32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F.
32	XXXXXX1E	1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00.
64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F 00, 01, 02.
64	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D.

1.3.8 Configuration Register 5 (CFR5x)

Configuration Register 5 controls the Octal SPI device behavior.

Table 22. Configuration Register 5

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
CFR5N[7] CFR5V[7]	RESRVD	Reserved for Future Use	N -> R/W V -> R/W	0	These bits are Reserved for future use. This bit must always be written/loaded to its default state.
CFR5N[6] CFR5V[6]	RESRVD	Reserved for Future Use	N -> R/W V -> R/W	1	
CFR5N[5:2] CFR5V[5:2]	RESRVD	Reserved for Future Use	N -> R/W V -> R/W	0000	

Table 22. Configuration Register 5 (Continued)

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
CFR5N[1] CFR5V[1]	SDRDDR	Octal SPI SDR or DDR selection	N -> R/W V -> R/W	0	Description: The SDRDDR bit selects between SDR or DDR for all data transfers to the device. Based on SDRDDR selection, all transactions either are SDR or DDR. **Note** SDRDDR bit only controls the interface for Octal mode (8-8-8). Selection Options: 0 = SDR enabled 1 = DDR enabled Dependency: N/A
CFR5N[0] CFR5V[0]	OPI-IT	Octal Interface and Protocol Selection - I/O width set to 8 bits (8-8-8)	N -> R/W V -> R/W	0	Description: The OPI-IT bit selects the I/O width of the device to be 8-bits wide. When configured to 8-bits (OPI-IT) all transactions require Opcode, Address and Data always sent on all eight I/Os. Selection Options: 0 = Data Width set to 1 bit wide (1x) - Legacy Single SPI Protocol 1 = Data Width set to 8 wide (8x) - Octal Protocol Dependency: N/A

1.3.9 Interface CRC Enable Register (ICEV)

Interface CRC Enable Register controls the enabling/disabling of the Interface CRC function.

Table 23. Interface CRC Enable Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
ICEV[7:1]	RESVRD	Reserved for Future Use	V -> R	0000000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
ICEV[0]	ITCRCE	Interface CRC Selection	V -> R/W	0	Description: The ITCRCE bit controls enabling/disabling of the Interface CRC function. Selection Options: 0 = Interface CRC Enabled 1 = Interface CRC Disabled Dependency: N/A

1.3.10 Interface CRC Check-value Register (ICRV)

The Interface CRC Check-value Register (ICRV) stores the results of the CRC calculation on the command and Data Content over the interface for Protection.

Table 24. Interface CRC Check-value Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (hex)	Description
ICRV[31:0]	ITCRCV[31:0]	Interface CRC Checksum Value	V -> R	0xFFFFFFFF	Description: The ITCRCV[31:0] bits store the check-value of the CRC process on the memory array data contained within the starting address and the ending address. Selection Options: Checksum Value Dependency: N/A

1.3.11 Memory Array Data Integrity Check CRC Register (DCRV)

The memory array Data Integrity Check CRC Register (DCRV) stores the results of the CRC calculation on the data contained between the specified starting and ending addresses.

Table 25. Memory Array Data Integrity Check CRC Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (hex)	Description
DCRV[31:0]	DTCRCV[31:0]	Memory Array Data CRC Checksum Value	V -> R	0x00000000	Description: The DTCRCV[31:0 bits store the checksum value of the CRC process on the memory array data contained within the starting address and the ending address. Selection Options: Checksum Value Dependency: N/A

1.3.12 ECC Status Register (ESCV)

The ECC Status Register (ESCV) contains the ECC status of any error correction action performed on the unit data whose byte was addressed during last read.

Note Unit data is defined as the number of bytes over which the ECC is calculated. HL-T/HS-T family devices have a 16 bytes (128 bits) unit data.

Table 26. ECC Status Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
ECSV[7:5]	RESRVD	Reserved for Future Use	V -> R	000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
ECSV[4]	ECC2BT	ECC Error 2-bit Error Detection Flag	V -> R	0	Description: The ECC2BT bit indicates that a 2-bit ECC Error was detected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC2BT. **Note** ECC2BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC2BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed. **Note** ECC1BT is not valid if ECC2BT status flag is set. Selection Options: 0 = No 2-Bit ECC Error was detected in the data unit (16 bytes) 1 = 2-bit ECC Error was detected in the data unit (16 bytes) Dependency: N/A
ECSV[3]	ECC1BT	ECC Error 1-bit Error Detection and Correction Flag	V -> R	0	Description: The ECC1BT bit indicates that a 1-bit ECC Error was detected and corrected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC1BT. **Note** ECC1BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC1BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed. Selection Options: 0 = No 1-Bit ECC Error was detected in the data unit (16 bytes) 1 = 1-bit ECC Error was detected in the data unit (16 bytes) Dependency: N/A
ECSV[2:0]	RESRVD	Reserved for Future Use	V -> R	000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.

1.3.13 ECC Address Trap Register (EATV)

The ECC Address Trap Register (EATV) stores the address of the ECC unit data where either a 1-Bit/2-Bit error or only a 1-Bit error occurred during a read operation. It stores the ECC unit address of the first ECC error captured during a memory read operation since the last Clear ECC transaction.

Table 27. ECC Address Trap Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (hex)	Description
EATV[31:0]	ECCATP[31:0]	ECC 1-bit and 2-bit Error Address Trap Register	V -> R	0x00000000	Description: The Address Trap Register (ECCATP[31:0]) stores the ECC unit data address where a 1-Bit/2-Bit error occurred during a read operation. ECCATP[31:0] stores the ECC unit address of the first ECC error captured during a memory read operation since the last Clear ECC Status Register transaction (CLECC_0_0). **Note** ECCATP[31:0] is only updated during Read Instruction. **Note** Clear ECC Status Register transaction (CLECC_0_0), POR or Hardware/Software reset clears the EATV[31:0] to 0x00000000. Selection Options: ECC Error Data Unit Address Dependency: N/A

1.3.14 ECC Error Detection Count Register (ECTV)

The ECC Error Detection Counter Register (ECTV) stores the number of either 1-Bit/2-Bit or only 1-Bit ECC errors have occurred during read operations since the last POR or hardware/software reset.

Table 28. ECC Count Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (hex)	Description
ECTV[15:0]	ECCCNT[15:0]	ECC 1-bit and 2-bit Error Count Register	V -> R	0x0000	Description: The ECCCNT[15:0] stores the number of 1-bit/2-bit ECC errors occurred during read operations since the last POR or hardware/software reset. **Note** ECCCNT[15:0] is only updated during Read Instruction. **Note** Only one ECC error is counted for each data unit. If multiple read transactions access the same unit data containing an ECC error, the ECCCNT[15:0] will increment each time the unit data is read. **Note** Once the count reaches 0xFFFF, theECCCNT[15:0] will stop incrementing **Note** POR or Hardware/Software reset clears the ECCNT[15:0] to 0x0000. Selection Options: ECC Error Count Dependency: N/A

1.3.15 Advanced Sector Protection Register (ASPO)

The ASP Register (ASPO) configures the behavior of Advanced Sector Protection scheme.

Table 29. Advanced Sector Protection Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
ASPO[15:6]	RESRVD	Reserved for Future Use	N -> R/1	1111111111	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
ASPO[5]	ASPRDP	Read Password Based Protection Selection	N -> R/1	1	Description: The ASPRDP bit selects the Read Password Mode Protection mode. Read Password Protection mode works in conjunction with Password Protection mode to protect all sectors from Read/Erase/Program. Based on TBPROT configuration bit (CFR1x[5]), either the top or bottom sector is available for reading. Selection Options: 0 = Read Password Protection Mode is enabled 1 = Read Password Protection Mode is disabled Dependency: TBPROT (CFR1x[5])
ASPO[4]	ASPDYB	Dynamic Protection (DYB) for all sectors at power-up Selection	N -> R/1	1	Description: The ASPDYB bit selects whether all DYB bits (sectors) are in the protected state following power-up or hardware reset. DYB bits will individually need to be reset to change sector protections. Selection Options: 0 = DYB based sector protection enabled at power-up or hardware reset 1 = DYB based sector protection disabled at power-up or hardware reset Dependency: N/A
ASPO[3]	ASPPPB	Permanent Protection (PPB) bits for all sectors programmability Selection	N -> R/1	1	Description: The ASPPPB bit selects whether all PPB bits are one-time programmable making PPB sector protection permanent. **Note** ASPPPB disables PPB erase transaction (ERPPB_0_0). Selection Options: 0 = PPB bits are one-time programmable 1 = PPB bits can be erased and programmed as desired Dependency: N/A
ASPO[2]	ASPPWD	Password Based Protection Selection	N -> R/1	1	Description: The ASPPWD bit selects the Password Protection Mode. Password Protection mode protects all PPB bits, all registers and all memory from erase/program till the correct password is entered. The ASPPWD can also be used in combination with the ASPRDP to protect sectors from being read as well till the correct password is provided – except for top or bottom sector which is available for reading based on TBPROT configuration bit (CFR1x[5]). **Note** When ASPPAS is selected, ASPO[15:0] are protected against program operations. Selection Options: 0 = Password Protection Mode is enabled 1 = Password Protection Mode is disabled Dependency: N/A
ASPO[1]	ASPPER	Persistent Protection Selection (Register Protection Selection)	N -> R/1	1	Description: The ASPPER bit selects the Persistent Protection Mode. The Persistent Protection mode (ASPPER) protects the ASPO[15:0], CFR1x[6, 5, 4, 2] and CFR3x[3] registers from erase or program. Selection Options: 0 = Persistent Protection Mode is enabled 1 = Persistent Protection Mode is disabled Dependency: N/A
ASPO[0]	ASPPRM	Permanent Protection Selection	N -> R/1	1	Description: The ASPPRM bit selects the Permanent Protection Mode. The Permanent Protection mode (ASPPRM) permanently protects the PPB bits from erase or program. ASPPRM bit should be programmed once all the PPB based sector protections are finalized. **Note** Permanent protection is independent of the PPBLOCK bit. Selection Options: 0 = Permanent Protection Mode is enabled 1 = Permanent Protection Mode is disabled Dependency: N/A

1.3.16 ASP Password Register (PWDO)

The ASP Password Register (PWDO) is used to permanently define a password.

Table 30. Password Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (hex)	Description
PWDO[63:0]	PASWRD[63:0]	Password Register	N -> R/1	0xFFFFFFFFFFFFFFFF	Description: The PASWRD[63:0] permanently stores a password used in password protected modes of operation. When the Password Protection Mode is enabled, this register will output the undefined data upon read password request. Selection Options: Password Dependency: N/A

1.3.17 ASP PPB Lock Register (PPLV)

The PPBLCK bit in the ASP PPB Lock Register (PPLV) is used to protect the PPB bits.

Table 31. ASP PPB Lock Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
PPLV[7:1]	RESVRD	Reserved for Future Use	V -> R	0000000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
PPLV[0]	PPBLCK	PPB Temporary Protection Selection	V -> R/W	1, ASPO[2:1]	Description: The PPBLCK bit is used to temporarily protect all the PPB bits. Selection Options: 1 = PPB Bits can be erased or programmed 0 = PPB bits are protected against erase or program till the next POR or hardware reset Dependency: N/A

1.3.18 ASP PPB Access Register (PPAV)

The ASP PPB Access Register (PPAV) is used to provide the state of each sector's PPB protection bit.

Table 32. ASP PPB Access Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
PPAV[7:0]	PPBACS[7:0]	Sector Based PPB Protection Status	N -> R/W	11111111	Description: The PPBACS[7:0] bits are used to provide the state of the individual sector's PPB bit. Selection Options: FF = PPB for the sector addressed by the Read PPB transaction (RDPPB_4_0) is 1, not protecting that sector from program or erase operations 00 = PPB for the sector addressed by the Read PPB transaction (RDPPB_4_0) is 0, protecting that sector from program or erase operations Dependency: N/A

1.3.19 ASP Dynamic Block Access Register (DYAV)

The ASP DYB Access Register (DYAV) is used to provide the state of each sector's DYB protection bit.

Table 33. ASP DYB Access Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
DYAV[7:0]	DYBACS[7:0]	Sector Based DYB Protection Status	V -> R/W	11111111	Description: The DYBACS[7:0] bits are used to provide the state of the individual sector's DYB bit. Selection Options: FF = DYB for the sector addressed by the Read DYB transaction (RDDYB_4_0) is 1, not protecting that sector from program or erase operations 00 = DYB for the sector addressed by the Read DYB transaction (RDDYB_4_0) is 0, protecting that sector from program or erase operations Dependency: N/A

1.3.20 AutoBoot Register (ATBN)

The AutoBoot Register (ATBN) provides a means to automatically read boot code as part of the power-on reset, or hardware reset process.

Table 34. AutoBoot Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
ATBN[31:9]	STADR[22:0]	Starting Address Selection where AutoBoot will start reading data from	N -> R/W	00000000000000000000000	Description: The STADR[22:0] bits set the starting address from which the device will output the read data. Selection Options: Address Bits Dependency: N/A
ATBN[8:1]	STDLY[7:0]	AutoBoot Read Starting Delay Selection	N -> R/W	00000000	Description: The STDLY[7:0] bits specify the initial delay (clock cycles) needed by the host before it can accept data. **Note** STDLY[7:0]=0x00 is valid for SPI up to 50 MHz. STDLY[7:0] = 0x01 or higher is valid for SPI up to 166 MHz. STDLY[7:0] = 0x05 or higher is valid for HL-T Octal up to 166 MHz and HS-T Octal up to 200 MHz. Selection Options: Address Bits Dependency: N/A
ATBN[0]	ATBTEN	AutoBoot Feature Selection	N -> R/W	0	Description: The ATBTEN bit enables or disables the AutoBoot feature. Selection Options: 0 = AutoBoot feature disabled 1 = AutoBoot feature enabled Dependency: N/A

1.3.21 Sector Erase Count Register (SECV)

The Sector Erase Count Register (SECV) contains the number of times the addressed sector has been erased.

Table 35. Sector Erase Count Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (hex)	Description
SECV[23]	SECCPT	Sector Erase Count Corruption Status Flag	V -> R	0x0	Description: The SECCPT bit is used to determine if the reported sector erase count is corrupted and was reset. **Note** If SECCPT is set due to count corruption, it will reset to 0 on the next successful erase operation on the selected sector. Selection Options: 0 = Sector Erase Count is not corrupted and is valid 1 = Sector Erase Count is corrupted and is not valid Dependency: N/A
SECV[22:0]	SECVAL[22:0]	Sector Erase Count Value	V -> R	0x000000	Description: The SECVAL[22:0] bits store the number of times a sector has been erased Selection Options: Value Dependency: N/A

1.3.22 INT# Pin Configuration Register (INCV) - Octal Only

The INT# pin Configuration Register (INCV) configures which internal event will trigger a HIGH to LOW transition on the INT# output pin.

Note When INCV disables a particular feature from driving the INT# pin, it will prevent the corresponding INSV bit(s) from being updated.

Note Clearing a bit within INCV has no effect on INSV, and it is a system responsibility to independently clear the INSV as required.

Table 36. Interrupt Configuration Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
INCV[7]	INTBEN	INT# pin Enable Selection	V -> R/W	1	Description: The INT# pin is an open-drain output used to indicate to the host system that an event has occurred within the memory device. The INTBEN bit enables or disables the functionality controlling INT# pin. Selection Options: 0 = INT# pin functionality is enabled 1 = INT# pin functionality is disabled Dependency: N/A
INCV[6:5]	RESRVD	Reserved for Future Use	V -> R/W	11	These bits are Reserved for future use. This bit must always be written/ loaded to its default state.
INCV[4]	REYBSY	Ready/Busy Transition Selection	V -> R/W	1	Description: The REYBSY bit enables or disables whether device ready/ busy state will transition INT#. Selection Options: 0 = A Busy to Ready transition will cause a HIGH to LOW transition on the INT# output 1 = Ready/Busy transitions will not transition the INT# output Dependency: N/A
INCV[3:2]	RESRVD	Reserved for Future Use	V -> R/W	11	These bits are Reserved for future use. This bit must always be written/ loaded to its default state.
INCV[1]	ECC2BT	ECC 2-bit Error Detection Selection0	V -> R/W	1	Description: The ECC2BT bit enables or disables whether a 2-bit ECC detection error will transition INT#. Selection Options: 0 = 2-bit ECC detection will cause a HIGH to LOW transition the INT# output 1 = 2-bit ECC detection will not transition the INT# output Dependency: N/A

Table 36. Interrupt Configuration Register (Continued)

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
INCV[0]	ECC1BT	ECC 1-bit Error Detection and Correction Selection	V -> R/W	1	Description: The ECC1BT bit enables or disables whether a 1-bit ECC detection and correction error will transition INT#. Selection Options: 0 = 1-bit ECC detection and correction will cause a HIGH to LOW transition the INT# output 1 = 1-bit ECC detection and correction will not transition the INT# output Dependency: N/A

1.3.23 INT# Pin Status Register (INSV) - Octal Only

The INT# Pin Status Register (INSV) indicates which internal event(s) has occurred since the last time the ISR was cleared.

Table 37. Interrupt Status Register

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
INSV[7:5]	RESRVD	Reserved for Future Use	V -> R/W	111	These bits are Reserved for future use. This bit must always be written/ loaded to its default state.
INSV[4]	REYBSY	Ready/Busy Transition	V -> R/W	1	Description: The REYBSY bit indicates whether the device's ready/busy status has caused a transition on INT#. Selection Options: 0 = A Busy to Ready transition has occurred 1 = A Busy to Ready transition has not occurred Dependency: N/A
INSV[3:2]	RESRVD	Reserved for Future Use	V -> R/W	11	These bits are Reserved for future use. This bit must always be written/ loaded to its default state.
INSV[1]	ECC2BT	ECC 2-bit Error Detection	V -> R/W	1	Description: The ECC2BT bit indicates whether a 2-bit ECC detection error has caused a transition on INT#. Selection Options: 0 = 2-bit error detection has occurred 1 = 2-bit error detection has not occurred Dependency: N/A
INSV[0]	ECC1BT	ECC 1-bit Error Detection and Correction	V -> R/W	1	Description: The ECC1BT bit indicates whether a 1-bit ECC correction error has caused a transition on INT#. Selection Options: 0 = 1-bit error correction has occurred 1 = 1-bit error correction has not occurred Dependency: N/A

1.3.24 EnduraFlex Architecture Selection Register (EFXx)

The EnduraFlex Architecture Selection registers (EFXx) define the long retention / high endurance regions based on a four pointer based architecture.

Table 38. EnduraFlex Architecture Selection Register (Pointer 4)

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
EFX4O[10:2]	EPTAD4[8:0]	EnduraFlex Pointer 4 Address Selection	N -> R/1	111111111	Description: The EPTAD4[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined. Selection Options: Pointer Address Dependency: N/A
EFX4O[1]	ERGNT4	EnduraFlex Pointer 4 based Region Type Selection	N -> R/1	1	Description: The ERGNT4 bit defines whether the region is long retention or high endurance. Selection Options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A
EFX4O[0]	EPTEB4	EnduraFlex Pointer 4 Enable# Selection	N -> R/1	1	Description: The EPTEN4 bit define whether the wear leveling pointer is enabled/disabled. Selection Options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A

Table 39. EnduraFlex Architecture Selection Register (Pointer 3)

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
EFX3O[10:2]	EPTAD3[8:0]	EnduraFlex Pointer 3 Address Selection	N -> R/1	111111111	Description: The EPTAD3[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined. Selection Options: Pointer Address Dependency: N/A
EFX3O[1]	ERGNT3	EnduraFlex Pointer 3 based Region Type Selection	N -> R/1	1	Description: The ERGNT3 bit defines whether the region is long retention or high endurance. Selection Options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A
EFX3O[0]	EPTEB3	EnduraFlex Pointer 3 Enable# Selection	N -> R/1	1	Description: The EPTEN3 bit define whether the wear leveling pointer is enabled/disabled. Selection Options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A

Table 40. EnduraFlex Architecture Selection Register (Pointer 2)

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
EFX2O[10:2]	EPTAD2[8:0]	EnduraFlex Pointer 2 Address Selection	N -> R/1	111111111	Description: The EPTAD2[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined. Selection Options: Pointer Address Dependency: N/A
EFX2O[1]	ERGNT2	EnduraFlex Pointer 2 based Region Type Selection	N -> R/1	1	Description: The ERGNT2 bit defines whether the region is long retention or high endurance. Selection Options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A
EFX2O[0]	EPTEB2	EnduraFlex Pointer 2 Enable# Selection	N -> R/1	1	Description: EPTEN2 bit define whether the wear leveling pointer is enabled/disabled. Selection Options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A

Table 41. EnduraFlex Architecture Selection Register (Pointer 1)

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
EFX1O[10:2]	EPTAD1[8:0]	EnduraFlex Pointer 1 Address Selection	N -> R/1	111111111	Description: The EPTAD1[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined. Selection Options: Pointer Address Dependency: N/A
EFX1O[1]	ERGNT1	EnduraFlex Pointer 1 based Region Type Selection	N -> R/1	1	Description: The ERGNT1 bit defines whether the region is long retention or high endurance. Selection Options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A
EFX1O[0]	EPTEB1	EnduraFlex Pointer 1 Enable# Selection	N -> R/1	1	Description: The EPTEN1 bit define whether the wear leveling pointer is enabled/disabled. Selection Options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A

Table 42. EnduraFlex Architecture Selection Register (Pointer 0)

Bit Number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory Default (binary)	Description
EFX0O[1]	GBLSEL	All Sectors based Region type Selection	N -> R/1	1	Description: The GBLSEL bit defines whether all sectors are defined as long retention region or high endurance region. **Note** If all other pointer registers are disabled, this bit defines the behavior of the entire memory space and is hardwired to start at Sector 0. Selection Options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A
EFX0O[0]	WRLVEN	Wear Leveling Enable Selection	N -> R/1	1	Description: The WRLVEN bit enables/disables the wear leveling feature. Selection Options: 0 = Wear Leveling Disabled 1 = Wear Leveling Enabled Dependency: N/A

1.4 Transaction Table

1.4.1 SPI (1S-1S-1S) Transaction Table

Table 43. SPI (1S-1S-1S) Transaction Table

Function	Transaction Name	Description	Prerequisite Transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction Format	Max Frequency (MHz)	Address Length
Read Device ID	RDIDN_0_0	**Read manufacturer and device identification** transaction provides read access to manufacturer and device identification.	–	9F (CMD)	–	–	–	–	–	–	–	–	Figure 10	166	N/A
	RSFDP_3_0	**Read JEDEC Serial Flash Discoverable Parameters** transaction sequentially accesses the Serial Flash Discovery Parameters (SFDP).	–	5A (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 11	156	3
	RDUID_0_0	**Read Unique ID** accesses a factory programmed 64-bit number which is unique to each device.	–	4C (CMD)	–	–	–	–	–	–	–	–	Figure 10	166	N/A
Register Access	RDSR1_0_0	**Read Status Register 1** transaction allows the Status Register 1 contents to be read from DQ1/SO.	–	05 (CMD)	–	–	–	–	–	–	–	–			
	RDSR2_0_0	**Read Status Register-2** transaction allows the Status Register-2 contents to be read from DQ1/SO.	–	07 (CMD)	–	–	–	–	–	–	–	–			
	RDARG_C_0	**Read Any Register** transaction provides a way to read all addressed nonvolatile and volatile device registers.	–	65 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 11		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	WRENB_0_0	**Write Enable** sets the Write Enable Latch bit of the Status Register 1 to 1 to enable write, program and erase transactions.	–	06 (CMD)	–	–	–	–	–	–	–	–	Figure 5		N/A
	WRDIS_0_0	**Write Disable** sets the Write Enable Latch bit of the Status Register 1 to 0 to disable write, program and erase transactions execution.	–	04 (CMD)	–	–	–	–	–	–	–	–			
	WRARG_C_1	**Write Any Register** transaction provides a way to write all addressed nonvolatile and volatile device registers.	WRENB_0_0	71 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–	–	Figure 8		3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–			4
	CLPEF_0_0	**Clear Program and Erase Failure Flags** transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag).	–	82 (CMD)	–	–	–	–	–	–	–	–	Figure 5		N/A
ECC	RDECC_4_0	**Read ECC Status** is used to determine the ECC status of the addressed data unit.	–	19 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 11		4
	CLECC_0_0	**Clear ECC Status Register** transaction resets ECC Status Register bit[4] (2-bit ECC Detection), ECC Status Register bit[3] (1-bit ECC Correction), Address Trap Register and ECC Detection Counter.	–	1B (CMD)	–	–	–	–	–	–	–	–	Figure 5		N/A
CRC	DICHK_4_1	**Data Integrity Check** transaction causes the device to perform a Data Integrity Check over a user defined address range.	–	5B (CMD)	Start ADDR [31:24]	Start ADDR [23:16]	Start ADDR [15:8]	Start ADDR [7:0]	End ADDR [31:24]	End ADDR [23:16]	End ADDR [15:8]	End ADDR [7:0]	Figure 7		4

Table 43. SPI (1S-1S-1S) Transaction Table (Continued)

Function	Transaction Name	Description	Prerequisite Transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction Format	Max Frequency (MHz)	Address Length
Read Flash Array	RDAY1_C_0	**Read** transaction reads out the memory contents at the given address. The maximum CK frequency for this transaction is 50 MHz frequency.	–	03 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 12	50	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	RDAY1_4_0		–	13 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
	RDAY2_C_0	**Read Fast** transaction reads out the memory contents at the given address. The maximum CK frequency for this transaction is 166 MHz frequency.	–	0B (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 11	166	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
Program Flash Array	PRPGE_4_1	**Program Page** programs 256B or 512B data to the memory array in one transaction.	WRENB_0_0	12 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	Figure 8		
Erase Flash Array	ER004_4_0	**Erase 4-KB Sector** transaction sets all the bits of a 4 KB sector to 1 (all bytes are FFh).	WRENB_0_0	21 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 6		
	ER256_4_0	**Erase 256-KB Sector** transaction sets all the bits of a 256 KB sector to 1 (all bytes are FFh).	WRENB_0_0	DC (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
	ERCHP_0_0	**Erase Chip** transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array.	WRENB_0_0	60 or C7 (CMD)	–	–	–	–	–	–	–	–	Figure 5		N/A
	EVERS_4_0	**Evaluate Erase Status** transaction verifies that the last erase operation on the addressed sector was completed successfully.	–	D0 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 6		4
	SEERC_4_0	**Sector Erase Count** transaction outputs the number of erase cycles for the sector of the inputed address from the Sector Erase Count Register.	–	5D (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 11		
Suspend / Resume	SPEPD_0_0	**Suspend Erase / Program / Data Integrity Check** transaction allows the system to interrupt a programming, erase or data integrity check operation.	–	B0 (CMD)	–	–	–	–	–	–	–	–	Figure 5		N/A
	RSEPD_0_0	**Resume Erase / Program / Data Integrity Check** transaction allows the system to resume a programming, erase or data integrity check operation.	–	7A (CMD)	–	–	–	–	–	–	–	–			
Secure Silicon Region	PRSSR_4_1	**Program Secure Silicon Region** transaction programs data in 1024 bytes of Secure Silicon Region.	WRENB_0_0	42 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	Figure 8		4
	RDSSR_4_0	**Read Secure Silicon Region** transaction reads data from the SSR.	–	4B (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 11		

Table 43. SPI (1S-1S-1S) Transaction Table (Continued)

Function	Transaction Name	Description	Prerequisite Transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction Format	Max Frequency (MHz)	Address Length
Advanced Sector Protection	RDDYB_4_0	**Read Dynamic Protection Bit** transaction reads the contents of the DYB Access Register.	–	E0 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 11	166	4
	WRDYB_4_1	**Write Dynamic Protection Bit** transaction writes to the DYB Access Register.	WRENB_0_0	E1 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–	Figure 8		
	RDPPB_4_0	**Read Persistent Protection Bit** transaction reads the contents of the PPB Access Register.	–	E2 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 11		
	PRPPB_4_0	**Program Persistent Protection Bit** transaction programs / writes the PPB Register to enable the sector protection.	WRENB_0_0	E3 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 6		
	ERPPB_0_0	**Erase Persistent Protection Bit** transaction sets all persistent protection bits to 1.	WRENB_0_0	E4 (CMD)	–	–	–	–	–	–	–	–	Figure 5		N/A
	WRPLB_0_0	**Write PPB Protection Lock Bit** transaction clears the PPB Lock to 0.	WRENB_0_0	A6 (CMD)	–	–	–	–	–	–	–	–			
	RDPLB_0_0	**Read Password Protection Mode Lock Bit** transaction shifts out the 8-bit PPB Lock Register contents with MSb first.	–	A7 (CMD)	–	–	–	–	–	–	–	–	Figure 10		
	PWDUL_0_1	**Password Unlock** transaction sends the 64-bit password to flash device. If the supplied password does not match the hidden password in the Password Register, the device is locked and only a hardware reset or POR will return the device to standby state, ready for new transactions such as a retry of the PWDUL_0_1. If the password does match, the PPB Lock bit is set to 1.	–	E9 (CMD)	Password [7:0]	Password [15:8]	Password [23:16]	Password [31:24]	Password [39:32]	Password [47:40]	Password [55:48]	Password [63:56]	Figure 9		
Reset	SRSTE_0_0	**Software Reset Enable** command is required immediately before a SFRST_0_0 transaction.	–	66 (CMD)	–	–	–	–	–	–	–	–	Figure 5		
	SFRST_0_0	**Software Reset** transaction restores the device to its initial power up state, by reloading volatile registers from nonvolatile default values.	SRSTE_0_0	99 (CMD)	–	–	–	–	–	–	–	–			
Deep Power Down	ENDPD_0_0	**Enter Deep Power Down Mode** transaction shifts device in the lowest power consumption mode.	–	B9 (CMD)	–	–	–	–	–	–	–	–			

1.4.2 Octal (8S-8S-8S, 8D-8D-8D) Transaction Table

Table 44. Octal (8S-8S-8S, 8D-8D-8D) Transaction Table

Function	Transaction Name	Description	Prerequisite Transaction	Byte 1 (Hex) CK ↑ Edge[20]	Byte 2 (Hex) CK ↓ Edge[20]	Byte 3 (Hex) CK ↑ Edge[20]	Byte 4 (Hex) CK ↓ Edge[20]	Byte 5 (Hex) CK ↑ Edge[20]	Byte 6 (Hex) CK ↓ Edge[20]	Byte 7 (Hex) CK ↑ Edge[20]	Byte 8 (Hex) CK ↓ Edge[20]	Byte 9 (Hex) CK ↑ Edge[20]	Byte 10 (Hex) CK ↓ Edge[20]	Byte 11 (Hex) CK ↑ Edge[20]	Byte 12 (Hex) CK ↓ Edge[20]	Byte 13 (Hex) CK ↑ Edge[20]	Byte 14 (Hex) CK ↓ Edge[20]	Transaction Format (SDR/DDR)	HL-T / HS-T Max Frequency (MHz)	Address Length
Read Device ID	RDIDN_4_0	**Read manufacturer and device identification** transaction provides read access to manufacturer and device identification.	–	9F (CMD)	9F (CMD)	00 (ADDR)	00 (ADDR)	00 (ADDR)	00 (ADDR)	–	–	–	–	–	–	–	–	Figure 23 / Figure 24	166/ 200	4
	RSFDP_4_0	**Read JEDEC Serial Flash Discoverable Parameters** transaction sequentially accesses the Serial Flash Discovery Parameters (SFDP).	–	5A (CMD)	5A (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–		92 (SDR) / 85 (DDR)	
	RDUID_4_0	**Read Unique ID** accesses a factory programmed 64-bit number which is unique to each device.	–	4C (CMD)	4C (CMD)	00 (ADDR)	00 (ADDR)	00 (ADDR)	00 (ADDR)	–	–	–	–	–	–	–	–			
Register Access	RDSR1_4_0	**Read Status Register 1** transaction allows the Status Register 1 contents to be read from DQ[7:0]	–	05 (CMD)	05 (CMD)	00 (ADDR)	00 (ADDR)	00 (ADDR)	00 (ADDR)	–	–	–	–	–	–	–	–	Figure 23 / Figure 25		
	RDSR2_4_0	**Read Status Register-2** transaction allows the Status Register-2 contents to be read from DQ[7:0]	–	07 (CMD)	07 (CMD)	00 (ADDR)	00 (ADDR)	00 (ADDR)	00 (ADDR)	–	–	–	–	–	–	–	–			
	RDARG_4_0	**Read Any Register** transaction provides a way to read all addressed nonvolatile and volatile device registers.	–	65 (CMD)	65 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–	Figure 23 / Figure 24		
	WRENB_0_0	**Write Enable** sets the Write Enable Latch bit of the Status Register 1 to 1 to enable write, program and erase transactions.	–	06 (CMD)	06 (CMD)	–	–	–	–	–	–	–	–	–	–	–	–	Figure 14 / Figure 15	166/ 200	N/A
	WRDIS_0_0	**Write Disable** sets the Write Enable Latch bit of the Status Register 1 to 0 to disable write, program and erase transactions execution.	–	04 (CMD)	04 (CMD)	–	–	–	–	–	–	–	–	–	–	–	–			
	WRARG_4_1	**Write Any Register** transaction provides a way to write all addressed nonvolatile and volatile device registers.	WRENB_0_0	71 (CMD)	71 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–	–	–	–	–	Figure 20 / Figure 21		4
	CLPEF_0_0	**Clear Program and Erase Failure Flags** transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag)	–	82 (CMD)	82 (CMD)	–	–	–	–	–	–	–	–	–	–	–	–	Figure 14 / Figure 15		N/A
ECC	RDECC_4_0	**Read ECC Status** is used to determine the ECC status of the addressed data unit.	–	19 (CMD)	19 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–	Figure 23 / Figure 25		4
	CLECC_0_0	**Clear ECC Status Register** transaction resets ECC Status Register bit[4] (2-bit ECC Detection), ECC Status Register bit[3] (1-bit ECC Correction), Address Trap Register and ECC Detection Counter.	–	1B (CMD)	1B (CMD)	–	–	–	–	–	–	–	–	–	–	–	–	Figure 14 / Figure 15		N/A

Note
20. In case of Octal DDR protocol.

Table 44. Octal (8S-8S-8S, 8D-8D-8D) Transaction Table (Continued)

Function	Transaction Name	Description	Prerequisite Transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Byte 10 (Hex)	Byte 11 (Hex)	Byte 12 (Hex)	Byte 13 (Hex)	Byte 14 (Hex)	Transaction Format (SDR/DDR)	HL-T / HS-T Max Frequency (MHz)	Address Length
				CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]			
CRC	RDCRC_4_0	**Read Interface CRC Register** transaction allows the volatile Interface CRC Register contents to be read	–	64 (CMD)	64 (CMD)	00 (ADDR)	00 (ADDR)	00 (ADDR)	00 (ADDR)	–	–	–	–	–	–	–	–	Figure 23 / Figure 24	166 / 200	4
	DICHK_4_1	**Data Integrity Check** transaction causes the device to perform a Data Integrity Check over a user defined address range.	–	5B (CMD)	5B (CMD)	00 (ADDR)	00 (ADDR)	00 (ADDR)	00 (ADDR)	Start ADDR [31:24]	Start ADDR [23:16]	Start ADDR [15:8]	Start ADDR [7:0]	End ADDR [31:24]	End ADDR [23:16]	End ADDR [15:8]	End ADDR [7:0]	Figure 18 / Figure 19		
Read Flash Array	RDAY1_4_0	**Read Octal SDR** transaction reads out the memory contents at the given address on DQ[7:0]. The maximum CK frequency for this SDR transaction is 200-MHz frequency	–	EC (CMD)	EC (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–	Figure 23		
	RDAY2_4_0	**Read Octal DDR** transaction reads out the memory contents at the given address on DQ[7:0]. The maximum CK frequency for this DDR transaction is 200-MHz frequency	–	EE (CMD)	EE (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–	Figure 24		
Program Flash Array	PRPGE_4_1	**Program Page** programs 256B or 512B data to the memory array in one transaction.	WRENB_0_0	12 (CMD)	12 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	–	–	–	–	Figure 20 / Figure 21		
Erase Flash Array	ER004_4_0	**Erase 4-KB Sector** transaction sets all the bits of a 4 KB sector to 1 (all bytes are FFh).	WRENB_0_0	21 (CMD)	21 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–	Figure 16 / Figure 17		
	ER256_4_0	**Erase 256-KB Sector** transaction sets all the bits of a 256 KB sector to 1 (all bytes are FFh).	WRENB_0_0	DC (CMD)	DC (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–			
	ERCHP_0_0	**Erase Chip** transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array.	WRENB_0_0	60 or C7 (CMD)	60 or C7 (CMD)	–	–	–	–	–	–	–	–	–	–	–	–	Figure 14 / Figure 15		N/A
	EVERS_4_0	**Evaluate Erase Status** transaction verifies that the last erase operation on the addressed sector was completed successfully.	–	D0 (CMD)	D0 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–	Figure 16 / Figure 17		4
	SEERC_4_0	**Sector Erase Count** transaction outputs the number of erase cycles for the sector of the inputed address from the Sector Erase Count Register.	–	5D (CMD)	5D (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–			
Suspend / Resume	SPEPD_0_0	**Suspend Erase / Program / Data Integrity Check** transaction allows the system to interrupt a programming, erase or data integrity check operation	–	B0 (CMD)	B0 (CMD)	–	–	–	–	–	–	–	–	–	–	–	–	Figure 14 / Figure 15		N/A
	RSEPD_0_0	**Resume Erase / Program / Data Integrity Check** transaction allows the system to resume a programming, erase or data integrity check operation	–	30 (CMD)	30 (CMD)	–	–	–	–	–	–	–	–	–	–	–	–			

Note
20. In case of Octal DDR protocol.

Table 44. Octal (8S-8S-8S, 8D-8D-8D) Transaction Table (Continued)

Function	Transaction Name	Description	Prerequisite Transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Byte 10 (Hex)	Byte 11 (Hex)	Byte 12 (Hex)	Byte 13 (Hex)	Byte 14 (Hex)	Transaction Format (SDR/DDR)	HL-T / HS-T Max Frequency (MHz)	Address Length
				CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]	CK ↑ Edge[20]	CK ↓ Edge[20]			
Secure Silicon Region	PRSSR_4_1	**Program Secure Silicon Region** transaction programs data in 1024 bytes of Secure Silicon Region	WRENB_0_0	42 (CMD)	42 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	–	–	–	–	Figure 20 / Figure 21	166 / 200	4
	RDSSR_4_0	**Read Secure Silicon Region** transaction reads data from the SSR.	–	4B (CMD)	4B (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–	Figure 23 / Figure 24		
Advanced Sector Protection	RDDYB_4_0	**Read Dynamic Protection Bit** transaction reads the contents of the DYB Access Register.	–	E0 (CMD)	E0 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–	Figure 23 / Figure 25		4
	WRDYB_4_1	**Write Dynamic Protection Bit** transaction writes to the DYB Access Register	WRENB_0_0	E1 (CMD)	E1 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–	–	–	–	–	Figure 20 / Figure 22		
	RDPPB_4_0	**Read Persistent Protection Bit** transaction reads the contents of the PPB Access Register	–	E2 (CMD)	E2 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–	Figure 23 / Figure 25		
	PRPPB_4_0	**Program Persistent Protection Bit** transaction programs / writes the PPB Register to enable the sector protection.	WRENB_0_0	E3 (CMD)	E3 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	–	–	–	Figure 16 / Figure 17		
	ERPPB_0_0	**Erase Persistent Protection Bit** transaction sets all persistent protection bits to 1.	WRENB_0_0	E4 (CMD)	E4 (CMD)	–	–	–	–	–	–	–	–	–	–	–	–	Figure 14 / Figure 15		N/A
	WRPLB_0_0	**Write PPB Protection Lock Bit** transaction clears the PPB Lock to 0	WRENB_0_0	2C (CMD)	2C (CMD)	–	–	–	–	–	–	–	–	–	–	–	–			
	RDPLB_4_0	**Read Password Protection Mode Lock Bit** transaction shifts out the 8-bit PPB Lock Register contents with MSb first	–	2D (CMD)	2D (CMD)	00 (ADDR)	00 (ADDR)	00 (ADDR)	00 (ADDR)	–	–	–	–	–	–	–	–	Figure 23 / Figure 25		4
	PWDUL_4_1	**Password Unlock** transaction sends the 64-bit password to flash device. If the supplied password does not match the hidden password in the Password Register, the device is locked and only a hardware reset or POR will return the device to standby state, ready for new transactions such as a retry of the PWDUL_0_1. If the password does match, the PPB Lock bit is set to 1.	–	E9 (CMD)	E9 (CMD)	00 (ADDR)	00 (ADDR)	00 (ADDR)	00 (ADDR)	Password [7:0]	Password [15:8]	Password [23:16]	Password [31:24]	Password [39:32]	Password [47:40]	Password [55:48]	Password [63:56]	Figure 20 / Figure 21		N/A
Reset	SRSTE_0_0	**Software Reset Enable** command is required immediately before a SFRST_0_0 transaction	–	66 (CMD)	66 (CMD)	–	–	–	–	–	–	–	–	–	–	–	–	Figure 14 / Figure 15		
	SFRST_0_0	**Software Reset** transaction restores the device to its initial power up state, by reloading volatile registers from nonvolatile default values	SFRSE_0_0	99 (CMD)	99 (CMD)	–	–	–	–	–	–	–	–	–	–	–	–			
Deep Power Down	ENDPD_0_0	**Enter Deep Power Down Mode** transaction shifts device in the lowest power consumption mode	–	B9 (CMD)	B9 (CMD)	–	–	–	–	–	–	–	–	–	–	–	–			

Note
20. In case of Octal DDR protocol.

1.5 Device Identification

1.5.1 JEDEC SFDP Rev D

1.5.1.1 JEDEC SFDP Rev D Header Table

Table 45. JEDEC SFDP Rev D Header Table

SFDP Byte Address	SFDP DWORD Name	Data	Description
00h	SFDP Header	53h	This is the entry point for Read SFDP (5Ah) command i.e., location zero within SFDP space ASCII “S”
01h		46h	ASCII “F”
02h		44h	ASCII “D”
03h		50h	ASCII “P”
04h		08h	SFDP Minor Revision (08h = JEDEC JESD216 Revision D)
05h		01h	SFDP Major Revision (01h = JEDEC JESD216 Revision D)
06h		05h	Number of Parameter Headers (zero based, 05h = 6 parameters)
07h		FEh	xSPI NOR Profile 1 Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 8 WAIT states (Booting up in 1S-1S-1S mode)
08h	1st Parameter Header	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
09h		00h	Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)
0Ah		01h	Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)
0Bh		14h	Parameter Table Length (14h = 20 DWORDs are in the Parameter table)
0Ch		00h	Parameter Table Pointer Byte 0 (DWORD = 4 byte aligned) JEDEC Basic SPI Flash parameter byte offset = 0100h address
0Dh		01h	Parameter Table Pointer Byte 1
0Eh		00h	Parameter Table Pointer Byte 2
0Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
10h	2nd Parameter Header	84h	Parameter ID LSB (84h = 4-Byte Address Instruction Table)
11h		00h	Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)
12h		01h	Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)
13h		02h	Parameter Table Length (2h = 2 DWORDs are in the Parameter table)
14h		50h	Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) 4-Byte Address Instruction Table byte offset = 0150h address
15h		01h	Parameter Table Pointer Byte 1
16h		00h	Parameter Table Pointer Byte 2
17h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
18h	3rd Parameter Header	05h	Parameter ID LSB (05h = JEDEC xSPI Profile 1.0)
19h		00h	Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)
1Ah		01h	Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)
1Bh		05h	Parameter Table Length (5h = 5 DWORDs are in the Parameter table)
1Ch		58h	Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) JEDEC xSPI Profile 1.0 = 0158h address
1Dh		01h	Parameter Table Pointer Byte 1
1Eh		00h	Parameter Table Pointer Byte 2
1Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)

Table 45. JEDEC SFDP Rev D Header Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
20h	4th Parameter Header	87h	Parameter ID LSB (87h = JEDEC Status, Control and Configuration Register Map)
21h		00h	Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)
22h		01h	Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)
23h		1Ch	Parameter Table Length (1Ch = 28 DWORDs are in the Parameter table)
24h		6Ch	Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) JEDEC Status, Control and Configuration Register Map = 016Ch address
25h		01h	Parameter Table Pointer Byte 1
26h		00h	Parameter Table Pointer Byte 2
27h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
28h	5th Parameter Header	0Ah	Parameter ID LSB (0Ah = Command Sequences to change to Octal DDR (8D-8D-8D) mode)
29h		00h	Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)
2Ah		01h	Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)
2Bh		04h	Parameter Table Length (4h = 4 DWORDs are in the Parameter table)
2Ch		DCh	Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) Command Sequences to Change to Octal DDR (8D-8D-8D) Mode = 1DCh address
2Dh		01h	Parameter Table Pointer Byte 1
2Eh		00h	Parameter Table Pointer Byte 2
2Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
30h	6th Parameter Header	81h	Parameter ID LSB (81h = JEDEC Sector Map)
31h		00h	Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)
32h		01h	Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)
33h		16h	Parameter Table Length (16h = 22 DWORDs are in the Parameter table)
34h		ECh	Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) JEDEC Sector Map = 1ECh address
35h		01h	Parameter Table Pointer Byte 1
36h		00h	Parameter Table Pointer Byte 2
37h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)

Table 46. JEDEC SFDP Rev D Parameter Table

SFDP Byte Address	SFDP DWORD Name	Data	Description
100h	JEDEC Basic Flash Parameter DWORD-1	E7h	Bits 7:5 = unused = 111b Bit 4 = 50h is Volatile Status Register write instruction and Status Register is default = 0b Bit 3 = Block Protect Bits are nonvolatile / volatile = 0b Bit 2 = Program Buffer > 64 Bytes = 1b Bits 1:0 = Uniform 4 KB erase is unavailable = 11b
101h		21h	Bits 15:8 = 4 KB erase instruction = 21h
102h		8Ah	Bit 23 = Unused = 1b Bit 22 = (1-1-4) Fast Read NOT supported = 0b Bit 21 = (1-4-4) Fast Read NOT supported = 0b Bit 20 = (1-2-2) Fast Read NOT supported = 0b Bit19 = Supports DDR, Yes = 1b Bit 18:17 = 3- or 4-Byte addressing (for example, defaults to 3-Byte mode; enters 4-Byte mode on command) = 01b Bit 16 = (1-1-2) Fast Read NOT supported = 0b
103h		FFh	Bits 31:24 = Unused = FFh
104h	JEDEC Basic Flash Parameter DWORD-2	FFh	Density in bits, zero based, 256 Mb = 0FFFFFFFh Density in bits, zero based, 512 Mb = 1FFFFFFFh Density in bits, zero based, 1 Gb = 3FFFFFFFh
105h		FFh	
106h		FFh	
107h		0Fh for 256M 1Fh for 512M 3Fh for 1G	
108h	JEDEC Basic Flash Parameter DWORD-3	00h	Not Supported
109h		00h	
10Ah		00h	
10Bh		00h	
10Ch	JEDEC Basic Flash Parameter DWORD-4	00h	Not Supported
10Dh		00h	
10Eh		00h	
10Fh		00h	
110h	JEDEC Basic Flash Parameter DWORD-5	EEh	Bits 7:5 = Reserved = 111b Bit 4 = Not Supported = 0b Bit 3:1 = Reserved = 111b Bits 0 = Not Supported = 0b
111h		FFh	Reserved
112h		FFh	
113h		FFh	
114h	JEDEC Basic Flash Parameter DWORD-6	FFh	Reserved
115h		FFh	
116h		00h	Not Supported
117h		00h	
118h	JEDEC Basic Flash Parameter DWORD-7	FFh	Reserved
119h		FFh	
11Ah		00h	Not Supported
11Bh		00h	
11Ch	JEDEC Basic Flash Parameter DWORD-8	0Ch	Erase Type 1 Size, 4 KB erase instruction = Erase type size = 2^N (where N = 12) = 0Ch
11Dh		21h	Erase Type 1 Instruction
11Eh		00h	Erase Type 2 Not Supported
11Fh		FFh	Erase Type 2 Not Supported
120h	JEDEC Basic Flash Parameter DWORD-9	00h	Erase Type 3 Not Supported
121h		FFh	Erase Type 3 Not Supported
122h		12h	Erase Type 4 Size, 256 KB erase instruction = Erase type size = 2^N (where N = 18) = 12h
123h		DCh	Erase Type 4 Instruction

Table 46. JEDEC SFDP Rev D Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
124h	JEDEC Basic Flash Parameter DWORD-10	23h	Bits 31:30 = Erase type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 128 ms = 10b Bits 29:25 = Erase type 4 Erase, Typical time count = 00101b (typ erase time = count +1 * units = 6 * 128 ms = 768 ms) Bits 24:23 = Erase type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 22:18 = Erase type 3 Erase, Typical time count = 11111b (RFU) Bits 17:16 = Erase type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 15:11 = Erase type 2 Erase, Typical time count = 11111b (RFU) Bits 10:9 = Erase type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16ms = 01b Bits 8:4 = Erase type 1 Erase, Typical time count = 00010b (typ erase time = count +1 * units = 3 * 16 ms = 48 ms) Bits 3:0 = Count = (Max Erase time / (2 * Typical Erase time))- 1 = 0011b
125h		FAh	
126h		FFh	
127h		8Bh	
128h	JEDEC Basic Flash Parameter DWORD-11	91h	Bits 31 = Reserved = 1b Bits 30:29 = Chip Erase Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 11b (256M, 512M, and 1G) Bits 28:24 = Chip Erase Typical time count = 00001b (256M), 00011b (512M), and 00110b (1G) Bits 23:19 = Byte Program Typical Time, additional byte = 11111b Bits 18:14 = Byte Program Typical Time, first byte = 11111b Bits 13 = Page Program Typical Time unit (0: 8 µs, 1: 64 µs) = 64 µs = 1b Bits 12:8 = Page Program Typical Time Count = 01000 (typ Program time = count +1 * units = 9 * 64 µs = 576 µs) Bits 7:4 = Page Size (512B) = 2^N bytes = 1001h Bits 3:0 = Count = [Max page program time / (2 * Typical page program time)] - 1 = 0001b
129h		E8h	
12Ah		FFh	
12Bh		E1h for 256M E3h for 512M E6h for 1G	
12Ch	JEDEC Basic Flash Parameter DWORD-12	ECh	Bit 31 = Suspend and Resume supported = 0b Bits 30:29 = Suspend in-progress erase max latency units (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs) = 64 µs = 11b Bits 28:24 = Suspend in-progress erase max latency count = 00000b, max erase suspend latency = count +1 * units = 1 * 64 µs = 64 µs Bits 23:20 = Erase resume to suspend interval count = 0001b, interval = count +1 * 64 µs = 2 * 64 µs = 128 µs Bits 19:18 = Suspend in-progress program max latency units (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs) = 64 µs = 11b Bits 17:13 = Suspend in-progress program max latency count = 00000b, max erase suspend latency = count +1 * units = 1 * 64 µs = 64 µs Bits 12:9 = Program resume to suspend interval count = 0001b, interval = count +1 * 64 µs = 2 * 64 µs = 128 µs Bit 8 = Reserved = 1b Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx1xb: May not initiate a page program in the erase suspended sector size + x1xxb: May not initiate a read in the erase suspended sector size + 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1110b Bits 3:0 = Prohibited Operations During Program Suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a new page program anywhere (program nesting not permitted) + x1xxb: May not initiate a read in the program suspended page size + 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1100b
12Dh		03h	
12Eh		1Ch	
12Fh		60h	
130h	JEDEC Basic Flash Parameter DWORD-13	30h	Bits 7:0 = Program Resume Instruction = 30h
131h		B0h	Bits 15:8 = Program Suspend Instruction = B0h
132h		30h	Bits 23:16 = Erase Resume Instruction = 30h
133h		B0h	Bits 31:24 = Erase Suspend Instruction = B0h
134h	JEDEC Basic Flash Parameter DWORD-14	F7h	Bits 7:4 = RFU = Fh Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0 = ready; 1 = busy). Bits 1:0 = RFU = 11b
135h		66h	Bit 31 = DPD Supported = supported = 0 Bits 30:23 = Enter DPD Instruction = B9h Bits 22:15 = Exit DPD Instruction not supported = 00h Bits 14:13 = Exit DPD to next operation delay units = (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 64 µs = 11b Bits 12:8 = Exit DPD to next operation delay count = 00110, Exit DPD to next operation delay = (count+1) * units = (6 + 1) * 64 µs = 448 µs
136h		72h	
137h		01h	
138h	JEDEC Basic Flash Parameter DWORD-15	00h	Bits 31:24 = Reserved = FFh Bit 23 = Hold or RESET Disable = Not Supported = 0b Bits 22:0 = Not supported = 000000h
139h		00h	
13Ah		00h	
13Bh		FFh	

Table 46. JEDEC SFDP Rev D Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
13Ch	JEDEC Basic Flash Parameter DWORD-16	F9h	Bit 7 = Reserved = 1 Bits 6:0 = Volatile or Nonvolatile Register and Write Enable Instruction for Status Register 1 xxx_xxx1b: Nonvolatile Status Register 1, powers-up to last written value, use instruction 06h to enable write. + xxx_1xxxb: Nonvolatile/Volatile Status Register 1 powers-up to last written value in the nonvolatile status register, use instruction 06h to enable write to nonvolatile status register. Volatile status register may be activated after power-up to override the nonvolatile status register, use instruction 50h to enable write and activate the volatile status register. + xx1_xxxxb: Status Register 1 contains a mix of volatile and nonvolatile bits. The 06h instruction is used to enable writing of the register. + x1x_xxxxb: Reserved + 1xx_xxxxb: Reserved = 1111001b
13Dh		10h	Bits 23:14 = Not supported =000h Bits 13:8 = Soft Reset and Rescue Sequence Support + x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode. = 010000b
13Eh		00h	
13Fh		A0h	Bits 31:24 = Enter 4-byte Addressing + xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Refer the vendor datasheet for the instruction set definition + 1xxx_xxxxb: Reserved = 1010_0000b
140h	JEDEC Basic Flash Parameter DWORD-17	00h	Not Supported
141h		00h	
142h		00h	
143h		00h	
144h	JEDEC Basic Flash Parameter DWORD-18	00h	Bit 31 = High byte and low byte of 16-bit words are in the same order when read in 1-1-1 mode and 8-8-8 mode = 0b Bit 30:29 = The Command Extension is the same as the Command = 00b Bit 28 = Reserved = 0b Bit 27:26 = Not supported = 00b Bits 25:24 = First rising edge of DS in the middle of the first data bit, start of first data bit aligned with the first falling edge of DS = 10b Bit 23 = JEDEC SPI Protocol Reset Supported = 1b Bit 22:18 = 00001b xSPI Support for drive strength Bits 17:0 = Reserved = 00000h
145h		00h	
146h		84h	
147h		02h	
148h	JEDEC Basic Flash Parameter DWORD-19	00h	Not Supported
149h		00h	
14Ah		00h	
14Bh		00h	
14Ch	JEDEC Basic Flash Parameter DWORD-20	FFh	Bits 31:28 = Maximum operation speed of device in 8D-8D-8D mode when utilizing Data Strobe = 1000b (200 MHz) / 0111b (166 MHz) Bits 27:24 = 8D-8D-8D mode without using Data Strobe is not characterized = 1110b Bits 23:20 = Maximum operation speed of device in 8S-8S-8S mode when utilizing Data Strobe = 1000b (200 MHz) / 0111b (166 MHz) Bits 19:16 = 8S-8S-8S mode without using Data Strobe is not characterized = 1110b Bit 15:0 = Not supported = FFFFh
14Dh		FFh	
14Eh		8Eh for HS-T 7Eh for HL-T	
14Fh		8Eh for HS-T 7Eh for HL-T	

Table 46. JEDEC SFDP Rev D Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
150h	JEDEC 4-Byte Address Instructions Parameter DWORD-1	43h	Supported = 1, Not Supported = 0 Bits 31:25 = Reserved = 1111_111b Bit 24 = Support for (1-8-8) Page Program Command, Instruction = 8Eh = 0b Bit 23 = Support for (1-1-8) Page Program Command, Instruction = 84h = 0b Bit 22 = Support for (1-8-8) DTR READ Command, Instruction = FDh = 0b Bit 21 = Support for (1-8-8) FAST_READ Command, Instruction = CCh = 0b Bit 20 = Support for (1-1-8) FAST_READ Command, Instruction = 7Ch = 0b Bit 19 = Support for nonvolatile individual sector lock write command, Instruction = E3h = 1b Bit 18 = Support for nonvolatile individual sector lock read command, Instruction = E2h = 1b Bit 17 = Support for volatile individual sector lock Write command, Instruction = E1h = 1b Bit 16 = Support for volatile individual sector lock Read command, Instruction = E0h = 1b Bit 15 = Support for (1-4-4) DTR_Read Command, Instruction = EEh = 0b Bit 14 = Support for (1-2-2) DTR_Read Command, Instruction = BEh = 0b Bit 13 = Support for (1-1-1) DTR_Read Command, Instruction = 0Eh = 0b Bit 12 = Support for Erase Command – Type 4 = 1b Bit 11 = Support for Erase Command – Type 3 = 0b Bit 10 = Support for Erase Command – Type 2 = 0b Bit 9 = Support for Erase Command – Type 1 = 1b Bit 8 = Support for (1-4-4) Page Program Command, Instruction = 3Eh = 0b Bit 7 = Support for (1-1-4) Page Program Command, Instruction = 34h = 0b Bit 6 = Support for (1-1-1) Page Program Command, Instruction = 12h = 1b Bit 5 = Support for (1-4-4) FAST_READ Command, Instruction = ECh = 0b Bit 4 = Support for (1-1-4) FAST_READ Command, Instruction = 6Ch = 0b Bit 3 = Support for (1-2-2) FAST_READ Command, Instruction = BCh = 0b Bit 2 = Support for (1-1-2) FAST_READ Command, Instruction = 3Ch = 0b Bit 1 = Support for (1-1-1) FAST_READ Command, Instruction = 0Ch = 1b Bit 0 = Support for (1-1-1) READ Command, Instruction = 13h = 1b
151h		12h	
152h		0Fh	
153h		FEh	
154h	JEDEC 4-Byte Address Instructions Parameter DWORD-2	21h	Bits 31:24 = DCh = Instruction for Erase Type 4 Bits 23:16 = Instruction for Erase Type 3: RFU Bits 15:8 = Instruction for Erase Type 2: RFU Bits 7:0 = 21h = Instruction for Erase Type 1
155h		FFh	
156h		FFh	
157h		DCh	
158h	JEDEC xSPI Profile 1.0 DWORD-1	00h	Bits 7:0 = Read Fast Wrapped command not supported = 00h
159h		EEh	Bits 15:8 = Read Fast command = EEh (DDR Read)
15Ah		80h	Bit 23 = Number of Additional Modifier Bytes Used for Write Register command = 4 bytes = 1b Bit 22 = Number of Data Bytes Used for Write Register command = 1 byte = 0b Bits 21:16 = Reserved = 000000b
15Bh		9Bh	Bit 31 = xSPI Support, Device implements the SFDP command in 8D-8D-8D protocol mode as defined in the Jedec xSPI spec = 1b Bit 30 = SFDP Command in 8D-8D-8D mode – Dummy Cycles = 8 bytes = 0b Bit 29 = Number of Additional Modifier Bytes Used for Read Status Register command = 0 bytes = 0b Bit 28 = Initial Latency (CK cycles) for Read Status Register command = 8 CK cycles = 1b Bit 27 = Number of Additional Modifier Bytes Used for Read Register command = 4 bytes = 1b Bit 26 = Initial Latency (CK cycles) for Read Volatile Register command = 4CK = 0b Bit 25 = Initial Latency (CK cycles) for Read Volatile Non-Register command = 8 CK cycles = 1b Bit 24 = Number of Additional Modifier Bytes Used for Write Status-Cfg Register command= 4 bytes = 1b
15Ch	JEDEC xSPI Profile 1.0 DWORD-2	00h	Write Nonvolatile Register command not supported
15Dh		00h	Write Volatile Register command not supported
15Eh		00h	Read NV Register command not supported
15Fh		00h	Read Volatile Register command not supported

Table 46. JEDEC SFDP Rev D Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
160h	JEDEC xSPI Profile 1.0 DWORD-3	00h	Bits 7:0 = Reserved = 00h
161h		B0h	Bit 31 = Read SFDP 8D-8D-8D command supported = 1b Bit 30 = Read Fast Wrapped command not supported = 0b Bit 29 = Setup Read Wrap command not supported = 0b Bit 28 = Erase 4 KB command supported = 1b Bit 27 = Erase 32 KB command not supported = 0b Bit 26 = Erase Chip command supported = 1b Bit 25 = Read Configuration Register command not supported = 0b Bit 24 = Read Flag Status Register command supported = 1b Bit 23 = Read Register command supported = 1b Bit 22 = Read Volatile Register command not supported = 0b Bit 21 = Read NV Register command not supported = 0b Bit 20 = Write Status-Configuration Register command not supported = 0b Bit 19 = Clear Flag Status Reg command supported = 1b Bit 18 = Write Register command supported = 1b Bit 17 = Write volatile register command not supported = 0b Bit 16 = Write NV register command not supported = 0b Bit 15 = Enter Deep Power Down command not supported = 1b Bit 14 = Exit Deep Power Down command not supported = 0b Bit 13 = Soft Reset command supported = 1b Bit 12 = Reset Enable command supported = 1b Bit 11 = Soft Reset and Enter default protocol mode command supported = 0b Bit 10 = Enter default protocol mode command not supported = 0b Bits 9:8 = Reserved = 00b
162h		8Ch	
163h		95h	
164h	JEDEC xSPI Profile 1.0 DWORD-4	A8h	Bits 31:12 = 00000h Bits 11:7 = 200 MHz operation: number of dummy cycles required = 23 = 10111b Bit 6:2 = 200 MHz operation: configuration bit pattern to set this number of dummy cycles = 01010b Bits 1:0 = Reserved = 00b
165h		0Bh	
166h		00h	
167h		00h	
168h	JEDEC xSPI Profile 1.0 DWORD-5	0Ch	Bits 31:27 = 166 MHz operation: number of dummy cycles required = 20 = 10100b Bit 26:22 = 166 MHz operation: configuration bit pattern to set this number of dummy cycles = 01000b Bits 21:17 = 133 MHz operation: number of dummy cycles required = 14 = 01110b Bit 16:12 = 133 MHz operation: configuration bit pattern to set this number of dummy cycles = 00101b Bits 11:7 = 100 MHz operation: number of dummy cycles required = 10 = 01010b Bit 6:2 = 100 MHz operation: configuration bit pattern to set this number of dummy cycles = 00011b Bits 1:0 = Reserved = 00b
169h		55h	
16Ah		1Ch	
16Bh		A2h	
16Ch	Status, Control and Configuration Register Map DWORD-1	00h	Bits 31:0 = Address offset for volatile registers = 00800000h
16Dh		00h	
16Eh		80h	
16Fh		00h	
170h	Status, Control and Configuration Register Map DWORD-2	00h	Bits 31:0 = Address offset for nonvolatile registers = 00000000h
171h		00h	
172h		00h	
173h		00h	
174h	Status, Control and Configuration Register Map DWORD-3	C0h	Bit 31 = Generic Addressable Read Status/Control register command for volatile registers supported for some (or all) registers = 1b Bit 30 = Generic Addressable Write Status/Control register command for volatile registers supported for some (or all) registers = 1b Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for volatile registers = 3 byte (default) = 10b Bit 27:26 = Number of dummy bytes used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 10b Bit 25:14 = Not supported = FFFh Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (8S-8S-8S) mode = 3 = 0011b Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (8D-8D-8D) mode = 3 = 0011b Bit 5:4 = Reserved = 00b Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 0000b
175h		CCh	
176h		FFh	
177h		EBh	

Table 46. JEDEC SFDP Rev D Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
178h	Status, Control and Configuration Register Map DWORD-4	88h	Bit 31 = Generic Addressable Read Status/Control register command for nonvolatile registers supported for some (or all) registers = 1b Bit 30 = Generic Addressable Write Status/Control register command for nonvolatile registers supported for some (or all) registers = 1b Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for nonvolatile registers = 3 byte (default) = 10b Bit 27:26 = Number of dummy bytes used for Generic Addressable Read Status/Control register command for nonvolatile registers in (1S-1S-1S) mode = 10b Bit 25:14 = Not supported = FFFh Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for nonvolatile registers in (8S-8S-8S) mode = 20 = 1110b (Max available option is 14 cycles) Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for nonvolatile registers in (8D-8D-8D) mode = 20 = 1110b (Max available option is 14 cycles) Bit 5:4 = Reserved = 00b Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for nonvolatile registers in (1S-1S-1S) mode = 1000b
179h		FBh	
17Ah		FFh	
17Bh		EBh	
17Ch	Status, Control and Configuration Register Map DWORD-5	00h	Bits 7:0 = Command used for write access = read only = 00h
17Dh		65h	Bits 15:8 = Command used for read access = 65h
17Eh		00h	Bits 23:16 = Address of register where WIP is located = 00h (status reg -1 volatile)
17Fh		90h	Bit 31 = Write In Progress (WIP) bit is supported = 1b Bit 30 = Write In Progress polarity, WIP = 1 indicates write is in progress = 0b Bits 29 = Reserved = 0b Bits 28 = Bit is set /cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of WIP bit in register = bit [0] = 000b
180h	Status, Control and Configuration Register Map DWORD-6	06h	Bits 7:0 = Command used for write access
181h		05h	Bits 15:8 = Command used for read access
182h		00h	Bits 23:16 = Address of register where WEL is located = 00h (status reg -1 volatile)
183h		A1h	Bit 31 = Write Enable (WEL) bit is supported = 1b Bit 30 = Write Enable polarity, WEL = 1 means write is in progress = 0b Bits 29 = Write command is a direct command to wet WEL bit = 1b Bits 28 = Bit is accessed by direct commands to set WEL bit = 1b Bit 27 = Local address for WEL bit is found in last byte of the address = 0b Bits 26:24 = Bit location of WEL bit in register = bit [1] = 001b
184h	Status, Control and Configuration Register Map DWORD-7	00h	Bits 7:0 = Command used for write access = read only = 00h = Read Only
185h		65h	Bits 15:8 = Command used for read access = 65h
186h		00h	Bits 23:16 = Address of register where Program Error is located = 00h (status reg -1 volatile)
187h		96h	Bit 31 = Program Error bit supported = 1b Bit 30 = Positive polarity (Program Error = 0 indicates no error, Program Error = 1 indicates last Program operation created an error) = 0b Bit 29 = The device has separate bits for Program Error and Erase Error = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not Supported = 0b Bits 26:24 = Bit location of Program Error bit in register = bit [6] = 110b
188h	Status, Control and Configuration Register Map DWORD-8	00h	Bits 7:0 = Command used for write access = read only = 00h = Read Only
189h		65h	Bits 15:8 = Command used for read access = 65h
18Ah		00h	Bits 23:16 = Address of register where Erase Error is located = 00h
18Bh		95h	Bit 31 = Erase Error bit supported = 1b Bit 30 = Positive polarity Erase Error = 0 indicates no error, Erase Error = 1 indicates last erase operation created an error) = 0b Bit 29 = The device has separate bits for Program Error and Erase Error = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not Supported = 0b Bits 26:24 = Bit location of erase Error bit in register = bit [5] = 101b
18Ch	Status, Control and Configuration Register Map DWORD-9	71h	Bits 7:0 = Command used for write access = read only = 71h
18Dh		65h	Bits 15:8 = Command used for read access = 65h
18Eh		04h	Address of register where wait states bits are located = 04h (Configuration Reg - 3 volatile)
18Fh		97h	Bit 31 = Variable number of dummy cycles supported = 1b Bits 30:29 = Number of physical bits used to set wait states - 2 bit = 00b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not Supported = 0b Bits 26:24 = Bit location of LSB of physical bits in register = bit [7] = 111b

Table 46. JEDEC SFDP Rev D Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
190h	Status, Control and Configuration Register Map DWORD-10	71h	Bits 7:0 = Command used for write access = 71h
191h		65h	Bits 15:8 = Command used for read access = 65h
192h		03h	Address of register where wait states bits are located = 03h (Configuration Reg - 2 nonvolatile)
193h		D0h	Bit 31 = Variable number of dummy cycles supported = 1b Bits 30:29 = Number of physical bits used to set wait states - 4 bit = 10b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not Supported = 0b Bits 26:24 = Bit location of LSB of physical bits in register = bit [0] = 000b
194h	Status, Control and Configuration Register Map DWORD-11	A4h	Bit 31 = 30 dummy cycles supported = 0b Bit 30:26 = Bit pattern used to set 30 dummy cycles = 00000b Bit 25 = 28 dummy cycles supported = 1b Bit 24:20 = Bit pattern used to set 28 dummy cycles = 01111b Bit 19 = 26 dummy cycles supported = 1b Bit 18:14 = Bit pattern used to set 26 dummy cycles = 01101b Bit 13 = 24 dummy cycles supported = 1b Bit 12:8 = Bit pattern used to set 24 dummy cycles = 01011b Bit 7 = 22 dummy cycles supported = 1b Bit 6:2 = Bit pattern used to set 22 dummy cycles = 01001b Bits 1:0 = Reserved = 00b
195h		6Bh	
196h		FBh	
197h		02h	
198h	Status, Control and Configuration Register Map DWORD-12	90h	Bit 31 = 20 dummy cycles supported = 1b Bit 30:26 = Bit pattern used to set 20 dummy cycles = 01000b Bit 25 = 18 dummy cycles supported = 1b Bit 24:20 = Bit pattern used to set 18 dummy cycles = 00111b Bit 19 = 16 dummy cycles supported = 1b Bit 18:14 = Bit pattern used to set 16 dummy cycles = 00110b Bit 13 = 14 dummy cycles supported = 1b Bit 12:8 = Bit pattern used to set 14 dummy cycles = 00101b Bit 7 = 12 dummy cycles supported = 1b Bit 6:2 = Bit pattern used to set 12 dummy cycles = 00100b Bits 1:0 = Reserved = 00b
199h		A5h	
19Ah		79h	
19Bh		A2h	
19Ch	Status, Control and Configuration Register Map DWORD-13	00h	Bit 31 = 10 dummy cycles supported = 1b Bit 30:26 = Bit pattern used to set 10 dummy cycles = 00011b Bit 25 = 8 dummy cycles supported = 1b Bit 24:20 = Bit pattern used to set 8 dummy cycles = 00010b Bit 19 = 6 dummy cycles supported = 1b Bit 18:14 = Bit pattern used to set 6 dummy cycles = 00001b Bit 13 = 4 dummy cycles supported = 0b Bit 12:8 = Bit pattern used to set 4 dummy cycles = 00000b Bit 7 = 2 dummy cycles supported = 0b Bit 6:2 = Bit pattern used to set 2 dummy cycles = 00000b Bits 1:0 = Reserved = 00b
19Dh		40h	
19Eh		28h	
19Fh		8Eh	
1A0h	Status, Control and Configuration Register Map DWORD-14	00h	Not Supported
1A1h		00h	
1A2h		FFh	
1A3h		00h	
1A4h	Status, Control and Configuration Register Map DWORD-15	00h	Not Supported
1A5h		00h	
1A6h		FFh	
1A7h		00h	
1A8h	Status, Control and Configuration Register Map DWORD-16	71h	Bits 7:0 = Command used for write access = 71h
1A9h		65h	Bits 15:8 = Command used for read access = 65h
1AAh		06h	Bits 23:16 = Address of register where Octal Mode Enable volatile bit is located = 800006h (Configuration Reg - 5 volatile)
1ABh		90h	Bit 31 = Octal Mode Enable volatile bit supported = 1b Bits 30 = Octal Mode Enable volatile bit polarity: Positive (Octal Mode Enable bit = 1 indicates Octal mode is enabled) = 0b Bits 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of Octal Mode enable bit in register = bit [0] = 000b

Table 46. JEDEC SFDP Rev D Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
1ACh	Status, Control and Configuration Register Map DWORD-17	71h	Bits 7:0 = Command used for write access = 71h
1ADh		65h	Bits 15:8 = Command used for read access = 65h
1AEh		06h	Address of register where Octal Mode Enable nonvolatile bit is located = 06h (Configuration Reg - 5 nonvolatile)
1AFh		90h	Bit 31 = Octal Mode Enable nonvolatile bit supported = 1b Bits 30 = Octal Mode Enable nonvolatile bit polarity: Positive (Octal Mode Enable bit = 1 indicates Octal mode is enabled) = 0b Bit 29 = No OTP Bit = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of Octal Mode enable bit in register = bit [0] = 000b
1B0h	Status, Control and Configuration Register Map DWORD-18	00h	Not Supported
1B1h		00h	
1B2h		00h	
1B3h		00h	
1B4h	Status, Control and Configuration Register Map DWORD-19	00h	Not Supported
1B5h		00h	
1B6h		00h	
1B7h		00h	
1B8h	Status, Control and Configuration Register Map DWORD-20	71h	Bits 7:0 = Command used for write access = 71h
1B9h		65h	Bits 15:8 = Command used for read access = 65h
1BAh		06h	Address of register where STR Octal Mode Enable bit is located = 800006h (Configuration Reg - 5 Volatile)
1BBh		D1h	Bit 31 = STR Octal Mode Enable volatile bit supported = 1b Bits 30 = STR Octal Mode Enable volatile bit polarity: Inverted (STR Octal Mode Enable = 0 indicates STR Octal Mode is enabled) = 1b Bit 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of STR Octal Mode Enable bit in register = bit [1] = 001b
1BCh	Status, Control and Configuration Register Map DWORD-21	71h	Bits 7:0 = Command used for write access = 71h
1BDh		65h	Bits 15:8 = Command used for read access = 65h
1BEh		06h	Address of register where STR Octal Mode Enable bit is located = 06h (Configuration Reg - 5 Nonvolatile)
1BFh		D1h	Bit 31 = STR Octal Mode Enable nonvolatile bit supported = 1b Bits 30 = STR Octal Mode Enable nonvolatile bit polarity: Inverted (STR Octal Mode Enable = 0 indicates STR Octal Mode is enabled) = 1b Bit 29 = No OTP Bit = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of STR Octal Mode Enable nonvolatile bit in register = bit [1] = 001b
1C0h	Status, Control and Configuration Register Map DWORD-22	71h	Bits 7:0 = Command used for write access = 71h
1C1h		65h	Bits 15:8 = Command used for read access = 65h
1C2h		06h	Address of register where DTR Octal Mode Enable volatile bit is located = 800006h (Configuration Reg - 5 Volatile)
1C3h		91h	Bit 31 = DTR Octal Mode Enable volatile bit supported = 1b Bits 30 = DTR Octal Mode Enable volatile bit polarity positive (DSTR Octal Mode Enable = 1 indicates DTR Octal Mode is enabled) = 0b Bit 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of DTR Octal Mode Enable volatile bit in register = bit [1] = 001b
1C4h	Status, Control and Configuration Register Map DWORD-23	71h	Bits 7:0 = Command used for write access = 71h
1C5h		65h	Bits 15:8 = Command used for read access = 65h
1C6h		06h	Address of register where DTR Octal Mode Enable nonvolatile bit is located = 06h (Configuration Reg - 5 nonvolatile)
1C7h		91h	Bit 31 = DTR Octal Mode Enable nonvolatile bit supported = 1b Bits 30 = DTR Octal Mode Enable nonvolatile bit polarity positive (DSTR Octal Mode Enable = 1 indicates DTR Octal Mode is enabled) = 0b Bit 29 = No OTP Bit = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of DTR Octal Mode Enable bit in register = bit [1] = 001b

Table 46. JEDEC SFDP Rev D Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
1C8h	Status, Control and Configuration Register Map DWORD-24	00h	Not Supported
1C9h		00h	
1CAh		FFh	
1CBh		00h	
1CCh	Status, Control and Configuration Register Map DWORD-25	00h	Not Supported
1CDh		00h	
1CEh		FFh	
1CFh		00h	
1D0h	Status, Control and Configuration Register Map DWORD-26	71h	Bits 7:0 = Command used for write access = 71h
1D1h		65h	Bits 15:8 = Command used for read access = 65h
1D2h		05h	Address of register where Output Driver Strength volatile bits are located = 800005h (Configuration Reg - 4 Volatile)
1D3h		D7h	Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b Bit 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not Supported = 0b Bits 26:24 = Bit location of Most Significant Output Driver Strength bit in register = bit [7] = 111b
1D4h	Status, Control and Configuration Register Map DWORD-27	71h	Bits 7:0 = Command used for write access = 71h
1D5h		65h	Bits 15:8 = Command used for read access = 65h
1D6h		05h	Address of register where Output Driver Strength nonvolatile bits are located = 05h (Configuration Reg - 4 non- volatile)
1D7h		D7h	Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b Bit 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not Supported = 0b Bits 26:24 = Bit location of Most Significant Output Driver Strength bit in register = bit [7] = 111b
1D8h	Status, Control and Configuration Register Map DWORD-28	00h	Bit 7:0 = Reserved = 00h
1D9h		00h	Bit 15:8 = Reserved = 00h
1DAh		EEh	Bits 31:29 = Bit pattern to support Driver type 0 = 60 Ohms = 011b Bits 28:26 = Bit pattern to support Driver type 1 = 45 Ohms = 100b Bits 25:23 = Bit pattern to support Driver type 2 = 30 Ohms = 101b Bits 22:20 = Bit pattern to support Driver type 3 = 20 Ohms = 110b Bits 19:17 = Bit pattern to support Driver type 4 = 15 Ohms = 111b Bit 16 = Reserved = 0b
1DBh		72h	
1DCh	Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD -1	00h	Bits 7:0 = Byte 3 of first command sequence
1DDh		00h	Bits 15:8 = Byte 2 of first command sequence
1DEh		06h	Bits 23:16 = Byte 1 of first command sequence
1DFh		01h	Bits 24:31 = Length of first command sequence = 1 byte
1E0h	Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD -2	00h	Bits 7:0 = Byte 7 of first command sequence
1E1h		00h	Bits 15:8 = Byte 6 of first command sequence
1E2h		00h	Bits 23:16 = Byte 5 of first command sequence
1E3h		00h	Bits 24:31 = Byte 4 of first command sequence
1E4h	Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD -3	80h	Bits 7:0 = Byte 3 of second command sequence - volatile register address
1E5h		00h	Bits 15:8 = Byte 2 of second command sequence - volatile register address
1E6h		71h	Bits 23:16 = Byte 1 of second command sequence
1E7h		06h	Bits 24:31 = Length of second command sequence = 6 bytes
1E8h	Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD -4	00h	Bits 7:0 = Byte 7 of second command sequence
1E9h		03h	Bits 15:8 = Byte 6 of second command sequence
1EAh		06h	Bits 23:16 = Byte 5 of second command sequence - volatile register address
1EBh		00h	Bits 24:31 = Byte 4 of second command sequence - volatile register address

Sector Map Parameter Table Notes

Table 47 provides a means to identify how the device address map is configured and provides a sector map for each supported configuration. This is done by defining a sequence of commands to read out the relevant configuration register bits that affect the selection of an address map. When more than one configuration bit must be read, all the bits are concatenated into an index value that is used to select the current address map.

To identify the sector map configuration in device the following configuration bits are read in the following MSb to LSb order to form the configuration map index value:

- CFR3N[3] - 0 = Hybrid Architecture, 1 = Uniform Architecture
- CFR1N[2] - 0 = 4-KB parameter sectors at bottom, 1 = 4-KB sectors at top
- CFR1N[6] - 0 = 4-KB parameter grouped together, 1 = 4-KB sectors split between bottom and top
- The value of some configuration bits may make other configuration bit values not relevant (don't care), hence not all possible combinations of the index value define valid address maps. Only selected configuration bit combinations are supported by the SFDP Sector Map Parameter table (see Table 48). Other combinations must not be used in configuring the sector address map when using this SFDP parameter table to determine the sector map. The following index value combinations are supported.

Table 47. Sector Map Parameter

CFR3N[3]	CFR1N[2]	CFR1N[6]	Index Value	Description
0	0	0	00h	4-KB sectors at bottom with remainder 256-KB sectors
0	1	0	03h	4-KB sectors at top with remainder 256-KB sectors
0	X	1	01h	4-KB sectors split between top and bottom with remainder 256-KB sectors
1	X	X	04h	Uniform 256-KB sectors

Table 48. JEDEC SFDP Rev D, Sector Map Parameter Table

SFDP Byte Address	SFDP DWORD Name	Data	Description
1ECh	JEDEC Sector Map Parameter DWORD-1 Config. Detect-1	FCh	Config. Detect -1 Uniform 256 KB Sectors or Hybrid Sectors Bits 31:24 = Read data mask = 0000_1000b: Select bit 3 of the data byte for UNHYSA value 0 = Hybrid map with 4 KB parameter sectors 1= Uniform map Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = Not the end descriptor = 0
1EDh		65h	
1EEh		FFh	
1EFh		08h	
1F0h	JEDEC Sector Map Parameter DWORD-2 Config. Detect-1	04h	Bits 31:0 = Address Value Configuration Register 3 (bit 3) = 00800004h
1F1h		00h	
1F2h		80h	
1F3h		00h	
1F4h	JEDEC Sector Map Parameter DWORD-3 Config. Detect-2	FCh	Config. Detect-2 4 KB Hybrid Sectors Split between Top and Bottom Bits 31:24 = Read data mask = 0100_0000b: Select bit 6of the data byte for SP4KBS value 0 = 4 KB parameter sectors are grouped together 1 = 4 KB parameter sectors are split between High and Low Addresses Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = Not the end descriptor = 0
1F5h		65h	
1F6h		FFh	
1F7h		40h	
1F8h	JEDEC Sector Map Parameter DWORD-4 Config. Detect-2	02h	Bits 31:0 = Address Value Configuration Register 1 (bit 6)= 00800002h
1F9h		00h	
1FAh		80h	
1FBh		00h	
1FCh	JEDEC Sector Map Parameter DWORD-5 Config. Detect-3	FDh	Config Detect-3 4 KB Hybrid Sectors on Top or Bottom Bits 31:24 = Read data mask = 0000_0100b: Select bit 2 of the data byte for TB4KBS value 0 = 4 KB parameter sectors at bottom 1 = 4 KB parameter sectors at top Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = Not the end descriptor = 1
1FDh		65h	
1FEh		FFh	
1FFh		04h	
200h	JEDEC Sector Map Parameter DWORD-6 Config. Detect-3	02h	Bits 31:0 = Address Value Configuration Register 1 (bit 2)= 00800002h
201h		00h	
202h		80h	
203h		00h	
204h	JEDEC Sector Map Parameter DWORD-7 Config-0 Header	FEh	Configuration Index 00h 4 KB sectors at bottom with remainder 256 KB Bits 31:24 = RFU = FFh Bits 23:16 = Region count (DWORDs -1) = 02h: Three regions Bits 15:8 = Configuration ID = 00h, 4 KB sectors bottom with remainder 256 KB Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = Not the end descriptor = 0
205h		00h	
206h		02h	
207h		FFh	

Table 48. JEDEC SFDP Rev D, Sector Map Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
208h	JEDEC Sector Map Parameter DWORD-8 Config-0 Region-0	F1h	Region 0 of 4 KB sectors Bits 31:8 = Region size (32 4 KB) = 0001F3h: Region size as count-1 of 256 Byte units = 32 x 4 KB sectors = 128 KB Count = 128 KB/256 = 500, value = count -1 = 500-1 = 499 = 1F3h Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region
209h		F3h	
20Ah		01h	
20Bh		00h	
20Ch	JEDEC Sector Map Parameter DWORD-9 Config-0 Region-1	F8h	Region 1 of 128 KB sector Bits 31:8 = Region size = 0001F3h: Region size as count-1 of 256 Byte units = 1 x 128 KB sectors = 128 KB Count = 128 KB/256 = 500, value = count -1 = 500-1 = 499 = 1F3h Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 128 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region
20Dh		F3h	
20Eh		01h	
20Fh		00h	
210h	JEDEC Sector Map Parameter DWORD-10 Config-0 Region-2	F8h	Region 2 Uniform 256 KB sectors Bits 31:8 = 512 Mb device Region size = 03E417h: Region size as count-1 of 256 Byte units = 255 x 256 KB sectors = 65,280KB Count = 65,280KB/256 = 255,000 value = count -1 = 255,000-1 = 254,999= 3E417h Bits 31:8 = 1 Gb device Region size = 01FEFFh: Region size as count-1 of 256 Byte units = 511 x 256 KB sectors = 130,816 KB Count = 130,816 KB/256 = 511,000, value = count -1 = 511,000-1 = 510,999 = 7CC17h Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region
211h		17h	
212h		E4h(512 Mb) CCh (1 Gb)	
213h		03h (512 Mb) 07h (1 Gb)	
214h	JEDEC Sector Map Parameter DWORD-11 Config-3 Header	FEh	Configuration Index 03h 4 KB sectors at Top with remainder 256 KB Bits 31:24 = RFU = FFh Bits 23:16 = Region count (DWORDs -1) = 02h: Three regions Bits 15:8 = Configuration ID = 03h: 4 KB sectors at top with remainder 256 KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = Not the end descriptor = 0
215h		03h	
216h		02h	
217h		FFh	
218h	JEDEC Sector Map Parameter DWORD-12 Config-3 Region-0	F8h	Region 0 Uniform 256 KB sectors Bits 31:8 = 512 Mb device Region size = 03E417h: Region size as count-1 of 256 Byte units = 255 x 256 KB sectors = 65,280KB Count = 65,280KB/256 = 255,000 value = count -1 = 255,000-1 = 254,999 = 3E417h Bits 31:8 = 1 Gb device Region size = 01FEFFh: Region size as count-1 of 256 Byte units = 511 x 256 KB sectors = 130,816KB Count = 130,816 KB/256 = 511,000, value = count -1 = 511,000-1 = 510,999 = 7CC17h Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region
219h		17h	
21Ah		E4h(512 Mb) CCh (1 Gb)	
21Bh		03h (512 Mb) 07h (1 Gb)	

Table 48. JEDEC SFDP Rev D, Sector Map Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
21Ch	JEDEC Sector Map Parameter DWORD-13 Config-3 Region-1	F8h	Region 1 of 128 KB sector Bits 31:8 = Region size = 0001F3h: Region size as count-1 of 256 Byte units = 1 x 128 KB sectors = 128 KB Count = 128 KB/256 = 500, value = count -1 = 500-1 = 499 = 1F3hBits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 128 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region
21Dh		F3h	
21Eh		01h	
21Fh		00h	
220h	JEDEC Sector Map Parameter DWORD-14 Config-3 Region-2	F1h	Region 2 of 4 KB sectors Bits 31:8 = Region size (32 4 KB) = 0001F3h: Region size as count-1 of 256 Byte units = 32 x 4 KB sectors = 128 KB Count = 128 KB/256 = 500, value = count -1 = 500-1 = 499 = 1F3h Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region
221h		F3h	
222h		01h	
223h		00h	
224h	JEDEC Sector Map Parameter DWORD-15 Config-1 Header	FEh	Configuration Index 01h 4 KB sectors split between Bottom and Top with remainder 256 KB Bits 31:24 = RFU = FFh Bits 23:16 = Region count (DWORDs -1) = 04h: Five regions Bits 15:8 = Configuration ID = 01h: 4 KB sectors split between bottom and top with remainder 256 KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = Not the end descriptor = 0
225h		01h	
226h		04h	
227h		FFh	
228h	JEDEC Sector Map Parameter DWORD-16 Config-1 Region-0	F1h	Region 0 of 4 KB sectors Bits 31:8 = Region size (32 4 KB) = 0001F3h: Region size as count-1 of 256 Byte units = 32 x 4 KB sectors = 128 KB Count = 128 KB/256 = 500, value = count -1 = 500-1 = 499 = 1F3h Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region
229h		F3h	
22Ah		01h	
22Bh		00h	
22Ch	JEDEC Sector Map Parameter DWORD-17 Config-1 Region-1	F8h	Region 1 of 192 KB sector Bits 31:8 = Region size = 0002EDh: Region size as count-1 of 256 Byte units = 1 x 192 KB sectors = 192 KB Count = 192 KB/256 = 750, value = count -1 = 750-1 = 749 = 2EDh Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 192 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region
22Dh		EDh	
22Eh		02h	
22Fh		00h	
230h	JEDEC Sector Map Parameter DWORD-18 Config-1 Region-2	F8h	Region 2 Uniform 256 KB sectors Bits 31:8 = 512 Mb device Region size = 03E02Fh: Region size as count-1 of 256 Byte units = 254 x 256 KB sectors = 65,024 KB Count = 65,024 KB/256 = 254,000 value = count -1 = 254,000-1 = 253,999 = 3E02Fh Bits 31:8 = 1 Gb device Region size = 07C82Fh: Region size as count-1 of 256 Byte units = 510 x 256 KB sectors = 130,560 KB Count = 130,560 KB/256 = 510,000, value = count -1 = 510,000-1 = 509,999 = 7C82Fh Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region
231h		2Fh	
232h		E0h (512 Mb) C8h (1 Gb)	
233h		03h (512 Mb) 07h (1 Gb)	

Table 48. JEDEC SFDP Rev D, Sector Map Parameter Table (Continued)

SFDP Byte Address	SFDP DWORD Name	Data	Description
234h	JEDEC Sector Map Parameter DWORD-19 Config-1 Region-3	F8h	Region 3of 192 KB sector Bits 31:8 = Region size = 0002EDh: Region size as count-1 of 256 Byte units = 1 x 192 KB sectors = 192 KB Count = 192 KB/256 = 750, value = count -1 = 750-1 = 749 = 2EDh Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 192 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 22 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region
235h		EDh	
236h		02h	
237h		00h	
238h	JEDEC Sector Map Parameter DWORD-20 Config-1 Region-5	F1h	Region 5 of 4 KB sectors Bits 31:8 = Region size (32 4 KB) = 0001F3h: Region size as count-1 of 256 Byte units = 32 x 4 KB sectors = 128 KB Count = 128 KB/256 = 500, value = count -1 = 500-1 = 499 = 1F3h Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region
239h		F3h	
23Ah		01h	
23Bh		00h	
23Ch	JEDEC Sector Map Parameter DWORD-21 Config-4 Header	FFh	Configuration Index 04h Uniform 256 KB sectors Bits 31:24 = RFU = FFh Bits 23:16 = Region count (DWORDs -1) = 00h: One region Bits 15:8 = Configuration ID = 04h: Uniform 256 KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 1= Not the end descriptor = 0
23Dh		04h	
23Eh		00h	
23Fh		FFh	
240h	JEDEC Sector Map Parameter DWORD-22 Config-4 Region-0	F8h	Region 0 Uniform 256 KB sectors Bits 31:8 = 512 Mb device Region size = 03E7FFh: Region size as count-1 of 256 Byte units = 256 x 256 KB sectors = 65,536KB Count = 65,280KB/256 = 256,000 value = count -1 = 256,000-1 = 255,999= 3E7FFh Bits 31:8 = 1 Gb device Region size = 07CFFFh: Region size as count-1 of 256 Byte units = 512 x 256 KB sectors = 131,072 KB Count = 131,072 KB/256 = 512,000, value = count -1 = 512,000-1 = 511,999 = 7CFFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region
241h		FFh	
242h		E7h(512 Mb) CFh (1 Gb)	
243h		03h (512 Mb) 07h (1 Gb)	

1.5.2 Manufacturer and Device ID

Table 49. Manufacturer and Device ID

Byte Address	Data	Description
00h	34h	Manufacturer ID for Cypress
01h	5Ah (HL-T) / 5Bh (HS-T)	Device ID MSB - Memory Interface Type
02h	19h (256 Mb) / 1Ah (512 Mb) / 1Bh (1 Gb)	Device ID LSB - Density
03h	0Fh	ID Length - number bytes following. Adding this value to the current location of 03h gives the address of the last valid location in the ID legacy address map.
04h	03h (Default Configuration)	Physical Sector Architecture The HS/L-T family may be configured with or without 4 KB parameter sectors in addition to the uniform sectors. 03h = Uniform 256 KB with thirty-two 4 KB Parameter Sectors)
05h	90h (HL-T/HS-T Family)	Family ID
06h - 0Fh	FFh	Reserved

1.5.3 Unique Device ID

Table 50. Unique Device ID

Byte Address	Data	Description
00h to 07h	8-Byte Unique Device ID	64-bit unique ID number

Revision History

Document Revision History

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Revision	**ECN#**	**Issue Date**	**Description of Change**
**	6696705	Oct 12, 2019	New development guide.