SLE 66R01xx

Wafer specification

Document release reference: Z8F50812207-E

About this document

Scope and purpose

This document describes the SLE 66R01xx chip layout and provides product-specific data and information about the production sites.

The document is only valid in combination with the latest version of the general issue of the chip delivery specification for wafer (document number: Z8F50306400).

Intended audience

This document is intended for Infineon partners and customers who further process sawn wafers delivered by Infineon Technologies.

Important notes

It is intended for use in SMD or in stacked die packages only.

Infineon ICs are extensively tested, but failure mechanisms according to chip-package interaction or solely package-related need to be evaluated and qualified by wafer/bare die customers. Refer to [1] and [2] accordingly.

This product will be provided exclusively inkless.

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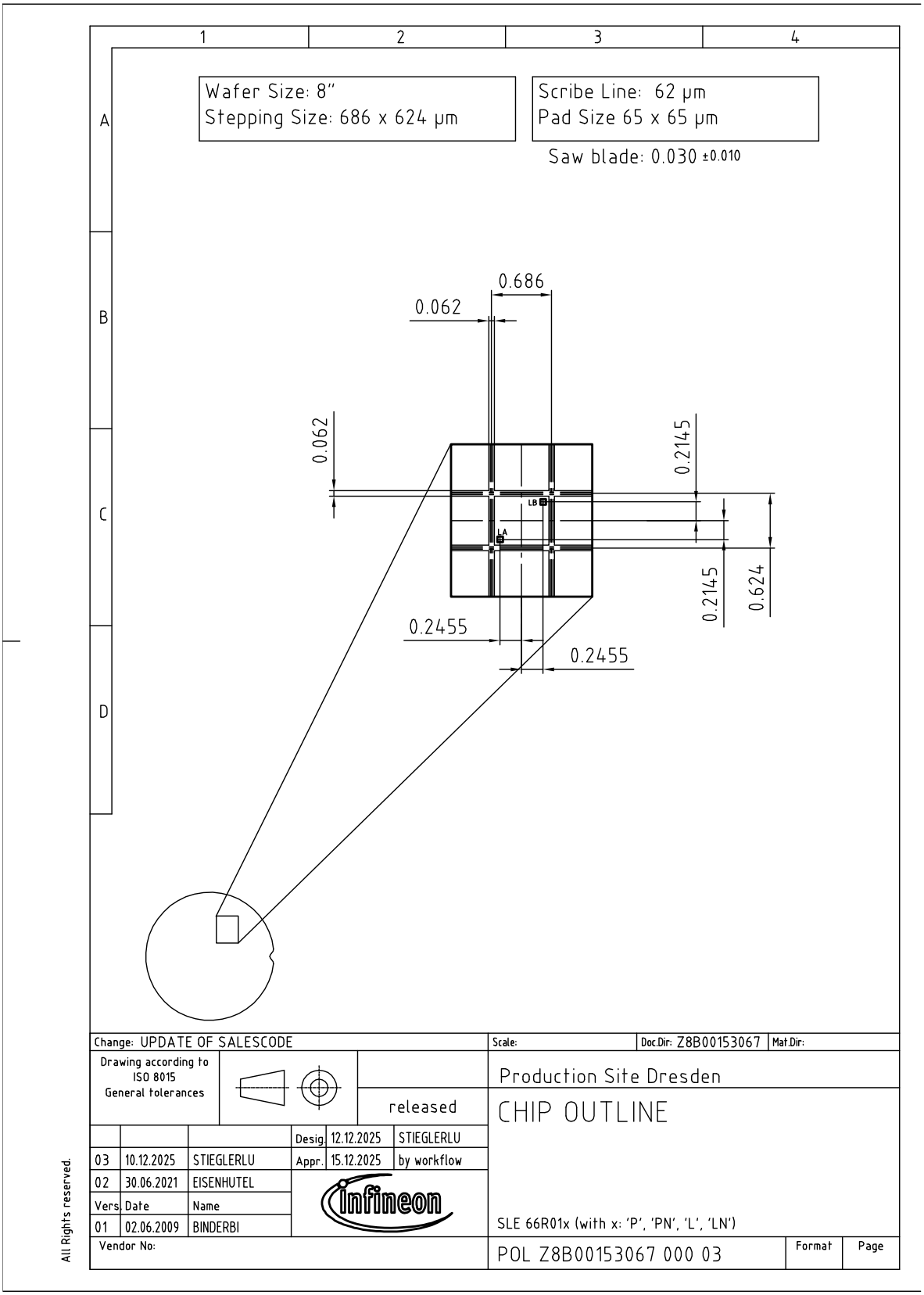
1 Overview of wafer characteristics

Table 1 Location: Dresden

Chip features	Description
Lot number coding	ZA...
Type	A
Stepping size	0.686 mm x 0.624 mm
Chip thickness[1)]	120 µm
Scribe line	62 µm
Possible systems on wafer	68,889
Pad metallization material on front	AlCu
Pad metallization thickness on front	650 nm ± 100 nm
Passivation material and thickness	Plasmaoxide/Plasmanitride: 650 nm ± 100 nm Photoimide: 2.5 µm ± 0.5 µm
Bonding area pad size	See chip layout
Bond pad material	AlCu
Recommended condition for die and wire bonding climate	23° C ± 1K, 30 – 60% rel. humidity

1) For tolerances, see the wafer delivery specification general issue[3]

A Chip layout, type



References

[1] JEDEC JEP156A: *Chip-Package Interaction Understanding, Identification, and Evaluation*; 2018-03

[2] JEDEC JEP122H: *Failure Mechanisms And Models For Semiconductor Devices Failure Mechanisms And Models For Semiconductor Devices*; 2016-09

[3] Infineon Technologies: *Wafer Specification - General Issue, Chip delivery specification for thinned 200 mm/300 mm wafer , unsawn/sawn (latest revision)*; document release reference: Z8F50306400

Revision history

Reference	Description
Revision 5.1, 2026-02-24	
Overview of wafer characteristics	Chip thickness added
Whole document	New layout
Revision 5.0, 2026-02-17 (Internal review)	
Appendix A	Layout adaption of chip outline drawing
Revision 4.0, 2021-06-16	
	Change document classification
Revision 3.0, 2012-10-01	
Unification of sales codes	Additional sales codes
Revision 2.0, 2012-04-26	
	Deliveries only with mapping
Revision 1.0, 2009-06-02	
	Initial version

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