

8

7

6

5

4

3

CY P/N

610-60673-01

SH

1

REV

3.0

1

ECO NO.

REV

DATE

DESCRIPTION

DRAWN

CHECKED

APPROVED

--

1.0

12/07/23

INITIAL RELEASE

ECAD

SANTHOSH

SANTHOSH

--

2.0

23/10/23

DESIGN CHANGES

SANTHOSH

SANTHOSH

SANTHOSH

--

3.0

08/05/24

SPI SIGNAL IMPROVEMENTS

SANTHOSH

SANTHOSH

SANTHOSH

--

4.0

29/04/25

SILK UPDATE

SANTHOSH

SANTHOSH

SANTHOSH

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:

A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 600-60673-01_04.TGZ OR 600-60673-01_04.ZIP

B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.

C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.

D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.

E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.

F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2 DIELECTRIC MATERIAL:

A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).

B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF .076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.

C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.

D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

E. LAMINATE : FR4 OR EQUIVALENT (ROHS COMPLIANT) Tg>170 deg C, DIELECTRIC CONSTANT (Er) BETWEEN 3.2 to 3.7 @ 7 GHz..

F. LAYERS : 8 COPPER LAYERS, FINISHED THICKNESS 1.2 MM +/- 10% OF FINISH NOMINAL (W/O SOLDER MASK) (RECOMMENDATION :USE LAMINATE IPC CLASS B/L OR EQUIVALENT TO ACHIVE ABOVE SPECIFIED LIMITS)

44.92

+/- 10%

(XXXX)

(XXXX)

(XXXX)

(XXXX)

(XXXX)

(XXXX)

L01 - TOP

L02 - GND1

L03 - SIG1

L04 - PWR1

L05 - PWR2

L06 - SIG2

L07 - GND2

L06 - BOT

COPPER WT

1.85

1.85

1.85

2.067

2.067

1.85

1.85

1.85

SE IMP OHMS

50E

--

50E

--

--

50E

--

50E

SE TRACE WIDTH

6.2

4.0

4.0

6.2

REF LAYER

L2

L2

L7

L7

CPW(50E) WIDTH/SPACE

6.2/3.9

REF LAYER

L2

CPW(50E) WIDTH/SPACE

17.8/15

REF LAYER

L3

DIFF IMP OHMS

100E

100E

100E

100E

DIFF TRACE WIDTH/SPACE

3.5/4.4

3.5/7.1

3.5/7.1

3.5/4.4

REF LAYER

L2

L2

L7

L7

DIFF IMP OHMS

90E

90E

90E

90E

DIFF TRACE WIDTH/SPACE

4.5/4.4

4.5/7.1

4.5/7.1

4.5/4.4

REF LAYER

L2

L7

L7

STACK-UP (UNITS IN MILS)

3. DRILLING:

A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+ .0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.

B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

C. FILL ALL THRU VIAS USING NON-CONDUCTIVE EPOXY AND OVERPLATE WITH COPPER, .005 [.0002] MINIMUM THICKNESS. DIMPLE DEPTH IN BGA PADS SHALL BE .025 [.001] MAXIMUM. THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.

D. FILL ALL MICROVIAS WITH COPPER PLATING OR NON-CONDUCTIVE EPOXY; DIMPLE DEPTH IN BGA PADS SHALL BE .025 [.001] MAXIMUM. FOR EPOXY FILL, OVERPLATE WITH COPPER, .005 [.0002] MINIMUM AND THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.

E. FILL ALL BURIED VIAS USING NON-CONDUCTIVE EPOXY AND OVERPLATE WITH COPPER, .005 [.0002] MINIMUM THICKNESS. THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.

4. SOLDER MASK:

A. APPLY LPI SOLDER MASK USING PROVIDED DATA.

B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR RED.

C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:

A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INKJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.

B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.

C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:

A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.

B. ALL PCBs SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.

C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7 FINAL FINISH:

A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

B. FINAL FINISH ON EDGE CONNECTOR CONTACTS SHALL BE ELECTROLYTIC HARD GOLD PLATING, .76 MICROMETERS [30 MICROINCHES] MINIMUM, OVER ELECTROLYTIC NICKEL PLATING, 1.27 MICROMETERS [50 MICROINCHES] MINIMUM.

8. IMPEDANCE:

A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.

B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBs SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS

.xxx .xx

±.127 ±.25

[±.005] [±.01]

ANGLES ±.5°

DO NOT SCALE DRAWING

APPROVALS

DATE

DRAWN

SANTHOSH

29/04/25

ENGINEER

BHARATH

29/04/25

CHECKER

SANTHOSH

29/04/25

QA

-

-

PROJ. ENG.

-

-

SEE BOM

SEE BOM

NEXT ASSY

USED ON

APPLICATION

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MATERIAL

2

FINISH

7

infineon

Infineon Technologies AG
IFAG MUC Am Campeon 1-15
85579 NEUBIBERG - GERMANY

TITLE

PCB FABRICATION,
PSoC™ EDGE E84 SOM

SIZE

D

CAGE CODE

-

INFINEON P/N

610-60673-01

SCALE

1/1

SHEET

1 OF 2

REV

04

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ANY PISH - GENERAL

ANY PISH - GENERAL

ALLEGRO FILE 600-60673-01_04.BRD

