

8

7

6

5

4

3

2

1

2

10

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:

A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 600-60647-01\_06.TGZ OR 610-60647-01\_06.ZIP.

B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.

C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.

D. REMOVE ALL BURRS AND BREAK SHARP EDGES. .381 [.015] MAX RADIUS.

E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.

F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:

A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).

B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF .076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.

C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.

D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:

A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+ .0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.

B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

4. SOLDER MASK:

A. APPLY LPI SOLDER MASK USING PROVIDED DATA.

B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLACK.

C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:

A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.

B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.

C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:

A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.

B. ALL PCBs SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.

C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7. FINAL FINISH:

A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:

A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.

B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBs SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.

10. NET TIE:

A. SEPERATE ELECTRICAL LAYER "SHORT\_BOTTOM.ART" IS INCLUDED IN THE ARTWORK PACKAGE THIS LAYER WILL ELECTRICALLY SHORT FEW DISCRETE IN BOTTOM LAYER, FOR REFERENCE PLEASE CHECK DETAIL3.ART LAYER

61.69MILS  
+/- 10%

( 3.558 MIL )

( 5.000 )

( 35.839 )

( 5.000 )

( 3.558 )

LAYER DESCRIPTION

L01 - TOP

L02 - PLANE

L03 - SIGNAL

L04 - SIGNAL

L05 - PLANE

L06 - BOTTOM

START COPPER WT

0.5 OZ

1.0 OZ

1.0 OZ

1.0 OZ

0.5 OZ

SE IMP OHMS

50E

--

50E

--

50E

SE TRACE WIDTH

5.90MIL

-----

6.2MIL

-----

5.90MIL

REF LAYER

L02

---

L02

---

L05

CPW SPACE

-----

-----

-----

-----

-----

DIFF IMP OHMS

90E

---

90E

---

90E

DIFF TRACE WIDTH/SPACE

4.5/4.5MIL

----

4.5/5.5MIL

----

4.5/4.5MIL

REF LAYER

L02

---

L02

---

L05

DIFF IMP OHMS

100E

---

100E

---

100E

DIFF TRACE WIDTH/SPACE

4.0/6.0MIL

----

4.0/7.4MIL

----

4.0/6.0MIL

REF LAYER

L02

---

L02

---

L05

STACK-UP

SEE BOM  
NEXT ASSY

SEE BOM  
USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED  
DIMENSIONS ARE IN METRIC  
WITH INCHES IN BRACKETS  
.XXX .XX ANGLES  
±.064 ±.13 ±.5°  
[±.005] [±.01]

2

7

DO NOT SCALE DRAWING

APPROVALS

DATE

PURSHOTHAMA 06/23/25

ENGINEER RAJASHREE 28/04/25

CHECKER

QA

PROJ. ENG.

-

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SUCH USER POSSESSES AUTHORIZATION FROM Infineon

FINISH

Infineon

Infineon Technologies AG  
Am Compeen 1-15  
85579 NEUBIBERG - GERMANY

TITLE

PCB FABRICATION,  
PSOC Edge E8  
Evaluation Kit

SIZE

D

CAGE CODE

-

INFINEON P/N

610-60647-01

SHEET

1 OF 2

REV

06

COMPUTER GENERATED DRAWING  
DO NOT CHANGE MANUALLY

FAB NOTES REV 04/05/17

7

6

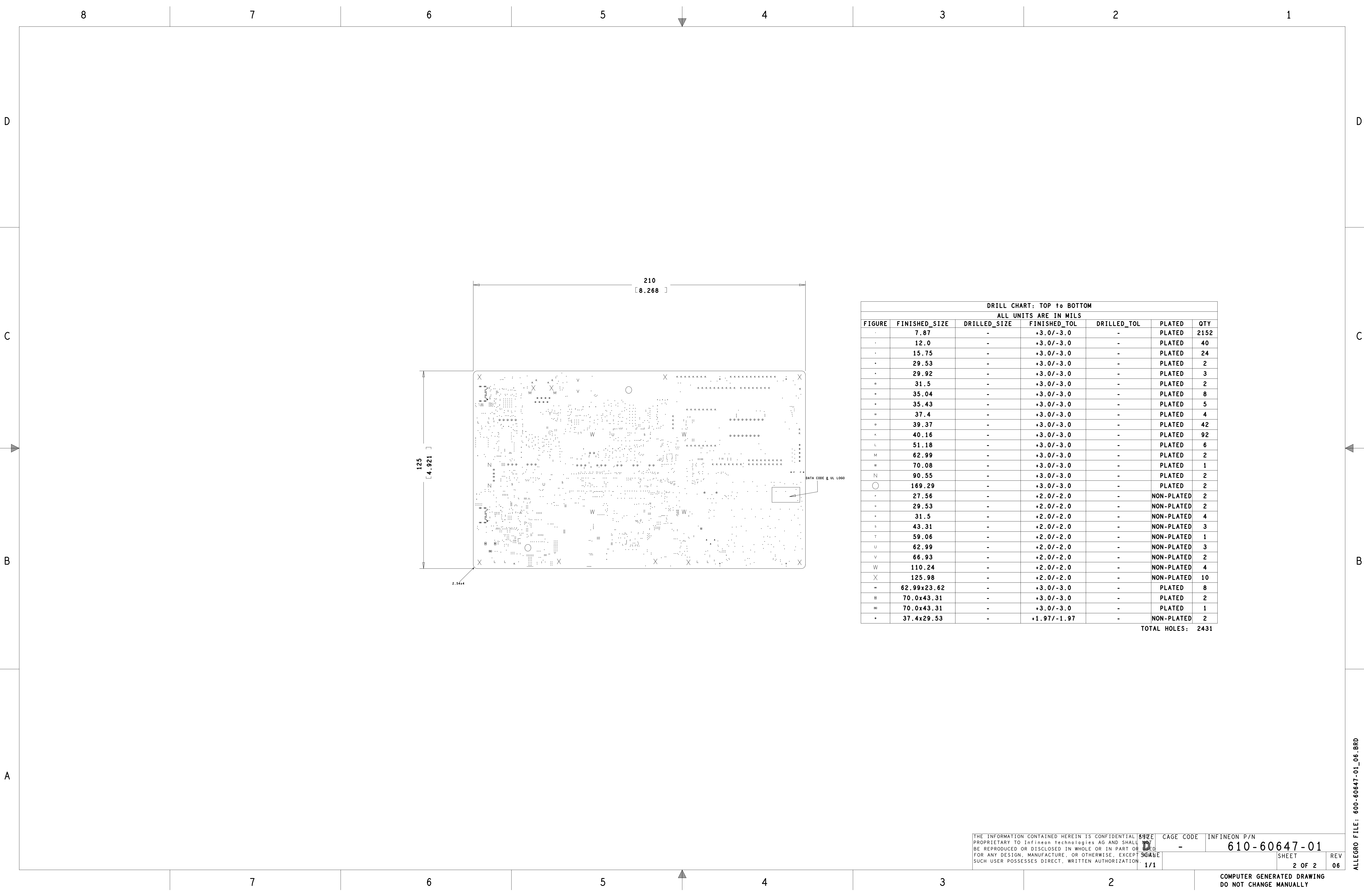
5

4

3

2

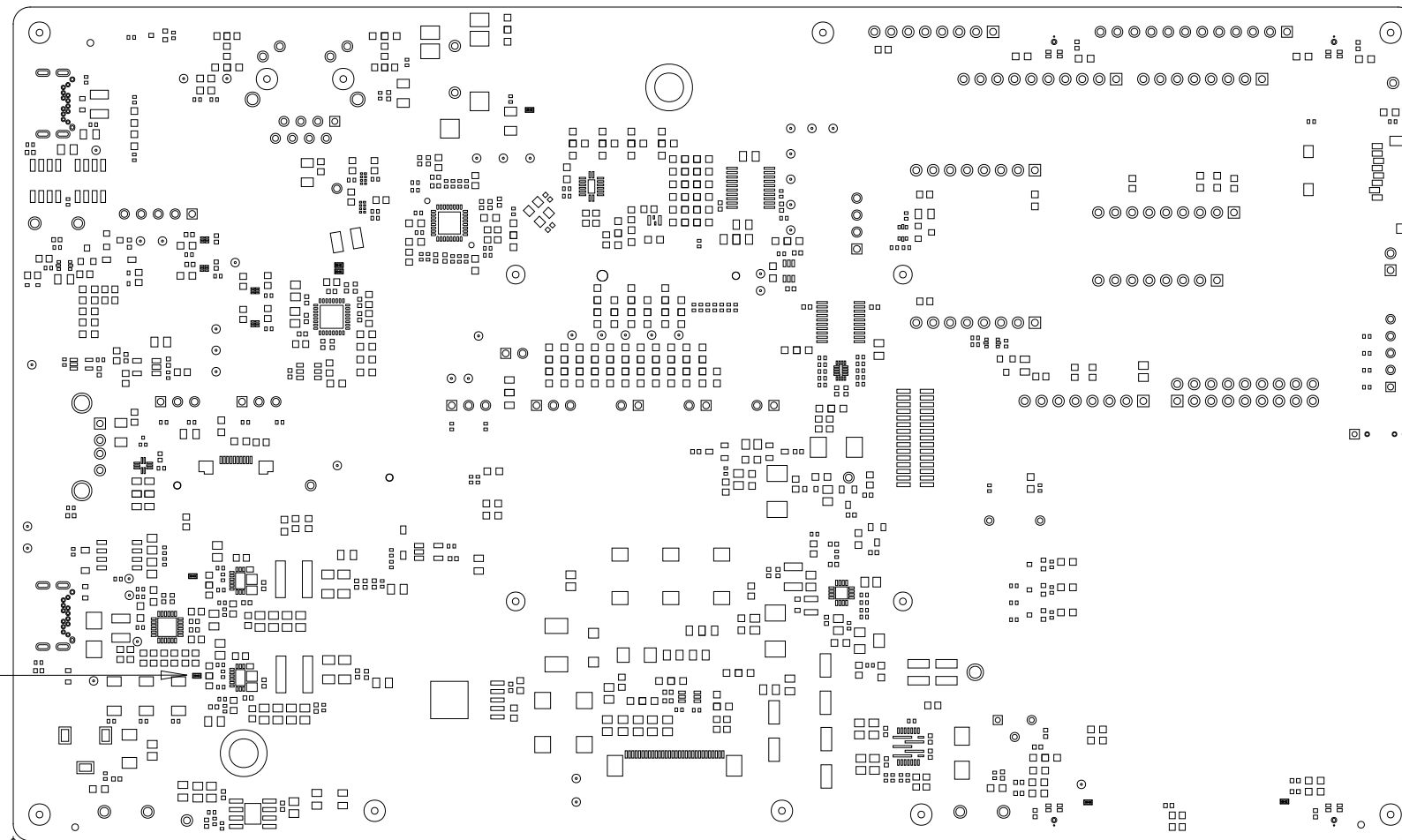
ALLEGRO FILE: 600-60647-01\_06.BRD



DRILL CHART: TOP to BOTTOM						
ALL UNITS ARE IN MILS						
FIGURE	FINISHED_SIZE	DRILLED_SIZE	FINISHED_TOL	DRILLED_TOL	PLATED	QTY
-	7.87	-	+3.0/-3.0	-	PLATED	2152
-	12.0	-	+3.0/-3.0	-	PLATED	40
-	15.75	-	+3.0/-3.0	-	PLATED	24
*	29.53	-	+3.0/-3.0	-	PLATED	2
*	29.92	-	+3.0/-3.0	-	PLATED	3
o	31.5	-	+3.0/-3.0	-	PLATED	2
*	35.04	-	+3.0/-3.0	-	PLATED	8
*	35.43	-	+3.0/-3.0	-	PLATED	5
o	37.4	-	+3.0/-3.0	-	PLATED	4
o	39.37	-	+3.0/-3.0	-	PLATED	42
x	40.16	-	+3.0/-3.0	-	PLATED	92
L	51.18	-	+3.0/-3.0	-	PLATED	6
M	62.99	-	+3.0/-3.0	-	PLATED	2
B	70.08	-	+3.0/-3.0	-	PLATED	1
N	90.55	-	+3.0/-3.0	-	PLATED	2
o	169.29	-	+3.0/-3.0	-	PLATED	2
*	27.56	-	+2.0/-2.0	-	NON-PLATED	2
*	29.53	-	+2.0/-2.0	-	NON-PLATED	2
*	31.5	-	+2.0/-2.0	-	NON-PLATED	4
S	43.31	-	+2.0/-2.0	-	NON-PLATED	3
T	59.06	-	+2.0/-2.0	-	NON-PLATED	1
U	62.99	-	+2.0/-2.0	-	NON-PLATED	3
V	66.93	-	+2.0/-2.0	-	NON-PLATED	2
W	110.24	-	+2.0/-2.0	-	NON-PLATED	4
X	125.98	-	+2.0/-2.0	-	NON-PLATED	10
o	62.99x23.62	-	+3.0/-3.0	-	PLATED	8
B	70.0x43.31	-	+3.0/-3.0	-	PLATED	2
o	70.0x43.31	-	+3.0/-3.0	-	PLATED	1
*	37.4x29.53	-	+1.97/-1.97	-	NON-PLATED	2

TOTAL HOLES: 2431

SHORT NET GND AND AGND  
TOTAL 7no's SHORT NET ON BOARD



**Infineon**  
Infineon Technologies AG  
Am Campeon 1-15  
85579 NEUBIBERG - GERMANY

PROJECT:	PSOC Edge E8 Evaluation Kit		
DRAWN BY:	PURSHOTHATHAMA		
LAYER:	DETAIL3		
DWG NO:	610-60647-01	REV:	06
		DATE:	06/23/25