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NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:

A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES  
600-60706-01\_02.TGZ or 610-60706-01\_02.zip

B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.

C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.

D. REMOVE ALL BURRS AND BREAK SHARP EDGES. .381 [.015] MAX RADIUS.

E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.

F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2

DIELECTRIC MATERIAL:

A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).

B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF .076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.

C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.

D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:

A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+ .0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.

B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

4. SOLDER MASK:

A. APPLY LPI SOLDER MASK USING PROVIDED DATA.

B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.

C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:

A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.

B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, IN BOTTOM UNUSED SPACE IN WHITE COLOR

C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:

A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.

B. ALL PCBs SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.

C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7

FINAL FINISH:

A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:

A. CONTROLLED IMPEDANCE NOT REQUIRED

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBs SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.

10

NET TIE:

A SEPERATE ELECTRICAL LAYER "SHORT\_BOTTOM.ART" IS INCLUDED IN THE ARTWORK PACKAGE THIS LAYER WILL ELECTRICALLY SHORT FEW DISCRETE IN BOTTOM LAYER, FOR REFERENCE PLEASE CHECK DETAIL3.ART LAYER

1.6mm  
+/- 10%

(FILL)

STACK-UP INCH

LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	CPW SPACE	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	CPW SPACE
L01 - TOP	1 OZ	--	.-----	-----	---	.-----/.-----	-----
L02 - BOTTOM	1 OZ	--	.-----	-----	---	.-----/.-----	-----

SEE BOM  
NEXT ASSY

SEE BOM  
USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED  
DIMENSIONS ARE IN METRIC  
WITH INCHES IN BRACKETS  
.XXX .XX ANGLES  
±.064 ±.13 ±.5°  
[±.005] [±.01]

2

7

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FINISH

DO NOT SCALE DRAWING

APPROVALS

DATE

PRAO 09/11/24

ENGINEER MADHU 09/10/24

CHECKER

QA

PROJ. ENG.

1/1

1 OF 1

REV 02

Infineon

Infineon Technologies AG  
Am Compeon 1-15  
85579 NEUBIBERG - GERMANY

TITLE

PCB FABRICATION,  
KIT PSC3M5 2GO

SIZE

CAGE CODE

CY P/N

D -

600-60706-01

SCALE

SHEET

REV

1/1

1 OF 1

02

COMPUTER GENERATED DRAWING  
DO NOT CHANGE MANUALLY

FAB NOTES REV 04/05/17

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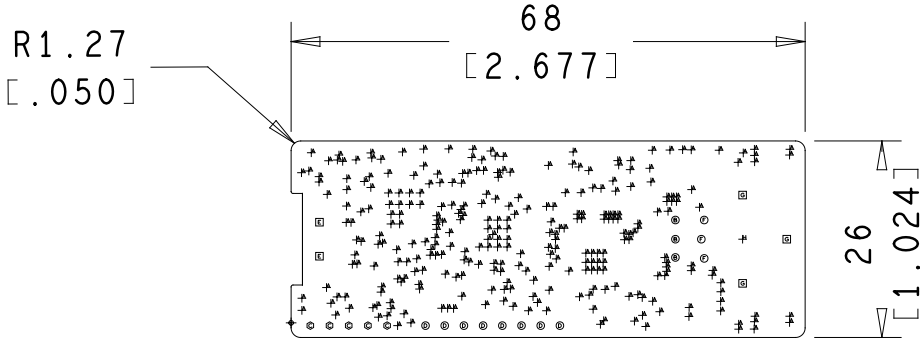
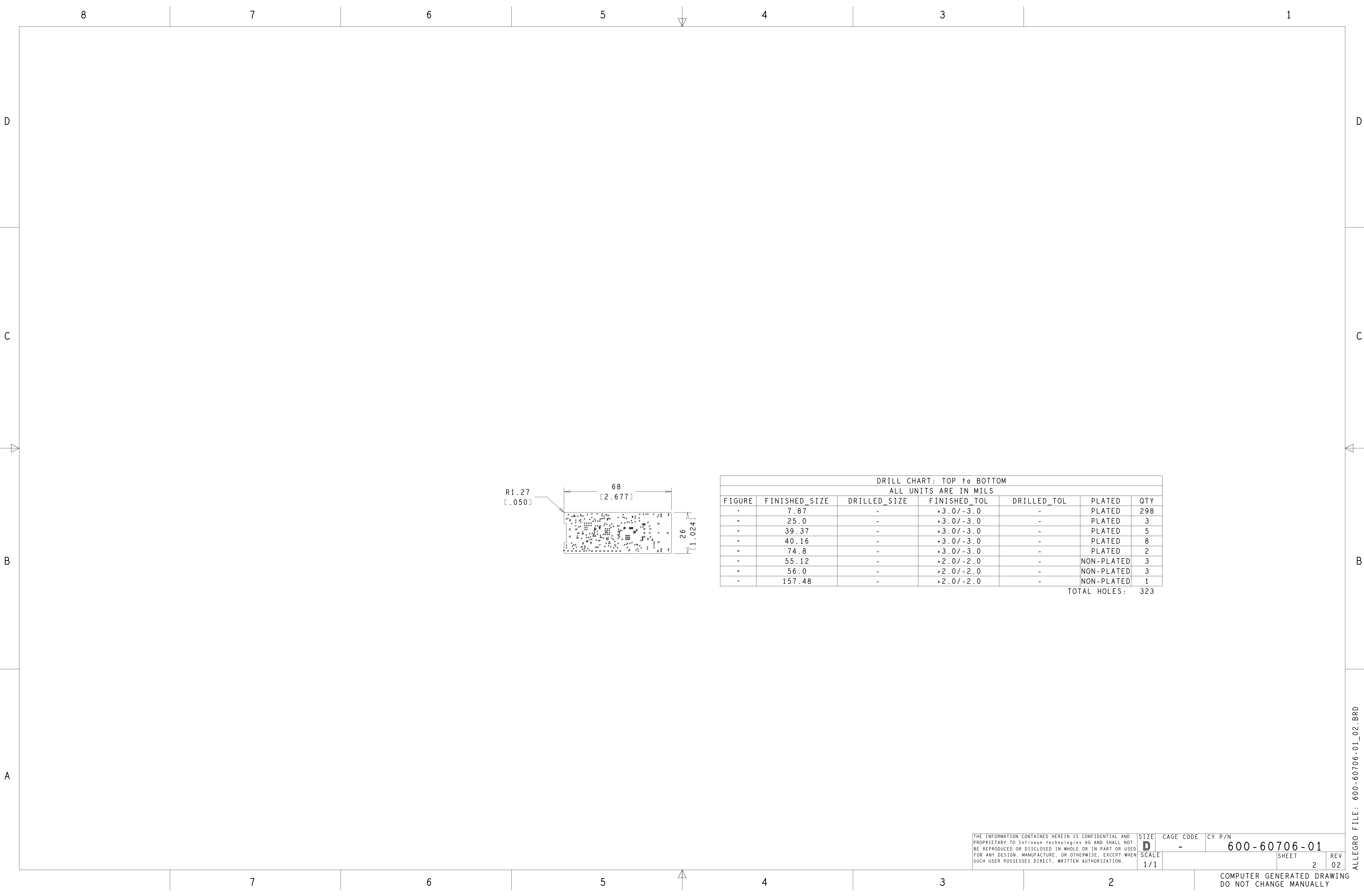
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ALLEGRO FILE: 600-60706-01\_02.BRD



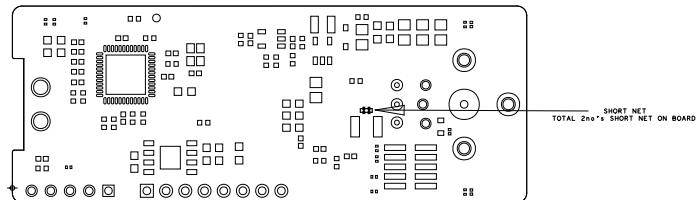
DRILL CHART: TOP to BOTTOM						
ALL UNITS ARE IN MILS						
FIGURE	FINISHED_SIZE	DRILLED_SIZE	FINISHED_TOL	DRILLED_TOL	PLATED	QTY
*	7.87	-	+3.0/-3.0	-	PLATED	298
*	25.0	-	+3.0/-3.0	-	PLATED	3
*	39.37	-	+3.0/-3.0	-	PLATED	5
*	40.16	-	+3.0/-3.0	-	PLATED	8
"	74.8	-	+3.0/-3.0	-	PLATED	2
"	55.12	-	+2.0/-2.0	-	NON-PLATED	3
"	56.0	-	+2.0/-2.0	-	NON-PLATED	3
*	157.48	-	+2.0/-2.0	-	NON-PLATED	1

TOTAL HOLES: 323

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SCALE 1/1				SHEET 2		REV 02	

COMPUTER GENERATED DRAWING  
DO NOT CHANGE MANUALLY

# ART FILM - detail13



Infineon Technologies AG  
Am Campeon 1-15  
85579 NEUBIBERG - GERMANY

PROJECT:	KIT PSC3M5 2G0		
DRAWN BY:	PRAO		
LAYER:	DETAIL3		
DWG NO:	600-60706-01	REV: 02	DATE: 09/11/2024

# ART FILM - detail13