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NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
- A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES  
600-60686-01\_03.TGZ OR 600-60686-01\_03.ZIP.
  - B. ALL SPECIFICATIONS/USING SHALL BE PER THEIR LATEST REVISIONS.
  - C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED  
ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING  
CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE  
DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER  
ELECTRICAL PERFORMANCE.
  - D. REMOVE ALL BURRS AND BREAK SHARP EDGES. .381 [.015] MAX RADIUS.
  - E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
  - F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2 DIELECTRIC MATERIAL:

- A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (ROHS COMPLIANT EPOXY-GLASS).
- B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF .076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
- C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
- D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:  
A. VIA DIAMETERS (TOL. =  $\pm .051/-$  DRILL DIAMETER [ $\pm .0020/-$  DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.  
B. LAYER-TO-LAYER MISREGISTRATION SHALL BE  $.127$  [ $.005$ ] MAXIMUM.

4. SOLDER MASK:
- A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
  - B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE
  - C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:
- A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
  - B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
  - C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

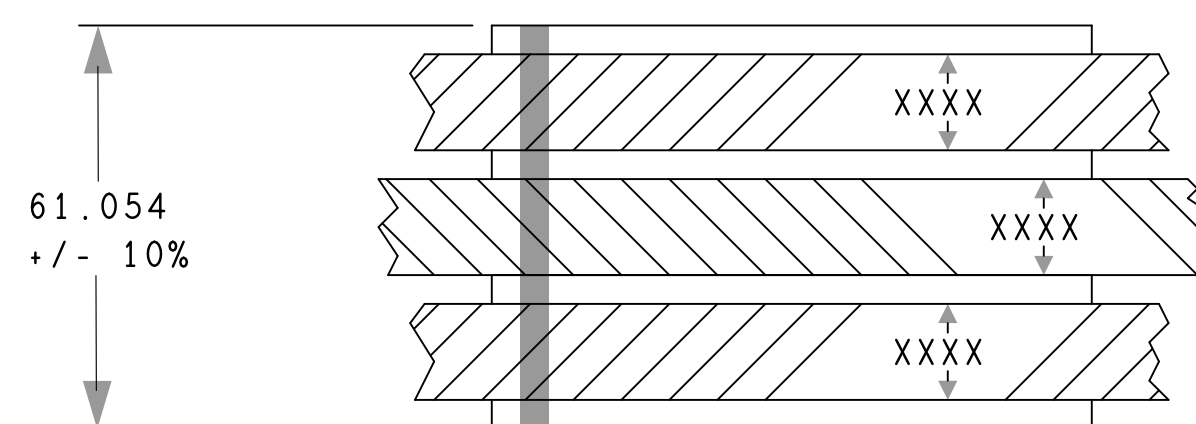
6. ELECTRICAL TEST
- A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++, DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
  - B. ALL PCBs SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
  - C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7 FINAL FINISH:

- A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:  
A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.  
B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBs SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.



LAYER DESCRIPTION	COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF LAYER
L01 - TOP	2.087	50E	5.80	L2
L02 - GND1	1.26	--	-----	---
L03 - GND2	1.26	--	-----	---
L04 - BOTTOM	2.087	50E	5.80	L3


STACK-UP ( UNITS IN MILS )

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	
<p>THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO Infineon Technologies AG AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHERE SUCH USER POSSESSES AUTHORIZATION FROM Infineon Technologies AG.</p>	

UNLESS OTHERWISE SPECIFIED  
DIMENSIONS ARE IN METRIC  
WITH INCHES IN BRACKETS

.XXX	.XX	ANGLES
±.064	±.13	±.5°
[+.005]	[+.01]	

DO NOT SCALE DRAWING	
APPROVALS	DATE
DRAWN SANTHOSH R	19/11/24
ENGINEER SANTHOSH G	19/11/24
CHECKER PURSHOTHAMA	19/11/24
QA -	-
PROJ. ENG. -	-

		Infineon Technologies AG Am Campeon 1-15 85579 NEUBERG - GERMANY	
TITLE			
PCB FABRICATION, KIT_PSC3_DB1			
SIZE	CAGE CODE	CY	P/N
D	-		610-60686-01
SCALE			SHEET
1/1			1 OF 2
			REV 03

COMPUTER GENERATED DRAWING  
DO NOT CHANGE MANUALLY

