Index

Page 01. Index
Page 02. Block Diagram
Page 03. Power Diagram
Page 04: Stack-up
Page 05. GR - High Speed
Page 06: GR - Misc
Page 07: GR - Power & GND
Page 08: TBT USBC Ports
Page 09: PMG1 - DMC
Page 10: PMG1 – PD Controller
Page 11: USBC Source path
Page 12: USB3.1 10G Hub
Page 13: USB2 Hub FL5801
Page 14: Foxville
Page 15: Foxville PWR
Page 16: RTL8153 ETH Controller
Page 17: Ethernet MUX
Page 18: DP1.4 MST – Main
Page 19: DP1.4 MST – PWR
Page 20: DP1.4 MST – Filters
Page 21: DP Tx1 Mux
Page 22: DP Tx2 Mux
Page 23: Display Ports
Page 24: HDMI Port
Page 25:InterConncet USB Ports
Page 26: PWR Supply – LV
Page 27: PWR Supply – LV1
Page 28: PWR Supply – DP
Page 29: PWR Supply – USB
Page 30: PWR Supply – 5V
Page 31: PWR Supply - HV
Page 32: Debug

Revision History

Rev.	Date	Comments
1.0	20/6/2021	Rev1 - PCB manufacture
1.0	20/6/2021	Rework – Connect VCC5v0 to VCC5v0_SYS BOM Change – Control Port B Load switch by PMG1 GPIO

Intel Confidential

THUNDERBOLT

Title: Index		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 1 of 17	

Block Diagram

CIO 20Gbps
PCIe
DP 8.1Gbps
USB3.1 10Gbps
USB2 480Mbps
MDI
USB PD CC
I2C
SPI

PD I2C
I2C ADDR:
0x38
0x3F
CC
EC I2C
CC

PMG1-S3
16Mb Flash (W25Q16JV)

Goshen Ridge
PortA (UFP)
PortB (DFP)
PortC (DFP)
PortD (DFP)
LC I2C
GR SPI
USB2.0
PCIe_CLKREF_P/N
Port E
SM BUS
PCIe_LANE0

16Mb Flash (W25Q16JV)

USB2 480Mbps
USB2 480Mbps
USB2 480Mbps

RTD2188
Rx0
Tx0
Tx1
Tx2
Tx3
HDMI2.1

PI3WVR13612
CH I
CH B
CH A

PI3WVR13612
CH B
CH A
CH I

VL822-Q7
UFP
DFP2
DFP3

To: IO Board

USB 1Gbe Controller (RTL8153B)

PI3L2500
CH B
CH A
CH A

USB2.0 Hub (FL5801)

USB2 480Mbps

PCIe Dual Outputs Generator (Si52112-B6)
DIFF1_P/N
DIFF0_P/N

PCIE_CLK100M

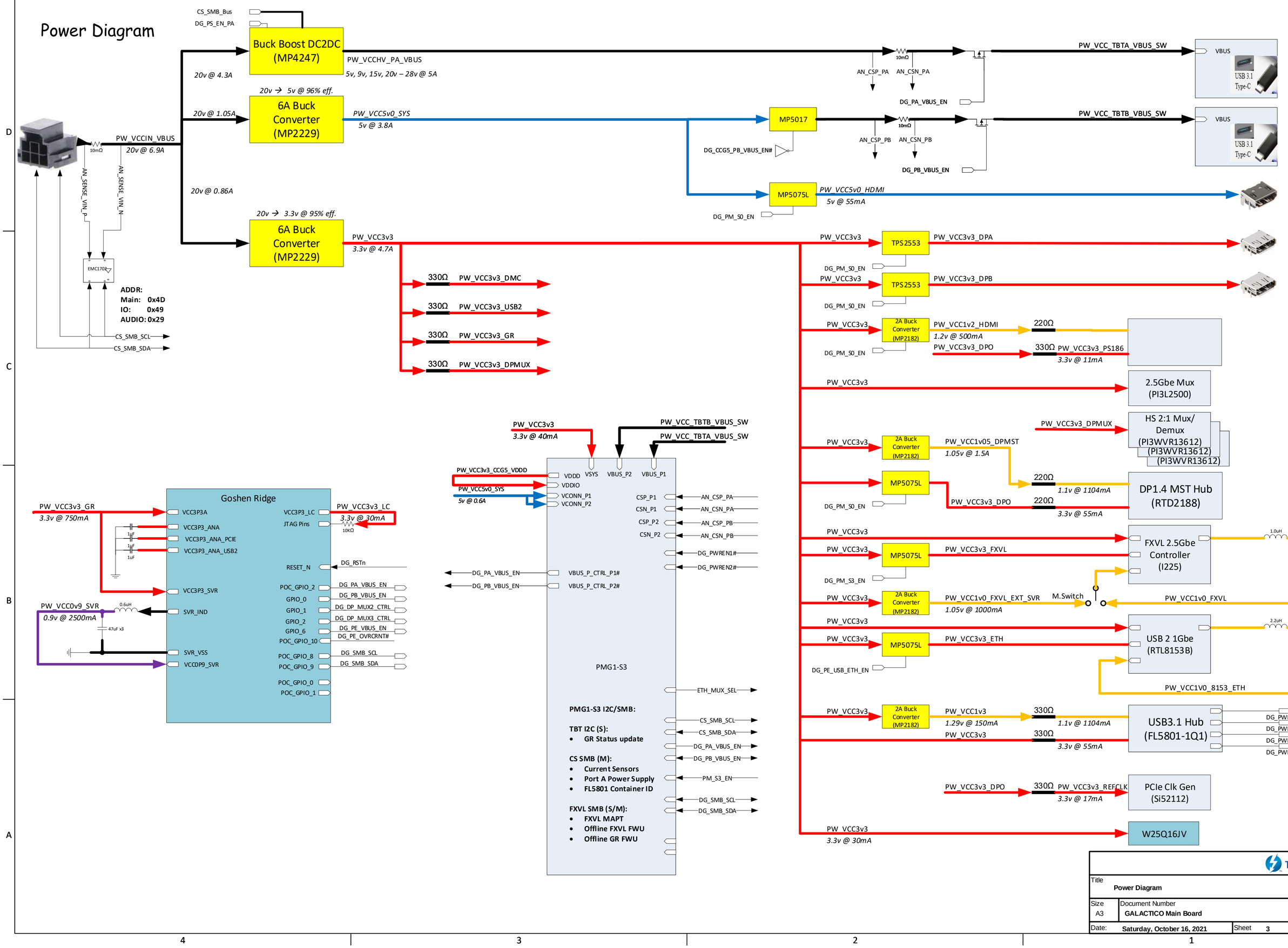
FXVL 2.5Gbe Controller (I225)

Intel Confidential

THUNDERBOLT

Title: Block Diagram		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 2 of 17	

Power Diagram



Title	Power Diagram
Size	A3
Document Number	GALACTICO Main Board
Rev	1.1
Date:	Saturday, October 16, 2021
Sheet	3 of 17

Stack-Up

Stack-Up - FR4 FL-170						Control Impedance																				Via Type
Layer			Copper		Core/PP	Er (Dk)				Single 50Ω @ 1GHz			Differential 85Ω @ 5GHz (CIO and USB3.1)				Differential 90Ω @ 5GHz (PCIe)				Differential 100Ω @ 5GHz (DP and USB2)				Reference Plane Layer	TH
Name	Purpose	Type	Foil [Oz]	Final [mil]	[mil]	@ 1GHz	@ 2GHz	@ 5GHz	@ 10GHz	W1 [mil]	D [mil]	Z [Ohm]	W1 [mil]	S [mil]	D [mil]	Z [Ohm]	W1 [mil]	S [mil]	D [mil]	Z [Ohm]	W1 [mil]	S [mil]	D [mil]	Z [Ohm]		v16c8
CS	Sig	S	0.5	1.2						6.5	15	48.95	5.5	4	15	85.22	4.8	4	15	89.93	3.7	4	15	98.8	Ref (L2)	
	2116	PP			4.00	4.10	4.00	3.90	3.70																	
L2	GND	G	1	1.2																					GND	
	5mil Core 1x2116	CORE			5.1	4.10	4.00	3.90	3.70																	
L3	Sig/PWR	V	1	1.2						4	15	45.19					3.5	5	15	84.99	3.5	5	15	84.99	Ref (L4)	
	2116	PP			4.10	4.10	4.00	3.90	3.70																	
L4	GND	G	1	1.2																					GND	
	3mil Core 1x1080	CORE			3	4.10	4.00	3.90	3.70																	
L5	Sig/PWR	V	1	1.2																						
	Mix	PP			17.80	4.30	4.10	3.90	3.80																	
L6	Sig/PWR	V	1	1.2																						
	3mil Core 1x1080	CORE			3	4.10	4.00	3.90	3.70																	
L7	GND	G	1	1.2																					GND	
	2116	PP			4.10	4.10	4.00	3.90	3.70																	
L8	Sig/PWR	V	1	1.2						4	15	45.19					3.5	5	15	84.99	3.5	5	15	84.99	Ref (L7)	
	5mil Core 1x2116	CORE			5.1	4.10	4.00	3.90	3.70																	
L9	GND	G	1	1.2																					GND	
	2116	PP			4.00	4.10	4.00	3.90	3.70																	
PS	Sig	S	0.5	1.2						6.5	15	48.95	5.5	4	15	85.22	4.8	4	15	89.93	3.7	4	15	98.8	Ref (L9)	
		Total	9	12	50.2																					
		Total	62.2	mil																						
		Total	1.58	mm																						

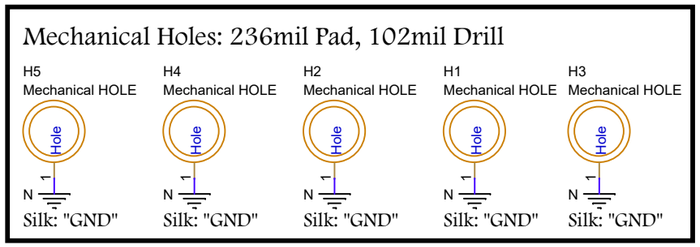
PCB1

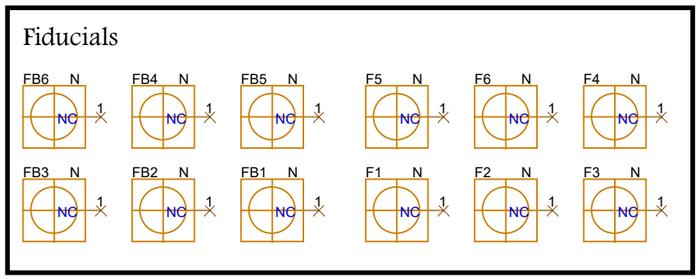


Y

ML1
TBT_Logo

ML2
Intel_logo_standard





<Core Design>

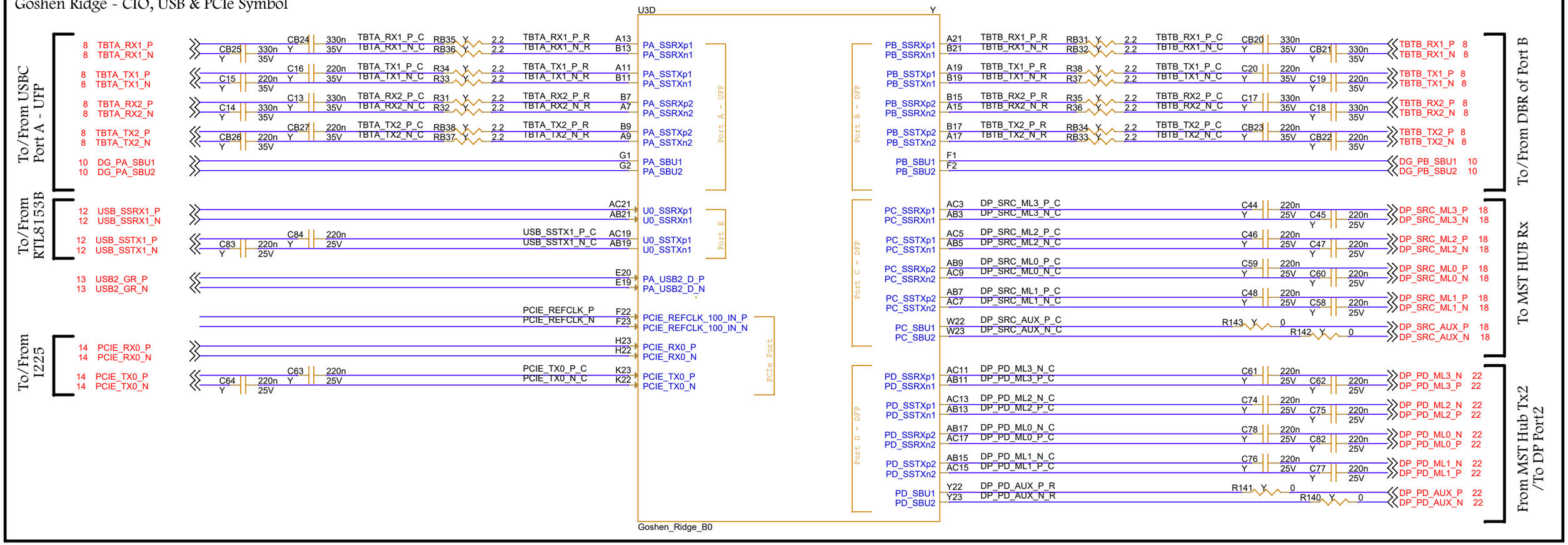
Intel Confidential

THUNDERBOLT

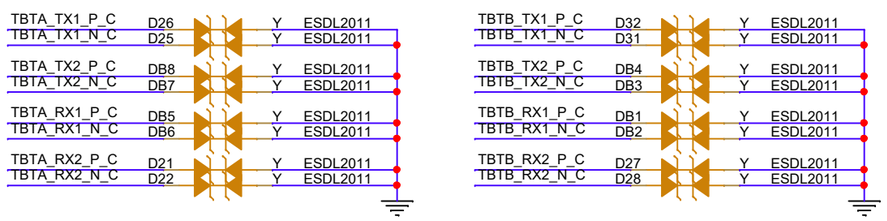
Title: Stack-Up		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 4 of 32	

Goshen Ridge - High Speed (CIO, USB and PCIe) Part

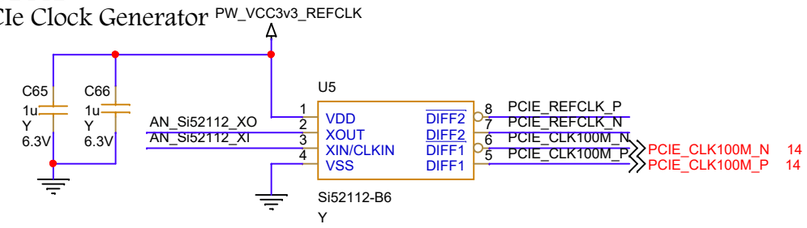
Goshen Ridge - CIO, USB & PCIe Symbol



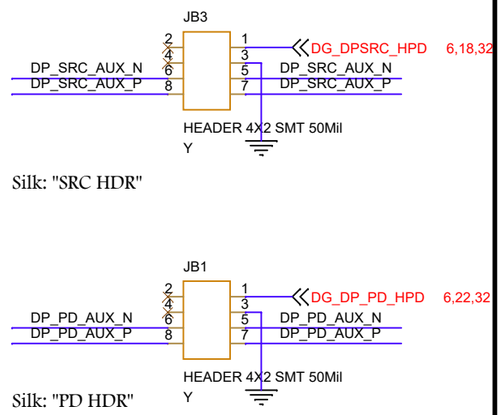
ESD Protection for Data Path



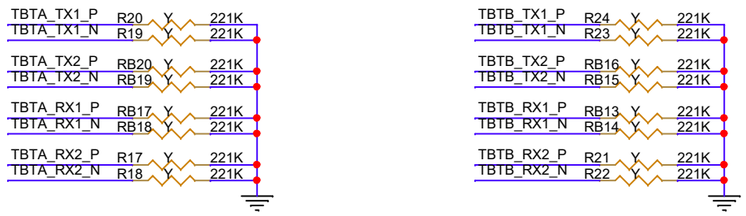
Si52112
PCIe Clock Generator



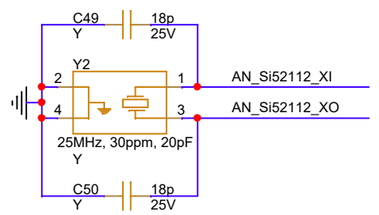
AUX Debug headers



Bleeding Resistors



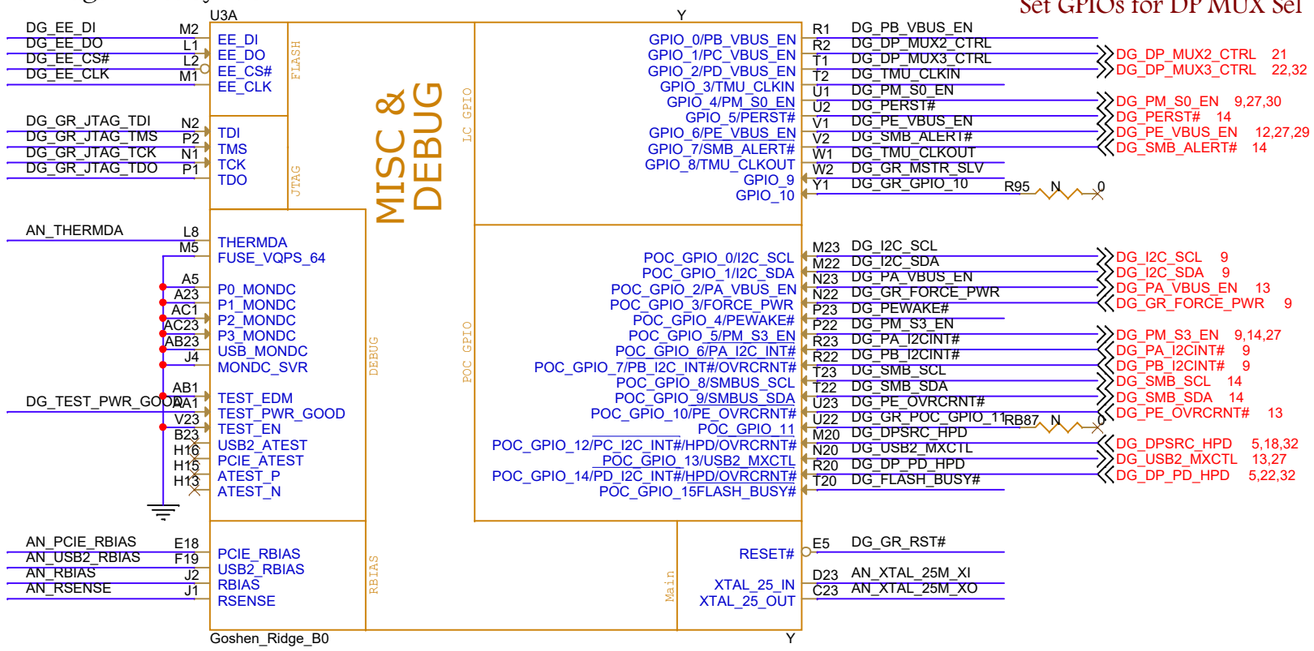
25MHz, 30ppm, 20pF 2.0 x 1.6 mm Crystal





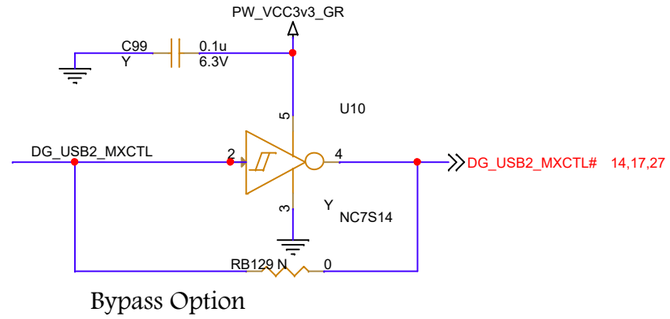
Goshen Ridge - Misc Part

Goshen Ridge - Misc Symbol



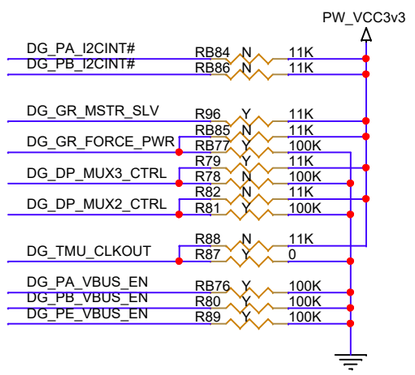
Set GPIOs for DP MUX Sel

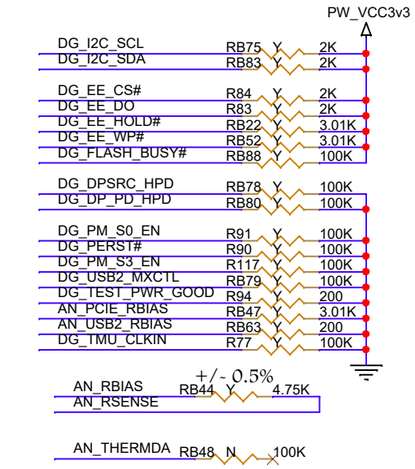
DG_USB2_MXCTL Inverter



Bypass Option

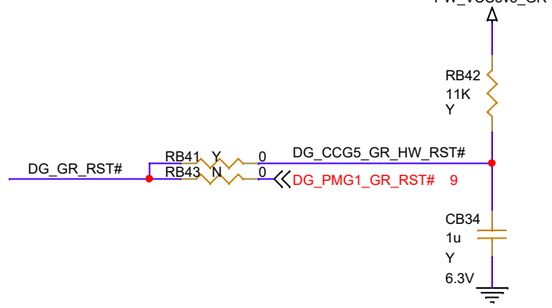
GR HW Configuration



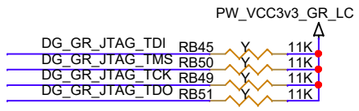


HPD MST TX2: Assy near GR PD_HPD
HPD MST Rx0: Assy near GR SRC_HPD

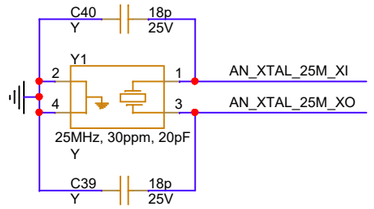
Goshen Ridge RESET



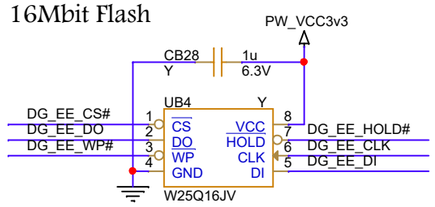
GR JTAG



25MHz, 30ppm, 20pF Crystal

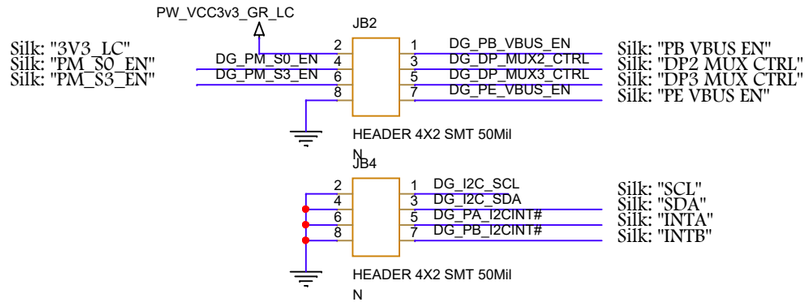


16Mbit Flash

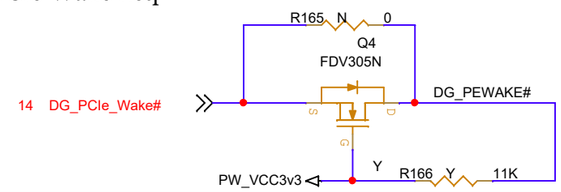


Silk: "GR NVM"

Debug Headers



PCIe Wake Req



<Core Design>

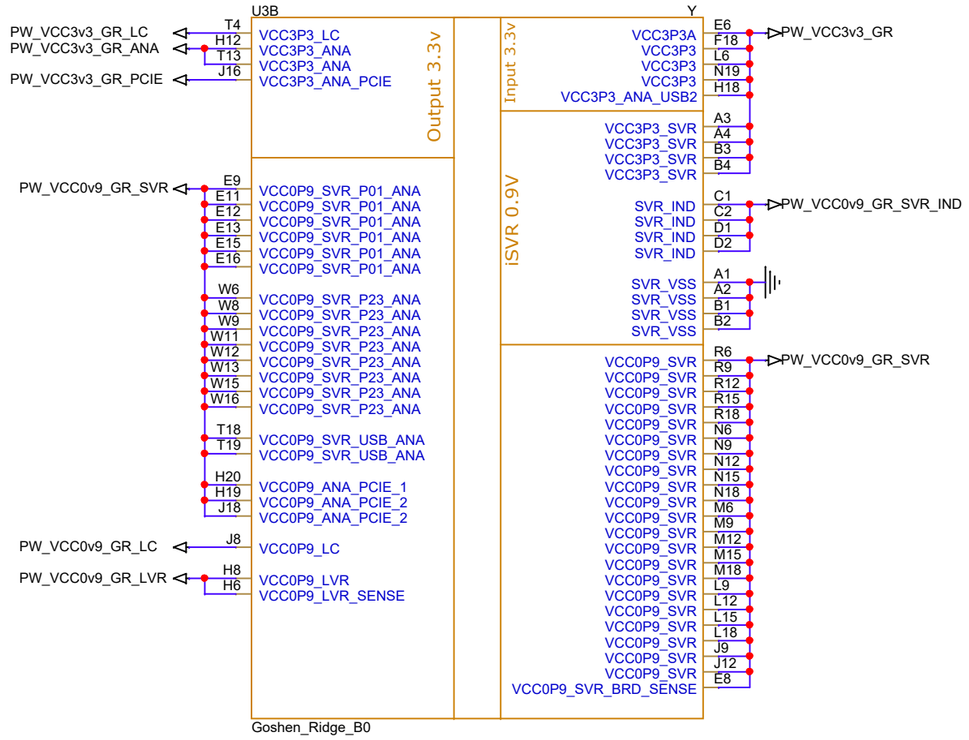
Intel Confidential

THUNDERBOLT

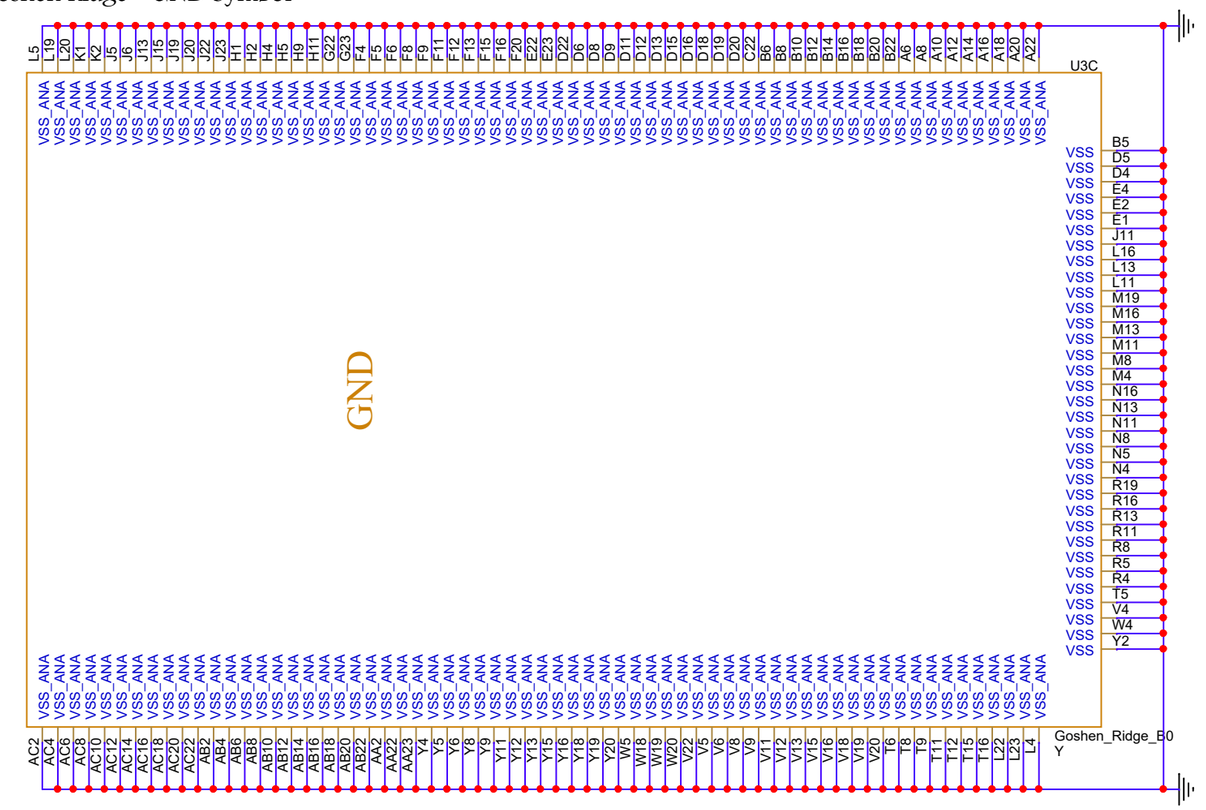
Title	GR - Misc Part	
Size A3	Document Number GALACTICO Main Board	Rev 1.1
Date: Saturday, October 16, 2021	Sheet 6 of 32	

Goshen Ridge - Power Supply & GND Parts

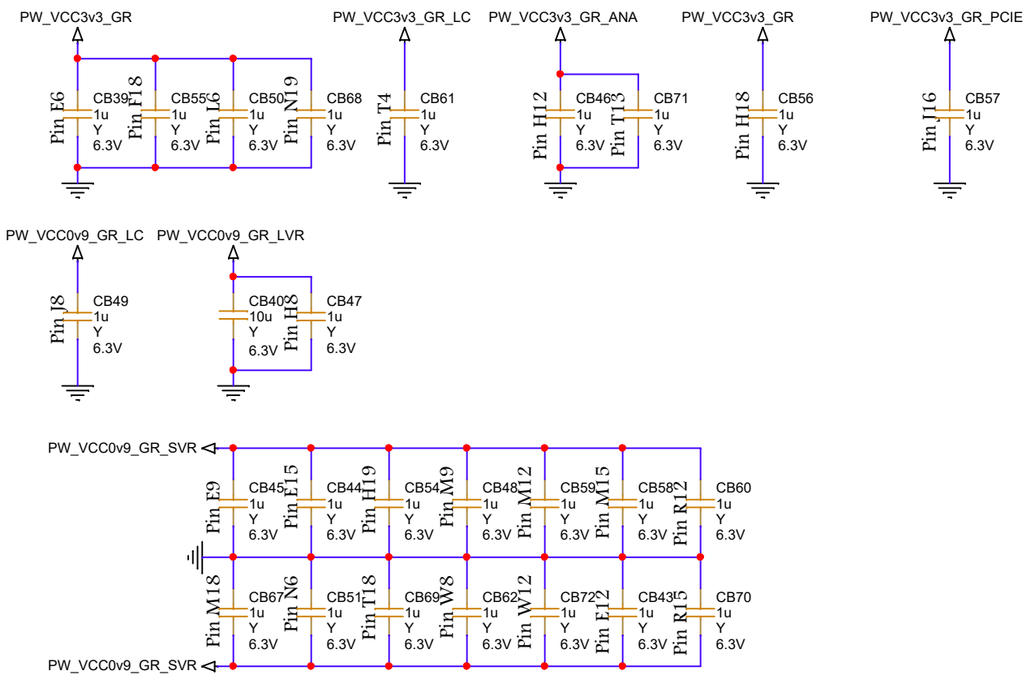
Goshen Ridge - Power Symbol



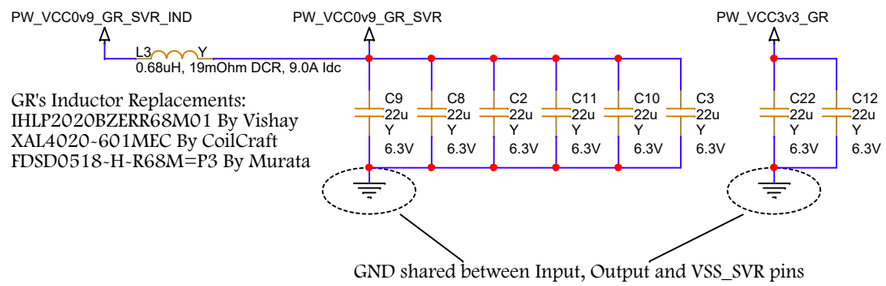
Goshen Ridge - GND Symbol



Goshen Ridge - Decoupling Capacitors



Goshen Ridge - iSVR Circuit



<Core Design>

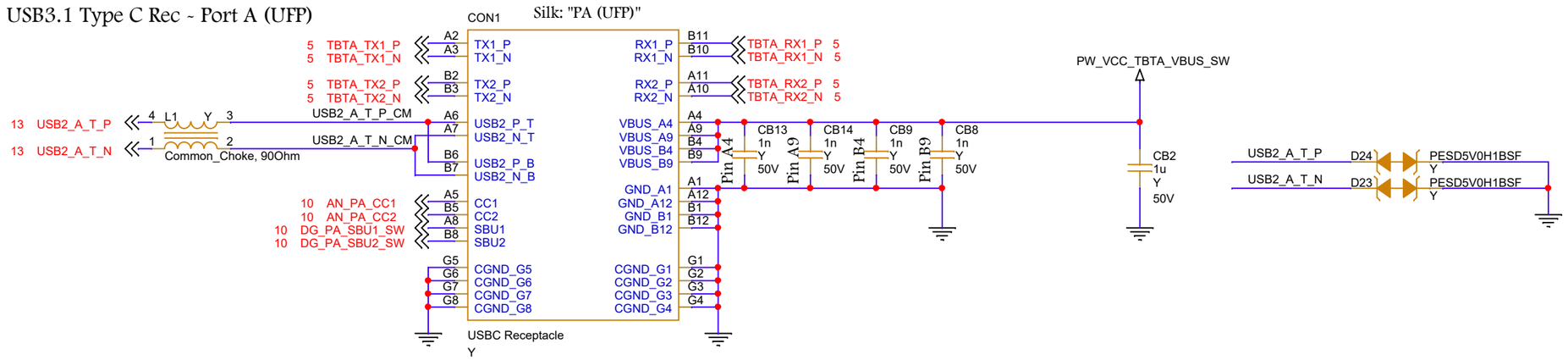
Intel Confidential

THUNDERBOLT

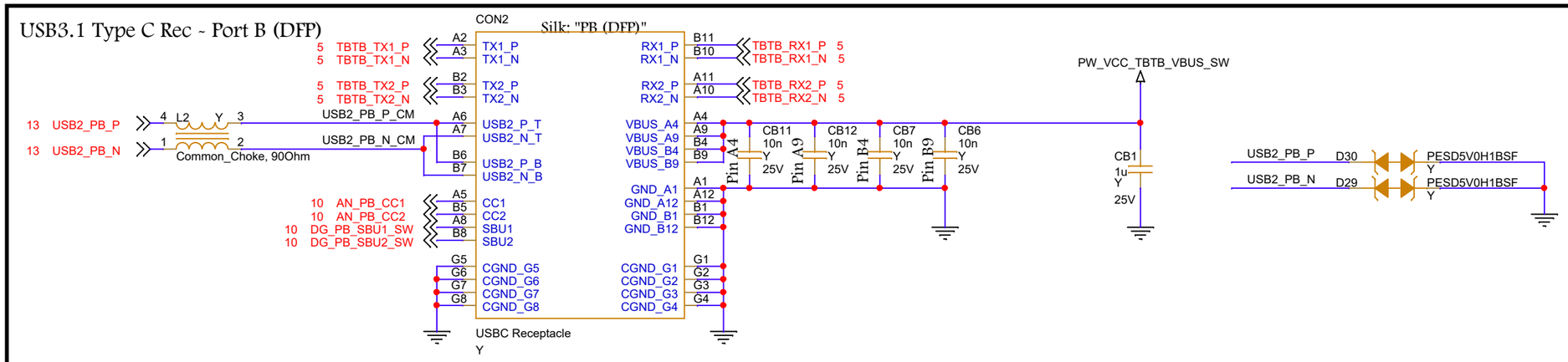
Title: GR - Power & GND Parts		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 7 of 32	

TBT USBC Ports - A, B

USB3.1 Type C Rec - Port A (UFP)



USB3.1 Type C Rec - Port B (DFP)



<Core Design>

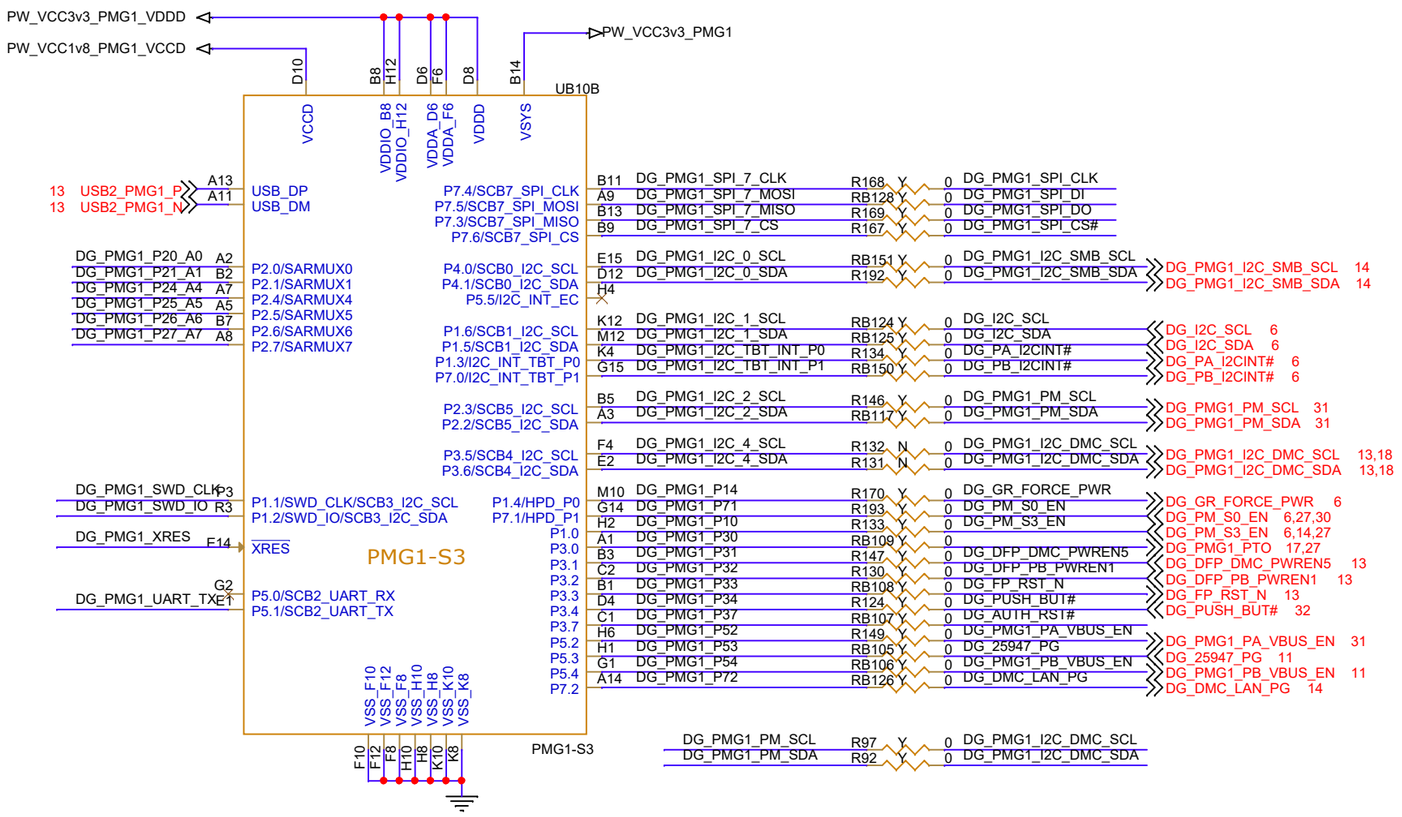
Intel Confidential

THUNDERBOLT

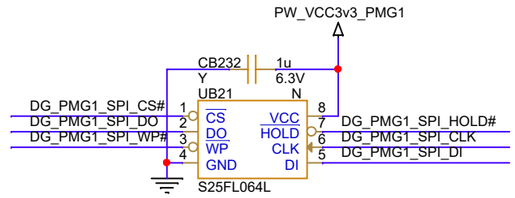
Title: TBT USBC Ports		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 8 of 32	

PMG1-S3 DMC Part

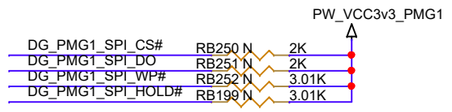
PMG1-S3 Symbol



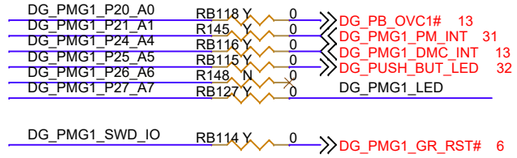
PMG1 16Mbit Flash



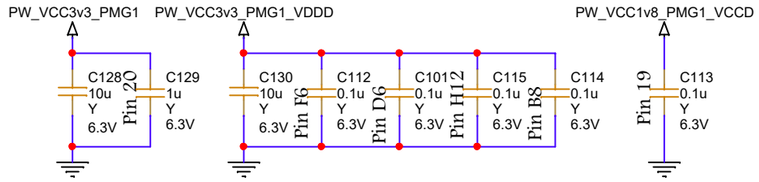
Silk: "PMG1 NVM"



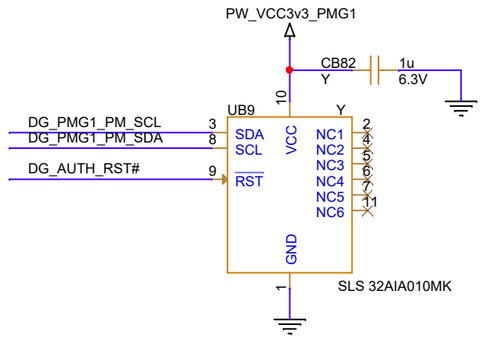
PMG1 GPIOs option



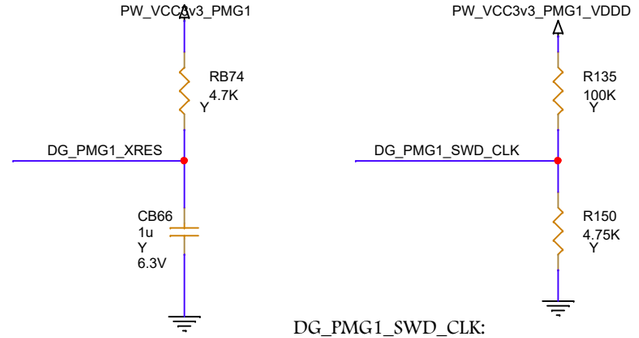
PMG1 Power Supply Filters



PD Authentication TBD

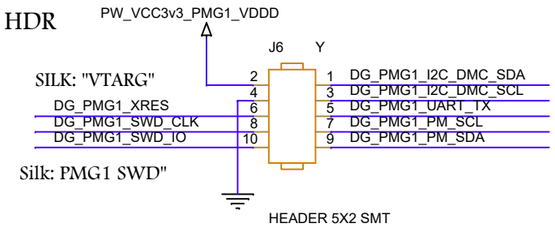


PMG1 HW Configuration



DG_PMG1_SWD_CLK:
Voltage Level for Port A & B, should be between 100mV to 200mV. Typical: 149mV.

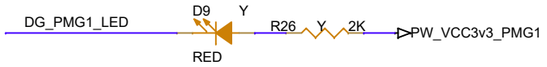
Debug HDR



Silk: PMG1 SWD"

HEADER 5X2 SMT

Debug LED



Silk: PMG1"

<Core Design>

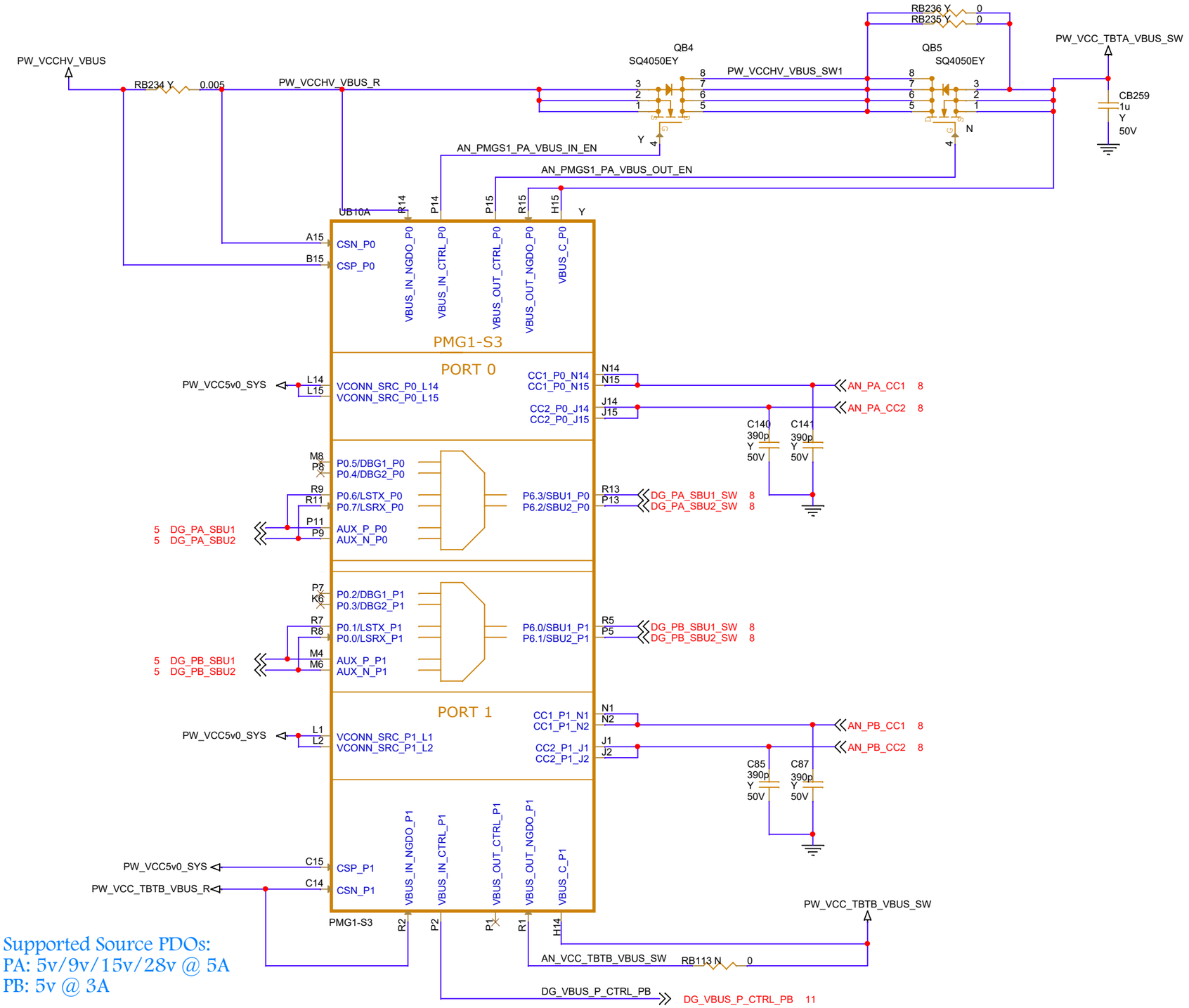
Intel Confidential

THUNDERBOLT

Title: PMG1 Dock Management Controller		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 9 of 32	

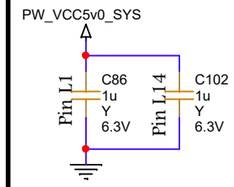
PMG1-S3 (PD Controller) - Port A & B

PMG1-S3 PD Symbol



Supported Source PDOs:
PA: 5v/9v/15v/28v @ 5A
PB: 5v @ 3A

PMG1 Power Supply Filters



<Core Design>

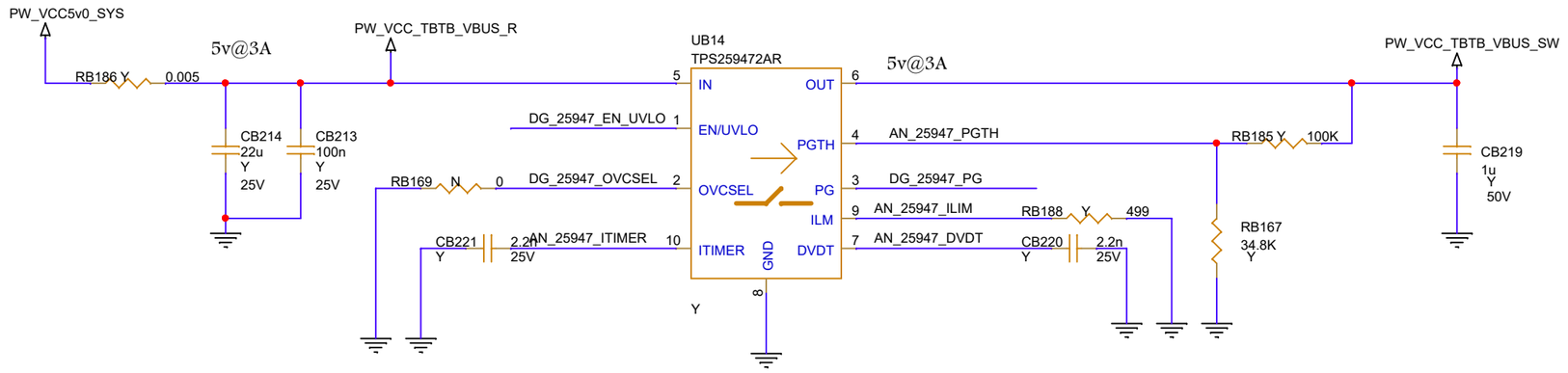
Intel Confidential

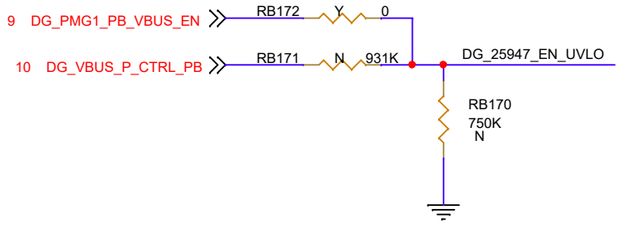
THUNDERBOLT

Title: PMG1 PD Controller		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Sunday, October 17, 2021	Sheet 10 of 32	

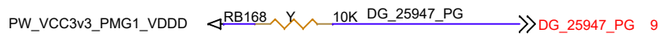
USBC Source Path for PB

Port B ~ VBUS Provider Path





Open ~ OV calmp Th = 5.7V



<Core Design>

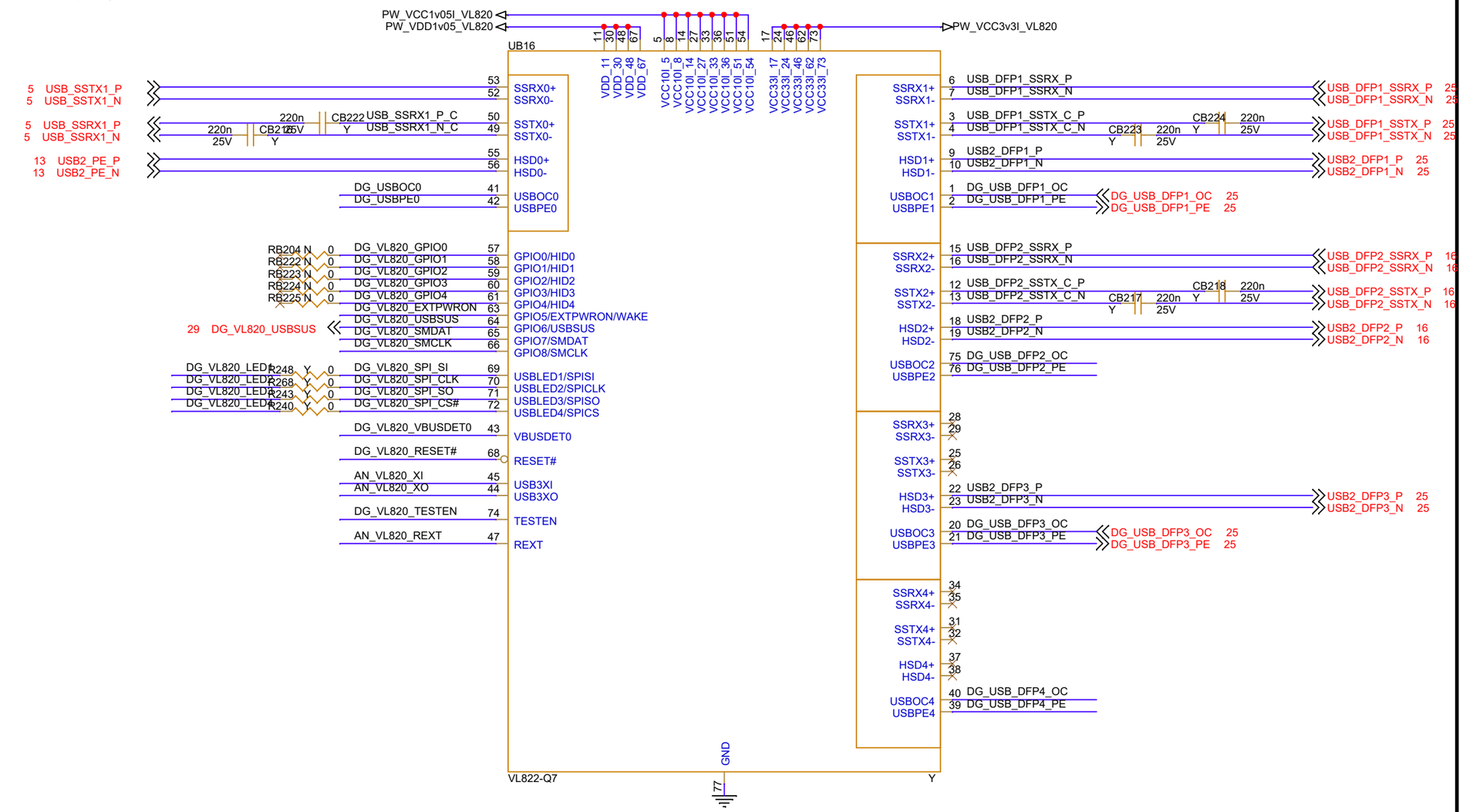
Intel Confidential

THUNDERBOLT

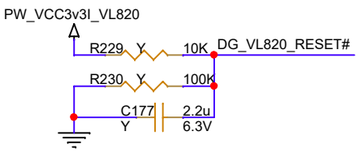
Title: USBC Source Path		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Sunday, October 17, 2021	Sheet 11 of 32	

USB3.1 Gen2 (10Gbps) HUB - VL822-Q7

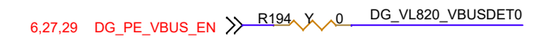
VL822-Q7 Symbol



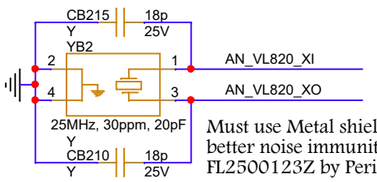
Reset Circuit



VBUS Detect

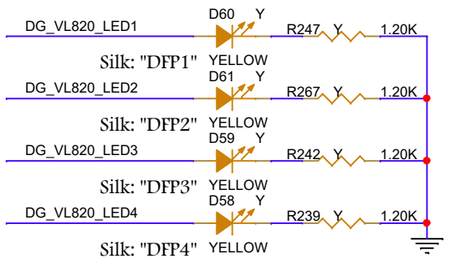


VL822 Crystal 25MHz, 30ppm, 20pF

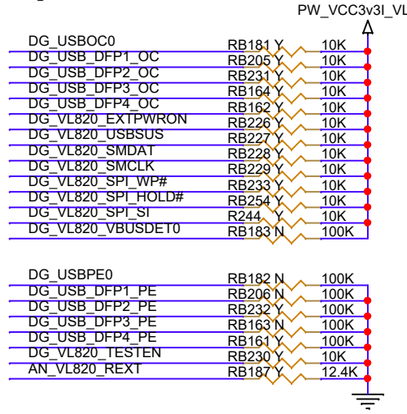


Must use Metal shielded crystal for better noise immunity. (Recommended: FL2500123Z by Pericom)

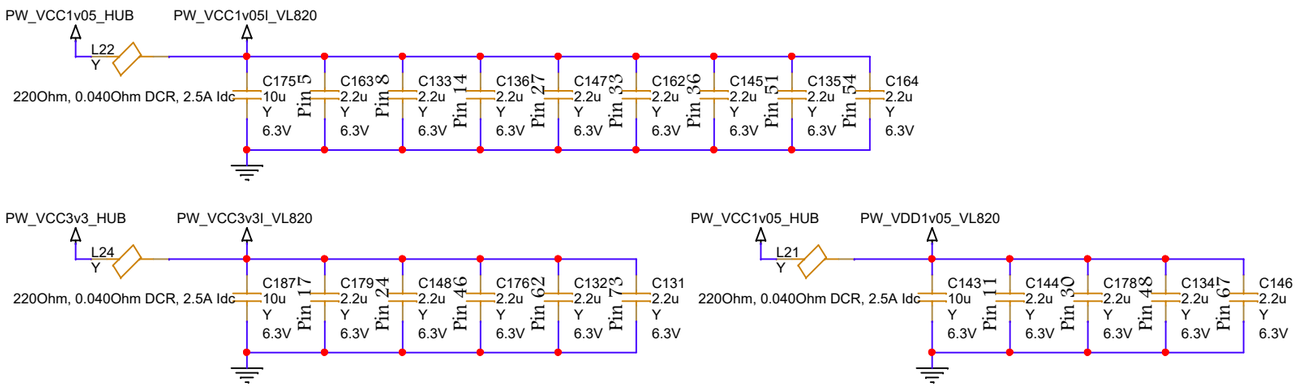
VL822 LEDs



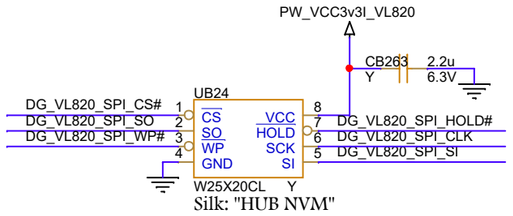
HW Pull-Up/Pull-Down



Power Supply Filters



2Mbit Flash



<Core Design>

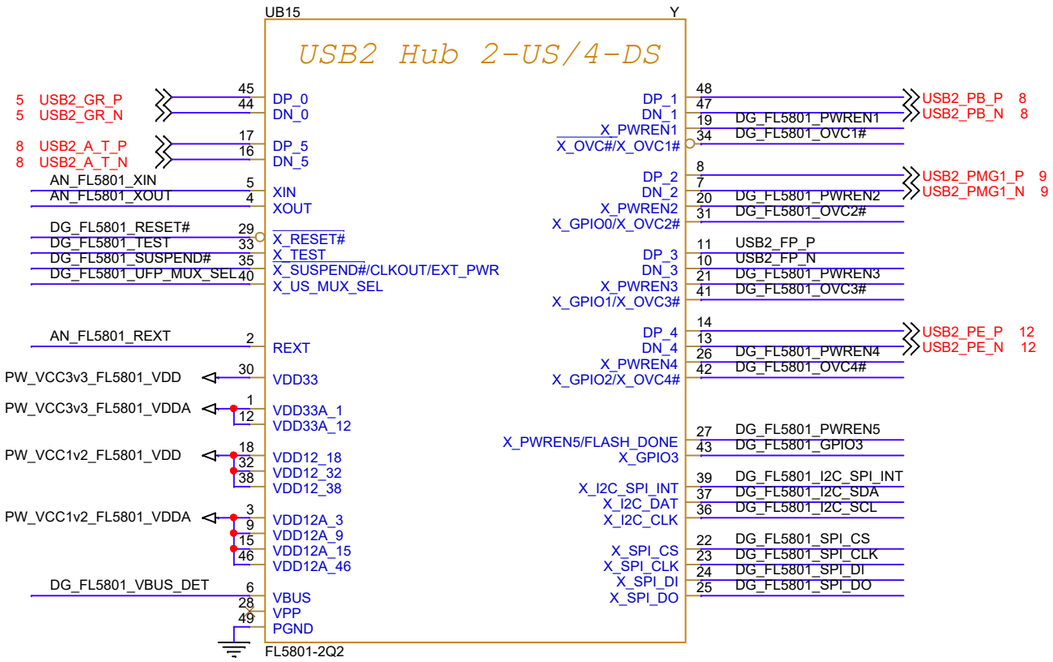
Intel Confidential

THUNDERBOLT

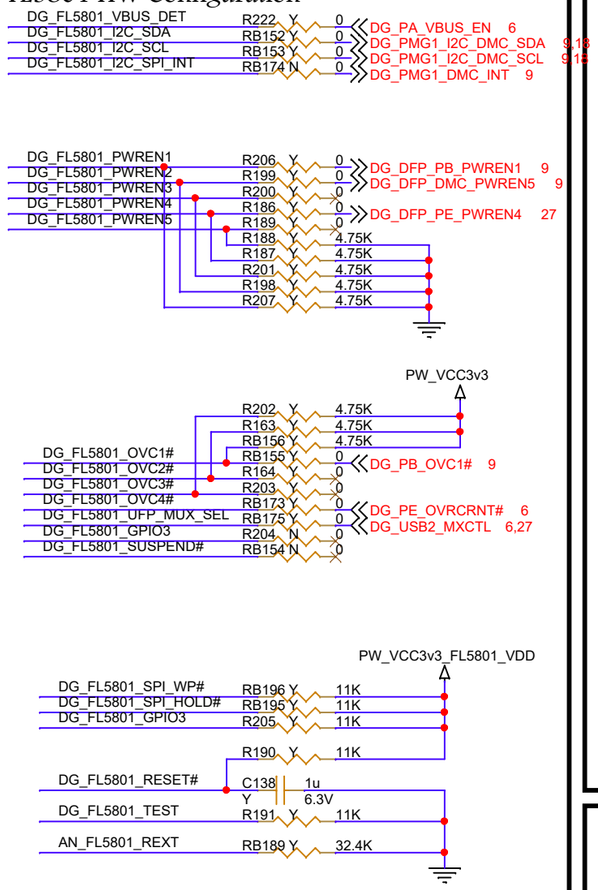
Title	USB3.1 Hub - VL822 Q7	
Size A3	Document Number GALACTICO Main Board	Rev 1.1
Date: Saturday, October 16, 2021	Sheet 12 of 32	

FL5801 - USB2 Hub 1-US/5-DS Configuration

FL5801 Symbol

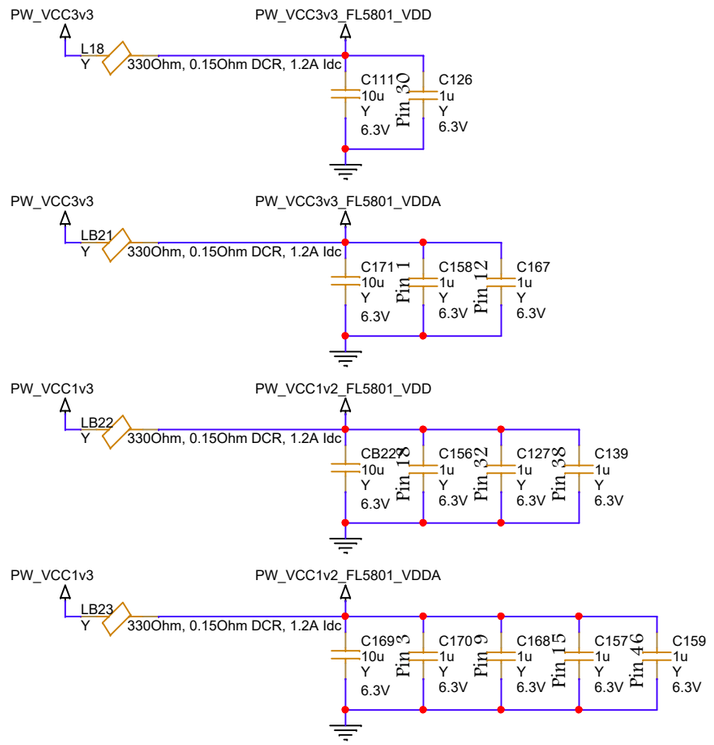


FL5801 HW Configuration

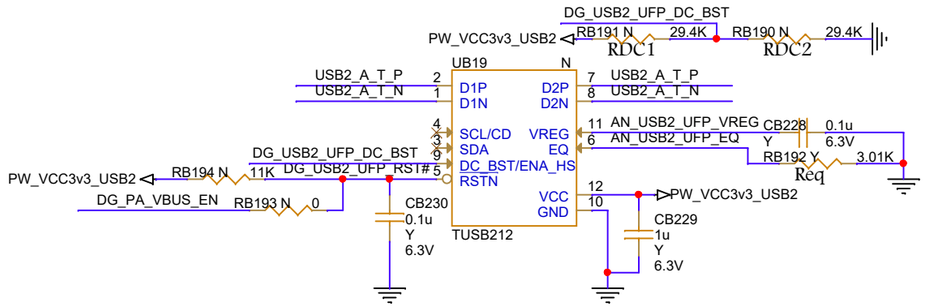


FL5801 Port Mapping
Port 0: GR USB2 (UFP)
Port 1: PB (DFP)
Port 2: DMC (DFP)
Port 3: N/C
Port 4: LAN CTRL (DFP)
Port 5: PA USB2 (UFP)

FL5801 Power Filters



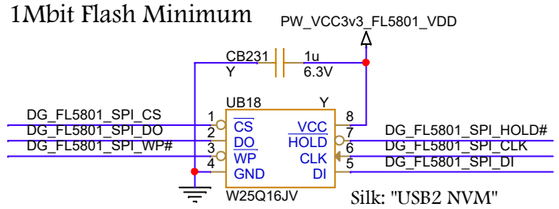
HUB UFP USB2 HS Re-Driver



DG_USB2_UFP_DC_BST:
Sets DC gain of the HS signal
VIL (40mV) : RDC1 = 'Y' ; RDC2 = 'N'
VIM (60mV): RDC1 = 'N' ; RDC2 = 'N'
VIH (80mV): RDC1 = 'N' ; RDC2 = 'Y'

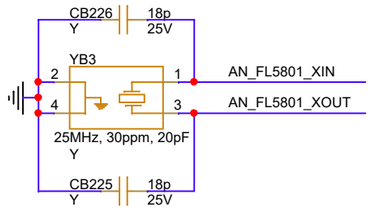
AN_USB2_UFP_EQ:
Sets AC boost of the HS signal
Level 0: Req = 0 Ohm
Level 1: Req = 1.69KOhm
Level 2: Req = 3.92KOhm
Level 3: Req = NA

1Mbit Flash Minimum

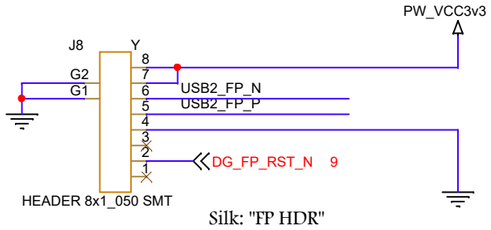


Silk: "USB2 NVM"

25MHz, 30ppm, 20pF 2.0 x 1.6 mm Crystal



FP interface



Silk: "FP HDR"

<Core Design>

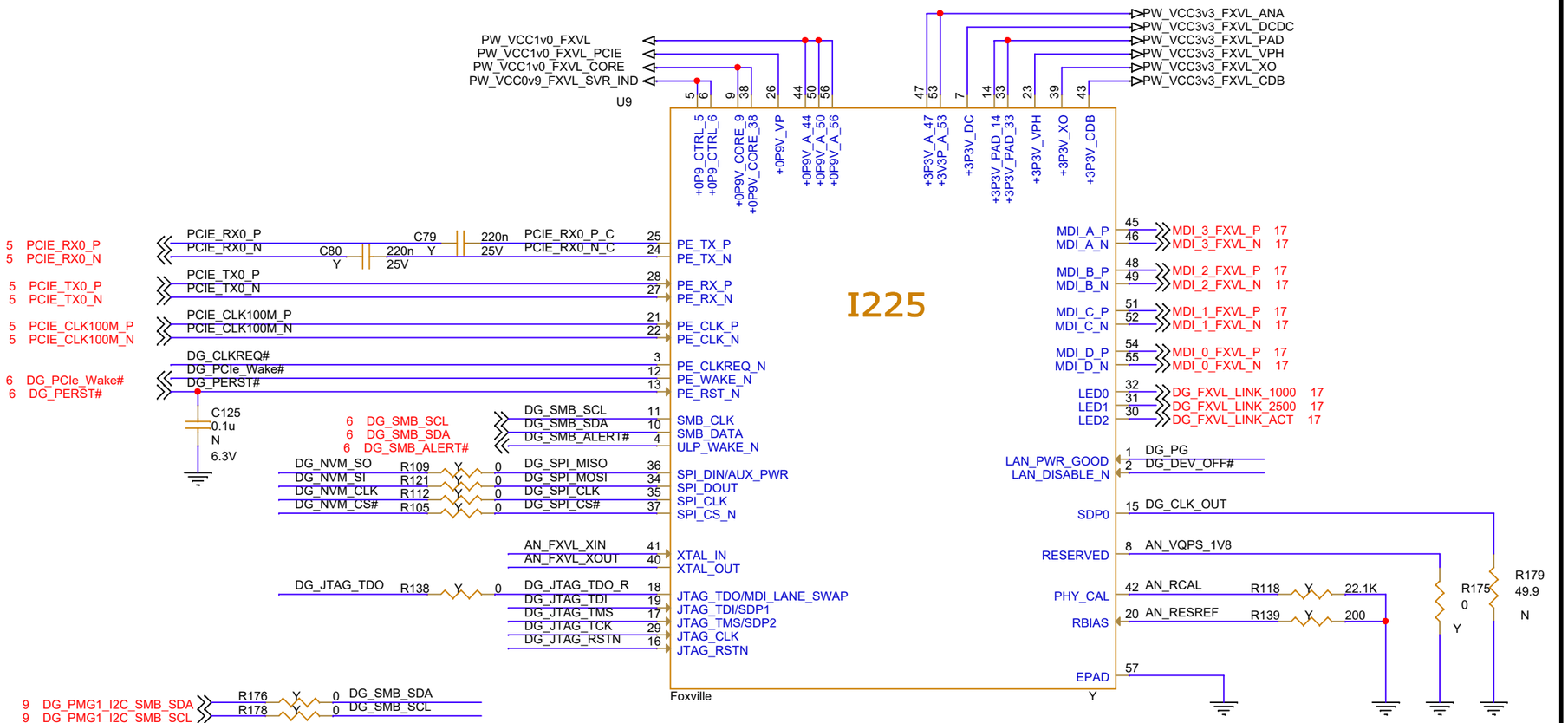
Intel Confidential

THUNDERBOLT

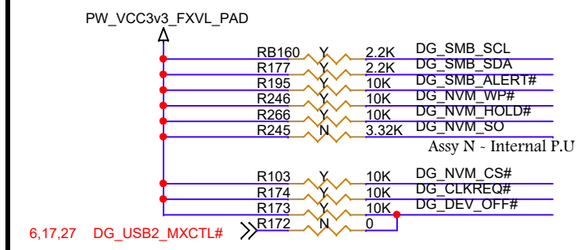
Title: USB2 Hub - FL5801		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 13 of 32	

Foxville

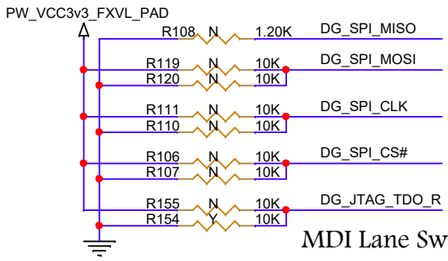
Foxville Main



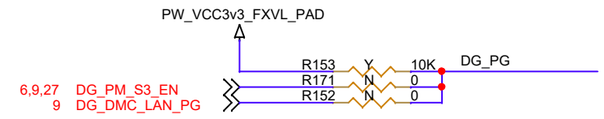
Foxville PU/PD



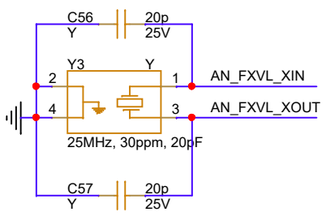
Foxville HW Strapping



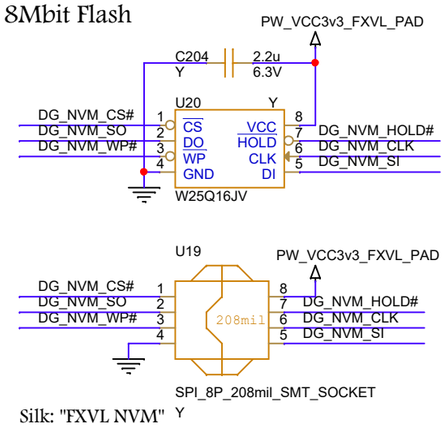
Foxville On Off (vPRO Mac addr rst)



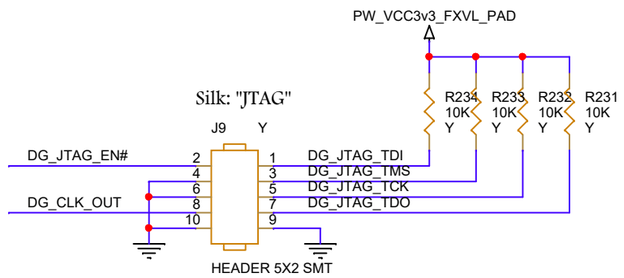
Foxville 25MHz / 3225 SMD Crystal



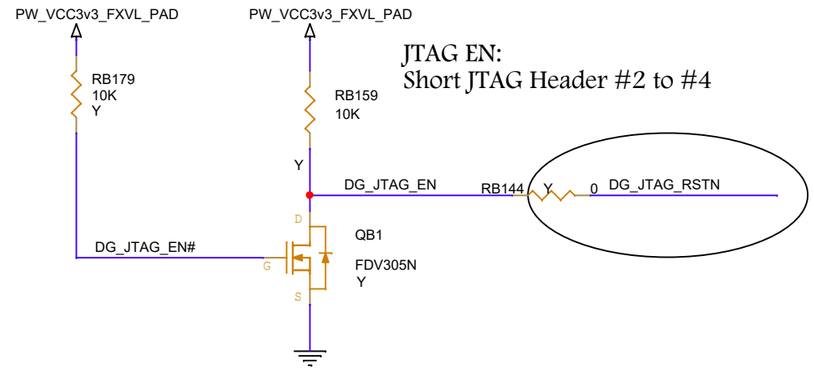
8Mbit Flash



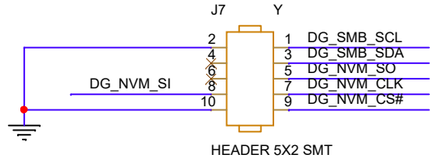
JTAG Header (Debug Only)



JTAG EN



AARDVARK Header (Debug Only)



<Core Design>

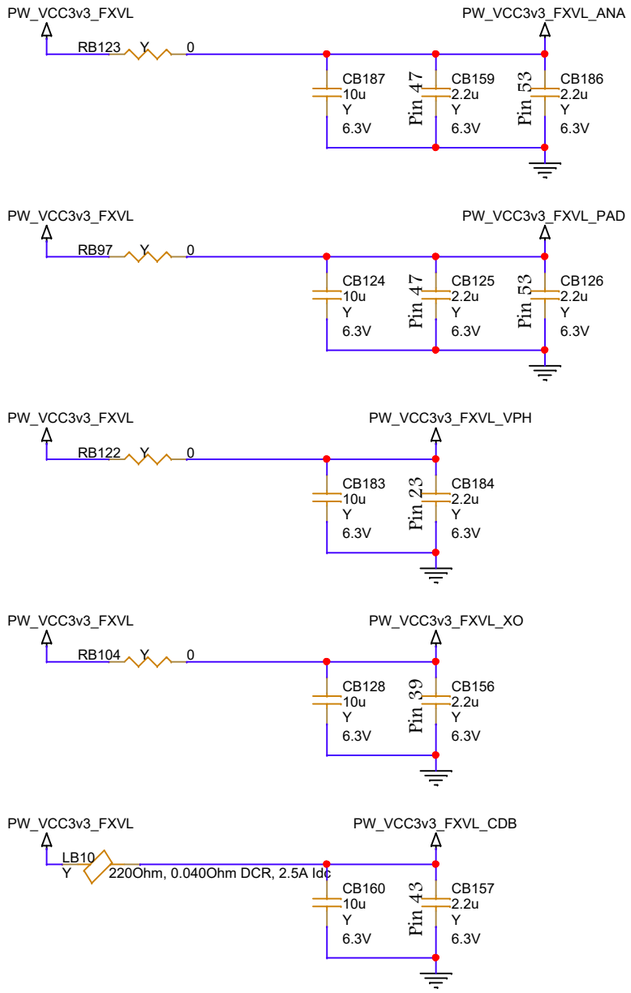
Intel Confidential

THUNDERBOLT

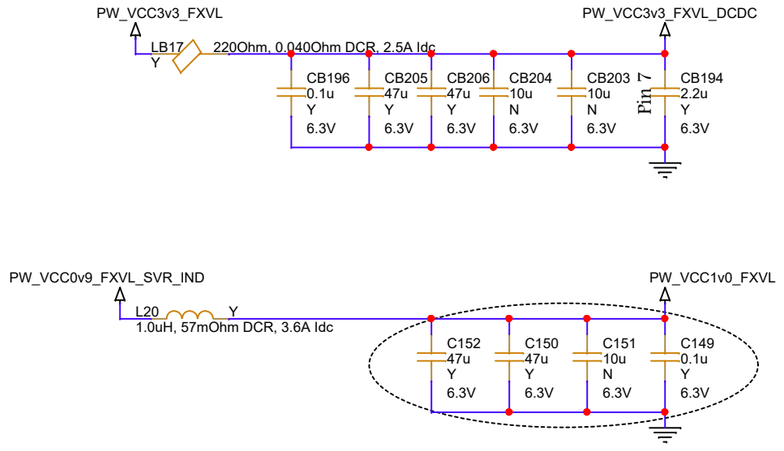
Title: Foxville - Main		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 14 of 32	

Foxville - Power Filtering and iSVR

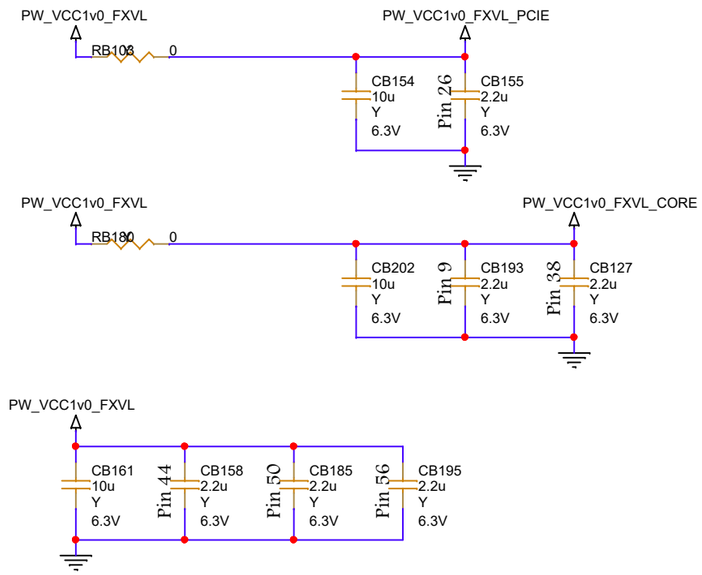
3.3V Filtering



Foxville Internal SVR



1.0V Filtering



<Core Design>

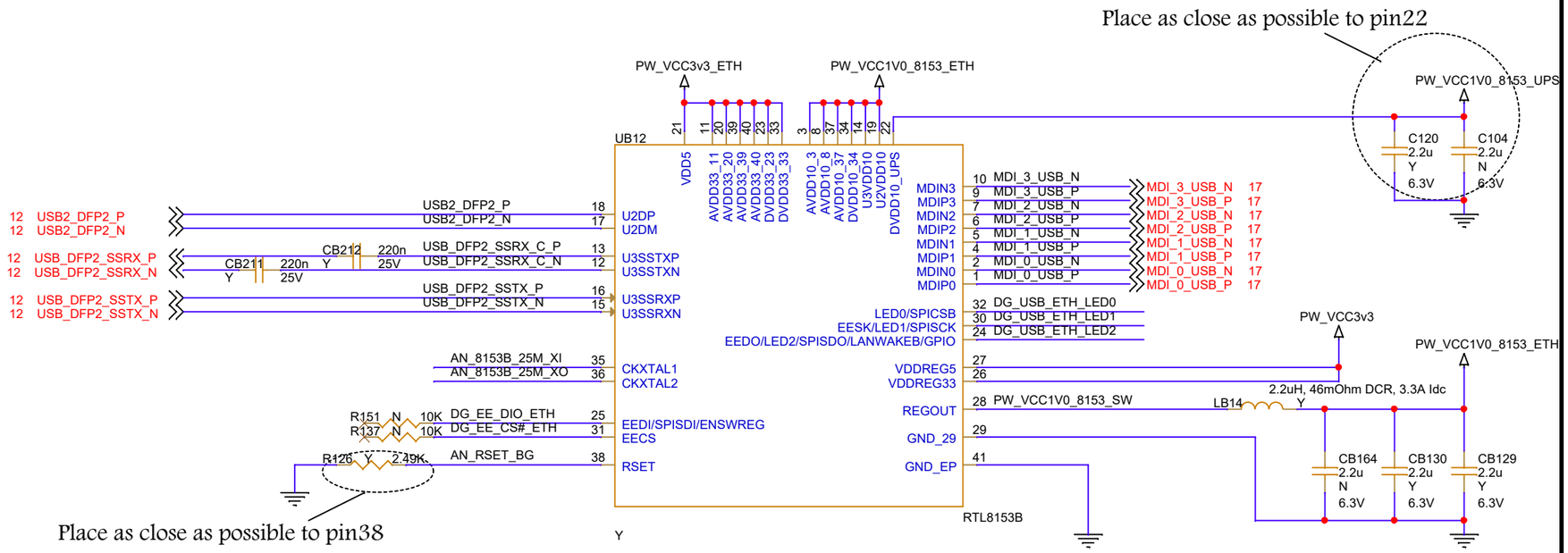
Intel Confidential

THUNDERBOLT

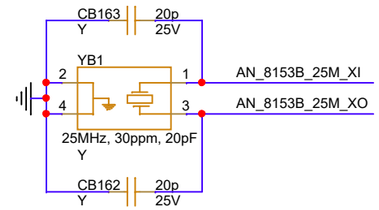
Title: Foxville - Power		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 15 of 32	

RTL8153B - USB3.0 to 10/100/1000M Gigabit ETH Controller

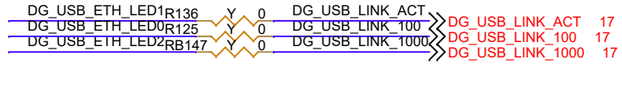
RTL8153B USB3.0 to Ethernet Controller



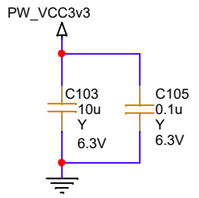
25MHz, 30ppm, 20pF LAN Crystal



USB ETH LED Signals



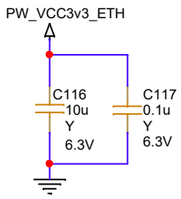
SVR VIN Capacitors



Place as close as possible to pin27

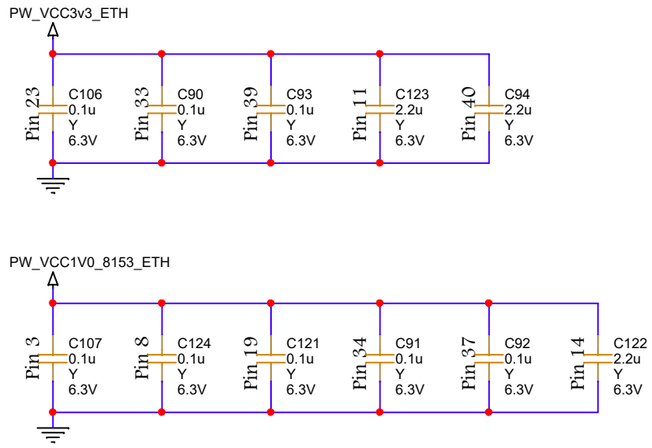
IC Power Circuit

3.3v @ 200mA



Place as close as possible to pin21

IC Decoupling



<Core Design>

Intel Confidential

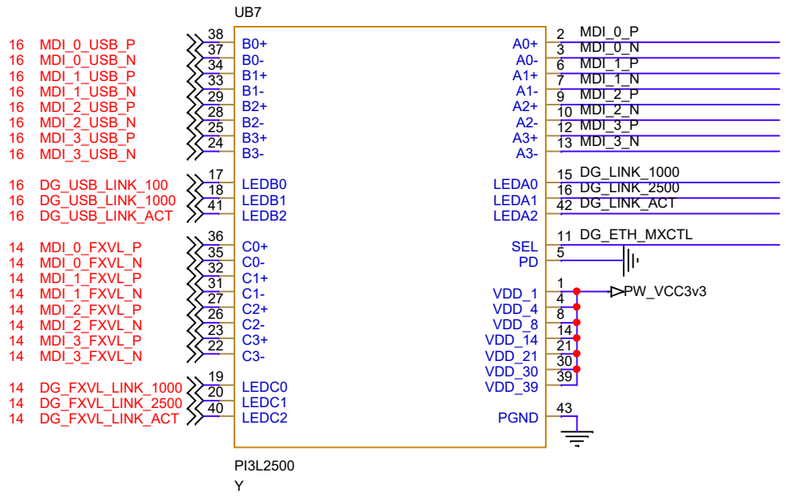
THUNDERBOLT

Title: RTL8153 USB ETH Controller		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 16 of 32	

Ethernet Connector

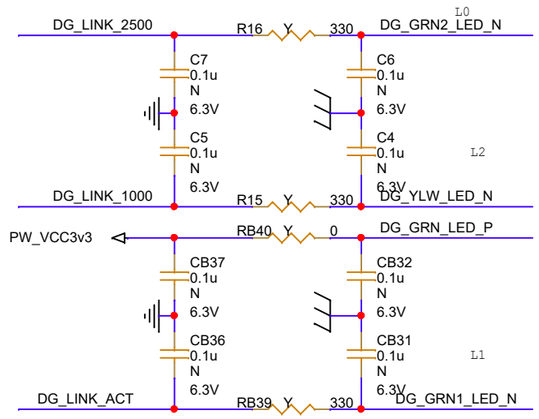
PI3L2500 Symbol

Ethernet 2:1 Switch



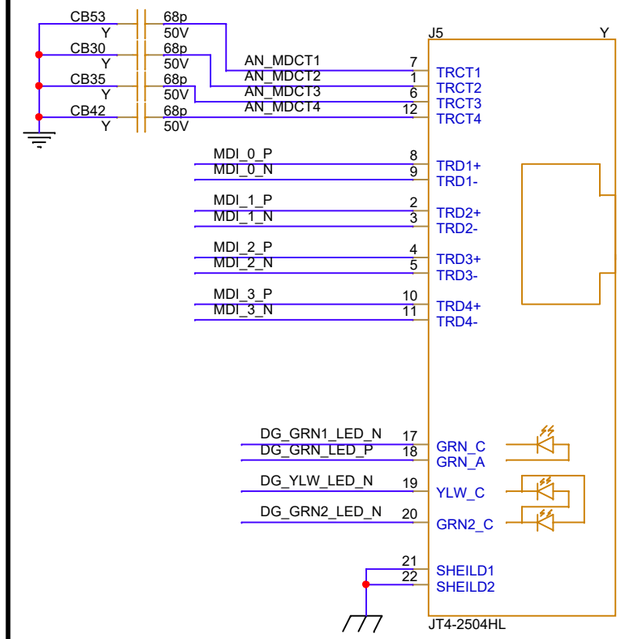
SEL '0' [PCIE TNL] - Bx -> Ax
SEL '1' [No PCIe] - Cx -> Ax

RJ45 LEDs Circuit

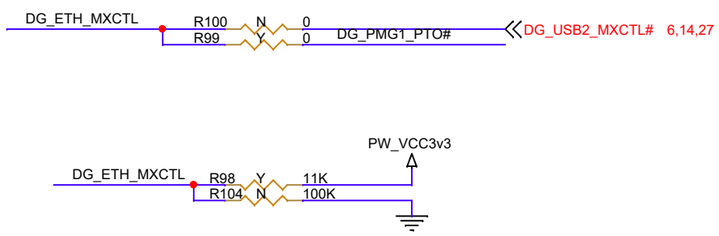


LEDs Defaults:
0 - LED 100/1G Yellow
1 - LED 2.5G Green
2 - LED LINKUP
All LEDs are active low.

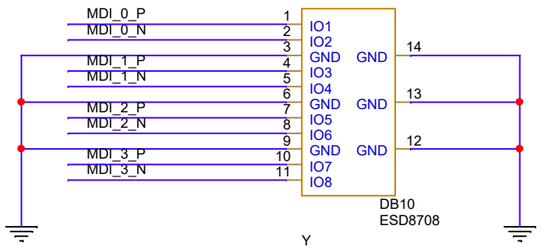
LAN RJ45 + Magnetics



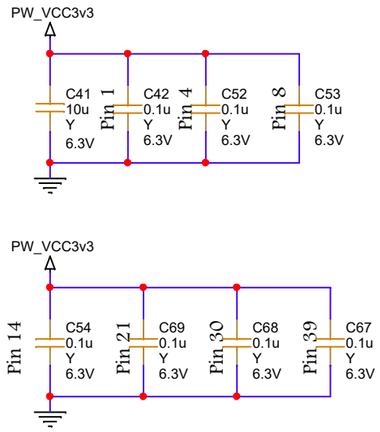
ETH MUX Control



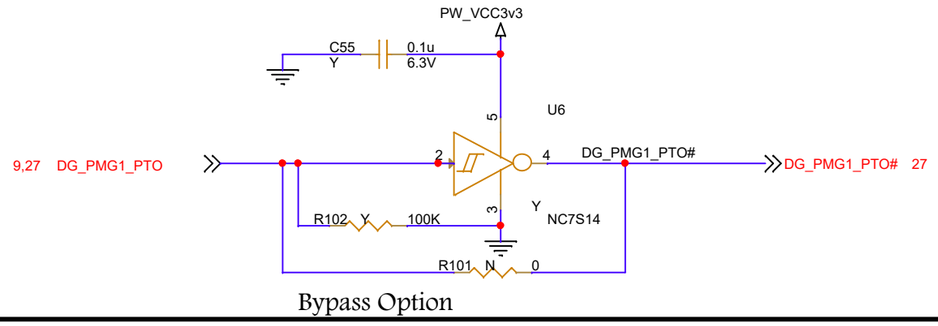
ESD Protection



PI3L2500 Decoupling

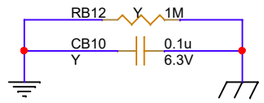


vPRO Enabled/Disabled



Bypass Option

GND Isolation



<Core Design>

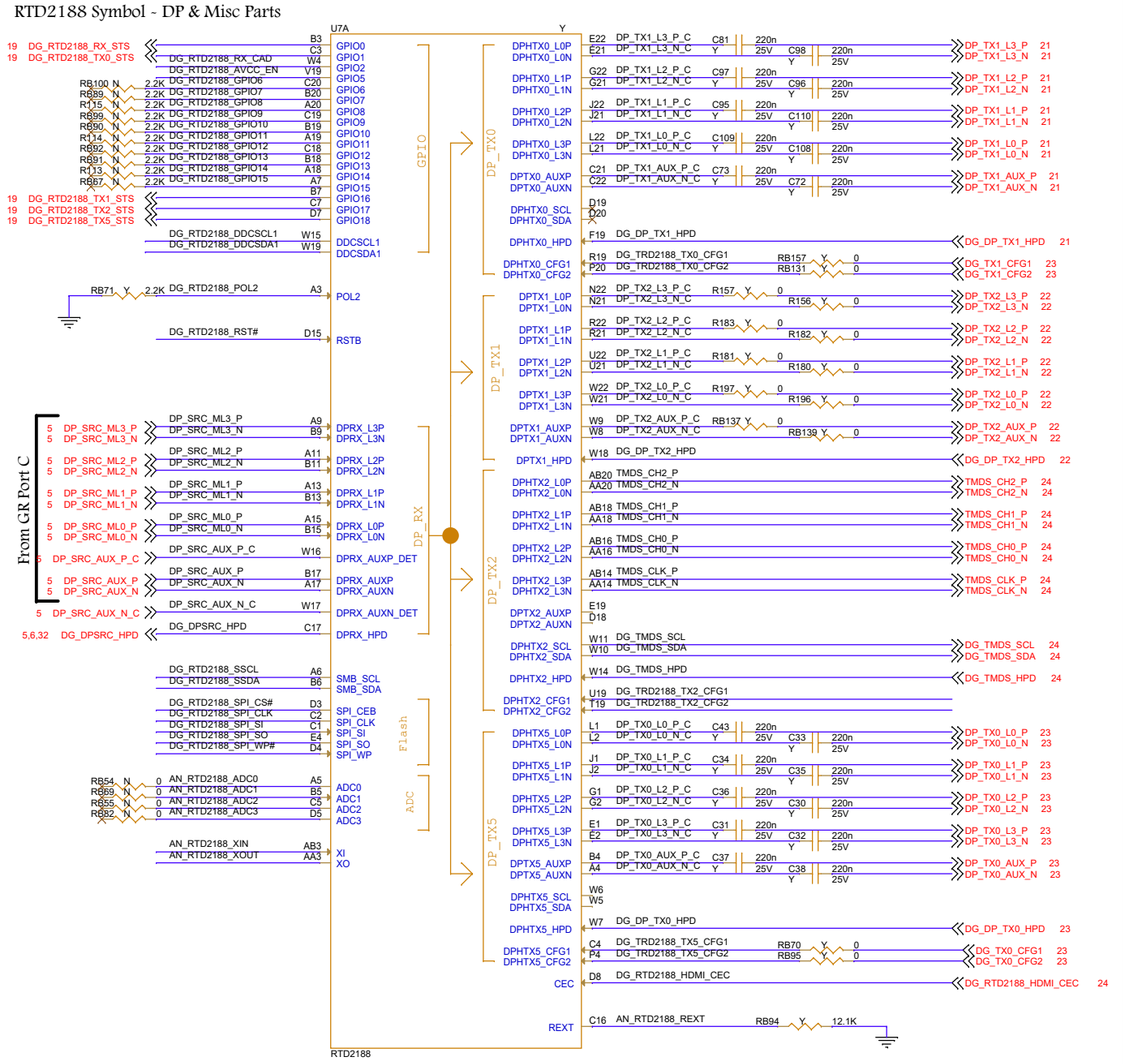
Intel Confidential

THUNDERBOLT

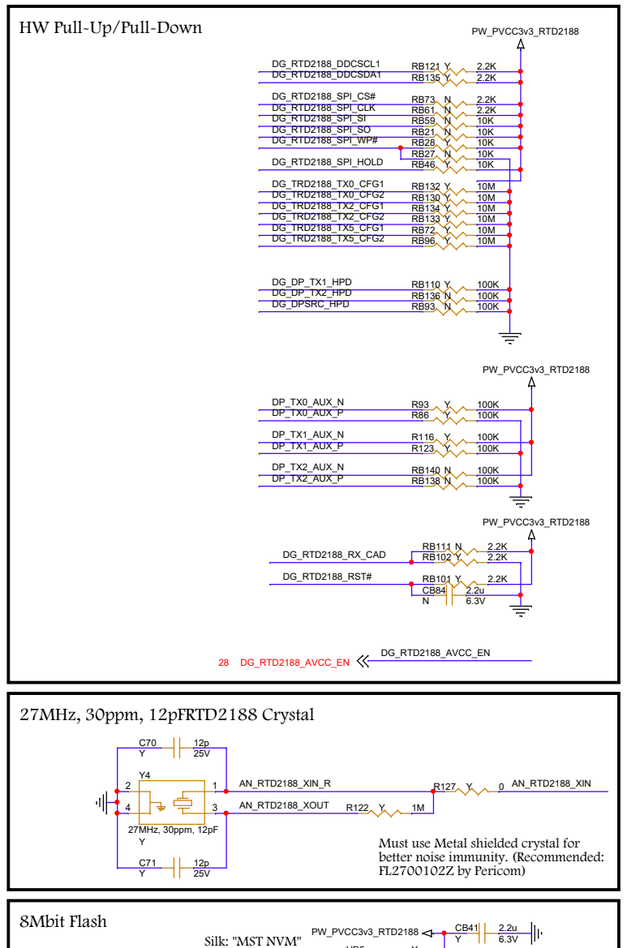
Title: 2.5GbE 2:1 Mux		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 17 of 32	

DP1.4 MST HUB (RTD2188) - High Speed & Misc.

RTD2188 Symbol - DP & Misc Parts



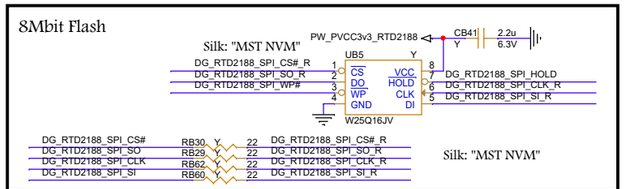
HW Pull-Up/Pull-Down



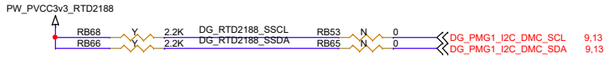
27MHz, 30ppm, 12pFRTD2188 Crystal

Must use Metal shielded crystal for better noise immunity. (Recommended: FL2700102Z by Pericom)

8Mbit Flash

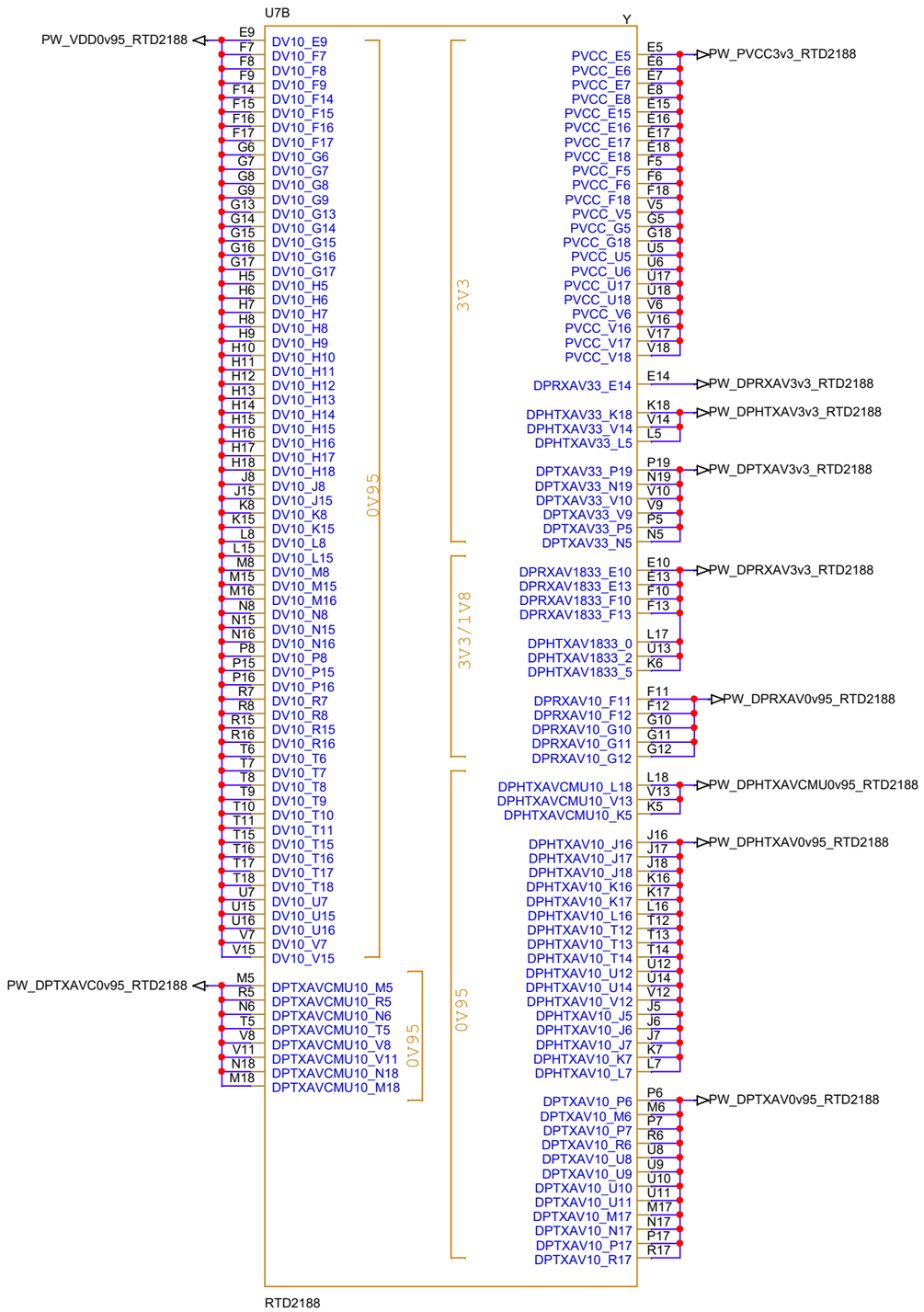


RTD2188 I2C

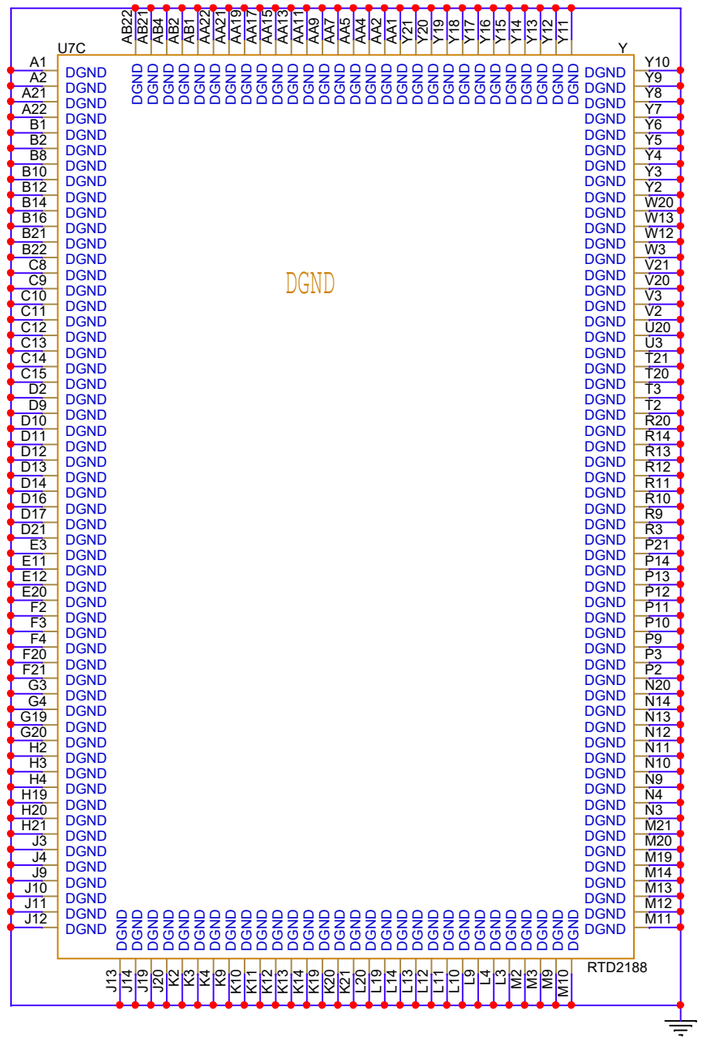


DP1.4 MST HUB (RTD2188) - Power

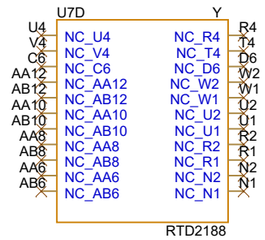
RTD2188 Symbol - POWER Part



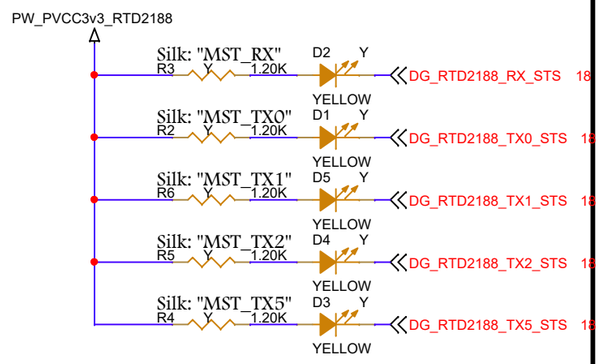
RTD2188 Symbol - GND Part



RTD2188 Symbol - N.C. Part



DP Stream Status



<Core Design>

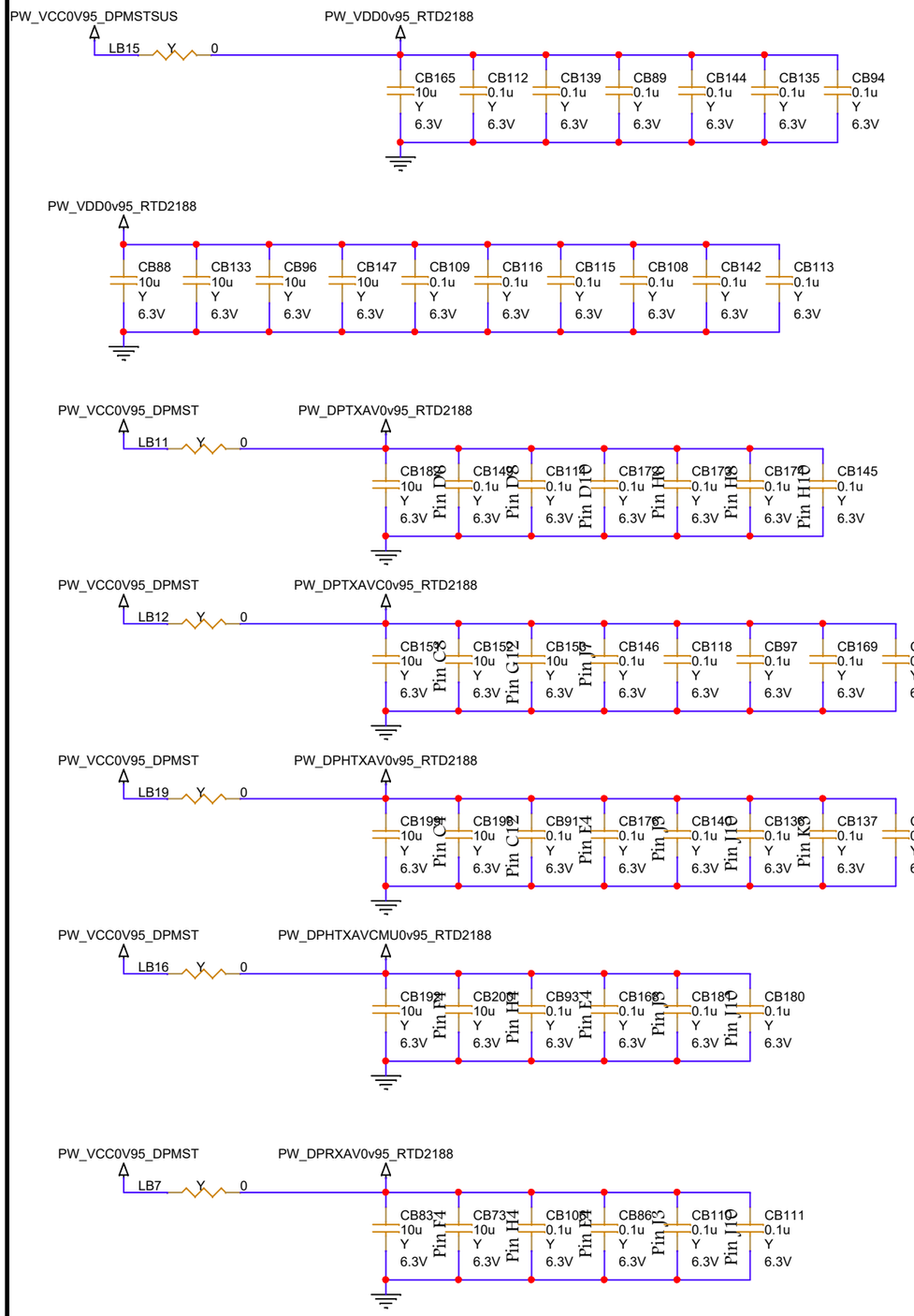
Intel Confidential

THUNDERBOLT

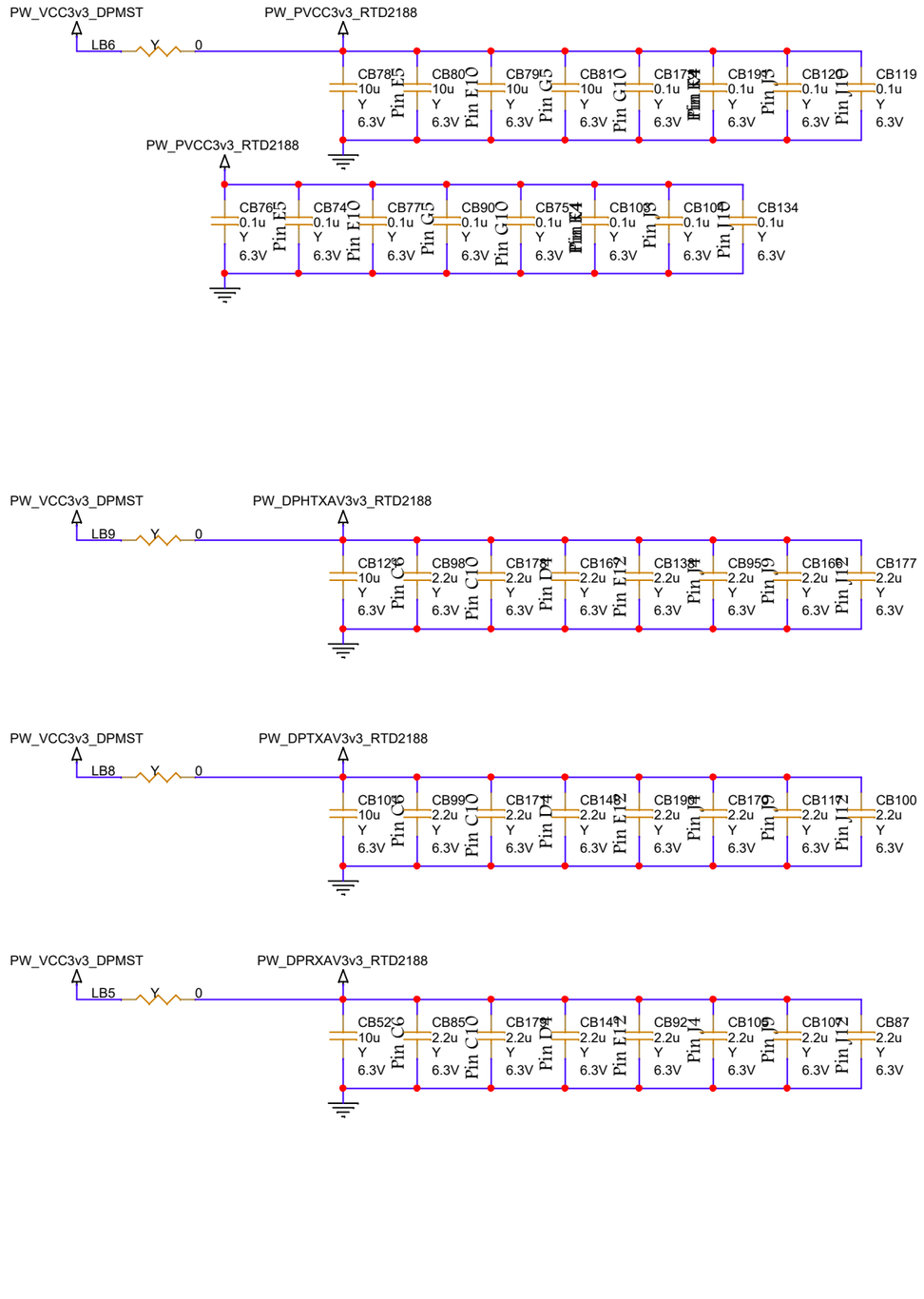
Title: DP1.4 MST Hub - Power		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 19 of 32	

DP1.4 MST HUB (RTD2188) - Filters

0v95 Power Supply Filters



3v3 Power Supply Filters



<Core Design>

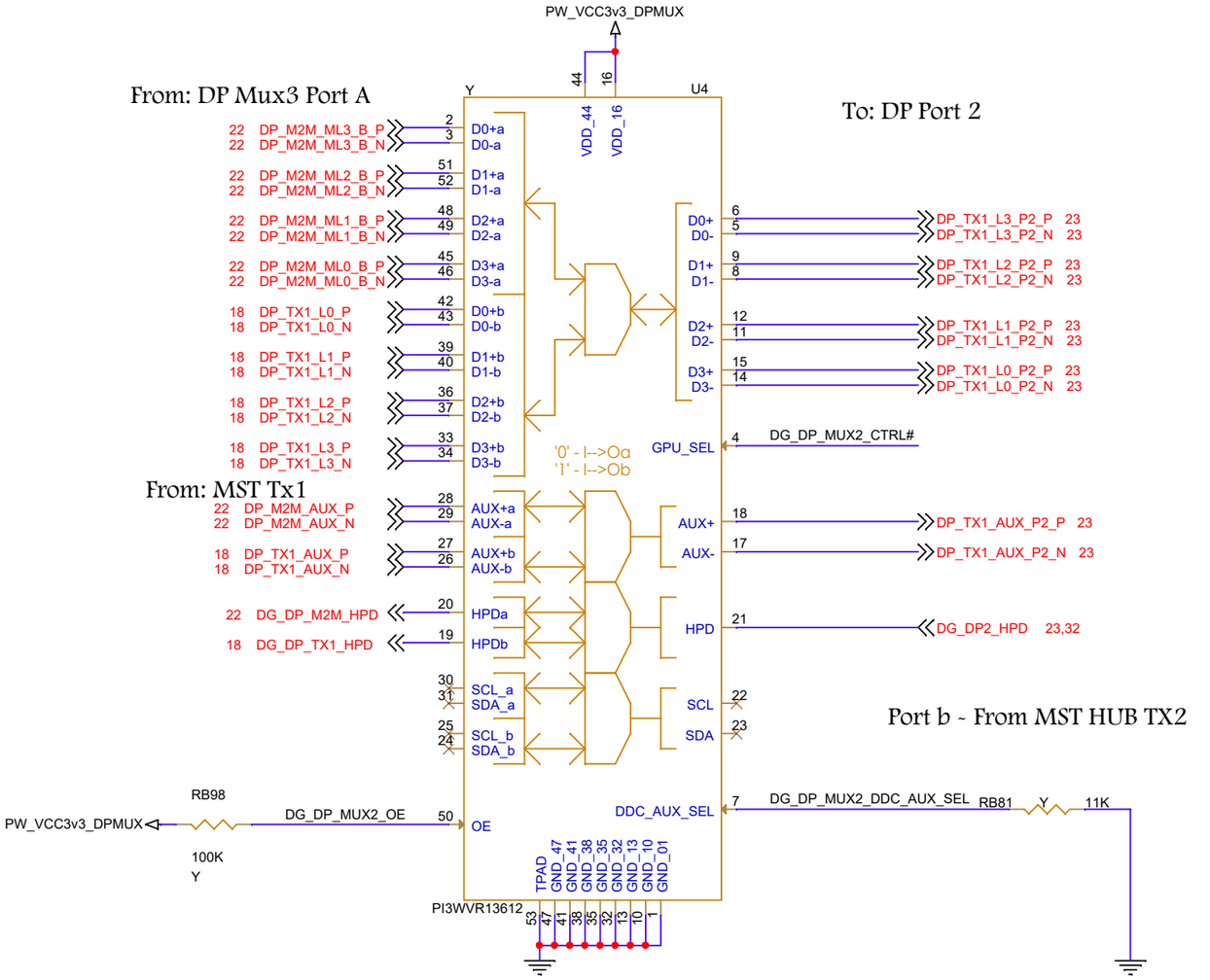
Intel Confidential

THUNDERBOLT

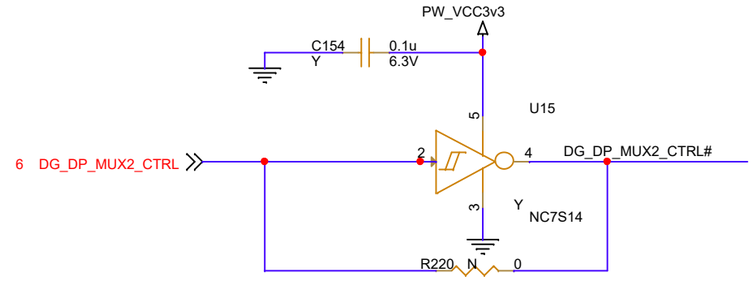
Title: DP1.4 MST Hub - Filters		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 20 of 32	

DP MUX 2

DP Mux2

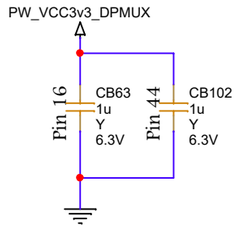


Mux Control Inverter



Bypass Option

DP Mux 2 Decoupling



<Core Design>

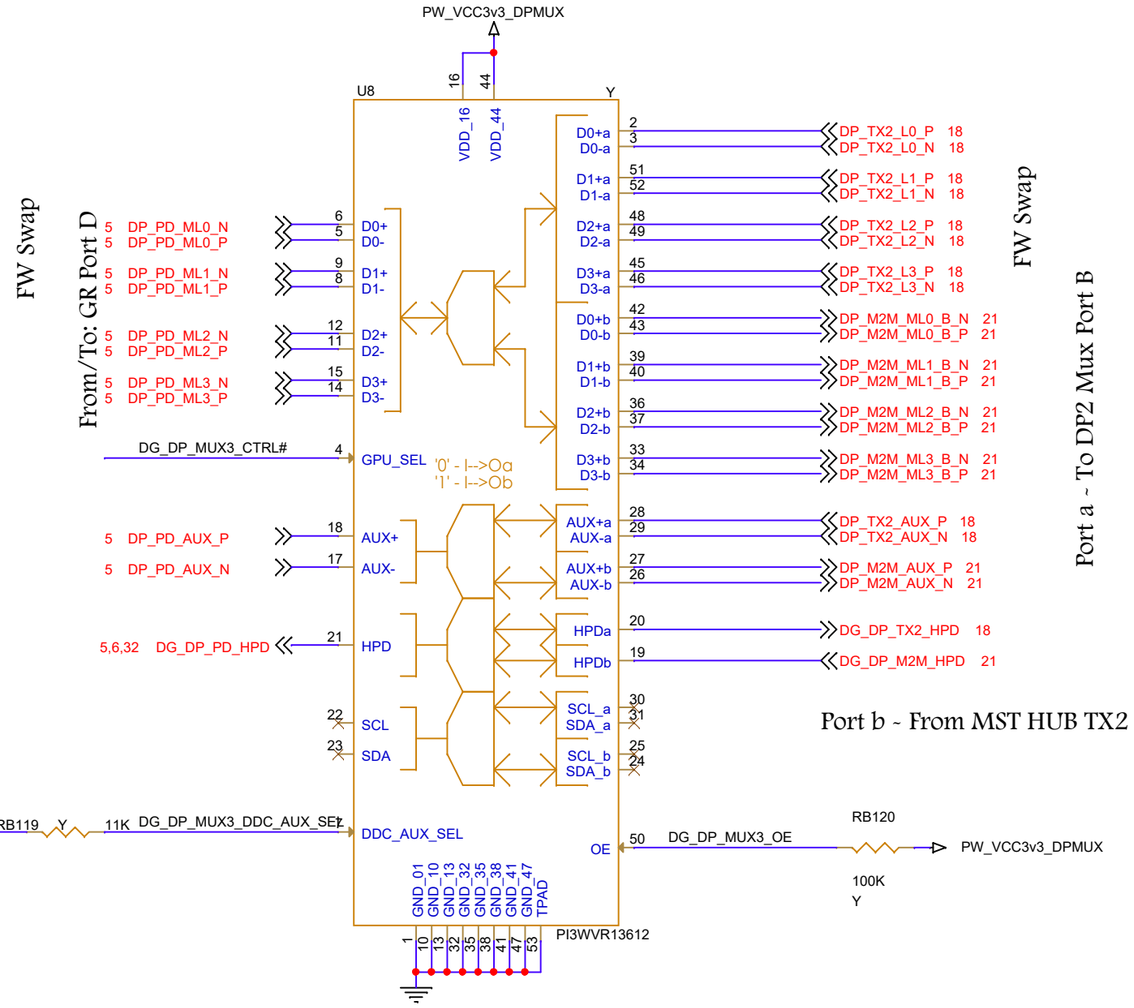
Intel Confidential

THUNDERBOLT

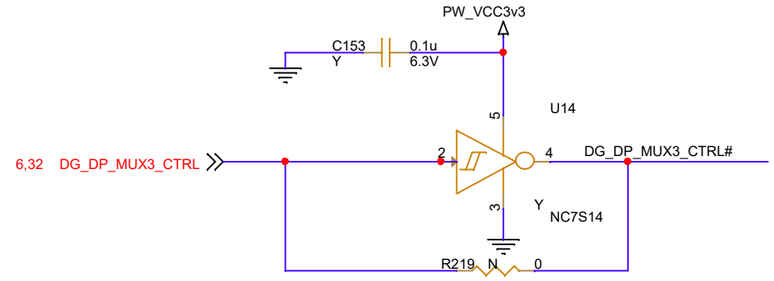
Title: DP TX1 MUX		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 21 of 32	

DP MUX 3

DP Mux3

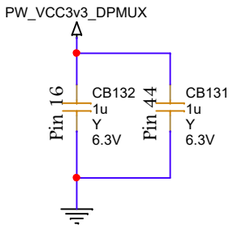


Mux Control Inverter



Bypass Option

DP Mux3 Decoupling



<Core Design>

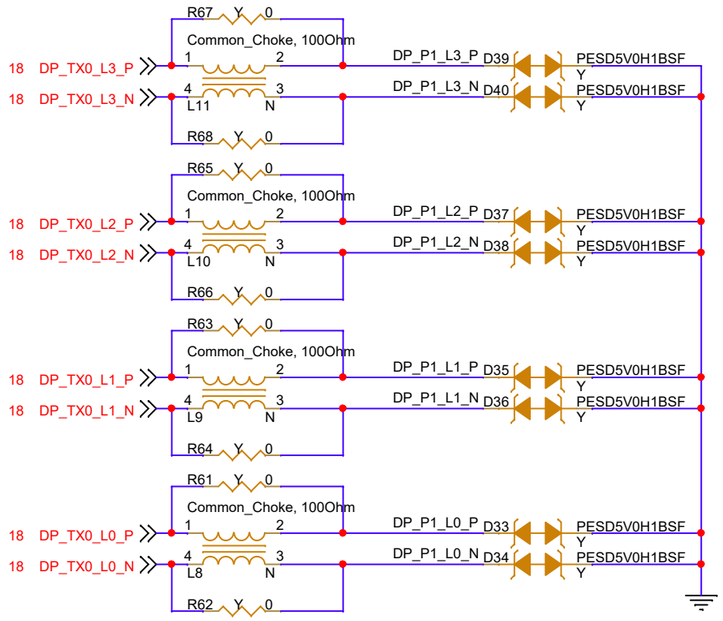
Intel Confidential

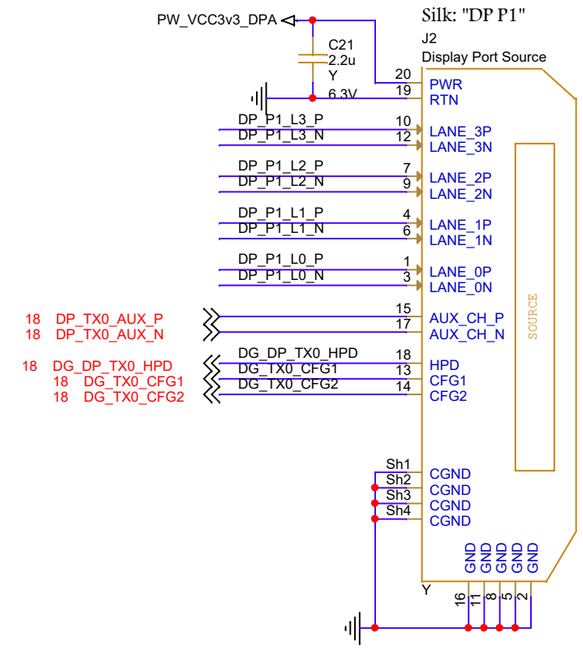
THUNDERBOLT

Title: DP TX2 MUX		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 22 of 32	

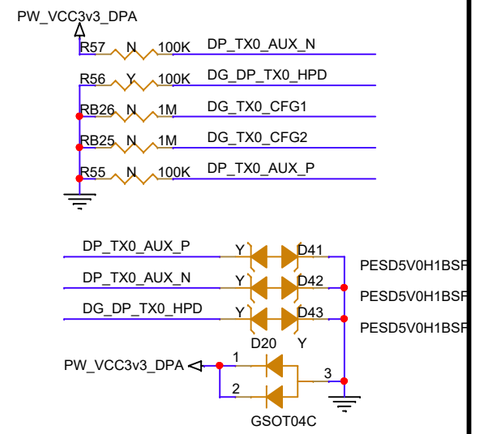
Display Ports

TX0 Display Port (DP 1.4)





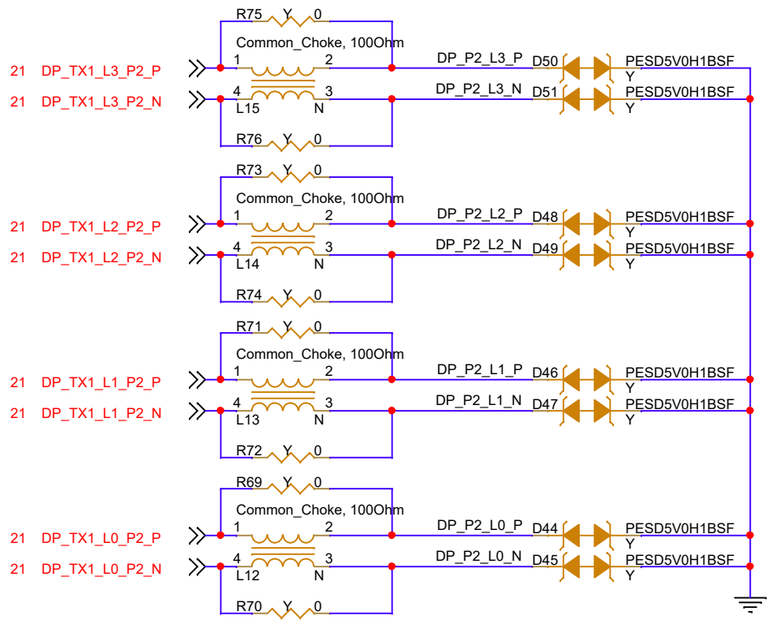
HW Pull-Up/Pull-Down

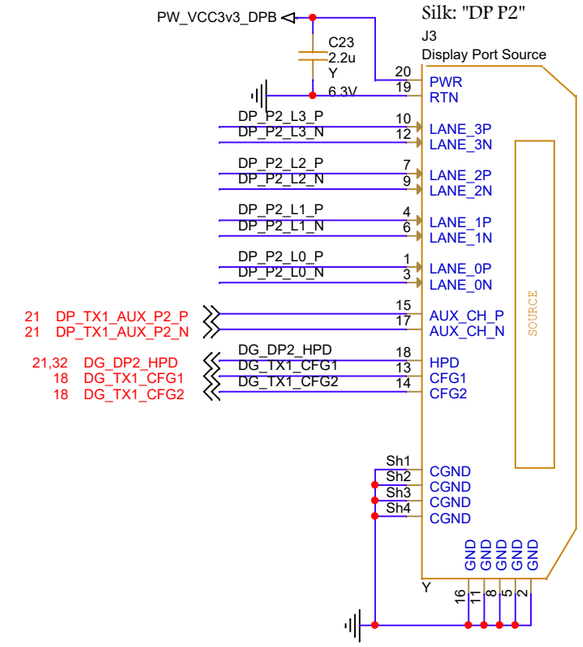


AUX Detection for DP TX0:
Assy near MST TX0

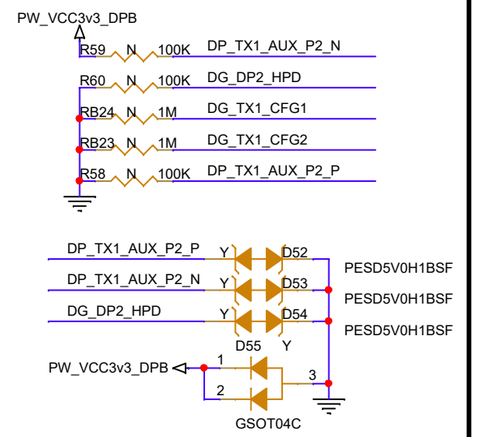
DG_DP1_HPD P.D. Assy near MST TX0

TX1 Display Port (DP 1.4)





HW Pull-Up/Pull-Down



AUX Detection for DP TX1:
Assy near MST Hub Tx1/GR_PD

DG_DP2_HPD P.D. Assy near GR SRC_HPD and MST Hub Tx1

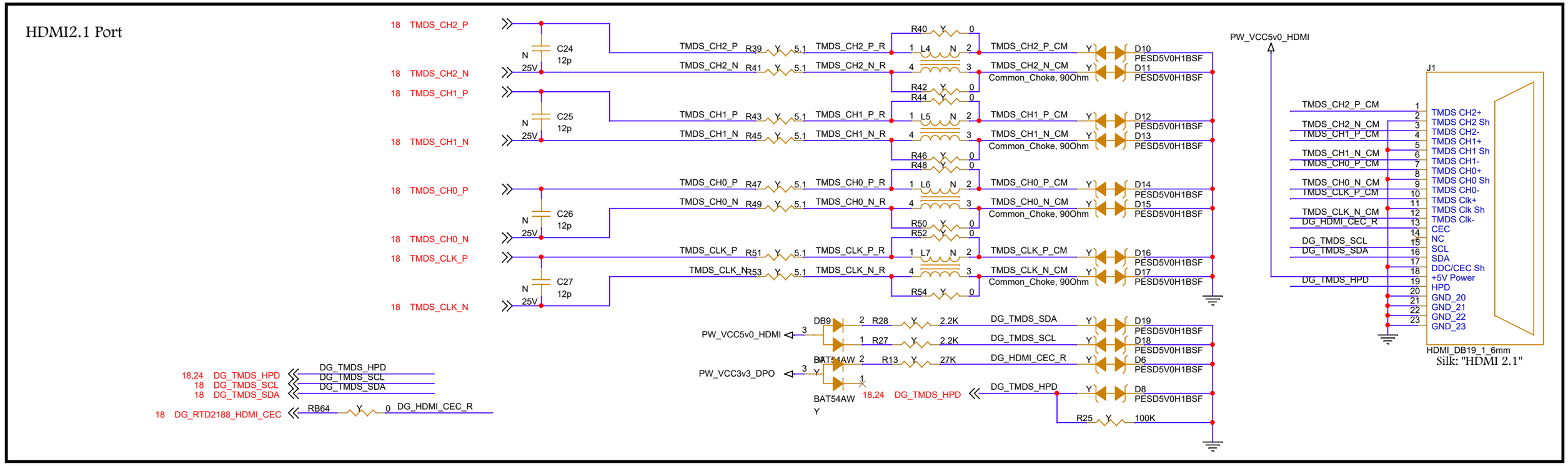
<Core Design>

Intel Confidential

THUNDERBOLT

Title: Display Ports		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 23 of 32	

HDMI2.1 Port



<Core Design>

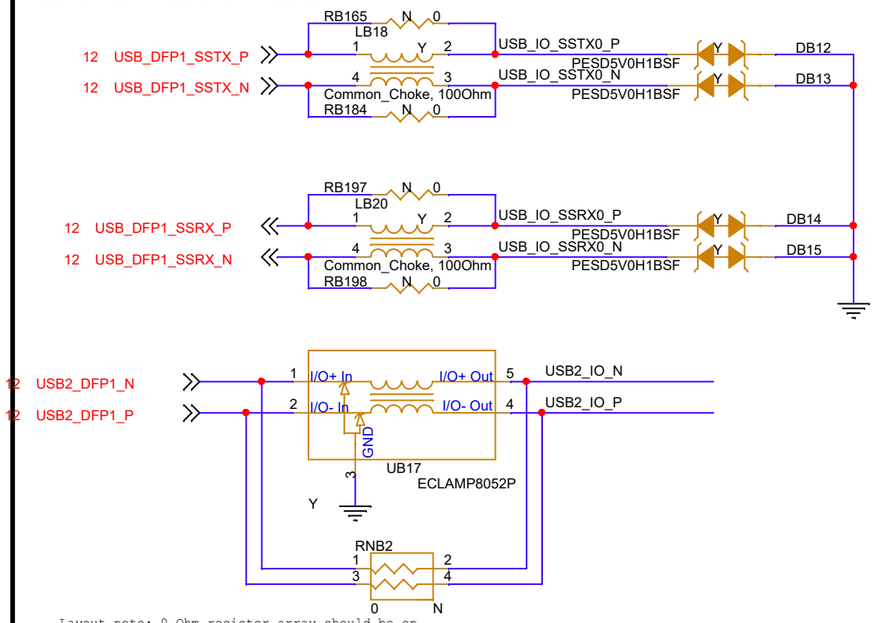
Intel Confidential

THUNDERBOLT

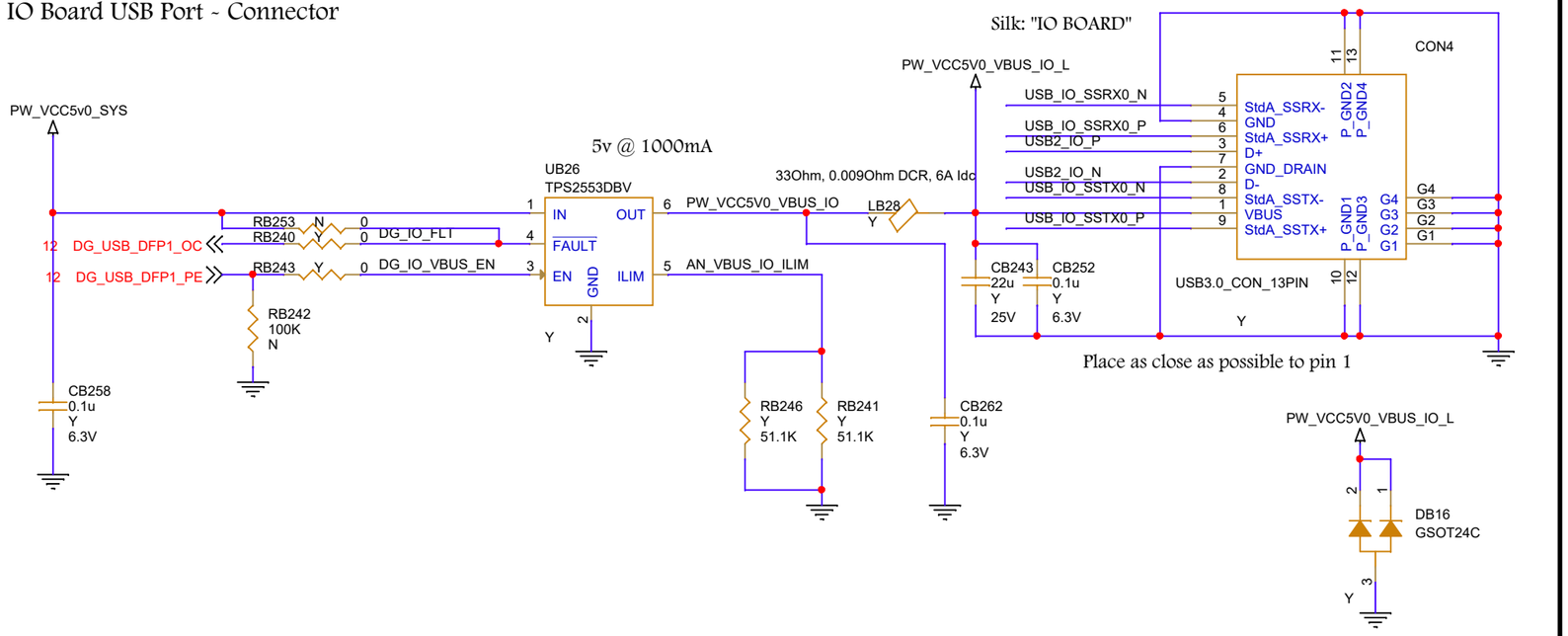
Title: HDMI Port		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 24 of 32	

USBA DFP for IO Board

IO Board USB Port ~ EMI

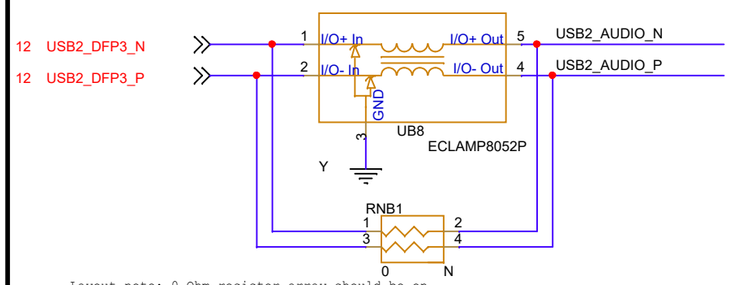


IO Board USB Port ~ Connector

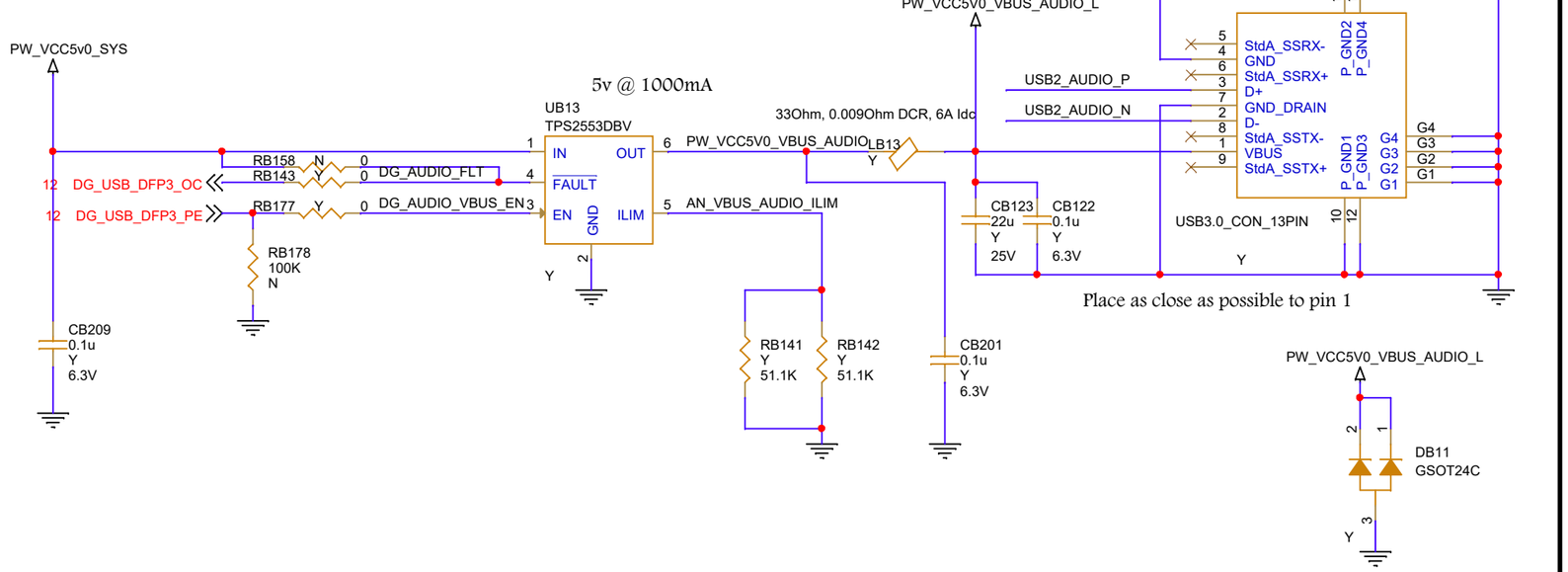


USBA DFP for AUDIO Board

AUDIO Board USB Port ~ EMI



AUDIO Board USB Port ~ Connector



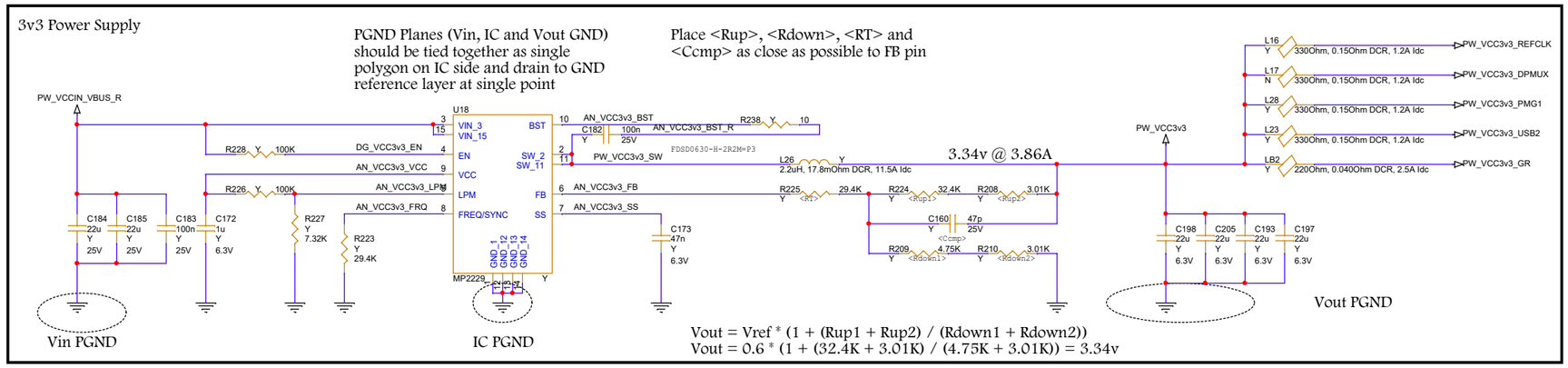
<Core Design>

Intel Confidential

THUNDERBOLT

Title: Interconnect USB Ports		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Sunday, October 17, 2021	Sheet 25 of 32	

Power Supply - LV (3.3v)



<Core Design>

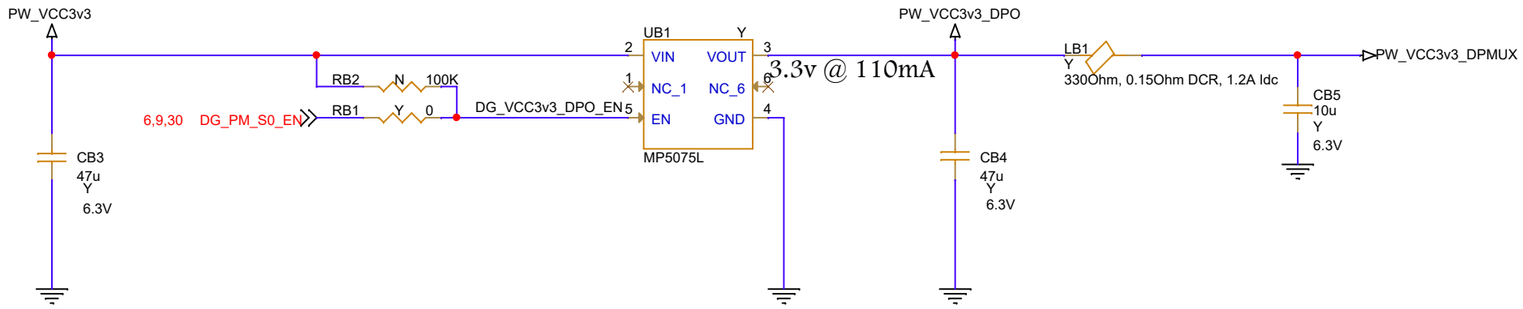
Intel Confidential

THUNDERBOLT

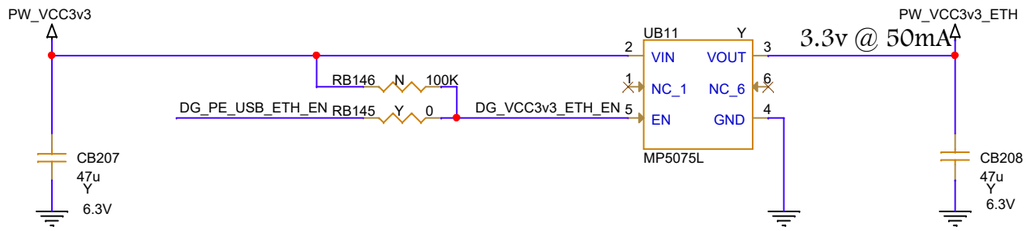
Title: Power Supply - LV (3.3v & 1.2v)			
Size: A2	Document Number: GALACTICO Main Board		Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 26 of 32		

Power Supply - LV (3.3v & 1.2v)

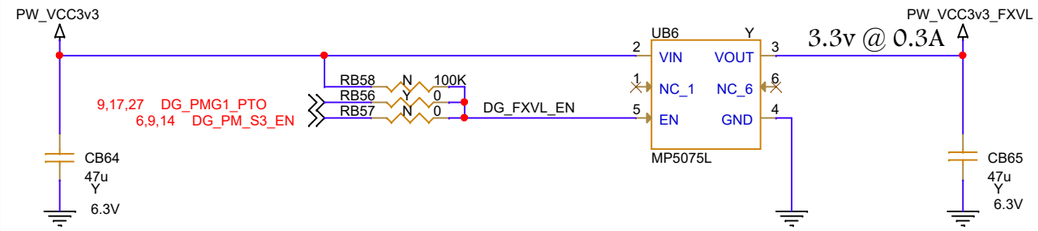
VCC3v3 S0 Power Switch



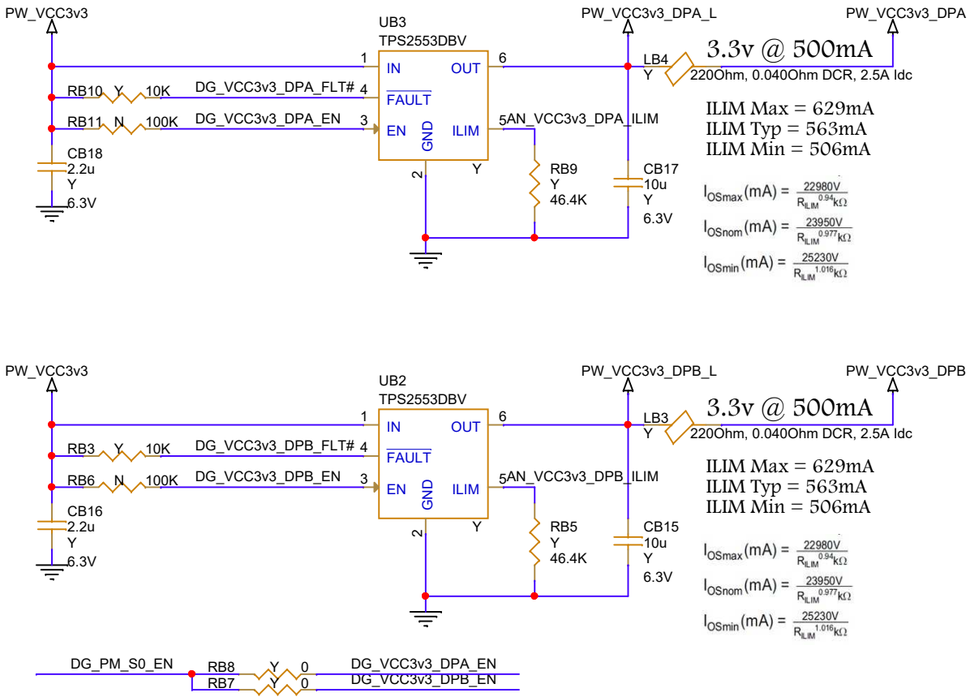
VCC3v3 USB ETH Power Switch



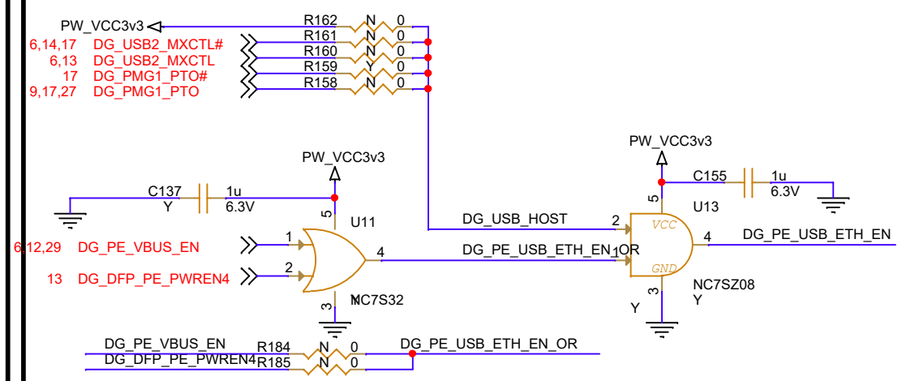
3v3_FXVL Power Rail



3v3 Current Limiter for DP Ports



RTL8153 VBUS Enable

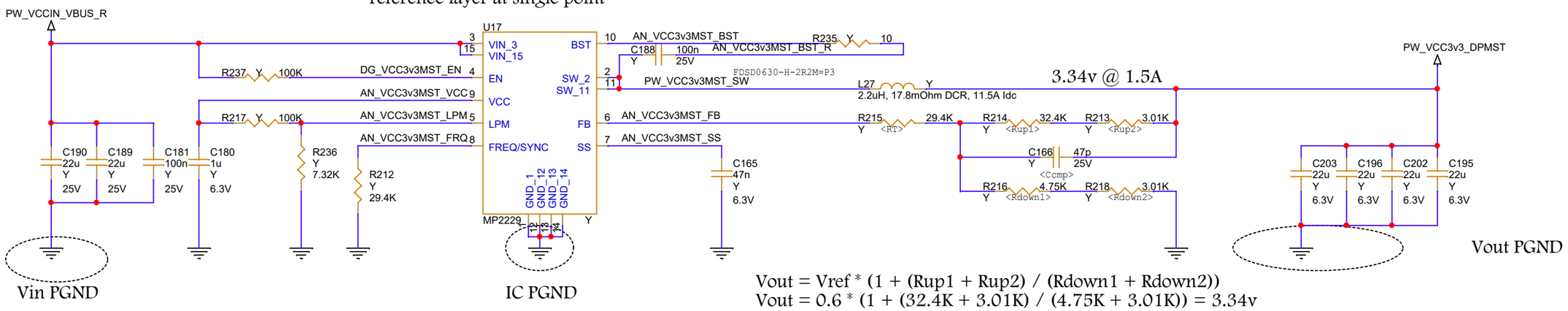


Power Supply - LV (3.3v)

3v3 Power Supply

PGND Planes (Vin, IC and Vout GND) should be tied together as single polygon on IC side and drain to GND reference layer at single point

Place <Rup>, <Rdown>, <RT> and <Ccmp> as close as possible to FB pin

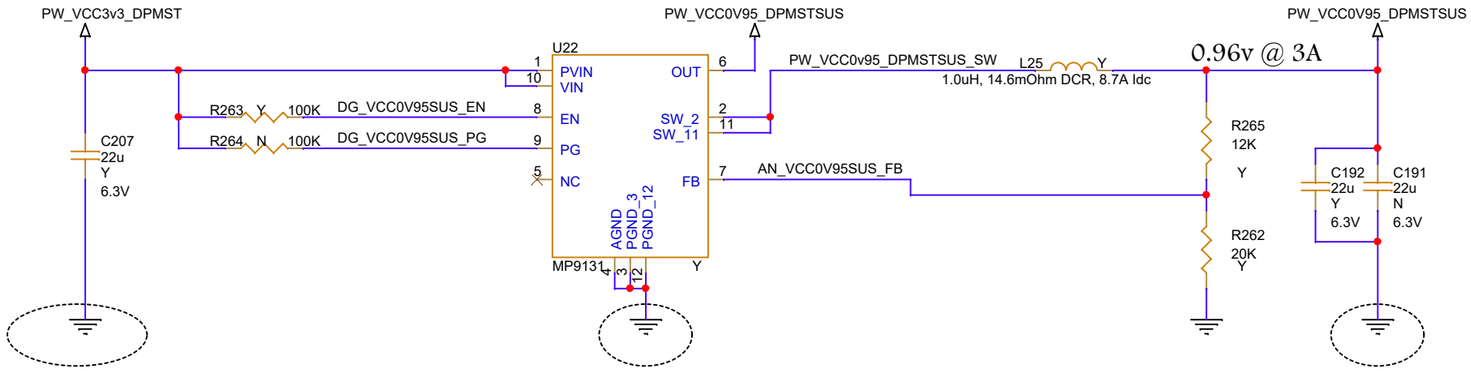


Vout = Vref * (1 + (Rup1 + Rup2) / (Rdown1 + Rdown2))
Vout = 0.6 * (1 + (32.4K + 3.01K) / (4.75K + 3.01K)) = 3.34v

1.05v Power Rail to RTD2188

Vout = Vref * (1 +Rup / Rdown)
Vout = 0.6 * (1 + 12K / 20K) = 0.96v

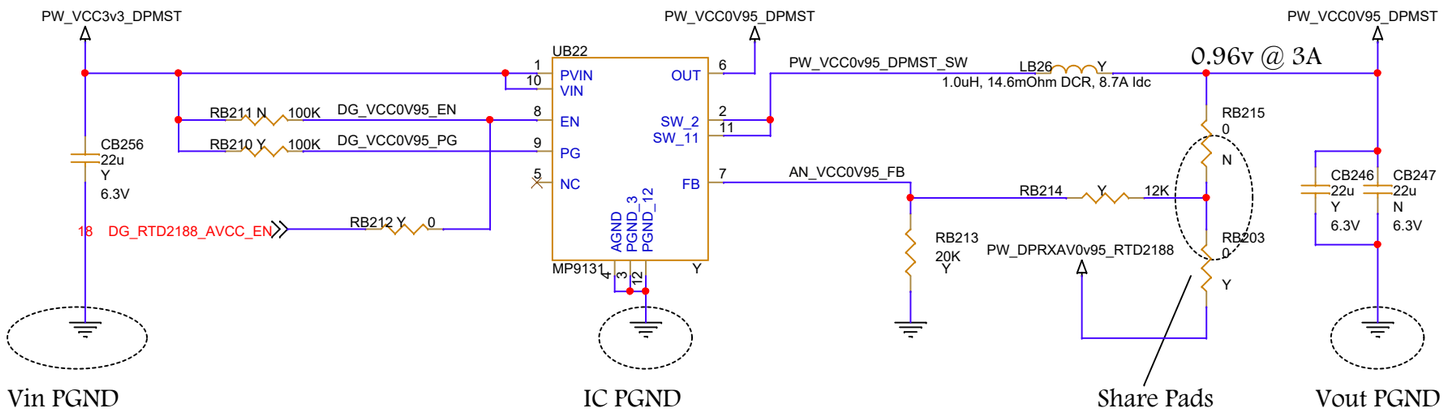
eff. = 86.71%



1.05v Power Rail to RTD2188

Vout = Vref * (1 +Rup / Rdown)
Vout = 0.6 * (1 + 12K / 20K) = 0.96v

eff. = 86.71%



<Core Design>

Intel Confidential

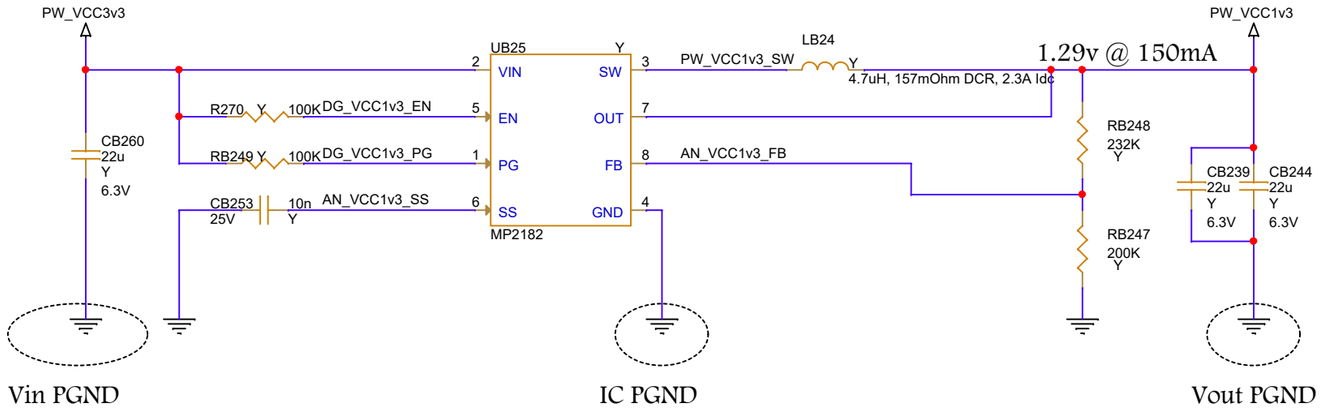
THUNDERBOLT

Title: Power Supply - DP		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 28 of 32	

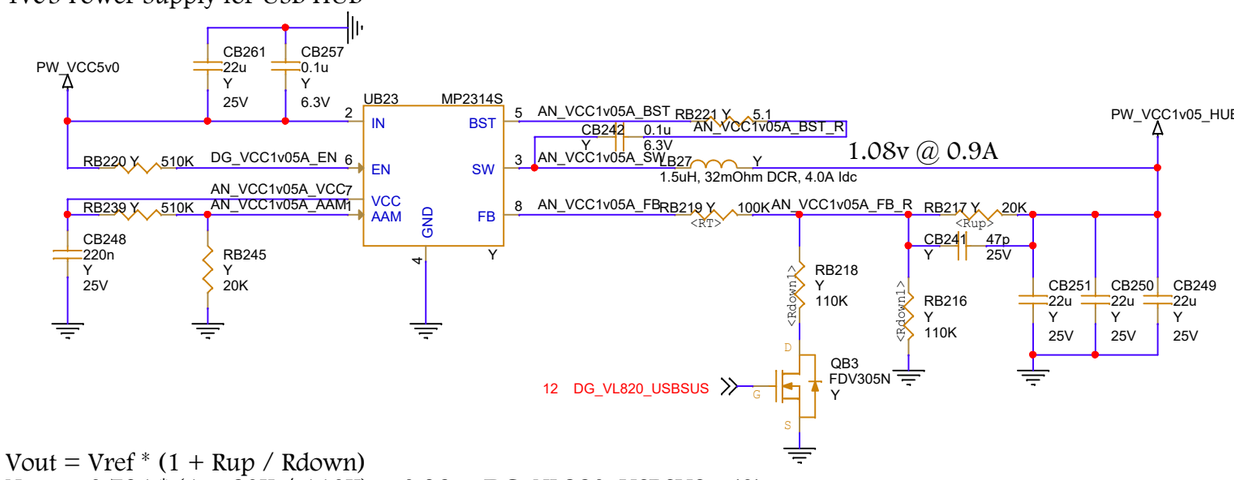
Power Supply - USB HUBs

1.3v Power Rail to FL5801

Vout = Vref * (1 +Rup / Rdown) eff. = 90.6%
Vout = 0.6 * (1 + 232K / 200K) = 1.29v



1v05 Power Supply for USB HUB



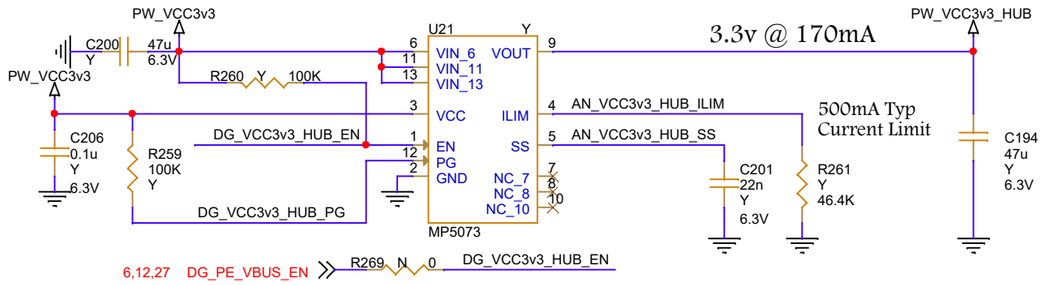
Vout = Vref * (1 + Rup / Rdown)
Vout = 0.791 * (1 + 20K / 110K) = 0.93v ; DG_VL820_USBSUS = '0'
Vout = 0.791 * (1 + 20K / (110K || 110K)) = 1.08v ; DG_VL820_USBSUS = '1'

1v05 Power Supply VIN Rework



Connect CB261.2 to CB238.1

VCC3v3 USB HUB Power Switch



<Core Design>

Intel Confidential

THUNDERBOLT

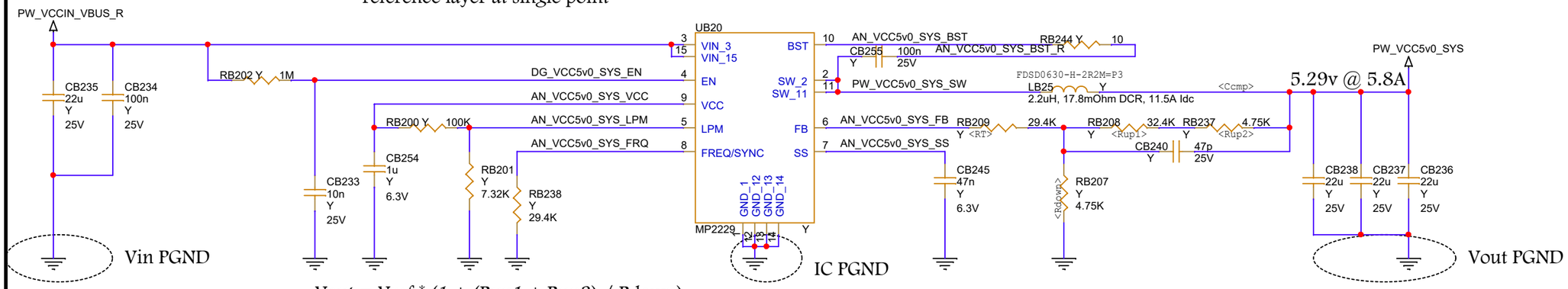
Title: Power Supply - USB		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Sunday, October 17, 2021	Sheet 29 of 32	

Power Supply - LV (5v & 1.2v)

5v0_SYS2 Power Supply

PGND Planes (Vin, IC and Vout GND) should be tied together as single polygon on IC side and drain to GND reference layer at single point

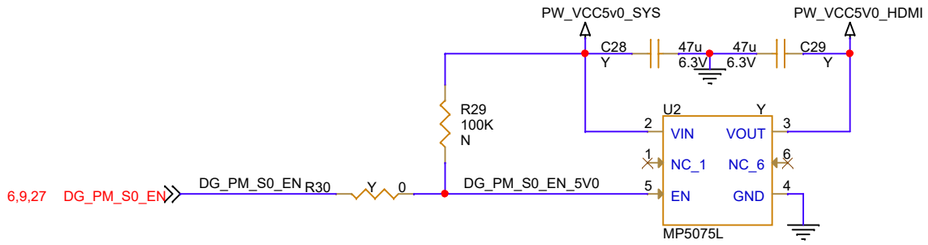
Place <Rup>, <Rdown>, <RT> and <Ccmp> as close as possible to FB pin



Vout = Vref * (1 + (Rup1 + Rup2) / Rdown)
Vout = 0.6 * (1 + (32.4K + 4.75K / 4.75K) = 5.29v

5V0_HDMI Power Rail

5.0v @ 55mA



<Core Design>

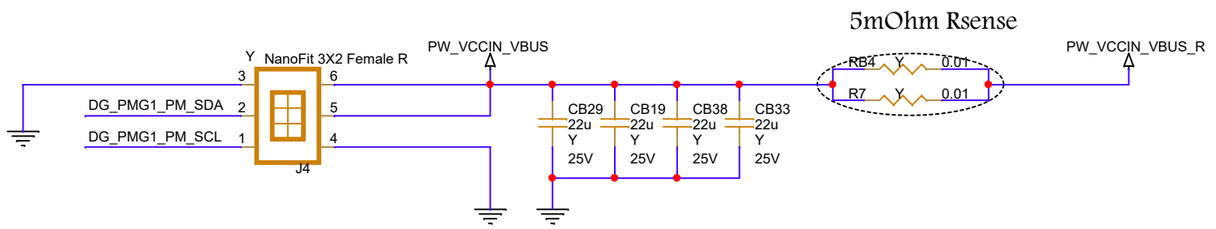
Intel Confidential

THUNDERBOLT

Title: Power Supply - 5v		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Sunday, October 17, 2021	Sheet 30 of 32	

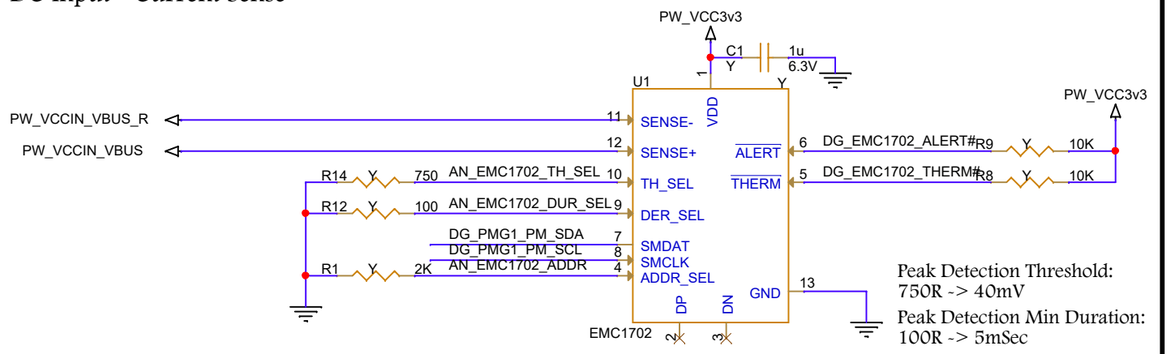
Power Supply - HV (DC Input, USB-PD HV)

20v @ 8.5A DC Input



Silk: "DC IN"
Current rated 7.5A per pin

DC Input - Current Sense

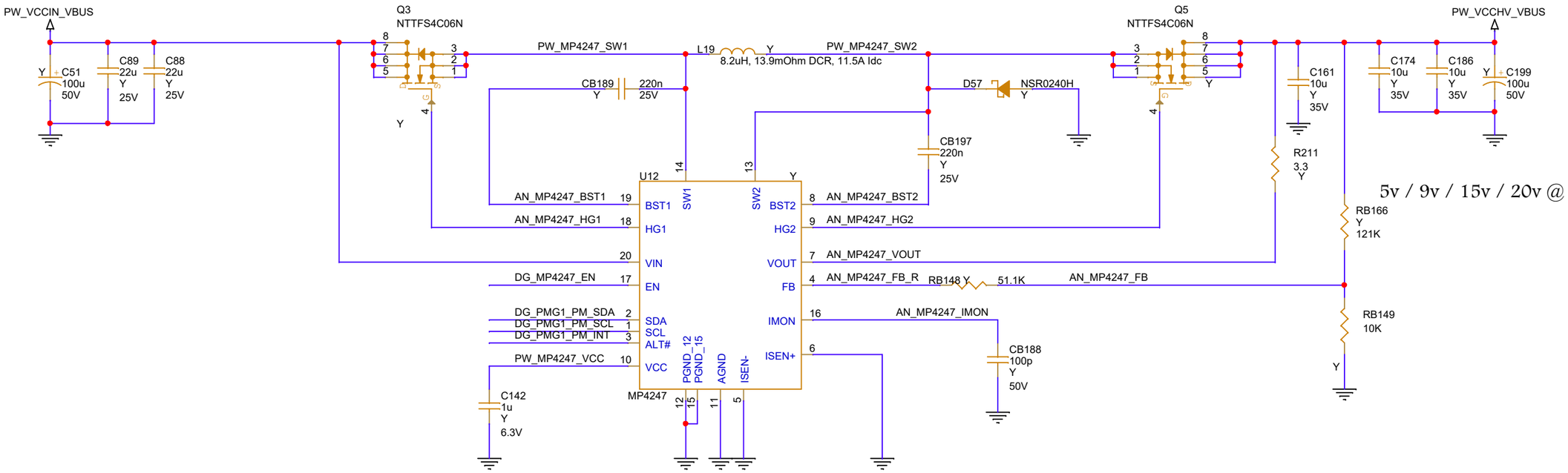


Peak Detection Threshold:
750R -> 40mV
Peak Detection Min Duration:
100R -> 5mSec

I[src] = FSC * V[sense]/2047
FSC = FSR/R[sense] = 80mV/5mOhms = 16A

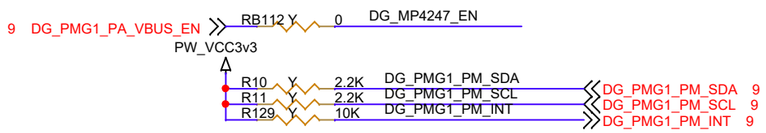
7 bits Address:
Main Board: 0x29 [R= 2k]
IO Board: 0x2A [R= 2.7k]
Audio Board: 0x2B [R= 3.6k]

VCCHV Buck/Boost Converter



5v / 9v / 15v / 20v @ 3.0A; 28V @ 5A

VCCHV Buck/Boost Converter Ctrl



MP4247 I2C Address 0x67

<Core Design>

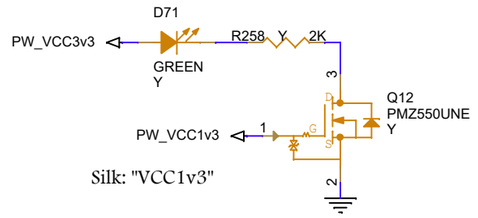
Intel Confidential

THUNDERBOLT

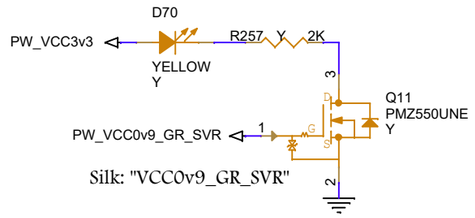
Title: Power Supply - HV (DC IN and VCCHV)		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 31 of 32	

Debug LEDs

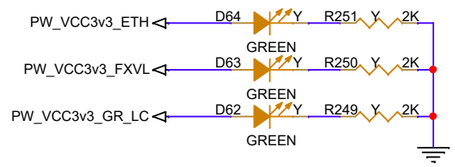
1v3 Power Indicator (Debug Only)



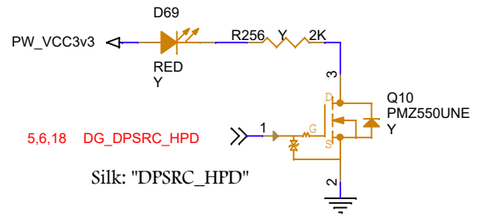
0v9 GR SVR Power Indicator (Debug Only)



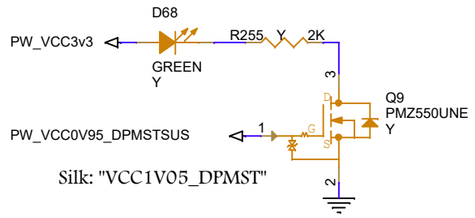
3v3 Power Indicators (Debug Only)



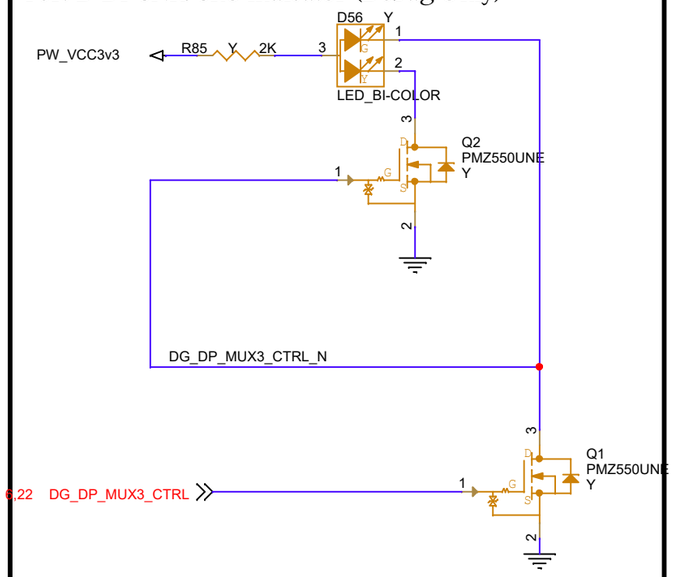
DPSRC_HPD Indicator (Debug Only)



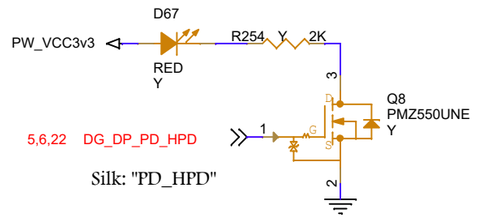
1v05 Power Indicator (Debug Only)



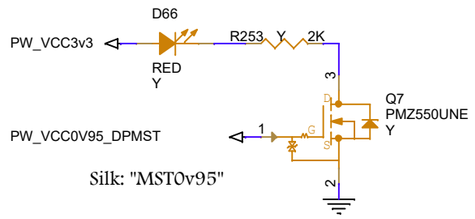
Port D DP SNK/SRC Indicator (Debug Only)



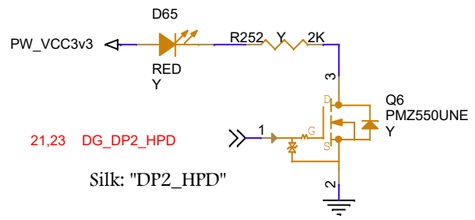
PD_HPD Indicator (Debug Only)



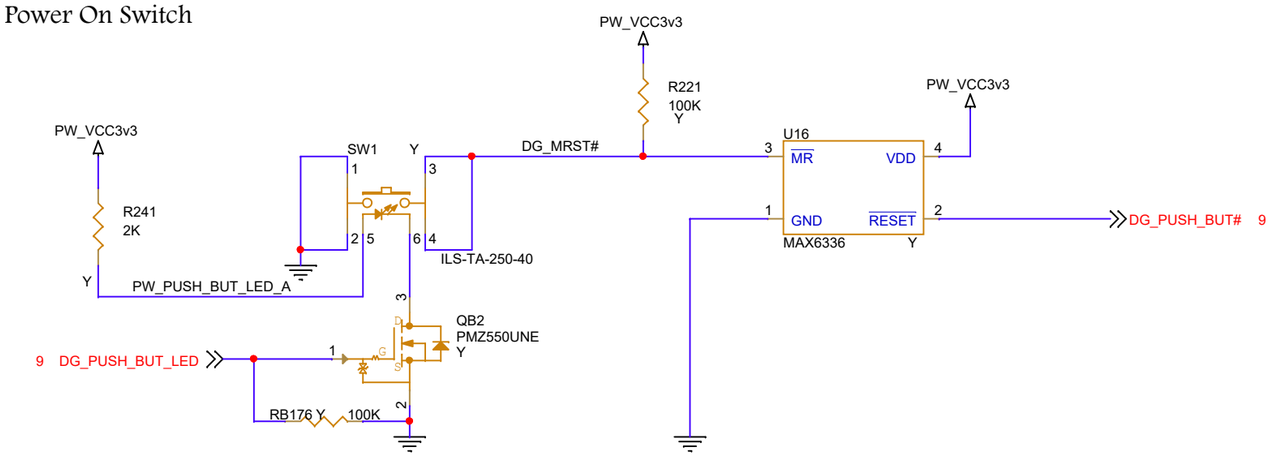
DP1_HPD Indicator (Debug Only)



DP2_HPD Indicator (Debug Only)



Power On Switch



<Core Design>

Intel Confidential

THUNDERBOLT

Title: Debug LEDs		
Size: A3	Document Number: GALACTICO Main Board	Rev: 1.1
Date: Saturday, October 16, 2021	Sheet 32 of 32	