Revision History

Version	Date	Updated by	Approved by	Modifications
10	2015-07-02	VL		First draft

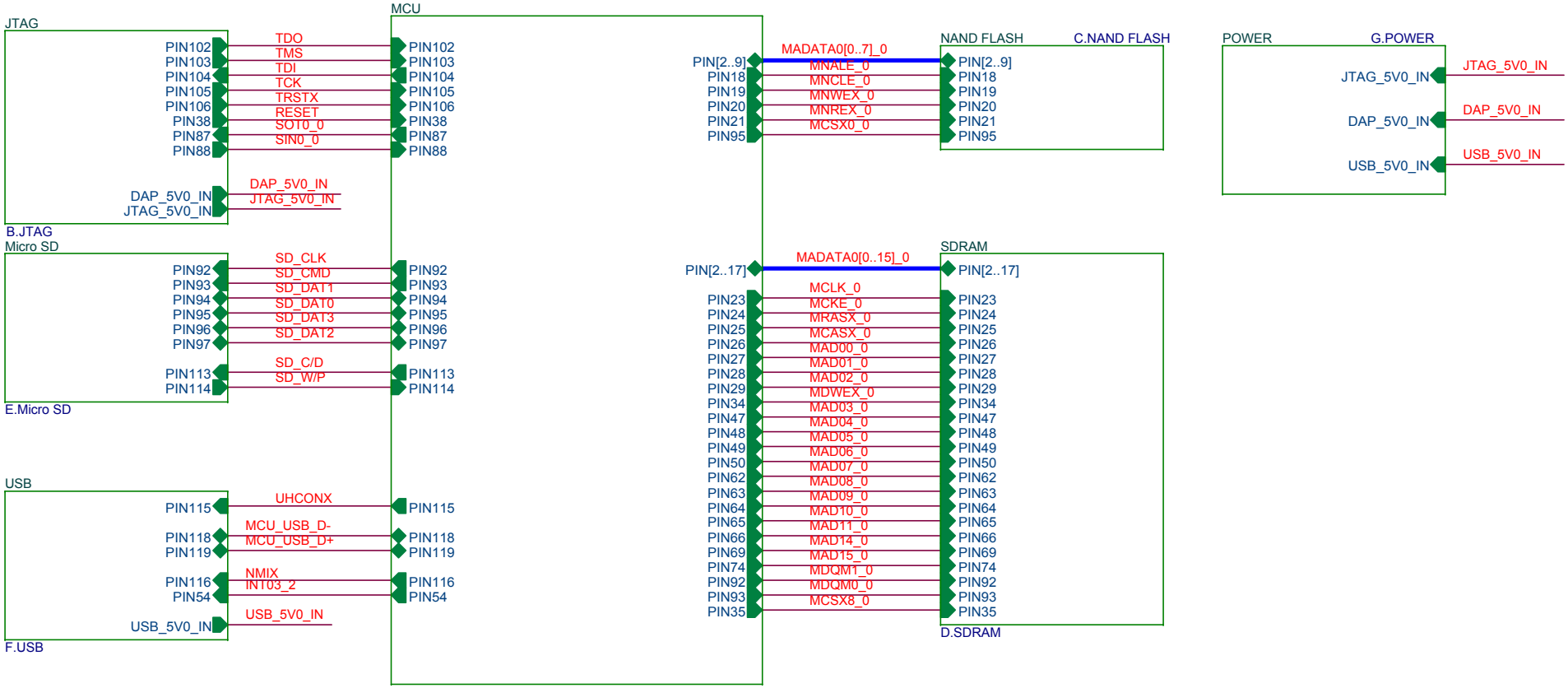
Cypress

Author: VL

Title: FM4-120L-S6E2HG

Size	Document Number	Rev
A4	Cover	V10

Date: Friday, August 21, 2015 Sheet 1 of 9

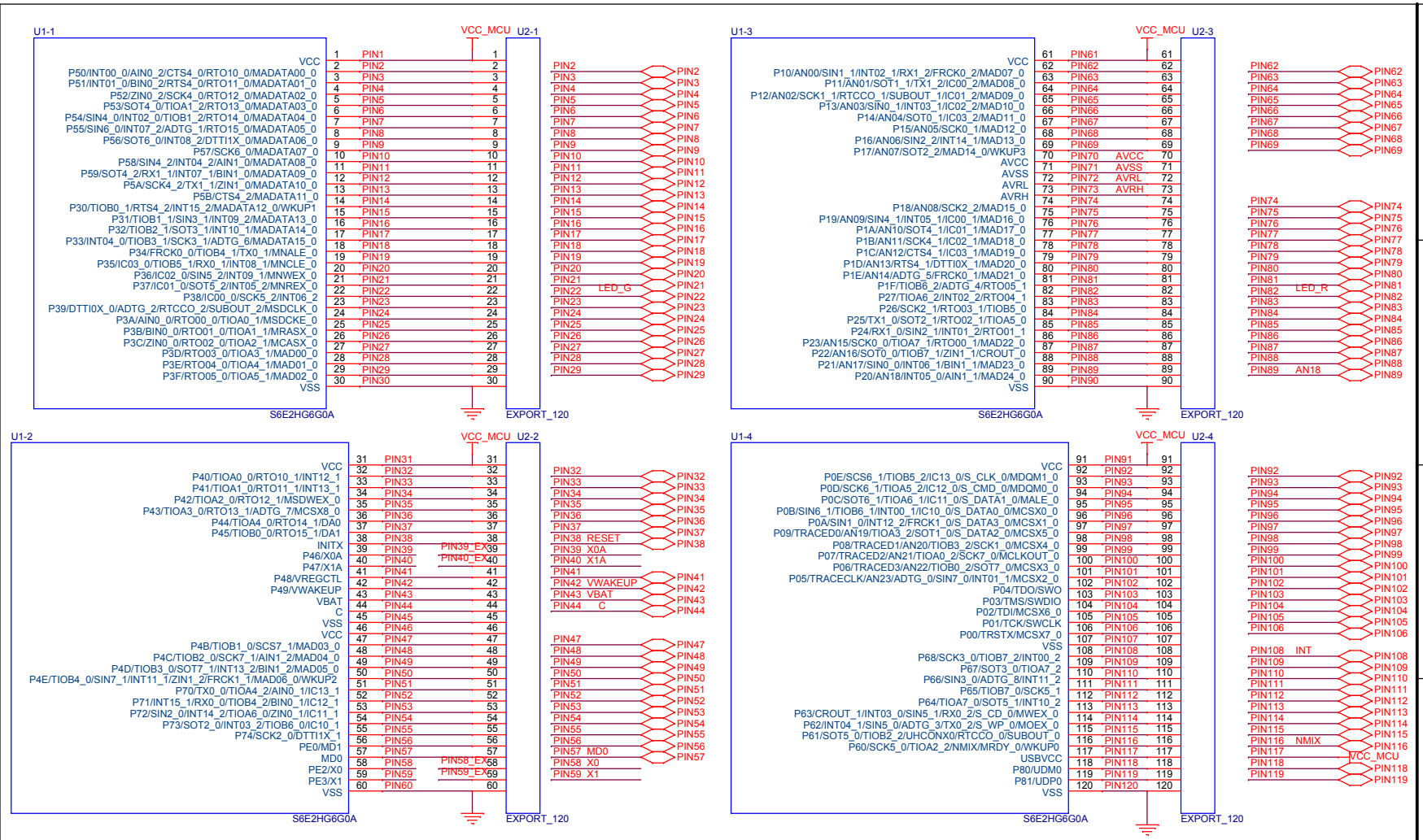


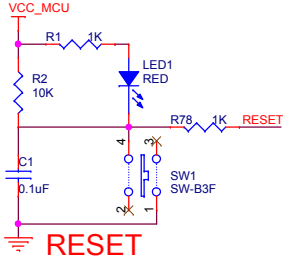
Cypress
Author: VL

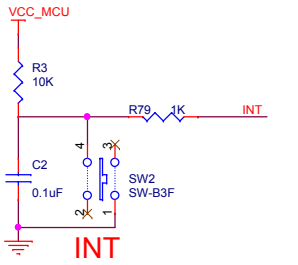
Title
FM4-120L-S6E2HG

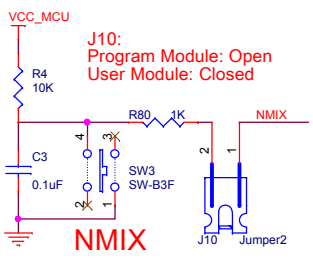
Size	Document Number	Rev
A4	Hierarchical_Page	V10

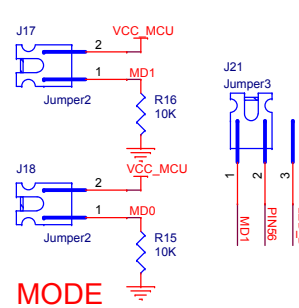
Date: Friday, August 21, 2015 Sheet 2 of 9

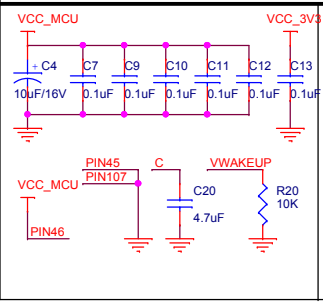


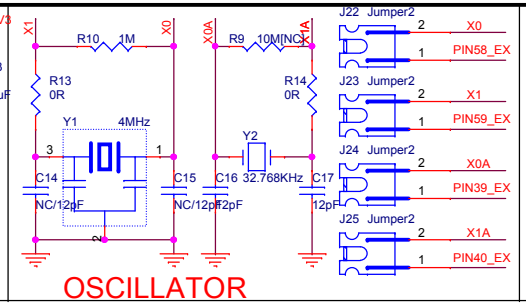


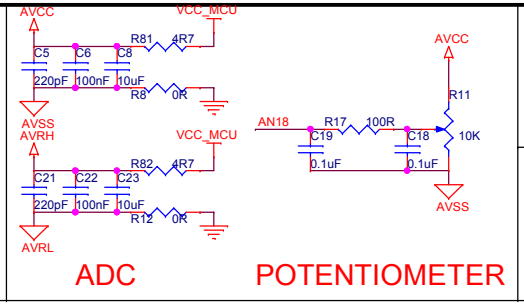


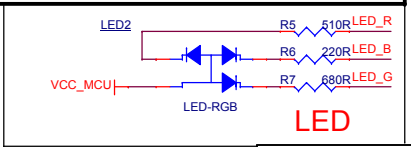


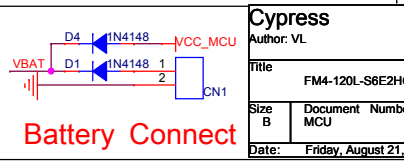












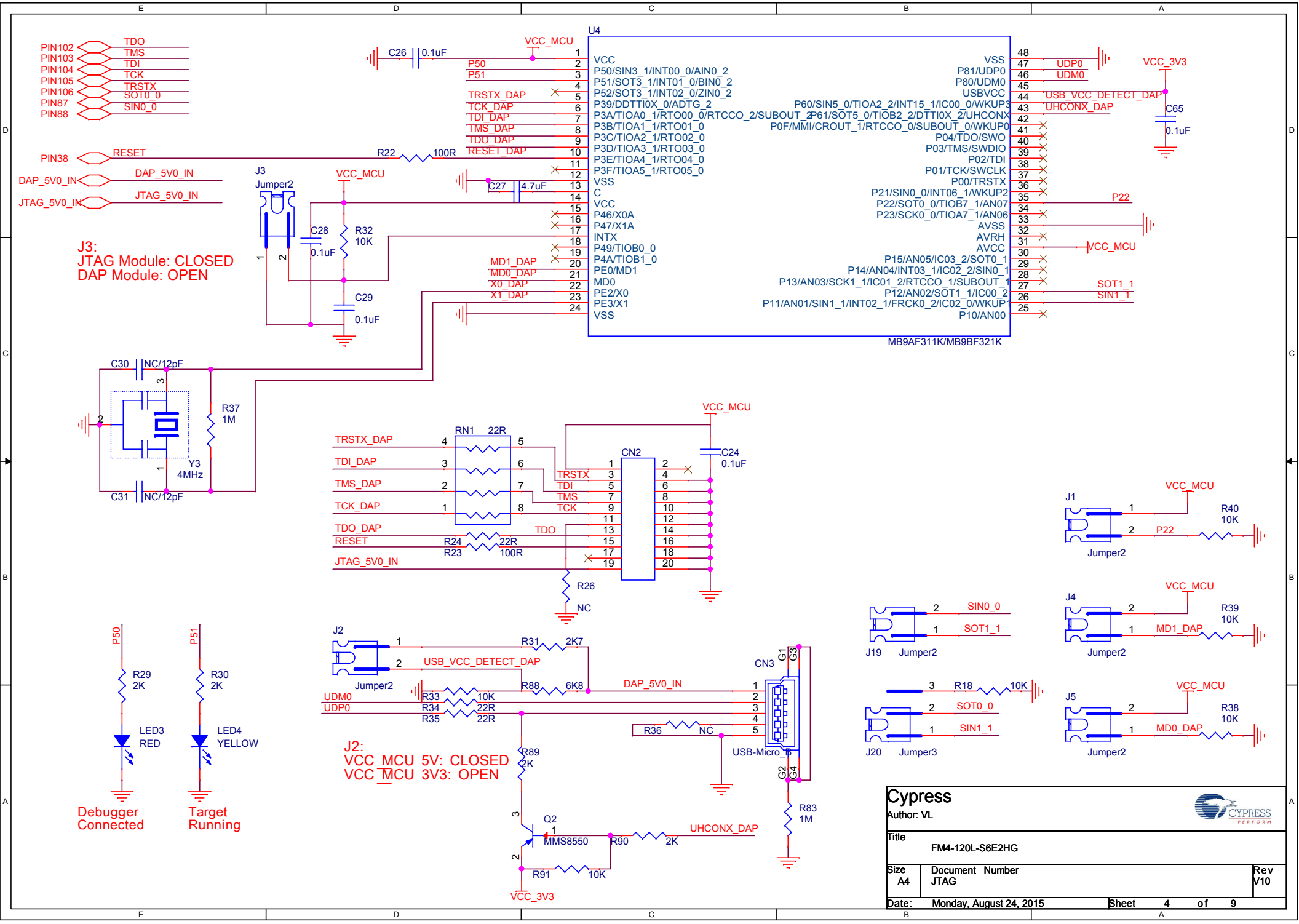
Cypress

Author: VL

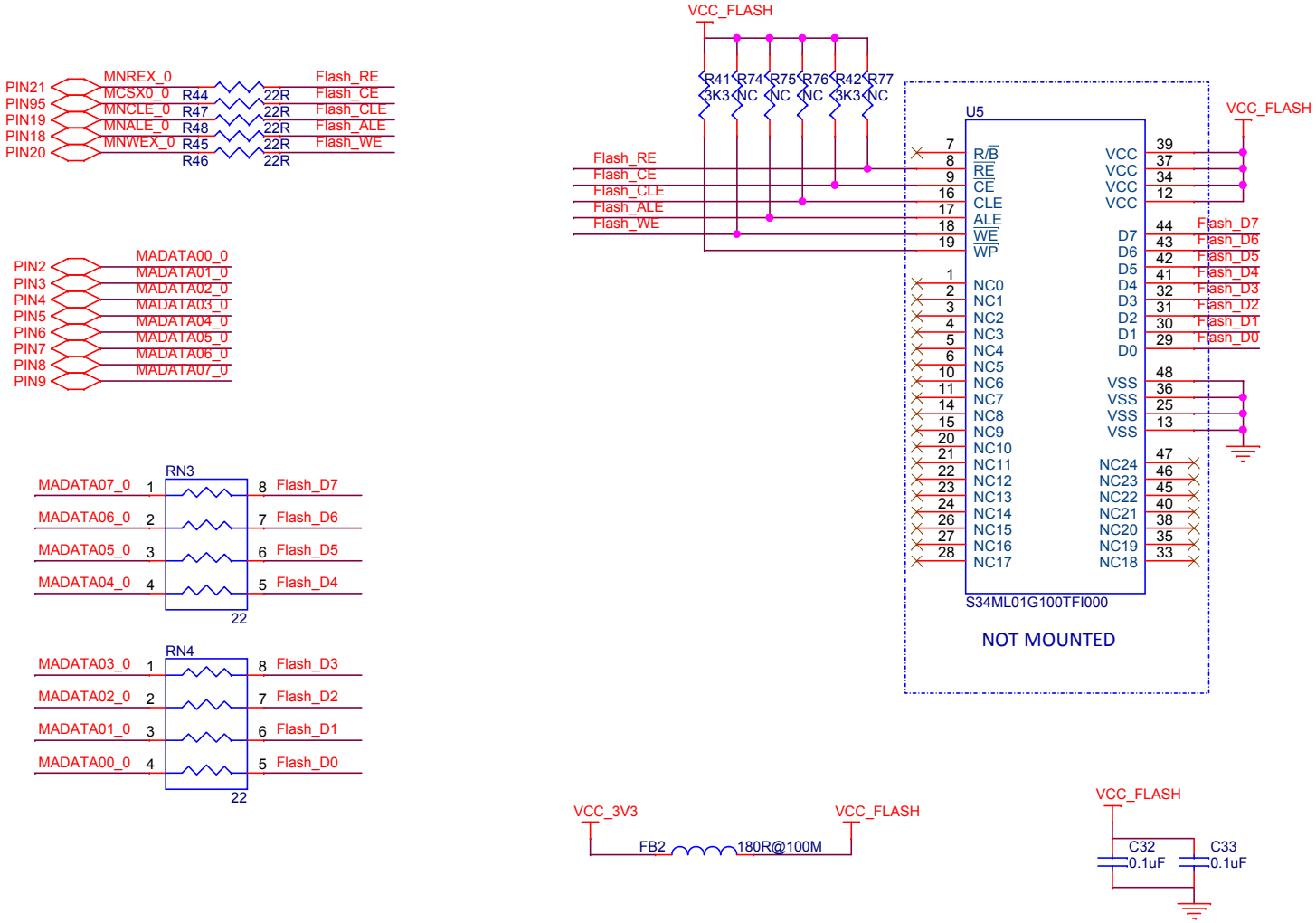
Title: FM4-120L-S6E2HG

Size	Document Number	Rev
B	MCU	V10

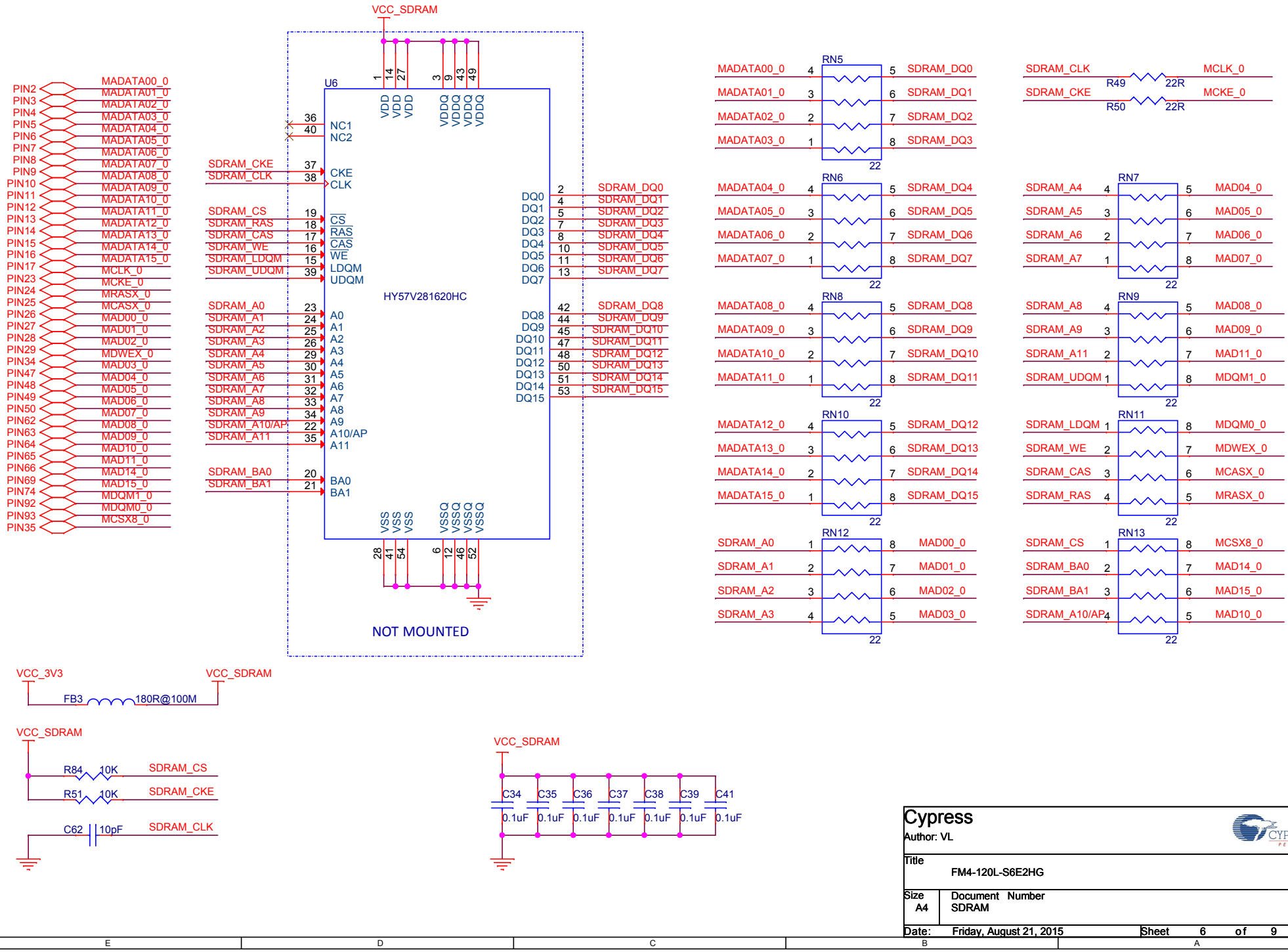
Date: Friday, August 21, 2015 Sheet 3 of 9

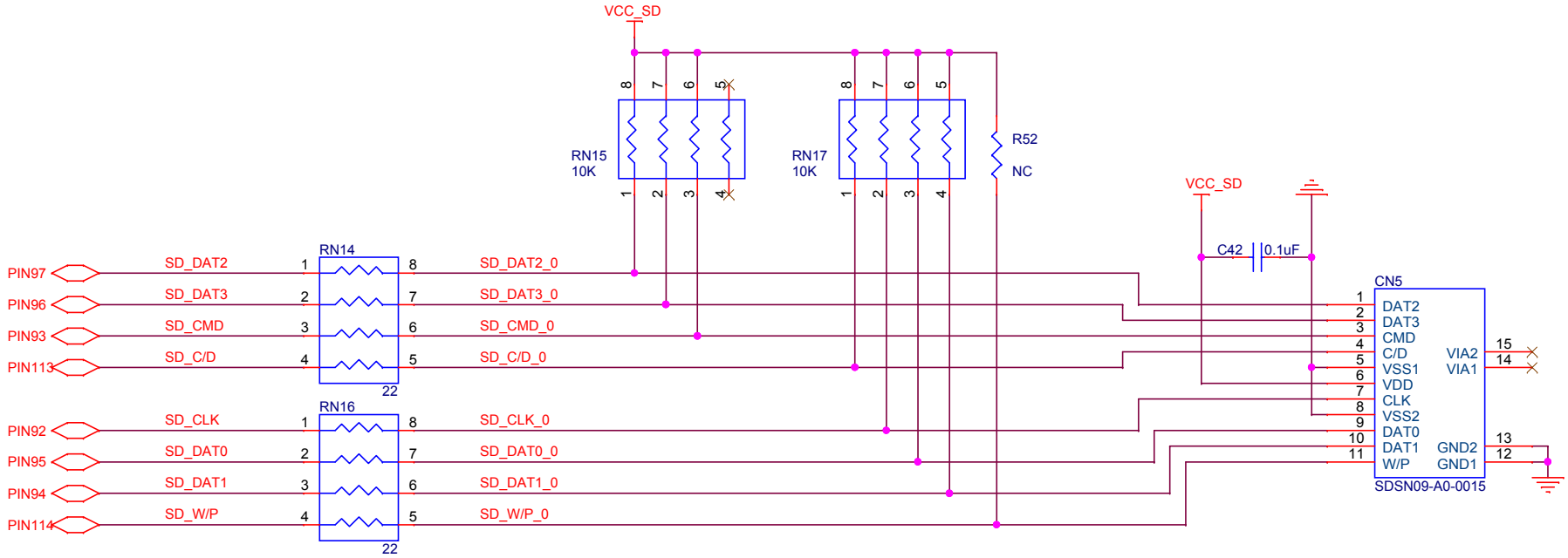


Cypress		
Author: VL		
Title: FM4-120L-S6E2HG		
Size: A4	Document Number: JTAG	Rev: V10
Date: Monday, August 24, 2015	Sheet 4 of 9	

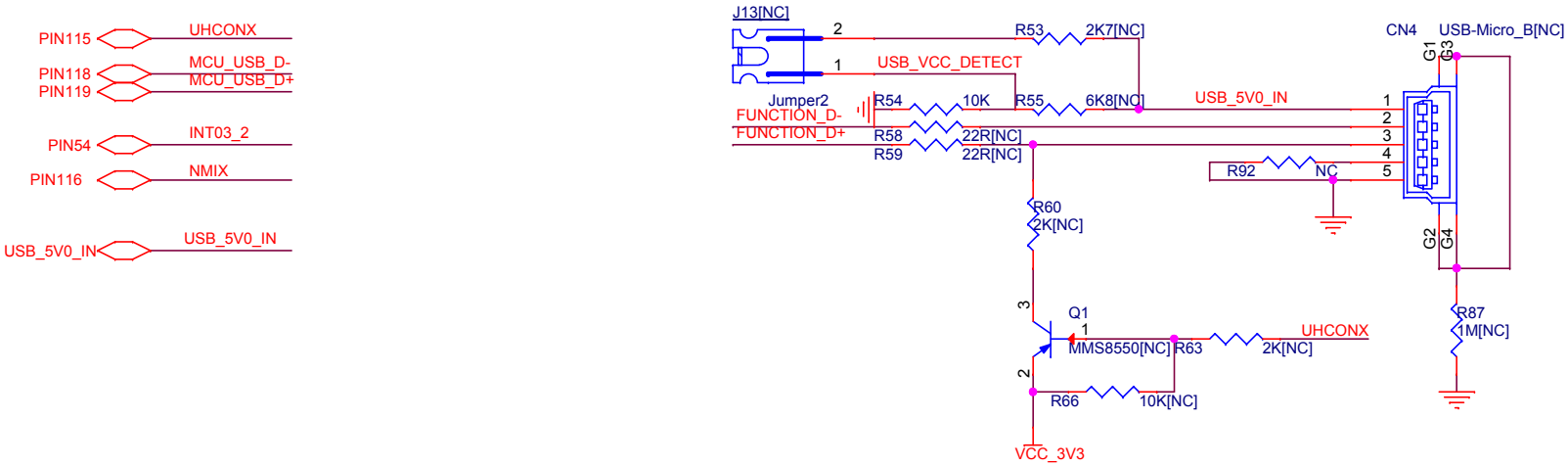


Cypress		
Author: vl		
Title: FM4-120L-S6E2HG		
Size: A4	Document Number: NAND FLASH	Rev: V10
Date: Friday, August 21, 2015	Sheet 5 of 9	

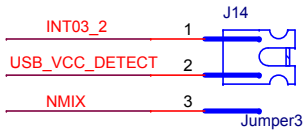

VCC_SDRAM
U6
HY57V281620HC
NOT MOUNTED
RN5
RN6
RN7
RN8
RN9
RN10
RN11
RN12
RN13
R49 22R
R50 22R
FB3 180R@100M
VCC_3V3
R84 10K
R51 10K
C62 10pF
C34 C35 C36 C37 C38 C39 C41
0.1uF
Cypress
Author: VL
Title
FM4-120L-S6E2HG
Size A4
Document Number SDRAM
Rev V10
Date: Friday, August 21, 2015
Sheet 6 of 9

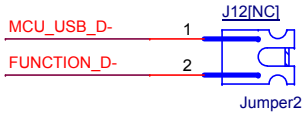


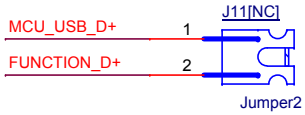
Cypress		
Author: VL		
Title	FM4-120L-S6E2HG	
Size A4	Document Number Micro SD	Rev V10
Date: Friday, August 21, 2015	Sheet 7 of 9	



J13:
VCC_MCU 5V: CLOSED
VCC_MCU 3V3: OPEN





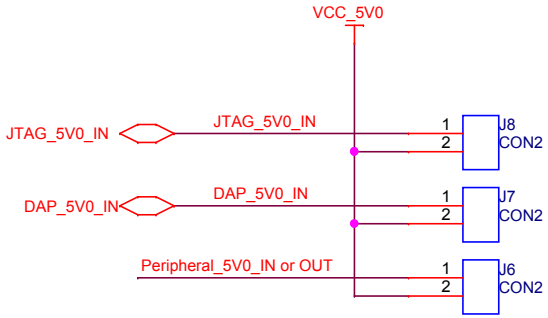


NC : NOT MOUNTED

J14:
Program Module: Closed Pin2 to Pin3
User Module: Closed Pin2 to Pin1

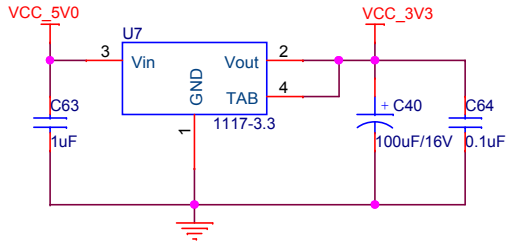
J11, J12:
Function: CLOSED
Host: OPEN

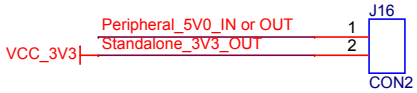
Cypress Author: VL		
Title: FM4-120L-S6E2HG		
Size: A4	Document Number: USB	Rev: V10
Date: Friday, August 21, 2015	Sheet 8 of 9	



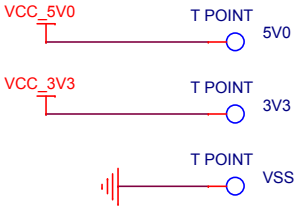
5V Power Select:

JTAG Module: Closed J8
DAP Module: Closed J7
Peripheral 5V0 IN or OUT: Closed J6

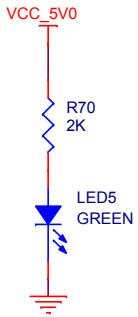


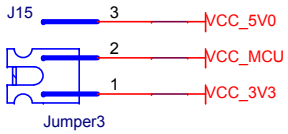


J16: Conect to Peripheral Board
For 5V Input or 5VOutput or 3V3 Output



TEST POINT





J15:
VCC_MCU 3V3: Closed Pin2 to Pin1
VCC_MCU 5V0: Closed Pin2 to Pin3

Cypress Author: VL		
Title: FM4-120L-S6E2HG		
Size: A4	Document Number: POWER	Rev: V10
Date: Friday, August 21, 2015	Sheet 9 of 9	