

CYW9RPIM2BASE1

M.2 WIFI BASEBOARD

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Drawing Numbers

PCBA	121-90768-01
PCB	600-90768-01
FAB DRW	610-90768-01
ASSY DRW	620-90768-01
SCH DRW	630-90768-01

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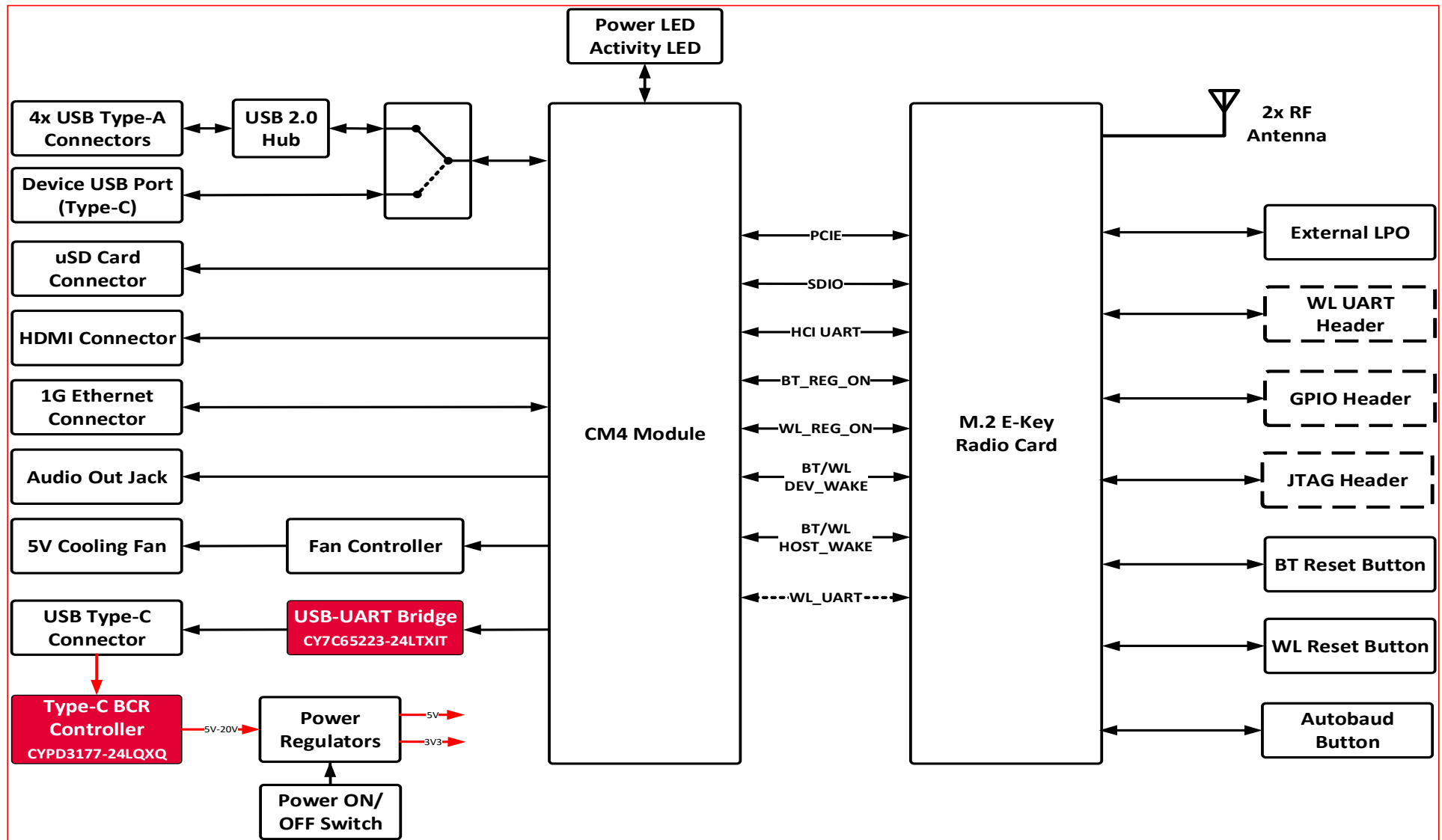
SCH Title : CYW9RPIM2BASE1

Page Title: Title Page

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Block Diagram



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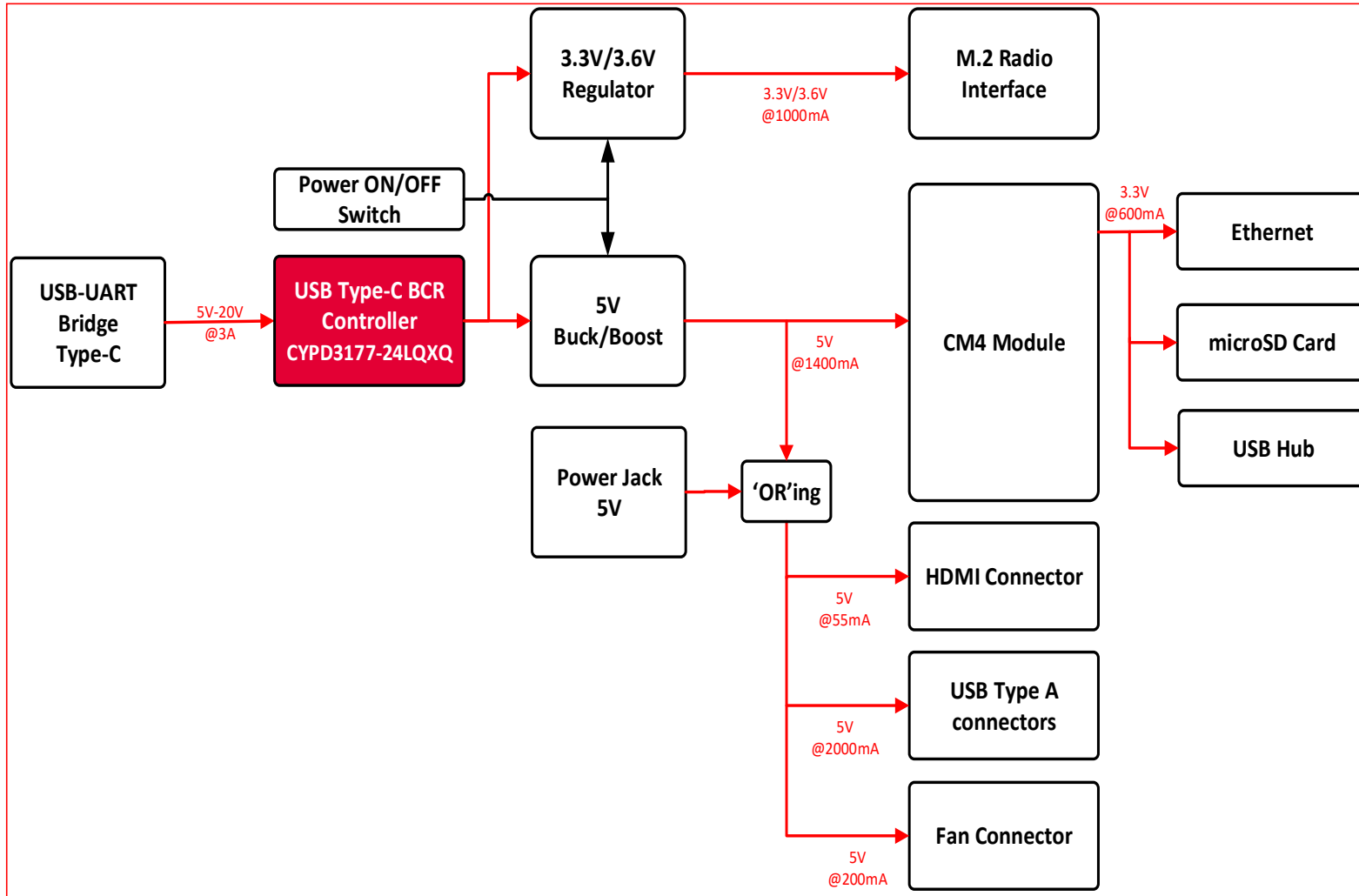
Page Title: Block Diagram

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Power Management Unit Block Diagram



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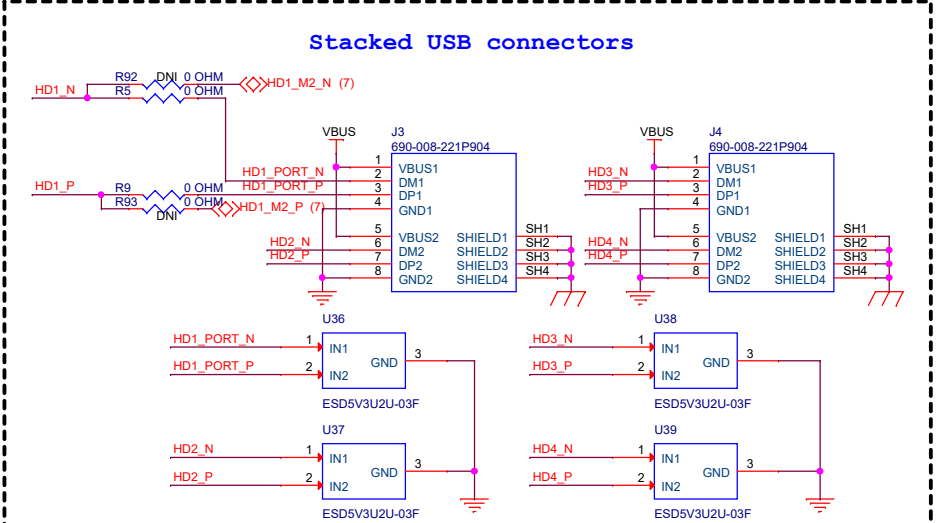
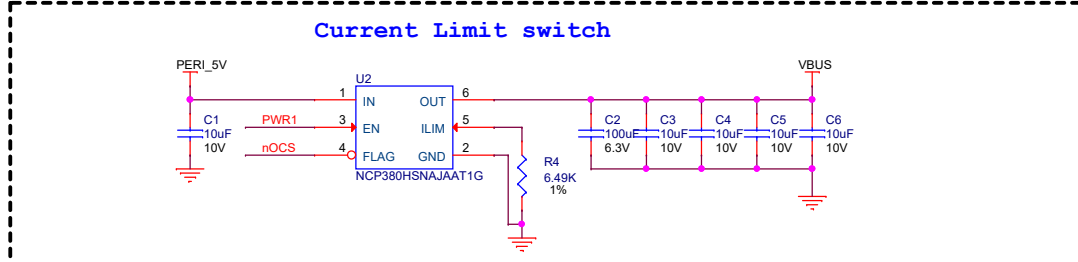
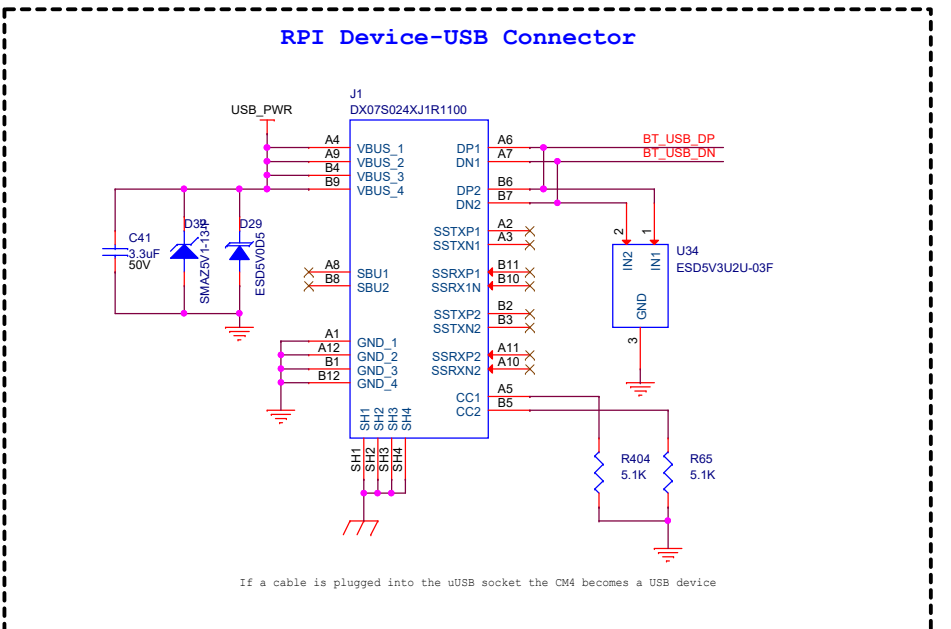
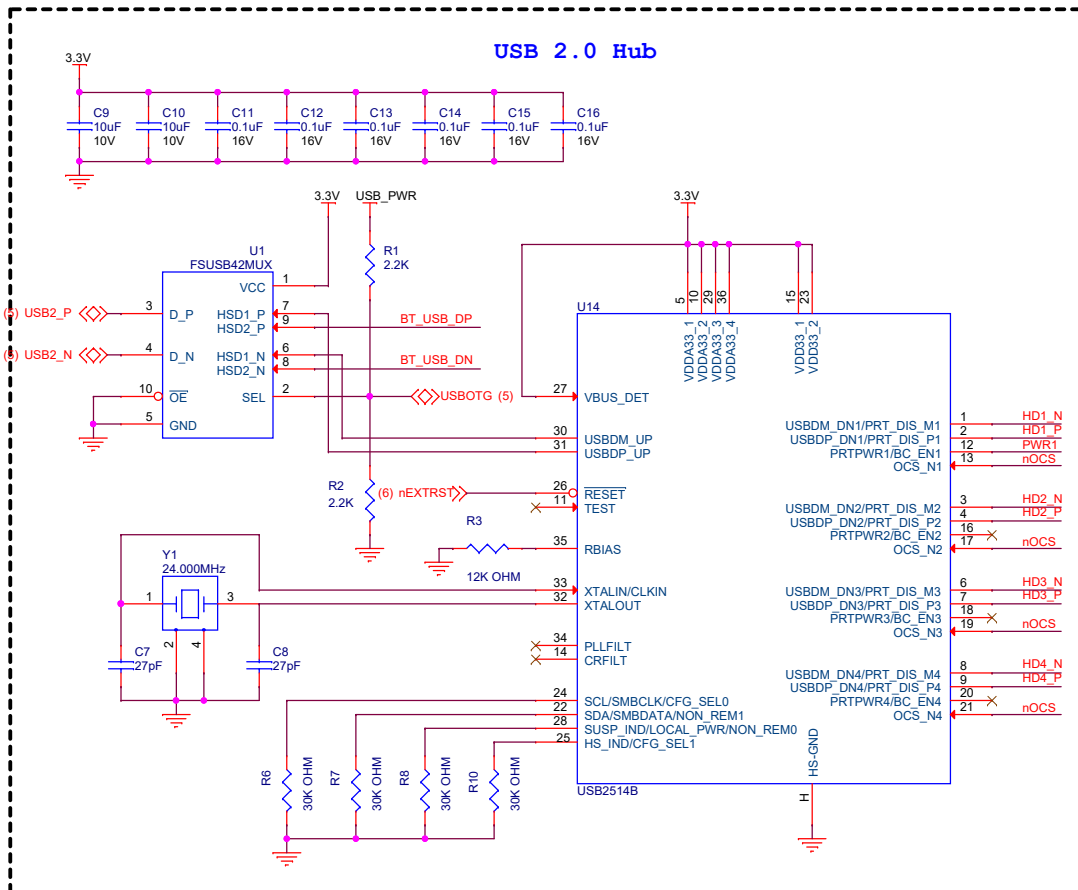


SCH Title : **CYW9RPIM2BASE1**

Page Title: **PMU Block Diagram**

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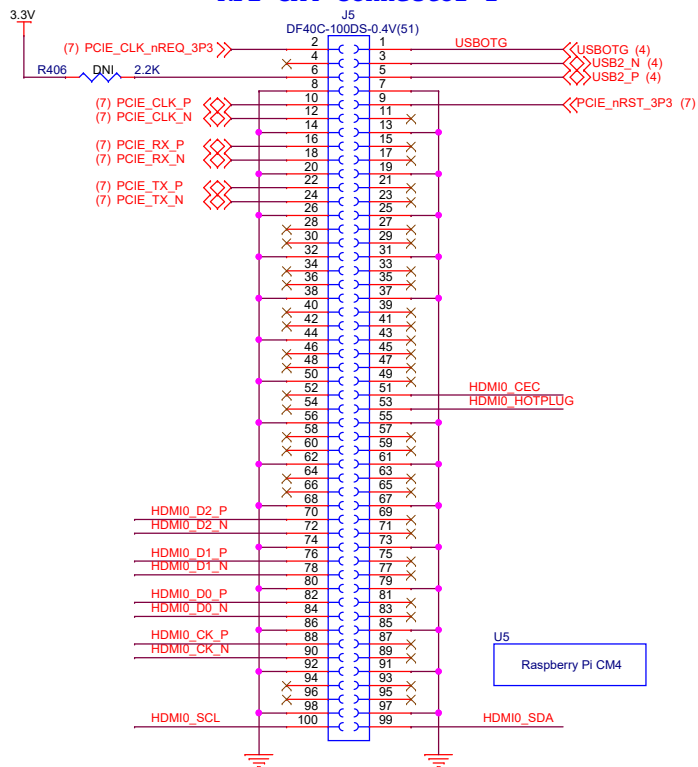


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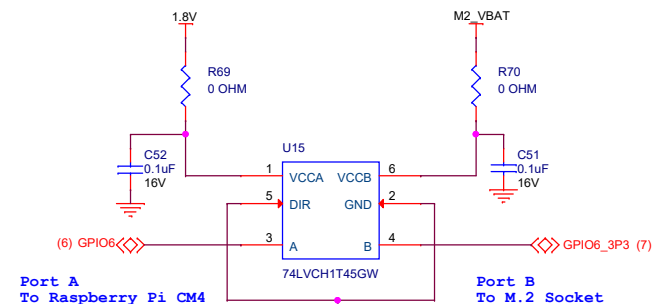


SCH Title : CYW9RPM2BASE1				
Page Title: USB				
Size B	Document Number 630-90768-01	Drawn By RAVEENDRANAT	Approved By RKAD	Rev 3.0
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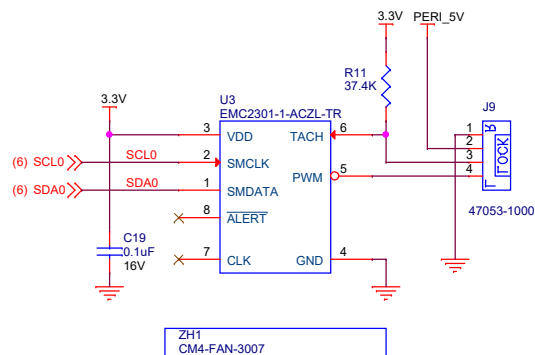
RPi CM4 Connector 1



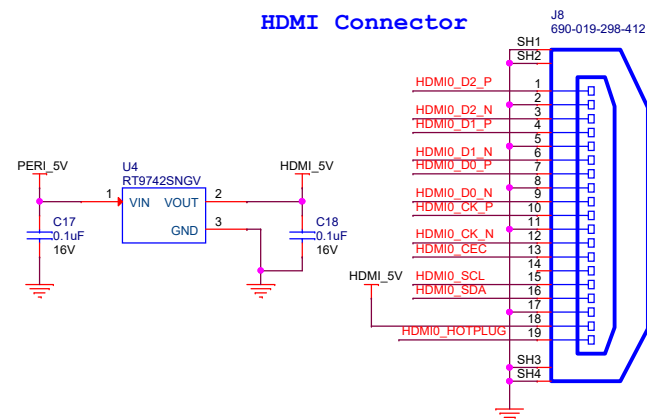
GPIO Level Translator



Fan Controller



HDMI Connector



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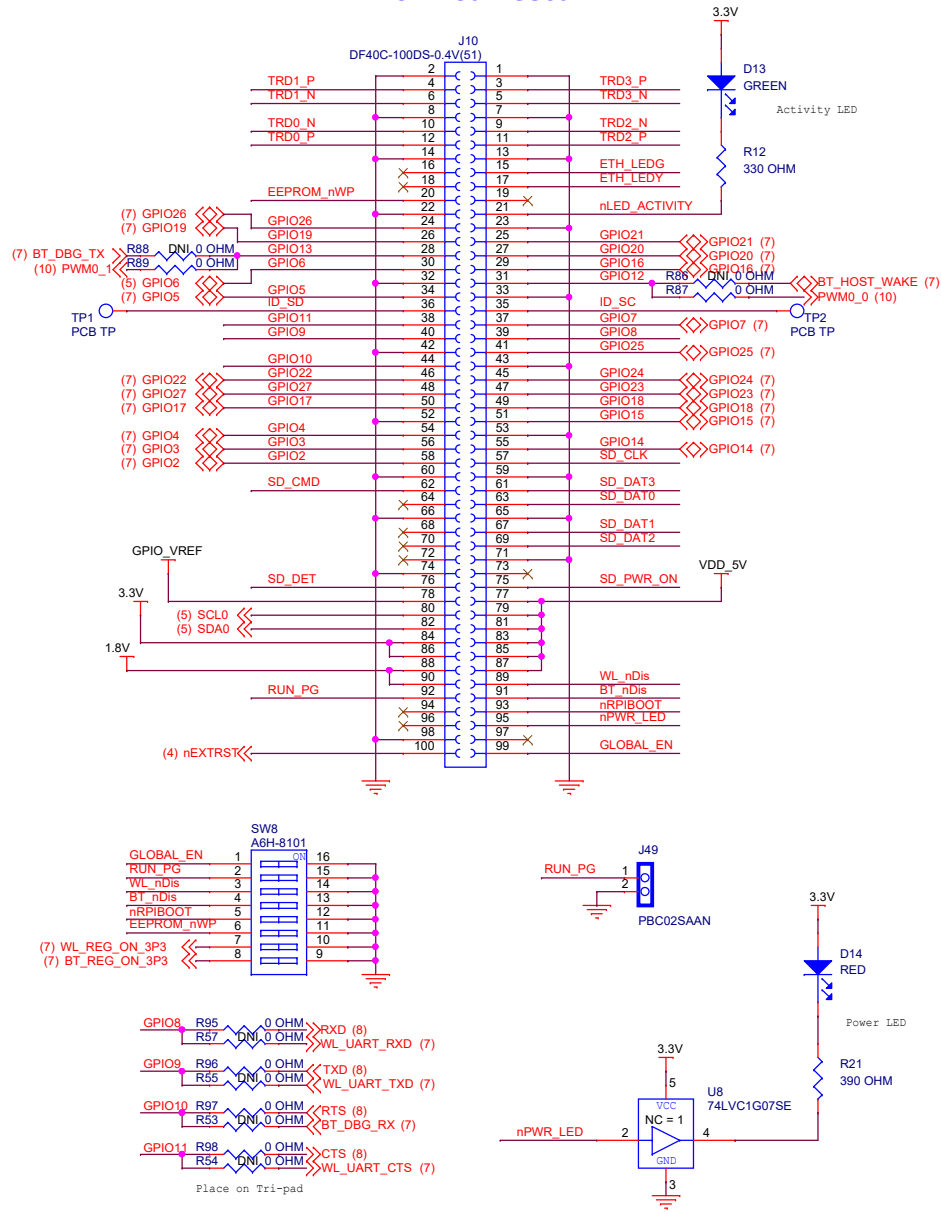


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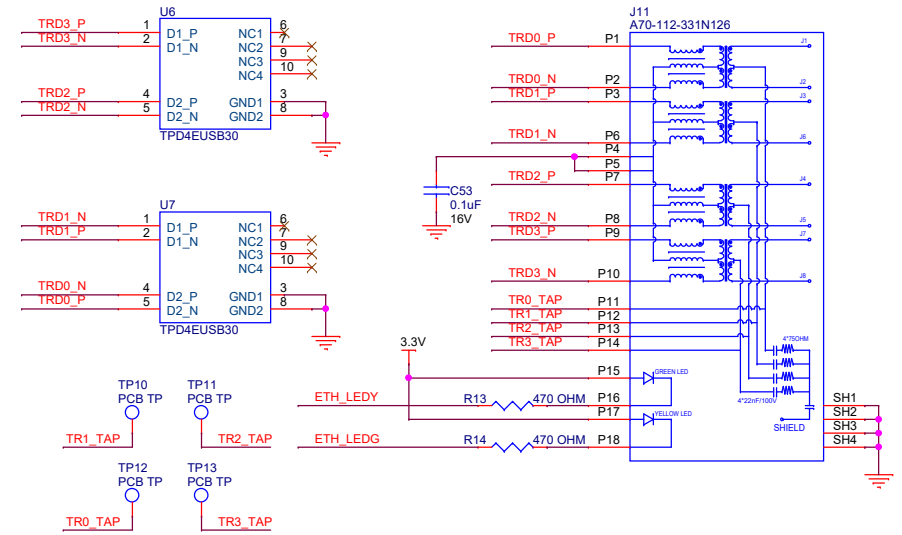
Page Title : CM4 HDMI & Fan Control

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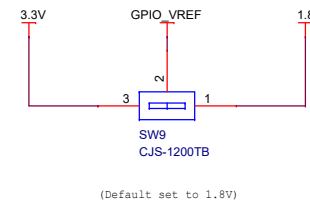
RPi CM4 Connector 2



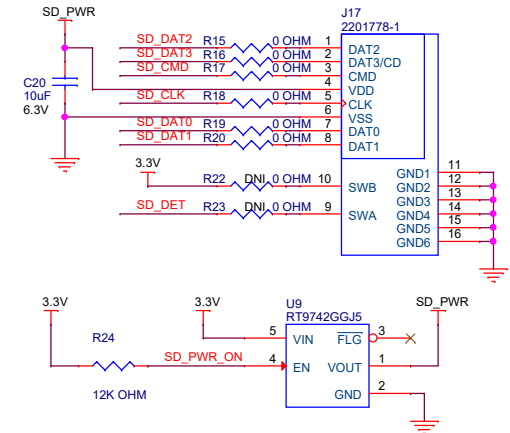
1G Ethernet Interface



CM4 GPIO Voltage Select



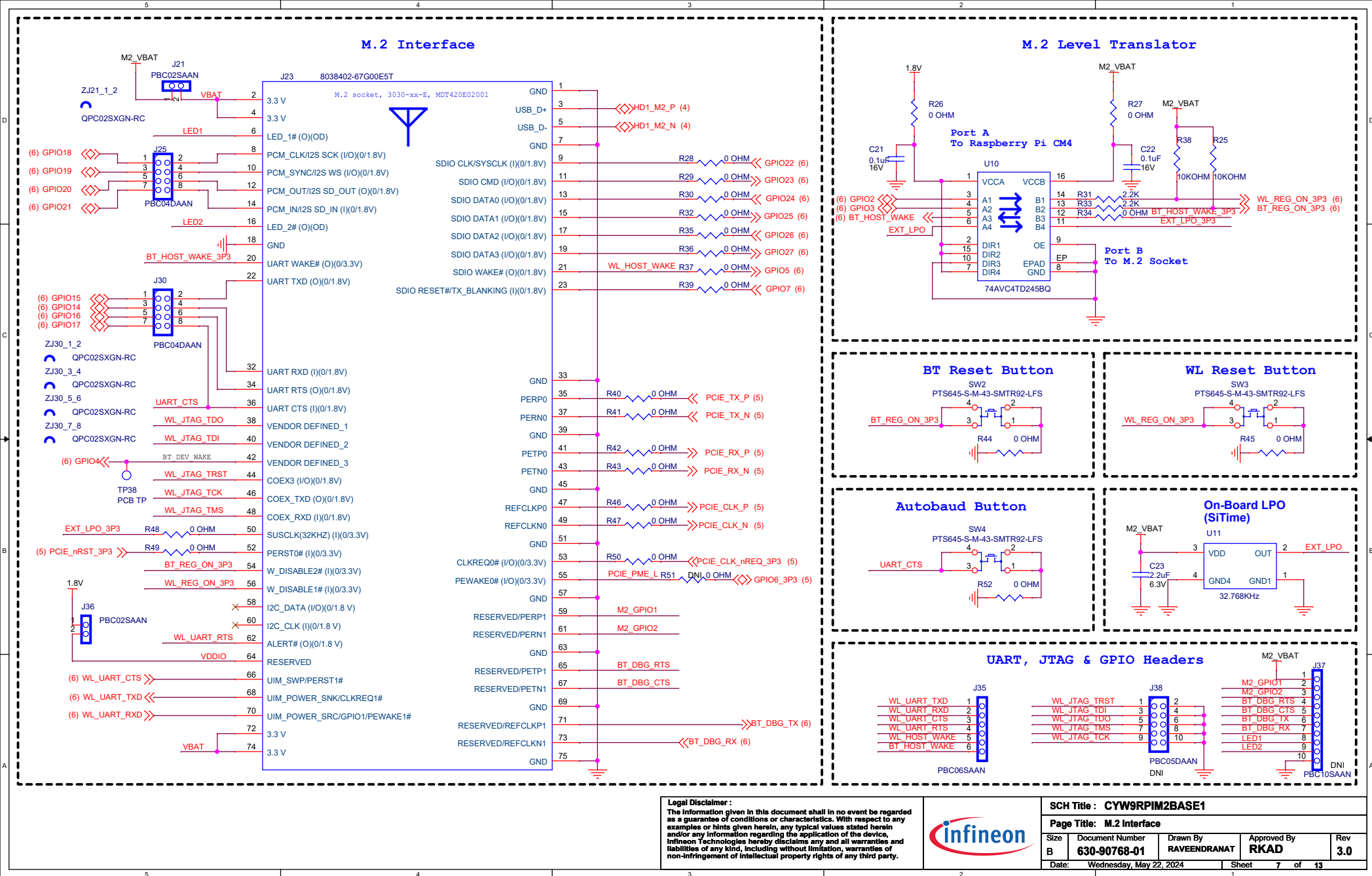
SD Card Interface

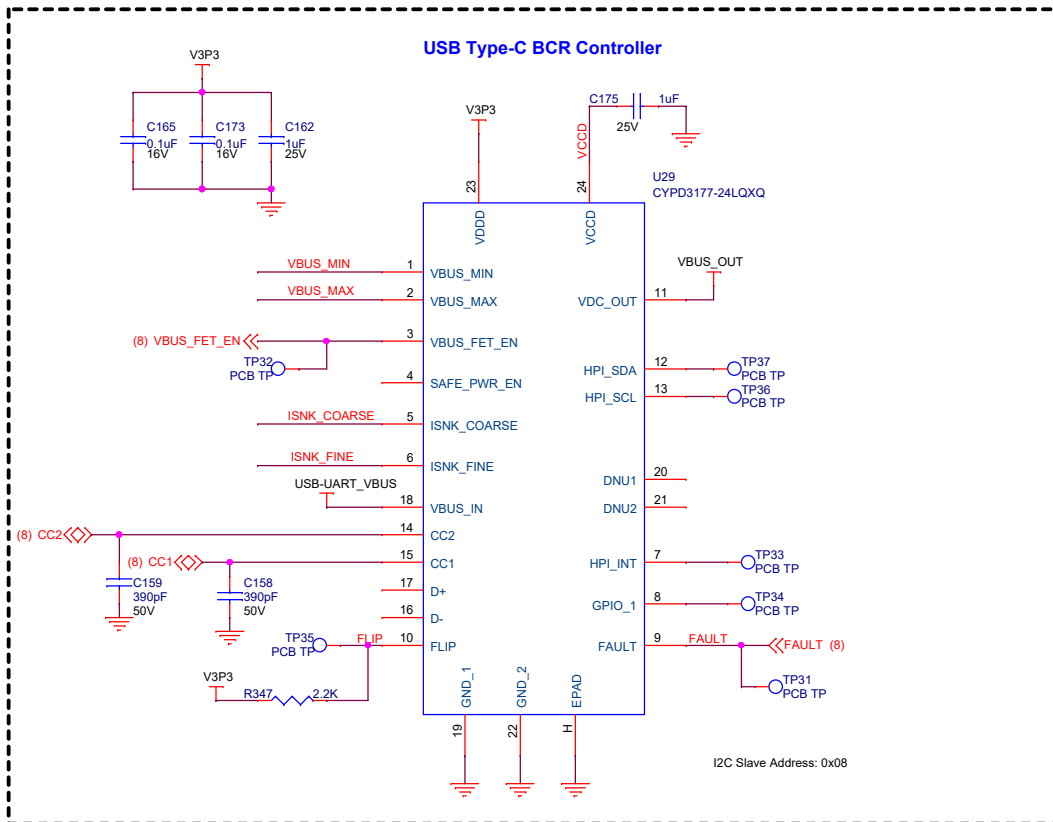


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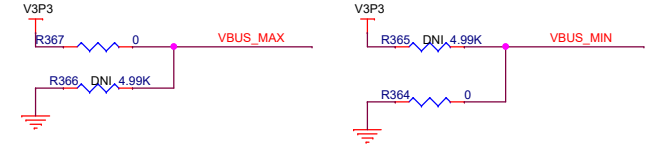
SCH Title : CYW9RPIM2BASE1				
Page Title : CM4 GPIO & Ethernet				
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VBUS Voltage Selectors: VBUS_MAX and VBUS_MIN

Requested voltage = (VBUS_MIN -> VBUS_MAX)
= 5V or 20V



VBUS_MAX is decided by the Resistor options.
Default VBUS_MAX is set to 20V

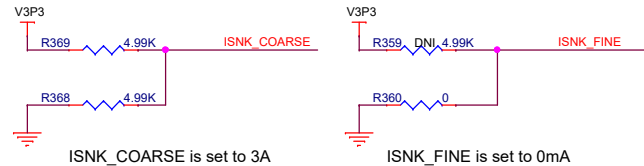
VBUS_MIN is set to 5V

VBUS_MIN and VBUS_MAX Resistor Options Table

V3P3 RATIO	0/6	1/6	2/6	3/6	>=5/6
VBUS_MAX, VBUS_MIN	5V	9V	12V	15V	20V
PULLUP* (R365, R367)	None	4.99K	4.99K	4.99K	0
PULLDOWN* (R364, R366)	0	1K	2.4K	4.99K	None

VBUS CURRENT SELECTORS: ISNK_COARSE and ISNK_FINE

Requested (RDO) current = ISNK_COARSE + ISNK_FINE = 3000mA



ISNK_COARSE and ISNK_FINE Resistor Options Table

V3P3 RATIO	0/6	1/6	2/6	3/6	4/6	>=5/6
ISNK_COARSE	0A	1A	2A	3A	4A	5A
ISNK_FINE	0mA	250mA	500mA	750mA	900mA	
PULLUP* (R359, R369)	None	4.99K	4.99K	4.99K	4.99K	0
PULLDOWN* (R360, R368)	0	1K	2.4K	4.99K	10K	None

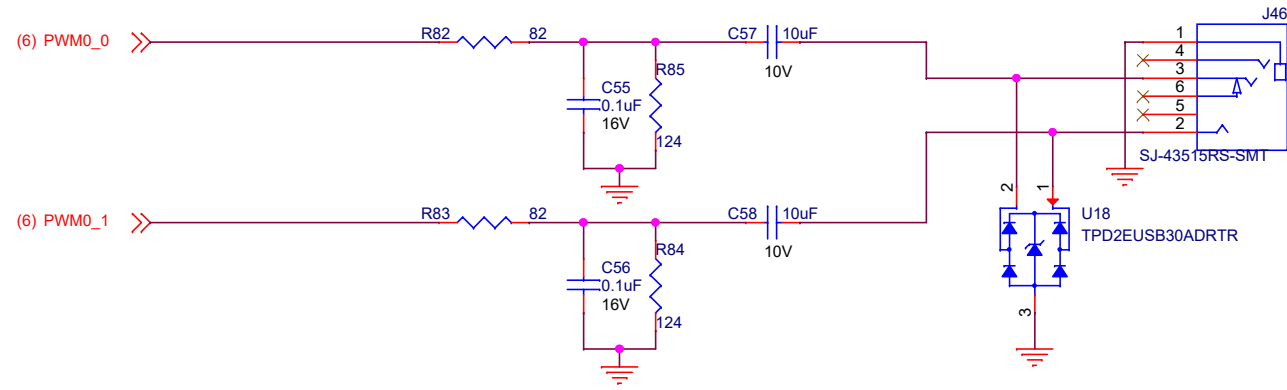
*When pullup-pulldown combination is 0-none or none-0, use any resistor instead of 0-ohm

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Page Title: Type-C BCR Controller				
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Audio Out



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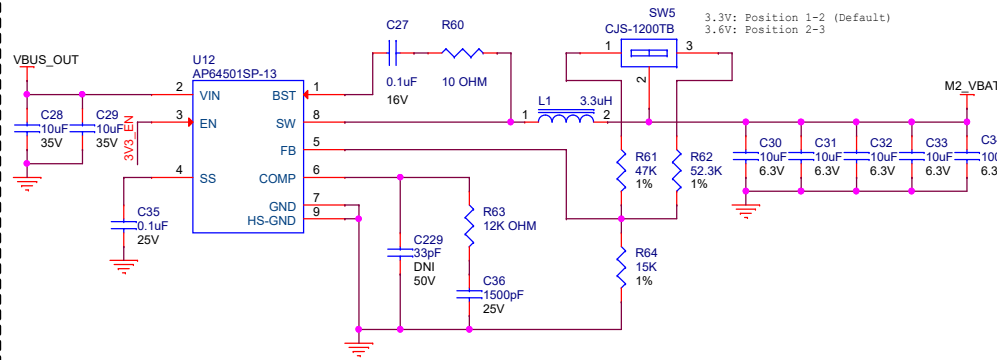


SCH Title : CYW9RPIM2BASE1

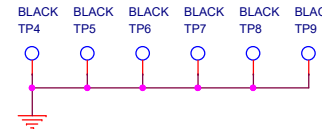
Page Title: Audio Out

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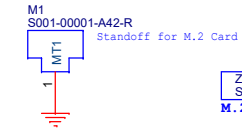
M.2 3.3V/3.6V Regulator



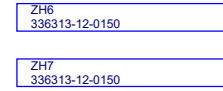
GND Testpoints



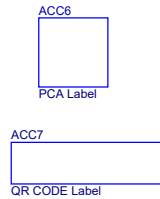
M.2 Connector Accessories



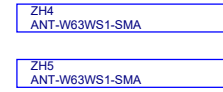
SMA Cable



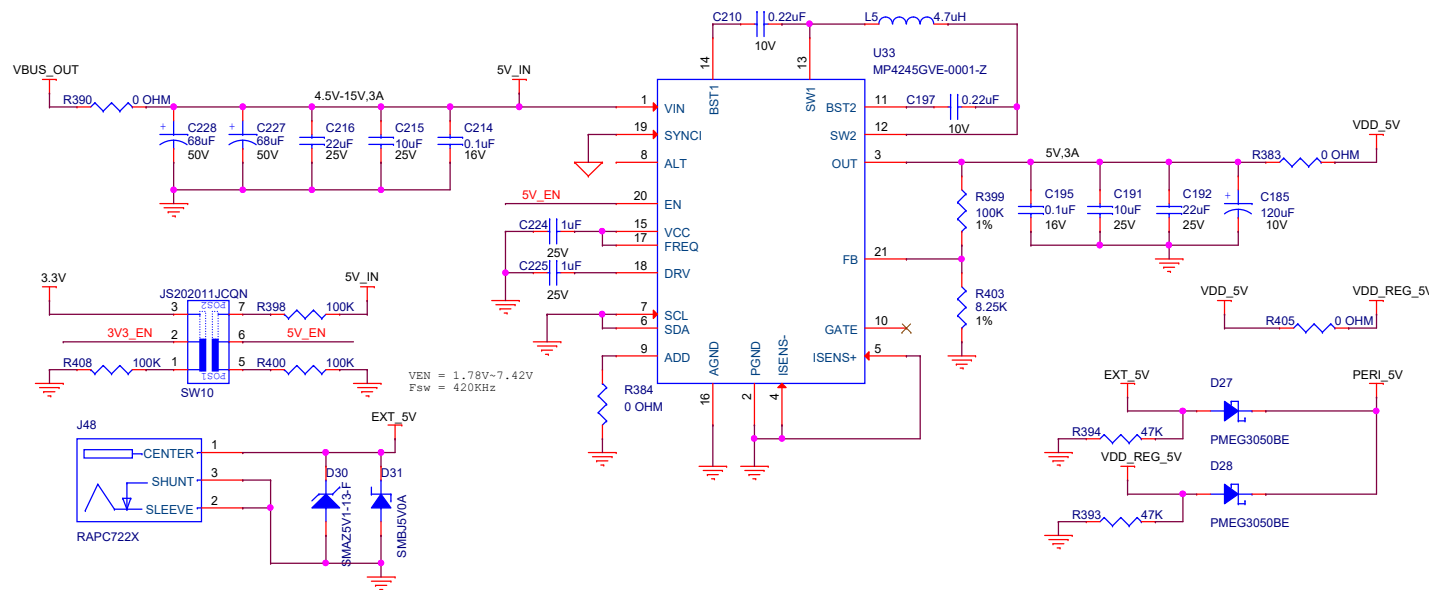
Labels



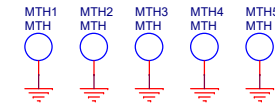
Antenna



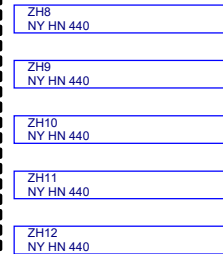
5V Buck-Boost Regulator



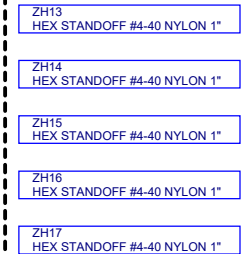
Mounting Holes



Hex Nut



Hex Standoff



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Page Title : Power Supply

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CM4 GPIOs:	M.2 I/F:	Shared Functions:
GPIO2	WL_REG_ON	
GPIO3	BT_REG_ON	
GPIO4	BT_DEV_WAKE	
GPIO5	SDIO_WAKE	
GPIO6	PCIE_PME_L	
GPIO7	SDIO_RESET#	
GPIO8	WL_UART_RXD	RPI_UART_RXD
GPIO9	WL_UART_TXD	RPI_UART_TXD
GPIO10	BT_DBG_RX	RPI_UART_RTS
GPIO11	WL_UART_CTS	RPI_UART_CTS
GPIO12	BT_HOST_WAKE	AUDIO_OUT_PWM0_0
GPIO13	BT_DBG_TX	AUDIO_OUT_PWM0_1
GPIO14	UART_RXD	
GPIO15	UART_TXD	
GPIO16	UART_RTS	
GPIO17	UART_CTS	
GPIO18	PCM_CLK	
GPIO19	PCM_SYNC	
GPIO20	PCM_OUT	
GPIO21	PCM_IN	
GPIO22	SDIO_CLK	
GPIO23	SDIO_CMD	
GPIO24	SDIO_DATA0	
GPIO25	SDIO_DATA1	
GPIO26	SDIO_DATA2	
GPIO27	SDIO_DATA3	

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SCH Title : CYW9RPIM2BASE1				
Page Title: GPIO Mappings and Config.				
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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	Orig. of Change	DATE
1.0	Initial Release	CLEU	3/18/2022
2.0	1. Updated on-board LPO connection 2. Populated R48 and R49	CLEU	8/23/2022
3.0	1. Added USB-UART bridge for RPI debug 2. J1 changed to Type-C Connector 3. Removed J6 and J7 and updated U15 to 1-bit level shifter. 4. Added 100nF cap between GND and P4,P5 pins of J11. 5. J40, J15,J16,J18,J19,J20,J24 and J31 headers changed to dip switches. 6. J35,J37 and J38 made DNI 7. Added PWM audio output option. 8. Main input power supply changed from 12V DC jack to Type-C connector with BCR controller. Also changed Fan part to 5V. 9. Added power ON-OFF switch(SW10)	RAVEENDRANAT	1/12/2024

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SCH Title : CYW9RPIM2BASE1				
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ERROR: undefined lename
OFFENDING COMMAND: baseboard/gerber/arena31result.txt
STACK: