

8

7

6

5

4

3

P/N

610-90768-01

SH

1

REV

03

1

ECO NO.

REV

DATE

DESCRIPTION

DRAWN

CHECKED

APPROVED

CLEU-102

1.0

03/24/22

INITIAL RELEASE

JYUN

CLEU

CLEU

CLEU-105

2.0

08/24/22

ROTATE SD CARD CONNECTOR

LIKZ

CLEU

CLEU

NA

3.0

03/01/24

POWER SUPPLY AND DEBUG UART UPDATE

SANTHOSH R

SANTHOSH R

NIKHIL K

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:

A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 600-90768-01\_03.TGZ OR 600-90768-01\_03.ZIP

B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.

C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.

D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.

E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.

F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2 DIELECTRIC MATERIAL:

A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).

B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF .076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.

C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.

D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:

A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+0.020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.

B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

4. SOLDER MASK:

A. APPLY LPI SOLDER MASK USING PROVIDED DATA.

B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLACK.

C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:

A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.

B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.

C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:

A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.

B. ALL PCBs SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.

C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7 FINAL FINISH:

A. FINAL FINISH ON ALL EXPOSED CONDUCTORS SHALL BE IMMERSION SILVER PER IPC-4553, .15 - .38 MICROMETERS [6 - 15 MICROINCHES] THICK.

8. IMPEDANCE:

A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.

B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBs SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.

59.40  
+/- 10%

(3.0)

(21.0)

(3.4)

(21.0)

(3.0)

LAYER DESCRIPTION

COPPER WT

SE IMP OHMS

SE TRACE WIDTH

REF LAYER

DIFF IMP OHMS

DIFF TRACE WIDTH/SPACE

REF LAYER

DIFF IMP OHMS

DIFF TRACE WIDTH/SPACE

L01 - TOP

1.4

50

5.5

2

100

4.5/6.5

2

90

5.0/5.0

L02 - GND

1.3

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L03 - PWR

1.3

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L04 - GND

1.3

50

4.4

3/5

100

4.0/9.7

3/5

90

4.2/6.0

L05 - GND

1.3

50

4.0

4/6

100

3.4/8.7

4/6

90

3.7/5.2

L06 - BOTTOM

1.4

50

5.5

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5

90

5.0/5.0

STACK-UP ( UNIT : MIL )

SEE BOM

SEE BOM

NEXT ASSY

USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS

.xxx

.xx

ANGLES

±.064

±.13

±.5°

[±.005]

[±.01]

MATERIAL

2

FINISH

7

DO NOT SCALE DRAWING

APPROVALS

DATE

DRAWN

SANTHOSH R

03/01/24

ENGINEER

NIKHIL K

03/01/24

CHECKER

SANTHOSH R

03/01/24

QA

PROJ. ENG.

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Infineon

Infineon Technologies AG  
IFAG MUC Am Campeon 1-15  
85579 NEUBIBERG - GERMANY

TITLE

PCB FABRICATION,  
CYW9RPIM2BASE1

SIZE

D

CAGE CODE

-

P/N

610-90768-01

SCALE

1/1

SHEET

1 OF 2

REV

03

COMPUTER GENERATED DRAWING  
DO NOT CHANGE MANUALLY

FAB NOTES REV 08/01/14

7

6

5

4

3

2

ALLEGRO BOARD FILE : 600-90768-01\_03

