CYW9P62S1-43012CAR-01
PSoC 6 (1M) with CYW43012 USI SiP Carrier Module

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Drawing Numbers

PCBA	121-60559-01
PCB	600-60559-01
FAB DRW	610-60559-01
ASSY DRW	620-60559-01
SCH DRW	630-60559-01

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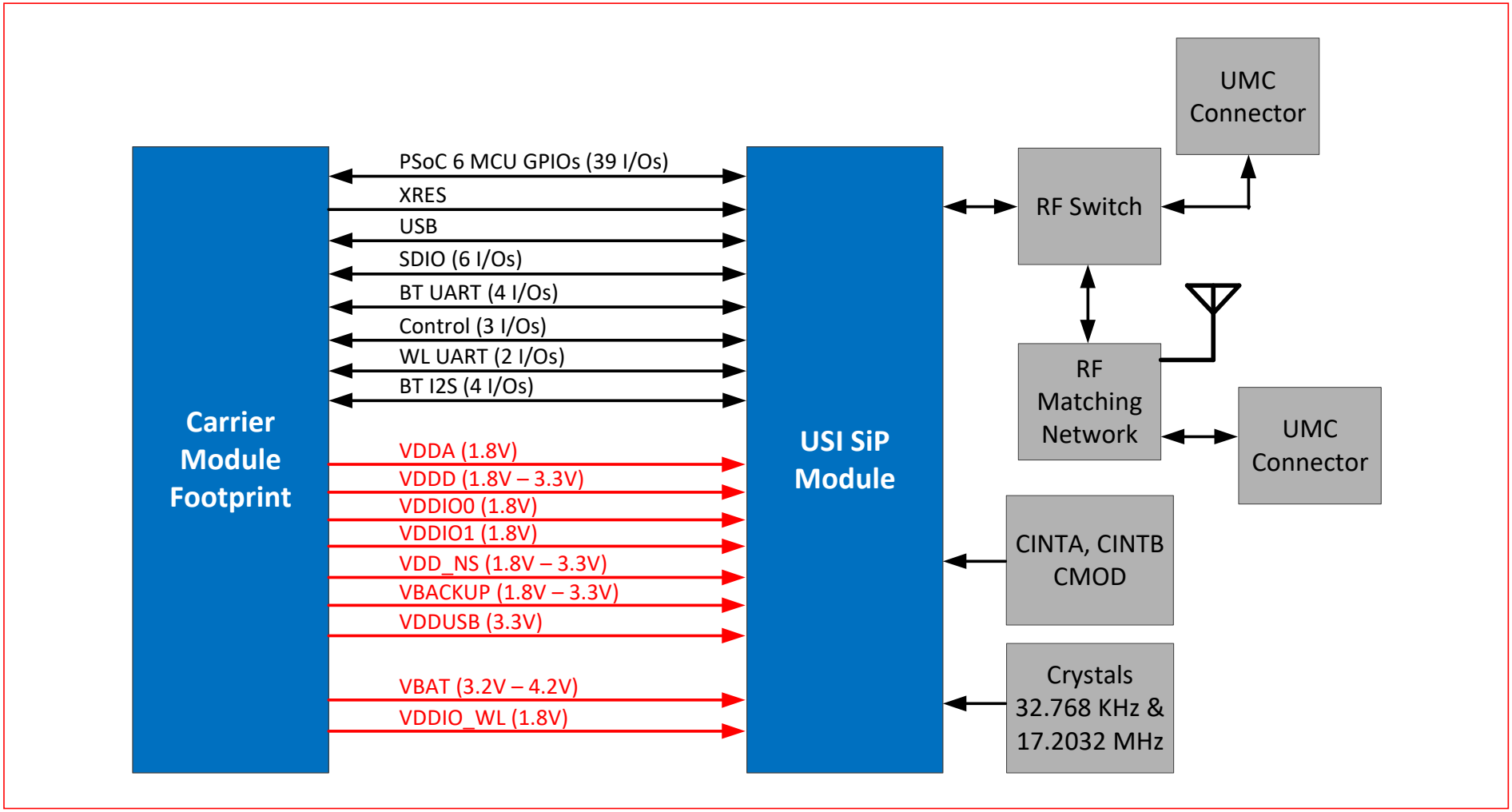
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Page Title : Title Page

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Block Diagram



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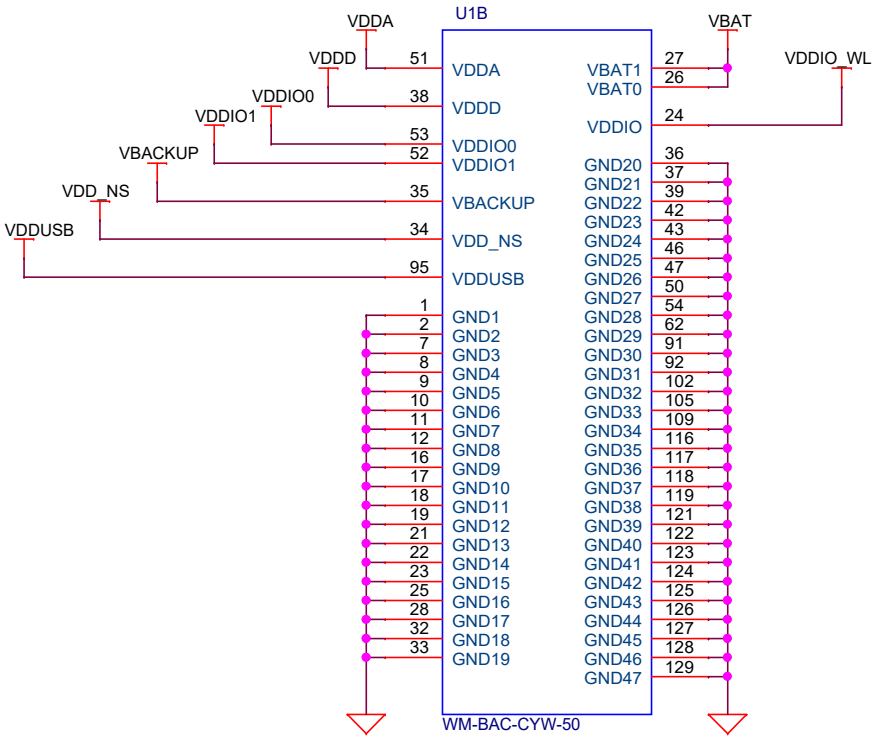
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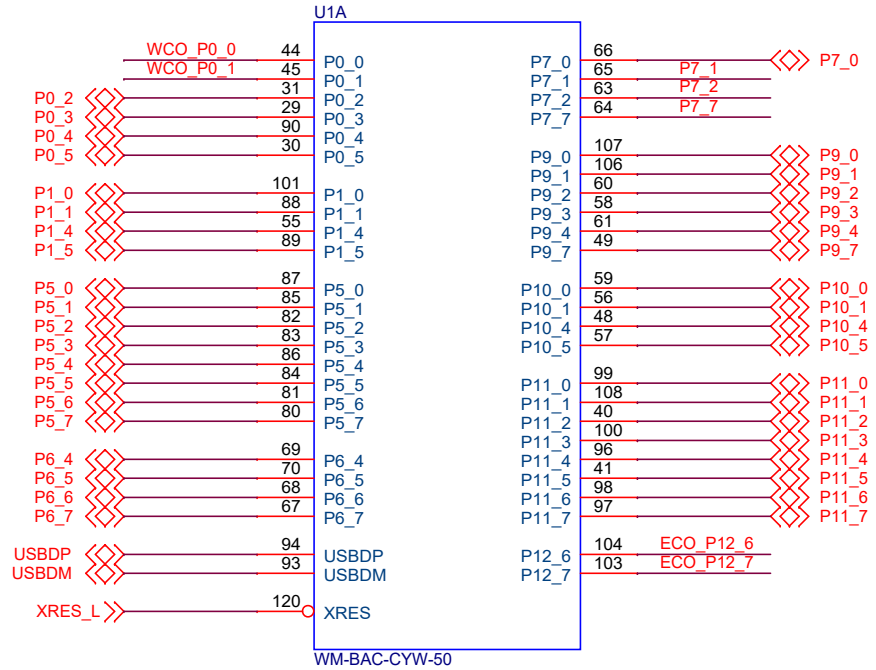
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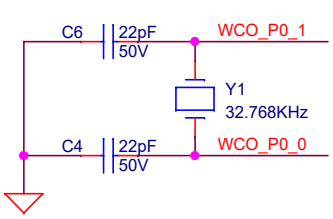
USI SiP Module Power



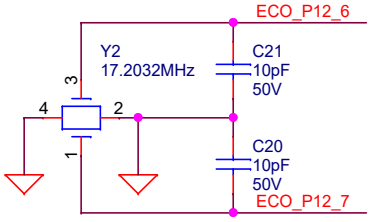
USI SiP Module PSoC 6 MCU Signals



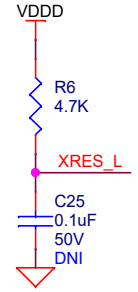
WCO



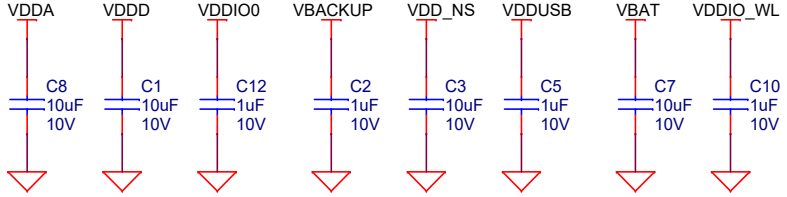
ECO



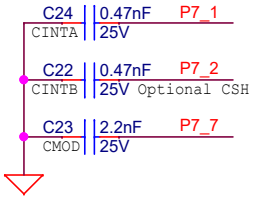
Pull-up for Reset



Decoupling Capacitors



CINT, CMOD & CSH

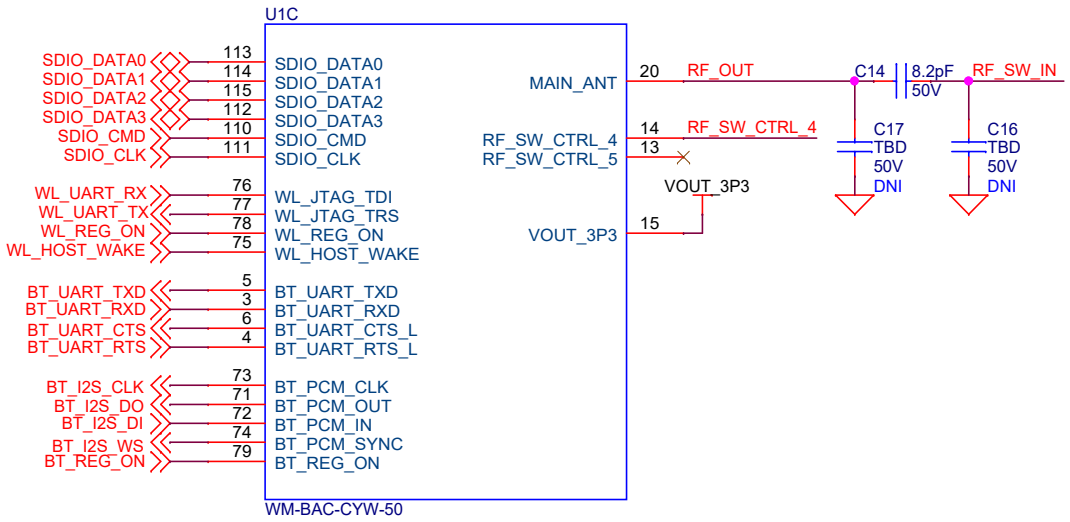


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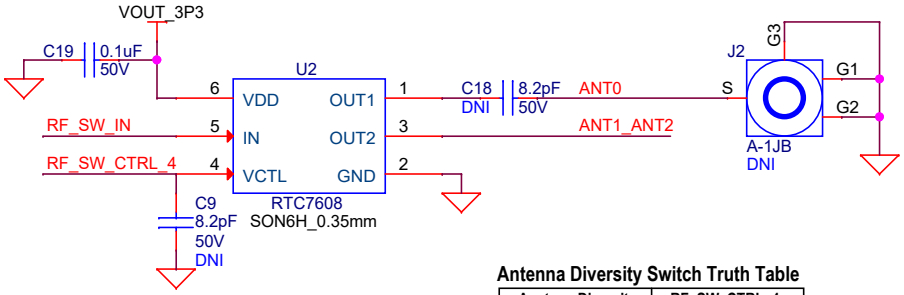
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USI SiP Module CYW43012 Signals



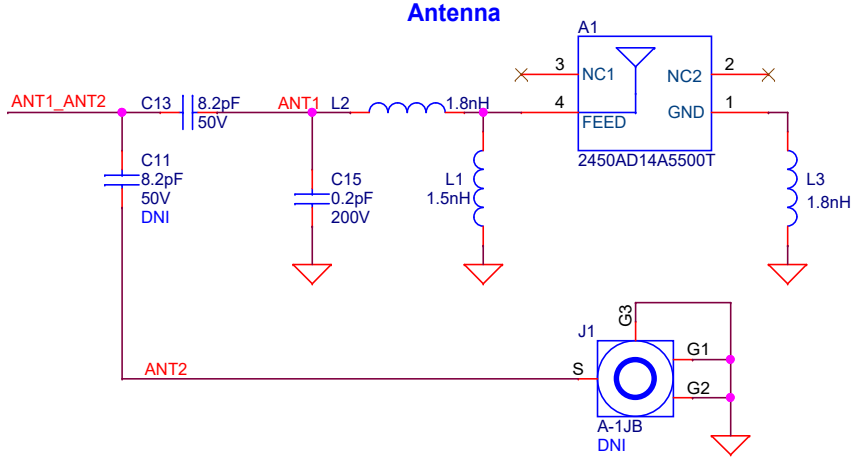
Antenna Diversity Switch



Antenna Diversity Switch Truth Table

Anetnna Diversity	RF_SW_CTRL_4
ANT1 (default)	0
ANT0	1

Antenna



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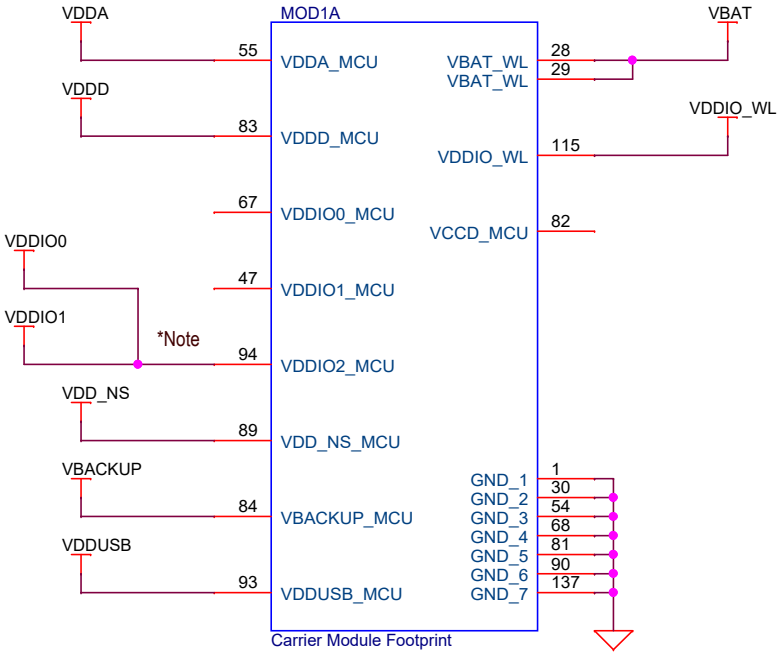
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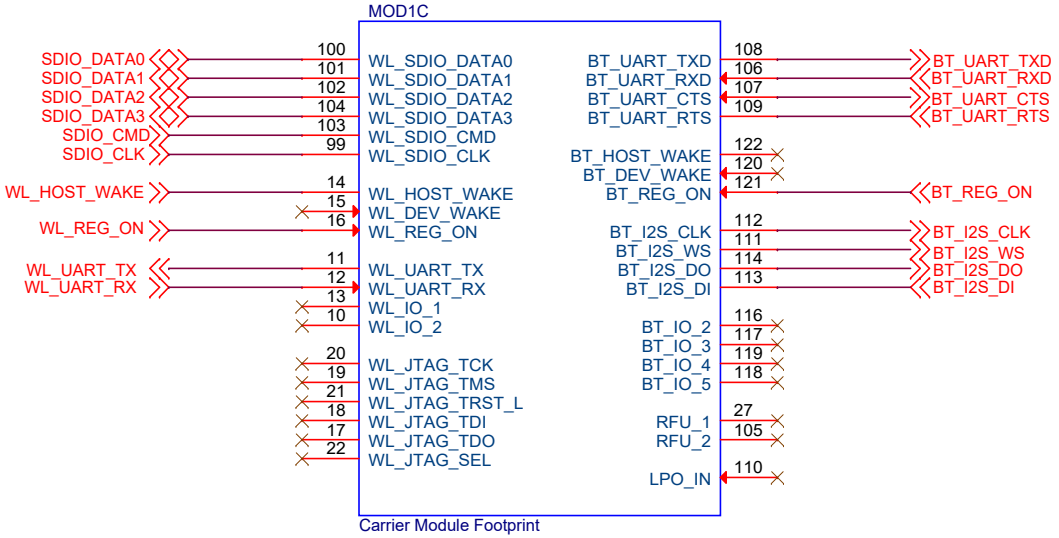
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Carrier Module Footprint (Power)



Note: In WM-BAC-CYW-50, VDDIO0 & VDDIO1 need to be same voltage as VDDIO_WL.
VDDIO2_MCU will be same voltage as VDDIO_WL as per baseboard design, the reason
VDDIO0 & VDDIO1 connected to VDDIO2_MCU

Carrier Module Footprint (Wi-Fi BT Signals)

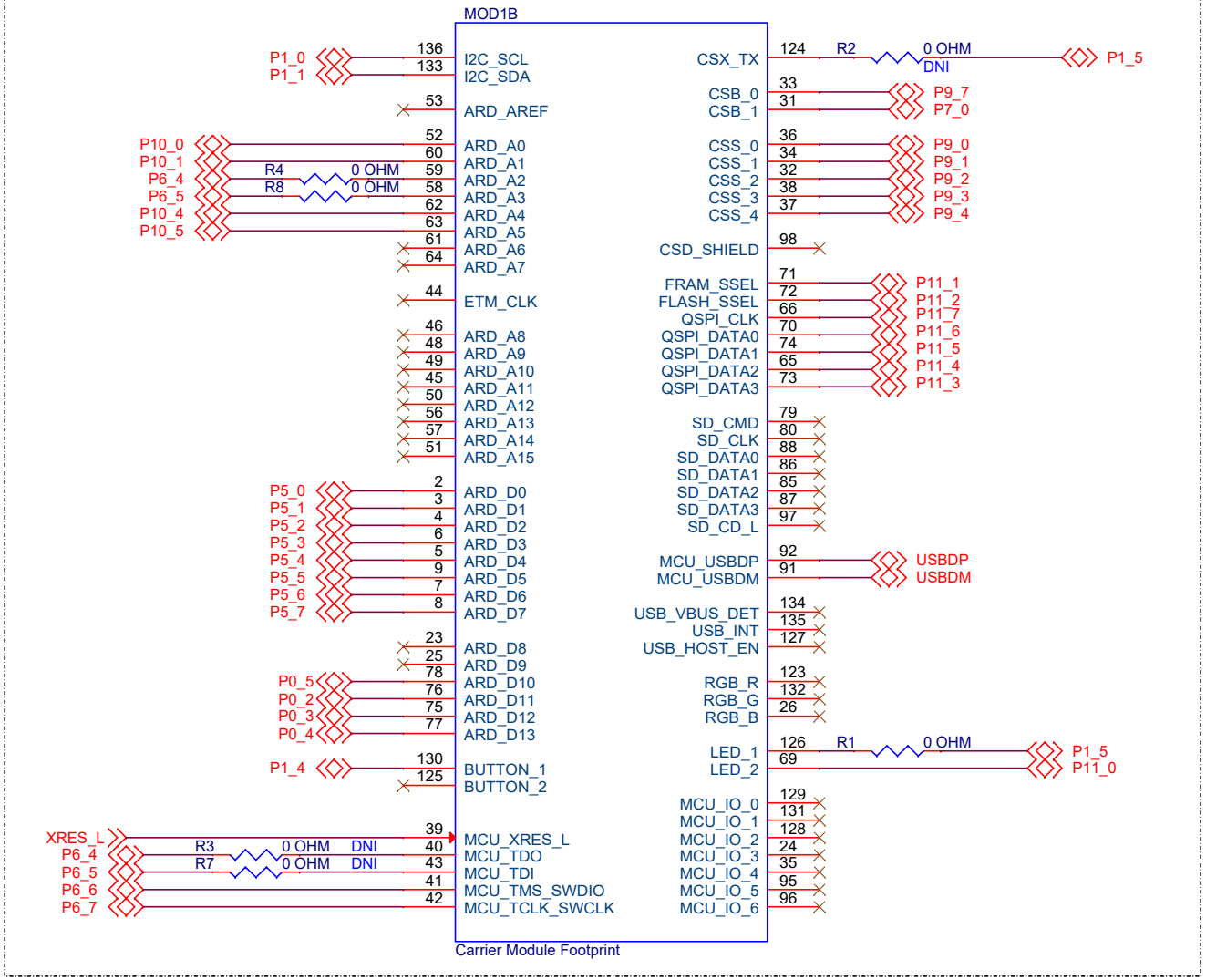


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Carrier Module Footprint (PSoC 6 MCU Signals)



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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	Orig. of Change	DATE
01	Internal Release	AARA	2019/07/10
02	Internal Release	AARA	2019/10/31
03	Initial Release	TARE	2020/01/16

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