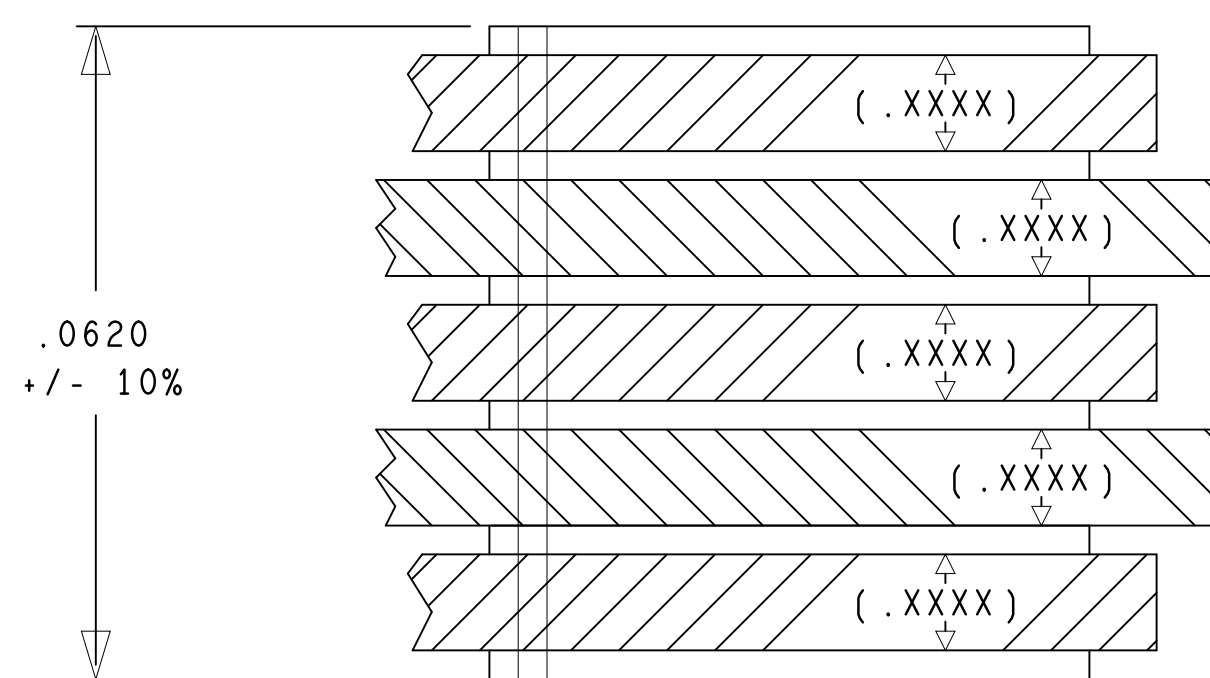


Diagram illustrating a 1D chain with 8 sites. The sites are numbered 1 to 8 from right to left. The occupancy of each site is as follows:

- Site 1: Red fermion
- Site 2: Blue fermion
- Site 3: Red fermion
- Site 4: Blue fermion
- Site 5: Red fermion
- Site 6: Blue fermion
- Site 7: Red fermion
- Site 8: Blue fermion

NOTES: UNLESS OTHERWISE SPECIFIED



1. SPECIFICATIONS/TOLERANCES:
 - A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 600-60607-01_02.TG2 OR 610-60607-01_02.ZIP.
 - B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
 - C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
 - D. REMOVE ALL BURRS AND BREAK SHARP EDGES. .381 [.015] MAX RADIUS.
 - E. PARENTHEThICAL INFORMATION IS FOR REFERENCE ONLY.
 - F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.
2. DIELECTRIC MATERIAL:
 - A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (R6HS COMPLIANT EPOXY-GLASS).
 - B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF .076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
 - C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
 - D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.
3. DRILLING:
 - A. VIA DIAMETERS [TOL. = +.051/- DRILL DIAMETER [+ .0020/- DRILL DIAMETER]] SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
 - B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.
4. SOLDER MASK:
 - A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
 - B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.
 - C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.
5. MARKING:
 - A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
 - B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
 - C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.
6. ELECTRICAL TEST:
 - A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
 - B. ALL PCBs SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
 - C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.
7. FINAL FINISH:
 - A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.
8. IMPEDANCE:
 - A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
 - B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.
9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBs SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.



LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF LAYER	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER
L01 - TOP	0.5 OZ	50	.0060	02	90	.0050/.0080	02
L02 - PLANE	1.0 OZ	--	-----	---	---	----	---
L03 - SIGNAL	1.0 OZ	50	.0060	02	90	.0050/.0080	02
L04 - SIGNAL	1.0 OZ	50	.0060	05	---	-----	--
L05 - PLANE	1.0 OZ	--	-----	---	---	----	---
L06 - BOTTOM	0.5 OZ	50	.0060	05	90	.0050/.0080	05

STACK - UP

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	
<p>THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO Infineon Technologies AG AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHERE SUCH USER POSSESSES AUTHORIZATION FROM Infineon Technologies AG.</p>	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS		
.XXX ±.064 [+.005]	.XX ±.13 [+.01]	ANGLES ±.5°
MATERIAL		
FINISH		

DO NOT SCALE DRAWING	
APPROVALS	DATE
DRAWN TESSOLVE	03/06/21
ENGINEER AARA	03/06/21
CHECKER AARA	03/06/21
QA	
PROJ. ENG.	

Infineon Technologies AG
Am Campeon 1-15
85579 NEUBIBERG - GERMANY

TITLE

PCB FABRICATION,

CY8CEVAL-06XS2 PSoc™ 6XS2 evaluation kit

SIZE	CAGE CODE	CY P/N
D	-	610-60607-01

SCALE	SHEET
1/1	1 OF 2

REV 03

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ALLEGRO FILE: 600-60607-01_02.BRD

D

C

B

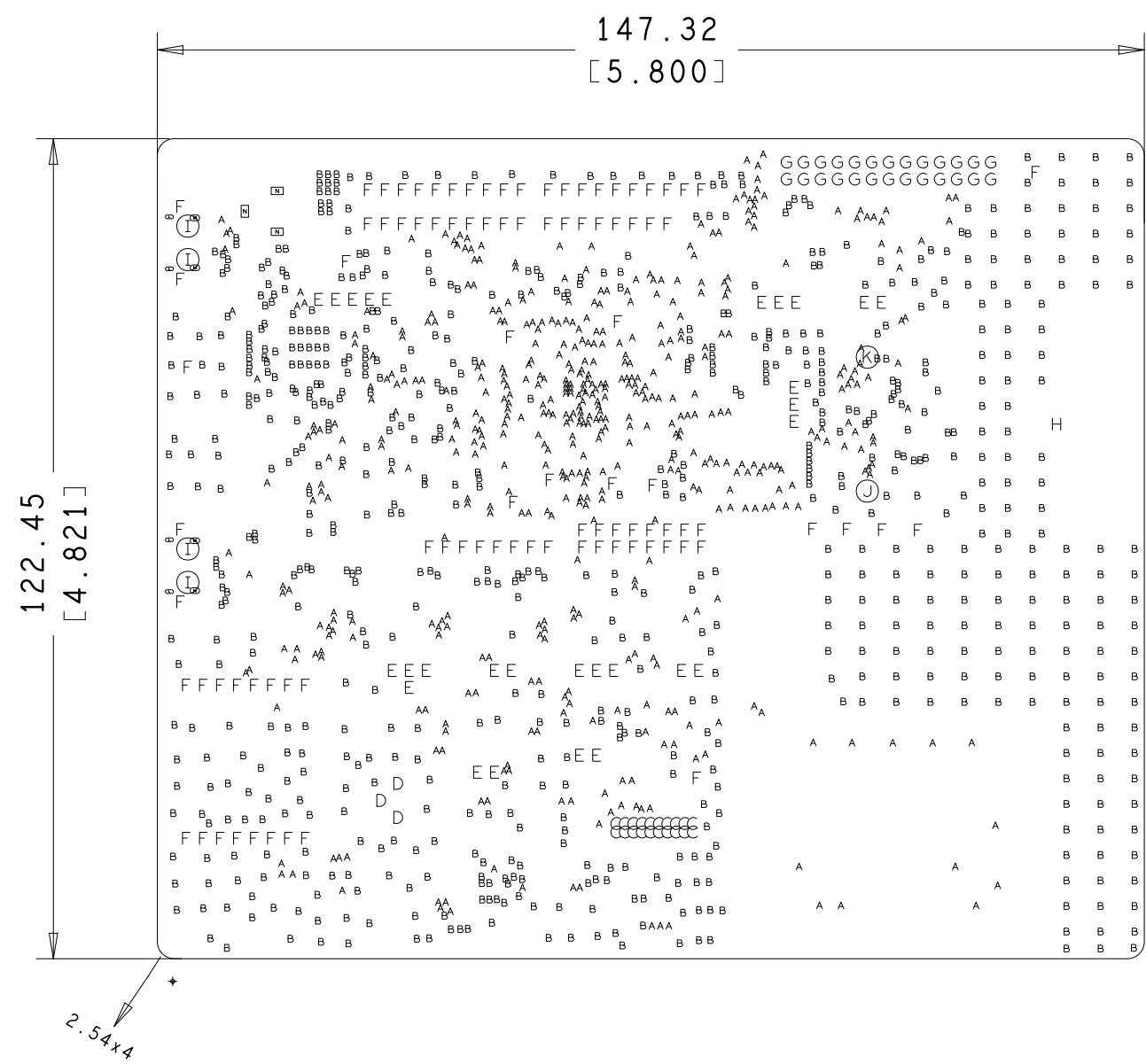
A

D

C

B

ALLEGRO FILE: 600-60607-01_02.BRD



DRILL CHART: TOP to BOTTOM						
ALL UNITS ARE IN MILS						
FIGURE	FINISHED_SIZE	ROTATION	TOLERANCE_DRILL	TOLERANCE_TRAVEL	PLATED	QTY
A	7.87	-	+1.97/-7.87	-	PLATED	498
B	9.84	-	+1.97/-9.84	-	PLATED	719
C	27.56	-	+2.99/-2.99	-	PLATED	20
D	29.92	-	+2.99/-2.99	-	PLATED	3
E	39.37	-	+2.95/-2.95	-	PLATED	28
F	40.16	-	+2.99/-2.99	-	PLATED	96
G	41.34	-	+2.95/-2.95	-	PLATED	26
H	169.29	-	+2.95/-2.95	-	PLATED	1
①	31.5	-	+1.97/-1.97	-	NON-PLATED	4
②	43.31	-	+1.97/-1.97	-	NON-PLATED	1
③	62.99	-	+1.97/-1.97	-	NON-PLATED	1
④	47.24x21.65	0.000	+2.99/-2.99	+2.99/-2.99	PLATED	4
⑤	55.12x33.46	0.000	+2.99/-2.99	+2.99/-2.99	PLATED	4
⑥	70.0x43.31	0.000	+3.0/-3.0	+3.0/-3.0	PLATED	2
⑦	70.0x43.31	90.000	+3.0/-3.0	+3.0/-3.0	PLATED	1