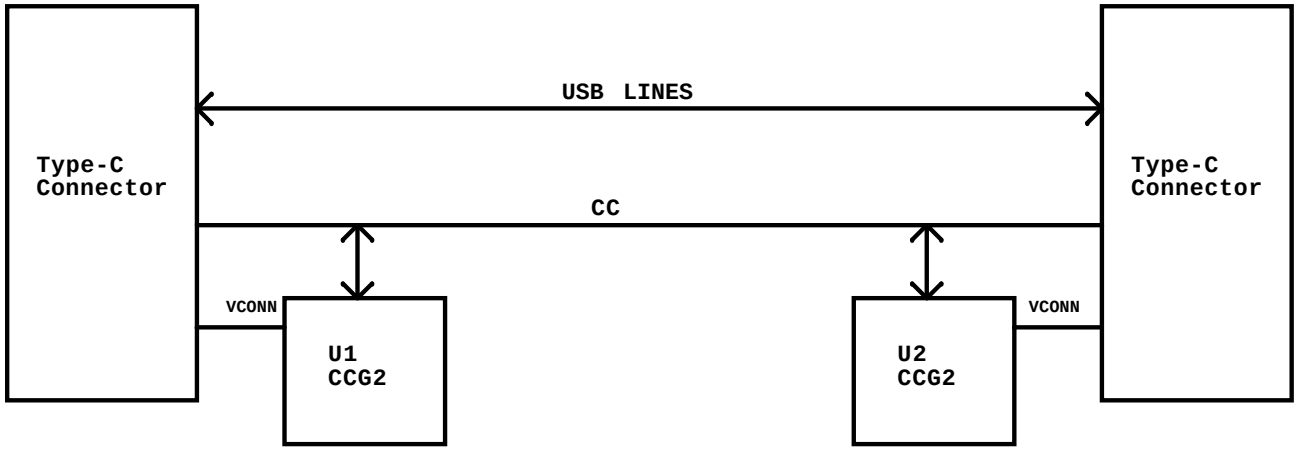
BLOCK DIAGRAM



PCA: 121-60200-01
PCB: 600-60233-01
FAB DRW: 610-60223-01
ASSY DRW: 620-60231-01

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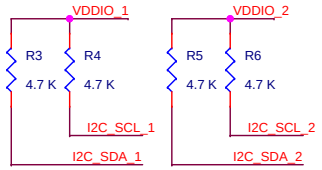
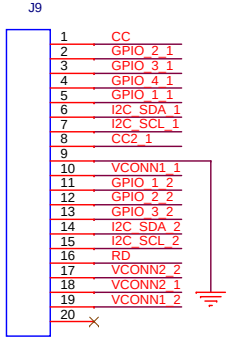
I2C pullups

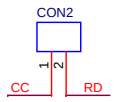


All resisitances are NO LOAD

Header to bring out various signals

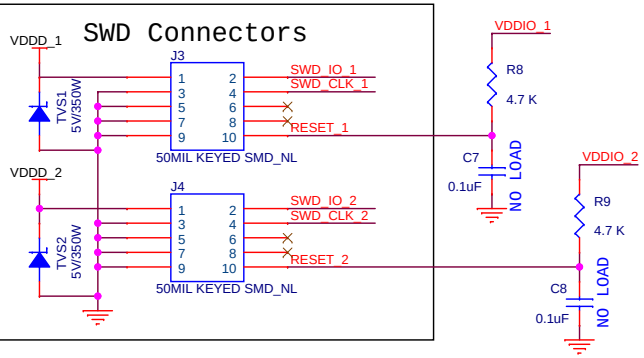


Enable RD on CC



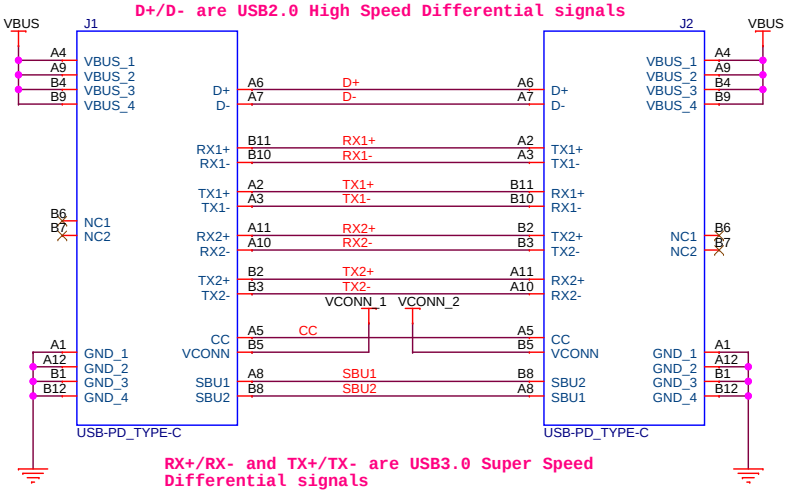
NO LOAD

SWD Connectors



USB Type-C Plugs

D+/D- are USB2.0 High Speed Differential signals



RX+/RX- and TX+/TX- are USB3.0 Super Speed Differential signals

Dual Chip Configuration Both Powered

PCA:	121-60200-01
PCB:	600-60233-01
FAB DRW:	610-60223-01
ASSY DRW:	620-60231-01

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Revision	Description of the change
02	Updating for the sanity no changes in the schematic
03	Changing the revision number to match with Layout
04	Changing the revision number to match with Layout
05	Adding a pull-up on the XRES line of each chip
06	Added Jumper J8 Increases R1 and R2 from 150 Ohms to 1K Ohms
07	Replaced U2 with CYPD2103-14LHXIT Updated jumpers, changes jumper numbers Added additional TVS diode for J4 and seperated VDDD rails for both the chips U1 and U2 Changed LED from P2[1] to P1[5]
08	Changed the MPN to CY4502

PCA: 121-60200-01
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