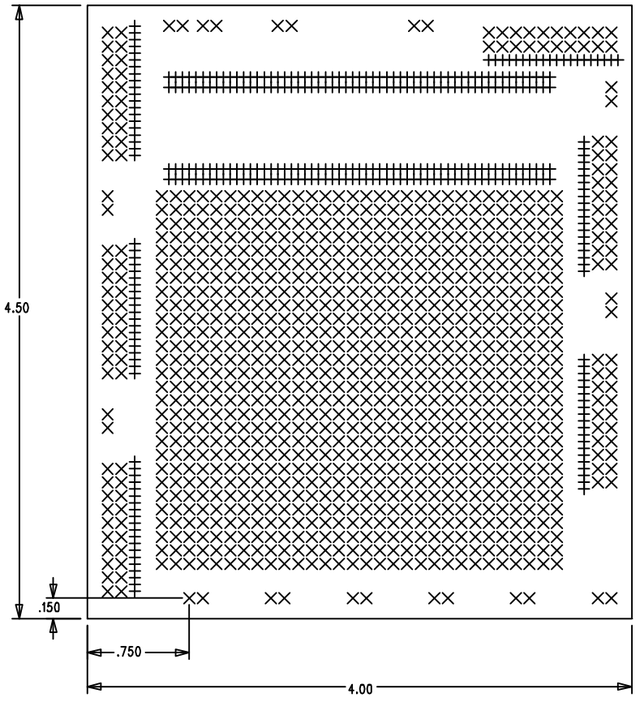
REVISION RECORD			
LTR	DESCRIPTION	APPD	DATE
*A	RELEASE FOR PROTO	SYK	7/12/00



SIZE	QTY	SYM	PLTD
20	348	+	PLTD
37	988	X	PLTD

13. Minimum trace thikness is .010 maximum .050 minimum trace to trace .010.
12. .060" maximum on all inside corners.
11. Dimensions and tolerances per ANSI Y14.5M
10. Fabricate boards in accordance with IPC-6012, Class 2 products.
9. Board shall meetl the requirements of UL796 with a flammablity rating of 94V-D vendor's of logo or desination shall be on solder side of board.
8. Remove all burrs and break sharp edges .015 Max.
7. Silkscreen component & solder side of board using permanent, non-conductive, epoxy base ink; white in color.
6. Warp or Twist of board shall not exceed .010 inch per inch.
5. Boards are to be manufactured using the solder-mask over bare copper (SMOBC) process. Solder-mask shall be Liquid Photoimageable (LPI), semi gloss green in color; and must meet the requirements of IPC-SM-840, for Class 'T' products.
4. Conductor widths and spacing shall be within +/-20% of artwork orginals.
3. All holes shall be located within .003' Diametor of true position layer to layer registration shall be within .003'. All holes surrounded by land shall have a minimum annualar ring of .003.
2. Unless otherwise specified, all hole dimensions apply after plating . Specified hole sizes are to be held within a tolerance of +/-.003". Copper plating on hole walls shall be .0008" 'average minimum', and .0007" minimum
1. Material: Plastic Sheet, Laminaed Glass-Epoxy, as per. MIL-SH-13949H/4. Copper clad with 1oz./sq.' on all "Signal" layers, and 2oz/sq.' on "Plane" layers. "Outer" layers to have aminimum of 1oz/sq.' finished. Laminate using pre-preg materials as per. MIL-S-13949H/12. Finished overall board thickness to be .062"+/-.007".

Notes: Unless Otherwise Specified

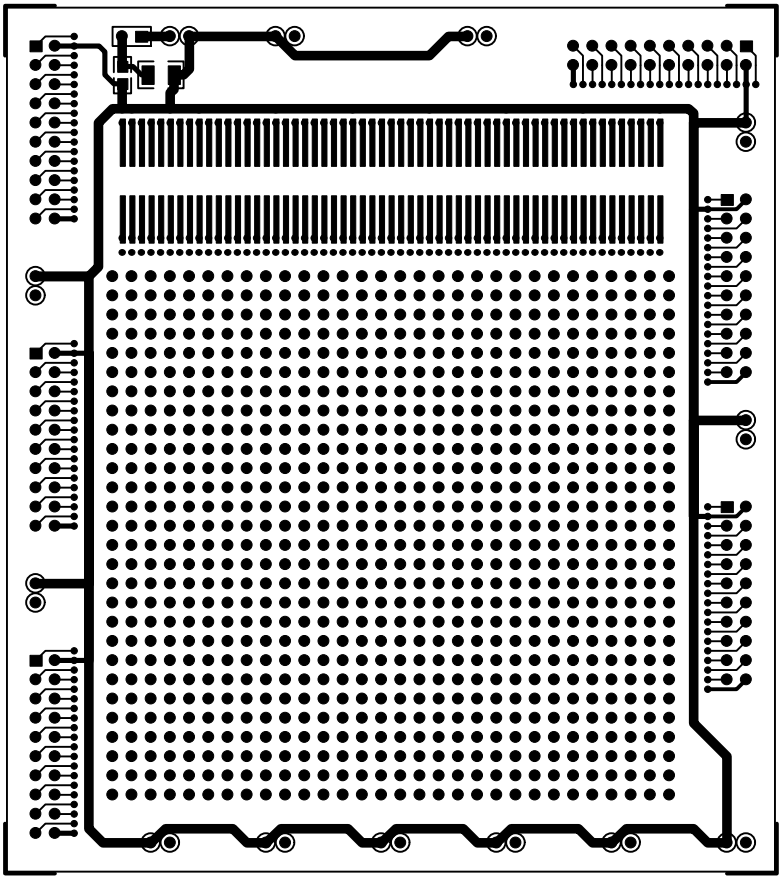
DRAWN: M.KINGSLEY	DATED: 07-12-00	
CHECKED: M.DEJULIO	DATED: 07-12-00	
ENG: S.KOLOKOWSKY	DATED: 07-12-00	
RELEASED:	DATED:	

COMPANY: CYPRESS SEMICONDUCTOR
PCB DESIGN
15050 Avenue of Science, San Diego CA 92128

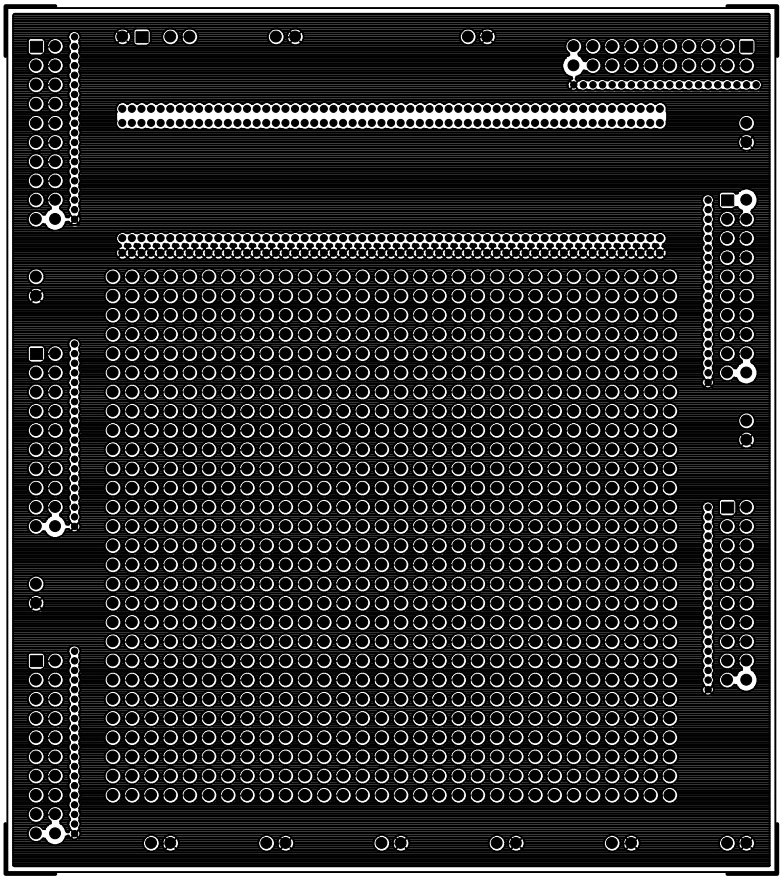
TITLE: FX2 BREADBOARD

MODEL	DRAWING NO:	REV:
FX2	PDC-9022	*A

SCALE:1/1 SHEET: 1 OF 1



CYPRESS SEMICONDUCTOR			15050 Avenue of Science San Diego, CA 92128 Tel: (858) 613-7900 Fax: (858) 676-6896
ENGINEER: Lane Hauck PHONE: 858-613-7927	TITLE: FX2 BREADBOARD		FILE NAME: PDC-9022-A.PCB
PCB DESIGNER: MIKE KINGSLEY PHONE: 858-613-7931	PART NO.: PDC-9022	REV: *A	DATE: 12-JULY-00
COMPONENT SIDE LAYER 1			GERBER: COMP9022.pho



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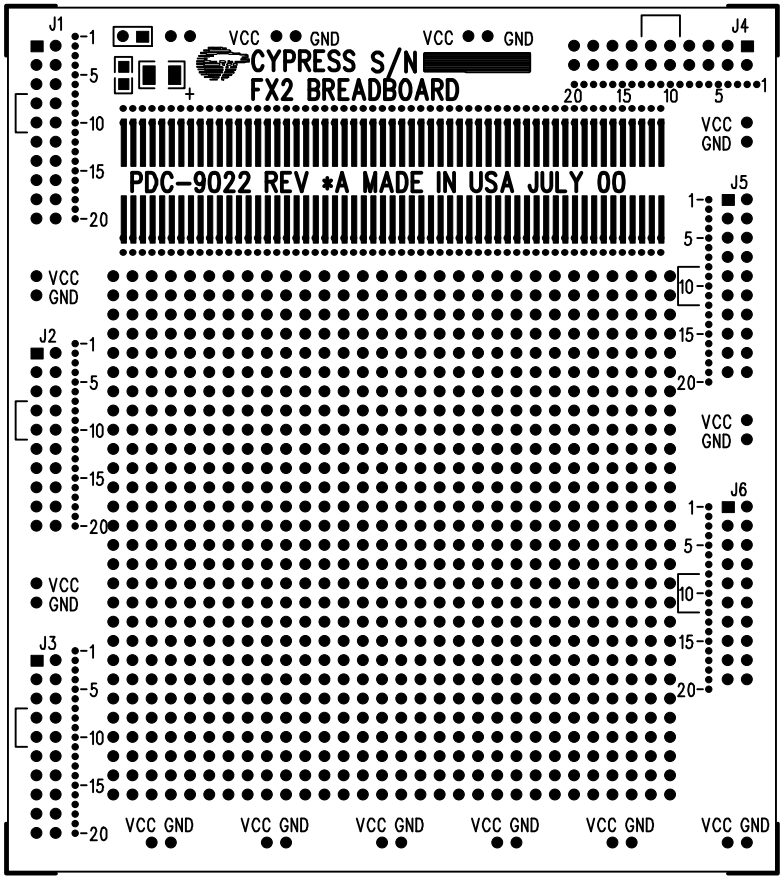
PCB DESIGNER: MIKE KINGSLEY PHONE: 858-613-7931	PART NO.: PDC-9022	REV: *A	DATE: 12-JULY-00
SOLDER SIDE LAYER 2			GERBER: SOLDER9022.pho



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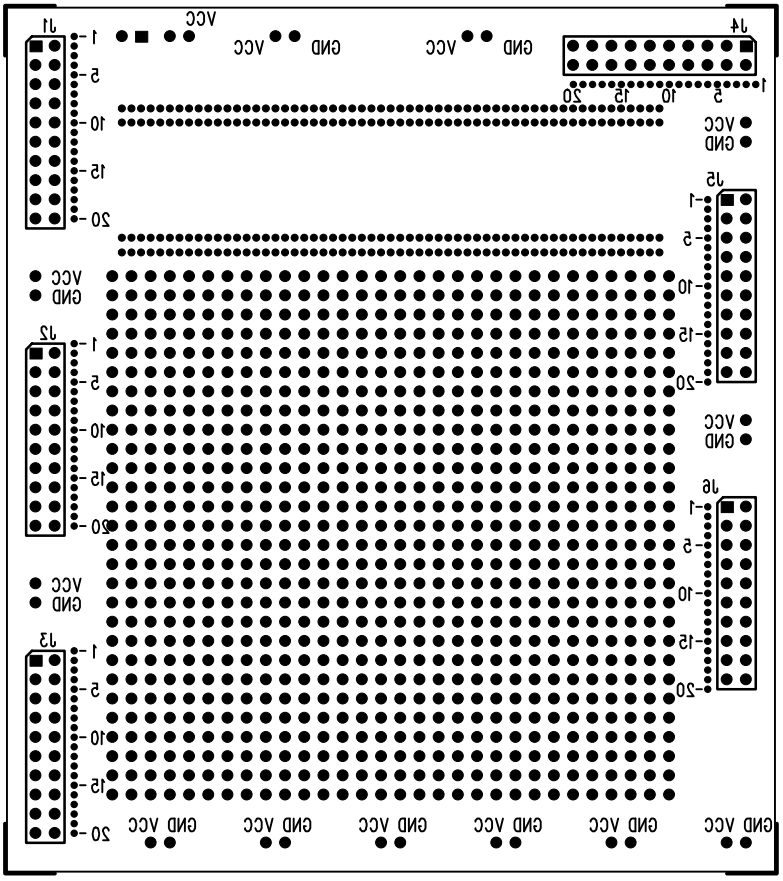
PCB DESIGNER: MIKE KINGSLEY PHONE: 858-613-7931	PART NO.: PDC-9022	REV: *A	DATE: 12-JULY-00
SILKSCREEN COMPONENT SIDE			GERBER: SLKCP9022.pho



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ENGINEER: Lane Hauck PHONE: 858-613-7927	TITLE: FX2 BREADBOARD		FILE NAME: PDC-9022-A.PCB
PCB DESIGNER: MIKE KINGSLEY PHONE: 858-613-7931	PART NO.: PDC-9022	REV: *A	DATE: 12-JULY-00
SILKSCREEN SOLDER SIDE			GERBER: SLKSD9022.pho