



WHITEPAPER

Switch faster, regulate faster, protect faster with PSOC™ Control C3 Performance Line microcontrollers

How high-speed control, precision timing, and hardware acceleration enable next-generation PSUs, IBCs, and BBUs

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Abstract

AI data center power design has entered a new phase, but it does comes with challenges. The first challenge is architectural: how to move enough power into dense AI racks efficiently. The next challenge is control: How to switch faster, regulate faster, protect faster, and still keep the firmware architecture manageable. In power supply units (PSUs), intermediate bus converters (IBCs), and battery backup units (BBUs), GaN and SiC power stages are pushing switching frequencies higher while AI workloads are demanding faster dynamic response from every conversion stage.

This whitepaper continues the discussion from Empowering AI Power Supply Innovation with PSOC™ Control C3 Performance Line. Instead of revisiting the rack-level power architecture trends, it focuses on the microcontroller features that make high-frequency digital power practical: the Programmable Power Control Accelerator (PPCA), 25 MSPS ADC subsystem, sub-100 ps high-resolution PWM, comparators with slope generation, hardware 3P3Z filters, Custom Logic Block, Event Processing Unit, PMBus and CAN FD interfaces, safety libraries, and security capabilities. The goal is to help power designers connect system-level pain points to silicon-level solutions.

When a PSU must run an interleaved PFC stage and an LLC stage, when an IBC must regulate a 48 V or high-voltage intermediate bus close to the load, or when a BBU must transition between charge, discharge, ORing, and protection states, PSOC™ Control C3 Performance Line microcontrollers (MCUs) provide a control architecture built for the timing, sensing, and compute requirements of modern data center power.

Top 3 control challenges in PSU, IBC, and BBU designs

1. Higher switching frequency compresses the entire control timeline

GaN and SiC power devices help designers increase power density by increasing the efficiency of the system or by enabling higher switching frequency and smaller magnetics. But higher switching frequency also compresses the time available for measurement, computation, PWM update, protection decisions, and communication with the rest of the system. In a high-frequency PSU or IBC, the controller cannot simply run a traditional sequential firmware loop and hope to keep up. The control path must become deterministic and closely coupled to the analog and PWM hardware.

This timing pressure is even more visible in interleaved and multi-level topologies. A three-phase or multi-phase PFC stage needs synchronized current sampling and phase-specific PWM updates. A multi-phase IBC needs current sharing, phase shedding, and fast transient correction. A BBU or Capacitor Bank Unit (CBU) converter needs bidirectional control while preserving safe operation during fast charge and discharge transitions. The higher the switching frequency, the less tolerance there is for interrupt jitter, bus contention, or firmware delays.

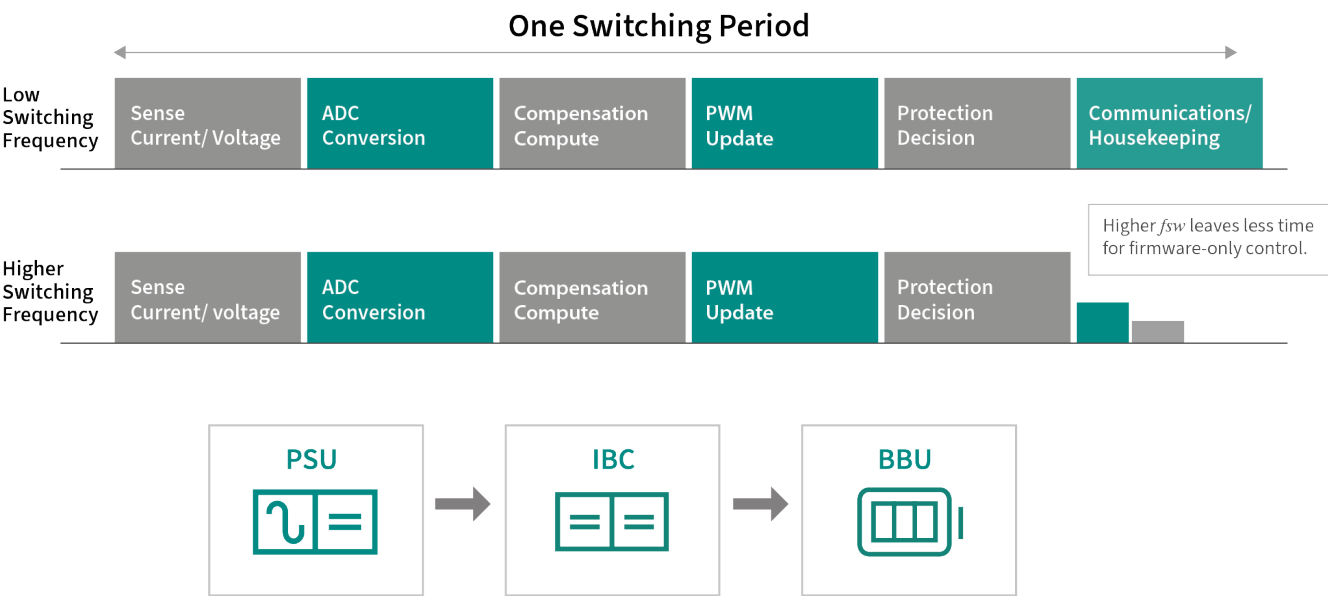


Figure 1:Higher switching frequency compresses the control timeline in PSUs, IBCs, and BBUs. Higher control-loop frequency requires faster sensing and lower-latency compute

2. Higher control-loop frequency requires faster sensing and lower-latency compute

Switching faster is not enough. All power stages must also regulate faster. Load profiles can move quickly as accelerators enter and exit high-compute states, and downstream voltage rails expect tight regulation. To support high control-loop frequency, the MCU must acquire voltage and current samples at the right instant, process compensation quickly, and update PWM edges before the next cycle. If the ADC, compute engine, and timer subsystem are not tightly synchronized, loop bandwidth is limited by controller latency rather than power-stage capability.

For PSUs, this affects PFC current loops, output-voltage loops, and resonant-stage control. For IBCs, it affects bus regulation close to high-current processors. For BBUs, it affects charge-current regulation, discharge-current control, and the transition between standby and ride-through modes. In each case, a controller optimized only for general embedded processing can become the bottleneck. The MCU must include dedicated real-time control resources that reduce software overhead and keep the loop path predictable.

3. Fast GaN switching increases sensitivity to timing, protection, and noise

GaN devices switch quickly, which is essential for efficiency and density, but fast edges also make the control system more sensitive to dead-time error, propagation delay, false trips, measurement noise, and layout-induced transients. The controller must therefore provide fine PWM edge control, fast fault detection, configurable blanking and filtering, and the ability to route events directly from sensing hardware to PWM action. Relying only on firmware response can be too slow for the protection timing required by high-frequency GaN-based stages. This is especially important in compact data center modules where power density, forced-air or liquid-cooling constraints, EMI limits, and high-current paths are tightly coupled. The controller must help designers shape switching behavior, sample at low-noise points, suppress spurious events, and still react immediately to real faults. A feature-rich digital power MCU is not only a compute device; it becomes part of the power-stage timing and protection strategy.

PSOC™ Control C3 Performance Line MCUs feature dive

PPCA: Real-time control partitioned away from housekeeping software

The Programmable Power Control Accelerator (PPCA) is the central feature that makes PSOC™ Control C3 Performance Line different from a general-purpose MCU. The device combines a main Arm® Cortex®-M33 CPU running up to 180 MHz with a PPCA subsystem that includes up to two additional Arm® Cortex®-M33 cores running up to 200 MHz. This enables time-critical control loops to run separately from communications, diagnostics, telemetry, state machines, firmware update tasks, and system supervision.

In a PSU, one PPCA core can focus on a high-speed current loop while another handles a voltage loop, phase management, or a second power stage. In a IBC, PPCA resources can be assigned to multi-phase current sharing and fast bus regulation. In a BBU, PPCA resources can support bidirectional control, charge/discharge modes, and protection-critical decisions without overloading the main Central Processing Unit (CPU). This partitioning helps preserve deterministic timing as switching frequency and loop frequency rise.

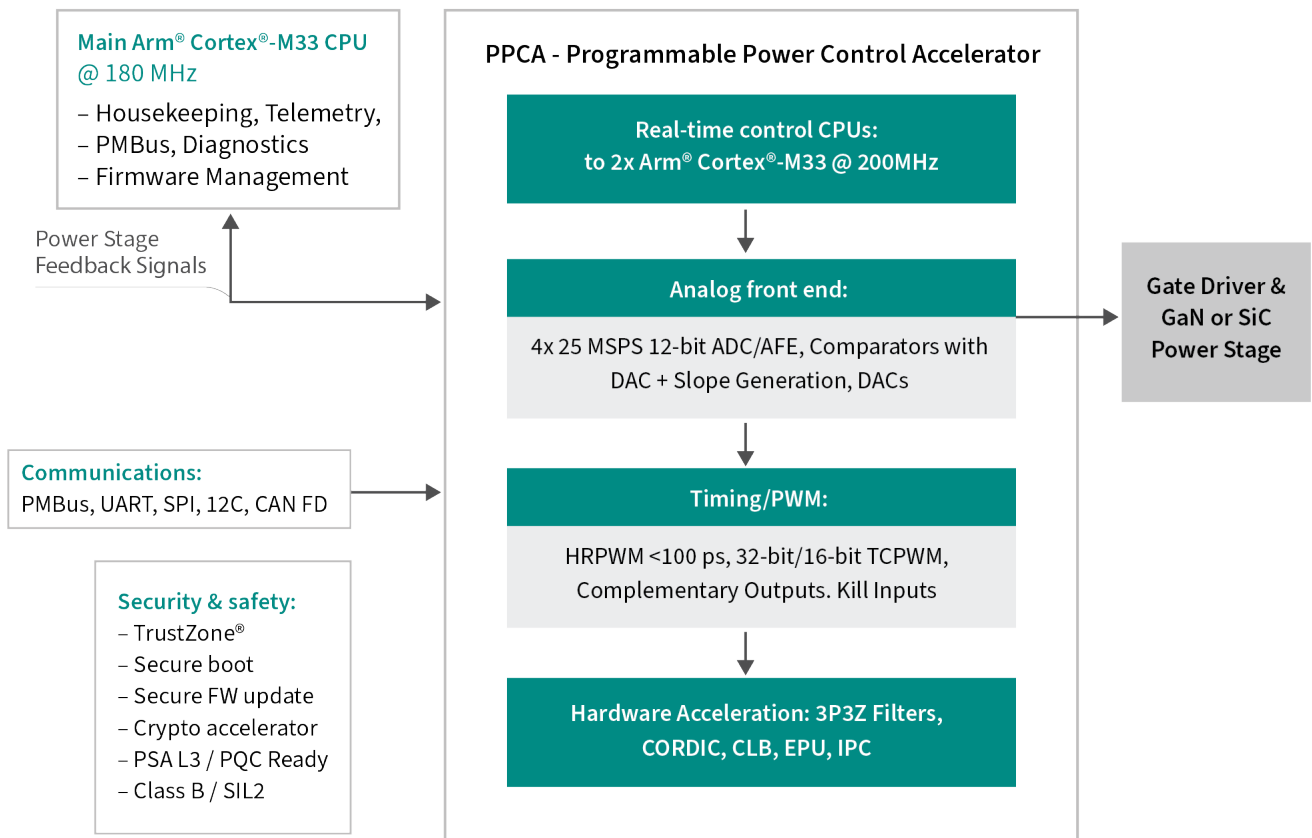


Figure 2: PSOC™ Control C3 Performance Line MCUs feature architecture for high-frequency digital power.

MSPS ADC subsystem: Sampling fast enough for high-frequency power conversion

PSOC™ Control C3 Performance Line MCUs integrates four 12-bit SAR ADC modules operating up to 25 MSPS with parallel sampling of up to 24 channels and oversampling capability on selected channels. This supports synchronized acquisition of phase currents, input voltage, output voltage, bus voltage, battery current, temperature, and auxiliary feedback signals. High sample rate is important because it allows designers to place measurements at the right point in the switching cycle rather than accepting noisy or delayed samples.

For GaN-based designs, this matters because switching transitions are fast and measurement windows can be narrow. In PSUs and IBCs, precise sampling improves current-loop stability, ripple cancellation, and phase balancing. In BBUs, it supports accurate charge and discharge control as well as fast detection of abnormal battery-side or bus-side conditions. The ADC subsystem is tightly connected to the real-time control architecture so that sensing does not become a bottleneck.

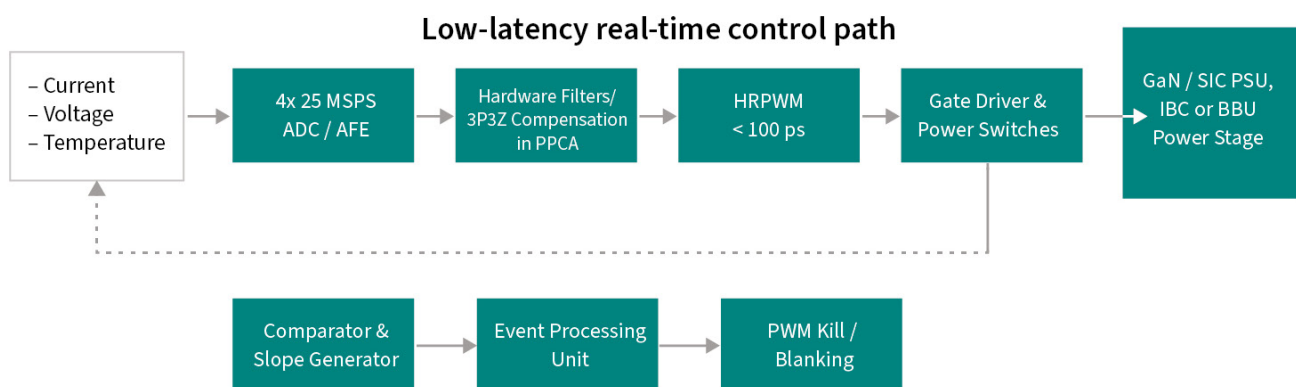


Figure 3: This diagram show low-latency, real-time control path from sensing to PWM update.
Sub-100 ps HRPWM: precise edge placement for GaN and multi-level power stages

High switching frequency places extreme demands on PWM resolution. Small timing errors can affect dead time, duty-cycle accuracy, zero-voltage switching windows, current ripple, and efficiency. PSOC™ Control C3 Performance Line MCUs include high-resolution PWM capability with sub-100 ps typical resolution for period, duty-cycle, and dead-time control, supported by 32-bit and 16-bit TCPWM resources, complementary outputs, synchronous operation, shadow updates, and kill inputs.

In PSU PFC stages, HRPWM enables fine phase and duty control across interleaved channels. In LLC, DAB, and other resonant or phase-shifted DC-DC stages, it helps control frequency, phase shift, and dead time precisely. In BBU converters, it supports efficient bidirectional switching and mode transitions.

For GaN stages, this level of timing resolution helps designers take advantage of fast switching while managing the timing sensitivity that comes with it.

Comparators, slope generators, EPU, and CLB: hardware-assisted protection and event control

Fast power stages need fast protection. PSOC™ Control C3 Performance Line includes differential comparators with slope generators, a configurable Event Processing Unit (EPU), and a Custom Logic Block (CLB). These resources allow the device to detect threshold events, apply blanking or filtering, combine or route events, and trigger PWM actions without waiting for a software interrupt path.

This is valuable when protecting GaN or SiC stages from overcurrent, short-circuit, shoot-through, reverse-current, or abnormal bus events. In PSUs, hardware event routing can support cycle-by-cycle protection and fault containment. In IBCs, it can support current sharing and rapid disconnect behavior. In BBUs, it can help manage ORing, hot-swap, inrush, and charge/discharge protection. The result is a system where protection timing is defined by hardware pathways rather than variable firmware latency.

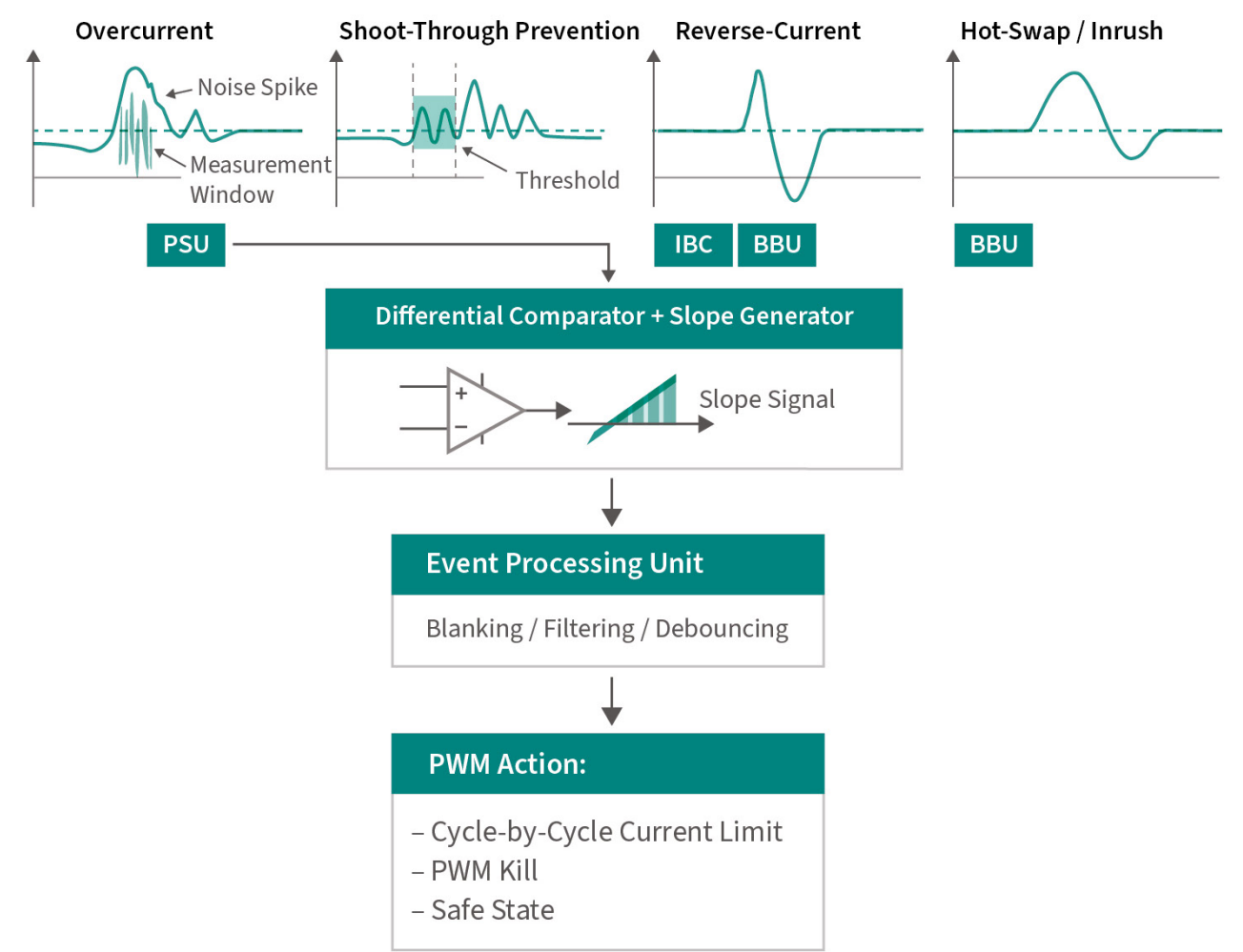


Figure 4: Hardware-assisted protection path for fast GaN switching events.
Hardware 3P3Z filters and CORDIC: Faster compensation with less CPU burden

High control-loop frequency increases the cost of every instruction in the control path. PSOC™ Control C3 Performance Line MCUs include two independent 3P3Z hardware filter blocks with six channels, as well as CORDIC accelerators for mathematical operations. These blocks help offload compensation and computation from the CPU, reducing loop latency and preserving compute bandwidth for application-level functions.

For PSU designers, hardware filters can support digital compensation in PFC and DC-DC loops. For IBC designers, they help sustain high-bandwidth regulation in multi-phase converters. For BBU designers, they support stable control across changing battery voltage, bus voltage, charge current, discharge current, and mode transitions. By accelerating repetitive control math, the MCU helps designers raise loop frequency without turning the firmware into a timing bottleneck.

Communications, safety, and security: Keeping high-speed power manageable in the system

High-frequency digital power still has to operate as part of a larger rack system. PSOC™ Control C3 Performance Line MCUs provide serial communication blocks for I2C, SPI, UART, and PMBus, including PMBus support up to 1 Mbps, plus CAN FD support up to 8 Mbps. This allows the same MCU platform to manage telemetry, configuration, event reporting, firmware updates, and module-level coordination in PSUs, IBCs, and BBUs.

The family also supports safety and security expectations for connected power infrastructure, including Class B and SIL 2 compliant safety libraries, Arm® TrustZone®, Secure Boot, secure firmware update, secure debug, cryptographic acceleration, true random number generation, protected memory features, PSA Level 3-certified security options, and Post-Quantum Cryptography (PQC) support.

These capabilities help designers maintain a secure and serviceable control platform while the PPCA and power-control peripherals handle the real-time workload. PQC support is especially important for long-life AI data center power infrastructure because PSUs, IBCs, and BBUs may remain deployed through multiple cryptographic transition cycles.

PSOC™ Control C3 Performance Line MCUs support PQC-oriented firmware protection through ML-DSA (Module-Lattice-Based Digital Signature Algorithm) digital signature standard defined by NIST in FIPS 204 from Infineon Edge Protect Bootloader to comply with PQC based FW Authentication and Hash-based signature approaches such as LMS/XMSS for secure boot and firmware updates, while also supporting hybrid security flows during the migration from classical public-key algorithms to post-quantum methods.

Together with hardware cryptographic acceleration, secure key management, secure storage, attestation, and DICE-ready support for SPDm-based device Secure Communication between PSU and BMC (Baseboard Management Controller) to support authenticating identity, collecting integrity measurements, and establishing encrypted communication sessions. These capabilities will enhance Datacenter PSUs for the reliable way to determine whether a device should be trusted, and what it is allowed to do, before granting access to keys, management interfaces, or control functions. PQC helps protect firmware authenticity and platform trust over the full lifecycle of connected power modules.

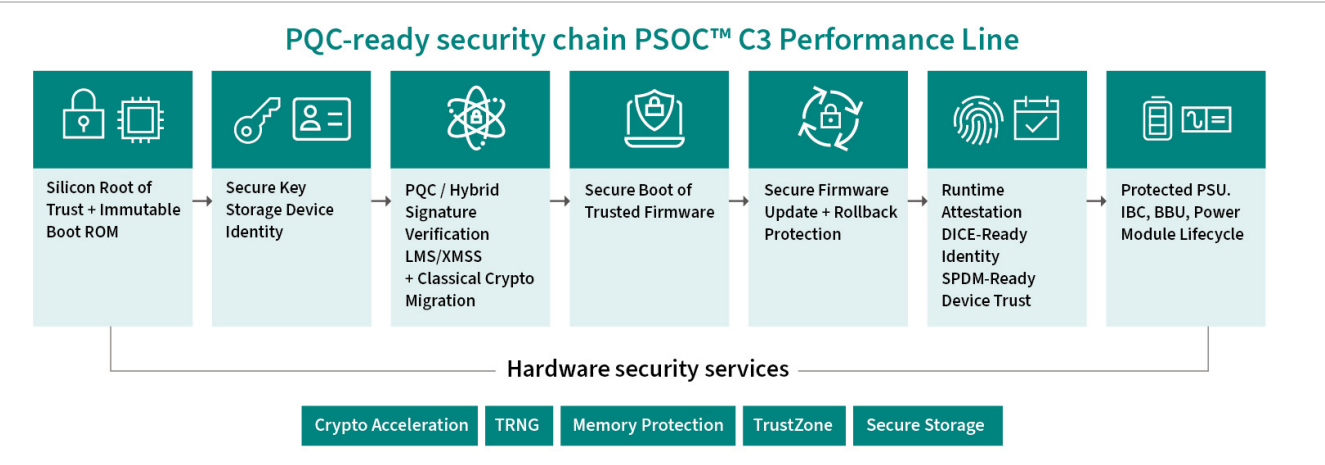


Figure 5: This diagram shows PQC-ready firmware protection for connected PSU, IBC, and BBU modules

4. PSOC Control C3 Performance Line Application Mapping

Power Supply Units: High-frequency PFC and DC-DC control

In AI server PSUs, PSOC™ Control C3 Performance Line MCUs are well suited for interleaved PFC, T-Type Vienna PFC, totem-pole PFC, LLC, and multi-phase DC-DC stages. The PPCA supports parallel real-time loops, the ADC subsystem captures synchronized voltage and current feedback, HRPWM provides fine timing control, and hardware events support fast protection. Together, these features help engineers increase switching frequency and control-loop frequency while keeping the design deterministic.

IBCs: tight regulation close to the load

IBCs must regulate intermediate rails with high efficiency, high density, and fast load response. PSOC™ Control C3 Performance Line supports multi-phase current sharing, high-frequency switching, synchronized sampling, precise PWM updates, and fast protection in compact DC-DC modules. These features are especially relevant for 48 V IBC designs and future high-voltage IBC designs where GaN-based switching and tight bus regulation can improve system efficiency and transient performance.

BBUs and CBUs: Bidirectional control, ride-through, and peak shaving

BBUs and CBUs add another dimension to digital power control because they must manage energy storage as well as conversion. PSOC™ Control C3 Performance Line MCUs can support bidirectional buck/boost, multi-level boost/buck, DAB, LLC, ORing, hot-swap, charge control, discharge control, and protection functions. Its fast ADCs, PPCA cores, HRPWM, comparators, EPU, and communications interfaces help manage transitions between charging, discharging, standby, and fault states.

For high-voltage BBU platforms, full digital control helps manage efficiency, thermal limits, current sharing, and battery protection while supporting the responsiveness needed for ride-through and peak-shaving events. The same feature set that benefits PSUs and IBCs—fast sensing, deterministic control, precise PWM, and hardware protection—also applies to the bidirectional and protection-heavy nature of BBU and CBU designs.

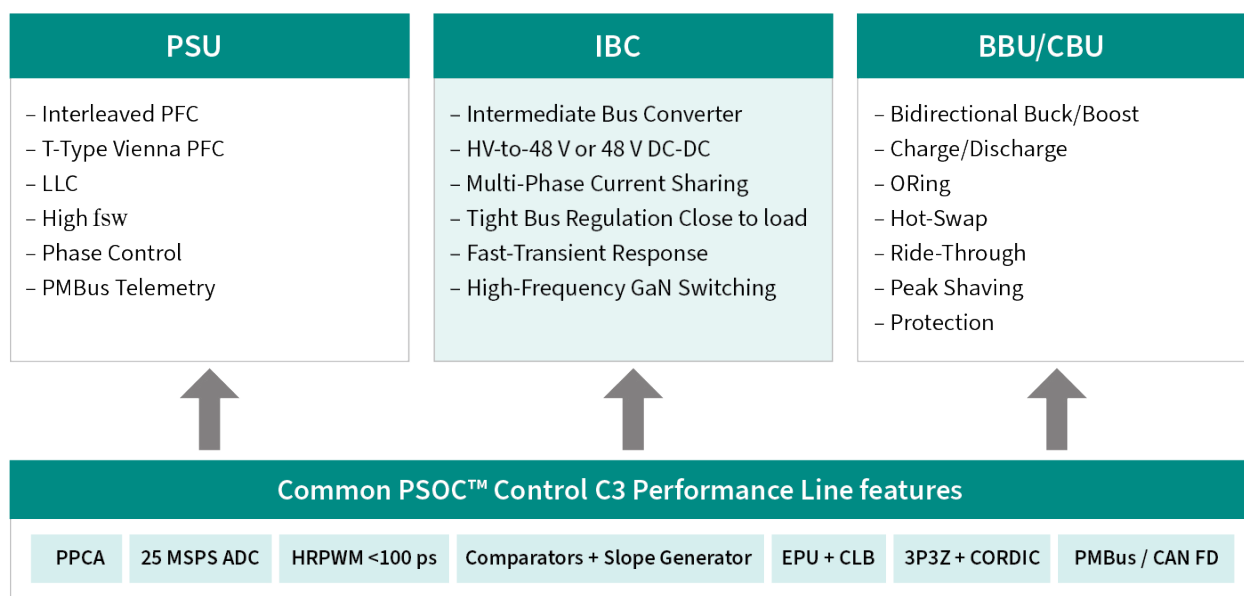


Figure 6: PSOC™ Control C3 Performance Line MCUs feature mapping across PSU, IBC, and BBU/CBU applications.

Summary

The next step in AI data center power innovation is not only about moving to new rack architectures or adopting wide-bandgap devices. It is about making those devices controllable at the switching and loop frequencies required by high-density PSUs, IBCs, and BBUs. Fast GaN switching creates opportunities for higher density and efficiency, but it also increases demands on sensing, timing, computation, and protection.

PSOC™ Control C3 Performance Line MCUs address these demands with a feature set purpose-built for digital power: PPCA real-time control cores, 25 MSPS ADCs, sub-100 ps HRPWM, comparators with slope generation, hardware filters, CORDIC, CLB, EPU, PMBus and CAN FD, safety libraries, and security. By combining these features in a scalable MCU platform, Infineon helps designers build power systems that switch faster, regulate faster, protect faster, and remain manageable across the full product lifecycle.

Additional Resources

Empowering AI Power Supply Innovation with PSOC™ Control C3 Performance Line

- [PSOC™ Control C3 Performance Line datasheet](#)
- [PSOC™ Control C3 Performance Line NPI longform presentation](#)
- [Designing a 30kW 3-Phase Interleaved Type Vienna PFC for AI Server Power Supply whitepaper](#)
- [Infineon BBU and CBU application material for AI data centers](#)
- [ModusToolbox™ software with Power Suite](#)
- [ModusToolbox™ software with Power Suite PSOC™ Control C3M8 evaluation kit \(KIT_PSC3M8_EVK\)](#)
- [PSOC™ Control low-voltage LLC development expansion kit \(KIT_PSC3_LLC1\)](#)
- [Countering security threats of quantum attacks with PSOC™ Control microcontrollers](#)

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