TR1273: MIPI RFFE Device I/O Structures

IFX RF Switches and Antenna Tuners

About this document

Scope and purpose

This technical report provides application guideline when UE Baseband or RF Transceiver MIPI Master with undefined MIPI RFFE I/O driver impedance is used. Spatial cosideration has to be taken to control Infineon's latest MIPI RFFE switches and antenna tuners designs supporting multiple default USID addresses via SDATA and SCLK lines swapping when using this type of MIPI Master.

All MIPI-RFFE relavant data referring to the following source:
"Specification for RF Front-End Control Interface", Version 2.1 - 18 December 2017

Intended audience

This technical report is intended to support development engineers to implement MIPI RFFE devices into UE applications.

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1 MIPI RFFE I/O structures

This section describes the MIPI RFFE standard for the input and output signals of the MIPI RFFE bus.

Main focus is the implementation of the SDATA and SCLK interfaces of the MIPI RFFE bus in to the UE application using the latest transceiver models.

1.1 MIPI RFFE 2.1 specification for I/O structures

In the following pictures the stuctures for SCLK and SDATA line are shown. Both structures (*section 5.1 in the MIPPI RFFE specification*) require a dedicated pull down resistor at master side. It is possible to have it implemented indide the master device or outside at the SDATA or SCLK line.

Clear statement in the MIPI Specification 2.1, Section 5.1:

“Internal pull-downs shall be **implemented only on RFFE master devices**, and shall only be enabled on the current BOM, or under its control if located externally or in another Master.”

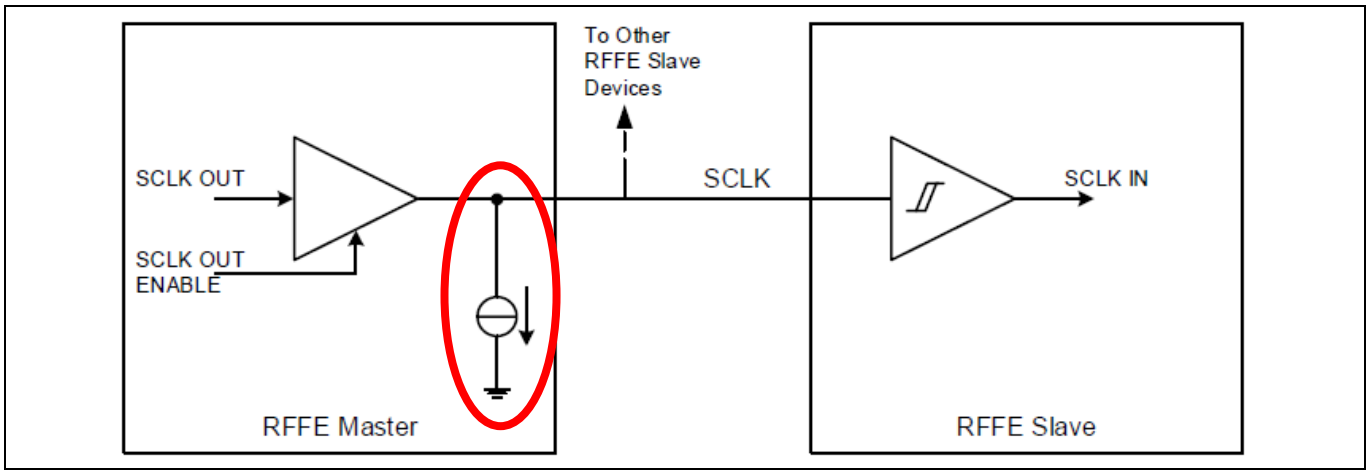

Figure 1 SCLK master and slave I/O cells

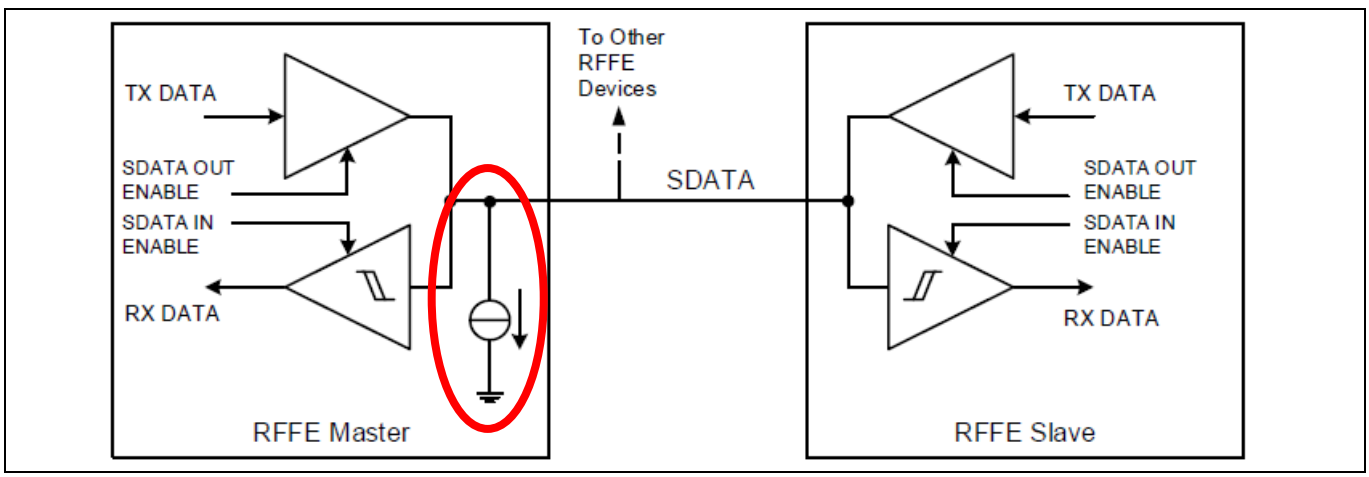

Figure 2 SDATA master and slave I/O cells

Depending on the number of slaves on the MIPI RFFE bus, the pull-down Resistance should be in the range of 20 – 200 kΩ, referring to figure 3.

Master Scenario	SCLK Pull-Down Value, $R_{effective}$	SDATA Pull-Down Value, $R_{effective}$	Units
	Typical	Typical	
Single-Master/Multi-Master (Static)[1]	20 – 200	20 – 200	kΩ
Multi-Master (Dynamic)[1,2]	10 – 100	10 – 100	kΩ

Figure 3 RFFE pull-down device requirements

1.2 Application environment of standard MIPI slaves and the latest master

The RF transceiver's which does not provide proper MIPI RFFE I/O interface impedances can cause floating impedances for SDATA and SCLK lines. These floting impedances may casue communicataion error between master and slave. For such a combination of master and slave, application circuit must fix the issue as it is not allowed to have a pull down in the Slave IC.

The MIPI specification describes a workaround by implementing separate external pull downs if the Master IC has no internal pull downs. These pull downs (e.g. 100kOhm) allowing a stable low level of the SDATA and SCLK line if no communication is ongoing.

For Infineon's MIPI RFFE switches and antenna tuners requires pull down registor at the SDATA line for correct communication between master and slave. The SCLK logic level should be kept low after VIO is high until the first SSC in the SDATA. If the SCLK logic can be guaranteed for this time then the pull down registor is not needed.

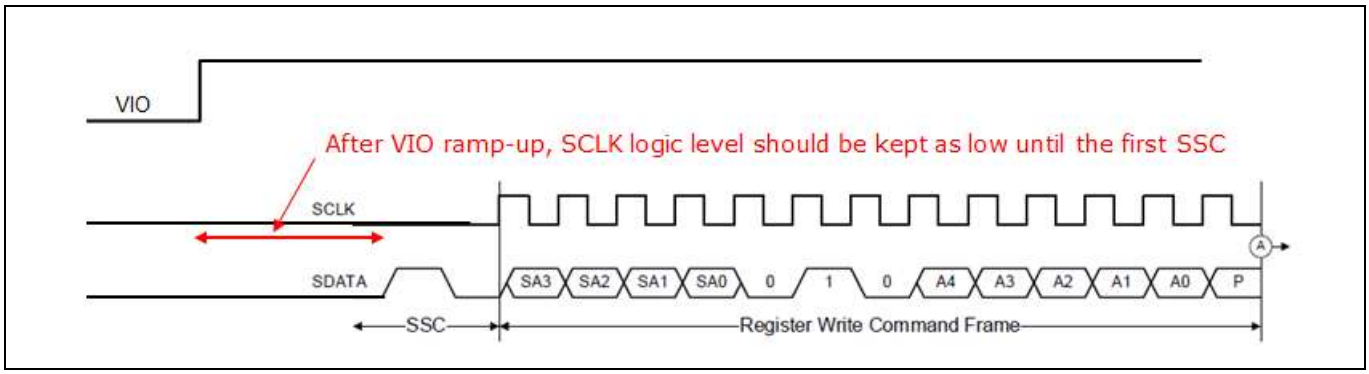

Figure 4 MIPI RFFE timing diagramm

For Infineon's RF devices featured by the SCLK/SDATA swap function to expand the selectable default USID addresses, a clean SCLK line is very important to have the right USID and get a proper communication done. This "clean" SCLK can only be reached by a pull-down in the bus of the SCLK. This has to be provided by the Master or has to be implemented with an external component.

If no pull –down and there is an unexpected signal at SCLK line higher then the threshold high level, the device would swap the SCLK and SDATA behavior (because this would be seen as a SSC on SCLK line and swap to SDATA line). This ends in a different USID of the device and no communication could be started.

In case the master can not provide a pull-down solution, a pull down according to figure 3 (e.g. 100kOhm) can be added at the SCLK line of our MIPI RFFE decices as shown in Figure 5.

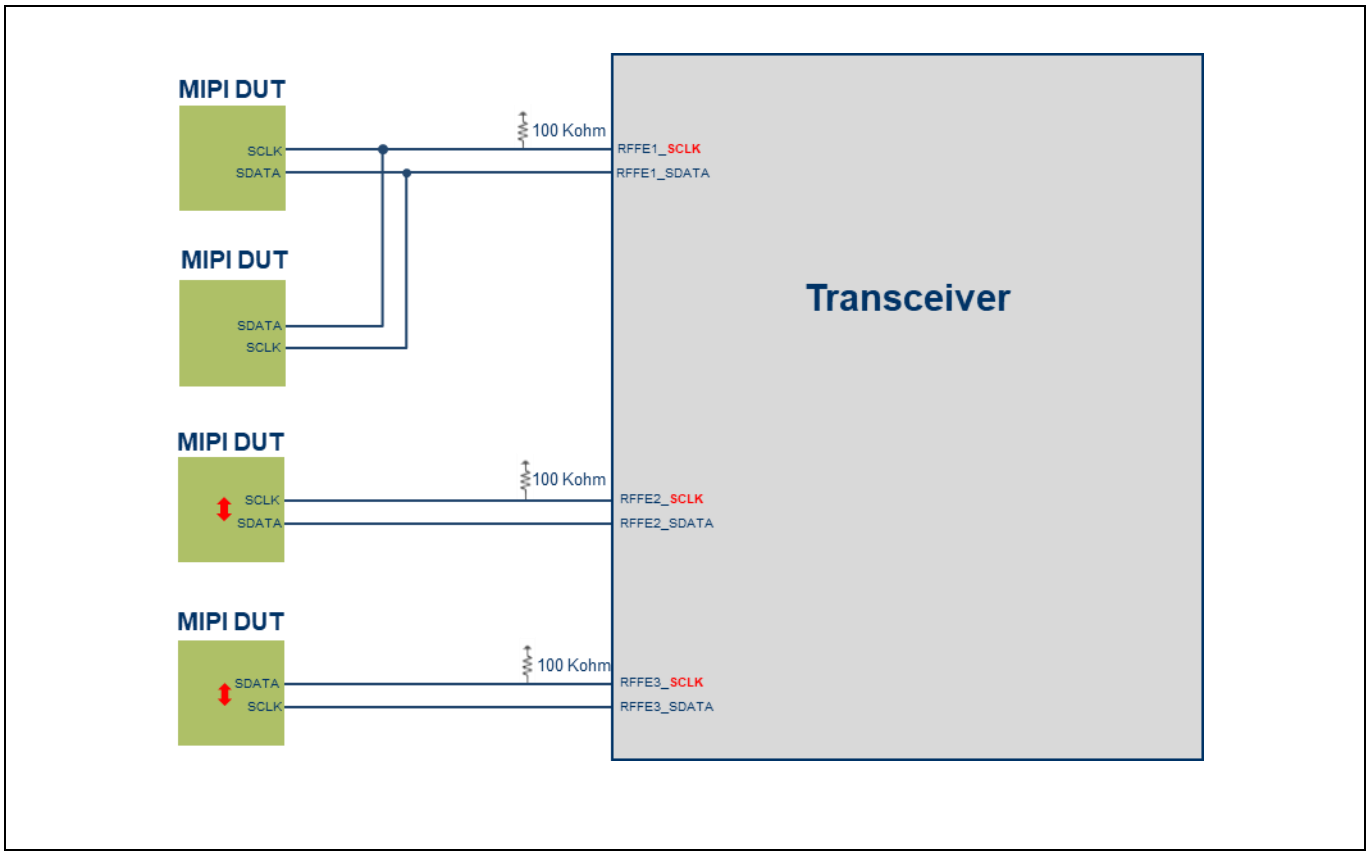

Figure 5 Application environment to secure MIPI RFFE communication

2 SCLK / SDATA swap feature to expand MIPI RFFE USIDs

Infineon's SWAP SCLK/SDATA Feature allows to increase the number of possible hardware enabled USID's by factor 2. That means the device itself provides minimum 2 USID's by swapping SCLK and SDATA. This results in an easy way to use 2 identical slave devices from Infineon without any Software change on baseband side to program a different USID.

Figure 6 below shows the swap feature in a graphical way.

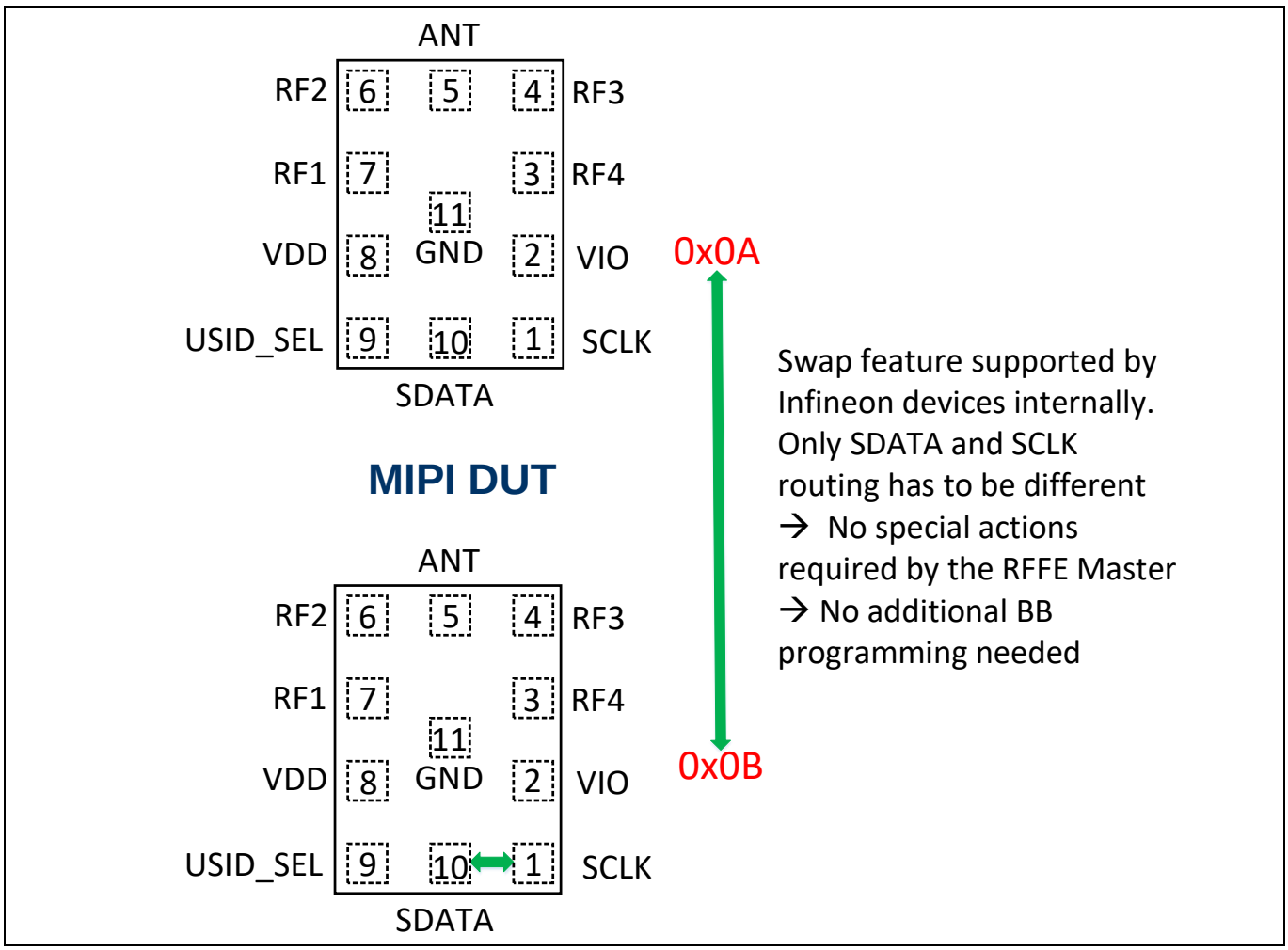

Figure 6 Infineon's MIPI RFFE SDATS/SCLK swap feature to multible possible USID's

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Major changes since the last revision

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