Single Event Effect Test Report on Infineon Rad-Hard MOSFETs
*****BUY06CS family*****

Dr. Tudor Chirila	PMM RFS D HIR	
Dietmar Schwertberger	PMM RFS D HIR	
Dr. Bernd Eisener	PMM RFS D HIR	

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§1 SCOPE

This test report describes Single Event Effect (SEE) tests and results for radiation hardened MOSFETs from Infineon for device types BUY06CS, in accordance to ESCC Basic Specification 25100.

In total two (2) different chip sizes of the same wafer technology numbered #1 and #2 have been tested with 124Xe and 208Pb ions of LET and penetration as given in table 1. Concurrently, TID hardness tests were performed for the same device designs issued from the same wafer lots, see separated report.

Tests have been performed at the facilities CYCLONE at Louvain-la-Neuve, Belgium (Tests L15, L17) and SPIRAL of Grand Accélérateur National d'Ions Lourds (GANIL), Caen, France (Test SEE2).

Run	Location	Ion	Chip size	Degrader	Air [mm]	LET [MeVcm^2/mg]	Range [µm]
L15	Louvain	$^{124}Xe^{35+}$	#1	---	---	62.5	73.1
L17	Louvain	$^{124}Xe^{35+}$	#1	---	---	62.5	73.1
SEE2	GANIL	$^{208}Pb^{56+}$	#2	Al 100µm	150	95.7	86.7

Table 1: Overview of SEE Tests for BUY06CS chip size #1,2 and beam characteristics (LET and ion penetration depths) for Xe and Pb ions for sources CYCLONE (Louvain) and SPIRAL (GANIL).

§2 DEVICE INFORMATION

Chip size	**Part Type**	**BVdss [V]**	**Vgs(th) [V]**	**Rds(on) [mOhm]**	**Idmax [A]**
#1	BUY06CS23K	60	2.0 – 4.0	40	23 (RT)
	BUY06CS35J			35	35 (RT)
#2	BUY06CS80A	60	2.0 – 4.0	6.5	80 (RT)

§2.1 APPLICABLE DOCUMENTS

- BUY06CS ESCC Draft Detail Specification for HiRel RadHard Power-MOS 60V family, Version October 2018.
- ESCC Basic Specification 25100

§2.2 DEVICES MARKINGS AND SAMPLE PREPARATION

In order to contact devices with the TO test sockets on bias boards, chips have been soldered and bonded to respective 3-pin PCB-TO-adapter boards to connect Gate/Drain/Source contacts of the MOSFETs.

Devices' numbers are written on the PCB with a permanent marker. The number correlates in the sample list to the lot and wafer number.

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§2.3 PARAMETER MEASUREMENTS

Test samples have passed on-wafer tests, notably BVDSS, Vgs(th), RDSON, IDSS, IGSS with their parameters within predetermined upper/lower limits.

Parameter measurements have been performed on adapter-mounted devices to check that devices have not been degraded. Specifically, IDSS(60V), IGSS(+/-20V), RDSON(15/60A, Ugs=10V), VSD(23/80 A), Vgs(th)(1 mA), BVDSS(0.25 mA) are determined.

§3 TEST SET-UP

§3.1 TEST BOARD

The test board was designed to accommodate up to 10 test samples, each consisting of an individual bias circuit (fig. 1). This test board (fig. 2) was fixed to the mechanical positioning stage provided at the Louvain/GANIL beam line. All voltages UDS and UGS were provided via a flat band cable from a switch board. The oscilloscope output was left unconnected.

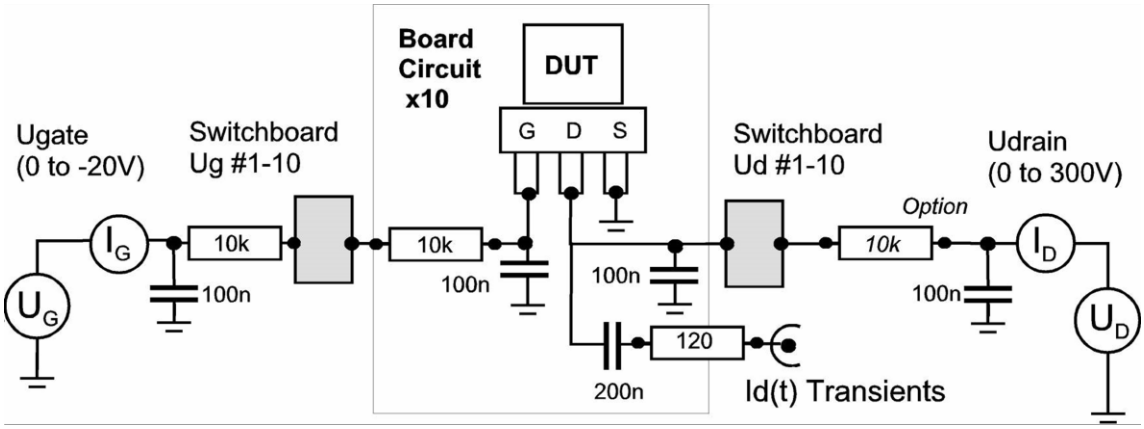

Fig. 1: Test circuit for SEB/SEGR test.

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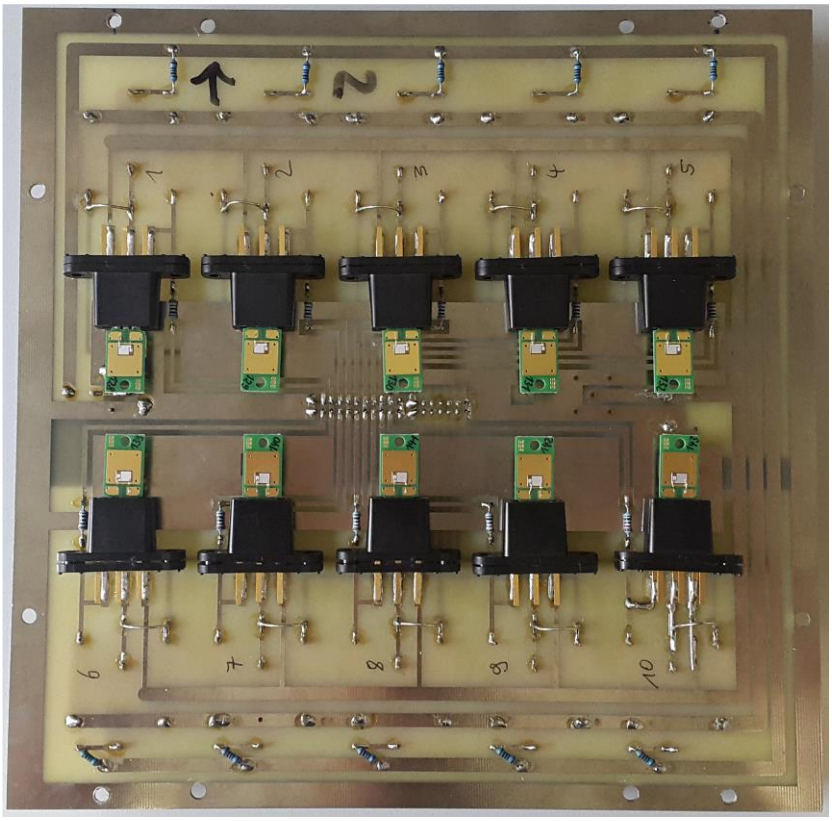

Fig. 2: Test-Board with 10 positions with TO test sockets. Separate bias of UDS and UGS for each device. Flat-band connector on back side.

§3.2 MEASUREMENT EQUIPMENT

As a voltage source for UDS and for ID current measurements a Keithley 237 High Voltage Measurement Unit has been employed. Gate voltage UGS and measurement of IG are provided by a Keithley 236 Source Measure Unit.

Voltages were set manually as were all recordings of run number, time, sample number, all current readings, specifically PIGS currents, are logged. The irradiation report provided by GANIL operators, in addition, give fluence values for each test run.

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§4 HEAVY ION IRRADIATION FACILITIES

§4.1 BEAM PARAMETERS

CYCLONE at UCL Louvain-la-Neuve is a cyclotron capable of providing a “cocktail” of heavy ions with about the same M/Q ratio. From a HIF cocktail 124Xe (35+ charge state) are selected with an energy of 995 MeV yielding the characteristics in Table 2. CYCLONE source was employed in irradiation run L15 and L17.

SPIRAL at GANIL Caen is a cyclotron capable of providing heavy ions of very high energy, in the order 28MeV/u, i.e. 6 GeV per ion for 208Xe (56+ charge state) employed in irradiation run SEE2.

Parameters were chosen to provide the highest possible LET for a given minimum of penetration depth about 70 µm, determined by the thickness of the – active – epitaxial layer of the MOSFETs (less than 35µm including top metallization and imide), see table 1.

§4.2 TESTING POSITION AND TEST BOARD MOUNTING

At CYCLONE test boards are mounted within a vacuum chamber with feedthroughs for electrical bias and signals. The ion beam is positioned on the device under test.

At GANIL irradiation is performed in air. The test board is screwed onto a motorized positioning frame (fig. 3). The beam exit of the vacuum tube has a 10 µm stainless steel window. Beam size is 200 mm (horizontal) and 50 mm (vertical). With the bias board as in fig. 2, all devices are irradiated simultaneously and further device positioning is usually not necessary. To achieve the desired LET/penetration, aluminium foil degraders and adjusted air distances are used.

In both facilities, ion incidence was chosen to be 0°, i.e., vertical incidence.

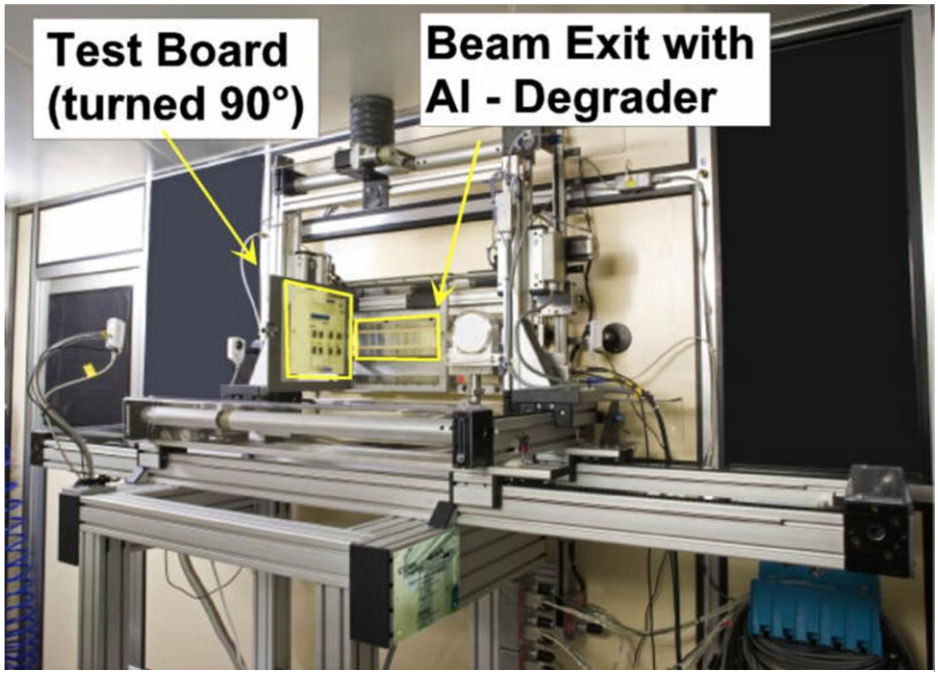

Fig. 3: Test Board positioning at GANIL beam line exit window

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§4.3 DOSIMETRY

Control of beam homogeneity and dosimetry as well as beam operation is the responsibility of ion beam providers. An irradiation log provided by GANIL gives actual flux values for each test run, including fluence-to-fail, if applicable.

§5 TEST SEQUENCE

§5.1 BEAM PARAMETERS AND TEST CRITERIA FOR ALL TESTS

- LET see Table 1
- Flux 3E+3 ions/cm^2/s
- Fluence 3E+5 ions/cm^2
- Normal incidence of ion beam
- Destructive mode. FAIL current criteria: IDS>2 µA or IGS>100 nA.
- Required number of test samples per test case: 1(for FAIL)/3(for PASS)
- Post Irradiation Gate Stress (PIGS) test at any UDS (at respective UDS, UGS down to -25V, in steps of -5V). FAIL criterion: either IDS or IGS>100nA

§5.2 TEST BIAS SEQUENCE FOR SEB-SOA

Test sequence for Single Event Breakdown (SEB-SOA):

UGS: 0 V
UDS: Start at 60V (or UDS,max). If *FAIL* occurs UDS is stepped-down by 5V until *PASS*.

§5.3 TEST BIAS SEQUENCE FOR SEGR-SOA

Test sequence for Single Event Gate Rupture (SEGR-SOA):

UGS: negative, starting at -15 V, steps of -5 V. For UGS at the edge of the SOA curve, smaller steps (-2,-3V) have been tested as well.

UDS: Start at maximum UDS at which PASS value was obtained for previous UGS-test sequence (or UGS=0V). If FAIL occurs UDS is stepped-down by 5V until PASS.

The combination of SEB-SOA and SEGR-SOA yields the Single Event Effect (SEE)-SOA.

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§6 TEST RESULTS

Devices of type BUY06CS in two chip sizes numbered #1,2 has been tested and maximum SEE-SOA for UDS/(negative)UGS combinations established.

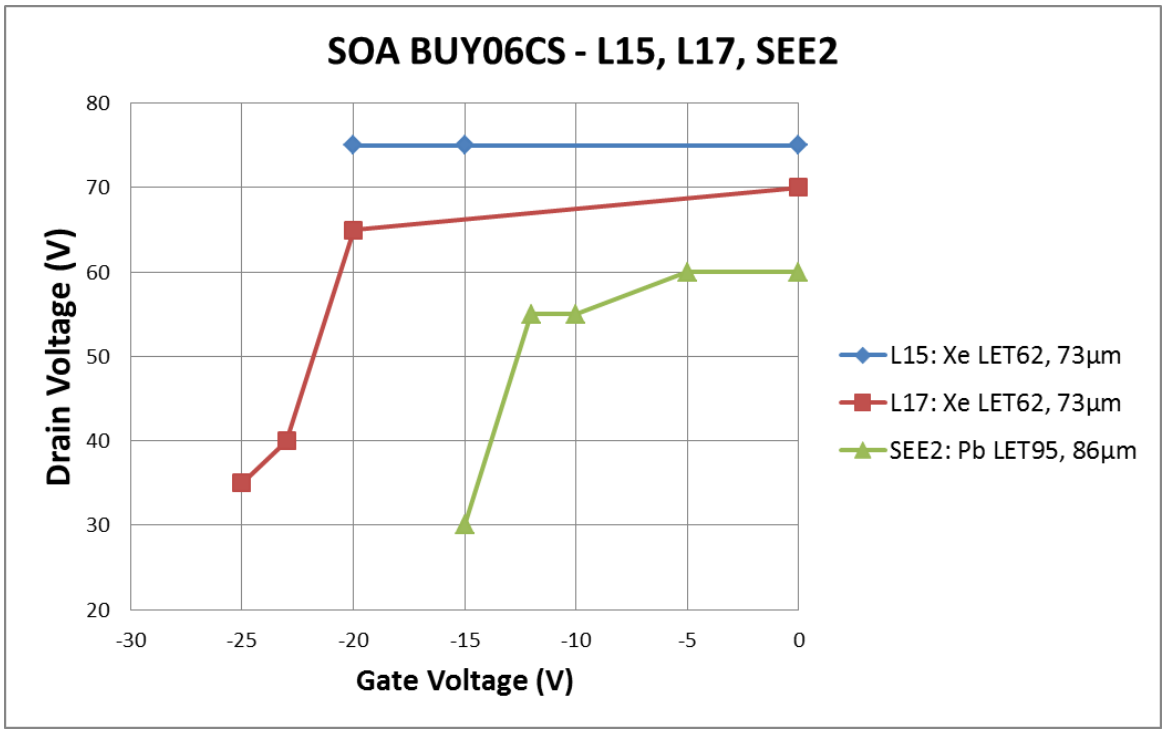

Fig. 5: Maximum SEE-SOA of BUY06CS as determined at test L15, L17 (CYCLONE) and SEE2 (GANIL) with Xe and Pb ions respectively.

§7 CONCLUSION

A series of SEE tests for two chips sizes of BUY06CS family MOSFETs have been performed.

Ion source CYCLONE (Louvain) with elevated LET and Xe ion penetration of 73 µm yielded a SOA in which the drain voltage exceeded the rated UDS (60V) up to UGS = -20V.

Ion source GANIL with high LET and Pb ion penetration range shows that the tested wafer technology is radiation hard even in extreme application conditions.

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§8 DETAILS OF TEST RUNS

Details of individual test runs L15, L17 and SEE2 are tabulated in this section.

test	*Board Pos*	*Test no.*	*chip*	*Flux (i/cm2/sec)*	*Fluence (/cm²)*	*Vds test(V)*	*Vgs test (V)*	*PIGS*	*COMMENTS*
no.5	6	1	49	3000	3.0E+05	60	0	ok	
		2				70	0	ok	
		3				75	0	ok	
		4				75	-15	ok	
		5				50	-20	ok	
		6				60	-20	ok	
		7				70	-20	ok	
		8				75	-20	ok	
		9				30	-25	ok	
		10				40	-25	fail	
	7	1	50			75	0	ok	
		2				75	-15	ok	
		3				60	-20	ok	
		4				70	-20	ok	
		5				75	-20	ok	
		6				30	-25	ok	
		7				35	-25	ok	
	8	1	51			75	0	ok	
		2				75	-15	ok	
		3				75	-20	ok	
		4				35	-25	fail	

Tab. 2: Test L15 – Wafer VE712018#17 – size #1.

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test	Board Pos	Test no.	chip	Flux (i/cm2/sec)	Fluence (/cm²)	Vds test(V)	Vgs test (V)	PIGS	COMMENTS
no.1	**1**	1	1	3000	3.0E+05	60	0	ok	
		2				60	-15	ok	
		3				60	-20	ok	
		4				30	-25	ok	
		5				40	-25	fail	80 sec
	2	1	2			60	0	ok	
		2				60	-20	ok	
		3				30	-25	ok	
		4				35	-25	ok	Functional
	3	1	3			60	0	ok	
		2				60	-20	ok	
		3				30	-25	ok	
		4				35	-25	ok	Functional
	4	1	4			30	-25	ok	
		2				35	-25	ok	Functional
	1	1	6			70	0	ok	
		2				70	-20	ok	
		3				38	-25	ok	
		4				50	-23	ok	
		5				60	-23	fail	10 sec
	2	1	7			70	0	ok	
		2				70	-20	ok	
		3				50	-23	fail	20 sec
	3	1	8			70	0	ok	
		2				70	-20	fail	90 sec
	4	1	9			65	-20	ok	
		2				38	-25	fail	90 sec
	5	1	10			65	-20	ok	
		2				40	-23	ok	
		3				45	-23	ok	Functional
	6	1	11			65	-20	ok	
		2				40	-23	ok	
		3				45	-23	fail	95 sec
	7	1	12			40	-23	ok	Functional

Tab. 3: Test L17 – Wafer VE737633#3 – size #1.

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test	Board Pos	Test no.	chip	Flux (i/cm2/sec)	Fluence (/cm²)	Vds test(V)	Vgs test (V)	PIGS	COMMENTS
no.2	6	1	25	3000	3.0E+05	60	0	ok	
		2				60	-5	ok	
		3				60	-15	fail	~12000 i
	7	1	26			60	0	ok	
		2				60	-5	ok	
		3				60	-10	ok	
		4				30	-15	ok	
		5				40	-15	fail	~20000 i
	8	1	27			60	0	ok	
		2				60	-5	ok	
		3				60	-10	PIGS fail	VG = -25V
	9	1	28			55	-10	ok	
		2				30	-15	ok	
		3				35	-15	fail	~183000 i
	10	1	29			55	-10	ok	
		2				30	-15	ok	Functional
	10	1	31			55	-10	ok	Functional
	1	1	32			35	-12	ok	
		2				40	-12	ok	
		3				45	-12	ok	
		4				50	-12	ok	
		5				52	-12	ok	
		6				55	-12	ok	
		7				60	-12	ok	Functional
	2	1	33			55	-12	ok	
		2				60	-12	PIGS fail	VG = -25V
	3	1	34			55	-12	ok	Functional

Tab. 4: Test SEE2 – Wafer VE751933#1 – size #2.

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