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PSoC 4000 Family

PSoC 4 Registers Technical Reference Manual (TRM)

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Register Mapping

The Register Mapping section discusses the registers of the PSoC 4 device. It lists all the registers in mapping tables, in address order. For Architecture details, see PSoC 4000 Family: PSoC 4 Architecture Technical Reference Manual (TRM).

Register General Conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Example	Description
'x' in a register name	ACBxxCR1	Multiple instances/address ranges of the same register
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
WOC	WOC:0	Write one to clear
WZC	WZC:0	Write zero to clear
RC	RC:0	Read to clear
WC	WC:0	Write to clear
NA	NA:000	Reserved
U	R:U	Undefined
00	RW : 00	Reset value is 0x00
XX	RW : XX	Register is not reset
Empty, grayed out table cell		Reserved bit or group of bits, unless otherwise stated. Write reserved bits to zero. Software cannot make any assumptions about return values.

1 CM0 Registers

This section discusses the CM0 registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

1.1 CM0 Register Details

Register	Address	Description
CM0_DWT_PID4	0xE0001FD0	Watchpoint Unit CoreSight ROM Table Peripheral ID #4
CM0_DWT_PID0	0xE0001FE0	Watchpoint Unit CoreSight ROM Table Peripheral ID #0
CM0_DWT_PID1	0xE0001FE4	Watchpoint Unit CoreSight ROM Table Peripheral ID #1
CM0_DWT_PID2	0xE0001FE8	Watchpoint Unit CoreSight ROM Table Peripheral ID #2
CM0_DWT_PID3	0xE0001FEC	Watchpoint Unit CoreSight ROM Table Peripheral ID #3
CM0_DWT_CID0	0xE0001FF0	Watchpoint Unit CoreSight ROM Table Component ID #0
CM0_DWT_CID1	0xE0001FF4	Watchpoint Unit CoreSight ROM Table Component ID #1
CM0_DWT_CID2	0xE0001FF8	Watchpoint Unit CoreSight ROM Table Component ID #2
CM0_DWT_CID3	0xE0001FFC	Watchpoint Unit CoreSight ROM Table Component ID #3
CM0_BP_PID4	0xE0002FD0	Breakpoint Unit CoreSight ROM Table Peripheral ID #4
CM0_BP_PID0	0xE0002FE0	Breakpoint Unit CoreSight ROM Table Peripheral ID #0
CM0_BP_PID1	0xE0002FE4	Breakpoint Unit CoreSight ROM Table Peripheral ID #1
CM0_BP_PID2	0xE0002FE8	Breakpoint Unit CoreSight ROM Table Peripheral ID #2
CM0_BP_PID3	0xE0002FEC	Breakpoint Unit CoreSight ROM Table Peripheral ID #3
CM0_BP_CID0	0xE0002FF0	Breakpoint Unit CoreSight ROM Table Component ID #0
CM0_BP_CID1	0xE0002FF4	Breakpoint Unit CoreSight ROM Table Component ID #1
CM0_BP_CID2	0xE0002FF8	Breakpoint Unit CoreSight ROM Table Component ID #2
CM0_BP_CID3	0xE0002FFC	Breakpoint Unit CoreSight ROM Table Component ID #3
CM0_SYST_CSR	0xE000E010	SysTick Control & Status
CM0_SYST_RVR	0xE000E014	SysTick Reload Value
CM0_SYST_CVR	0xE000E018	SysTick Current Value
CM0_SYST_CALIB	0xE000E01C	SysTick Calibration Value
CM0_ISER	0xE000E100	Interrupt Set-Enable Register
CM0_ICER	0xE000E180	Interrupt Clear Enable Register
CM0_ISPR	0xE000E200	Interrupt Set-Pending Register
CM0_ICPR	0xE000E280	Interrupt Clear-Pending Register
CM0_IPR0	0xE000E400	Interrupt Priority Registers
CM0_IPR1	0xE000E404	Interrupt Priority Registers. See CM0_IPR0 for the details of bit fields.

Register	Address	Description
CM0_IPR2	0xE000E408	Interrupt Priority Registers. See CM0_IPR0 for the details of bit fields.
CM0_IPR3	0xE000E40C	Interrupt Priority Registers. See CM0_IPR0 for the details of bit fields.
CM0_IPR4	0xE000E410	Interrupt Priority Registers. See CM0_IPR0 for the details of bit fields.
CM0_IPR5	0xE000E414	Interrupt Priority Registers. See CM0_IPR0 for the details of bit fields.
CM0_IPR6	0xE000E418	Interrupt Priority Registers. See CM0_IPR0 for the details of bit fields.
CM0_IPR7	0xE000E41C	Interrupt Priority Registers. See CM0_IPR0 for the details of bit fields.
CM0_CPUID	0xE000ED00	CPUID Register
CM0_ICSR	0xE000ED04	Interrupt Control State Register
CM0_AIRCR	0xE000ED0C	Application Interrupt and Reset Control Register
CM0_SCR	0xE000ED10	System Control Register
CM0_CCR	0xE000ED14	Configuration and Control Register
CM0_SHPR2	0xE000ED1C	System Handler Priority Register 2
CM0_SHPR3	0xE000ED20	System Handler Priority Register 3
CM0_SHCSR	0xE000ED24	System Handler Control and State Register
CM0_SCS_PID4	0xE000EFD0	System Control Space ROM Table Peripheral ID #4
CM0_SCS_PID0	0xE000EFE0	System Control Space ROM Table Peripheral ID #0
CM0_SCS_PID1	0xE000EFE4	System Control Space ROM Table Peripheral ID #1
CM0_SCS_PID2	0xE000EFE8	System Control Space ROM Table Peripheral ID #2
CM0_SCS_PID3	0xE000EFEC	System Control Space ROM Table Peripheral ID #3
CM0_SCS_CID0	0xE000EFF0	System Control Space ROM Table Component ID #0
CM0_SCS_CID1	0xE000EFF4	System Control Space ROM Table Component ID #1
CM0_SCS_CID2	0xE000EFF8	System Control Space ROM Table Component ID #2
CM0_SCS_CID3	0xE000EFFC	System Control Space ROM Table Component ID #3
CM0_ROM_SCS	0xE00FF000	CM0 CoreSight ROM Table Peripheral #0
CM0_ROM_DWT	0xE00FF004	CM0 CoreSight ROM Table Peripheral #1
CM0_ROM_BPU	0xE00FF008	CM0 CoreSight ROM Table Peripheral #2
CM0_ROM_END	0xE00FF00C	CM0 CoreSight ROM Table End Marker
CM0_ROM_CSMT	0xE00FFFCC	CM0 CoreSight ROM Table Memory Type
CM0_ROM_PID4	0xE00FFFD0	CM0 CoreSight ROM Table Peripheral ID #4
CM0_ROM_PID0	0xE00FFFE0	CM0 CoreSight ROM Table Peripheral ID #0
CM0_ROM_PID1	0xE00FFFE4	CM0 CoreSight ROM Table Peripheral ID #1
CM0_ROM_PID2	0xE00FFFE8	CM0 CoreSight ROM Table Peripheral ID #2
CM0_ROM_PID3	0xE00FFFEC	CM0 CoreSight ROM Table Peripheral ID #3
CM0_ROM_CID0	0xE00FFFF0	CM0 CoreSight ROM Table Component ID #0
CM0_ROM_CID1	0xE00FFFF4	CM0 CoreSight ROM Table Component ID #1
CM0_ROM_CID2	0xE00FFFF8	CM0 CoreSight ROM Table Component ID #2
CM0_ROM_CID3	0xE00FFFFC	CM0 CoreSight ROM Table Component ID #3

1.1.1 CM0_DWT_PID4

Watchpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0001FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

1.1.2 CM0_DWT_PID0

Watchpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0001FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 10

1.1.3 CM0_DWT_PID1

Watchpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0001FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

1.1.4 CM0_DWT_PID2

Watchpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0001FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

1.1.5 CM0_DWT_PID3

Watchpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0001FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

1.1.6 CM0_DWT_CID0

Watchpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0001FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

1.1.7 CM0_DWT_CID1

Watchpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0001FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

1.1.8 CM0_DWT_CID2

Watchpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0001FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

1.1.9 CM0_DWT_CID3

Watchpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0001FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

1.1.10 CM0_BP_PID4

Breakpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0002FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

1.1.11 CM0_BP_PID0

Breakpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0002FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 11

1.1.12 CM0_BP_PID1

Breakpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0002FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

1.1.13 CM0_BP_PID2

Breakpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0002FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

1.1.14 CM0_BP_PID3

Breakpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0002FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

1.1.15 CM0_BP_CID0

Breakpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0002FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

1.1.16 CM0_BP_CID1

Breakpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0002FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

1.1.17 CM0_BP_CID2

Breakpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0002FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

1.1.18 CM0_BP_CID3

Breakpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0002FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

1.1.19 CM0_SYST_CSR

SysTick Control & Status

Address: 0xE000E010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CLK-SOURCE	TICKINT	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							COUNT-FLAG

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	COUNTFLAG	Indicates whether the counter has counted to "0" since the last read of this register: '0': counter has not counted to "0". '1': counter has counted to "0". COUNTFLAG is set to '1' by a count transition from "1" to "0". COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register. Default Value: 0

1.1.19 CM0_SYST_CSR (continued)

2	CLKSOURCE	Indicates the SysTick counter clock source: '0': SysTick uses the low frequency clock "clk_lf". For this mode to function, "clk_lf" should be less than half the frequency of "clk_sys". Note that "clk_lf" is generated by a low accuracy ILO (Internal Low power Oscillator), with a target frequency of 32.768 kHz (frequency can be as low as 15 KHz and as high as 60 kHz). '1': SysTick uses the system/processor clock "clk_sys". In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided. in SF, TSG6M products, this functionality is not provided. For these products, this field should be set to '1', such that SysTick uses the system clock "clk_sys". Default Value: 0
1	TICKINT	Indicates whether counting to "0" causes the status of the SysTick exception to change to pending: '0': count to "0" does not affect the SysTick exception status. '1': count to "0" changes the SysTick exception status to pending. Changing the value of the counter to "0" by writing zero to the SYST_CVR register to "0" never changes the status of the SysTick exception. Default Value: 0
0	ENABLE	Indicates the enabled status of the SysTick counter: '0': counter is disabled. '1': counter is operating. Default Value: 0

1.1.20 CM0_SYST_RVR

SysTick Reload Value

Address: 0xE000E014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RELOAD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	RELOAD	The value to load into the SYST_CVR register when the counter reaches 0. Default Value: X

1.1.21 CM0_SYST_CVR

SysTick Current Value

Address: 0xE000E018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CURRENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CURRENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CURRENT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CURRENT	Current counter value. This is the value of the counter at the time it is sampled. Default Value: X

1.1.22 CM0_SYST_CALIB

SysTick Calibration Value

Address: 0xE000E01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access		RW	None					
Name	NOREF	SKEW	None [29:24]					

Bits	Name	Description
31	NOREF	Indicates whether a implementation defined reference clock is provided: '0': the reference clock is provided. '1': the reference clock is not provided. When this bit is '1', the SYST_CSR.CLKSOURCEis forced to '1' and cannot be cleared to '0'. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '0'. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '1'. Default Value: 0
30	SKEW	Indicates whether the 10ms calibration value is exact: '0': 10ms calibration value is exact. '1': 10ms calibration value is inexact, because of the clock frequency. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '1' (due to the low accuracy ILO). In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '0'. Default Value: X

1.1.22 CM0_SYST_CALIB (continued)

23 : 0	TENMS	Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is "0", the calibration value is not known. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is 0x00:00147. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is 0x00:0000. Default Value: X

1.1.23 CM0_ISER

Interrupt Set-Enable Register

Address: 0xE000E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETENA [31:24]							

Bits	Name	Description
31 : 0	SETENA	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

1.1.24 CM0_ICER

Interrupt Clear Enable Register

Address: 0xE000E180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRENA [31:24]							

Bits	Name	Description
31 : 0	CLRENA	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

1.1.25 CM0_ISPR

Interrupt Set-Pending Register

Address: 0xE000E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETPEND [31:24]							

Bits	Name	Description
31 : 0	SETPEND	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

1.1.26 CM0_ICPR

Interrupt Clear-Pending Register

Address: 0xE000E280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [31:24]							

Bits	Name	Description
31 : 0	CLRPEND	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

1.1.27 CM0_IPR0

Interrupt Priority Registers

Address: 0xE000E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

1.1.28 CM0_CPUID

CPUID Register

Address: 0xE000ED00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access								
Name	PARTNO [7:4]				REVISION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	PARTNO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access								
Name	VARIANT [23:20]				CONSTANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	IMPLEMENTER [31:24]							

Bits	Name	Description
31 : 24	IMPLEMENTER	Implementer code for ARM. Default Value: 65
23 : 20	VARIANT	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on page xii. Default Value: 0
19 : 16	CONSTANT	Indicates the architecture, ARMv6-M Default Value: 12
15 : 4	PARTNO	Indicates part number, Cortex-M0 Default Value: 3104
3 : 0	REVISION	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on page xii. For release r0p0. Default Value: 0

1.1.29 CM0_ICSR

Interrupt Control State Register

Address: 0xE000ED04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VECTACTIVE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			R
HW Access	RW				None			RW
Name	VECTPENDING [15:12]				None [11:9]			VECTAC-TIVE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None	R				
HW Access	RW	RW	None	RW				
Name	ISRPRE-EMPT	ISRPEND-ING	None	VECTPENDING [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None		RW1S	RW1C	RW1S	RW1C	None
HW Access	RW	None		RW	R	RW	R	None
Name	NMIPEND-SET	None [30:29]		PENDS-VSET	PENDSV-CLR	PENDST-SETb	PENDST-CLR	None

Bits	Name	Description
31	NMIPENDSET	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered. Default Value: 0
28	PENDSVSET	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
27	PENDSVCLR	Clears a pending PendSV interrupt. Default Value: 0
26	PENDSTSETb	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
25	PENDSTCLR	Clears a pending SysTick, whether set here or by the timer hardware. Default Value: 0
23	ISRPREEMPT	Indicates whether a pending exception will be serviced on exit from debug halt state. Default Value: 0

1.1.29 CM0_ICSR (continued)

22	ISRPENDING	Indicates if an external configurable, NVIC generated, interrupt is pending. Default Value: 0
20 : 12	VECTPENDING	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. Default Value: 0
8 : 0	VECTACTIVE	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] Default Value: 0

1.1.30 CM0_AIRCR

Application Interrupt and Reset Control Register

Address: 0xE000ED0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1C	None
HW Access	None					R	R	None
Name	None [7:3]					SYSRESE-TREQ	VECTCL-RACTIVE	None

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access		None						
Name	ENDIAN-NESS	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VECTKEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VECTKEY [31:24]							

Bits	Name	Description
31 : 16	VECTKEY	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is UN-PREDICTABLE. Readback value is UNKNOWN. Default Value: X
15	ENDIANNESS	Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information. Default Value: 0
2	SYSRESETREQ	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on page B1-240 for more information. Default Value: 0
1	VECTCLRACTIVE	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UN-PREDICTABLE. Default Value: 0

1.1.31 CM0_SCR

System Control Register

Address: 0xE000ED10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	None
HW Access	None			R	None	R	R	None
Name	None [7:5]			SEVON-PEND	None	SLEEP-DEEP	SLEEPON-EXIT	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SEVONPEND	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on page A6-197 for more information. Default Value: 0
2	SLEEPDEEP	An implementation can use this bit to select DeepSleep/Hibernate power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep/Hibernate (depends on PWR_CONTROL.HIBERNATE) Default Value: 0
1	SLEEPONEXIT	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on page B1-240 for more information. Default Value: 0

1.1.32 CM0_CCR

Configuration and Control Register

Address: 0xE000ED14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	None		
HW Access	None					None		
Name	None [7:4]				UN-ALIGN_TRP	None		

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	None
HW Access	None							None
Name	None [15:10]						STKALIGN	None

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	STKALIGN	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. Default Value: 1
3	UNALIGN_TRP	1: unaligned word and halfword accesses generate a HardFault exception. Default Value: 1

1.1.33 CM0_SHPR2

System Handler Priority Register 2

Address: 0xE000ED1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_11 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_11	Priority of system handler 11, SVCall Default Value: 0

1.1.34 CM0_SHPR3

System Handler Priority Register 3

Address: 0xE000ED20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_14 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_15 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_15	Priority of system handler 15, SysTick Default Value: 0
23 : 22	PRI_14	Priority of system handler 14, PendSV Default Value: 0

1.1.35 CM0_SHCSR

System Handler Control and State Register

Address: 0xE000ED24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None						
HW Access	RW	None						
Name	SVCALL-PENDED	None						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SVCALLPENDED	0 SVCall is not pending. 1 SVCall is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.) Default Value: 0

1.1.36 CM0_SCS_PID4

System Control Space ROM Table Peripheral ID #4

Address: 0xE000EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

1.1.37 CM0_SCS_PID0

System Control Space ROM Table Peripheral ID #0

Address: 0xE000EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 8

1.1.38 CM0_SCS_PID1

System Control Space ROM Table Peripheral ID #1

Address: 0xE000EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

1.1.39 CM0_SCS_PID2

System Control Space ROM Table Peripheral ID #2

Address: 0xE000EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

1.1.40 CM0_SCS_PID3

System Control Space ROM Table Peripheral ID #3

Address: 0xE000EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

1.1.41 CM0_SCS_CID0

System Control Space ROM Table Component ID #0

Address: 0xE000EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

1.1.42 CM0_SCS_CID1

System Control Space ROM Table Component ID #1

Address: 0xE000EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

1.1.43 CM0_SCS_CID2

System Control Space ROM Table Component ID #2

Address: 0xE000EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

1.1.44 CM0_SCS_CID3

System Control Space ROM Table Component ID #3

Address: 0xE000EFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

1.1.45 CM0_ROM_SCS

CM0 CoreSight ROM Table Peripheral #0

Address: 0xE00FF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to SCS ROM Table Default Value: 4293980163

1.1.46 CM0_ROM_DWT

CM0 CoreSight ROM Table Peripheral #1

Address: 0xE00FF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to DWT ROM Table Default Value: 4293926915

1.1.47 CM0_ROM_BPU

CM0 CoreSight ROM Table Peripheral #2

Address: 0xE00FF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to BPU ROM Table Default Value: 4293931011

1.1.48 CM0_ROM_END

CM0 CoreSight ROM Table End Marker

Address: 0xE00FF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	End marker in peripheral list Default Value: 0

1.1.49 CM0_ROM_CSMT

CM0 CoreSight ROM Table Memory Type

Address: 0xE00FFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

1.1.50 CM0_ROM_PID4

CM0 CoreSight ROM Table Peripheral ID #4

Address: 0xE00FFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

1.1.51 CM0_ROM_PID0

CM0 CoreSight ROM Table Peripheral ID #0

Address: 0xE00FFFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 113

1.1.52 CM0_ROM_PID1

CM0 CoreSight ROM Table Peripheral ID #1

Address: 0xE00FFFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 180

1.1.53 CM0_ROM_PID2

CM0 CoreSight ROM Table Peripheral ID #2

Address: 0xE00FFFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

1.1.54 CM0_ROM_PID3

CM0 CoreSight ROM Table Peripheral ID #3

Address: 0xE00FFFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

1.1.55 CM0_ROM_CID0

CM0 CoreSight ROM Table Component ID #0

Address: 0xE00FFFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

1.1.56 CM0_ROM_CID1

CM0 CoreSight ROM Table Component ID #1

Address: 0xE00FFFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 16

1.1.57 CM0_ROM_CID2

CM0 CoreSight ROM Table Component ID #2

Address: 0xE00FFFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

1.1.58 CM0_ROM_CID3

CM0 CoreSight ROM Table Component ID #3

Address: 0xE00FFFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

2 CPUSS Registers

This section discusses the CPUSS registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

2.1 CPUSS Register Mapping Details

Register	Address	Description
CPUSS_CONFIG	0x40100000	Configuration register
CPUSS_SYSREQ	0x40100004	SYSCALL control register
CPUSS_SYSARG	0x40100008	SYSARG control register
CPUSS_PROTECTION	0x4010000C	Protection control register
CPUSS_PRIV_ROM	0x40100010	ROM privilege register
CPUSS_PRIV_RAM	0x40100014	RAM privilege register
CPUSS_PRIV_FLASH	0x40100018	ROM privilege register
CPUSS_WOUNDING	0x4010001C	Wounding register
CPUSS_FLASH_CTL	0x40100030	FLASH control register
CPUSS_ROM_CTL	0x40100034	ROM control register

2.1.1 CPUSS_CONFIG

Configuration register

Address: 0x40100000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							VECT_IN_RAM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VECT_IN_RAM	0': Vector Table is located at 0x0000:0000 in flash '1': Vector Table is located at 0x2000:0000 in SRAM Note that vectors for RESET and FAULT are always fetched from ROM. Value in flash/RAM is ignored for these vectors. Default Value: 0

2.1.2 CPUSS_SYSREQ

SYSCALL control register

Address: 0x40100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	SYSCALL_COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	SYSCALL_COMMAND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	R	RW	RW	None		
HW Access	R	W	RW	A	R	None		
Name	SYSCALL_REQ	HMASTER_0	ROM_ACCESS_EN	PRIVILEGED	DIS_RESET_VECT_REL	None [26:24]		

Bits	Name	Description
31	SYSCALL_REQ	CPU/DAP writes a '1' to this field to request a SystemCall. The HMASTER_0 field indicates the source of the write access. Setting this field to '1' immediate results in a NMI. The SystemCall NMI interrupt handler sets this field to '0' after servicing the request. Default Value: 0
30	HMASTER_0	Indicates the source of the write access to the SYSREQ register. '0': CPU write access. '1': DAP write access. HW sets this field when the SYSREQ register is written to and SYSCALL_REQ is '0' (the last time it is set is when SW sets SYSCALL_REQ from '0' to '1'). Default Value: 0
29	ROM_ACCESS_EN	Indicates that executing from Boot ROM is enabled. HW sets this field to '1', on reset or when the SystemCall NMI vector is fetched from Boot ROM. HW sets this field to '0', when the CPU is NOT executing from either Boot or System ROM. This bit is used for debug purposes only. Default Value: 1

2.1.2 CPUSS_SYSREQ (continued)

28	PRIVILEGED	Indicates whether the system is in privileged ('1') or user mode ('0'). Only CPU SW executing from ROM can set this field to '1' when ROM_ACCESS_EN is '1' (the CPU is executing a SystemCall NMI interrupt handler). Any other write to this field sets is to '0'. This field is used as the AHB-Lite hprot[1] signal to implement Cypress proprietary user/privileged modes. These modes are used to enable/disable access to specific MMIO registers and memory regions. Default Value: 1
27	DIS_RESET_VECT_REL	Disable Reset Vector fetch relocation: '0': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are redirected to ROM. '1': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are made to flash. Note that this field defaults to '0' on reset, ensuring actual reset vector fetches are always made to ROM. Note that this field does not affect DAP accesses. Flash DfT routines may set this bit to '1' to enable uninhibited read-back of programmed data in the first flash page. Default Value: 0
15 : 0	SYSCALL_COMMAND	Opcode of the system call being requested. Default Value: 0

2.1.3 CPUSS_SYSARG

SYSARG control register

Address: 0x40100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	SYSCALL_ARG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	SYSCALL_ARG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	SYSCALL_ARG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	SYSCALL_ARG [31:24]							

Bits	Name	Description
31 : 0	SYSCALL_ARG	Argument to System Call specified in SYSREQ. Semantics of argument depends on system call made. Typically a pointer to a parameter block. Default Value: 0

2.1.4 CPUSS_PROTECTION

Protection control register

Address: 0x4010000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				A			
Name	None [7:4]				PROTECTION_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None						
HW Access	R	None						
Name	PROTEC-TION_LOCK	None [30:24]						

Bits	Name	Description
31	PROTECTION_LOCK	Setting this field will block (ignore) any further writes to the PROTECTION_MODE field in this register. Once '1', this field cannot be cleared. Default Value: 0
3 : 0	PROTECTION_MODE	Current protection mode; this field is available as a global signal everywhere in the system. Writes to this field are ignored when PROTECTION_LOCK is '1': 0b1xxx: BOOT 0b01xx: KILL 0b001x: PROTECTED 0b0001: OPEN 0b0000: VIRGIN (also used for DEAD mode, but then FLASH_LOCK is also set) Default Value: 15

2.1.5 CPUSS_PRIV_ROM

ROM privilege register

Address: 0x40100010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BROM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	BROM_PROT_LIMIT	Indicates the limit where the privileged area of the Boot ROM partition starts in increments of 256 Bytes. "0": Entire Boot ROM is Privileged. "1": First 256 Bytes are User accessable. ... BROM_PROT_LIMIT >= "Boot ROM partition capacity": Entire Boot ROM partition is user mode accessible. Default Value: 0

2.1.6 CPUSS_PRIV_RAM

RAM privilege register

Address: 0x40100014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RAM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RAM_PROT_LIMIT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	RAM_PROT_LIMIT	Indicates the limit where the privileged area of SRAM starts in increments of 256 Bytes. "0": Entire SRAM is Privileged. "1": First 256 Bytes are User accessable. Any number larger than the size of the SRAM indicates that the entire SRAM is user mode accessible. Default Value: 0

2.1.7 CPUSS_PRIV_FLASH

ROM privilege register

Address: 0x40100018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLASH_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					FLASH_PROT_LIMIT [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	FLASH_PROT_LIMIT	Indicates the limit where the privileged area of flash starts in increments of 256 Bytes. "0": Entire flash is Privileged. "1": First 256 Bytes are User accessable. Any number larger than the size of the flash indicates that the entire flash is user mode accessible. Note that SuperVisory rows are always User accessable. If FLASH_PROT_LIMIT defines a non-empty privileged area, the boot ROM will assume that a system call table exists at the beginning of the Flash privileged area and use it for all SystemCalls made using SYSREQ. Default Value: 0

2.1.8 CPUSS_WOUNDING

Wounding register

Address: 0x4010001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW1S			None	RW1S		
HW Access	None	R			None	R		
Name	None	FLASH_WOUND [22:20]			None	RAM_WOUND [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 20	FLASH_WOUND	Indicates the amount of accessible flash in this part. The value in this field is effectively write-once (it is only possible to set bits, not clear them). The remainder portion of flash is not accessible and will return an AHB-Lite bus error. "0": entire memory accessible "1": first 1/2 of the memory accessible "2": first 1/4 of the memory accessible "3": first 1/8 of the memory accessible "4": first 1/16 of the memory accessible "5": first 1/32 of the memory accessible "6": first 1/64 of the memory accessible "7": first 1/128 of the memory accessible (used for the DEAD protection mode) Default Value: 0

2.1.8 CPUSS_WOUNDING (continued)

18 : 16	RAM_WOUND	Indicates the amount of accessible RAM 0 memory capacitty in this part. The value in this field is effectively write-once (it is only possible to set bits, not clear them). The remainder portion of SRAM is not accessible and will return an AHB-Lite bus error. "0": entire memory accessible "1": first 1/2 of the memory accessible "2": first 1/4 of the memory accessible "3": first 1/8 of the memory accessible "4": first 1/16 of the memory accessible "5": first 1/32 of the memory accessible "6": first 1/64 of the memory accessible "7": first 1/128 of the memory accessible Default Value: 0

2.1.9 CPUSS_FLASH_CTL

FLASH control register

Address: 0x40100030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			PREF_EN	None [3:2]		FLASH_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW1C
Name	None [15:9]							FLASH_IN-VALIDATE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLASH_INVALIDATE	1': Invalidates the content of the flash controller's buffers. Default Value: 0
4	PREF_EN	Prefetch enable: '0': disabled. This is a desirable seeting when FLASH_WS is "0" or when predictable execution behavior is required. '1': enabled. Default Value: 0
1 : 0	FLASH_WS	Amount of ROM wait states: "0": 0 wait states (fast flash: [0, 24] MHz system frequency, slow flash: [0, 16] MHz system frequency) "1": 1 wait state (fast flash: [24, 48] MHz system frequency, slow flash: [16, 32] MHz system frequency) "2": 2 wait states (slow flash: [32, 48] MHz system frequency) "3": undefined Default Value: 0

2.1.10 CPUSS_ROM_CTL

ROM control register

Address: 0x40100034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ROM_WS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ROM_WS	Amount of ROM wait states: '0': 0 wait states. Use this setting for newer, faster ROM design. Use this setting for older, slower ROM design and frequencies in the range [0, 24] MHz. '1': 1 wait state. Use this setting for older, slower ROM design and frequencies in the range <24, 48] MHz. CPUSSv2 supports two types of ROM memory: an older, slower design (operating at up to 24 MHz) and a newer, faster design (operating at up to 48 MHz). The older design requires 1 wait state for frequencies above 24 MHz. The newer design never requires wait states. All chips after Street Fighter will use the newer design. As a result, all chips after Street Fighter can always use 0 wait states. Default Value: 0

3 GPIO Registers

This section discusses the GPIO registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

3.1 GPIO Register Mapping Details

Register	Address	Description
GPIO_PRT0_DR	0x40040000	Port output data register
GPIO_PRT0_PS	0x40040004	Port IO pad state register
GPIO_PRT0_PC	0x40040008	Port configuration register
GPIO_PRT0_INTR_CFG	0x4004000C	Port interrupt configuration register
GPIO_PRT0_INTR	0x40040010	Port interrupt status register
GPIO_PRT0_PC2	0x40040018	Port configuration register 2
GPIO_PRT0_DR_SET	0x40040040	Port output data set register
GPIO_PRT0_DR_CLR	0x40040044	Port output data clear register
GPIO_PRT0_DR_INV	0x40040048	Port output data invert register
GPIO_PRT1_DR	0x40040100	Port output data register. See GPIO_PRT0_DR for the details of bit fields.
GPIO_PRT1_PS	0x40040104	Port IO pad state register. See GPIO_PRT0_PS for the details of bit fields.
GPIO_PRT1_PC	0x40040108	Port configuration register. See GPIO_PRT0_PC for the details of bit fields.
GPIO_PRT1_INTR_CFG	0x4004010C	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT1_INTR	0x40040110	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT1_PC2	0x40040118	Port configuration register 2. See GPIO_PRT0_PC2 for the details of bit fields.
GPIO_PRT1_DR_SET	0x40040140	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT1_DR_CLR	0x40040144	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT1_DR_INV	0x40040148	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT2_DR	0x40040200	Port output data register
GPIO_PRT2_PS	0x40040204	Port IO pad state register
GPIO_PRT2_PC	0x40040208	Port configuration register
GPIO_PRT2_INTR_CFG	0x4004020C	Port interrupt configuration register
GPIO_PRT2_INTR	0x40040210	Port interrupt status register
GPIO_PRT2_PC2	0x40040218	Port configuration register 2
GPIO_PRT0_DR_SET	0x40040240	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT0_DR_CLR	0x40040244	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT0_DR_INV	0x40040248	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.

Register	Address	Description
GPIO_PRT3_DR	0x40040300	Port output data register
GPIO_PRT3_PS	0x40040304	Port IO pad state register
GPIO_PRT3_PC	0x40040308	Port configuration register
GPIO_PRT3_INTR_CFG	0x4004030C	Port interrupt configuration register
GPIO_PRT3_INTR	0x40040310	Port interrupt status register
GPIO_PRT3_PC2	0x40040318	Port configuration register 2
GPIO_PRT3_DR_SET	0x40040340	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT3_DR_CLR	0x40040344	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT3_DR_INV	0x40040348	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_INTR_CAUSE0	0x40041000	Interrupt port cause register
GPIO_INTR_CAUSE1	0x40041004	Interrupt port cause register. See GPIO_INTR_CAUSE0 for the details of bit fields.
GPIO_INTR_CAUSE2	0x40041008	Interrupt port cause register. See GPIO_INTR_CAUSE0 for the details of bit fields.
GPIO_INTR_CAUSE3	0x4004100C	Interrupt port cause register. See GPIO_INTR_CAUSE0 for the details of bit fields.

3.1.1 GPIO_PRT0_DR

Port output data register

Address: 0x40040000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

3.1.2 GPIO_PRT0_PS

Port IO pad state register

Address: 0x40040004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

3.1.2 GPIO_PRT0_PS (continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

3.1.3 GPIO_PRT0_PC

Port configuration register

Address: 0x40040008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0

3.1.3 GPIO_PRT0_PC (continued)

14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF :** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT :** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU :** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1 :** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z :** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1 :** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1 :** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU :** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

3.1.4 GPIO_PRT0_INTR_CFG

Port interrupt configuration register

Address: 0x4004000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

3.1.4 GPIO_PRT0_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0
		0x0: DISABLE : Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

3.1.5 GPIO_PRT0_INTR

Port interrupt status register

Address: 0x40040010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

3.1.5 GPIO_PRT0_INTR (continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

3.1.6 GPIO_PRT0_PC2

Port configuration register 2

Address: 0x40040018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

3.1.6 GPIO_PRT0_PC2 (continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

3.1.7 GPIO_PRT0_DR_SET

Port output data set register

Address: 0x40040040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

3.1.8 GPIO_PRT0_DR_CLR

Port output data clear register

Address: 0x40040044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

3.1.9 GPIO_PRT0_DR_INV

Port output data invert register

Address: 0x40040048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

3.1.10 GPIO_PRT2_DR

Port output data register

Address: 0x40040200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DATA0	IO pad 0 output data. Default Value: 0

3.1.11 GPIO_PRT2_PS

Port IO pad state register

Address: 0x40040204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

3.1.12 GPIO_PRT2_PC

Port configuration register

Address: 0x40040208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0

3.1.12 GPIO_PRT2_PC (continued)

0x0: OFF :

Mode 0 (analog mode): Output buffer off (high Z). Input buffer off.

0x1: INPUT :

Mode 1: Output buffer off (high Z). Input buffer on.

0x2: 0_PU :

Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on.

0x3: PD_1 :

Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on.

0x4: 0_Z :

Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.

0x5: Z_1 :

Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.

0x6: 0_1 :

Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.

0x7: PD_PU :

Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

3.1.13 GPIO_PRT2_INTR_CFG

Port interrupt configuration register

Address: 0x4004020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

3.1.13 GPIO_PRT2_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

3.1.14 GPIO_PRT2_INTR

Port interrupt status register

Address: 0x40040210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							A
Name	None [7:1]							DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

3.1.15 GPIO_PRT2_PC2

Port configuration register 2

Address: 0x40040218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

3.1.16 GPIO_PRT3_DR

Port output data register

Address: 0x40040300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					RW	RW	RW
Name	None [7:3]					DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

3.1.17 GPIO_PRT3_PS

Port IO pad state register

Address: 0x40040304

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

3.1.18 GPIO_PRT3_PC

Port configuration register

Address: 0x40040308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							DM2

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0

3.1.18 GPIO_PRT3_PC (continued)

2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF :** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT :** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU :** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1 :** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z :** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1 :** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1 :** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU :** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

3.1.19 GPIO_PRT3_INTR_CFG

Port interrupt configuration register

Address: 0x4004030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

3.1.19 GPIO_PRT3_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0
		0x0: DISABLE : Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

3.1.20 GPIO_PRT3_INTR

Port interrupt status register

Address: 0x40040310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [23:19]					PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

3.1.21 GPIO_PRT3_PC2

Port configuration register 2

Address: 0x40040318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

3.1.22 GPIO_INTR_CAUSE0

Interrupt port cause register

Address: 0x40041000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				PORT_INT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a shared/combined interrupt line "gpio_interrupt". The SW ISR reads the register to determine which IO port(s) is responsible for the shared/combined interrupt line "gpio_interrupt". Once, the IO port(s) is determined, the IO port's INTR register is read to determine the IO pad(s) in the IO port that caused the interrupt. Default Value: 0

4 HSIOM Registers

This section discusses the HSIOM registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

4.1 HSIOM Register Mapping Details

Register	Address	Description
HSIOM_PORT_SEL0	0x40020000	Port selection register
HSIOM_PORT_SEL1	0x40020100	Port selection register. See HSIOM_PORT_SEL0 for the details of bit fields.
HSIOM_PORT_SEL2	0x40020200	Port selection register
HSIOM_PORT_SEL3	0x40020300	Port selection register
HSIOM_PUMP_CTL	0x40022000	Pump control

4.1.1 HSIOM_PORT_SEL0

Port selection register

Address: 0x40020000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

4.1.1 HSIOM_PORT_SEL0 (continued)

0x0: GPIO :

SW controlled GPIO.

0x1: GPIO_DSI :

SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI :

DSI controlled "out" and "oe_n".

0x3: DSI_GPIO :

DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE :

CSD sense connection (analog mode)

0x5: CSD_SHIELD :

CSD shield connection (analog mode)

0x6: AMUXA :

AMUXBUS A connection.

0x7: AMUXB :

AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0 :

Chip specific Active source 0 connection.

0x9: ACT_1 :

Chip specific Active source 1 connection.

0xa: ACT_2 :

Chip specific Active source 2 connection.

0xb: ACT_3 :

Chip specific Active source 3 connection.

4.1.1 HSIOM_PORT_SEL0 (continued)

0xc: LCD_COM :

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: LCD_SEG :

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0 :

Chip specific DeepSleep source 0 connection.

0xd: DS_1 :

Chip specific DeepSleep source 1 connection.

0xe: DS_2 :

Chip specific DeepSleep source 2 connection.

0xf: DS_3 :

Chip specific DeepSleep source 3 connection.

4.1.2 HSIOM_PORT_SEL2

Port selection register

Address: 0x40020200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0 **0x0: GPIO :** SW controlled GPIO. **0x1: GPIO_DSI :** SW controlled "out", DSI controlled "oe_n". **0x2: DSI_DSI :** DSI controlled "out" and "oe_n". **0x3: DSI_GPIO :** DSI controlled "out", SW controlled "oe_n".

4.1.2 HSIOM_PORT_SEL2 (continued)

0x4: CSD_SENSE :

CSD sense connection (analog mode)

0x5: CSD_SHIELD :

CSD shield connection (analog mode)

0x6: AMUXA :

AMUXBUS A connection.

0x7: AMUXB :

AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0 :

Chip specific Active source 0 connection.

0x9: ACT_1 :

Chip specific Active source 1 connection.

0xa: ACT_2 :

Chip specific Active source 2 connection.

0xb: ACT_3 :

Chip specific Active source 3 connection.

0xc: LCD_COM :

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: LCD_SEG :

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0 :

Chip specific DeepSleep source 0 connection.

4.1.2 HSIOM_PORT_SEL2 (continued)

0xd: DS_1 :

Chip specific DeepSleep source 1 connection.

0xe: DS_2 :

Chip specific DeepSleep source 2 connection.

0xf: DS_3 :

Chip specific DeepSleep source 3 connection.

4.1.3 HSIOM_PORT_SEL3

Port selection register

Address: 0x40020300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0 **0x0: GPIO :** SW controlled GPIO. **0x1: GPIO_DSI :** SW controlled "out", DSI controlled "oe_n". **0x2: DSI_DSI :** DSI controlled "out" and "oe_n".

4.1.3 HSIOM_PORT_SEL3 (continued)

0x3: DSI_GPIO :

DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE :

CSD sense connection (analog mode)

0x5: CSD_SHIELD :

CSD shield connection (analog mode)

0x6: AMUXA :

AMUXBUS A connection.

0x7: AMUXB :

AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0 :

Chip specific Active source 0 connection.

0x9: ACT_1 :

Chip specific Active source 1 connection.

0xa: ACT_2 :

Chip specific Active source 2 connection.

0xb: ACT_3 :

Chip specific Active source 3 connection.

0xc: LCD_COM :

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: LCD_SEG :

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

4.1.3 HSIOM_PORT_SEL3 (continued)

0xc: DS_0 :

Chip specific DeepSleep source 0 connection.

0xd: DS_1 :

Chip specific DeepSleep source 1 connection.

0xe: DS_2 :

Chip specific DeepSleep source 2 connection.

0xf: DS_3 :

Chip specific DeepSleep source 3 connection.

4.1.4 HSIOM_PUMP_CTL

Pump control

Address: 0x40022000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CLOCK_-SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Pump enabled: '0': Disabled. '1': Enabled. Default Value: 0
0	CLOCK_SEL	Clock select: '0': External clock. '1': Internal clock (deprecated). Default Value: 0

5 PERI Registers

This section discusses the PERI registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

5.1 PERI Register Mapping Details

Register	Address	Description
PERI_DIV_CMD	0x40010000	Divider command register
PERI_PCLK_CTL0	0x40010100	Programmable clock control register
PERI_PCLK_CTL1	0x40010104	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL2	0x40010108	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL3	0x4001010C	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_DIV_16_CTL0	0x40010300	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL1	0x40010304	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL2	0x40010308	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL3	0x4001030C	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.

5.1.1 PERI_DIV_CMD

Divider command register

Address: 0x40010000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	SEL_TYPE [7:6]		SEL_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	PA_SEL_TYPE [15:14]		PA_SEL_DIV [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	RW1C	None					
Name	ENABLE	DISABLE	None [29:24]					

Bits	Name	Description
31	ENABLE	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The SEL_DIV and SEL_TYPE fields specify which divider is to be enabled. The enabled divider may be phase aligned to either "clk_hf" (typical usage) or to ANY enabled divider. The PA_SEL_DIV and P_SEL_TYPE fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of "clk_hf"/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to "clk_hf" takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. Default Value: 0

5.1.1 PERI_DIV_CMD (continued)

30	DISABLE	Clock divider disable command (mutually exlusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The SEL_DIV and SEL_TYPE fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. Default Value: 0
15 : 14	PA_SEL_TYPE	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
13 : 8	PA_SEL_DIV	(PA_SEL_TYPE, PA_SEL_DIV) pecifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_SEL_DIV is "63" and "PA_SEL_TYPE" is "3", "clk_hf" is used as reference. Default Value: 63
7 : 6	SEL_TYPE	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
5 : 0	SEL_DIV	(SEL_TYPE, SEL_DIV) specifies the divider on which the command (DISABLE/ENABLE) is performed. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock signal(s) are generated. Default Value: 63

5.1.2 PERI_PCLK_CTL0

Programmable clock control register

Address: 0x40010100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None				RW	
HW Access	R		None				R	
Name	SEL_TYPE [7:6]		None [5:2]				SEL_DIV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
1 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 3

5.1.3 PERI_DIV_16_CTL0

Divider control register (for 16.0 divider)

Address: 0x40010300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

6 SCB Registers

This section discusses the SCB registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

6.1 SCB Register Mapping Details

Register	Address	Description
SCB_CTRL	0x40060000	Generic control register.
SCB_STATUS	0x40060004	Generic status register.
SCB_I2C_CTRL	0x40060060	I2C control register.
SCB_I2C_STATUS	0x40060064	I2C status register.
SCB_I2C_M_CMD	0x40060068	I2C master command register.
SCB_I2C_S_CMD	0x4006006C	I2C slave command register.
SCB_I2C_CFG	0x40060070	I2C configuration register.
SCB_TX_CTRL	0x40060200	Transmitter control register.
SCB_TX_FIFO_CTRL	0x40060204	Transmitter FIFO control register.
SCB_TX_FIFO_STATUS	0x40060208	Transmitter FIFO status register.
SCB_TX_FIFO_WR	0x40060240	Transmitter FIFO write register.
SCB_RX_CTRL	0x40060300	Receiver control register.
SCB_RX_FIFO_CTRL	0x40060304	Receiver FIFO control register.
SCB_RX_FIFO_STATUS	0x40060308	Receiver FIFO status register.
SCB_RX_MATCH	0x40060310	Slave address and mask register.
SCB_RX_FIFO_RD	0x40060340	Receiver FIFO read register.
SCB_RX_FIFO_RD_SILENT	0x40060344	Receiver FIFO read register.
SCB_EZ_DATA0	0x40060400	Memory buffer registers.
SCB_EZ_DATA1	0x40060404	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA2	0x40060408	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA3	0x4006040C	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA4	0x40060410	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA5	0x40060414	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA6	0x40060418	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA7	0x4006041C	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA8	0x40060420	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA9	0x40060424	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.

Register	Address	Description
SCB_EZ_DATA10	0x40060428	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA11	0x4006042C	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA12	0x40060430	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA13	0x40060434	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA14	0x40060438	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA15	0x4006043C	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA16	0x40060440	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA17	0x40060444	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA18	0x40060448	Memory buffer registers. SeeSCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA19	0x4006044C	Memory buffer registers. SeeSCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA20	0x40060450	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA21	0x40060454	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA22	0x40060458	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA23	0x4006045C	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA24	0x40060460	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA25	0x40060464	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA26	0x40060468	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA27	0x4006046C	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA28	0x40060470	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA29	0x40060474	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA30	0x40060478	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_EZ_DATA31	0x4006047C	Memory buffer registers. See SCB_EZ_DATA0 for the details of bit fields.
SCB_INTR_CAUSE	0x40060E00	Active clocked interrupt signal register
SCB_INTR_I2C_EC	0x40060E80	Externally clocked I2C interrupt request register
SCB_INTR_I2C_EC_MASK	0x40060E88	Externally clocked I2C interrupt mask register
SCB_INTR_I2C_EC_MASKED	0x40060E8C	Externally clocked I2C interrupt masked register
SCB_INTR_M	0x40060F00	Master interrupt request register.
SCB_INTR_M_SET	0x40060F04	Master interrupt set request register
SCB_INTR_M_MASK	0x40060F08	Master interrupt mask register.
SCB_INTR_M_MASKED	0x40060F0C	Master interrupt masked request register
SCB_INTR_S	0x40060F40	Slave interrupt request register.
SCB_INTR_S_SET	0x40060F44	Slave interrupt set request register.
SCB_INTR_S_MASK	0x40060F48	Slave interrupt mask register.
SCB_INTR_S_MASKED	0x40060F4C	Slave interrupt masked request register
SCB_INTR_TX	0x40060F80	Transmitter interrupt request register.
SCB_INTR_TX_SET	0x40060F84	Transmitter interrupt set request register
SCB_INTR_TX_MASK	0x40060F88	Transmitter interrupt mask register.
SCB_INTR_TX_MASKED	0x40060F8C	Transmitter interrupt masked request register
SCB_INTR_RX	0x40060FC0	Receiver interrupt request register.
SCB_INTR_RX_SET	0x40060FC4	Receiver interrupt set request register.
SCB_INTR_RX_MASK	0x40060FC8	Receiver interrupt mask register.
SCB_INTR_RX_MASKED	0x40060FCC	Receiver interrupt masked request register

6.1.1 SCB_CTRL

Generic control register.

Address: 0x40060000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_-MODE	EZ_MODE	EC_OP_-MODE	EC_AM_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP, select the specific operation mode and oversampling factor. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3

6.1.1 SCB_CTRL (continued)

		0x0: I2C : Inter-Integrated Circuits (I2C) mode. **0x1: SPI :** Serial Peripheral Interface (SPI) mode. **0x2: UART :** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is 0 and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames mot seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0

6.1.1 SCB_CTRL (continued)

9	EC_OP_MODE	Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0
8	EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

6.1.1 SCB_CTRL (continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period. In SPI master mode, the valid range is [3, 15]. At an IP frequency of 48 MHz, the maximum IP bit rate is 12 Mbps. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock "spi_clk_out" to SPI MISO input "spi_miso_in" round trip delay is introducing significant delays (multiple "spi_clk_out" cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. The maximum IP bit rate of 12 Mbps provides an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps. The maximum bit rates provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency): - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required IP clock frequency): - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. IP clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. IP clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. IP clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. IP clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. IP clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. IP clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

6.1.2 SCB_STATUS

Generic status register.

Address: 0x40060004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

6.1.3 SCB_I2C_CTRL

I2C control register.

Address: 0x40060060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_-DATA_NACK	S_NOT_READY_AD-DR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENER-AL_IGNORE	None	M_NOT_READY_-DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_-MODE	SLAVE_-MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

6.1.3 SCB_I2C_CTRL (continued)

15	S_NOT_READY_-DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	S_NOT_READY_AD-DR_NACK	For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when: - EC_AM is '0', EC_OP is '0' and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_-DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1

6.1.3 SCB_I2C_CTRL (continued)

7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be >= 8 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 IP clock cycles and <= 16 IP clock cycles. Default Value: 8
3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF high time should be >= 5 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

6.1.4 SCB_I2C_STATUS

I2C status register.

Address: 0x40060064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0

6.1.4 SCB_I2C_STATUS (continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

6.1.5 SCB_I2C_M_CMD

I2C master command register.

Address: 0x40060068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

6.1.5 SCB_I2C_M_CMD (continued)

1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

6.1.6 SCB_I2C_S_CMD

I2C slave command register.

Address: 0x4006006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

6.1.7 SCB_I2C_CFG

I2C configuration register.

Address: 0x40060070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_-FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_-FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. Default Value: 2

6.1.7 SCB_I2C_CFG (continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. Default Value: 3

6.1.8 SCB_TX_CTRL

Transmitter control register.

Address: 0x40060200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

6.1.9 SCB_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40060204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

6.1.10 SCB_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40060208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

6.1.11 SCB_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40060240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

6.1.12 SCB_RX_CTRL

Receiver control register.

Address: 0x40060300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

6.1.13 SCB_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40060304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

6.1.14 SCB_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40060308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

6.1.15 SCB_RX_MATCH

Slave address and mask register.

Address: 0x40060310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

6.1.16 SCB_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40060340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

6.1.17 SCB_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40060344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

6.1.18 SCB_EZ_DATA0

Memory buffer registers.

Address: 0x40060400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

6.1.19 SCB_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40060E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [7:5]			I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

6.1.20 SCB_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40060E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0

6.1.20 SCB_INTR_I2C_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when EC_AM is '1'. Default Value: 0

6.1.21 SCB_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40060E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.22 SCB_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40060E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

6.1.23 SCB_INTR_M

Master interrupt request register.

Address: 0x40060F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

6.1.24 SCB_INTR_M_SET

Master interrupt set request register

Address: 0x40060F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.25 SCB_INTR_M_MASK

Master interrupt mask register.

Address: 0x40060F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.26 SCB_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40060F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

6.1.27 SCB_INTR_S

Slave interrupt request register.

Address: 0x40060F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0

6.1.27 SCB_INTR_S (continued)

5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

6.1.28 SCB_INTR_S_SET

Slave interrupt set request register.

Address: 0x40060F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.28 SCB_INTR_S_SET (continued)

1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.29 SCB_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40060F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.29 SCB_INTR_S_MASK (continued)

1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.30 SCB_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40060F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0

6.1.30 SCB_INTR_S_MASKED (continued)

1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

6.1.31 SCB_INTR_TX

Transmitter interrupt request register.

Address: 0x40060F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0

6.1.31 SCB_INTR_TX (continued)

1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

6.1.32 SCB_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40060F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.33 SCB_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40060F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.34 SCB_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40060F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

6.1.35 SCB_INTR_RX

Receiver interrupt request register.

Address: 0x40060FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0

6.1.35 SCB_INTR_RX (continued)

3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET: BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL. Only used in FIFO mode. Default Value: 0

6.1.36 SCB_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40060FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.37 SCB_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40060FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.38 SCB_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40060FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

7 SFLASH Registers

This section discusses the SFLASH registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

7.1 SFLASH Register Mapping Details

Register	Address	Description
SFLASH_SILICON_ID	0x0FFFF144	Silicon ID
SFLASH_HIB_KEY_DELAY	0x0FFFF150	Hibernate wakeup value for PWR_KEY_DELAY
SFLASH_DPSLP_KEY_DELAY	0x0FFFF152	DeepSleep wakeup value for PWR_KEY_DELAY
SFLASH_SWD_CONFIG	0x0FFFF154	SWD pinout selector (not present in TSG4/TSG5-M)
SFLASH_SWD_LISTEN	0x0FFFF158	Listen Window Length
SFLASH_FLASH_START	0x0FFFF15C	Flash Image Start Address
SFLASH_CSD_TRIM1_HVIDAC	0x0FFFF160	CSD Trim Data for HVIDAC operation
SFLASH_CSD_TRIM2_HVIDAC	0x0FFFF161	CSD Trim Data for HVIDAC operation
SFLASH_CSD_TRIM1_CSD	0x0FFFF162	CSD Trim Data for (normal) CSD operation
SFLASH_CSD_TRIM2_CSD	0x0FFFF163	CSD Trim Data for (normal) CSD operation
SFLASH_IMO_TRIM_USBMODE_24	0x0FFFF1BE	USB IMO TRIM 24MHz
SFLASH_IMO_TRIM_USBMODE_48	0x0FFFF1BF	USB IMO TRIM 48MHz
SFLASH_IMO_TCTRIM_LT0	0x0FFFF1CC	IMO TempCo Trim Register (SRSS-Lite)
SFLASH_IMO_TCTRIM_LT1	0x0FFFF1CD	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT2	0x0FFFF1CE	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT3	0x0FFFF1CF	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT4	0x0FFFF1D0	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT5	0x0FFFF1D1	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT6	0x0FFFF1D2	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT7	0x0FFFF1D3	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT8	0x0FFFF1D4	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT9	0x0FFFF1D5	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT10	0x0FFFF1D6	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.

Register	Address	Description
SFLASH_IMO_TCTRIM_LT11	0x0FFFF1D7	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT12	0x0FFFF1D8	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT13	0x0FFFF1D9	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT14	0x0FFFF1DA	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT15	0x0FFFF1DB	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT16	0x0FFFF1DC	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT17	0x0FFFF1DD	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT18	0x0FFFF1DE	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT19	0x0FFFF1DF	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT20	0x0FFFF1E0	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT21	0x0FFFF1E1	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT22	0x0FFFF1E2	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT23	0x0FFFF1E3	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT24	0x0FFFF1E4	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT0	0x0FFFF1E5	IMO Frequency Trim Register (SRSS-Lite)
SFLASH_IMO_TRIM_LT1	0x0FFFF1E6	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT2	0x0FFFF1E7	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT3	0x0FFFF1E8	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT4	0x0FFFF1E9	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT5	0x0FFFF1EA	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT6	0x0FFFF1EB	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT7	0x0FFFF1EC	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT8	0x0FFFF1ED	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT9	0x0FFFF1EE	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT10	0x0FFFF1EF	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT11	0x0FFFF1F0	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT12	0x0FFFF1F1	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT13	0x0FFFF1F2	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT14	0x0FFFF1F3	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.

Register	Address	Description
SFLASH_IMO_TRIM_LT15	0x0FFFF1F4	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT16	0x0FFFF1F5	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT17	0x0FFFF1F6	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT18	0x0FFFF1F7	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT19	0x0FFFF1F8	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT20	0x0FFFF1F9	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT21	0x0FFFF1FA	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT22	0x0FFFF1FB	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT23	0x0FFFF1FC	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT24	0x0FFFF1FD	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.

7.1.1 SFLASH_SILICON_ID

Silicon ID

Address: 0x0FFFF144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: X

7.1.2 SFLASH_HIB_KEY_DELAY

Hibernate wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

7.1.3 SFLASH_DPSLP_KEY_DELAY

DeepSleep wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF152

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

7.1.4 SFLASH_SWD_CONFIG

SWD pinout selector (not present in TSG4/TSG5-M)

Address: 0x0FFFF154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							
Name	None [7:1]							SWD_SELECT

Bits	Name	Description
0	SWD_SELECT	0: Use Primary SWD location 1: Use Alternate SWD location Default Value: X

7.1.5 SFLASH_SWD_LISTEN

Listen Window Length

Address: 0x0FFFF158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	CYCLES [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	CYCLES [31:24]							

Bits	Name	Description
31 : 0	CYCLES	Number of clock cycles Default Value: X

7.1.6 SFLASH_FLASH_START

Flash Image Start Address

Address: 0x0FFFF15C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDRESS [31:24]							

Bits	Name	Description
31 : 0	ADDRESS	Start Address Default Value: X

7.1.7 SFLASH_CSD_TRIM1_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

7.1.8 SFLASH_CSD_TRIM2_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF161

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

7.1.9 SFLASH_CSD_TRIM1_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF162

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

7.1.10 SFLASH_CSD_TRIM2_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF163

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

7.1.11 SFLASH_IMO_TRIM_USBMODE_24

USB IMO TRIM 24MHz

Address: 0x0FFFF1BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TRIM_24 [7:0]							

Bits	Name	Description
7 : 0	TRIM_24	TRIM value for IMO with USB at 24MHz Default Value: X

7.1.12 SFLASH_IMO_TRIM_USBMODE_48

USB IMO TRIM 48MHz

Address: 0x0FFFF1BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TRIM_24 [7:0]							

Bits	Name	Description
7 : 0	TRIM_24	TRIM value for IMO with USB at 24MHz Default Value: X

7.1.13 SFLASH_IMO_TCTRIM_LT0

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF1CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

7.1.14 SFLASH_IMO_TRIM_LT0

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF1E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

8 SPCIF Registers

This section discusses the SPCIF registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

8.1 SPCIF Register Mapping Details

Register	Address	Description
SPCIF_GEOMETRY	0x40110000	Flash/NVL geometry information
SPCIF_INTR	0x401107F0	SPCIF interrupt request register
SPCIF_INTR_SET	0x401107F4	SPCIF interrupt set request register
SPCIF_INTR_MASK	0x401107F8	SPCIF interrupt mask register
SPCIF_INTR_MASKED	0x401107FC	SPCIF interrupt masked request register

8.1.1 SPCIF_GEOMETRY

Flash/NVL geometry information

Address: 0x40110000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FLASH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	FLASH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R		R		R			
HW Access	W		W		W			
Name	FLASH_ROW [23:22]		NUM_FLASH [21:20]		SFLASH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access		None						
Name	DE_CP-D_LP	None [30:24]						

Bits	Name	Description
31	DE_CPD_LP	0': SRAM busy wait loop has not been copied. '1': Busy wait loop has been written into SRAM. Default Value: 0
23 : 22	FLASH_ROW	Page size in 64 Byte multiples (chip dependent): "0": 64 byte "1": 128 byte "2": 192 byte "3": 256 byte The page size is used to detemine the number of Bytes in a page for Flash page based operations (e.g. PGM_PAGE). Note: the field name FLASH_ROW is misleading, as this field specifies the number of Bytes in a page, rather than the number of Bytes in a row. In a single plane flash macro architecture, a page consists of a single row. However, in a multi plane flash macro architecture, a page consists of multiple rows from different planes. Default Value: Undefined

8.1.1 SPCIF_GEOMETRY (continued)

21 : 20	NUM_FLASH	Number of flash macros (chip dependent): "0": 1 flash macro "1": 2 flash macros "2": 3 flash macros "3": 4 flash macros Default Value: Undefined
19 : 16	SFLASH	Supervisory flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the supervisory flash capacity of all flash macros together: "0": 256 Bytes. "1": 2*256 Bytes. ... "15": 16*256 Bytes. Default Value: Undefined
15 : 0	FLASH	Regular flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the flash capacity of all flash macros together: "0": 256 Bytes. "1": 2*256 Bytes. ... "65535": 65536*256 Bytes. Default Value: Undefined

8.1.2 SPCIF_INTR

SPCIF interrupt request register

Address: 0x401107F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Timer counter value reaches "0". Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

8.1.3 SPCIF_INTR_SET

SPCIF interrupt set request register

Address: 0x401107F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Write INTR_SET field with '1' to set corresponding INTR field. Default Value: 0

8.1.4 SPCIF_INTR_MASK

SPCIF interrupt mask register

Address: 0x401107F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Mask for corresponding field in INTR register. Default Value: 0

8.1.5 SPCIF_INTR_MASKED

SPCIF interrupt masked request register

Address: 0x401107FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Logical and of corresponding request and mask fields. Default Value: 0

9 SRSSLT Registers

This section discusses the SRSSLT registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

9.1 SRSSLT Register Mapping Details

Register	Address	Description
PWR_CONTROL	0x40030000	Power Mode Control
PWR_KEY_DELAY	0x40030004	Power System Key&Delay Register
PWR_DDFT_SELECT	0x4003000C	Power DDFT Mode Selection Register
TST_MODE	0x40030014	Test Mode Control Register
CLK_SELECT	0x40030028	Clock Select Register
CLK_ILO_CONFIG	0x4003002C	ILO Configuration
CLK_IMO_CONFIG	0x40030030	IMO Configuration
CLK_DFT_SELECT	0x40030034	Clock DFT Mode Selection Register
WDT_DISABLE_KEY	0x40030038	Watchdog Disable Key Register
WDT_COUNTER	0x4003003C	Watchdog Counter Register
WDT_MATCH	0x40030040	Watchdog Match Register
SRSS_INTR	0x40030044	SRSS Interrupt Register
SRSS_INTR_SET	0x40030048	SRSS Interrupt Set Register
SRSS_INTR_MASK	0x4003004C	SRSS Interrupt Mask Register
RES_CAUSE	0x40030054	Reset Cause Observation Register
PWR_BG_TRIM1	0x40030F00	Bandgap Trim Register
PWR_BG_TRIM2	0x40030F04	Bandgap Trim Register
CLK_IMO_SELECT	0x40030F08	IMO Frequency Select Register
CLK_IMO_TRIM1	0x40030F0C	IMO Trim Register
CLK_IMO_TRIM2	0x40030F10	IMO Trim Register
PWR_PWRSYS_TRIM1	0x40030F14	Power System Trim Register
CLK_IMO_TRIM3	0x40030F18	IMO Trim Register

9.1.1 PWR_CONTROL

Power Mode Control

Address: 0x40030000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R			
HW Access	None		RW	RW	RW			
Name	None [7:6]		LP-M_READY	DEBUG_-SESSION	POWER_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None			R		RW	RW
HW Access	A	None			RW		R	R
Name	EXT_VCCD	None [22:20]			SPARE [19:18]		OVER_-TEMP_-THRESH	OVER_-TEMP_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	EXT_VCCD	Always write 0 except as noted below. PSoC4-S0 and MBR3 CapSense products may set this bit if Vccd is provided externally (on Vccd pin). Setting this bit turns off the active regulator and will lead to system reset (BOD) unless both Vddd and Vccd pins are supplied externally. This register bit only resets for XRES, POR, or a detected BOD. Default Value: 0
19 : 18	SPARE	Spare AHB readback bits that are hooked to PWR_PWRSYS_TRIM1.SPARE_TRIM[1:0] through spare logic equivalent to bitwise inversion. Engineering only. Default Value: 0
17	OVER_TEMP_THRESH	Over-temperature threshold. 0: TEMP_HIGH condition occurs between 120C and 125C. 1: TEMP_HIGH condition occurs between 60C and 75C (used for testing). Default Value: 0
16	OVER_TEMP_EN	Enables the die over temperature sensor. Must be enabled when using the TEMP_HIGH interrupt. Default Value: 0

9.1.1 PWR_CONTROL (continued)

5	LPM_READY	Indicates whether the low power mode regulator is ready to enter DEEPSLEEP mode. 0: If DEEPSLEEP mode is requested, device will enter SLEEP mode. When low power regulators are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP works as described. Default Value: 0
4	DEBUG_SESSION	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) Default Value: 0 **0x0: NO_SESSION :** No debug session active **0x1: SESSION_ACTIVE :** Debug session is active
3 : 0	POWER_MODE	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. Default Value: 0 **0x0: RESET :** RESET state **0x1: ACTIVE :** ACTIVE state **0x2: SLEEP :** SLEEP state **0x3: DEEP_SLEEP :** DEEP_SLEEP state

9.1.2 PWR_KEY_DELAY

Power System Key Register

Address: 0x40030004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay to wait for references to settle on wakeup from deepsleep. BOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. The default assumes the output of the predivider is 48MHz + 3%. Firmware may scale this setting according to the fastest actual clock frequency that can occur when waking from DEEPSLEEP. Default Value: 248

9.1.3 PWR_DDFT_SELECT

Power DDFT Mode Selection Register

Address: 0x4003000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DDFT1_SEL [7:4]				DDFT0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	DDFT1_SEL	Select signal for power DDFT output #1 Default Value: 0 **0x0: WAKEUP :** wakeup **0x1: AWAKE :** awake **0x2: ACT_POWER_EN :** act_power_en **0x3: ACT_POWER_UP :** act_power_up

9.1.3 PWR_DDFT_SELECT (continued)

		0x4: ACT_POWER_GOOD : act_power_good **0x5: ACT_REF_VALID :** act_ref_valid **0x6: ACT_REG_VALID :** act_reg_valid **0x7: ACT_COMP_OUT :** act_comp_out **0x8: ACT_TEMP_HIGH :** act_temp_high **0x9: DPSLP_COMP_OUT :** dpslp_comp_out **0xa: DPSLP_POWER_UP :** dpslp_power_up **0xb: AWAKE_DELAYED :** awake_delayed **0xc: LPM_READY :** lpm_ready **0xd: SLEEPHOLDACK_N :** sleepholdack_n **0xe: GND :** 1'b0 **0xf: PWR :** 1'b1
3 : 0	DDFT0_SEL	Select signal for power DDFT output #0 Default Value: 0

9.1.3 PWR_DDFT_SELECT (continued)

0x0: WAKEUP :

wakeup

0x1: AWAKE :

awake

0x2: ACT_POWER_EN :

act_power_en

0x3: ACT_POWER_UP :

act_power_up

0x4: ACT_POWER_GOOD :

act_power_good

0x5: ACT_REF_EN :

srss_adft_control_act_ref_en

0x6: ACT_COMP_EN :

srss_adft_control_act_comp_en

0x7: DPSLP_REF_EN :

srss_adft_control_dpslp_ref_en

0x8: DPSLP_REG_EN :

srss_adft_control_dpslp_reg_en

0x9: DPSLP_COMP_EN :

srss_adft_control_dpslp_comp_en

0xa: OVER_TEMP_EN :

pwr_control_over_temp_en

0xb: SLEEPHOLDREQ_N :

sleepholdreq_n

9.1.3 PWR_DDFT_SELECT (continued)

0xc: ADFT_BUF_EN :

adft_buf_en

0xd: ATPG_OBSERVE :

ATPG observe point (no functional purpose)

0xe: GND :

1'b0

0xf: PWR :

1'b1

9.1.4 TST_MODE

Test Mode Control Register

Address: 0x40030014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	
HW Access	None					RW	None	
Name	None [7:3]					SWD_CON-NECTED	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	None	RW	None			
HW Access	R	RW	None	A	None			
Name	TEST_-MODE	TEST_KEY_DFT_EN	None	BLOCK_ALT_XRES	None [27:24]			

Bits	Name	Description
31	TEST_MODE	0: Normal operation mode 1: Test mode (any test mode) Setting this bit will prevent BootROM from yielding execution to Flash image. Default Value: 0
30	TEST_KEY_DFT_EN	This bit is set when a XRES test mode key is shifted in. It is the value of the test_key_dft_en signal. When this bit is set, the BootROM will not yield execution to the FLASH image (same function as setting TEST_MODE bit below). Default Value: 0
28	BLOCK_ALT_XRES	Relevant only for parts that have the alternate XRES mechanism of overloading a GPIO pin temporarily as alternate XRES during test. When set, this bit blocks the alternate XRES function, such that the pin can be used for normal I/O or for ddft/adft observation. This register bit only resets for XRES, POR, or a detected BOD. Default Value: 0

9.1.4 TST_MODE (continued)

2	SWD_CONNECTED	0: SWD not active 1: SWD activated (Line Reset & Connect sequence passed) (Note: this bit replaces TST_CTRL.SWD_CONNECTED and is present in all M0S8 products except TSG4) Default Value: 0

9.1.5 CLK_SELECT

Clock Select Register

Address: 0x40030028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	SYSCLK_DIV [7:6]		PUMP_SEL [5:4]		HFCLK_DIV [3:2]		HFCLK_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SYSCLK_DIV	Select clk_sys prescaler value. Default Value: 0 **0x0: NO_DIV :** clk_sys= clk_hf/1 **0x1: DIV_BY_2 :** clk_sys= clk_hf/2 **0x2: DIV_BY_4 :** clk_sys= clk_hf/4 **0x3: DIV_BY_8 :** clk_sys= clk_hf/8

9.1.5 CLK_SELECT (continued)

5 : 4	PUMP_SEL	Selects clock source for charge pump clock. This clock is not guaranteed to be glitch free when changing any of its sources or settings. Default Value: 0 **0x0: GND :** No clock, connect to gnd **0x1: IMO :** Use main IMO output **0x2: HFCLK :** Use clk_hf (using selected source after predivider but before prescaler)
3 : 2	HFCLK_DIV	Selects clk_hf predivider value. Default Value: 2 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2 :** Divide selected clock source by 2 **0x2: DIV_BY_4 :** Divide selected clock source by 4 **0x3: DIV_BY_8 :** Divide selected clock source by 8
1 : 0	HFCLK_SEL	Selects a source for clk_hf and dsi_in[0]. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default Value: 0 **0x0: IMO :** IMO - Internal R/C Oscillator **0x1: EXTCLK :** EXTCLK - External Clock Pin **0x2: ECO :** ECO - External-Crystal Oscillator or PLL subsystem output

9.1.6 CLK_ILO_CONFIG

ILO Configuration

Address: 0x4003002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	ENABLE	None						

Bits	Name	Description
31	ENABLE	Master enable for ILO oscillator. This bit is hardware set whenever the WD_DISABLE_KEY is not set to the magic value. Default Value: 1

9.1.7 CLK_IMO_CONFIG

IMO Configuration

Address: 0x40030030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None						

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. Clearing this bit will disable the IMO. Don't do this if the system is running off it. Default Value: 1

9.1.8 CLK_DFT_SELECT

Clock DFT Mode Selection Register

Address: 0x40030034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	R	R		R			
Name	None	DFT_EDGE0	DFT_DIV0 [5:4]		DFT_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW		RW			
HW Access	None	R	R		R			
Name	None	DFT_EDGE1	DFT_DIV1 [13:12]		DFT_SEL1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	DFT_EDGE1	Edge sensitivity for in-line divider on output #1 (only relevant when DIV1>0). Default Value: 0 **0x0: POSEDGE :** Use posedge for divider **0x1: NEGEDGE :** Use negedge for divider
13 : 12	DFT_DIV1	DFT Output Divide Down. Default Value: 0 **0x0: NO_DIV :** Direct Output

9.1.8 CLK_DFT_SELECT (continued)

		0x1: DIV_BY_2 : Divide by 2 **0x2: DIV_BY_4 :** Divide by 4 **0x3: DIV_BY_8 :** Divide by 8
11 : 8	DFT_SEL1	Select signal for DFT output #1 Default Value: 0 **0x0: NC :** Disabled - output is 0 **0x1: ILO :** clk_ilo: ILO output **0x2: IMO :** clk_imo: IMO primary output **0x3: ECO :** clk_eco: ECO output **0x4: EXTCLK :** clk_ext: external clock input **0x5: HFCLK :** clk_hf: root of the high-speed clock tree **0x6: LFCLK :** clk_lf: root of the low-speed clock tree **0x7: SYSCLK :** clk_sys: root of the CPU/AHB clock tree (gated version of clk_hf) **0x8: PUMPCLK :** clk_pump: clock provided to charge pumps in FLASH and PA

9.1.8 CLK_DFT_SELECT (continued)

		0x9: SLPCTRLCLK : clk_slpctrl: clock provided to SleepController
6	DFT_EDGE0	Edge sensitivity for in-line divider on output #0 (only relevant when DIV0>0). Default Value: 0 **0x0: POSEDGE :** Use posedge for divider **0x1: NEGEDGE :** Use negedge for divider
5 : 4	DFT_DIV0	DFT Output Divide Down. Default Value: 0 **0x0: NO_DIV :** Direct Output **0x1: DIV_BY_2 :** Divide by 2 **0x2: DIV_BY_4 :** Divide by 4 **0x3: DIV_BY_8 :** Divide by 8
3 : 0	DFT_SEL0	Select signal for DFT output #0 Default Value: 0 **0x0: NC :** Disabled - output is 0 **0x1: ILO :** clk_ilo: ILO output **0x2: IMO :** clk_imo: IMO primary output **0x3: ECO :** clk_eco: ECO output

9.1.8 CLK_DFT_SELECT (continued)

0x4: EXTCLK :

clk_ext: external clock input

0x5: HFCLK :

clk_hf: root of the high-speed clock tree

0x6: LFCLK :

clk_lf: root of the low-speed clock tree

0x7: SYSCLK :

clk_sys: root of the CPU/AHB clock tree (gated version of clk_hf)

0x8: PUMPCLK :

clk_pump: clock provided to charge pumps in FLASH and PA

0x9: SLPCTRLCLK :

clk_slpctrl: clock provided to SleepController

9.1.9 WDT_DISABLE_KEY

Watchdog Disable Key Register

Address: 0x40030038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Disables WDT reset when equal to 0xACED8865. The WDT reset functions normally for any other setting. Default Value: 0

9.1.10 WDT_COUNTER

Watchdog Counter Register

Address: 0x4003003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	Current value of WDT Counter Default Value: 0

9.1.11 WDT_MATCH

Watchdog Match Register

Address: 0x40030040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				IGNORE_BITS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	IGNORE_BITS	The number of MSB bits of the watchdog timer that are NOT checked against MATCH. This value provides control over the time-to-reset of the watchdog (which happens after 3 successive matches). Note that certain products may enforce a minimum value for this register through design time configuration. Default Value: 0
15 : 0	MATCH	Match value for Watchdog counter. Every time WDT_COUNTER reaches MATCH an interrupt is generated. Two unserviced interrupts will lead to a system reset (i.e. at the third match). Default Value: 4096

9.1.12 SRSS_INTR

SRSS Interrupt Register

Address: 0x40030044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						TEMP_HIGH	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	TEMP_HIGH	Regulator over-temp interrupt. This interrupt can occur when a short circuit exists on the vccd pin or when extreme loads are applied on IO-cells causing the die to overheat. Firmware is encourage to shutdown all IO cells and then go to DeepSleep mode when this interrupt occurs if protection against such conditions is desired. Default Value: 0
0	WDT_MATCH	WDT Interrupt Request. This bit is set each time WDT_COUNTR==WDT_MATCH. Clearing this bit also feeds the watch dog. Missing 2 interrupts in a row will generate brown-out reset. Due to internal synchronization, it takes 2 SYSCLK cycles to update after a W1C. Default Value: 0

9.1.13 SRSS_INTR_SET

SRSS Interrupt Set Register

Address: 0x40030048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	None
HW Access	None						A	None
Name	None [7:2]						TEMP_HIGH	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	TEMP_HIGH	Writing 1 to this bit internally sets the overtemp interrupt. This can be observed by reading SRSS_INTR.TEMP_HIGH. This bit always reads back as zero. Default Value: 0

9.1.14 SRSS_INTR_MASK

SRSS Interrupt Mask Register

Address: 0x4003004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						TEMP_HIGH	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	TEMP_HIGH	Masks REG_OVERTEMP interrupt Default Value: 0
0	WDT_MATCH	Clearing this bit will not forward the interrupt to the CPU. It will not, however, disable the WDT reset generation on 2 missed interrupts. Default Value: 0

9.1.15 RES_CAUSE

Reset Cause Observation Register

Address: 0x40030054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	None		RW1C
HW Access	None			A	A	None		A
Name	None [7:5]			RESET_SOFT	RESET_PROT_FAULT	None [2:1]		RESET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESET_SOFT	Cortex-M0 requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. Default Value: 0
3	RESET_PROT_FAULT	A protection violation occurred that requires a RESET. This includes, but is not limited to, hitting a debug breakpoint while in Privileged Mode. Default Value: 0
0	RESET_WDT	A WatchDog Timer reset has occurred since last power cycle. Default Value: 0

9.1.16 PWR_BG_TRIM1

Bandgap Trim Register

Address: 0x40030F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		REF_VTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	REF_VTRIM	Trims the bandgap reference voltage output. Used to trim the VBG to the voltage where its temperature curvature is minimal. Bit [5] is unused within the bandgap block. Default Value: 16

9.1.17 PWR_BG_TRIM2

Bandgap Trim Register

Address: 0x40030F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		REF_ITRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	REF_ITRIM	Trims the bandgap reference current output. Used to trim the IBG to the voltage where its temperature curvature is minimal. Default Value: 28

9.1.18 CLK_IMO_SELECT

IMO Frequency Select Register

Address: 0x40030F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					FREQ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	FREQ	Select operating frequency Default Value: 0 **0x0: 24_MHZ :** IMO runs at 24 MHz **0x1: 28_MHZ :** IMO runs at 28 MHz **0x2: 32_MHZ :** IMO runs at 32 MHz **0x3: 36_MHZ :** IMO runs at 36 MHz

9.1.18 CLK_IMO_SELECT (continued)

0x4: 40_MHZ :

IMO runs at 40 MHz

0x5: 44_MHZ :

IMO runs at 44 MHz

0x6: 48_MHZ :

IMO runs at 48 MHz

9.1.19 CLK_IMO_TRIM1

IMO Trim Register

Address: 0x40030F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. This field is hardware updated during USB osclock mode. This field is mapped to the most significant bits of the IMO trim imo_clk_trim[10:3]. The step size of 1 LSB on this field is approximately 120 kHz. Default Value: 128

9.1.20 CLK_IMO_TRIM2

IMO Trim Register

Address: 0x40030F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					RW		
Name	None [7:3]					FSOFFSET [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	FSOFFSET	Frequency trim bits. These bits are not trimmed during manufacturing and kept at 0 under normal operation. This field is hardware updated during USB osclock mode. This field is mapped to the least significant bits of the IMO trim imo_clk_trim[2:0]. The step size of 1 LSB on this field is approximately 15 kHz. Default Value: 0

9.1.21 PWR_PWRSYS_TRIM1

Power System Trim Register

Address: 0x40030F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SPARE_TRIM [7:4]				DPSLP_REF_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SPARE_TRIM	Active-Reference temperature compensation trim (repurposed from spare bits). Bits [7:6] - trim the Active-Reference IREF temperature coefficient (TC). 00: TC = 0 (unchanged) 01: TC = +80ppm/C 10: TC = -80ppm/C 11: TC = -150ppm/C Bits [5:4] - trim the Active-Reference VREF temperature coefficient (TC). 00: TC = 0 (unchanged) 01: TC = -50ppm/C 10: TC = -80ppm/C 11: TC = +150ppm/C Default Value: 0
3 : 0	DPSLP_REF_TRIM	Trims the DeepSleep reference that is used by the DeepSleep regulator and DeepSleep power comparator. Default Value: 0

9.1.22 CLK_IMO_TRIM3

IMO Trim Register

Address: 0x40030F18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

10 TCPWM Registers

This section discusses the TCPWM registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

10.1 TCPWM Register Mapping Details

Register	Address	Description
TCPWM_CTRL	0x40050000	TCPWM control register 0.
TCPWM_CMD	0x40050008	TCPWM command register.
TCPWM_INTR_CAUSE	0x4005000C	TCPWM Counter interrupt cause register.
TCPWM_CNT0_CTRL	0x40050100	Counter control register
TCPWM_CNT0_STATUS	0x40050104	Counter status register
TCPWM_CNT0_COUNTER	0x40050108	Counter count register
TCPWM_CNT0_CC	0x4005010C	Counter compare/capture register
TCPWM_CNT0_CC_BUFF	0x40050110	Counter buffered compare/capture register
TCPWM_CNT0_PERIOD	0x40050114	Counter period register
TCPWM_CNT0_PERIOD_BUFF	0x40050118	Counter buffered period register
TCPWM_CNT0_TR_CTRL0	0x40050120	Counter trigger control register 0
TCPWM_CNT0_TR_CTRL1	0x40050124	Counter trigger control register 1
TCPWM_CNT0_TR_CTRL2	0x40050128	Counter trigger control register 2
TCPWM_CNT0_INTR	0x40050130	Interrupt request register.
TCPWM_CNT0_INTR_SET	0x40050134	Interrupt set request register.
TCPWM_CNT0_INTR_MASK	0x40050138	Interrupt mask register.
TCPWM_CNT0_INTR_MASKED	0x4005013C	Interrupt masked request register

10.1.1 TCPWM_CTRL

TCPWM control register 0.

Address: 0x40050000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							COUNTER_ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	COUNTER_ENABLED	Counter enables for counters 0 up to CNT_NR-1. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_CTRL0, TR_CTRL1, and TR_CTRL2 register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_overflow", "tr_underflow" and "tr_compare_match"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0

10.1.2 TCPWM_CMD

TCPWM command register.

Address: 0x40050008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							COUNTER_CAPTURE

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [15:9]							COUNTER_RELOAD

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [23:17]							COUNTER_STOP

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [31:25]							COUNTER_START

Bits	Name	Description
24	COUNTER_START	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
16	COUNTER_STOP	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
8	COUNTER_RELOAD	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
0	COUNTER_CAPTURE	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'. Default Value: 0

10.1.3 TCPWM_INTR_CAUSE

TCPWM Counter interrupt cause register.

Address: 0x4005000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							COUNTER_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	COUNTER_INT	Counters interrupt signal active. If the counter is disabled through CTRL.COUNTER_ENABLED, the associated interrupt field is immediately set to '0'. Default Value: 0

10.1.4 TCPWM_CNT0_CTRL

Counter control register

Address: 0x40050100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER :** Timer mode **0x2: CAPTURE :** Capture mode **0x3: QUAD :** Quadrature encoding mode

10.1.4 TCPWM_CNT0_CTRL (continued)

		0x4: PWM : Pulse width modulation (PWM) mode **0x5: PWM_DT :** PWM with deadtime insertion mode **0x6: PWM_PR :** Pseudo random pulse width modulation
21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1 :** X1 encoding (QUAD mode) **0x1: X2 :** X2 encoding (QUAD mode) **0x2: X4 :** X4 encoding (QUAD mode)
		0x1: INV_OUT : When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: INV_COMPL_OUT :** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP :** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD.

10.1.4 TCPWM_CNT0_CTRL (continued)

		0x1: COUNT_DOWN : Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1 :** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2 :** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4 :** Divide by 4 (other-than-PWM_DT mode) **0x3: DIVBY8 :** Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16 :** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32 :** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64 :** Divide by 64 (other-than-PWM_DT mode)

10.1.4 TCPWM_CNT0_CTRL (continued)

		0x7: DIVBY128 : Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

10.1.5 TCPWM_CNT0_STATUS

Counter status register

Address: 0x40050104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

10.1.6 TCPWM_CNT0_COUNTER

Counter count register

Address: 0x40050108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

10.1.7 TCPWM_CNT0_CC

Counter compare/capture register

Address: 0x4005010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

10.1.8 TCPWM_CNT0_CC_BUFF

Counter buffered compare/capture register

Address: 0x40050110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

10.1.9 TCPWM_CNT0_PERIOD

Counter period register

Address: 0x40050114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

10.1.10 TCPWM_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x40050118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

10.1.11 TCPWM_CNT0_TR_CTRL0

Counter trigger control register 0

Address: 0x40050120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

10.1.11 TCPWM_CNT0_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

10.1.12 TCPWM_CNT0_TR_CTRL1

Counter trigger control register 1

Address: 0x40050124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event.

10.1.12 TCPWM_CNT0_TR_CTRL1 (continued)

		0x3: NO_EDGE_DET : No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event.

10.1.12 TCPWM_CNT0_TR_CTRL1 (continued)

		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.

10.1.13 TCPWM_CNT0_TR_CTRL2

Counter trigger control register 2

Address: 0x40050128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert

10.1.13 TCPWM_CNT0_TR_CTRL2 (continued)

		0x3: NO_CHANGE : No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change

10.1.14 TCPWM_CNT0_INTR

Interrupt request register.

Address: 0x40050130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

10.1.15 TCPWM_CNT0_INTR_SET

Interrupt set request register.

Address: 0x40050134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.16 TCPWM_CNT0_INTR_MASK

Interrupt mask register.

Address: 0x40050138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.17 TCPWM_CNT0_INTR_MASKED

Interrupt masked request register

Address: 0x4005013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

11 ROM Table Registers

This section discusses the ROM Table registers. It lists all the registers in mapping tables, in address order.

11.1 Register Details

Register	Address	Description
ROMTABLE_ADDR	0xF0000000	Link to Cortex M0 ROM Table.
ROMTABLE_DID	0xF0000FCC	Device Type Identifier register.
ROMTABLE_PID4	0xF0000FD0	Peripheral Identification Register 4.
ROMTABLE_PID5	0xF0000FD4	Peripheral Identification Register 5.
ROMTABLE_PID6	0xF0000FD8	Peripheral Identification Register 6.
ROMTABLE_PID7	0xF0000FDC	Peripheral Identification Register 7.
ROMTABLE_PID0	0xF0000FE0	Peripheral Identification Register 0.
ROMTABLE_PID1	0xF0000FE4	Peripheral Identification Register 1.
ROMTABLE_PID2	0xF0000FE8	Peripheral Identification Register 2.
ROMTABLE_PID3	0xF0000FEC	Peripheral Identification Register 3.
ROMTABLE_CID0	0xF0000FF0	Component Identification Register 0.
ROMTABLE_CID1	0xF0000FF4	Component Identification Register 1.
ROMTABLE_CID2	0xF0000FF8	Component Identification Register 2.
ROMTABLE_CID3	0xF0000FFC	Component Identification Register 3.

11.1.1 ROMTABLE_ADDR

Link to Cortex M0 ROM Table.

Address: 0xF0000000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						R	R
Name	None [7:2]						FOR-MAT_32BIT	PRESENT

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	R				None			
Name	ADDR_OFFSET [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [31:24]							

Bits	Name	Description
31 : 12	ADDR_OFFSET	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. Default Value: 983295
1	FORMAT_32BIT	ROM Table format: '0: 8-bit format. '1': 32-bit format. Default Value: 1
0	PRESENT	Entry present. Default Value: 1

11.1.2 ROMTABLE_DID

Device Type Identifier register.

Address: 0xF0000FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 1

11.1.3 ROMTABLE_PID4

Peripheral Identification Register 4.

Address: 0xF0000FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	COUNT	Size of ROM Table is 2^COUNT * 4 KByte. Default Value: 0
3 : 0	JEP_CONTINUATION	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. Default Value: Undefined

11.1.4 ROMTABLE_PID5

Peripheral Identification Register 5.

Address: 0xF0000FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

11.1.5 ROMTABLE_PID6

Peripheral Identification Register 6.

Address: 0xF0000FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

11.1.6 ROMTABLE_PID7

Peripheral Identification Register 7.

Address: 0xF0000FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

11.1.7 ROMTABLE_PID0

Peripheral Identification Register 0.

Address: 0xF0000FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PN_MIN	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. These part numbers are maintained in spec 40-9500. Default Value: Undefined

11.1.8 ROMTABLE_PID1

Peripheral Identification Register 1.

Address: 0xF0000FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	JEPID_MIN	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. This number is maintained in spec 40-9500. Default Value: Undefined
3 : 0	PN_MAJ	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. These part numbers are maintained in spec 40-9500. Default Value: Undefined

11.1.9 ROMTABLE_PID2

Peripheral Identification Register 2.

Address: 0xF0000FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R		
HW Access	R				None	R		
Name	REV [7:4]				None	JEPID_MAJ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV	Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is implemented in RTL by an ECO-able tie-off structure and is incremented on subsequent tape outs. Default Value: Undefined
2 : 0	JEPID_MAJ	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. This number is maintained in spec 40-9500. Default Value: Undefined

11.1.10 ROMTABLE_PID3

Peripheral Identification Register 3.

Address: 0xF0000FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV_AND	Minor REVision number (chip specific). For first tape out: 0x1. This field is implemented in RTL by an ECO-able tie-off structure and is incremented on subsequent tape outs. Default Value: Undefined
3 : 0	CM	Customer modified field. This field is used to track modifications to the original component design as a result of componenet IP reuse. Default Value: 0

11.1.11 ROMTABLE_CID0

Component Identification Register 0.

Address: 0xF0000FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 0 of 4-byte component identification 0xB105:100D. Default Value: 13

11.1.12 ROMTABLE_CID1

Component Identification Register 1.

Address: 0xF0000FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: "ROM Table". Default Value: 16

11.1.13 ROMTABLE_CID2

Component Identification Register 2.

Address: 0xF0000FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 2 of 4-byte component identification 0xB105:100D. Default Value: 5

11.1.14 ROMTABLE_CID3

Component Identification Register 3.

Address: 0xF0000FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 3 of 4-byte component identification 0xB105:100D. Default Value: 177

Revision History

Revision History

Document Title: PSoC 4000 Family PSoC 4 Registers Technical Reference Manual (TRM) Document Number: 001-90002			
Revision	**ECN#**	**Issue Date**	**Description of Change**
**	4186400	11/11/13	Specification for new silicon.
*A	4316501	04/10/14	Updated the clock divider descriptions in Clock trim and peripheral divider registers. Updated the IO select description of HSIOM registers. Updated SFLASH Registers.
*B	4994464	10/29/2015	Register addresses were updated to sync with PSoC Creator
*C	5515549	11/10/2016	No content update; sunset review
*D	5760861	06/02/2017	Updated logo and copyright information
*E	6509576	03/15/2019	Document size optimized. Removed “CapSense” Chapter
*F	8047856	08/05/2024	Added hyperlink in “Register Mapping” on page 8.