PSOC™ Edge E8x2, E8x3, E8x5, E8x6 registers

Reference manual

About this document

Scope and purpose

The reference manual lists all the registers in the mapping tables of the PSOC™ Edge E8x2, E8x3, E8x5, and E8x6 registers in address order.
For architecture details, see PSOC™ Edge E8x2, E8x3, E8x5, E8x6 architecture reference manual.

Intended audience

This reference manual is intended for the embedded hardware engineers, software developers, and system architects who want to understand the register details of the Infineon PSOC™ Edge E8x2, E8x3, E8x5, and E8x6 series of microcontrollers.

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Register mapping

The Register mapping section discusses the registers of the PSOC™ Edge devices. This document should be used in conjunction with PSOC™ Edge E8x2, E8x3, E8x5, E8x6 architecture reference manual. Register mapping section lists all the registers in mapping tables, in address order.

Register general conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Description	Explanation
RW	Read/Write	These bits can be both read and written.
R	Read only	These bits can only be read. Writing has no effect on the bit value.
W	Write only	These bits can only be written. Reading the bit returns the reset value.
RW1C	Read/Write ‘1’ to clear	These bits can be read as well as cleared by writing ‘1’. Writing ‘0’ has no effect on the bit value.
RW0C	Read/Write ‘0’ to clear	These bits can be read as well as cleared by writing ‘0’. Writing ‘1’ has no effect on the bit value.
RW1S	Read/Write ‘1’ to set	These bits can be read as well as set by writing ‘1’. Writing ‘0’ has no effect on the bit value.
A	Alias	This register is an additional alias or another register. This convention is used when a physical register is mapped to multiple addresses, typically for firmware debug purposes. See the corresponding register descriptions for more details.
None / Reserved	Reserved bits	Keep these bits at the default value
‘x’ in a register /bit field name	Multiple instances	Multiple instances/address ranges of the same register/bit field

Acronyms

This table lists the acronyms used in this document.

Table 1 Acronyms

Symbol	Unit of measure
ACG	Access Control Gating
ADC	Analog-to-Digital Converters
AES	Advanced Encryption Standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
AIRCR	Application Interrupt and Reset Control Register
AIU	Application Interface Unit
APBIC	Advanced Peripheral Bus Interconnect
APPCPUSS	Application CPU Subsystem

Acronyms

Table 1 Acronyms

Symbol	Unit of measure
ASC	Asynchronous Serial Communication
ASIC	Application Specific Integrated Circuit
ATB	Advanced Trace Bus
AUTOSAR	Automotive Open System Architecture
AXI	Advanced Extensible Interface
BLE	Bluetooth Low Energy
BNA	Buffer Not Available
BOD	Brownout Detect
BREG	Backup Register
BRESP	AXI Write Transaction Response Signal
BT	Bluetooth
C-AHB	Code AHB Interface
CAN-FD	Controller Area Network Flexible Data-rate
CBOR	Concise Binary Object Representation
CBS	Credit Base Shaping
CBS	Credit-Based Shaping
CCC	Common Command Code
CDR	Clock Data Recovery
CFI	Canonical Format Indicator
CIC	Cascaded Integrator Comb
CMD_RESP	Command Response
CMOS	Complementary Metal-Oxide Semiconductor
CoT	Chain of Trust
CPHA	Clock Phase
CPOL	Clock Polarity
CPU	Central Processing Unit
CQE	Command Queue Engine
CRC	Cyclic Redundancy Checker
CSV	Clock Supervision
CTB	Continuous Time Block
CTB	Continuous Time Block (Opamp Circuits)
CTI	Cross Trigger Interface
CTM	Cross Trigger Matrix
D-Cache	Data Cache
D-PHY	MIPI Physical layer standard used for MIPI DSI and CSI
DAA	Dynamic Address Allocation
DAP	Debug Access Port
DAR	Disable automatic retransmission

Acronyms

Table 1 Acronyms

Symbol	Unit of measure
DBI	Display Bus Interface
DBTP	Data Bit Timing and Prescaler Register
DCR	Device Characteristics Register
DDR	Double Data Rate
DE	Data Enable
DEMCR	Debug Exception and Monitor Control Register
DES	Data Encryption Standard
DHCSR	Debug Halting Control and Status Register
DICE	Device Identifier Composition Engine
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DP	Debug Port
DPI	Display Pixel Interface
DPLL	Digital Phase Locked Loop
DPU	Display Processor Unit
DSI	Digital Serial Interface (Usually in relation to MIPI DSI)
DSP	Digital Signal Processing
DTCM	Data Tightly Coupled Memory
DU	Data unit
DW	Data Wire
DWRR	Deficit Weighted Round Robin
E2E	End-to-End
ECC	Error Correcting Code
ECO	External Crystal Oscillator
ECT	Embedded Cross Triggering
EDC	Error Detection and Correction
EFEC	Extended Filter Elements Configuration
Em_EEPROM	Emulated Electrically Erasable Programmable Read-only Memory
EMAC	Ethernet Media Access Controller
eMMC	Embedded Multimedia Card
EOL	End of List
EOPF	End-of-Periodic-Frame Boundary
EP	Endpoint
ESD	Electrostatic Discharge
ETB	Embedded Trace Buffer
ETF	Embedded Trace Fifo
ETM	Embedded Trace Macrocell
ETS	Enhanced Transmission Selection

Acronyms

Table 1 Acronyms

Symbol	Unit of measure
FCS	Frame Check Sequence
FIFO	First In First Out
FIH	Fault Injection Hardening
FIR	Finite Impulse Response
FPU	Floating Point Unit
FS	Full Speed
GFC	Global Filter Configuration
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HAR	Human Activity Recognition
HCI	Host Controller Interface
HDR	High Date Rate
Hi-Z	High Impedance
HJ	Hot-Join
HPDMA	High Performance Direct Memory Access
HSIOM	High Speed I/O Matrix
HSM	Hardware Security Module
HUK	Hardware Unique Key
HV	High Voltage
I-Cache	Instruction Cache
I/O	Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound Bus
I3C	Improved Inter-Integrated Circuit
IBI	In-band Interrupts
ICER	Interrupt Clear Enable Register
IDAU	Implementation Defined Attribution Unit
IMO	Internal Main Oscillator
IOC	Interrupt on Complete
IP	Internet Protocol
IPC	Inter Processor Communication
IRQ	Interrupt Request
ISB	Instruction Synchronization Barrier
ISER	Interrupt Set Enable Register
ISR	Interrupt Service Routine
ITCM	Instructions Tightly Coupled Memory
ITM	Instrumentation Trace Macrocell
ITNS	Interrupt Target Non-secure

Acronyms

Table 1 Acronyms

Symbol	Unit of measure
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LCS	Life Cycle State
LIN	Local Interconnect Network
LLDP	Link Layer Discovery Protocol
LP	Low Power
LPCOMP	Low-Power Comparator
LPI	Low Power Idle
LPM	Link Power Management
LS	Low Speed
LSB	Least significant Byte
LUT	Look-up Table
LVD	Low Voltage Detector
LVTTL	Low Voltage Transistor-Transistor Logic
M_TTCAN	Time-Triggered CAN Module
M-AXI	Master AXI Interface
MAC	Media Access Control
MCU	Microcontroller Unit
MCWDT	Multi-counter Watchdog Timer
MDC	MDIO interface clock
MDIO	Management Data Input/Output
MII	Media-Independent Interface
MIPI	Mobile Industry Processor Interface
MISO	Master-in-slave-out
ML	Machine Learning
MMIO	Memory-mapped I/O
MNR	Message Number
MOSI	Master-out-slave-in
MPC	Memory Protection Controller
MPU	Memory Protection Unit
MR	Master Request
MRAM	Message RAM
MRL	Maximum Read Length
MSB	Most significant Byte
MSC	Master Security Controller
MSP	Main Stack Pointer
MTQ	Minimum Time Quanta
MVE	M-profile Vector Extension

Acronyms

Table 1 Acronyms

Symbol	Unit of measure
MWL	Maximum Write Length
NBTP	Nominal Bit Timing and Prescaler Register
NMI	Non-maskable Interrupt
NN	Neural Network
NPU	Neural Processing Unit
NTU	Network Time Unit
NVIC	Nested Vectored Interrupt Controller
NVM	Non-Volatile Memory
OEM	Original Equipment Manufacturer
OPC	Opcode
OTP	One-Time-Programmable Memory
OVD	Over Voltage Detector
OVP	Over Voltage Protection
OVT	Over Voltage Tolerant
P-AHB	Peripheral AHB Interface
P2P	Peer-to-Peer
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PEC	Packet Error Check
PendSV	Pending Supervisory
PHY	Ethernet Physical (transceiver component)
PID	Product Identification
PILO	Precision Internal Low-speed Oscillator
PKC	Public-Key Cryptography
PLL	Phase Locked Loop
POR	Power-on Reset
PPB	Private Peripheral Bus
PPC	Peripheral Protection Controller
PPU	Power Policy Unit
PRB	Programmable Reference Block
PRNG	Pseudo Random Number Generator
PSA	Platform Security Architecture
PSP	Process Stack Pointer
PSR	Program and Status Register
PSRR	Power Supply Rejection Ratio
PTComp	Programmable Threshold Comparator
PTM	Pulse Time Modulation
PTP	Precision Time Protocol

Acronyms

Table 1 Acronyms

Symbol	Unit of measure
PWM	Pulse-Width Modulation
RMII	Reduced Media-Independent Interface
RoT	Root of Trust
RRAM	Resistive Random Access Memory
RRESP	AXI Read Transaction Response Signal
RTC	Real-Time Clock
RTOS	Real-time Operating System
RWDS	Read-Write-Data-Strobe
RX	Receive
RZWI	Read Zero Write Ignore
S-AHB	Slave AHB Interface
SAR	Successive-Approximation-Register
SAU	Secure Attribution Unit
SCB	Serial Communication Block
SCL	Serial Clock
SDA	Serial Data
SDHC	Secure Digital Host Controller
SDIO	Secure Digital Input Output
SDR	Single Data Rate
SESIP	Security Evaluation Standard for IoT Platforms
SFD	Start Frame Delimiter
SFEC	Standard Filter Element Configuration
SFR	Special Function Register
SHA	Secure Hash Algorithm
SHCSR	System Handler Control and State Register
SHPR	System Handler Priority Registers
SIDFC	Standard ID Filter Configuration
SIMD	Single Instruction/Multiple Data
SIO	Special Input/Output
SIR	Slave Interrupt Request
SMI	Serial Management Interface
SMIF	Serial Memory Interface
SNAP	Subnetwork Access Protocol
SoC	System on Chip
SoCMEM	System On Chip Memory
SOF	Start of Frame
SPI	Serial Peripheral Interface
SPRAM	Single Port RAM

Acronyms

Table 1 Acronyms

Symbol	Unit of measure
SRAM	Static Random Access Memory
SRAMC	Static Random Access Memory Controller
SROM	Supervisory Read Only Memory
SRSS	System Resources Sub System
STT	State-Transition Table
SVCall	Supervisory Call
SWD	Serial Wire Debug
SWO	Serial Wire Output
SWV	Serial Wire Viewer
SYSCPUSS	System CPU Subsystem
TAP	Test Access Port
TCK	Test Clock
TCP/IP	Transmission Control Protocol/Internet Protocol
TCPWM	Timer/Counter Pulse-Width Modulator
TDES	Triple Data Encryption Standard
TDI	Test Data In
TDM	Time-Division Multiplexing
TDO	Test Data Out
TM	Time Mark
TMEX	Time Mark Event External
TMIN	Time Mark Event Internal
TMS	Test Mode Select
TPA	Trace Port Analyzer
TPIU	Trace Port Interface Unit
TRN	Turnaround Period
TRNG	True Random Number Generator
TSU	Timestamp Unit
TTCAN	Time-Triggered CAN
TTL	Transistor-Transistor Logic
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
UDP	User Datagram Protocol
ULP	Ultra Low Power
USB CTRL	USB Controller
USB OTG	USB On-The-Go
USB PHY	USB Physical Layer
USBHSSS	Universal Serial Bus High Speed Subsystem
UTMI	USB Transceiver Macrocell Interface

Acronyms

Table 1 Acronyms

Symbol	Unit of measure
VLAN	Virtual Local Area Network
VREG	Voltage Regulator
VTG	Video Timing Generation
VTOR	Vector Table Offset Register
VU	Vector Unit
WDR	Watchdog Reset
WDT	Watchdog Timer
WFE	Wait For Event
WFI	Wait For Interrupt
WIC	Wakeup Interrupt Controller
WWD	Wake Word Detection
XIDAM	Extended ID AND Mask
XIDFC	Extended ID Filter Configuration
XIP	Execute-In-Place
XN	Execute Never
XRES	External Reset

1 CPU Sub System (CPUSS) registers

This section discusses the CPUSS registers. It lists all the registers in mapping tables, in address order.

1.1 Register details

Register name	Address	Description
RAMC_PPU0_PWPR	0x42220000	Power Policy Register
RAMC_PPU0_PMER	0x42220004	Power Mode Emulation Register
RAMC_PPU0_PWSR	0x42220008	Power Status Register
RAMC_PPU0_DISR	0x42220010	Device Interface Input Current Status Register
RAMC_PPU0_MISR	0x42220014	Miscellaneous Input Current Status Register
RAMC_PPU0_STSR	0x42220018	Stored Status Register
RAMC_PPU0_UNLK	0x4222001C	Unlock register
RAMC_PPU0_PWCR	0x42220020	Power Configuration Register
RAMC_PPU0_PTCR	0x42220024	Power Mode Transition Configuration Register
RAMC_PPU0_IMR	0x42220030	Interrupt Mask Register
RAMC_PPU0_AIMR	0x42220034	Additional Interrupt Mask Register
RAMC_PPU0_ISR	0x42220038	Interrupt Status Register
RAMC_PPU0_AISR	0x4222003C	Additional Interrupt Status Register
RAMC_PPU0_IESR	0x42220040	Input Edge Sensitivity Register
RAMC_PPU0_OPSR	0x42220044	Operating Mode Active Edge Sensitivity Register
RAMC_PPU0_FUNRR	0x42220050	Functional Retention RAM Configuration Register
RAMC_PPU0_FULRR	0x42220054	Full Retention RAM Configuration Register
RAMC_PPU0_MEMRR	0x42220058	Memory Retention RAM Configuration Register
RAMC_PPU0_EDTR0	0x42220160	Power Mode Entry Delay Register 0
RAMC_PPU0_EDTR1	0x42220164	Power Mode Entry Delay Register 1
RAMC_PPU0_DCDR0	0x42220170	Device Control Delay Configuration Register 0
RAMC_PPU0_DCDR1	0x42220174	Device Control Delay Configuration Register 1
RAMC_PPU0_IDR0	0x42220FB0	PPU Identification Register 0
RAMC_PPU0_IDR1	0x42220FB4	PPU Identification Register 1
RAMC_PPU0_IIDR	0x42220FC8	Implementation Identification Register
RAMC_PPU0_AIDR	0x42220FCC	Architecture Identification Register
RAMC_PPU0_PID4	0x42220FD0	Implementation Defined Identification Register (PID4)
RAMC_PPU0_PID0	0x42220FE0	Implementation Defined Identification Register (PID0)
RAMC_PPU0_PID1	0x42220FE4	Implementation Defined Identification Register (PID1)
RAMC_PPU0_PID2	0x42220FE8	Implementation Defined Identification Register (PID2)

CPU Sub System (CPUSS) registers

Register name	Address	Description
RAMC_PPU0_PID3	0x42220FEC	Implementation Defined Identification Register (PID3)
RAMC_PPU0_ID0	0x42220FF0	Implementation Defined Identification Register (ID0)
RAMC_PPU0_ID1	0x42220FF4	Implementation Defined Identification Register (ID1)
RAMC_PPU0_ID2	0x42220FF8	Implementation Defined Identification Register (ID2)
RAMC_PPU0_ID3	0x42220FFC	Implementation Defined Identification Register (ID3)
RAMC_PPU1_PWPR	0x42221000	Power Policy Register. See RAMC_PPU0_PWPR for the details of bit fields.
RAMC_PPU1_PMER	0x42221004	Power Mode Emulation Register. See RAMC_PPU0_PMER for the details of bit fields.
RAMC_PPU1_PWSR	0x42221008	Power Status Register. See RAMC_PPU0_PWSR for the details of bit fields.
RAMC_PPU1_DISR	0x42221010	Device Interface Input Current Status Register. See RAMC_PPU0_DISR for the details of bit fields.
RAMC_PPU1_MISR	0x42221014	Miscellaneous Input Current Status Register. See RAMC_PPU0_MISR for the details of bit fields.
RAMC_PPU1_STSR	0x42221018	Stored Status Register. See RAMC_PPU0_STSR for the details of bit fields.
RAMC_PPU1_UNLK	0x4222101C	Unlock register. See RAMC_PPU0_UNLK for the details of bit fields.
RAMC_PPU1_PWCR	0x42221020	Power Configuration Register. See RAMC_PPU0_PWCR for the details of bit fields.
RAMC_PPU1_PTCR	0x42221024	Power Mode Transition Configuration Register. See RAMC_PPU0_PTCR for the details of bit fields.
RAMC_PPU1_IMR	0x42221030	Interrupt Mask Register. See RAMC_PPU0_IMR for the details of bit fields.
RAMC_PPU1_AIMR	0x42221034	Additional Interrupt Mask Register. See RAMC_PPU0_AIMR for the details of bit fields.
RAMC_PPU1_ISR	0x42221038	Interrupt Status Register. See RAMC_PPU0_ISR for the details of bit fields.
RAMC_PPU1_AISR	0x4222103C	Additional Interrupt Status Register. See RAMC_PPU0_AISR for the details of bit fields.
RAMC_PPU1_IESR	0x42221040	Input Edge Sensitivity Register. See RAMC_PPU0_IESR for the details of bit fields.
RAMC_PPU1_OPSR	0x42221044	Operating Mode Active Edge Sensitivity Register. See RAMC_PPU0_OPSR for the details of bit fields.
RAMC_PPU1_FUNRR	0x42221050	Functional Retention RAM Configuration Register. See RAMC_PPU0_FUNRR for the details of bit fields.

CPU Sub System (CPUSS) registers

Register name	Address	Description
RAMC_PPU1_FULRR	0x42221054	Full Retention RAM Configuration Register. See RAMC_PPU0_FULRR for the details of bit fields.
RAMC_PPU1_MEMRR	0x42221058	Memory Retention RAM Configuration Register. See RAMC_PPU0_MEMRR for the details of bit fields.
RAMC_PPU1_EDTR0	0x42221160	Power Mode Entry Delay Register 0. See RAMC_PPU0_EDTR0 for the details of bit fields.
RAMC_PPU1_EDTR1	0x42221164	Power Mode Entry Delay Register 1. See RAMC_PPU0_EDTR1 for the details of bit fields.
RAMC_PPU1_DCDR0	0x42221170	Device Control Delay Configuration Register 0. See RAMC_PPU0_DCDR0 for the details of bit fields.
RAMC_PPU1_DCDR1	0x42221174	Device Control Delay Configuration Register 1. See RAMC_PPU0_DCDR1 for the details of bit fields.
RAMC_PPU1_IDR0	0x42221FB0	PPU Identification Register 0. See RAMC_PPU0_IDR0 for the details of bit fields.
RAMC_PPU1_IDR1	0x42221FB4	PPU Identification Register 1. See RAMC_PPU0_IDR1 for the details of bit fields.
RAMC_PPU1_IIDR	0x42221FC8	Implementation Identification Register. See RAMC_PPU0_IIDR for the details of bit fields.
RAMC_PPU1_AIDR	0x42221FCC	Architecture Identification Register. See RAMC_PPU0_AIDR for the details of bit fields.
RAMC_PPU1_PID4	0x42221FD0	Implementation Defined Identification Register (PID4). See RAMC_PPU0_PID4 for the details of bit fields.
RAMC_PPU1_PID0	0x42221FE0	Implementation Defined Identification Register (PID0). See RAMC_PPU0_PID0 for the details of bit fields.
RAMC_PPU1_PID1	0x42221FE4	Implementation Defined Identification Register (PID1). See RAMC_PPU0_PID1 for the details of bit fields.
RAMC_PPU1_PID2	0x42221FE8	Implementation Defined Identification Register (PID2). See RAMC_PPU0_PID2 for the details of bit fields.
RAMC_PPU1_PID3	0x42221FEC	Implementation Defined Identification Register (PID3). See RAMC_PPU0_PID3 for the details of bit fields.
RAMC_PPU1_ID0	0x42221FF0	Implementation Defined Identification Register (ID0). See RAMC_PPU0_ID0 for the details of bit fields.
RAMC_PPU1_ID1	0x42221FF4	Implementation Defined Identification Register (ID1). See RAMC_PPU0_ID1 for the details of bit fields.

CPU Sub System (CPUSS) registers

Register name	Address	Description
RAMC_PPU1_ID2	0x42221FF8	Implementation Defined Identification Register (ID2). See RAMC_PPU0_ID2 for the details of bit fields.
RAMC_PPU1_ID3	0x42221FFC	Implementation Defined Identification Register (ID3). See RAMC_PPU0_ID3 for the details of bit fields.
ICACHE0_CTL	0x42223000	Cache control
ICACHE0_CMD	0x42223008	Cache command
ICACHE0_STATUS0	0x42223080	Cache status 0
ICACHE0_STATUS1	0x42223084	Cache status 1
ICACHE0_STATUS2	0x42223088	Cache status 2
CPUSS_PPU_PWPR	0x42225000	Power Policy Register
CPUSS_PPU_PMER	0x42225004	Power Mode Emulation Register
CPUSS_PPU_PWSR	0x42225008	Power Status Register
CPUSS_PPU_DISR	0x42225010	Device Interface Input Current Status Register
CPUSS_PPU_MISR	0x42225014	Miscellaneous Input Current Status Register
CPUSS_PPU_STSR	0x42225018	Stored Status Register
CPUSS_PPU_UNLK	0x4222501C	Unlock register
CPUSS_PPU_PWCR	0x42225020	Power Configuration Register
CPUSS_PPU_PTCR	0x42225024	Power Mode Transition Configuration Register
CPUSS_PPU_IMR	0x42225030	Interrupt Mask Register
CPUSS_PPU_AIMR	0x42225034	Additional Interrupt Mask Register
CPUSS_PPU_ISR	0x42225038	Interrupt Status Register
CPUSS_PPU_AISR	0x4222503C	Additional Interrupt Status Register
CPUSS_PPU_IESR	0x42225040	Input Edge Sensitivity Register
CPUSS_PPU_OPSR	0x42225044	Operating Mode Active Edge Sensitivity Register
CPUSS_PPU_FUNRR	0x42225050	Functional Retention RAM Configuration Register
CPUSS_PPU_FULRR	0x42225054	Full Retention RAM Configuration Register
CPUSS_PPU_MEMRR	0x42225058	Memory Retention RAM Configuration Register
CPUSS_PPU_EDTR0	0x42225160	Power Mode Entry Delay Register 0
CPUSS_PPU_EDTR1	0x42225164	Power Mode Entry Delay Register 1
CPUSS_PPU_DCDR0	0x42225170	Device Control Delay Configuration Register 0
CPUSS_PPU_DCDR1	0x42225174	Device Control Delay Configuration Register 1
CPUSS_PPU_IDR0	0x42225FB0	PPU Identification Register 0
CPUSS_PPU_IDR1	0x42225FB4	PPU Identification Register 1
CPUSS_PPU_IIDR	0x42225FC8	Implementation Identification Register
CPUSS_PPU_AIDR	0x42225FCC	Architecture Identification Register
CPUSS_PPU_PID4	0x42225FD0	Implementation Defined Identification Register (PID4)

CPU Sub System (CPUSS) registers

Register name	Address	Description
CPUSS_PPU_PID0	0x42225FE0	Implementation Defined Identification Register (PID0)
CPUSS_PPU_PID1	0x42225FE4	Implementation Defined Identification Register (PID1)
CPUSS_PPU_PID2	0x42225FE8	Implementation Defined Identification Register (PID2)
CPUSS_PPU_PID3	0x42225FEC	Implementation Defined Identification Register (PID3)
CPUSS_PPU_ID0	0x42225FF0	Implementation Defined Identification Register (ID0)
CPUSS_PPU_ID1	0x42225FF4	Implementation Defined Identification Register (ID1)
CPUSS_PPU_ID2	0x42225FF8	Implementation Defined Identification Register (ID2)
CPUSS_PPU_ID3	0x42225FFC	Implementation Defined Identification Register (ID3)
MXCM33_CM33_CTL	0x42260000	Control
MXCM33_CM33_CMD	0x42260004	Command
MXCM33_CM33_STATUS	0x42260008	Status
MXCM33_CM33_NMI_CTL0	0x42260080	CM33 NMI control
MXCM33_CM33_NMI_CTL1	0x42260084	CM33 NMI control. See MXCM33_CM33_NMI_CTL0 for the details of bit fields.
MXCM33_CM33_NMI_CTL2	0x42260088	CM33 NMI control. See MXCM33_CM33_NMI_CTL0 for the details of bit fields.
MXCM33_CM33_NMI_CTL3	0x4226008C	CM33 NMI control. See MXCM33_CM33_NMI_CTL0 for the details of bit fields.
MXCM33_CM33_EVENT_CTL	0x422600C0	CM33 event control
MXCM33_CM33_S_VECTOR_TABLE_BASE	0x42261000	CM33 secure vector table base
MXCM33_CM33_NS_VECTOR_TABLE_BASE	0x42261004	CM33 non-secure vector table base
MXCM33_CM33_PC_CTL	0x42262000	CM33 protection context control
MXCM33_CM33_PC0_HANDLER	0x42262040	CM33 protection context 0 handler
MXCM33_CM33_PC1_HANDLER	0x42262100	CM33 protection context 1 handler
MXCM33_CM33_PC2_HANDLER	0x42262140	CM33 protection context 2 handler
MXCM33_CM33_PC3_HANDLER	0x42262180	CM33 protection context 3 handler
CPUSS_IDENTITY	0x42290000	Identity
CPUSS_PRODUCT_ID	0x42290010	Product identifier and version (same as CoreSight RomTables)
CPUSS_DP_STATUS	0x42290020	Debug port status
CPUSS_BUFF_CTL	0x42290030	Buffer control
CPUSS_CAL_SUP_SET	0x42290040	Calibration support set and read
CPUSS_CAL_SUP_CLR	0x42290044	Calibration support clear and reset

CPU Sub System (CPUSS) registers

Register name	Address	Description
CPUSS_INFRA_CTL	0x42290050	Infrastructure Control
CPUSS_SYSTICK_S_CTL	0x42290100	Secure SysTick timer control
CPUSS_SYSTICK_NS_CTL	0x42290120	Non Secure SysTick timer control
CPUSS_INTR_MSC	0x42290200	Master security controller Interrupt
CPUSS_INTR_MASK_MSC	0x42290208	Master security controller Interrupt mask
CPUSS_INTR_MASKED_MSC	0x4229020C	Master security controller Interrupt masked
CPUSS_AP_CTL	0x42291000	Access port control
CPUSS_PROTECTION	0x42292004	Protection status
MS0_CTL	0x42294000	Master 'x' protection context control
MS4_CTL	0x42294040	Master 'x' protection context control. See MS0_CTL for the details of bit fields.
MS5_CTL	0x42294050	Master 'x' protection context control. See MS0_CTL for the details of bit fields.
MS6_CTL	0x42294060	Master 'x' protection context control
MS7_CTL	0x42294070	Master 'x' protection context control. See MS0_CTL for the details of bit fields.
MS8_CTL	0x42294080	Master 'x' protection context control. See MS0_CTL for the details of bit fields.
MS9_CTL	0x42294090	Master 'x' protection context control. See MS6_CTL for the details of bit fields.
MS10_CTL	0x422940A0	Master 'x' protection context control. See MS0_CTL for the details of bit fields.
MS11_CTL	0x422940B0	Master 'x' protection context control. See MS6_CTL for the details of bit fields.
MS29_CTL	0x422941D0	Master 'x' protection context control. See MS0_CTL for the details of bit fields.
MS31_CTL	0x422941F0	Master 'x' protection context control. See MS0_CTL for the details of bit fields.
MS_PC0_PC	0x42295000	Master 'x' protection context value
MS_PC0_PC_READ_MIR	0x42295004	Master 'x' protection context value read mirror register
MS_PC6_PC	0x42295060	Master 'x' protection context value
MS_PC6_PC_READ_MIR	0x42295064	Master 'x' protection context value read mirror register
MS_PC9_PC	0x42295090	Master 'x' protection context value. See MS_PC6_PC for the details of bit fields.
MS_PC9_PC_READ_MIR	0x42295094	Master 'x' protection context value read mirror register. See MS_PC6_PC_READ_MIR for the details of bit fields.
MS_PC11_PC	0x422950B0	Master 'x' protection context value. See MS_PC6_PC for the details of bit fields.

CPU Sub System (CPUSS) registers

Register name	Address	Description
MS_PC11_PC_READ_MIR	0x422950B4	Master 'x' protection context value read mirror register. See MS_PC6_PC_READ_MIR for the details of bit fields.
MS_PC31_PC	0x422951F0	Master 'x' protection context value. See MS_PC6_PC for the details of bit fields.
MS_PC31_PC_READ_MIR	0x422951F4	Master 'x' protection context value read mirror register. See MS_PC6_PC_READ_MIR for the details of bit fields.
CODE_MS0_MSC_ACG_CTL	0x42296000	CODE_MS0 master security Controller & ACG configuration
SYS_MS0_MSC_ACG_CTL	0x42296010	SYS_MS0 master security Controller & ACG configuration
SYS_MS1_MSC_ACG_CTL	0x42296014	SYS_MS1 master security Controller & ACG configuration
EXP_MS_MSC_ACG_CTL	0x42296020	EXP_MS master security Controller & ACG configuration
CPUSS_SL_CTL_SL_CTL	0x42298000	Slave control (Clock enables)
CPUSS_SL_CTL_SL_CTL2	0x42298004	Slave control2 (Reset enables)
M0SECCPUSS_STATUS_VERSION	0x42430100	IP Version
PPU_APPCPUSS_PWPR	0x44100000	Power Policy Register
PPU_APPCPUSS_PMER	0x44100004	Power Mode Emulation Register
PPU_APPCPUSS_PWSR	0x44100008	Power Status Register
PPU_APPCPUSS_DISR	0x44100010	Device Interface Input Current Status Register
PPU_APPCPUSS_MISR	0x44100014	Miscellaneous Input Current Status Register
PPU_APPCPUSS_STSR	0x44100018	Stored Status Register
PPU_APPCPUSS_UNLK	0x4410001C	Unlock register
PPU_APPCPUSS_PWCR	0x44100020	Power Configuration Register
PPU_APPCPUSS_PTCR	0x44100024	Power Mode Transition Configuration Register
PPU_APPCPUSS_IMR	0x44100030	Interrupt Mask Register
PPU_APPCPUSS_AIMR	0x44100034	Additional Interrupt Mask Register
PPU_APPCPUSS_ISR	0x44100038	Interrupt Status Register
PPU_APPCPUSS_AISR	0x4410003C	Additional Interrupt Status Register
PPU_APPCPUSS_IESR	0x44100040	Input Edge Sensitivity Register
PPU_APPCPUSS_OPSR	0x44100044	Operating Mode Active Edge Sensitivity Register
PPU_APPCPUSS_FUNRR	0x44100050	Functional Retention RAM Configuration Register
PPU_APPCPUSS_FULRR	0x44100054	Full Retention RAM Configuration Register
PPU_APPCPUSS_MEMRR	0x44100058	Memory Retention RAM Configuration Register
PPU_APPCPUSS_EDTR0	0x44100160	Power Mode Entry Delay Register 0
PPU_APPCPUSS_EDTR1	0x44100164	Power Mode Entry Delay Register 1
PPU_APPCPUSS_DCDR0	0x44100170	Device Control Delay Configuration Register 0

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Register name	Address	Description
PPU_APPCPUSS_DCDR1	0x44100174	Device Control Delay Configuration Register 1
PPU_APPCPUSS_IDR0	0x44100FB0	PPU Identification Register 0
PPU_APPCPUSS_IDR1	0x44100FB4	PPU Identification Register 1
PPU_APPCPUSS_IIDR	0x44100FC8	Implementation Identification Register
PPU_APPCPUSS_AIDR	0x44100FCC	Architecture Identification Register
PPU_APPCPUSS_PID4	0x44100FD0	Implementation Defined Identification Register (PID4)
PPU_APPCPUSS_PID0	0x44100FE0	Implementation Defined Identification Register (PID0)
PPU_APPCPUSS_PID1	0x44100FE4	Implementation Defined Identification Register (PID1)
PPU_APPCPUSS_PID2	0x44100FE8	Implementation Defined Identification Register (PID2)
PPU_APPCPUSS_PID3	0x44100FEC	Implementation Defined Identification Register (PID3)
PPU_APPCPUSS_ID0	0x44100FF0	Implementation Defined Identification Register (ID0)
PPU_APPCPUSS_ID1	0x44100FF4	Implementation Defined Identification Register (ID1)
PPU_APPCPUSS_ID2	0x44100FF8	Implementation Defined Identification Register (ID2)
PPU_APPCPUSS_ID3	0x44100FFC	Implementation Defined Identification Register (ID3)
PPU_CM55_0_PWPR	0x44101000	Power Policy Register
PPU_CM55_0_PMER	0x44101004	Power Mode Emulation Register
PPU_CM55_0_PWSR	0x44101008	Power Status Register
PPU_CM55_0_DISR	0x44101010	Device Interface Input Current Status Register
PPU_CM55_0_MISR	0x44101014	Miscellaneous Input Current Status Register
PPU_CM55_0_STSR	0x44101018	Stored Status Register
PPU_CM55_0_UNLK	0x4410101C	Unlock register
PPU_CM55_0_PWCR	0x44101020	Power Configuration Register
PPU_CM55_0_PTCR	0x44101024	Power Mode Transition Configuration Register
PPU_CM55_0_IMR	0x44101030	Interrupt Mask Register
PPU_CM55_0_AIMR	0x44101034	Additional Interrupt Mask Register
PPU_CM55_0_ISR	0x44101038	Interrupt Status Register
PPU_CM55_0_AISR	0x4410103C	Additional Interrupt Status Register
PPU_CM55_0_IESR	0x44101040	Input Edge Sensitivity Register
PPU_CM55_0_OPSR	0x44101044	Operating Mode Active Edge Sensitivity Register
PPU_CM55_0_FUNRR	0x44101050	Functional Retention RAM Configuration Register
PPU_CM55_0_FULRR	0x44101054	Full Retention RAM Configuration Register

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Register name	Address	Description
PPU_CM55_0_MEMRR	0x44101058	Memory Retention RAM Configuration Register
PPU_CM55_0_EDTR0	0x44101160	Power Mode Entry Delay Register 0
PPU_CM55_0_EDTR1	0x44101164	Power Mode Entry Delay Register 1
PPU_CM55_0_DCDR0	0x44101170	Device Control Delay Configuration Register 0
PPU_CM55_0_DCDR1	0x44101174	Device Control Delay Configuration Register 1
PPU_CM55_0_IDR0	0x44101FB0	PPU Identification Register 0
PPU_CM55_0_IDR1	0x44101FB4	PPU Identification Register 1
PPU_CM55_0_IIDR	0x44101FC8	Implementation Identification Register
PPU_CM55_0_AIDR	0x44101FCC	Architecture Identification Register
PPU_CM55_0_PID4	0x44101FD0	Implementation Defined Identification Register (PID4)
PPU_CM55_0_PID0	0x44101FE0	Implementation Defined Identification Register (PID0)
PPU_CM55_0_PID1	0x44101FE4	Implementation Defined Identification Register (PID1)
PPU_CM55_0_PID2	0x44101FE8	Implementation Defined Identification Register (PID2)
PPU_CM55_0_PID3	0x44101FEC	Implementation Defined Identification Register (PID3)
PPU_CM55_0_ID0	0x44101FF0	Implementation Defined Identification Register (ID0)
PPU_CM55_0_ID1	0x44101FF4	Implementation Defined Identification Register (ID1)
PPU_CM55_0_ID2	0x44101FF8	Implementation Defined Identification Register (ID2)
PPU_CM55_0_ID3	0x44101FFC	Implementation Defined Identification Register (ID3)
PD_CTL	0x44103000	Power Domain Control
PD_PWR_UP_DELAY	0x44103004	Active switch weak enable to active switch strong enable delay
MXCM55_CM55_CTL	0x44160000	Control
MXCM55_CM55_CMD	0x44160004	Command
MXCM55_CM55_STATUS	0x44160008	Status
MXCM55_CM55_TCM_CTL	0x4416000C	TCM control
MXCM55_CM55_NMI_CTL0	0x44160080	CM55 NMI control
MXCM55_CM55_NMI_CTL1	0x44160084	CM55 NMI control. See MXCM55_CM55_NMI_CTL0 for the details of bit fields.
MXCM55_CM55_NMI_CTL2	0x44160088	CM55 NMI control. See MXCM55_CM55_NMI_CTL0 for the details of bit fields.
MXCM55_CM55_NMI_CTL3	0x4416008C	CM55 NMI control. See MXCM55_CM55_NMI_CTL0 for the details of bit fields.

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Register name	Address	Description
MXCM55_CM55_EVENT_CTL	0x441600C0	CM55 EVENT control
MXCM55_CM55_S_VECTOR_TABLE_BASE	0x44161000	CM55 secure vector table base
MXCM55_CM55_NS_VECTOR_TABLE_BASE	0x44161004	CM55 non-secure vector table base
MXCM55_WOUNDING	0x441620C0	Wounding
APPCPUSS_IDENTITY	0x441C0000	Identity
APPCPUSS_PRODUCT_ID	0x441C0010	Product identifier and version (same as CoreSight RomTables)
APPCPUSS_DP_STATUS	0x441C0020	Debug port status
APPCPUSS_BUFF_CTL	0x441C0030	Buffer control
APPCPUSS_INFRA_CTL	0x441C0050	Infrastructure Control
APPCPUSS_SYSTICK_NS_CTL	0x441C0120	Non Secure SysTick timer control
APPCPUSS_INTR_MSC	0x441C0200	Master security controller Interrupt
APPCPUSS_INTR_MASK_MSC	0x441C0208	Master security controller Interrupt mask
APPCPUSS_INTR_MASKED_MSC	0x441C020C	Master security controller Interrupt masked
APPCPUSS_INTR_AHB2AXI	0x441C0300	AHB to AXI Bridge Interrupt
APPCPUSS_INTR_SET_AHB2AXI	0x441C0304	AHB to AXI Bridge Interrupt set
APPCPUSS_INTR_MASK_AHB2AXI	0x441C0308	AHB to AXI Bridge Interrupt mask
APPCPUSS_INTR_MASKED_AHB2AXI	0x441C030C	AHB to AXI Bridge Interrupt masked
APPCPUSS_AP_CTL	0x441C1000	Access port control
MS_CTL_MS13_CTL	0x441C40D0	Master 'x' protection context control
MS_CTL_MS14_CTL	0x441C40E0	Master 'x' protection context control. See MS_CTL_MS13_CTL for the details of bit fields.
MS_CTL_MS15_CTL	0x441C40F0	Master 'x' protection context control. See MS_CTL_MS13_CTL for the details of bit fields.
MS_CTL_MS19_CTL	0x441C4130	Master 'x' protection context control
MS_CTL_MS23_CTL	0x441C4170	Master 'x' protection context control. See MS_CTL_MS19_CTL for the details of bit fields.
MS_CTL_MS25_CTL	0x441C4190	Master 'x' protection context control. See MS_CTL_MS19_CTL for the details of bit fields.
MS_CTL_MS26_CTL	0x441C41A0	Master 'x' protection context control. See MS_CTL_MS19_CTL for the details of bit fields.
MS_CTL_MS27_CTL	0x441C41B0	Master 'x' protection context control. See MS_CTL_MS13_CTL for the details of bit fields.
MS_CTL_MS28_CTL	0x441C41C0	Master 'x' protection context control. See MS_CTL_MS13_CTL for the details of bit fields.
MS_CTL_MS_PC13_PC	0x441C50D0	Master 'x' protection context value
MS_CTL_MS_PC13_PC_READ_MIR	0x441C50D4	Master 'x' protection context value read mirror register
MS_CTL_MS_PC14_PC	0x441C50E0	Master 'x' protection context value. See MS_CTL_MS_PC13_PC for the details of bit fields.

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Register name	Address	Description
MS_CTL_MS_PC14_PC_READ_MIR	0x441C50E4	Master 'x' protection context value read mirror register. See MS_CTL_MS_PC13_PC_READ_MIR for the details of bit fields.
MS_CTL_MS_PC15_PC	0x441C50F0	Master 'x' protection context value. See MS_CTL_MS_PC13_PC for the details of bit fields.
MS_CTL_MS_PC15_PC_READ_MIR	0x441C50F4	Master 'x' protection context value read mirror register. See MS_CTL_MS_PC13_PC_READ_MIR for the details of bit fields.
MS_CTL_MS_PC19_PC	0x441C5130	Master 'x' protection context value. See MS_CTL_MS_PC13_PC for the details of bit fields.
MS_CTL_MS_PC19_PC_READ_MIR	0x441C5134	Master 'x' protection context value read mirror register. See MS_CTL_MS_PC13_PC_READ_MIR for the details of bit fields.
MS_CTL_MS_PC25_PC	0x441C5190	Master 'x' protection context value. See MS_CTL_MS_PC13_PC for the details of bit fields.
MS_CTL_MS_PC25_PC_READ_MIR	0x441C5194	Master 'x' protection context value read mirror register. See MS_CTL_MS_PC13_PC_READ_MIR for the details of bit fields.
MS_CTL_MS_PC26_PC	0x441C51A0	Master 'x' protection context value. See MS_CTL_MS_PC13_PC for the details of bit fields.
MS_CTL_MS_PC26_PC_READ_MIR	0x441C51A4	Master 'x' protection context value read mirror register. See MS_CTL_MS_PC13_PC_READ_MIR for the details of bit fields.
MS_CTL_MS_PC27_PC	0x441C51B0	Master 'x' protection context value. See MS_CTL_MS_PC13_PC for the details of bit fields.
MS_CTL_MS_PC27_PC_READ_MIR	0x441C51B4	Master 'x' protection context value read mirror register. See MS_CTL_MS_PC13_PC_READ_MIR for the details of bit fields.
MS_CTL_MS_PC28_PC	0x441C51C0	Master 'x' protection context value. See MS_CTL_MS_PC13_PC for the details of bit fields.
MS_CTL_MS_PC28_PC_READ_MIR	0x441C51C4	Master 'x' protection context value read mirror register. See MS_CTL_MS_PC13_PC_READ_MIR for the details of bit fields.
MS_CTL_AXIDMAC0_MSC_ACG_CTL	0x441C6010	AXI DMAC0 MSC and ACG configuration
MS_CTL_AXI_MS0_MSC_ACG_CTL	0x441C6030	AXI_MS0 master security Controller & ACG configuration
MS_CTL_AXI_MS1_MSC_ACG_CTL	0x441C6034	AXI_MS1 master security Controller & ACG configuration
MS_CTL_AXI_MS2_MSC_ACG_CTL	0x441C6038	AXI_MS2 master security Controller & ACG configuration
MS_CTL_AXI_MS3_MSC_ACG_CTL	0x441C603C	AXI_MS3 master security Controller & ACG configuration
MS_CTL_EXP_MS0_MSC_ACG_CTL	0x441C6040	EXP_MS0 master security Controller & ACG configuration

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Register name	Address	Description
MS_CTL_EXP_MS1_MSC_ACG_CTL	0x441C6044	EXP_MS1 master security Controller & ACG configuration
MS_CTL_EXP_MS2_MSC_ACG_CTL	0x441C6048	EXP_MS2 master security Controller & ACG configuration
APPCPUSS_SL_CTL_SL_CTL	0x441C8000	Slave control (Clock enables)
APPCPUSS_SL_CTL_SL_CTL2	0x441C8004	Slave control2 (Reset enables)
U550_ID	0x44600000	ID Register
U550_STATUS	0x44600004	Register describes the current operating status of the NPU
U550_CMD	0x44600008	Command register, reads as last written command
U550_RESET	0x4460000C	Request Reset and new security mode
U550_QBASE0	0x44600010	Base address of Command-queue bits [31 downto 0]. The address is 4-byte-aligned
U550_QBASE1	0x44600014	Address extension bits [47 downto 32] for queue base
U550_QREAD	0x44600018	Read offset in the command stream in bytes. Multiples of 4 in the range 0-16 MB
U550_QCONFIG	0x4460001C	AXI configuration for the command stream in the range 0-3. Same encoding as for REGIONCFG
U550_QSIZE	0x44600020	Size of the command stream in bytes. Multiples of 4 in the range 0-16 MB
U550_PROT	0x44600024	Protection level configured for the NPU when acting as an AXI master
U550_CONFIG	0x44600028	RTL configuration
U550_LOCK	0x4460002C	Lock register. This register is designed for driver use and does not affect NPU functionality
U550_REGIONCFG	0x4460003C	Base pointer configuration. Bits[2*k+1 downto 2*k] give the memory type for REGION[k]
U550_AXI_LIMIT0	0x44600040	AXI limits for port 0 counter 0
U550_AXI_LIMIT1	0x44600044	AXI limits for port 0 counter 1
U550_AXI_LIMIT2	0x44600048	AXI limits for port 1 counter 2
U550_AXI_LIMIT3	0x4460004C	AXI limits for port 1 counter 3
U550_BASEP0	0x44600080	Lower 32 bits of the base pointer for region index 0
U550_BASEP1	0x44600084	Upper 32-bits of the base pointer for region index 0
U550_BASEP2	0x44600088	Lower 32 bits of the base pointer for region index 1
U550_BASEP3	0x4460008C	Upper 32-bits of the base pointer for region index 1
U550_BASEP4	0x44600090	Lower 32 bits of the base pointer for region index 2
U550_BASEP5	0x44600094	Upper 32-bits of the base pointer for region index 2

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Register name	Address	Description
U550_BASEP6	0x44600098	Lower 32 bits of the base pointer for region index 3
U550_BASEP7	0x4460009C	Upper 32-bits of the base pointer for region index 3
U550_BASEP8	0x446000A0	Lower 32 bits of the base pointer for region index 4
U550_BASEP9	0x446000A4	Upper 32-bits of the base pointer for region index 4
U550_BASEP10	0x446000A8	Lower 32 bits of the base pointer for region index 5
U550_BASEP11	0x446000AC	Upper 32-bits of the base pointer for region index 5
U550_BASEP12	0x446000B0	Lower 32 bits of the base pointer for region index 6
U550_BASEP13	0x446000B4	Upper 32-bits of the base pointer for region index 6
U550_BASEP14	0x446000B8	Lower 32 bits of the base pointer for region index 7
U550_BASEP15	0x446000BC	Upper 32-bits of the base pointer for region index 7
U550_PMCR	0x44600180	PMU master control register
U550_PMCNTENSET	0x44600184	Count-enable set register
U550_PMCNTENCLR	0x44600188	Count-enable clear register
U550_PMOVSSET	0x4460018C	Overflow-flag status set register
U550_PMOVSCLR	0x44600190	Overflow-flag status clear register
U550_PMINTSET	0x44600194	Interrupt-enable set register
U550_PMINTCLR	0x44600198	Interrupt-enable clear register
U550_PMCCNTR_LO	0x446001A0	Performance-monitor cycle count low register
U550_PMCCNTR_HI	0x446001A4	Performance-monitor cycle count high register
U550_PMCCNTR_CFG	0x446001A8	Set start/stop event on the cycle counter.
U550_PMCAXI_CHAN	0x446001AC	Set which AXI channel monitor
U550_PMU_EVCNTR0	0x44600300	Performance monitor event counters
U550_PMU_EVCNTR1	0x44600304	Performance monitor event counters. See U550_PMU_EVCNTR0 for the details of bit fields.
U550_PMU_EVCNTR2	0x44600308	Performance monitor event counters. See U550_PMU_EVCNTR0 for the details of bit fields.
U550_PMU_EVCNTR3	0x4460030C	Performance monitor event counters. See U550_PMU_EVCNTR0 for the details of bit fields.
U550_PMU_ENTYPER0	0x44600380	Performance monitor event type control counters
U550_PMU_ENTYPER1	0x44600384	Performance monitor event type control counters. See U550_PMU_ENTYPER0 for the details of bit fields.
U550_PMU_ENTYPER2	0x44600388	Performance monitor event type control counters. See U550_PMU_ENTYPER0 for the details of bit fields.

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Register name	Address	Description
U550_PMU_ENTYPER3	0x4460038C	Performance monitor event type control counters. See U550_PMU_ENTYPER0 for the details of bit fields.
U550_PID4	0x44600FD0	Peripheral ID byte 4 (Arm = code 4)
U550_PID5	0x44600FD4	Peripheral ID byte 5. (reserved)
U550_PID6	0x44600FD8	Peripheral ID byte 6. (reserved)
U550_PID7	0x44600FDC	Peripheral ID byte 7. (reserved)
U550_PID0	0x44600FE0	Peripheral ID byte 0. This is bits[7 downto 0] of the part number.
U550_PID1	0x44600FE4	Peripheral ID byte 1. This is bits[11 downto 8] of the part number in bits[3 downto 0], and bits[3 downto 0] of the Arm ID in bits[7 downto 4].
U550_PID2	0x44600FE8	Peripheral ID byte 2. This is bits[6 downto 4] of the Arm ID in bits[2 downto 0], and bit 3 indicates format B.
U550_PID3	0x44600FEC	Peripheral ID byte 3
U550_CID0	0x44600FF0	Component ID byte 0
U550_CID1	0x44600FF4	Component ID byte 1
U550_CID2	0x44600FF8	Component ID byte 2
U550_CID3	0x44600FFC	Component ID byte 3
U550_ROT_INIT	0x44601000	Initial settings
U550_ACG_CTL	0x44601004	ACG Configuration of ARMU55 Bridge
U550_MXU55_PPU_PWPR	0x44602000	Power Policy Register
U550_MXU55_PPU_PMER	0x44602004	Power Mode Emulation Register
U550_MXU55_PPU_PWSR	0x44602008	Power Status Register
U550_MXU55_PPU_DISR	0x44602010	Device Interface Input Current Status Register
U550_MXU55_PPU_MISR	0x44602014	Miscellaneous Input Current Status Register
U550_MXU55_PPU_STSR	0x44602018	Stored Status Register
U550_MXU55_PPU_UNLK	0x4460201C	Unlock register
U550_MXU55_PPU_PWCR	0x44602020	Power Configuration Register
U550_MXU55_PPU_PTCR	0x44602024	Power Mode Transition Configuration Register
U550_MXU55_PPU_IMR	0x44602030	Interrupt Mask Register
U550_MXU55_PPU_AIMR	0x44602034	Additional Interrupt Mask Register
U550_MXU55_PPU_ISR	0x44602038	Interrupt Status Register
U550_MXU55_PPU_AISR	0x4460203C	Additional Interrupt Status Register
U550_MXU55_PPU_IESR	0x44602040	Input Edge Sensitivity Register
U550_MXU55_PPU_OPSR	0x44602044	Operating Mode Active Edge Sensitivity Register
U550_MXU55_PPU_FUNRR	0x44602050	Functional Retention RAM Configuration Register
U550_MXU55_PPU_FULRR	0x44602054	Full Retention RAM Configuration Register
U550_MXU55_PPU_MEMRR	0x44602058	Memory Retention RAM Configuration Register

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Register name	Address	Description
U550_MXU55_PPU_EDTR0	0x44602160	Power Mode Entry Delay Register 0
U550_MXU55_PPU_EDTR1	0x44602164	Power Mode Entry Delay Register 1
U550_MXU55_PPU_DCDR0	0x44602170	Device Control Delay Configuration Register 0
U550_MXU55_PPU_DCDR1	0x44602174	Device Control Delay Configuration Register 1
U550_MXU55_PPU_IDR0	0x44602FB0	PPU Identification Register 0
U550_MXU55_PPU_IDR1	0x44602FB4	PPU Identification Register 1
U550_MXU55_PPU_IIDR	0x44602FC8	Implementation Identification Register
U550_MXU55_PPU_AIDR	0x44602FCC	Architecture Identification Register
U550_MXU55_PPU_PID4	0x44602FD0	Implementation Defined Identification Register (PID4)
U550_MXU55_PPU_PID0	0x44602FE0	Implementation Defined Identification Register (PID0)
U550_MXU55_PPU_PID1	0x44602FE4	Implementation Defined Identification Register (PID1)
U550_MXU55_PPU_PID2	0x44602FE8	Implementation Defined Identification Register (PID2)
U550_MXU55_PPU_PID3	0x44602FEC	Implementation Defined Identification Register (PID3)
U550_MXU55_PPU_ID0	0x44602FF0	Implementation Defined Identification Register (ID0)
U550_MXU55_PPU_ID1	0x44602FF4	Implementation Defined Identification Register (ID1)
U550_MXU55_PPU_ID2	0x44602FF8	Implementation Defined Identification Register (ID2)
U550_MXU55_PPU_ID3	0x44602FFC	Implementation Defined Identification Register (ID3)
U550_PD_CTL	0x44603000	Power Domain Control. See PD_CTL for the details of bit fields.
U550_PD_PWR_UP_DELAY	0x44603004	Active switch weak enable to active switch strong enable delay. See PD_PWR_UP_DELAY for the details of bit fields.

1.1.1 RAMC_PPU0_PWPR

Description: Power Policy Register

Address: 0x42220000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			LOCK_EN	Reserved [11:9]			PWR_DY-N_EN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							OP_DY-N_EN

Bits	Name	Description
24	OP_DYN_EN	Reserved Default Value: 0x0
19 : 16	OP_POLICY	Reserved Default Value: 0x0
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. When this bit is set to 1 dynamic transitions are enabled for power modes, allowing transitions to be initiated by changes on power mode DEVACTIVE inputs. Default Value: 0x1
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), MEM_RET(2), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x8

1.1.2 RAMC_PPU0_PMER

Description: Power Mode Emulation Register

Address: 0x42220004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							EMU_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	EMU_EN	Reserved Default Value: 0x0

1.1.3 RAMC_PPU0_PWSR

Description: Power Status Register

Address: 0x42220008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PWR_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved			R
HW Access	Reserved			RW	Reserved			RW
Name	Reserved [15:13]			LOCK_STA-TUS	Reserved [11:9]			PWR_DY-N_STATUS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [23:20]				OP_STATUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [31:25]							OP_DY-N_STATUS

Bits	Name	Description
24	OP_DYN_STATUS	Reserved Default Value: 0x0
19 : 16	OP_STATUS	Reserved Default Value: 0x0
12	LOCK_STATUS	Reserved Default Value: 0x0
8	PWR_DYN_STATUS	Power mode dynamic transition status. When set to 1 power mode dynamic transitions are enabled. There might be a delay in dynamic transitions becoming active or inactive if the PPU is transitioning when PWR_DYN_EN is programmed. Default Value: 0x0
3 : 0	PWR_STATUS	Power mode status. These bits reflect the current power mode of the PPU. See PPU_PWPR.PWR_POLICY for power mode enumeration. Default Value: 0x0

1.1.4 RAMC_PPU0_DISR

Description: Device Interface Input Current Status Register

Address: 0x42220010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PWR_DEVACTIVE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					R		
HW Access	Reserved					RW		
Name	Reserved [15:11]					PWR_DEVACTIVE_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	OP_DEVACTIVE_STATUS [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVE_STATUS	Reserved Default Value: 0x0
10 : 0	PWR_DEVACTIVE_STATUS	Status of the power mode DEVACTIVE inputs. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 0 is for Q-channel device 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0

1.1.5 RAMC_PPU0_MISR

Description: Miscellaneous Input Current Status Register

Address: 0x42220014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							PCSMPAC-CEPT_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DEVACCEPT_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DEVDENY_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	DEVDENY_STATUS	Status of the device interface DEVDENY inputs. There is one bit for each device interface DEVQDENY. For example, bit 16 is for Q-Channel 0 DEVQDENY, and bit 17 for Q-Channel 1 DEVQDENY. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
15 : 8	DEVACCEPT_STATUS	Status of the device interface DEVACCEPT inputs. There is one bit for each device interface DEVQACCEPTn. For example, bit 8 is for Q-Channel 0 DEVQACCEPTn and bit 9 for Q-Channel 1 DEVQACCEPTn. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
0	PCSMPACCEPT_STA-TUS	The status of the PCSMPACCEPT input. Default Value: 0x0

1.1.6 RAMC_PPU0_STSR

Description: Stored Status Register

Address: 0x42220018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	STORED_DEVDENY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	STORED_DEVDENY	Reserved (this PPU has a single Q-channel) Default Value: 0x0

1.1.7 RAMC_PPU0_UNLK

Description: Unlock register

Address: 0x4222001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							UNLOCK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	UNLOCK	Reserved Default Value: 0x0

1.1.8 RAMC_PPU0_PWCR

Description: Power Configuration Register

Address: 0x42220020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVREQEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PWR_DEVACTIVEEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_DEVACTIVEEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	OP_DEVACTIVEEN [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVEEN	Reserved Default Value: 0x0
18 : 8	PWR_DEVACTIVEEN	These bits enable the power mode DEVACTIVE inputs. When a bit is to 1 the related DEVACTIVE input is enabled, when set to 0 it is disabled. All available bits are reset to 1. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE, and bit 9 for the Q-Channel 1 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x001
7 : 0	DEVREQEN	When set to 1 enables the device interface handshake for transitions. All available bits are reset to 1. There is one bit for each device interface channel. For example, bit 0 is for Q-Channel 0, and bit 1 is for Q-Channel 1. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x01

1.1.9 RAMC_PPU0_PTCR

Description: Power Mode Transition Configuration Register

Address: 0x42220024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						DBG_RE-COV_POR ST_EN	WARM_RS T_DEVREQ EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	DBG_RE-COV_PORST_EN	Reserved Default Value: 0x0
0	WARM_RST_DEVREQEN	Transition behavior between ON and WARM_RST. This bit should not be modified when the PPU is in WARM_RST, or if the PPU is performing a transition, otherwise PPU behavior is UN-PREDICTABLE. 0: The PPU does not perform a device interface handshake when transitioning between ON and WARM_RST. 1: The PPU performs a device interface handshake when transitioning between ON and WARM_RST. This disables all Q-Channels for this transition. Default Value: 0x0

1.1.10 RAMC_PPU0_IMR

Description: Interrupt Mask Register

Address: 0x42220030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		LOCKED_IRQ_MASK	EMU_DENY_IRQ_MASK	EMU_ACCEPT_IRQ_MASK	STA_DENY_IRQ_MASK	STA_ACCEPT_IRQ_MASK	STA_POLICY_TRN_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	LOCKED_IRQ_MASK	Reserved Default Value: 0x1
4	EMU_DENY_IRQ_MASK	Reserved Default Value: 0x1
3	EMU_ACCEPT_IRQ_MASK	Reserved Default Value: 0x1
2	STA_DENY_IRQ_MASK	Static transition denial event mask. Default Value: 0x0
1	STA_ACCEPT_IRQ_MASK	Static transition acceptance event mask. Default Value: 0x1
0	STA_POLICY_TRN_IRQ_MASK	Static full policy transition completion event mask. Default Value: 0x0

1.1.11 RAMC_PPU0_AIMR

Description: Additional Interrupt Mask Register

Address: 0x42220034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	RW	RW	RW
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ_MASK	STA_POLICY_PWR_IRQ_MASK	DYN_DENY_IRQ_MASK	DYN_ACCEPT_IRQ_MASK	UNSPT_POLICY_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ_MASK	Reserved Default Value: 0x1
3	STA_POLICY_PWR_IRQ_MASK	Reserved Default Value: 0x1
2	DYN_DENY_IRQ_MASK	Dynamic transition denial event mask. Default Value: 0x1
1	DYN_ACCEPT_IRQ_MASK	Dynamic transition acceptance event mask. Default Value: 0x1
0	UNSPT_POLICY_IRQ_MASK	Unsupported Policy event mask. Default Value: 0x0

1.1.12 RAMC_PPU0_ISR

Description: Interrupt Status Register

Address: 0x42220038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	Reserved	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	Reserved	R	R	R	R	R	R
Name	OTH-ER_IRQ	Reserved	LOCKED_IRQ	EMU_DE-NY_IRQ	EMU_AC-CEPT_IRQ	STA_DE-NY_IRQ	STA_AC-CEPT_IRQ	STA_POLI-CY_TRN_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	PWR_ACTIVE_EDGE_IRQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW1C		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_ACTIVE_EDGE_IRQ [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	OP_ACTIVE_EDGE_IRQ [31:24]							

Bits	Name	Description
31 : 24	OP_ACTIVE_EDGE_IRQ	Indicates which operating mode DEVPACTIVE inputs caused the input edge event. When operating modes are not supported this field is reserved. Default Value: 0x0
18 : 8	PWR_ACTIVE_EDGE_IRQ	Indicates which power mode DEVACTIVE inputs caused the input edge event. Bits for unused channels are the MSBs and are reserved. There is one bit for each device Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x00
7	OTHER_IRQ	Indicates there is an interrupt event pending in the Additional Interrupt Status Register (PPU_AISR). Default Value: 0x0
5	LOCKED_IRQ	Reserved Default Value: 0x0
4	EMU_DENY_IRQ	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ	Reserved Default Value: 0x0
2	STA_DENY_IRQ	Static transition denial event status. Default Value: 0x0
1	STA_ACCEPT_IRQ	Static transition acceptance event status. Default Value: 0x0

1.1.12 RAMC_PPU0_ISR (continued)

0	STA_POLICY_TRN_IRQ	Static full policy transition completion event status. Default Value: 0x0

1.1.13 RAMC_PPU0_AISR

Description: Additional Interrupt Status Register

Address: 0x4222003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ	STA_POLICY_PWR_IRQ	DYN_DENY_IRQ	DYN_ACCEPT_IRQ	UNSPT_POLICY_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ	Reserved Default Value: 0x0
2	DYN_DENY_IRQ	Dynamic transition denial event status. Default Value: 0x0
1	DYN_ACCEPT_IRQ	Dynamic transition acceptance event status. Default Value: 0x0
0	UNSPT_POLICY_IRQ	Unsupported Policy event status. Default Value: 0x0

1.1.14 RAMC_PPU0_IESR

Description: Input Edge Sensitivity Register

Address: 0x42220040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE03_EDGE [7:6]		DEVACTIVE02_EDGE [5:4]		DEVACTIVE01_EDGE [3:2]		DEVACTIVE00_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE07_EDGE [15:14]		DEVACTIVE06_EDGE [13:12]		DEVACTIVE05_EDGE [11:10]		DEVACTIVE04_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		RW		RW	
HW Access	Reserved		R		R		R	
Name	Reserved [23:22]		DEVACTIVE10_EDGE [21:20]		DEVACTIVE09_EDGE [19:18]		DEVACTIVE08_EDGE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 20	DEVACTIVE10_EDGE	Reserved Default Value: 0x0
19 : 18	DEVACTIVE09_EDGE	Reserved Default Value: 0x0
17 : 16	DEVACTIVE08_EDGE	Reserved Default Value: 0x0
15 : 14	DEVACTIVE07_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE06_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE05_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE04_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE03_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE02_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE01_EDGE	Reserved Default Value: 0x0

1.1.14 RAMC_PPU0_IESR (continued)

1 : 0	DEVACTIVE00_EDGE	DEVACTIVE 0 edge sensitivity. Default Value: 0x0

1.1.15 RAMC_PPU0_OPSR

Description: Operating Mode Active Edge Sensitivity Register

Address: 0x42220044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE19_EDGE [7:6]		DEVACTIVE18_EDGE [5:4]		DEVACTIVE17_EDGE [3:2]		DEVACTIVE16_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE23_EDGE [15:14]		DEVACTIVE22_EDGE [13:12]		DEVACTIVE21_EDGE [11:10]		DEVACTIVE20_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	DEVACTIVE23_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE22_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE21_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE20_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE19_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE18_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE17_EDGE	Reserved Default Value: 0x0
1 : 0	DEVACTIVE16_EDGE	Reserved Default Value: 0x0

1.1.16 RAMC_PPU0_FUNRR

Description: Functional Retention RAM Configuration Register

Address: 0x42220050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FUNC_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FUNC_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.17 RAMC_PPU0_FULRR

Description: Full Retention RAM Configuration Register

Address: 0x42220054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FULL_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FULL_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.18 RAMC_PPU0_MEMRR

Description: Memory Retention RAM Configuration Register

Address: 0x42220058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	MEM_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.19 RAMC_PPU0_EDTR0

Description: Power Mode Entry Delay Register 0

Address: 0x42220160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOGIC_RET_DEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	FULL_RET_DEL [31:24]							

Bits	Name	Description
31 : 24	FULL_RET_DEL	Reserved Default Value: 0x00
23 : 16	LOGIC_RET_DEL	Reserved Default Value: 0x00
15 : 8	MEM_RET_DEL	Reserved Default Value: 0x00
7 : 0	OFF_DEL	Reserved Default Value: 0x00

1.1.20 RAMC_PPU0_EDTR1

Description: Power Mode Entry Delay Register 1

Address: 0x42220164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FUNC_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	FUNC_RET_DEL	Reserved Default Value: 0x00
7 : 0	MEM_OFF_DEL	Reserved Default Value: 0x00

1.1.21 RAMC_PPU0_DCDR0

Description: Device Control Delay Configuration Register 0

Address: 0x42220170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CLKEN_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ISO_CLKEN_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RST_HWSTAT_DLY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	RST_HWSTAT_DLY	Reserved Default Value: 0x0
15 : 8	ISO_CLKEN_DLY	Reserved Default Value: 0x0
7 : 0	CLKEN_RST_DLY	Reserved Default Value: 0x0

1.1.22 RAMC_PPU0_DCDR1

Description: Device Control Delay Configuration Register 1

Address: 0x42220174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ISO_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CLKEN_ISO_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	CLKEN_ISO_DLY	Reserved Default Value: 0x0
7 : 0	ISO_RST_DLY	Reserved Default Value: 0x0

1.1.23 RAMC_PPU0_IDR0

Description: PPU Identification Register 0

Address: 0x42220FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	NUM_OPMODE [7:4]				DEVCHAN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	STA_-FUNC_RET_SPT	STA_-FULL_RET_SPT	STA_MEM_OFF_SPT	STA_LG-C_RET_SPT	STA_MEM_RET_EMU_SPT	STA_MEM_RET_SPT	STA_OFF_EMU_SPT	STA_OFF_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	Reserved	R	R	R
HW Access	RW	RW	RW	RW	Reserved	RW	RW	RW
Name	DY-N_MEM_RET_EMU_SPT	DY-N_MEM_RET_SPT	DY-N_OFF_EMU_SPT	DY-N_OFF_SPT	Reserved	STA_DB-G_RE-COV_SPT	STA_WRM_RST_SPT	STA_ON_SPT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [31:30]		DY-N_WRM_RST_SPT	DY-N_ON_SPT	DYN_-FUNC_RET_SPT	DYN_-FULL_RET_SPT	DY-N_MEM_OFF_SPT	DYN_LG-C_RET_SPT

Bits	Name	Description
29	DYN_WRM_RST_SPT	Dynamic WARM_RST support. Default Value: 0x0
28	DYN_ON_SPT	Dynamic ON support. Default Value: 0x1
27	DYN_FUNC_RET_SPT	Dynamic FUNC_RET support. Default Value: 0x0
26	DYN_FULL_RET_SPT	Dynamic FULL_RET support. Default Value: 0x0
25	DYN_MEM_OFF_SPT	Dynamic MEM_OFF support. Default Value: 0x0
24	DYN_LGC_RET_SPT	Dynamic LOGIC_RET support. Default Value: 0x0
23	DY-N_MEM_RET_EMU_SPT	Dynamic MEM_RET_EMU support Default Value: 0x0
22	DYN_MEM_RET_SPT	Dynamic MEM_RET support. Default Value: 0x1

1.1.23 RAMC_PPU0_IDR0 (continued)

21	DYN_OFF_EMU_SPT	Dynamic OFF_EMU support. Default Value: 0x0
20	DYN_OFF_SPT	Dynamic OFF support. Default Value: 0x1
18	STA_DBG_RECOV_SPT	DBG_RECOV support. Default Value: 0x0
17	STA_WRM_RST_SPT	WARM_RST support. Ignore this bit. Do not use WARM_RST. Default Value: 0x1
16	STA_ON_SPT	ON support. Default Value: 0x1
15	STA_FUNC_RET_SPT	FUNC_RET support. Default Value: 0x0
14	STA_FULL_RET_SPT	FULL_RET support. Default Value: 0x0
13	STA_MEM_OFF_SPT	MEM_OFF support. Default Value: 0x0
12	STA_LGC_RET_SPT	LOGIC_RET support. Default Value: 0x0
11	STA_MEM_RET_EMU_SPT	MEM_RET_EMU support. Default Value: 0x0
10	STA_MEM_RET_SPT	MEM_RET support. Default Value: 0x1
9	STA_OFF_EMU_SPT	OFF_EMU support. Default Value: 0x0
8	STA_OFF_SPT	OFF support. Default Value: 0x1
7 : 4	NUM_OPMODE	No. of operating modes supported is NUM_OPMODE + 1. Default Value: 0x0
3 : 0	DEVCHAN	No. of Device Interface Channels. The device enumeration is: Device 0: PDCM Default Value: 1

1.1.24 RAMC_PPU0_IDR1

Description: PPU Identification Register 1

Address: 0x42220FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	Reserved	R	R	R
HW Access	Reserved	RW	RW	RW	Reserved	RW	RW	RW
Name	Reserved	FUNC_RET_RAM_REG	FULL_RET_RAM_REG	MEM_RET_RAM_REG	Reserved	LOCK_SPT	SW_DEV_DEL_SPT	PWR_-MODE_EN-TRY_DEL_SPT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved	R	R	R
HW Access	Reserved			RW	Reserved	RW	RW	RW
Name	Reserved [15:13]			OFF_MEM_RET_TRANS	Reserved	OP_AC-TIVE	STA_POLI-CY_OP_IRQ_SPT	STA_POLI-CY_P-WR_IRQ_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	OFF_MEM_RET_TRANS	OFF to MEM_RET direct transition. Indicates if direct transitions from OFF to MEM_RET and from OFF_EMU to MEM_RET_EMU are supported. Default Value: 0x0
10	OP_ACTIVE	Reserved Default Value: 0x0
9	STA_POLI-CY_OP_IRQ_SPT	Operating policy transition completion event status. Default Value: 0x0
8	STA_POLICY_P-WR_IRQ_SPT	Power policy transition completion event status. Default Value: 0x0
6	FUNC_RET_RAM_REG	Indicates if the PPU_FUNRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
5	FULL_RET_RAM_REG	Indicates if the PPU_FULRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
4	MEM_RET_RAM_REG	Indicates if the PPU_MEMRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
2	LOCK_SPT	Lock and the lock interrupt event are supported. Default Value: 0x0

1.1.24 RAMC_PPU0_IDR1 (continued)

1	SW_DEV_DEL_SPT	Software device delay control configuration support. Default Value: 0x0
0	PWR_MODE_EN- TRY_DEL_SPT	Power mode entry delay support. Default Value: 0x0

1.1.25 RAMC_PPU0_IIDR

Description: Implementation Identification Register

Address: 0x42220FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IMPLEMENTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	REVISION [15:12]				IMPLEMENTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PRODUCT_ID [23:20]				VARIANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 20	PRODUCT_ID	PPU part identification. Default Value: 0x0B5
19 : 16	VARIANT	Major revision of the product. Default Value: 0
15 : 12	REVISION	Minor revision of the product. Default Value: 0
11 : 0	IMPLEMENTER	Implementer identification. [11:8] The JEP106 continuation code of the implementer. [7] Always 0. [6:0] The JEP106 identity code of the implementer. For an Arm implementation, bits [11:0] are 0x43B. Default Value: 0x43B

1.1.26 RAMC_PPU0_AIDR

Description: Architecture Identification Register

Address: 0x42220FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	ARCH_REV_MAJOR [7:4]				ARCH_REV_MINOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ARCH_REV_MAJOR	0x1 - PPU architecture major revision 1. Other Values - Reserved. Default Value: 0x1
3 : 0	ARCH_REV_MINOR	0x1 - PPU Architecture minor revision 1. Other Values - Reserved. Default Value: 0x1

1.1.27 RAMC_PPU0_PID4

Description: Implementation Defined Identification Register (PID4)

Address: 0x42220FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				IMPLEMENTER_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	IMPLEMENTER_11_8	The JEP106 continuation code of the implementer, which is 0x4 hardcoded value. Default Value: 0x4

1.1.28 RAMC_PPU0_PID0

Description: Implementation Defined Identification Register (PID0)

Address: 0x42220FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID_7_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PRODUCT_ID_7_0	PPU part identification bits [7:0]. Default Value: 0xB5

1.1.29 RAMC_PPU0_PID1

Description: Implementation Defined Identification Register (PID1)

Address: 0x42220FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	IMPLEMENTER_3_0 [7:4]				PRODUCT_ID_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	IMPLEMENTER_3_0	JEP106_ID bits [3:0] Default Value: 0xB
3 : 0	PRODUCT_ID_11_8	PPU part identification bits [11:8] Default Value: 0x0

1.1.30 RAMC_PPU0_PID2

Description: Implementation Defined Identification Register (PID2)

Address: 0x42220FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R	R		
HW Access	RW				RW	RW		
Name	REV_CONST [7:4]				CON-ST_HIGH	IMPLEMENTER_6_4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	REV_CONST	Constant LOW Revision (4 bits) Default Value: 0x0
3	CONST_HIGH	Constant HIGH Default Value: 0x1
2 : 0	IMPLEMENTER_6_4	JEP106_ID bits [6:4] Default Value: 0x3

1.1.31 RAMC_PPU0_PID3

Description: Implementation Defined Identification Register (PID3)

Address: 0x42220FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PID3_REVISION [7:4]				PID3_REV_CONST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	PID3_REVISION	Minor revision of the product. Default Value: 0x0
3 : 0	PID3_REV_CONST	Constant LOW (4 bits) Default Value: 0x0

1.1.32 RAMC_PPU0_ID0

Description: Implementation Defined Identification Register (ID0)

Address: 0x42220FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID0	ID0 hard coded value Default Value: 0x0D

1.1.33 RAMC_PPU0_ID1

Description: Implementation Defined Identification Register (ID1)

Address: 0x42220FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID1	ID1 hardcoded value Default Value: 0xF0

1.1.34 RAMC_PPU0_ID2

Description: Implementation Defined Identification Register (ID2)

Address: 0x42220FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID2	ID2 hardcoded value Default Value: 0x05

1.1.35 RAMC_PPU0_ID3

Description: Implementation Defined Identification Register (ID3)

Address: 0x42220FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID3	ID3 hardcoded value Default Value: 0xB1

1.1.36 ICACHE0_CTL

Description: Cache control

Address: 0x42223000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved	RW				
HW Access	R	R	Reserved	R				
Name	CA_EN	PREF_EN	Reserved	SET_ADDR [28:24]				

Bits	Name	Description
31	CA_EN	Cache enable: 0: Disabled. The cache tag valid bits are reset to "0"s and the cache LRU information is set to "1"s (making way 0 the LRU way and way 3 the MRU way). 1: Enabled. Default Value: 1
30	PREF_EN	Prefetch enable: 0: Disabled. 1: Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is "1". Default Value: 1
28 : 24	SET_ADDR	Specifies the cache set for which cache information is provided in STATUS0/1/2. Default Value: 0
17 : 16	WAY	Specifies the cache way for which cache information is provided in STATUS0/1/2. Default Value: 0

1.1.37 ICACHE0_CMD

Description: Cache command

Address: 0x42223008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1S	RW1S
HW Access	Reserved						RW1C	RW1C
Name	Reserved [7:2]						BUFF_INV	INV

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	BUFF_INV	Invalidation of buffers (does not invalidate the caches). SW writes a "1" to clear the buffers. HW sets this field to "0" when the operation is completed. Default Value: 0
0	INV	Invalidation of cahce and buffer. SW writes a "1" to clear the caches. HW sets this field to "0" when the operation is completed. The caches' LRU structures are also reset to their default state. Default Value: 0

1.1.38 ICACHE0_STATUS0

Description: Cache status 0

Address: 0x42223080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALID32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALID32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALID32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALID32 [31:24]							

Bits	Name	Description
31 : 0	VALID32	Sixteen valid bits of the cache line specified by CTL.WAY and CTL.SET_ADDR. Default Value: 0

1.1.39 ICACHE0_STATUS1

Description: Cache status 1

Address: 0x42223084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TAG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TAG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TAG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TAG [31:24]							

Bits	Name	Description
31 : 0	TAG	Cache line address of the cache line specified by CTL.WAY and CTL.SET_ADDR. Default Value: Undefined

1.1.40 ICACHE0_STATUS2

Description: Cache status 2

Address: 0x42223088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [7:6]		LRU [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	LRU	Six bit LRU representation of the cache set specified by CTL.SET_ADDR. The encoding of the field is as follows ("X_LRU_Y" indicates that way X is Less Recently Used than way Y): Bit 5: 0_LRU_1: way 0 less recently used than way 1. Bit 4: 0_LRU_2. Bit 3: 0_LRU_3. Bit 2: 1_LRU_2. Bit 1: 1_LRU_3. Bit 0: 2_LRU_3. Default Value: 0x3F

1.1.41 CPUSS_PPU_PWPR

Description: Power Policy Register

Address: 0x42225000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			LOCK_EN	Reserved [11:9]			PWR_DYN_EN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							OP_DYN_EN

Bits	Name	Description
24	OP_DYN_EN	Reserved Default Value: 0x0
19 : 16	OP_POLICY	Reserved Default Value: 0x0
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. When this bit is set to 1 dynamic transitions are enabled for power modes, allowing transitions to be initiated by changes on power mode DEVACTIVE inputs. Default Value: 0x1
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), FULL_RET(5), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x8

1.1.42 CPUSS_PPU_PMER

Description: Power Mode Emulation Register

Address: 0x42225004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							EMU_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	EMU_EN	Reserved Default Value: 0x0

1.1.43 CPUSS_PPU_PWSR

Description: Power Status Register

Address: 0x42225008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PWR_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved			R
HW Access	Reserved			RW	Reserved			RW
Name	Reserved [15:13]			LOCK_STA-TUS	Reserved [11:9]			PWR_DY-N_STATUS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [23:20]				OP_STATUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [31:25]							OP_DY-N_STATUS

Bits	Name	Description
24	OP_DYN_STATUS	Reserved Default Value: 0x0
19 : 16	OP_STATUS	Reserved Default Value: 0x0
12	LOCK_STATUS	Reserved Default Value: 0x0
8	PWR_DYN_STATUS	Power mode dynamic transition status. When set to 1 power mode dynamic transitions are enabled. There might be a delay in dynamic transitions becoming active or inactive if the PPU is transitioning when PWR_DYN_EN is programmed. Default Value: 0x0
3 : 0	PWR_STATUS	Power mode status. These bits reflect the current power mode of the PPU. See PPU_PWPR.PWR_POLICY for power mode enumeration. Default Value: 0x0

1.1.44 CPUSS_PPU_DISR

Description: Device Interface Input Current Status Register

Address: 0x42225010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PWR_DEVACTIVE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					R		
HW Access	Reserved					RW		
Name	Reserved [15:11]					PWR_DEVACTIVE_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	OP_DEVACTIVE_STATUS [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVE_STATUS	Reserved Default Value: 0x0
10 : 0	PWR_DEVACTIVE_STATUS	Status of the power mode DEVACTIVE inputs. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 0 is for Q-channel device 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0

1.1.45 CPUSS_PPU_MISR

Description: Miscellaneous Input Current Status Register

Address: 0x42225014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							PCSMPAC-CEPT_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DEVACCEPT_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DEVDENY_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	DEVDENY_STATUS	Status of the device interface DEVDENY inputs. There is one bit for each device interface DEVQDENY. For example, bit 16 is for Q-Channel 0 DEVQDENY, and bit 17 for Q-Channel 1 DEVQDENY. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
15 : 8	DEVACCEPT_STATUS	Status of the device interface DEVACCEPT inputs. There is one bit for each device interface DEVQACCEPTn. For example, bit 8 is for Q-Channel 0 DEVQACCEPTn and bit 9 for Q-Channel 1 DEVQACCEPTn. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
0	PCSMPACCEPT_STA-TUS	The status of the PCSMPACCEPT input. Default Value: 0x0

1.1.46 CPUSS_PPU_STSR

Description: Stored Status Register

Address: 0x42225018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	STORED_DEVDENY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	STORED_DEVDENY	Status of the DEVDENY signals from the last device interface Q-Channel transition. For Q-Channel: There is one bit for each device interface DEVQDENY. For example, bit 0 is for Q-Channel 0 DEVQDENY, and bit 1 for Q-Channel 1 DEVQDENY. Refer to PPU_DISR.PWR_DEVACTIVE_STATUS for device enumeration. Default Value: 0x0

1.1.47 CPUSS_PPU_UNLK

Description: Unlock register

Address: 0x4222501C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							UNLOCK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	UNLOCK	Reserved Default Value: 0x0

1.1.48 CPUSS_PPU_PWCR

Description: Power Configuration Register

Address: 0x42225020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVREQEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PWR_DEVACTIVEEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_DEVACTIVEEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	OP_DEVACTIVEEN [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVEEN	Reserved Default Value: 0x00
18 : 8	PWR_DEVACTIVEEN	These bits enable the power mode DEVACTIVE inputs. When a bit is to 1 the related DEVACTIVE input is enabled, when set to 0 it is disabled. All available bits are reset to 1. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE, and bit 9 for the Q-Channel 1 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x03
7 : 0	DEVREQEN	When set to 1 enables the device interface handshake for transitions. All available bits are reset to 1. There is one bit for each device interface channel. For example, bit 0 is for Q-Channel 0, and bit 1 is for Q-Channel 1. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x03

1.1.49 CPUSS_PPU_PTCR

Description: Power Mode Transition Configuration Register

Address: 0x42225024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						DBG_RE-COV_POR ST_EN	WARM_RS T_DEVREQ EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	DBG_RE-COV_PORST_EN	Reserved Default Value: 0x0
0	WARM_RST_DEVREQEN	Transition behavior between ON and WARM_RST. This bit should not be modified when the PPU is in WARM_RST, or if the PPU is performing a transition, otherwise PPU behavior is UN-PREDICTABLE. 0: The PPU does not perform a device interface handshake when transitioning between ON and WARM_RST. 1: The PPU performs a device interface handshake when transitioning between ON and WARM_RST. This disables all Q-Channels for this transition. Default Value: 0x0

1.1.50 CPUSS_PPU_IMR

Description: Interrupt Mask Register

Address: 0x42225030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		LOCKED_IRQ_MASK	EMU_DENY_IRQ_MASK	EMU_ACCEPT_IRQ_MASK	STA_DENY_IRQ_MASK	STA_ACCEPT_IRQ_MASK	STA_POLICY_TRN_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	LOCKED_IRQ_MASK	Reserved Default Value: 0x0
4	EMU_DENY_IRQ_MASK	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ_MASK	Reserved Default Value: 0x0
2	STA_DENY_IRQ_MASK	Static transition denial event mask. Default Value: 0x0
1	STA_ACCEPT_IRQ_MASK	Static transition acceptance event mask. Default Value: 0x1
0	STA_POLICY_TRN_IRQ_MASK	Static full policy transition completion event mask. Default Value: 0x0

1.1.51 CPUSS_PPU_AIMR

Description: Additional Interrupt Mask Register

Address: 0x42225034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	RW	RW	RW
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ_MASK	STA_POLICY_PWR_IRQ_MASK	DYN_DENY_IRQ_MASK	DYN_ACCEPT_IRQ_MASK	UNSPT_POLICY_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ_MASK	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ_MASK	Reserved Default Value: 0x0
2	DYN_DENY_IRQ_MASK	Dynamic transition denial event mask. Default Value: 0x1
1	DYN_ACCEPT_IRQ_MASK	Dynamic transition acceptance event mask. Default Value: 0x1
0	UNSPT_POLICY_IRQ_MASK	Unsupported Policy event mask. Default Value: 0x0

1.1.52 CPUSS_PPU_ISR

Description: Interrupt Status Register

Address: 0x42225038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	Reserved	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	Reserved	R	R	R	R	R	R
Name	OTH-ER_IRQ	Reserved	LOCKED_IRQ	EMU_DE-NY_IRQ	EMU_AC-CEPT_IRQ	STA_DE-NY_IRQ	STA_AC-CEPT_IRQ	STA_POLI-CY_TRN_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	PWR_ACTIVE_EDGE_IRQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW1C		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_ACTIVE_EDGE_IRQ [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	OP_ACTIVE_EDGE_IRQ [31:24]							

Bits	Name	Description
31 : 24	OP_ACTIVE_EDGE_IRQ	Indicates which operating mode DEVPACTIVE inputs caused the input edge event. When operating modes are not supported this field is reserved. Default Value: 0x0
18 : 8	PWR_ACTIVE_EDGE_IRQ	Indicates which power mode DEVACTIVE inputs caused the input edge event. Bits for unused channels are the MSBs and are reserved. There is one bit for each device Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x00
7	OTHER_IRQ	Indicates there is an interrupt event pending in the Additional Interrupt Status Register (PPU_AISR). Default Value: 0x0
5	LOCKED_IRQ	Reserved Default Value: 0x0
4	EMU_DENY_IRQ	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ	Reserved Default Value: 0x0
2	STA_DENY_IRQ	Static transition denial event status. Default Value: 0x0
1	STA_ACCEPT_IRQ	Static transition acceptance event status. Default Value: 0x0

1.1.52 CPUSS_PPU_ISR (continued)

0	STA_POLICY_TRN_IRQ	Static full policy transition completion event status. Default Value: 0x0

1.1.53 CPUSS_PPU_AISR

Description: Additional Interrupt Status Register

Address: 0x4222503C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ	STA_POLICY_PWR_IRQ	DYN_DENY_IRQ	DYN_ACCEPT_IRQ	UNSPT_POLICY_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ	Reserved Default Value: 0x0
2	DYN_DENY_IRQ	Dynamic transition denial event status. Default Value: 0x0
1	DYN_ACCEPT_IRQ	Dynamic transition acceptance event status. Default Value: 0x0
0	UNSPT_POLICY_IRQ	Unsupported Policy event status. Default Value: 0x0

1.1.54 CPUSS_PPU_IESR

Description: Input Edge Sensitivity Register

Address: 0x42225040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE03_EDGE [7:6]		DEVACTIVE02_EDGE [5:4]		DEVACTIVE01_EDGE [3:2]		DEVACTIVE00_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE07_EDGE [15:14]		DEVACTIVE06_EDGE [13:12]		DEVACTIVE05_EDGE [11:10]		DEVACTIVE04_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		RW		RW	
HW Access	Reserved		R		R		R	
Name	Reserved [23:22]		DEVACTIVE10_EDGE [21:20]		DEVACTIVE09_EDGE [19:18]		DEVACTIVE08_EDGE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 20	DEVACTIVE10_EDGE	Reserved Default Value: 0x0
19 : 18	DEVACTIVE09_EDGE	Reserved Default Value: 0x0
17 : 16	DEVACTIVE08_EDGE	Reserved Default Value: 0x0
15 : 14	DEVACTIVE07_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE06_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE05_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE04_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE03_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE02_EDGE	DEVACTIVE 2 edge sensitivity. Default Value: 0x0
3 : 2	DEVACTIVE01_EDGE	DEVACTIVE 1 edge sensitivity. Default Value: 0x0

1.1.54 CPUSS_PPU_IESR (continued)

1 : 0	DEVACTIVE00_EDGE	DEVACTIVE 0 edge sensitivity. Default Value: 0x0

1.1.55 CPUSS_PPU_OPSR

Description: Operating Mode Active Edge Sensitivity Register

Address: 0x42225044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE19_EDGE [7:6]		DEVACTIVE18_EDGE [5:4]		DEVACTIVE17_EDGE [3:2]		DEVACTIVE16_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE23_EDGE [15:14]		DEVACTIVE22_EDGE [13:12]		DEVACTIVE21_EDGE [11:10]		DEVACTIVE20_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	DEVACTIVE23_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE22_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE21_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE20_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE19_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE18_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE17_EDGE	Reserved Default Value: 0x0
1 : 0	DEVACTIVE16_EDGE	Reserved Default Value: 0x0

1.1.56 CPUSS_PPU_FUNRR

Description: Functional Retention RAM Configuration Register

Address: 0x42225050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FUNC_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FUNC_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.57 CPUSS_PPU_FULRR

Description: Full Retention RAM Configuration Register

Address: 0x42225054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FULL_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FULL_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.58 CPUSS_PPU_MEMRR

Description: Memory Retention RAM Configuration Register

Address: 0x42225058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	MEM_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.59 CPUSS_PPU_EDTR0

Description: Power Mode Entry Delay Register 0

Address: 0x42225160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOGIC_RET_DEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	FULL_RET_DEL [31:24]							

Bits	Name	Description
31 : 24	FULL_RET_DEL	Reserved Default Value: 0x00
23 : 16	LOGIC_RET_DEL	Reserved Default Value: 0x00
15 : 8	MEM_RET_DEL	Reserved Default Value: 0x00
7 : 0	OFF_DEL	Reserved Default Value: 0x00

1.1.60 CPUSS_PPU_EDTR1

Description: Power Mode Entry Delay Register 1

Address: 0x42225164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FUNC_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	FUNC_RET_DEL	Reserved Default Value: 0x00
7 : 0	MEM_OFF_DEL	Reserved Default Value: 0x00

1.1.61 CPUSS_PPU_DCDR0

Description: Device Control Delay Configuration Register 0

Address: 0x42225170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CLKEN_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ISO_CLKEN_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RST_HWSTAT_DLY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	RST_HWSTAT_DLY	Reserved Default Value: 0x0
15 : 8	ISO_CLKEN_DLY	Reserved Default Value: 0x0
7 : 0	CLKEN_RST_DLY	Reserved Default Value: 0x0

1.1.62 CPUSS_PPU_DCDR1

Description: Device Control Delay Configuration Register 1

Address: 0x42225174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ISO_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CLKEN_ISO_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	CLKEN_ISO_DLY	Reserved Default Value: 0x0
7 : 0	ISO_RST_DLY	Reserved Default Value: 0x0

1.1.63 CPUSS_PPU_IDR0

Description: PPU Identification Register 0

Address: 0x42225FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	NUM_OPMODE [7:4]				DEVCHAN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	STA_-FUNC_RET_SPT	STA_-FULL_RET_SPT	STA_MEM_OFF_SPT	STA_LG-C_RET_SPT	STA_MEM_RET_EMU_SPT	STA_MEM_RET_SPT	STA_OFF_EMU_SPT	STA_OFF_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	Reserved	R	R	R
HW Access	RW	RW	RW	RW	Reserved	RW	RW	RW
Name	DY-N_MEM_RET_EMU_SPT	DY-N_MEM_RET_SPT	DY-N_OFF_EMU_SPT	DY-N_OFF_SPT	Reserved	STA_DB-G_RE-COV_SPT	STA_WRM_RST_SPT	STA_ON_SPT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [31:30]		DY-N_WRM_RST_SPT	DY-N_ON_SPT	DYN_-FUNC_RET_SPT	DYN_-FULL_RET_SPT	DY-N_MEM_OFF_SPT	DYN_LG-C_RET_SPT

Bits	Name	Description
29	DYN_WRM_RST_SPT	Dynamic WARM_RST support. Default Value: 0x0
28	DYN_ON_SPT	Dynamic ON support. Default Value: 0x1
27	DYN_FUNC_RET_SPT	Dynamic FUNC_RET support. Default Value: 0x0
26	DYN_FULL_RET_SPT	Dynamic FULL_RET support. Default Value: 0x1
25	DYN_MEM_OFF_SPT	Dynamic MEM_OFF support. Default Value: 0x0
24	DYN_LGC_RET_SPT	Dynamic LOGIC_RET support. Default Value: 0x0
23	DY-N_MEM_RET_EMU_SPT	Dynamic MEM_RET_EMU support Default Value: 0x0
22	DYN_MEM_RET_SPT	Dynamic MEM_RET support. Default Value: 0x0

1.1.63 CPUSS_PPU_IDR0 (continued)

21	DYN_OFF_EMU_SPT	Dynamic OFF_EMU support. Default Value: 0x0
20	DYN_OFF_SPT	Dynamic OFF support. Default Value: 0x1
18	STA_DBG_RECOV_SPT	DBG_RECOV support. Default Value: 0x0
17	STA_WRM_RST_SPT	WARM_RST support. Ignore this bit. Do not use WARM_RST. Default Value: 0x1
16	STA_ON_SPT	ON support. Default Value: 0x1
15	STA_FUNC_RET_SPT	FUNC_RET support. Default Value: 0x0
14	STA_FULL_RET_SPT	FULL_RET support. Default Value: 0x1
13	STA_MEM_OFF_SPT	MEM_OFF support. Default Value: 0x0
12	STA_LGC_RET_SPT	LOGIC_RET support. Default Value: 0x0
11	STA_MEM_RET_EMU_SPT	MEM_RET_EMU support. Default Value: 0x0
10	STA_MEM_RET_SPT	MEM_RET support. Default Value: 0x0
9	STA_OFF_EMU_SPT	OFF_EMU support. Default Value: 0x0
8	STA_OFF_SPT	OFF support. Default Value: 0x1
7 : 4	NUM_OPMODE	No. of operating modes supported is NUM_OPMODE + 1. Default Value: 0x0
3 : 0	DEVCHAN	No. of Device Interface Channels. 0: This is a P-Channel PPU. Refer to PPU_IDR1.OP_ACTIVE for the number of DEVPACTIVE inputs and their meaning. non-zero: The value is the number of Q-Channels. The device enumeration is: Device 0: SRSS PDCM, Device 1: CPUSS SEQ between SS level LPD500 EXP & PERI Q-Channel Default Value: 0x2

1.1.64 CPUSS_PPU_IDR1

Description: PPU Identification Register 1

Address: 0x42225FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	Reserved	R	R	R
HW Access	Reserved	RW	RW	RW	Reserved	RW	RW	RW
Name	Reserved	FUNC_RET_RAM_REG	FULL_RET_RAM_REG	MEM_RET_RAM_REG	Reserved	LOCK_SPT	SW_DEV_DEL_SPT	PWR_MODE_ENTRY_DEL_SPT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved	R	R	R
HW Access	Reserved			RW	Reserved	RW	RW	RW
Name	Reserved [15:13]			OFF_MEM_RET_TRANS	Reserved	OP_ACTIVE	STA_POLICY_OP_IRQ_SPT	STA_POLICY_PWR_IRQ_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	OFF_MEM_RET_TRANS	OFF to MEM_RET direct transition. Indicates if direct transitions from OFF to MEM_RET and from OFF_EMU to MEM_RET_EMU are supported. Default Value: 0x0
10	OP_ACTIVE	Operating mode use model for dynamic transitions. 0: Ladder use model. 1: Independent use model. When operating modes are not supported (PPU_IDR0.NUM_OPMODE==0), this field is reserved. Default Value: 0x0
9	STA_POLICY_OP_IRQ_SPT	Operating policy transition completion event status. Default Value: 0x0
8	STA_POLICY_PWR_IRQ_SPT	Power policy transition completion event status. Default Value: 0x0
6	FUNC_RET_RAM_REG	Indicates if the PPU_FUNRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
5	FULL_RET_RAM_REG	Indicates if the PPU_FULRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
4	MEM_RET_RAM_REG	Indicates if the PPU_MEMRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0

1.1.64 CPUSS_PPU_IDR1 (continued)

2	LOCK_SPT	Lock and the lock interrupt event are supported. Default Value: 0x0
1	SW_DEV_DEL_SPT	Software device delay control configuration support. Default Value: 0x0
0	PWR_MODE_EN- TRY_DEL_SPT	Power mode entry delay support. Default Value: 0x0

1.1.65 CPUSS_PPU_IIDR

Description: Implementation Identification Register

Address: 0x42225FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IMPLEMENTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	REVISION [15:12]				IMPLEMENTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PRODUCT_ID [23:20]				VARIANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 20	PRODUCT_ID	PPU part identification. Default Value: 0x0B5
19 : 16	VARIANT	Major revision of the product. Default Value: 0
15 : 12	REVISION	Minor revision of the product. Default Value: 0
11 : 0	IMPLEMENTER	Implementer identification. [11:8] The JEP106 continuation code of the implementer. [7] Always 0. [6:0] The JEP106 identity code of the implementer. For an Arm implementation, bits [11:0] are 0x43B. Default Value: 0x43B

1.1.66 CPUSS_PPU_AIDR

Description: Architecture Identification Register

Address: 0x42225FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	ARCH_REV_MAJOR [7:4]				ARCH_REV_MINOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ARCH_REV_MAJOR	0x1 - PPU architecture major revision 1. Other Values - Reserved. Default Value: 0x1
3 : 0	ARCH_REV_MINOR	0x1 - PPU Architecture minor revision 1. Other Values - Reserved. Default Value: 0x1

1.1.67 CPUSS_PPU_PID4

Description: Implementation Defined Identification Register (PID4)

Address: 0x42225FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				IMPLEMENTER_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	IMPLEMENTER_11_8	The JEP106 continuation code of the implementer, which is 0x4 hardcoded value. Default Value: 0x4

1.1.68 CPUSS_PPU_PID0

Description: Implementation Defined Identification Register (PID0)

Address: 0x42225FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID_7_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PRODUCT_ID_7_0	PPU part identification bits [7:0]. Default Value: 0xB5

1.1.69 CPUSS_PPU_PID1

Description: Implementation Defined Identification Register (PID1)

Address: 0x42225FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	IMPLEMENTER_3_0 [7:4]				PRODUCT_ID_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	IMPLEMENTER_3_0	JEP106_ID bits [3:0] Default Value: 0xB
3 : 0	PRODUCT_ID_11_8	PPU part identification bits [11:8] Default Value: 0x0

1.1.70 CPUSS_PPU_PID2

Description: Implementation Defined Identification Register (PID2)

Address: 0x42225FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R	R		
HW Access	RW				RW	RW		
Name	REV_CONST [7:4]				CON-ST_HIGH	IMPLEMENTER_6_4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	REV_CONST	Constant LOW Revision (4 bits) Default Value: 0x0
3	CONST_HIGH	Constant HIGH Default Value: 0x1
2 : 0	IMPLEMENTER_6_4	JEP106_ID bits [6:4] Default Value: 0x3

1.1.71 CPUSS_PPU_PID3

Description: Implementation Defined Identification Register (PID3)

Address: 0x42225FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PID3_REVISION [7:4]				PID3_REV_CONST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	PID3_REVISION	Minor revision of the product. Default Value: 0x0
3 : 0	PID3_REV_CONST	Constant LOW (4 bits) Default Value: 0x0

1.1.72 CPUSS_PPU_ID0

Description: Implementation Defined Identification Register (ID0)

Address: 0x42225FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID0	ID0 hard coded value Default Value: 0x0D

1.1.73 CPUSS_PPU_ID1

Description: Implementation Defined Identification Register (ID1)

Address: 0x42225FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID1	ID1 hardcoded value Default Value: 0xF0

1.1.74 CPUSS_PPU_ID2

Description: Implementation Defined Identification Register (ID2)

Address: 0x42225FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID2	ID2 hardcoded value Default Value: 0x05

1.1.75 CPUSS_PPU_ID3

Description: Implementation Defined Identification Register (ID3)

Address: 0x42225FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID3	ID3 hardcoded value Default Value: 0xB1

1.1.76 MXCM33_CM33_CTL

Description: Control

Address: 0x42260000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			
HW Access	Reserved			R	Reserved			
Name	Reserved [7:5]			CPU_WAIT	Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	RW	RW	RW	RW
HW Access	Reserved			R	R	R	R	R
Name	Reserved [15:13]			LOCKSAU	LOCKNSM-PU	LOCKSM-PU	LOCKSVTAIRCR	LOCKNS-VTOR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved		RW	RW	RW	RW	RW
HW Access	R	Reserved		R	R	R	R	R
Name	IDC_MASK	Reserved [30:29]		IXC_MASK	UFC_MASK	OFC_MASK	DZC_MASK	IOC_MASK

Bits	Name	Description
31	IDC_MASK	CPU FPU exception mask for the CPU's FPCSR.IDC "input denormalized" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: if the CPU FPCSR.FZ field is set to '1', denormalized inputs are "flushed to zero". Dependent on the FPU algorithm, this may or may not occur frequently. To prevent frequent CPU FPU interrupts as a result of denormalized inputs, this field may be set to '0'. Default Value: 0
28	IXC_MASK	CPU FPU exception mask for the CPU's FPCSR.IXC "inexact" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the "inexact" condition is set as a result of rounding. Rounding may occur frequently and is typically not an error condition. To prevent frequent CPU FPU interrupts as a result of rounding, this field is typically set to '0'. Default Value: 0
27	UFC_MASK	CPU FPU exception mask for the CPU's FPCSR.UFC "underflow" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0
26	OFC_MASK	CPU FPU exception mask for the CPU's FPCSR.OFC "overflow" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0

1.1.76 MXCM33_CM33_CTL (continued)

25	DZC_MASK	CPU FPU exception mask for the CPU's FPCSR.DZC "divide by zero" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0
24	IOC_MASK	CPU floating point unit (FPU) exception mask for the CPU's FPCSR.IOC "invalid operation" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the ARM architecture does NOT support FPU exceptions; i.e. there is no precise FPU exception handler. Instead, FPU conditions are captured in the CPU's FPCSR register and the conditions are provided as CPU interface signals. The interface signals are "masked" with the fields provided by this register (CM33_CTL). The "masked" signals are reduced/OR-ed into a single CPU floating point interrupt signal. The associated CPU interrupt handler allows for imprecise handling of FPU exception conditions. Note: the CPU's FPCSR exception conditions are "sticky". Typically, the CPU FPU interrupt handler will clear the exception condition(s) to '0'. Note: by default, the FPU exception masks are '0'. Therefore, FPU exception conditions will NOT activate the CPU's floating point interrupt. Default Value: 0
12	LOCKSAU	Asserting this bit prevents changes to Secure SAU memory regions already programmed. All writes to the registers are ignored. '1': Disables writes to the SAU_CTRL, SAU_RNR, SAU_RBAR and SAU_RLAR registers from software or from a debug agent connected to the processor. '0': Unlocks these registers. This signal has no affect if the Cortex-M33 processor has not been configured with support for the Armv8-M Security Extension, or if no SAU regions have been configured. Default Value: 0
11	LOCKNSMPU	Asserting this bit prevents changes to Nonsecure MPU memory regions already programmed. All writes to the registers are ignored. '1': Disables writes to the MPU_CTRL_NS, MPU_RNR_NS, MPU_RBAR_NS, MPU_RLAR_NS, MPU_RBAR_A_NSn and MPU_RLAR_A_NSn from software or from a debug agent connected to the processor. '0': Unlocks these registers. This signal has no affect if the Cortex-M33 processor has been configured without any Nonsecure MPU regions. Default Value: 0
10	LOCKSMPU	Asserting this bit prevents changes to programmed Secure MPU memory regions and all writes to the registers are ignored. '1': Disables writes to the MPU_CTRL, MPU_RNR, MPU_RBAR, MPU_RLAR, MPU_RBAR_An and MPU_RLAR_An from software or from a debug agent connected to the processor in Secure state. '0': Unlocks these registers. This bit has no affect if the Cortex-M33 processor has not been configured with support for the Armv8-M Security Extension, or if no Secure MPU regions have been configured. Default Value: 0
9	LOCKSVTAIRCR	Asserting this bit prevents changes to: - The Secure vector table base address. - Handling of Secure interrupt priority. - BusFault, HardFault, and NMI security target settings in the processor. '1': Disables writes to the VTOR_S,AIRCR.PRIS, and AIRCR.BFHFNMINS registers. '0': Unlocks these registers. Default Value: 0
8	LOCKNSVTOR	Asserting this bit prevents changes to the Non-secure vector table base address. '1': Disables writes to the VTOR_NS register. '0': Unlocks this register. Default Value: 0
4	CPU_WAIT	When this signal is '1' out of reset, it forces the CPU into a quiescent state that delays its boot-up sequence and instruction execution until this signal is driven '0'. Default Value: 1

1.1.77 MXCM33_CM33_CMD

Description: Command

Address: 0x42260004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	Reserved
HW Access	Reserved						RW1S	Reserved
Name	Reserved [7:2]						ENABLED	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 0xFA05
1	ENABLED	Processor enable: '0': Disabled. Processor clock is turned off and reset is activated. After SW clears this field to '0', HW automatically sets this field to '1'. This effectively results in a CM33 reset, followed by a CM33 warm boot. '1': Enabled. Note: The intent is that this bit is modified only through an external probe or by the other CM33 while this CM33 is in Sleep or DeepSleep power mode. If this field is cleared to '0' by this CM33 itself, it should be done under controlled conditions (such that undesirable side effects can be prevented). Note: The CM33 CPU has a AIRCR.SYSRESETREQ register field that allows the CM33 to reset the complete device (ENABLED only disables/enables the CM33), resulting in a warm boot. This CPU register field has similar "built-in protection" as this register to prevent accidental system writes (the upper 16-bits of the register need to be written with a 0x05fa key value; see CPU user manual for more details). Default Value: 1

1.1.78 MXCM33_CM33_STATUS

Description: Status

Address: 0x42260008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						SLEEP-DEEP	SLEEPING

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SLEEPDEEP	Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. Default Value: 0
0	SLEEPING	Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. Default Value: 0

1.1.79 MXCM33_CM33_NMI_CTL0

Description: CM33 NMI control

Address: 0x42260080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	SYSTEM_INT_IDX	System interrupt select for CPU NMI. The reset value ("1023") ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. Default Value: 1023

1.1.80 MXCM33_CM33_EVENT_CTL

Description: CM33 event control

Address: 0x422600C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			MASK [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	MASK	One mask bit for each CPU (other than itself). 0: Mask is not set. 1: RX event from the corresponding CPU is masked. Bit 0: Other CM33 CPU event Bit 1: CM55_0 CPU event Bit 2: CM55_1 CPU event Bit 3: CM55_2 CPU event Bit 4: CM55_3 CPU event Default Value: 0

1.1.81 MXCM33_CM33_S_VECTOR_TABLE_BASE

Description: CM33 secure vector table base

Address: 0x42261000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ADDR25	Reserved [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR25 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR25 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR25 [31:24]							

Bits	Name	Description
31 : 7	ADDR25	Address of CM33 secure vector table to be used at reset. Default value: ADDR25: 0x0200000 if PROM is present (points to Secure ROM start address i.e. 0x1000_0000). ADDR25: 0x0680000 if PROM is not present (points to Secure RAMC0 start address i.e. 0x3400_0000). Default Value: 6815744

1.1.82 MXCM33_CM33_NS_VECTOR_TABLE_BASE

Description: CM33 non-secure vector table base

Address: 0x42261004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ADDR25	Reserved [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR25 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR25 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR25 [31:24]							

Bits	Name	Description
31 : 7	ADDR25	Address of CM33 non-secure vector table to be used at reset. Default value: ADDR25: 0x0000000 if PROM is present (points to Non-Secure ROM start address i.e. 0x0000_0000). ADDR25: 0x0480000 if PROM is not present (points to Non-Secure RAMC0 start address i.e. 0x2400_0000). Default Value: 4718592

1.1.83 MXCM33_CM33_PC_CTL

Description: CM33 protection context control

Address: 0x42262000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				VALID [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	VALID	Valid fields for the protection context handler CM33_PCi_HANDLER registers: Bit 0: Valid field for CM33_PC0_HANDLER. Bit 1: Valid field for CM33_PC1_HANDLER. Bit 2: Valid field for CM33_PC2_HANDLER. Bit 3: Valid field for CM33_PC3_HANDLER. Default Value: 0

1.1.84 MXCM33_CM33_PC0_HANDLER

Description: CM33 protection context 0 handler

Address: 0x42262040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 0 handler. This field is used to detect entry to Cypress "trusted" code through an exception/interrupt. Default Value: 0

1.1.85 MXCM33_CM33_PC1_HANDLER

Description: CM33 protection context 1 handler

Address: 0x42262100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 1 handler. Default Value: 0

1.1.86 MXCM33_CM33_PC2_HANDLER

Description: CM33 protection context 2 handler

Address: 0x42262140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 2 handler. Default Value: 0

1.1.87 MXCM33_CM33_PC3_HANDLER

Description: CM33 protection context 3 handler

Address: 0x42262180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 3 handler. Default Value: 0

1.1.88 CPUSS_IDENTITY

Description: Identity

Address: 0x42290000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved		R	R
HW Access	W				Reserved		W	W
Name	PC [7:4]				Reserved [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [15:14]		MS [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
13 : 8	MS	This field specifies the bus master identifier of the transfer that reads the register. Default Value: Undefined
7 : 4	PC	This field specifies the protection context of the transfer that reads the register. Default Value: Undefined
1	NS	This field specifies the security setting ('0': secure mode; '1': non-secure mode) of the transfer that reads the register. Default Value: Undefined
0	P	This field specifies the privileged setting ('0': user mode; '1': privileged mode) of the transfer that reads the register. Default Value: Undefined

1.1.89 CPUSS_PRODUCT_ID

Description: Product identifier and version (same as CoreSight RomTables)

Address: 0x42290010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FAMILY_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [15:12]				FAMILY_ID [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	W				W			
Name	MINOR_REV [23:20]				MAJOR_REV [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 20	MINOR_REV	Minor Revision, starts with 1, increments with metal layer only tape-out (implemented with metal ECO-able tie-off) Default Value: Undefined
19 : 16	MAJOR_REV	Major Revision, starts with 1, increments with all layer tape-out (implemented with metal ECO-able tie-off) Default Value: Undefined
11 : 0	FAMILY_ID	Family ID. Common ID (Partnumber a.k.a. Silicon ID) for a product family. Default Value: 277

1.1.90 CPUSS_DP_STATUS

Description: Debug port status

Address: 0x42290020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [7:4]				SWJ_SWD_SEL	SWJ_-JTAG_SEL	SWJ_DE-BUG_EN	SWJ_CON-NECTED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	SWJ_SWD_SEL	Specifies if the SWD interface is selected. '0': SWD not selected. '1': SWD selected. Default Value: 0
2	SWJ_JTAG_SEL	Specifies if the JTAG interface is selected. '0': JTAG not selected. '1': JTAG selected. Default Value: 0
1	SWJ_DEBUG_EN	Specifies if SWJ debug is enabled, i.e. CDBGPWRUPACK is '1' and thus debug clocks are on: '0': Disabled. '1': Enabled. Default Value: 0
0	SWJ_CONNECTED	Specifies if the SWJ debug port is connected; i.e. debug host interface is active: '0': Not connected/not active. '1': Connected/active. Default Value: 0

1.1.91 CPUSS_BUFF_CTL

Description: Buffer control

Address: 0x42290030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							WRITE_BUFF

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	WRITE_BUFF	Specifies if write transfer can be buffered in the bus infrastructure bridges: '0': Write transfers are not buffered, independent of the transfer's bufferable attribute. '1': Write transfers can be buffered, if the transfer's bufferable attribute indicates that the transfer is a bufferable/posted write. This bit controls buffering only for subsystems that interfaced using the AHB2AHB bridge, not for components utilised from the ARM SIE200, such as the 32-bit SYS interconnect in SYSCPUSS, Peripheral Group0, MSC etc. Default Value: 1

1.1.92 CPUSS_CAL_SUP_SET

Description: Calibration support set and read

Address: 0x42290040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Read without side effect, write 1 to set Default Value: 0

1.1.93 CPUSS_CAL_SUP_CLR

Description: Calibration support clear and reset

Address: 0x42290044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	A							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	A							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	A							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Read side effect: when read all bits are cleared, write 1 to clear a specific bit Note: no exception for the debug host, it also causes the read side effect Default Value: 0

1.1.94 CPUSS_INFRA_CTL

Description: Infrastructure Control

Address: 0x42290050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							CLOCK_-FORCE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CLOCK_FORCE	Force Infrastructure clock gating to be always ON. 0: Disabled 1: Enabled Default Value: 0

1.1.95 CPUSS_SYSTICK_S_CTL

Description: Secure SysTick timer control

Address: 0x42290100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved				RW	
HW Access	R	R	Reserved				R	
Name	NOREF	SKEW	Reserved [29:26]				CLOCK_SOURCE [25:24]	

Bits	Name	Description
31	NOREF	Specifies if an external clock source is provided: '0': An external clock source is provided. '1': An external clock source is NOT provided and only the CPU internal clock can be used as SysTick timer clock source. Default Value: 0
30	SKEW	Specifies the precision of the clock source and if the TENMS field represents exactly 10 ms (clock source frequency is a multiple of 100 Hz). This affects the suitability of the SysTick timer as a SW real-time clock: '0': Precise. '1': Imprecise. Default Value: 1
25 : 24	CLOCK_SOURCE	Specifies an external clock source: "0": The low frequency clock "clk_lf" is selected. The precision of this clock depends on whether the low frequency clock source is a SRSS internal RC oscillator (imprecise) or a device external crystal oscillator (precise). "1": The internal main oscillator (IMO) clock "clk_imo" is selected. o "2": The external crystal oscillator (ECO) clock "clk_eco" is selected. "3": The SRSS "clk_timer" is selected ("clk_timer" is a divided/gated version of "clk_hf" or "clk_imo"). Note: If NOREF is '1', the CLOCK_SOURCE value is NOT used. Note: It is SW's responsibility to provide the correct NOREF, SKEW and TENMS field values for the selected clock source. Default Value: 0
23 : 0	TENMS	Specifies the number of clock source cycles (minus 1) that make up 10 ms. E.g., for a 32,768 Hz reference clock, TENMS is 328 - 1 = 327. Default Value: 327

1.1.96 CPUSS_SYSTICK_NS_CTL

Description: Non Secure SysTick timer control

Address: 0x42290120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved				RW	
HW Access	R	R	Reserved				R	
Name	NOREF	SKEW	Reserved [29:26]				CLOCK_SOURCE [25:24]	

Bits	Name	Description
31	NOREF	Specifies if an external clock source is provided: '0': An external clock source is provided. '1': An external clock source is NOT provided and only the CPU internal clock can be used as SysTick timer clock source. Default Value: 0
30	SKEW	Specifies the precision of the clock source and if the TENMS field represents exactly 10 ms (clock source frequency is a multiple of 100 Hz). This affects the suitability of the SysTick timer as a SW real-time clock: '0': Precise. '1': Imprecise. Default Value: 1
25 : 24	CLOCK_SOURCE	Specifies an external clock source: "0": The low frequency clock "clk_lf" is selected. The precision of this clock depends on whether the low frequency clock source is a SRSS internal RC oscillator (imprecise) or a device external crystal oscillator (precise). "1": The internal main oscillator (IMO) clock "clk_imo" is selected. o "2": The external crystal oscillator (ECO) clock "clk_eco" is selected. "3": The SRSS "clk_timer" is selected ("clk_timer" is a divided/gated version of "clk_hf" or "clk_imo"). Note: If NOREF is '1', the CLOCK_SOURCE value is NOT used. Note: It is SW's responsibility to provide the correct NOREF, SKEW and TENMS field values for the selected clock source. Default Value: 0
23 : 0	TENMS	Specifies the number of clock source cycles (minus 1) that make up 10 ms. E.g., for a 32,768 Hz reference clock, TENMS is 328 - 1 = 327. Default Value: 327

1.1.97 CPUSS_INTR_MSC

Description: Master security controller Interrupt

Address: 0x42290200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1C	RW1C	RW1C	RW1C
HW Access	Reserved				A	A	A	A
Name	Reserved [7:4]				EXP_MS_MSC	SYS_MS1_MSC	SYS_MS0_MSC	CODE_MS0_MSC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	EXP_MS_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on SYSCPUSS external EXP AHB5 bus master interfaces. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0
2	SYS_MS1_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on SYSCPUSS external SYS AHB5 bus master interface 1. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0
1	SYS_MS0_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on SYSCPUSS external SYS AHB5 bus master interface 0. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0
0	CODE_MS0_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on SYSCPUSS external CODE AHB5 bus master interface 0. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0

1.1.98 CPUSS_INTR_MASK_MSC

Description: Master security controller Interrupt mask

Address: 0x42290208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				EXP_MS_MSC	SYS_MS1_MSC	SYS_MS0_MSC	CODE_MS0_MSC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	EXP_MS_MSC	Mask bit for the corresponding field in the SYSCPUSS_INTR_MSC register. Default Value: 0
2	SYS_MS1_MSC	Mask bit for the corresponding field in the SYSCPUSS_INTR_MSC register. Default Value: 0
1	SYS_MS0_MSC	Mask bit for the corresponding field in the SYSCPUSS_INTR_MSC register. Default Value: 0
0	CODE_MS0_MSC	Mask bit for the corresponding field in the SYSCPUSS_INTR_MSC register. Default Value: 0

1.1.99 CPUSS_INTR_MASKED_MSC

Description: Master security controller Interrupt masked

Address: 0x4229020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [7:4]				EXP_MS_MSC	SYS_MS1_MSC	SYS_MS0_MSC	CODE_MS0_MSC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	EXP_MS_MSC	Logical AND of corresponding SYSCPUSS_INTR_MSC and SYSCPUSS_INTR_MASK_MSC bit fields. Default Value: 0
2	SYS_MS1_MSC	Logical AND of corresponding SYSCPUSS_INTR_MSC and SYSCPUSS_INTR_MASK_MSC bit fields. Default Value: 0
1	SYS_MS0_MSC	Logical AND of corresponding SYSCPUSS_INTR_MSC and SYSCPUSS_INTR_MASK_MSC bit fields. Default Value: 0
0	CODE_MS0_MSC	Logical AND of corresponding SYSCPUSS_INTR_MSC and SYSCPUSS_INTR_MASK_MSC bit fields. Default Value: 0

1.1.100 CPUSS_AP_CTL

Description: Access port control

Address: 0x42291000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	Reserved	RW	RW	RW
HW Access	R	R	R	R	Reserved	R	R	R
Name	CM33_0_SPNID_ENABLE	CM33_0_SPID_ENABLE	CM33_0_NID_ENABLE	CM33_0_DBG_ENABLE	Reserved	SYS_ENABLE	CM33_1_ENABLE	CM33_0_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	Reserved	RW	Reserved		RW	RW
HW Access	Reserved	R	Reserved	R	Reserved		R	R
Name	Reserved	SYS_SECURE_ENABLE	Reserved	CM33_0_SECURE_ENABLE	Reserved [11:10]		CM33_1_NID_ENABLE	CM33_1_DBG_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	Reserved	RW1S	RW1S	RW1S
HW Access	R	R	R	R	Reserved	R	R	R
Name	CM33_0_SPNID_DISABLE	CM33_0_SPID_DISABLE	CM33_0_NID_DISABLE	CM33_0_DBG_DISABLE	Reserved	SYS_DISABLE	CM33_1_DISABLE	CM33_0_DISABLE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW1S	Reserved	RW1S	Reserved		RW1S	RW1S
HW Access	Reserved	R	Reserved	R	Reserved		R	R
Name	Reserved	SYS_SECURE_DISABLE	Reserved	CM33_0_SECURE_DISABLE	Reserved [27:26]		CM33_1_NID_DISABLE	CM33_1_DBG_DISABLE

Bits	Name	Description
30	SYS_SECURE_DISABLE	Disables the system secure AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Infineon boot code with information from OTP memory. The access port is only enabled when SYS_SECURE_DISABLE is '0' and SYS_SECURE_ENABLE is '1'. Default Value: 0
28	CM33_0_SECURE_DISABLE	Disables the CM33_0 secure AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Infineon boot code with information from OTP memory. The access port is only enabled when CM33_0_DISABLE is '0' and CM33_0_ENABLE is '1'. Default Value: 0

1.1.100 CPUSS_AP_CTL (continued)

25	CM33_1_NID_DISABLE	Disable Non-invasive debug for CM33_1. '1': Disables all trace and non-invasive debug features. '0': Enables all trace and non-invasive debug features. Typically, this field is set by the Infineon boot code with information from OTP memory. The non-invasive debug is only enabled when CM33_1_NID_DISABLE is '0' and CM33_1_NID_ENABLE is '1'. Default Value: 0
24	CM33_1_DBG_DISABLE	Disable Invasive debug for CM33_1. '1': Disables all halt-mode and invasive debug features. '0': Enables invasive debug features. Typically, this field is set by the Infineon boot code with information from OTP memory. The invasive debug is only enabled when CM33_1_DBG_DISABLE is '0' and CM33_1_DBG_ENABLE is '1'. Default Value: 0
23	CM33_0_SPNID_DISABLE	Secure non-invasive debug disable for CM33_0. '1': Disables non-invasive debug features when the processor is in Secure state. '0': Enables non-invasive debug features when the processor is in Secure state. Typically, this field is set by the Infineon boot code with information from OTP memory. The non-invasive debug in secure state is only enabled when CM33_0_SPNID_DISABLE is '0' and CM33_0_SPNID_ENABLE is '1'. Default Value: 0
22	CM33_0_SPID_DISABLE	Secure invasive debug disable for CM33_0. '1': disables all halt mode and invasive debug features when the processor is in Secure state. '0': Enables all halt mode and invasive debug features when the processor is in Secure state. Typically, this field is set by the Infineon boot code with information from OTP memory. The invasive debug in secure state is only enabled when CM33_0_SPID_DISABLE is '0' and CM33_0_SPID_ENABLE is '1'. Default Value: 0
21	CM33_0_NID_DISABLE	Disable Non-invasive debug for CM33_0. '1': Disables all trace and non-invasive debug features. '0': Enables all trace and non-invasive debug features. Typically, this field is set by the Infineon boot code with information from OTP memory. The non-invasive debug is only enabled when CM33_0_NID_DISABLE is '0' and CM33_0_NID_ENABLE is '1'. Default Value: 0
20	CM33_0_DBG_DISABLE	Disable Invasive debug for CM33_0. '1': Disables all halt-mode and invasive debug features. '0': Enables invasive debug features. Typically, this field is set by the Infineon boot code with information from OTP memory. The invasive debug is only enabled when CM33_0_DBG_DISABLE is '0' and CM33_0_DBG_ENABLE is '1'. Default Value: 0
18	SYS_DISABLE	Disables the system AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Infineon boot code with information from OTP memory. The access port is only enabled when SYS_DISABLE is '0' and SYS_ENABLE is '1'. Default Value: 0
17	CM33_1_DISABLE	Disables the CM33_1 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Infineon boot code with information from OTP memory. The access port is only enabled when CM33_1_DISABLE is '0' and CM33_1_ENABLE is '1'. Default Value: 0
16	CM33_0_DISABLE	Disables the CM33_0 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Infineon boot code with information from OTP memory. The access port is only enabled when CM33_0_DISABLE is '0' and CM33_0_ENABLE is '1'. Default Value: 0

1.1.100 CPUSS_AP_CTL (continued)

14	SYS_SECURE_ENABLE	Enables the system secure AP interface: '0': Disabled. '1': Enabled. Default Value: 0
12	CM33_0_SECURE_ENABLE	Enables the CM33_0 secure AP interface: '0': Disabled. '1': Enabled. Default Value: 0
9	CM33_1_NID_ENABLE	Non-invasive debug enable for CM33_1. '0': Disables all trace and non-invasive debug features. '1': Enables all trace and non-invasive debug features. Default Value: 0
8	CM33_1_DBG_ENABLE	Invasive debug enable for CM33_1. '0': Disables all halt-mode and invasive debug features. '1': Enables invasive debug features. Default Value: 0
7	CM33_0_SPNID_ENABLE	Secure non-invasive debug enable for CM33_0. '0': Disables non-invasive debug features when the processor is in Secure state. '1': Enables non-invasive debug features when the processor is in Secure state. Default Value: 0
6	CM33_0_SPID_ENABLE	Secure invasive debug enable for CM33_0. '0': disables all halt mode and invasive debug features when the processor is in Secure state. '1': Enables all halt mode and invasive debug features when the processor is in Secure state. Default Value: 0
5	CM33_0_NID_ENABLE	Non-invasive debug enable for CM33_0. '0': Disables all trace and non-invasive debug features. '1': Enables all trace and non-invasive debug features. Default Value: 0
4	CM33_0_DBG_ENABLE	Invasive debug enable for CM33_0. '0': Disables all halt-mode and invasive debug features. '1': Enables invasive debug features. Default Value: 1
2	SYS_ENABLE	Enables the system AP interface: '0': Disabled. '1': Enabled. Default Value: 0
1	CM33_1_ENABLE	Enables the CM33_1 AP interface: '0': Disabled. '1': Enabled. Default Value: 0
0	CM33_0_ENABLE	Enables the CM33_0 AP interface: '0': Disabled. '1': Enabled. Default Value: 0

1.1.101 CPUSS_PROTECTION

Description: Protection status

Address: 0x42292004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STATE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	STATE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	STATE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	STATE [31:24]							

Bits	Name	Description
31 : 0	STATE	Protection state: PROTECTION is "0x5B719A4F": UNKNOWN state. PROTECTION is "0x5D48F714": VIRGIN state. PROTECTION is "0xC39D5455": OPEN state PROTECTION is "0x652372F7": NORMAL state. PROTECTION is "0x8DF117A1": SECURE state. PROTECTION is "0xFBF6D1B6": RMA state PROTECTION is "0x2E94B3DD": DEAD state. PROTECTION is "0x3A5BC6F1": CORRUPTED state. PROTECTION is "0x3F80442F": TESTMODE state. The following state transitions are allowed (and enforced by HW): - UNKNOWN => VIRGIN/RMA/OPEN/NORMAL/SECURE/DEAD/CORRUPTED - RMA/OPEN/NORMAL/SECURE => DEAD - RMA/OPEN/NORMAL/SECURE => TESTMODE - RMA/OPEN/NORMAL/SECURE => CORRUPTED An attempt to make a NOT allowed state transition will NOT affect this register field. Default Value: 0x5B719A4F **0x5b719a4f: UNKNOWN :** **0x5d48f714: VIRGIN :** **0xc39d5455: OPEN :** **0x652372f7: NORMAL :**

1.1.101 CPUSS_PROTECTION (continued)

0x8df117a1: SECURE :

0xfbf6d1b6: RMA :

0x2e94b3dd: DEAD :

0x3a5bc6f1: CORRUPTED :

0x3f80442f: TESTMODE :

1.1.102 MS0_CTL

Description: Master 'x' protection context control

Address: 0x42294000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PC_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	PC_MASK	Protection context mask for protection contexts "15" down to "0". Bit PC_MASK[i] indicates if the MS_PC_STRUCT[x].PC[3:0] protection context field can be set to the value "i": - PC_MASK[i] is '0': MS_PC_STRUCT[x].PC[3:0] can NOT be set to "i"; and PC[3:0] is not changed. - PC_MASK[i] is '1': MS_PC_STRUCT[x].PC[3:0] can be set to "i". Note: When CM33_0 CM33_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK[i] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 0, 1, 2 or 3 through HW (HW modifies MS_PC_STRUCT[x].PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts. Default Value: 4

1.1.103 MS6_CTL

Description: Master 'x' protection context control

Address: 0x42294060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PC_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	PC_MASK	Protection context mask for protection contexts "15" down to "0". Bit PC_MASK[i] indicates if the MS_PC_STRUCT[x].PC[3:0] protection context field can be set to the value "i": - PC_MASK[i] is '0': MS_PC_STRUCT[x].PC[3:0] can NOT be set to "i"; and PC[3:0] is not changed. - PC_MASK[i] is '1': MS_PC_STRUCT[x].PC[3:0] can be set to "i". Note: When CM33_0 CM33_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK[i] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 0, 1, 2 or 3 through HW (HW modifies MS_PC_STRUCT[x].PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts. Default Value: 4
1	NS	Master security controller configuration. 0: Bus master is secure. Master can send both secure and non-secure transfers. Accesses to secure addresses are not blocked and the security flag, HNONSEC, is set accordingly. 1: Bus master is non-secure. Master can send only non-secure transfers. Access to secure addresses, that is, outside the Uncheck regions, are blocked. Default Value: 0
0	P	Privileged setting ('0': user mode; '1': privileged mode). Notes: This field is ONLY used for masters that do NOT provide their own user/privileged access control attribute. The default/reset field value provides privileged mode access capabilities. Default Value: 1

1.1.104 MS_PC0_PC

Description: Master 'x' protection context value

Address: 0x42295000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				RW			
Name	Reserved [23:20]				PC_SAVED [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 16	PC_SAVED	Saved protection context. Modifications to this field are constrained by the associated MS_CTL_STRUCT[x].CTL.PC_MASK. Note: this field is ONLY used by the CM33_0. Default Value: 2

3 : 0	PC	Active protection context (PC). Modifications to this field are constrained by the associated MS_CTL_STRUCT[x].CTL.PC_MASK value. PC[3:0] can be set to "i" only if the corresponding mask bit (PC_MASK[i]) is '1'.
		The CM33_0 PC register is special: the PC field is modifiable by BOTH HW and SW (for all other masters, the PC field is modifiable by SW ONLY. For CM33_0 PC field HW modifications, the following holds:
		* On entry of a CM33_PC0/1/2/3_HANDLER exception/interrupt handler:
		IF (the new PC is the same as MS_PC_STRUCT[0].PC)
		PC is not affected; PC_SAVED is not affected.
		ELSE IF (CM33_PC_CTL.VALID[MS_PC_STRUCT[0].PC])
		An AHB5 bus error is generated for the exception handler fetch;
		PC is not affected; PC_SAVED is not affected.
		ELSE
		PC = "new PC"; PC_SAVED = PC (push operation).
		* On entry of any other exception/interrupt handler:
		PC = PC_SAVED; PC_SAVED is not affected (pop operation).
		
		Note: this field is NOT used by the DW controllers, DMA controllers as they inherit the protection context from master that configures the corresponding channel.
		Default Value: 2

1.1.105 MS_PC0_PC_READ_MIR

Description: Master 'x' protection context value read mirror register

Address: 0x42295004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [23:20]				PC_SAVED [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 16	PC_SAVED	Read-only mirror of PC.PC_SAVED Default Value: 2
3 : 0	PC	Read-only mirror of PC.PC Default Value: 2

1.1.106 MS_PC6_PC

Description: Master 'x' protection context value

Address: 0x42295060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description

3 : 0	PC	Active protection context (PC). Modifications to this field are constrained by the associated MS_CTL_STRUCT[x].CTL.PC_MASK value. PC[3:0] can be set to "i" only if the corresponding mask bit (PC_MASK[i]) is '1'.
		The CM33_0 PC register is special: the PC field is modifiable by BOTH HW and SW (for all other masters, the PC field is modifiable by SW ONLY. For CM33_0 PC field HW modifications, the following holds:
		* On entry of a CM33_PC0/1/2/3_HANDLER exception/interrupt handler:
		IF (the new PC is the same as MS_PC_STRUCT[0].PC)
		PC is not affected; PC_SAVED is not affected.
		ELSE IF (CM33_PC_CTL.VALID[MS_PC_STRUCT[0].PC])
		An AHB5 bus error is generated for the exception handler fetch;
		PC is not affected; PC_SAVED is not affected.
		ELSE
		PC = "new PC"; PC_SAVED = PC (push operation).
		* On entry of any other exception/interrupt handler:
		PC = PC_SAVED; PC_SAVED is not affected (pop operation).
		
		Note: this field is NOT used by the DW controllers, DMA controllers as they inherit the protection context from master that configures the corresponding channel.
		Default Value: 2

1.1.107 MS_PC6_PC_READ_MIR

Description: Master 'x' protection context value read mirror register

Address: 0x42295064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	PC	Read-only mirror of PC.PC Default Value: 2

1.1.108 CODE_MS0_MSC_ACG_CTL

Description: CODE_MS0 master security Controller & ACG configuration

Address: 0x42296000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.109 SYS_MS0_MSC_ACG_CTL

Description: SYS_MS0 master security Controller & ACG configuration

Address: 0x42296010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.110 SYS_MS1_MSC_ACG_CTL

Description: SYS_MS1 master security Controller & ACG configuration

Address: 0x42296014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.111 EXP_MS_MSC_ACG_CTL

Description: EXP_MS master security Controller & ACG configuration

Address: 0x42296020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.112 CPUSS_SL_CTL_SL_CTL

Description: Slave control (Clock enables)

Address: 0x42298000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	Reserved	RW	RW	Reserved	RW	Reserved
HW Access	R	R	Reserved	R	R	Reserved	R	Reserved
Name	DW1_ENABLED	DW0_ENABLED	Reserved	RAMC1_ENABLED	RAMC0_ENABLED	Reserved	RRAMC_ENABLED	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW	RW	Reserved	
HW Access	Reserved				R	R	Reserved	
Name	Reserved [15:12]				FAULT_ENABLED	IPC_ENABLED	Reserved [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	FAULT_ENABLED	Default Value: 1
10	IPC_ENABLED	Default Value: 1
7	DW1_ENABLED	Default Value: 1
6	DW0_ENABLED	Default Value: 1
4	RAMC1_ENABLED	Default Value: 1
3	RAMC0_ENABLED	Default Value: 1
1	RRAMC_ENABLED	Default Value: 1

1.1.113 CPUSS_SL_CTL_SL_CTL2

Description: Slave control2 (Reset enables)

Address: 0x42298004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	Reserved	RW	RW	Reserved	RW	Reserved
HW Access	R	R	Reserved	R	R	Reserved	R	Reserved
Name	DW1_RST	DW0_RST	Reserved	RAMC1_RST	RAMC0_RST	Reserved	RRAMC_RST	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW	RW	Reserved	
HW Access	Reserved				R	R	Reserved	
Name	Reserved [15:12]				FAULT_RST	IPC_RST	Reserved [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	FAULT_RST	Default Value: 0
10	IPC_RST	Default Value: 0
7	DW1_RST	Default Value: 0
6	DW0_RST	Default Value: 0
4	RAMC1_RST	Default Value: 0
3	RAMC0_RST	Default Value: 0
1	RRAMC_RST	Default Value: 0

1.1.114 M0SECCPUSS_STATUS_VERSION

Description: IP Version

Address: 0x42430100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	MINOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	MAJOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	MAJOR	IP Major Revision Number Local parameter M0SEC_VERSION[15:8] Default Value: Undefined
7 : 0	MINOR	IP Minor Revision Number Local parameter M0SEC_VERSION[7:0] Default Value: Undefined

1.1.115 PPU_APPCPUSS_PWPR

Description: Power Policy Register

Address: 0x44100000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			LOCK_EN	Reserved [11:9]			PWR_DYN_EN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							OP_DYN_EN

Bits	Name	Description
24	OP_DYN_EN	Reserved Default Value: 0x0
19 : 16	OP_POLICY	Reserved Default Value: 0x0
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. When this bit is set to 1 dynamic transitions are enabled for power modes, allowing transitions to be initiated by changes on power mode DEVACTIVE inputs. Default Value: 0x1
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), FULL_RET(5), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x8

1.1.116 PPU_APPCPUSS_PMER

Description: Power Mode Emulation Register

Address: 0x44100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							EMU_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	EMU_EN	Reserved Default Value: 0x0

1.1.117 PPU_APPCPUSS_PWSR

Description: Power Status Register

Address: 0x44100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PWR_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved			R
HW Access	Reserved			RW	Reserved			RW
Name	Reserved [15:13]			LOCK_STA-TUS	Reserved [11:9]			PWR_DY-N_STATUS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [23:20]				OP_STATUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [31:25]							OP_DY-N_STATUS

Bits	Name	Description
24	OP_DYN_STATUS	Reserved Default Value: 0x0
19 : 16	OP_STATUS	Reserved Default Value: 0x0
12	LOCK_STATUS	Reserved Default Value: 0x0
8	PWR_DYN_STATUS	Power mode dynamic transition status. When set to 1 power mode dynamic transitions are enabled. There might be a delay in dynamic transitions becoming active or inactive if the PPU is transitioning when PWR_DYN_EN is programmed. Default Value: 0x0
3 : 0	PWR_STATUS	Power mode status. These bits reflect the current power mode of the PPU. See PPU_PWPR.PWR_POLICY for power mode enumeration. Default Value: 0x0

1.1.118 PPU_APPCPUSS_DISR

Description: Device Interface Input Current Status Register

Address: 0x44100010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PWR_DEVACTIVE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					R		
HW Access	Reserved					RW		
Name	Reserved [15:11]					PWR_DEVACTIVE_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	OP_DEVACTIVE_STATUS [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVE_STATUS	Reserved Default Value: 0x0
10 : 0	PWR_DEVACTIVE_STATUS	Status of the power mode DEVACTIVE inputs. For Q-Channel: There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 0 is for the Q-Channel 0 DEVQACTIVE, and bit 1 for the QChannel 1 DEVQACTIVE. For a Q-Channel PPU bits [10:8] are always reserved as only 8 device interface QChannels are supported. For P-Channel: There is one bit for each bit of the power mode DEVPACTIVE inputs. For example, bit 10 is for DEVPACTIVE[10], and bit 9 is for DEVPACTIVE[9]. Bit 0 relates to DEVPACTIVE[0] and is always 0 Default Value: 0x0

1.1.119 PPU_APPCPUSS_MISR

Description: Miscellaneous Input Current Status Register

Address: 0x44100014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							PCSMPAC-CEPT_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DEVACCEPT_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DEVDENY_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	DEVDENY_STATUS	Status of the device interface DEVDENY inputs. There is one bit for each device interface DEVQDENY. For example, bit 16 is for Q-Channel 0 DEVQDENY, and bit 17 for Q-Channel 1 DEVQDENY. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
15 : 8	DEVACCEPT_STATUS	Status of the device interface DEVACCEPT inputs. There is one bit for each device interface DEVQACCEPTn. For example, bit 8 is for Q-Channel 0 DEVQACCEPTn and bit 9 for Q-Channel 1 DEVQACCEPTn. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
0	PCSMPACCEPT_STA-TUS	The status of the PCSMPACCEPT input. Default Value: 0x0

1.1.120 PPU_APPCPUSS_STSR

Description: Stored Status Register

Address: 0x44100018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	STORED_DEVDENY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	STORED_DEVDENY	Status of the DEVDENY signals from the last device interface Q-Channel transition. For Q-Channel: There is one bit for each device interface DEVQDENY. For example, bit 0 is for Q-Channel 0 DEVQDENY, and bit 1 for Q-Channel 1 DEVQDENY. Refer to PPU_DISR.PWR_DEVACTIVE_STATUS for device enumeration. Default Value: 0x0

1.1.121 PPU_APPCPUSS_UNLK

Description: Unlock register

Address: 0x4410001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							UNLOCK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	UNLOCK	Reserved Default Value: 0x0

1.1.122 PPU_APPCPUSS_PWCR

Description: Power Configuration Register

Address: 0x44100020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVREQEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PWR_DEVACTIVEEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_DEVACTIVEEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	OP_DEVACTIVEEN [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVEEN	Reserved Default Value: 0x00
18 : 8	PWR_DEVACTIVEEN	These bits enable the power mode DEVACTIVE inputs. When a bit is to 1 the related DEVACTIVE input is enabled, when set to 0 it is disabled. All available bits are reset to 1. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE, and bit 9 for the Q-Channel 1 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x03
7 : 0	DEVREQEN	When set to 1 enables the device interface handshake for transitions. All available bits are reset to 1. There is one bit for each device interface channel. For example, bit 0 is for Q-Channel 0, and bit 1 is for Q-Channel 1. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x03

1.1.123 PPU_APPCPUSS_PTCR

Description: Power Mode Transition Configuration Register

Address: 0x44100024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						DBG_RE-COV_POR ST_EN	WARM_RS T_DEVREQ EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	DBG_RE-COV_PORST_EN	Reserved Default Value: 0x0
0	WARM_RST_DEVREQEN	Transition behavior between ON and WARM_RST. This bit should not be modified when the PPU is in WARM_RST, or if the PPU is performing a transition, otherwise PPU behavior is UN-PREDICTABLE. 0: The PPU does not perform a device interface handshake when transitioning between ON and WARM_RST. 1: The PPU performs a device interface handshake when transitioning between ON and WARM_RST. This disables all Q-Channels for this transition. Default Value: 0x0

1.1.124 PPU_APPCPUSS_IMR

Description: Interrupt Mask Register

Address: 0x44100030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		LOCKED_IRQ_MASK	EMU_DENY_IRQ_MASK	EMU_ACCEPT_IRQ_MASK	STA_DENY_IRQ_MASK	STA_ACCEPT_IRQ_MASK	STA_POLICY_TRN_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	LOCKED_IRQ_MASK	Reserved Default Value: 0x0
4	EMU_DENY_IRQ_MASK	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ_MASK	Reserved Default Value: 0x0
2	STA_DENY_IRQ_MASK	Static transition denial event mask. Default Value: 0x0
1	STA_ACCEPT_IRQ_MASK	Static transition acceptance event mask. Default Value: 0x1
0	STA_POLICY_TRN_IRQ_MASK	Static full policy transition completion event mask. Default Value: 0x0

1.1.125 PPU_APPCPUSS_AIMR

Description: Additional Interrupt Mask Register

Address: 0x44100034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	RW	RW	RW
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ_MASK	STA_POLICY_PWR_IRQ_MASK	DYN_DENY_IRQ_MASK	DYN_ACCEPT_IRQ_MASK	UNSPT_POLICY_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ_MASK	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ_MASK	Reserved Default Value: 0x0
2	DYN_DENY_IRQ_MASK	Dynamic transition denial event mask. Default Value: 0x1
1	DYN_ACCEPT_IRQ_MASK	Dynamic transition acceptance event mask. Default Value: 0x1
0	UNSPT_POLICY_IRQ_MASK	Unsupported Policy event mask. Default Value: 0x0

1.1.126 PPU_APPCPUSS_ISR

Description: Interrupt Status Register

Address: 0x44100038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	Reserved	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	Reserved	R	R	R	R	R	R
Name	OTH-ER_IRQ	Reserved	LOCKED_IRQ	EMU_DE-NY_IRQ	EMU_AC-CEPT_IRQ	STA_DE-NY_IRQ	STA_AC-CEPT_IRQ	STA_POLI-CY_TRN_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	PWR_ACTIVE_EDGE_IRQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW1C		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_ACTIVE_EDGE_IRQ [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	OP_ACTIVE_EDGE_IRQ [31:24]							

Bits	Name	Description
31 : 24	OP_ACTIVE_EDGE_IRQ	Indicates which operating mode DEVPACTIVE inputs caused the input edge event. When operating modes are not supported this field is reserved. Default Value: 0x0
18 : 8	PWR_ACTIVE_EDGE_IRQ	Indicates which power mode DEVACTIVE inputs caused the input edge event. Bits for unused channels are the MSBs and are reserved. There is one bit for each device Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x00
7	OTHER_IRQ	Indicates there is an interrupt event pending in the Additional Interrupt Status Register (PPU_AISR). Default Value: 0x0
5	LOCKED_IRQ	Reserved Default Value: 0x0
4	EMU_DENY_IRQ	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ	Reserved Default Value: 0x0
2	STA_DENY_IRQ	Static transition denial event status. Default Value: 0x0
1	STA_ACCEPT_IRQ	Static transition acceptance event status. Default Value: 0x0

1.1.126 PPU_APPCPUSS_ISR (continued)

0	STA_POLICY_TRN_IRQ	Static full policy transition completion event status. Default Value: 0x0

1.1.127 PPU_APPCPUSS_AISR

Description: Additional Interrupt Status Register

Address: 0x4410003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ	STA_POLICY_PWR_IRQ	DYN_DENY_IRQ	DYN_ACCEPT_IRQ	UNSPT_POLICY_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ	Reserved Default Value: 0x0
2	DYN_DENY_IRQ	Dynamic transition denial event status. Default Value: 0x0
1	DYN_ACCEPT_IRQ	Dynamic transition acceptance event status. Default Value: 0x0
0	UNSPT_POLICY_IRQ	Unsupported Policy event status. Default Value: 0x0

1.1.128 PPU_APPCPUSS_IESR

Description: Input Edge Sensitivity Register

Address: 0x44100040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE03_EDGE [7:6]		DEVACTIVE02_EDGE [5:4]		DEVACTIVE01_EDGE [3:2]		DEVACTIVE00_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE07_EDGE [15:14]		DEVACTIVE06_EDGE [13:12]		DEVACTIVE05_EDGE [11:10]		DEVACTIVE04_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		RW		RW	
HW Access	Reserved		R		R		R	
Name	Reserved [23:22]		DEVACTIVE10_EDGE [21:20]		DEVACTIVE09_EDGE [19:18]		DEVACTIVE08_EDGE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 20	DEVACTIVE10_EDGE	Reserved Default Value: 0x0
19 : 18	DEVACTIVE09_EDGE	Reserved Default Value: 0x0
17 : 16	DEVACTIVE08_EDGE	Reserved Default Value: 0x0
15 : 14	DEVACTIVE07_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE06_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE05_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE04_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE03_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE02_EDGE	DEVACTIVE 2 edge sensitivity. Default Value: 0x0
3 : 2	DEVACTIVE01_EDGE	DEVACTIVE 1 edge sensitivity. Default Value: 0x0

1.1.128 PPU_APPCPUSS_IESR (continued)

1 : 0	DEVACTIVE00_EDGE	DEVACTIVE 0 edge sensitivity. Default Value: 0x0

1.1.129 PPU_APPCPUSS_OPSR

Description: Operating Mode Active Edge Sensitivity Register

Address: 0x44100044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE19_EDGE [7:6]		DEVACTIVE18_EDGE [5:4]		DEVACTIVE17_EDGE [3:2]		DEVACTIVE16_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE23_EDGE [15:14]		DEVACTIVE22_EDGE [13:12]		DEVACTIVE21_EDGE [11:10]		DEVACTIVE20_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	DEVACTIVE23_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE22_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE21_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE20_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE19_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE18_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE17_EDGE	Reserved Default Value: 0x0
1 : 0	DEVACTIVE16_EDGE	Reserved Default Value: 0x0

1.1.130 PPU_APPCPUSS_FUNRR

Description: Functional Retention RAM Configuration Register

Address: 0x44100050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FUNC_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FUNC_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.131 PPU_APPCPUSS_FULRR

Description: Full Retention RAM Configuration Register

Address: 0x44100054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FULL_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FULL_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.132 PPU_APPCPUSS_MEMRR

Description: Memory Retention RAM Configuration Register

Address: 0x44100058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	MEM_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.133 PPU_APPCPUSS_EDTR0

Description: Power Mode Entry Delay Register 0

Address: 0x44100160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOGIC_RET_DEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	FULL_RET_DEL [31:24]							

Bits	Name	Description
31 : 24	FULL_RET_DEL	Reserved Default Value: 0x00
23 : 16	LOGIC_RET_DEL	Reserved Default Value: 0x00
15 : 8	MEM_RET_DEL	Reserved Default Value: 0x00
7 : 0	OFF_DEL	Reserved Default Value: 0x00

1.1.134 PPU_APPCPUSS_EDTR1

Description: Power Mode Entry Delay Register 1

Address: 0x44100164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FUNC_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	FUNC_RET_DEL	Reserved Default Value: 0x00
7 : 0	MEM_OFF_DEL	Reserved Default Value: 0x00

1.1.135 PPU_APPCPUSS_DCDR0

Description: Device Control Delay Configuration Register 0

Address: 0x44100170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CLKEN_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ISO_CLKEN_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RST_HWSTAT_DLY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	RST_HWSTAT_DLY	Reserved Default Value: 0x0
15 : 8	ISO_CLKEN_DLY	Reserved Default Value: 0x0
7 : 0	CLKEN_RST_DLY	Reserved Default Value: 0x0

1.1.136 PPU_APPCPUSS_DCDR1

Description: Device Control Delay Configuration Register 1

Address: 0x44100174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ISO_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CLKEN_ISO_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	CLKEN_ISO_DLY	Reserved Default Value: 0x0
7 : 0	ISO_RST_DLY	Reserved Default Value: 0x0

1.1.137 PPU_APPCPUSS_IDR0

Description: PPU Identification Register 0

Address: 0x44100FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	NUM_OPMODE [7:4]				DEVCHAN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	STA_-FUNC_RET_SPT	STA_-FULL_RET_SPT	STA_MEM_OFF_SPT	STA_LG-C_RET_SPT	STA_MEM_RET_EMU_SPT	STA_MEM_RET_SPT	STA_OFF_EMU_SPT	STA_OFF_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	Reserved	R	R	R
HW Access	RW	RW	RW	RW	Reserved	RW	RW	RW
Name	DY-N_MEM_RET_EMU_SPT	DY-N_MEM_RET_SPT	DY-N_OFF_EMU_SPT	DY-N_OFF_SPT	Reserved	STA_DB-G_RE-COV_SPT	STA_WRM_RST_SPT	STA_ON_SPT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [31:30]		DY-N_WRM_RST_SPT	DY-N_ON_SPT	DYN_-FUNC_RET_SPT	DYN_-FULL_RET_SPT	DY-N_MEM_OFF_SPT	DYN_LG-C_RET_SPT

Bits	Name	Description
29	DYN_WRM_RST_SPT	Dynamic WARM_RST support. Default Value: 0x0
28	DYN_ON_SPT	Dynamic ON support. Default Value: 0x1
27	DYN_FUNC_RET_SPT	Dynamic FUNC_RET support. Default Value: 0x0
26	DYN_FULL_RET_SPT	Dynamic FULL_RET support. Default Value: 0x1
25	DYN_MEM_OFF_SPT	Dynamic MEM_OFF support. Default Value: 0x0
24	DYN_LGC_RET_SPT	Dynamic LOGIC_RET support. Default Value: 0x0
23	DY-N_MEM_RET_EMU_SPT	Dynamic MEM_RET_EMU support Default Value: 0x0
22	DYN_MEM_RET_SPT	Dynamic MEM_RET support. Default Value: 0x0

1.1.137 PPU_APPCPUSS_IDR0 (continued)

21	DYN_OFF_EMU_SPT	Dynamic OFF_EMU support. Default Value: 0x0
20	DYN_OFF_SPT	Dynamic OFF support. Default Value: 0x1
18	STA_DBG_RECOV_SPT	DBG_RECOV support. Default Value: 0x0
17	STA_WRM_RST_SPT	WARM_RST support. Ignore this bit. Do not use WARM_RST. Default Value: 0x1
16	STA_ON_SPT	ON support. Default Value: 0x1
15	STA_FUNC_RET_SPT	FUNC_RET support. Default Value: 0x0
14	STA_FULL_RET_SPT	FULL_RET support. Default Value: 0x1
13	STA_MEM_OFF_SPT	MEM_OFF support. Default Value: 0x0
12	STA_LGC_RET_SPT	LOGIC_RET support. Default Value: 0x0
11	STA_MEM_RET_EMU_SPT	MEM_RET_EMU support. Default Value: 0x0
10	STA_MEM_RET_SPT	MEM_RET support. Default Value: 0x0
9	STA_OFF_EMU_SPT	OFF_EMU support. Default Value: 0x0
8	STA_OFF_SPT	OFF support. Default Value: 0x1
7 : 4	NUM_OPMODE	No. of operating modes supported is NUM_OPMODE + 1. Default Value: 0x0
3 : 0	DEVCHAN	No. of Device Interface Channels. 0: This is a P-Channel PPU. Refer to PPU_IDR1.OP_ACTIVE for the number of DEVPACTIVE inputs and their meaning. non-zero: The value is the number of Q-Channels. The device enumeration is: Device 0: SRSS PDCM, Device 1: CPUSS SEQ between SS level LPD500 EXP & PERI Q-Channel Default Value: 0x2

1.1.138 PPU_APPCPUSS_IDR1

Description: PPU Identification Register 1

Address: 0x44100FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	Reserved	R	R	R
HW Access	Reserved	RW	RW	RW	Reserved	RW	RW	RW
Name	Reserved	FUNC_RET_RAM_REG	FULL_RET_RAM_REG	MEM_RET_RAM_REG	Reserved	LOCK_SPT	SW_DEV_DEL_SPT	PWR_-MODE_EN-TRY_DEL_SPT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved	R	R	R
HW Access	Reserved			RW	Reserved	RW	RW	RW
Name	Reserved [15:13]			OFF_MEM_RET_TRANS	Reserved	OP_AC-TIVE	STA_POLI-CY_OP_IRQ_SPT	STA_POLI-CY_P-WR_IRQ_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	OFF_MEM_RET_TRANS	OFF to MEM_RET direct transition. Indicates if direct transitions from OFF to MEM_RET and from OFF_EMU to MEM_RET_EMU are supported. Default Value: 0x0
10	OP_ACTIVE	Operating mode use model for dynamic transitions. 0: Ladder use model. 1: Independent use model. When operating modes are not supported (PPU_IDR0.NUM_OPMODE==0), this field is reserved. Default Value: 0x0
9	STA_POLI-CY_OP_IRQ_SPT	Operating policy transition completion event status. Default Value: 0x0
8	STA_POLICY_P-WR_IRQ_SPT	Power policy transition completion event status. Default Value: 0x0
6	FUNC_RET_RAM_REG	Indicates if the PPU_FUNRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
5	FULL_RET_RAM_REG	Indicates if the PPU_FULRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
4	MEM_RET_RAM_REG	Indicates if the PPU_MEMRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0

1.1.138 PPU_APPCPUSS_IDR1 (continued)

2	LOCK_SPT	Lock and the lock interrupt event are supported. Default Value: 0x0
1	SW_DEV_DEL_SPT	Software device delay control configuration support. Default Value: 0x0
0	PWR_MODE_EN- TRY_DEL_SPT	Power mode entry delay support. Default Value: 0x0

1.1.139 PPU_APPCPUSS_IIDR

Description: Implementation Identification Register

Address: 0x44100FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IMPLEMENTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	REVISION [15:12]				IMPLEMENTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PRODUCT_ID [23:20]				VARIANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 20	PRODUCT_ID	PPU part identification. Default Value: 0x0B6
19 : 16	VARIANT	Major revision of the product. Default Value: 1
15 : 12	REVISION	Minor revision of the product. Default Value: 0
11 : 0	IMPLEMENTER	Implementer identification. [11:8] The JEP106 continuation code of the implementer. [7] Always 0. [6:0] The JEP106 identity code of the implementer. For an Arm implementation, bits [11:0] are 0x43B. Default Value: 0x43B

1.1.140 PPU_APPCPUSS_AIDR

Description: Architecture Identification Register

Address: 0x44100FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	ARCH_REV_MAJOR [7:4]				ARCH_REV_MINOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ARCH_REV_MAJOR	0x1 - PPU architecture major revision 1. Other Values - Reserved. Default Value: 0x1
3 : 0	ARCH_REV_MINOR	0x1 - PPU Architecture minor revision 1. Other Values - Reserved. Default Value: 0x1

1.1.141 PPU_APPCPUSS_PID4

Description: Implementation Defined Identification Register (PID4)

Address: 0x44100FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				IMPLEMENTER_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	IMPLEMENTER_11_8	The JEP106 continuation code of the implementer, which is 0x4 hardcoded value. Default Value: 0x4

1.1.142 PPU_APPCPUSS_PID0

Description: Implementation Defined Identification Register (PID0)

Address: 0x44100FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID_7_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PRODUCT_ID_7_0	PPU part identification bits [7:0]. Default Value: 0xB6

1.1.143 PPU_APPCPUSS_PID1

Description: Implementation Defined Identification Register (PID1)

Address: 0x44100FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	IMPLEMENTER_3_0 [7:4]				PRODUCT_ID_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	IMPLEMENTER_3_0	JEP106_ID bits [3:0] Default Value: 0xB
3 : 0	PRODUCT_ID_11_8	PPU part identification bits [11:8] Default Value: 0x0

1.1.144 PPU_APPCPUSS_PID2

Description: Implementation Defined Identification Register (PID2)

Address: 0x44100FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R	R		
HW Access	RW				RW	RW		
Name	REV_CONST [7:4]				CON-ST_HIGH	IMPLEMENTER_6_4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	REV_CONST	Revision 1(4 bits) Default Value: 0x1
3	CONST_HIGH	Constant HIGH Default Value: 0x1
2 : 0	IMPLEMENTER_6_4	JEP106_ID bits [6:4] Default Value: 0x3

1.1.145 PPU_APPCPUSS_PID3

Description: Implementation Defined Identification Register (PID3)

Address: 0x44100FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PID3_REVISION [7:4]				PID3_REV_CONST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	PID3_REVISION	Minor revision of the product. Default Value: 0x0
3 : 0	PID3_REV_CONST	Constant LOW (4 bits) Default Value: 0x0

1.1.146 PPU_APPCPUSS_ID0

Description: Implementation Defined Identification Register (ID0)

Address: 0x44100FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID0	ID0 hard coded value Default Value: 0x0D

1.1.147 PPU_APPCPUSS_ID1

Description: Implementation Defined Identification Register (ID1)

Address: 0x44100FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID1	ID1 hardcoded value Default Value: 0xF0

1.1.148 PPU_APPCPUSS_ID2

Description: Implementation Defined Identification Register (ID2)

Address: 0x44100FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID2	ID2 hardcoded value Default Value: 0x05

1.1.149 PPU_APPCPUSS_ID3

Description: Implementation Defined Identification Register (ID3)

Address: 0x44100FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID3	ID3 hardcoded value Default Value: 0xB1

1.1.150 PPU_CM55_0_PWPR

Description: Power Policy Register

Address: 0x44101000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			LOCK_EN	Reserved [11:9]			PWR_DYN_EN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							OP_DYN_EN

Bits	Name	Description
24	OP_DYN_EN	Operating mode dynamic transition enable. When this bit is set to 0b1 dynamic transitions are enabled for operating modes, allowing transitions to be initiated by changes on operating mode DEVACTIVE inputs. Default Value: 0x1
19 : 16	OP_POLICY	Operating mode policy. When static operating mode transitions are enabled,OP_DYN_EN is set to 0b0, then this is the target operating mode for the PPU. When dynamic operating mode transitions are enabled,OP_DYN_EN is set to 0b1, then this is the minimum operating mode for the PPU. Default Value: 0x1
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. When this bit is set to 1 dynamic transitions are enabled for power modes, allowing transitions to be initiated by changes on power mode DEVACTIVE inputs. Default Value: 0x1
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), FULL_RET(5), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x0

1.1.151 PPU_CM55_0_PMER

Description: Power Mode Emulation Register

Address: 0x44101004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							EMU_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	EMU_EN	Reserved Default Value: 0x0

1.1.152 PPU_CM55_0_PWSR

Description: Power Status Register

Address: 0x44101008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PWR_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved			R
HW Access	Reserved			RW	Reserved			RW
Name	Reserved [15:13]			LOCK_STATUS	Reserved [11:9]			PWR_DYN_STATUS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [23:20]				OP_STATUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [31:25]							OP_DYN_STATUS

Bits	Name	Description
24	OP_DYN_STATUS	Operating mode dynamic transition enable. When this bit is set to 0b1 dynamic transitions are enabled for operating modes, allowing transitions to be initiated by changes on operating mode DEVACTIVE inputs. Default Value: 0x0
19 : 16	OP_STATUS	Operating mode policy. When static operating mode transitions are enabled,OP_DYN_EN is set to 0b0, then this is the target operating mode for the PPU. When dynamic operating mode transitions are enabled,OP_DYN_EN is set to 0b1, then this is the minimum operating mode for the PPU. Default Value: 0x0
12	LOCK_STATUS	Reserved Default Value: 0x0
8	PWR_DYN_STATUS	Power mode dynamic transition status. When set to 1 power mode dynamic transitions are enabled. There might be a delay in dynamic transitions becoming active or inactive if the PPU is transitioning when PWR_DYN_EN is programmed. Default Value: 0x0
3 : 0	PWR_STATUS	Power mode status. These bits reflect the current power mode of the PPU. See PPU_PWPR.PWR_POLICY for power mode enumeration. Default Value: 0x0

1.1.153 PPU_CM55_0_DISR

Description: Device Interface Input Current Status Register

Address: 0x44101010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PWR_DEVACTIVE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					R		
HW Access	Reserved					RW		
Name	Reserved [15:11]					PWR_DEVACTIVE_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	OP_DEVACTIVE_STATUS [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVE_STATUS	Reserved Default Value: 0x0
10 : 0	PWR_DEVACTIVE_STATUS	Status of the power mode DEVACTIVE inputs. For Q-Channel: There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 0 is for the Q-Channel 0 DEVQACTIVE, and bit 1 for the QChannel 1 DEVQACTIVE. For a Q-Channel PPU bits [10:8] are always reserved as only 8 device interface QChannels are supported. For P-Channel: There is one bit for each bit of the power mode DEVPACTIVE inputs. For example, bit 10 is for DEVPACTIVE[10], and bit 9 is for DEVPACTIVE[9]. Bit 0 relates to DEVPACTIVE[0] and is always 0 Default Value: 0x0

1.1.154 PPU_CM55_0_MISR

Description: Miscellaneous Input Current Status Register

Address: 0x44101014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							PCSMPACCEPT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DEVACCEPT_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DEVDENY_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	DEVDENY_STATUS	Status of the device interface DEVDENY inputs. There is one bit for each device interface DEVQDENY. For example, bit 16 is for Q-Channel 0 DEVQDENY, and bit 17 for Q-Channel 1 DEVQDENY. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
15 : 8	DEVACCEPT_STATUS	Status of the device interface DEVACCEPT inputs. There is one bit for each device interface DEVQACCEPTn. For example, bit 8 is for Q-Channel 0 DEVQACCEPTn and bit 9 for Q-Channel 1 DEVQACCEPTn. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
0	PCSMPACCEPT_STATUS	The status of the PCSMPACCEPT input. Default Value: 0x0

1.1.155 PPU_CM55_0_STSR

Description: Stored Status Register

Address: 0x44101018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	STORED_DEVDENY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	STORED_DEVDENY	Status of the DEVDENY signals from the last device interface Q-Channel transition. For Q-Channel: There is one bit for each device interface DEVQDENY. For example, bit 0 is for Q-Channel 0 DEVQDENY, and bit 1 for Q-Channel 1 DEVQDENY. Refer to PPU_DISR.PWR_DEVACTIVE_STATUS for device enumeration. Default Value: 0x0

1.1.156 PPU_CM55_0_UNLK

Description: Unlock register

Address: 0x4410101C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							UNLOCK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	UNLOCK	Reserved Default Value: 0x0

1.1.157 PPU_CM55_0_PWCR

Description: Power Configuration Register

Address: 0x44101020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVREQEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PWR_DEVACTIVEEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_DEVACTIVEEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	OP_DEVACTIVEEN [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVEEN	Reserved Default Value: 0x00
18 : 8	PWR_DEVACTIVEEN	These bits enable the power mode DEVACTIVE inputs. When a bit is to 1 the related DEVACTIVE input is enabled, when set to 0 it is disabled. All available bits are reset to 1. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE, and bit 9 for the Q-Channel 1 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x03
7 : 0	DEVREQEN	When set to 1 enables the device interface handshake for transitions. All available bits are reset to 1. There is one bit for each device interface channel. For example, bit 0 is for Q-Channel 0, and bit 1 is for Q-Channel 1. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x03

1.1.158 PPU_CM55_0_PTCR

Description: Power Mode Transition Configuration Register

Address: 0x44101024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						DBG_RE-COV_POR ST_EN	WARM_RS T_DEVREQ EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	DBG_RE-COV_PORST_EN	Reserved Default Value: 0x0
0	WARM_RST_DEVREQEN	Transition behavior between ON and WARM_RST. This bit should not be modified when the PPU is in WARM_RST, or if the PPU is performing a transition, otherwise PPU behavior is UN-PREDICTABLE. 0: The PPU does not perform a device interface handshake when transitioning between ON and WARM_RST. 1: The PPU performs a device interface handshake when transitioning between ON and WARM_RST. This disables all Q-Channels for this transition. Default Value: 0x0

1.1.159 PPU_CM55_0_IMR

Description: Interrupt Mask Register

Address: 0x44101030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		LOCKED_IRQ_MASK	EMU_DENY_IRQ_MASK	EMU_ACCEPT_IRQ_MASK	STA_DENY_IRQ_MASK	STA_ACCEPT_IRQ_MASK	STA_POLICY_TRN_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	LOCKED_IRQ_MASK	Reserved Default Value: 0x0
4	EMU_DENY_IRQ_MASK	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ_MASK	Reserved Default Value: 0x0
2	STA_DENY_IRQ_MASK	Static transition denial event mask. Default Value: 0x0
1	STA_ACCEPT_IRQ_MASK	Static transition acceptance event mask. Default Value: 0x1
0	STA_POLICY_TRN_IRQ_MASK	Static full policy transition completion event mask. Default Value: 0x0

1.1.160 PPU_CM55_0_AIMR

Description: Additional Interrupt Mask Register

Address: 0x44101034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	RW	RW	RW
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ_MASK	STA_POLICY_PWR_IRQ_MASK	DYN_DENY_IRQ_MASK	DYN_ACCEPT_IRQ_MASK	UNSPT_POLICY_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ_MASK	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ_MASK	Reserved Default Value: 0x0
2	DYN_DENY_IRQ_MASK	Dynamic transition denial event mask. Default Value: 0x1
1	DYN_ACCEPT_IRQ_MASK	Dynamic transition acceptance event mask. Default Value: 0x1
0	UNSPT_POLICY_IRQ_MASK	Unsupported Policy event mask. Default Value: 0x0

1.1.161 PPU_CM55_0_ISR

Description: Interrupt Status Register

Address: 0x44101038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	Reserved	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	Reserved	R	R	R	R	R	R
Name	OTH-ER_IRQ	Reserved	LOCKED_IRQ	EMU_DE-NY_IRQ	EMU_AC-CEPT_IRQ	STA_DE-NY_IRQ	STA_AC-CEPT_IRQ	STA_POLI-CY_TRN_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	PWR_ACTIVE_EDGE_IRQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW1C		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_ACTIVE_EDGE_IRQ [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	OP_ACTIVE_EDGE_IRQ [31:24]							

Bits	Name	Description
31 : 24	OP_ACTIVE_EDGE_IRQ	Indicates which operating mode DEVPACTIVE inputs caused the input edge event. When operating modes are not supported this field is reserved. Default Value: 0x0
18 : 8	PWR_ACTIVE_EDGE_IRQ	Indicates which power mode DEVACTIVE inputs caused the input edge event. Bits for unused channels are the MSBs and are reserved. There is one bit for each device Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x00
7	OTHER_IRQ	Indicates there is an interrupt event pending in the Additional Interrupt Status Register (PPU_AISR). Default Value: 0x0
5	LOCKED_IRQ	Reserved Default Value: 0x0
4	EMU_DENY_IRQ	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ	Reserved Default Value: 0x0
2	STA_DENY_IRQ	Static transition denial event status. Default Value: 0x0
1	STA_ACCEPT_IRQ	Static transition acceptance event status. Default Value: 0x0

1.1.161 PPU_CM55_0_ISR (continued)

0	STA_POLICY_TRN_IRQ	Static full policy transition completion event status. Default Value: 0x0

1.1.162 PPU_CM55_0_AISR

Description: Additional Interrupt Status Register

Address: 0x4410103C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ	STA_POLICY_PWR_IRQ	DYN_DENY_IRQ	DYN_ACCEPT_IRQ	UNSPT_POLICY_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ	Reserved Default Value: 0x0
2	DYN_DENY_IRQ	Dynamic transition denial event status. Default Value: 0x0
1	DYN_ACCEPT_IRQ	Dynamic transition acceptance event status. Default Value: 0x0
0	UNSPT_POLICY_IRQ	Unsupported Policy event status. Default Value: 0x0

1.1.163 PPU_CM55_0_IESR

Description: Input Edge Sensitivity Register

Address: 0x44101040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE03_EDGE [7:6]		DEVACTIVE02_EDGE [5:4]		DEVACTIVE01_EDGE [3:2]		DEVACTIVE00_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE07_EDGE [15:14]		DEVACTIVE06_EDGE [13:12]		DEVACTIVE05_EDGE [11:10]		DEVACTIVE04_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		RW		RW	
HW Access	Reserved		R		R		R	
Name	Reserved [23:22]		DEVACTIVE10_EDGE [21:20]		DEVACTIVE09_EDGE [19:18]		DEVACTIVE08_EDGE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 20	DEVACTIVE10_EDGE	Reserved Default Value: 0x0
19 : 18	DEVACTIVE09_EDGE	Reserved Default Value: 0x0
17 : 16	DEVACTIVE08_EDGE	Reserved Default Value: 0x0
15 : 14	DEVACTIVE07_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE06_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE05_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE04_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE03_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE02_EDGE	DEVACTIVE 2 edge sensitivity. Default Value: 0x0
3 : 2	DEVACTIVE01_EDGE	DEVACTIVE 1 edge sensitivity. Default Value: 0x0

1.1.163 PPU_CM55_0_IESR (continued)

1 : 0	DEVACTIVE00_EDGE	DEVACTIVE 0 edge sensitivity. Default Value: 0x0

1.1.164 PPU_CM55_0_OPSR

Description: Operating Mode Active Edge Sensitivity Register

Address: 0x44101044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE19_EDGE [7:6]		DEVACTIVE18_EDGE [5:4]		DEVACTIVE17_EDGE [3:2]		DEVACTIVE16_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE23_EDGE [15:14]		DEVACTIVE22_EDGE [13:12]		DEVACTIVE21_EDGE [11:10]		DEVACTIVE20_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	DEVACTIVE23_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE22_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE21_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE20_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE19_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE18_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE17_EDGE	Reserved Default Value: 0x0
1 : 0	DEVACTIVE16_EDGE	Reserved Default Value: 0x0

1.1.165 PPU_CM55_0_FUNRR

Description: Functional Retention RAM Configuration Register

Address: 0x44101050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FUNC_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FUNC_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.166 PPU_CM55_0_FULRR

Description: Full Retention RAM Configuration Register

Address: 0x44101054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FULL_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FULL_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.167 PPU_CM55_0_MEMRR

Description: Memory Retention RAM Configuration Register

Address: 0x44101058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	MEM_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.168 PPU_CM55_0_EDTR0

Description: Power Mode Entry Delay Register 0

Address: 0x44101160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOGIC_RET_DEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	FULL_RET_DEL [31:24]							

Bits	Name	Description
31 : 24	FULL_RET_DEL	Reserved Default Value: 0x00
23 : 16	LOGIC_RET_DEL	Reserved Default Value: 0x00
15 : 8	MEM_RET_DEL	Reserved Default Value: 0x00
7 : 0	OFF_DEL	Reserved Default Value: 0x00

1.1.169 PPU_CM55_0_EDTR1

Description: Power Mode Entry Delay Register 1

Address: 0x44101164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FUNC_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	FUNC_RET_DEL	Reserved Default Value: 0x00
7 : 0	MEM_OFF_DEL	Reserved Default Value: 0x00

1.1.170 PPU_CM55_0_DCDR0

Description: Device Control Delay Configuration Register 0

Address: 0x44101170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CLKEN_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ISO_CLKEN_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RST_HWSTAT_DLY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	RST_HWSTAT_DLY	Reserved Default Value: 0x0
15 : 8	ISO_CLKEN_DLY	Reserved Default Value: 0x0
7 : 0	CLKEN_RST_DLY	Reserved Default Value: 0x0

1.1.171 PPU_CM55_0_DCDR1

Description: Device Control Delay Configuration Register 1

Address: 0x44101174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ISO_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CLKEN_ISO_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	CLKEN_ISO_DLY	Reserved Default Value: 0x0
7 : 0	ISO_RST_DLY	Reserved Default Value: 0x0

1.1.172 PPU_CM55_0_IDR0

Description: PPU Identification Register 0

Address: 0x44101FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	NUM_OPMODE [7:4]				DEVCHAN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	STA_-FUNC_RET_SPT	STA_-FULL_RET_SPT	STA_MEM_OFF_SPT	STA_LG-C_RET_SPT	STA_MEM_RET_EMU_SPT	STA_MEM_RET_SPT	STA_OFF_EMU_SPT	STA_OFF_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	Reserved	R	R	R
HW Access	RW	RW	RW	RW	Reserved	RW	RW	RW
Name	DY-N_MEM_RET_EMU_SPT	DY-N_MEM_RET_SPT	DY-N_OFF_EMU_SPT	DY-N_OFF_SPT	Reserved	STA_DB-G_RE-COV_SPT	STA_WRM_RST_SPT	STA_ON_SPT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [31:30]		DY-N_WRM_RST_SPT	DY-N_ON_SPT	DYN_-FUNC_RET_SPT	DYN_-FULL_RET_SPT	DY-N_MEM_OFF_SPT	DYN_LG-C_RET_SPT

Bits	Name	Description
29	DYN_WRM_RST_SPT	Dynamic WARM_RST support. Default Value: 0x0
28	DYN_ON_SPT	Dynamic ON support. Default Value: 0x1
27	DYN_FUNC_RET_SPT	Dynamic FUNC_RET support. Default Value: 0x0
26	DYN_FULL_RET_SPT	Dynamic FULL_RET support. Default Value: 0x1
25	DYN_MEM_OFF_SPT	Dynamic MEM_OFF support. Default Value: 0x0
24	DYN_LGC_RET_SPT	Dynamic LOGIC_RET support. Default Value: 0x0
23	DY-N_MEM_RET_EMU_SPT	Dynamic MEM_RET_EMU support Default Value: 0x0
22	DYN_MEM_RET_SPT	Dynamic MEM_RET support. Default Value: 0x0

1.1.172 PPU_CM55_0_IDR0 (continued)

21	DYN_OFF_EMU_SPT	Dynamic OFF_EMU support. Default Value: 0x0
20	DYN_OFF_SPT	Dynamic OFF support. Default Value: 0x1
18	STA_DBG_RECOV_SPT	DBG_RECOV support. Default Value: 0x0
17	STA_WRM_RST_SPT	WARM_RST support. Ignore this bit. Do not use WARM_RST. Default Value: 0x1
16	STA_ON_SPT	ON support. Default Value: 0x1
15	STA_FUNC_RET_SPT	FUNC_RET support. Default Value: 0x0
14	STA_FULL_RET_SPT	FULL_RET support. Default Value: 0x1
13	STA_MEM_OFF_SPT	MEM_OFF support. Default Value: 0x0
12	STA_LGC_RET_SPT	LOGIC_RET support. Default Value: 0x0
11	STA_MEM_RET_EMU_SPT	MEM_RET_EMU support. Default Value: 0x0
10	STA_MEM_RET_SPT	MEM_RET support. Default Value: 0x0
9	STA_OFF_EMU_SPT	OFF_EMU support. Default Value: 0x0
8	STA_OFF_SPT	OFF support. Default Value: 0x1
7 : 4	NUM_OPMODE	No. of operating modes supported is NUM_OPMODE + 1. Default Value: 0x0
3 : 0	DEVCHAN	No. of Device Interface Channels. 0: This is a P-Channel PPU. Refer to PPU_IDR1.OP_ACTIVE for the number of DEVPACTIVE inputs and their meaning. non-zero: The value is the number of Q-Channels. The device enumeration is: Device 0: SRSS PDCM, Device 1: CPUSS SEQ between SS level LPD500 EXP & PERI Q-Channel Default Value: 0x2

1.1.173 PPU_CM55_0_IDR1

Description: PPU Identification Register 1

Address: 0x44101FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	Reserved	R	R	R
HW Access	Reserved	RW	RW	RW	Reserved	RW	RW	RW
Name	Reserved	FUNC_RET_RAM_REG	FULL_RET_RAM_REG	MEM_RET_RAM_REG	Reserved	LOCK_SPT	SW_DEV_DEL_SPT	PWR_-MODE_EN-TRY_DEL_SPT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved	R	R	R
HW Access	Reserved			RW	Reserved	RW	RW	RW
Name	Reserved [15:13]			OFF_MEM_RET_TRANS	Reserved	OP_AC-TIVE	STA_POLI-CY_OP_IRQ_SPT	STA_POLI-CY_P-WR_IRQ_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	OFF_MEM_RET_TRANS	OFF to MEM_RET direct transition. Indicates if direct transitions from OFF to MEM_RET and from OFF_EMU to MEM_RET_EMU are supported. Default Value: 0x0
10	OP_ACTIVE	Operating mode use model for dynamic transitions. 0: Ladder use model. 1: Independent use model. When operating modes are not supported (PPU_IDR0.NUM_OPMODE==0), this field is reserved. Default Value: 0x0
9	STA_POLI-CY_OP_IRQ_SPT	Operating policy transition completion event status. Default Value: 0x0
8	STA_POLICY_P-WR_IRQ_SPT	Power policy transition completion event status. Default Value: 0x0
6	FUNC_RET_RAM_REG	Indicates if the PPU_FUNRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
5	FULL_RET_RAM_REG	Indicates if the PPU_FULRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
4	MEM_RET_RAM_REG	Indicates if the PPU_MEMRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0

1.1.173 PPU_CM55_0_IDR1 (continued)

2	LOCK_SPT	Lock and the lock interrupt event are supported. Default Value: 0x0
1	SW_DEV_DEL_SPT	Software device delay control configuration support. Default Value: 0x0
0	PWR_MODE_EN- TRY_DEL_SPT	Power mode entry delay support. Default Value: 0x0

1.1.174 PPU_CM55_0_IIDR

Description: Implementation Identification Register

Address: 0x44101FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IMPLEMENTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	REVISION [15:12]				IMPLEMENTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PRODUCT_ID [23:20]				VARIANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 20	PRODUCT_ID	PPU part identification. Default Value: 0x0B6
19 : 16	VARIANT	Major revision of the product. Default Value: 1
15 : 12	REVISION	Minor revision of the product. Default Value: 0
11 : 0	IMPLEMENTER	Implementer identification. [11:8] The JEP106 continuation code of the implementer. [7] Always 0. [6:0] The JEP106 identity code of the implementer. For an Arm implementation, bits [11:0] are 0x43B. Default Value: 0x43B

1.1.175 PPU_CM55_0_AIDR

Description: Architecture Identification Register

Address: 0x44101FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	ARCH_REV_MAJOR [7:4]				ARCH_REV_MINOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ARCH_REV_MAJOR	0x1 - PPU architecture major revision 1. Other Values - Reserved. Default Value: 0x1
3 : 0	ARCH_REV_MINOR	0x1 - PPU Architecture minor revision 1. Other Values - Reserved. Default Value: 0x1

1.1.176 PPU_CM55_0_PID4

Description: Implementation Defined Identification Register (PID4)

Address: 0x44101FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				IMPLEMENTER_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	IMPLEMENTER_11_8	The JEP106 continuation code of the implementer, which is 0x4 hardcoded value. Default Value: 0x4

1.1.177 PPU_CM55_0_PID0

Description: Implementation Defined Identification Register (PID0)

Address: 0x44101FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID_7_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PRODUCT_ID_7_0	PPU part identification bits [7:0]. Default Value: 0xB6

1.1.178 PPU_CM55_0_PID1

Description: Implementation Defined Identification Register (PID1)

Address: 0x44101FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	IMPLEMENTER_3_0 [7:4]				PRODUCT_ID_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	IMPLEMENTER_3_0	JEP106_ID bits [3:0] Default Value: 0xB
3 : 0	PRODUCT_ID_11_8	PPU part identification bits [11:8] Default Value: 0x0

1.1.179 PPU_CM55_0_PID2

Description: Implementation Defined Identification Register (PID2)

Address: 0x44101FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R	R		
HW Access	RW				RW	RW		
Name	REV_CONST [7:4]				CON-ST_HIGH	IMPLEMENTER_6_4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	REV_CONST	Revision 1(4 bits) Default Value: 0x1
3	CONST_HIGH	Constant HIGH Default Value: 0x1
2 : 0	IMPLEMENTER_6_4	JEP106_ID bits [6:4] Default Value: 0x3

1.1.180 PPU_CM55_0_PID3

Description: Implementation Defined Identification Register (PID3)

Address: 0x44101FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PID3_REVISION [7:4]				PID3_REV_CONST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	PID3_REVISION	Minor revision of the product. Default Value: 0x0
3 : 0	PID3_REV_CONST	Constant LOW (4 bits) Default Value: 0x0

1.1.181 PPU_CM55_0_ID0

Description: Implementation Defined Identification Register (ID0)

Address: 0x44101FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID0	ID0 hard coded value Default Value: 0x0D

1.1.182 PPU_CM55_0_ID1

Description: Implementation Defined Identification Register (ID1)

Address: 0x44101FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID1	ID1 hardcoded value Default Value: 0xF0

1.1.183 PPU_CM55_0_ID2

Description: Implementation Defined Identification Register (ID2)

Address: 0x44101FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID2	ID2 hardcoded value Default Value: 0x05

1.1.184 PPU_CM55_0_ID3

Description: Implementation Defined Identification Register (ID3)

Address: 0x44101FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID3	ID3 hardcoded value Default Value: 0xB1

1.1.185 PD_CTL

Description: Power Domain Control

Address: 0x44103000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							BLEED_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	BLEED_EN	Activates bleed feature for the controlled power domain Default Value: 0

1.1.186 PD_PWR_UP_DELAY

Description: Active switch weak enable to active switch strong enable delay

Address: 0x44103004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COUNT_LOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_COUNT_LOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	MEM_COUNT_LOAD	Load value for counter running on clk_pwr (10MHz) providing the timing from weak MEM switch enable to strong MEM switch enable. Default is 5 for ~500ns Default Value: 0
7 : 0	COUNT_LOAD	Load value for counter running on clk_pwr (10MHz) providing the timing from weak ACTIVE switch enable to strong ACTIVE switch enable. Default is 5 for ~500ns Default Value: 5

1.1.187 MXCM55_CM55_CTL

Description: Control

Address: 0x44160000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			
HW Access	Reserved			R	Reserved			
Name	Reserved [7:5]			CPU_WAIT	Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	LOCKTCM	LOCKDCA-IC	LOCKPAHB	LOCKSAU	LOCKNSM-PU	LOCKSM-PU	LOCKSVTAIRCR	LOCKNS-VTOR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [23:18]						LOCKDT-GU	LOCKITGU

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved		RW	RW	RW	RW	RW
HW Access	R	Reserved		R	R	R	R	R
Name	IDC_MASK	Reserved [30:29]		IXC_MASK	UFC_MASK	OFC_MASK	DZC_MASK	IOC_MASK

Bits	Name	Description
31	IDC_MASK	CPU FPU exception mask for the CPU's FPCSR.IDC "input denormalized" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: if the CPU FPCSR.FZ field is set to '1', denormalized inputs are "flushed to zero". Dependent on the FPU algorithm, this may or may not occur frequently. To prevent frequent CPU FPU interrupts as a result of denormalized inputs, this field may be set to '0'. Default Value: 0
28	IXC_MASK	CPU FPU exception mask for the CPU's FPCSR.IXC "inexact" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the "inexact" condition is set as a result of rounding. Rounding may occur frequently and is typically not an error condition. To prevent frequent CPU FPU interrupts as a result of rounding, this field is typically set to '0'. Default Value: 0
27	UFC_MASK	CPU FPU exception mask for the CPU's FPCSR.UFC "underflow" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0
26	OFC_MASK	CPU FPU exception mask for the CPU's FPCSR.OFC "overflow" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0

1.1.187 MXCM55_CM55_CTL (continued)

25	DZC_MASK	CPU FPU exception mask for the CPU's FPCSR.DZC "divide by zero" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0
24	IOC_MASK	CPU floating point unit (FPU) exception mask for the CPU's FPCSR.IOC "invalid operation" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the ARM architecture does NOT support FPU exceptions; i.e. there is no precise FPU exception handler. Instead, FPU conditions are captured in the CPU's FPCSR register and the conditions are provided as CPU interface signals. The interface signals are "masked" with the fields provided by this register (CM55_CTL). The "masked" signals are reduced/OR-ed into a single CPU floating point interrupt signal. The associated CPU interrupt handler allows for imprecise handling of FPU exception conditions. Note: the CPU's FPCSR exception conditions are "sticky". Typically, the CPU FPU interrupt handler will clear the exception condition(s) to '0'. Note: by default, the FPU exception masks are '0'. Therefore, FPU exception conditions will NOT activate the CPU's floating point interrupt. Default Value: 0
17	LOCKDTGU	Asserting this bit prevents changes to the security gating configuration of the DTCM. '1': Disables writes to the DTGUCTRL, DTGU_LUTn from software or from a debug agent connected to the processor. '0': Unlocks these registers. Default Value: 0
16	LOCKITGU	Asserting this bit prevents changes to the security gating configuration of the ITCM. '1': Disables writes to the ITGUCTRL, ITGU_LUTn from software or from a debug agent connected to the processor. '0': Unlocks these registers. Default Value: 0
15	LOCKTCM	Asserting this bit prevents changes to the TCM configuration. All writes to the registers are ignored. '1': Disables writes to the ITCMCR, DTCMCR from software or from a debug agent connected to the processor. '0': Unlocks these registers. Default Value: 0
14	LOCKDCAIC	Disable access to the instruction cache direct cache access registers DCAICLR and DCAICRR. Setting this bit to '1' prevents direct access to the instruction cache Tag or Data RAM content. This is required when using eXecutable Only Memory (XOM) on the AXI master interface. When LOCKDCAIC is asserted: DCAICLR is RAZ/WI. DCAICRR is RAZ. Default Value: 0
13	LOCKPAHB	Setting this bit to '1' disable writes to the PAHBCR register from software or from a debug agent connected to the processor. Asserting this signal prevents changes to P-AHB port enable status in PAHBCR.EN. Default Value: 0
12	LOCKSAU	Asserting this bit prevents changes to Secure SAU memory regions already programmed. All writes to the registers are ignored. '1': Disables writes to the SAU_CTRL, SAU_RNR, SAU_RBAR and SAU_RLAR registers from software or from a debug agent connected to the processor. '0': Unlocks these registers. This signal has no affect if the Cortex-M55 processor has not been configured with support for the Armv8-M Security Extension, or if no SAU regions have been configured. Default Value: 0

1.1.187 MXCM55_CM55_CTL (continued)

11	LOCKNSMPU	Asserting this bit prevents changes to Nonsecure MPU memory regions already programmed. All writes to the registers are ignored. '1': Disables writes to the MPU_CTRL_NS, MPU_RNR_NS, MPU_RBAR_NS, MPU_RLAR_NS, MPU_RBAR_A_NSn and MPU_RLAR_A_NSn from software or from a debug agent connected to the processor. '0': Unlocks these registers. This signal has no affect if the Cortex-M55 processor has been configured without any Nonsecure MPU regions. Default Value: 0
10	LOCKSMPU	Asserting this bit prevents changes to programmed Secure MPU memory regions and all writes to the registers are ignored. '1': Disables writes to the MPU_CTRL, MPU_RNR, MPU_RBAR, MPU_RLAR, MPU_RBAR_An and MPU_RLAR_An from software or from a debug agent connected to the processor in Secure state. '0': Unlocks these registers. This bit has no affect if the Cortex-M55 processor has not been configured with support for the Armv8-M Security Extension, or if no Secure MPU regions have been configured. Default Value: 0
9	LOCKSVTAIRCR	Asserting this bit prevents changes to: - The Secure vector table base address. - Handling of Secure interrupt priority. - BusFault, HardFault, and NMI security target settings in the processor. '1': Disables writes to the VTOR_S,AIRCR.PRIS, and AIRCR.BFHFNMINS registers. '0': Unlocks these registers. Default Value: 0
8	LOCKNSVTOR	Asserting this bit prevents changes to the Non-secure vector table base address. '1': Disables writes to the VTOR_NS register. '0': Unlocks this register. Default Value: 0
4	CPU_WAIT	When this signal is '1' out of reset, it forces the CPU into a quiescent state that delays its boot-up sequence and instruction execution until this signal is driven '0'. Default Value: 1

1.1.188 MXCM55_CM55_CMD

Description: Command

Address: 0x44160004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							RW1C
Name	Reserved [7:1]							RESET

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 0xFA05
0	RESET	CM55 Processor reset: '1': RESET. Processor reset is activated. After SW set this field to '1', HW automatically clears this field to '0'. This effectively results in a CM55 reset, followed by a CM55 warm boot. This bit effectively enables WARM_RST state of the CM55 PPU and works only when dynamic transitions are enabled in CM55 PPU. '0': No reset of CM55. Note: The intent is that this bit is modified only through an external probe or by the other CPU while this CM55 is in Sleep or DeepSleep. If this field is set to '1' by this CM55 itself, it should be done under controlled conditions (such that undesirable side effects can be prevented). Note: The CM55 CPU has a AIRCR.SYSRESETREQ register field that allows the CM55 to reset the complete device (RESET field in this register only resets the CM55), resulting in a warm boot. This CPU register field has similar "built-in protection" as this register to prevent accidental system writes (the upper 16-bits of the register need to be written with a 0x05fa key value; see CPU user manual for more details). Default Value: 0

1.1.189 MXCM55_CM55_STATUS

Description: Status

Address: 0x44160008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						SLEEP-DEEP	SLEEPING

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SLEEPDEEP	Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. Default Value: 0
0	SLEEPING	Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. Default Value: 0

1.1.190 MXCM55_CM55_TCM_CTL

Description: TCM control

Address: 0x4416000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							ITC-M_READ_WS

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							DTC-M_READ_WS

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	DTCM_READ_WS	DTCM read wait states (writes have no wait states). '0': 0 wait states. '1': 1 wait state. Default Value: 0
0	ITCM_READ_WS	ITCM read wait states (writes have no wait states). '0': 0 wait states. '1': 1 wait state. Default Value: 0

1.1.191 MXCM55_CM55_NMI_CTL0

Description: CM55 NMI control

Address: 0x44160080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	SYSTEM_INT_IDX	System interrupt select for CPU NMI. The reset value ("1023") ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. Default Value: 1023

1.1.192 MXCM55_CM55_EVENT_CTL

Description: CM55 EVENT control

Address: 0x441600C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			MASK [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	MASK	One mask bit for each CPU (other than itself). 0: Mask is not set. 1: RX event from the corresponding CPU is masked. Bit 0: CM33_0 CPU event Bit 1: CM33_1 CPU event Bit 2: Other CM55 CPU event Bit 3: Reserved Bit 4: Reserved Default Value: 0

1.1.193 MXCM55_CM55_S_VECTOR_TABLE_BASE

Description: CM55 secure vector table base

Address: 0x44161000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ADDR25	Reserved [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR25 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR25 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR25 [31:24]							

Bits	Name	Description
31 : 7	ADDR25	Address of CM55 secure vector table to be used at reset. Default value: ADDR25: 0x0200000 (points to Secure TCM start address i.e. 0x1000_0000). Default Value: 2097152

1.1.194 MXCM55_CM55_NS_VECTOR_TABLE_BASE

Description: CM55 non-secure vector table base

Address: 0x44161004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ADDR25	Reserved [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR25 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR25 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR25 [31:24]							

Bits	Name	Description
31 : 7	ADDR25	Address of CM55 non-secure vector table to be used at reset. Default value: ADDR25: 0x0000000 (points to Non-Secure TCM start address i.e. 0x0000_0000). Default Value: 0

1.1.195 MXCM55_WOUNDING

Description: Wounding

Address: 0x441620C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							R
Name	Reserved [7:1]							FPU_WOUND

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	FPU_WOUND	When set to '1', disables support for CM55 FPU. Default Value: 0

1.1.196 APPCPUSS_IDENTITY

Description: Identity

Address: 0x441C0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved		R	R
HW Access	W				Reserved		W	W
Name	PC [7:4]				Reserved [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [15:14]		MS [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
13 : 8	MS	This field specifies the bus master identifier of the transfer that reads the register. Default Value: Undefined
7 : 4	PC	This field specifies the protection context of the transfer that reads the register. Default Value: Undefined
1	NS	This field specifies the security setting ('0': secure mode; '1': non-secure mode) of the transfer that reads the register. Default Value: Undefined
0	P	This field specifies the privileged setting ('0': user mode; '1': privileged mode) of the transfer that reads the register. Default Value: Undefined

1.1.197 APPCPUSS_PRODUCT_ID

Description: Product identifier and version (same as CoreSight RomTables)

Address: 0x441C0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FAMILY_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [15:12]				FAMILY_ID [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	W				W			
Name	MINOR_REV [23:20]				MAJOR_REV [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 20	MINOR_REV	Minor Revision, starts with 1, increments with metal layer only tape-out (implemented with metal ECO-able tie-off) Default Value: Undefined
19 : 16	MAJOR_REV	Major Revision, starts with 1, increments with all layer tape-out (implemented with metal ECO-able tie-off) Default Value: Undefined
11 : 0	FAMILY_ID	Family ID. Common ID for a product family. Default Value: 277

1.1.198 APPCPUSS_DP_STATUS

Description: Debug port status

Address: 0x441C0020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [7:4]				SWJ_SWD_SEL	SWJ_-JTAG_SEL	SWJ_DE-BUG_EN	SWJ_CON-NECTED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	SWJ_SWD_SEL	Specifies if the SWD interface is selected. '0': SWD not selected. '1': SWD selected. Default Value: 0
2	SWJ_JTAG_SEL	Specifies if the JTAG interface is selected. '0': JTAG not selected. '1': JTAG selected. Default Value: 0
1	SWJ_DEBUG_EN	Specifies if SWJ debug is enabled, i.e. CDBGPWRUPACK is '1' and thus debug clocks are on: '0': Disabled. '1': Enabled. Default Value: 0
0	SWJ_CONNECTED	Specifies if the SWJ debug port is connected; i.e. debug host interface is active: '0': Not connected/not active. '1': Connected/active. Default Value: 0

1.1.199 APPCPUSS_BUFF_CTL

Description: Buffer control

Address: 0x441C0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							WRITE_BUFF

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	WRITE_BUFF	Specifies if write transfer can be buffered in the bus infrastructure bridges: '0': Write transfers are not buffered, independent of the transfer's bufferable attribute. '1': Write transfers can be buffered, if the transfer's bufferable attribute indicates that the transfer is a bufferable/posted write. This bit controls buffering only for subsystems that interfaced using the AHB2AHB bridge, not for components utilised from ARM. Default Value: 1

1.1.200 APPCPUSS_INFRA_CTL

Description: Infrastructure Control

Address: 0x441C0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							CLOCK_-FORCE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CLOCK_FORCE	Force Infrastructure clock gating to be always ON. 0: Disabled 1: Enabled Default Value: 0

1.1.201 APPCPUSS_SYSTICK_NS_CTL

Description: Non Secure SysTick timer control

Address: 0x441C0120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved				RW	
HW Access	R	R	Reserved				R	
Name	NOREF	SKEW	Reserved [29:26]				CLOCK_SOURCE [25:24]	

Bits	Name	Description
31	NOREF	Specifies if an external clock source is provided: '0': An external clock source is provided. '1': An external clock source is NOT provided and only the CPU internal clock can be used as SysTick timer clock source. Default Value: 0
30	SKEW	Specifies the precision of the clock source and if the TENMS field represents exactly 10 ms (clock source frequency is a multiple of 100 Hz). This affects the suitability of the SysTick timer as a SW real-time clock: '0': Precise. '1': Imprecise. Default Value: 1
25 : 24	CLOCK_SOURCE	Specifies an external clock source: "0": The low frequency clock "clk_lf" is selected. The precision of this clock depends on whether the low frequency clock source is a SRSS internal RC oscillator (imprecise) or a device external crystal oscillator (precise). "1": The internal main oscillator (IMO) clock "clk_imo" is selected. The MXS40 platform uses a fixed frequency IMO clock. o "2": The external crystal oscillator (ECO) clock "clk_eco" is selected. "3": The SRSS "clk_timer" is selected ("clk_timer" is a divided/gated version of "clk_hf" or "clk_i-mo"). Note: If NOREF is '1', the CLOCK_SOURCE value is NOT used. Note: It is SW's responsibility to provide the correct NOREF, SKEW and TENMS field values for the selected clock source. Default Value: 0

1.1.201 APPCPUSS_SYSTICK_NS_CTL (continued)

23 : 0	TENMS	Specifies the number of clock source cycles (minus 1) that make up 10 ms. E.g., for a 32,768 Hz reference clock, TENMS is 328 - 1 = 327. Default Value: 327

1.1.202 APPCPUSS_INTR_MSC

Description: Master security controller Interrupt

Address: 0x441C0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	Reserved	RW1C	Reserved	
HW Access	A	A	A	A	Reserved	A	Reserved	
Name	AXI_MS3_MSC	AXI_MS2_MSC	AXI_MS1_MSC	AXI_MS0_MSC	Reserved	AXID-MAC0_MSC	Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW1C	RW1C	RW1C
HW Access	Reserved					A	A	A
Name	Reserved [15:11]					EXP_MS2_MSC	EXP_MS1_MSC	EXP_MS0_MSC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10	EXP_MS2_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on external AHB master 2 interface. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0
9	EXP_MS1_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on external AHB master 1 interface. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0
8	EXP_MS0_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on external AHB master 0 interface. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0
7	AXI_MS3_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on external AXI master 3 interface. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0

1.1.202 APPCPUSS_INTR_MSC (continued)

6	AXI_MS2_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on external AXI master 2 interface. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0
5	AXI_MS1_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on external AXI master 1 interface. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0
4	AXI_MS0_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on external AXI master 0 interface. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0
2	AXIDMAC0_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on AXI DMA controller 0 interface. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0

1.1.203 APPCPUSS_INTR_MASK_MSC

Description: Master security controller Interrupt mask

Address: 0x441C0208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	Reserved	RW	Reserved	
HW Access	R	R	R	R	Reserved	R	Reserved	
Name	AXI_MS3_MSC	AXI_MS2_MSC	AXI_MS1_MSC	AXI_MS0_MSC	Reserved	AXIDMAC0_MSC	Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [15:11]					EXP_MS2_MSC	EXP_MS1_MSC	EXP_MS0_MSC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10	EXP_MS2_MSC	Mask bit for the corresponding field in the APPCPUSS_INTR_MSC register. Default Value: 0
9	EXP_MS1_MSC	Mask bit for the corresponding field in the APPCPUSS_INTR_MSC register. Default Value: 0
8	EXP_MS0_MSC	Mask bit for the corresponding field in the APPCPUSS_INTR_MSC register. Default Value: 0
7	AXI_MS3_MSC	Mask bit for the corresponding field in the APPCPUSS_INTR_MSC register. Default Value: 0
6	AXI_MS2_MSC	Mask bit for the corresponding field in the APPCPUSS_INTR_MSC register. Default Value: 0
5	AXI_MS1_MSC	Mask bit for the corresponding field in the APPCPUSS_INTR_MSC register. Default Value: 0
4	AXI_MS0_MSC	Mask bit for the corresponding field in the APPCPUSS_INTR_MSC register. Default Value: 0
2	AXIDMAC0_MSC	Mask bit for the corresponding field in the APPCPUSS_INTR_MSC register. Default Value: 0

1.1.204 APPCPUSS_INTR_MASKED_MSC

Description: Master security controller Interrupt masked

Address: 0x441C020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	Reserved	R	Reserved	
HW Access	W	W	W	W	Reserved	W	Reserved	
Name	AXI_MS3_MSC	AXI_MS2_MSC	AXI_MS1_MSC	AXI_MS0_MSC	Reserved	AXID-MAC0_MSC	Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					R	R	R
HW Access	Reserved					W	W	W
Name	Reserved [15:11]					EXP_MS2_MSC	EXP_MS1_MSC	EXP_MS0_MSC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10	EXP_MS2_MSC	Logical AND of corresponding APPCPUSS_INTR_MSC and APPCPUSS_INTR_MASK_MSC bit fields. Default Value: 0
9	EXP_MS1_MSC	Logical AND of corresponding APPCPUSS_INTR_MSC and APPCPUSS_INTR_MASK_MSC bit fields. Default Value: 0
8	EXP_MS0_MSC	Logical AND of corresponding APPCPUSS_INTR_MSC and APPCPUSS_INTR_MASK_MSC bit fields. Default Value: 0
7	AXI_MS3_MSC	Logical AND of corresponding APPCPUSS_INTR_MSC and APPCPUSS_INTR_MASK_MSC bit fields. Default Value: 0
6	AXI_MS2_MSC	Logical AND of corresponding APPCPUSS_INTR_MSC and APPCPUSS_INTR_MASK_MSC bit fields. Default Value: 0
5	AXI_MS1_MSC	Logical AND of corresponding APPCPUSS_INTR_MSC and APPCPUSS_INTR_MASK_MSC bit fields. Default Value: 0
4	AXI_MS0_MSC	Logical AND of corresponding APPCPUSS_INTR_MSC and APPCPUSS_INTR_MASK_MSC bit fields. Default Value: 0

1.1.204 APPCPUSS_INTR_MASKED_MSC (continued)

2	AXIDMAC0_MSC	Logical AND of corresponding APPCPUSS_INTR_MSC and APPCPUSS_INTR_MASK_MSC bit fields. Default Value: 0

1.1.205 APPCPUSS_INTR_AHB2AXI

Description: AHB to AXI Bridge Interrupt

Address: 0x441C0300

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1C
HW Access	Reserved							RW1S
Name	Reserved [7:1]							BUFF_WRITE_ERR

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	BUFF_WRITE_ERR	Set to '1', when there is a buffered write error occurs in xhb500 ahb to axi bridge Default Value: 0

1.1.206 APPCPUSS_INTR_SET_AHB2AXI

Description: AHB to AXI Bridge Interrupt set

Address: 0x441C0304

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							BUFF_WRITE_ERR

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	BUFF_WRITE_ERR	Write INTR_SET_AHB2AXI field with '1' to set corresponding INTR_AHB2AXI.BUFF_WRITE_ERR field (a write of '0' has no effect). Default Value: 0

1.1.207 APPCPUSS_INTR_MASK_AHB2AXI

Description: AHB to AXI Bridge Interrupt mask

Address: 0x441C0308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							BUFF_WRITE_ERR

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	BUFF_WRITE_ERR	Mask for corresponding field in INTR_AHB2AXI register. Default Value: 0

1.1.208 APPCPUSS_INTR_MASKED_AHB2AXI

Description: AHB to AXI Bridge Interrupt masked

Address: 0x441C030C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							BUFF_WRITE_ERR

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	BUFF_WRITE_ERR	Logical and of corresponding INTR_AHB2AXI and INTR_MASK_AHB2AXI fields. Default Value: 0

1.1.209 APPCPUSS_AP_CTL

Description: Access port control

Address: 0x441C1000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	Reserved		RW	RW
HW Access	Reserved		R	R	Reserved		R	R
Name	Reserved [7:6]		CM55_0_NID_ENABLE	CM55_0_DBG_ENABLE	Reserved [3:2]		CM55_1_ENABLE	CM55_0_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [15:10]						CM55_1_NID_ENABLE	CM55_1_DBG_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW1S	RW1S	Reserved		RW1S	RW1S
HW Access	Reserved		R	R	Reserved		R	R
Name	Reserved [23:22]		CM55_0_NID_DISABLE	CM55_0_DBG_DISABLE	Reserved [19:18]		CM55_1_DISABLE	CM55_0_DISABLE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW1S	RW1S
HW Access	Reserved						R	R
Name	Reserved [31:26]						CM55_1_NID_DISABLE	CM55_1_DBG_DISABLE

Bits	Name	Description
25	CM55_1_NID_DISABLE	Refer CM55_0_NID_DISABLE description. Default Value: 0
24	CM55_1_DBG_DISABLE	Refer CM55_0_DBG_DISABLE description. Default Value: 0
21	CM55_0_NID_DISABLE	Disable Non-invasive debug for CM55_0. '1': Disables all trace and non-invasive debug features. '0': Enables all trace and non-invasive debug features. Typically, this field is set by the Cypress boot code with information from eFUSE. The non-invasive debug is only enabled when CM55_0_NID_DISABLE is '0' and CM55_0_NID_ENABLE is '1'. Default Value: 0
20	CM55_0_DBG_DISABLE	Disable Invasive debug for CM55_0. '1': Disables all halt-mode and invasive debug features. '0': Enables invasive debug features. Typically, this field is set by the Cypress boot code with information from eFUSE. The invasive debug is only enabled when CM55_0_DBG_DISABLE is '0' and CM55_0_DBG_ENABLE is '1'. Default Value: 0

1.1.209 APPCPUSS_AP_CTL (continued)

17	CM55_1_DISABLE	Disables the CM55_1 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when CM55_1_DISABLE is '0' and CM55_1_ENABLE is '1'. Default Value: 0
16	CM55_0_DISABLE	Disables the CM55_0 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when CM55_0_DISABLE is '0' and CM55_0_ENABLE is '1'. Default Value: 0
9	CM55_1_NID_ENABLE	Refer CM55_0_NID_ENABLE. Default Value: 0
8	CM55_1_DBG_ENABLE	Refer CM55_0_DBG_ENABLE. Default Value: 0
5	CM55_0_NID_ENABLE	Non-invasive debug enable for CM55_0. '0': Disables all trace and non-invasive debug features. '1': Enables all trace and non-invasive debug features. Default Value: 0
4	CM55_0_DBG_ENABLE	Invasive debug enable for CM55_0. '0': Disables all halt-mode and invasive debug features. '1': Enables invasive debug features. Default Value: 0
1	CM55_1_ENABLE	Enables the CM55_1 AP interface: '0': Disabled. '1': Enabled. Default Value: 0
0	CM55_0_ENABLE	Enables the CM55_0 AP interface: '0': Disabled. '1': Enabled. Default Value: 0

1.1.210 MS_CTL_MS13_CTL

Description: Master 'x' protection context control

Address: 0x441C40D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PC_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	PC_MASK	Protection context mask for protection contexts "15" down to "0". Bit PC_MASK[i] indicates if the MS_PC_STRUCT[x].PC[3:0] protection context field can be set to the value "i": - PC_MASK[i] is '0': MS_PC_STRUCT[x].PC[3:0] can NOT be set to "i"; and PC[3:0] is not changed. - PC_MASK[i] is '1': MS_PC_STRUCT[x].PC[3:0] can be set to "i". Note: When CM33_0 CM33_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK[i] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 0, 1, 2 or 3 through HW (HW modifies MS_PC_STRUCT[x].PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts. Default Value: 64
1	NS	Master security controller configuration. 0: Bus master is secure. Master can send both secure and non-secure transfers. Accesses to secure addresses are not blocked and the security flag, HNONSEC, is set accordingly. 1: Bus master is non-secure. Master can send only non-secure transfers. Access to secure addresses, that is, outside the Uncheck regions, are blocked. Default Value: 1
0	P	Privileged setting ('0': user mode; '1': privileged mode). Notes: This field is ONLY used for masters that do NOT provide their own user/privileged access control attribute. The default/reset field value provides privileged mode access capabilities. Default Value: 1

1.1.211 MS_CTL_MS19_CTL

Description: Master 'x' protection context control

Address: 0x441C4130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PC_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	PC_MASK	Protection context mask for protection contexts "15" down to "0". Bit PC_MASK[i] indicates if the MS_PC_STRUCT[x].PC[3:0] protection context field can be set to the value "i": - PC_MASK[i] is '0': MS_PC_STRUCT[x].PC[3:0] can NOT be set to "i"; and PC[3:0] is not changed. - PC_MASK[i] is '1': MS_PC_STRUCT[x].PC[3:0] can be set to "i". Note: When CM33_0 CM33_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK[i] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 0, 1, 2 or 3 through HW (HW modifies MS_PC_STRUCT[x].PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts. Default Value: 64

1.1.212 MS_CTL_MS_PC13_PC

Description: Master 'x' protection context value

Address: 0x441C50D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	PC	Active protection context (PC). Modifications to this field are constrained by the associated MS_CTL_STRUCT[x].CTL.PC_MASK value. PC[3:0] can be set to "i" only if the corresponding mask bit (PC_MASK[i]) is '1'. Note: When the APPCPUSS works with the M33SYSCPUSS, PCx_HANDLER is NOT implemented as CM33_0_PC_CTL.VALID[3:0] is exported to the APPCPUSS to clear PC_MASK[i] of the APPCPUSS masters. Default Value: 6

1.1.213 MS_CTL_MS_PC13_PC_READ_MIR

Description: Master 'x' protection context value read mirror register

Address: 0x441C50D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	PC	Read-only mirror of PC.PC Default Value: 6

1.1.214 MS_CTL_AXIDMAC0_MSC_ACG_CTL

Description: AXI DMAC0 MSC and ACG configuration

Address: 0x441C6010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.215 MS_CTL_AXI_MS0_MSC_ACG_CTL

Description: AXI_MS0 master security Controller & ACG configuration

Address: 0x441C6030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.216 MS_CTL_AXI_MS1_MSC_ACG_CTL

Description: AXI_MS1 master security Controller & ACG configuration

Address: 0x441C6034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.217 MS_CTL_AXI_MS2_MSC_ACG_CTL

Description: AXI_MS2 master security Controller & ACG configuration

Address: 0x441C6038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.218 MS_CTL_AXI_MS3_MSC_ACG_CTL

Description: AXI_MS3 master security Controller & ACG configuration

Address: 0x441C603C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.219 MS_CTL_EXP_MS0_MSC_ACG_CTL

Description: EXP_MS0 master security Controller & ACG configuration

Address: 0x441C6040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.220 MS_CTL_EXP_MS1_MSC_ACG_CTL

Description: EXP_MS1 master security Controller & ACG configuration

Address: 0x441C6044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.221 MS_CTL_EXP_MS2_MSC_ACG_CTL

Description: EXP_MS2 master security Controller & ACG configuration

Address: 0x441C6048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.222 APPCPUSS_SL_CTL_SL_CTL

Description: Slave control (Clock enables)

Address: 0x441C8000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	Reserved	RW
HW Access	Reserved					R	Reserved	R
Name	Reserved [7:3]					IPC_ENABLED	Reserved	AXIDMAC0_ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	IPC_ENABLED	0: IPC disabled 1: IPC enabled Default Value: 1
0	AXIDMAC0_ENABLED	Slave enable controls. Each bit indicates whether the respective slave is enabled or not. 0: Disabled 1: Enabled If the slave is disabled, its clock is gated off (constant "0"). Any access (MMIO AHB access) to slave when disabled result in AHB error response. Default Value: 1

1.1.223 APPCPUSS_SL_CTL_SL_CTL2

Description: Slave control2 (Reset enables)

Address: 0x441C8004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	Reserved	RW
HW Access	Reserved					R	Reserved	R
Name	Reserved [7:3]					IPC_RST	Reserved	AXID-MAC0_RST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	IPC_RST	0: IPC reset disabled 1: IPC reset enabled Default Value: 0
0	AXIDMAC0_RST	Slave reset controls. Each bit indicates whether the respective slave reset is enabled or not. 0: Disabled 1: Enabled If the slave is under reset enabled state, its clock is gated off (constant "0") and its resets are in activated state (rst_n = 0) Any access (MMIO AHB access) to slave when disabled result in AHB error response. Default Value: 0

1.1.224 U550_ID

Description: ID Register

Address: 0x44600000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	VERSION_MINOR [7:4]				VERSION_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	R				R			
Name	PRODUCT_MAJOR [15:12]				VERSION_MAJOR [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	R				R			
Name	ARCH_MINOR_REV [23:20]				ARCH_PATCH_REV [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	R				R			
Name	ARCH_MAJOR_REV [31:28]				ARCH_MINOR_REV [27:24]			

Bits	Name	Description
31 : 28	ARCH_MAJOR_REV	This is the major architecture version number, a in the architecture version a.b (Implementation-defined) Default Value: 1
27 : 20	ARCH_MINOR_REV	This is the minor architecture version number, b in the architecture version a.b (Implementation-defined) Default Value: 1
19 : 16	ARCH_PATCH_REV	This is the patch number of the architecture version a.b (Implementation-defined) Default Value: 0
15 : 12	PRODUCT_MAJOR	This is the X-part of the ML00X product number (Implementation-defined) Default Value: 4
11 : 8	VERSION_MAJOR	This is the n for the R-part of an RnPn release number Default Value: 2
7 : 4	VERSION_MINOR	This is the n for the P-part of an RnPn release number Default Value: 0
3 : 0	VERSION_STATUS	This is the version of the product (Implementation-defined) Default Value: 1

1.1.225 U550_STATUS

Description: Register describes the current operating status of the NPU

Address: 0x44600004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	R	R	R	R
HW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
Name	Reserved	PMU_IRQ_RAISED	CMD_END_REACHED	CMD_PARSE_ERROR	RESET_STATUS	BUS_STATUS	IRQ_RAISED	STATE

Bits	15	14	13	12	11	10	9	8
SW Access	R				R	Reserved		
HW Access	RW				RW	Reserved		
Name	FAULTING_CHANNEL [15:12]				FAULTING_INTERFACE	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	IRQ_HISTORY_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	IRQ_HISTORY_MASK [31:24]							

Bits	Name	Description
31 : 16	IRQ_HISTORY_MASK	IRQ History mask This is used for debug purposes. Each IRQ or Event operation provides a 16-bit mask which is logically ORed into these bits. The bits can be cleared using the command register. Default Value: 0
15 : 12	FAULTING_CHANNEL	Faulting channel on a bus abort. Read: 0=Cmd, 1=IFM, 2=Weights, 3=Scale+Bias, 4=Mem2Mem; Write: 8=OFM, 9=Mem2Mem Default Value: 0
11	FAULTING_INTERFACE	Faulting interface on bus abort. 0=AXI-M0, 1=AXI-M1 Default Value: 0
6	PMU_IRQ_RAISED	0=No PMU IRQ, 1=PMU IRQ raised. Cleared by using command register bit 1 Default Value: 0
5	CMD_END_REACHED	0=Not reached, 1=Reached. Cleared by writing QBASE or QSIZE when the NPU is in stopped state. Default Value: 0
4	CMD_PARSE_ERROR	0=No error, 1=Command-stream parsing error detected. Can only be cleared by a reset. Default Value: 0

1.1.225 U550_STATUS (continued)

3	RESET_STATUS	Reset is ongoing and only this register can be read (other registers read as 0 and writes are ignored). A value of 0 means the NPU is not being reset and can be accessed as normal. Default Value: 1
2	BUS_STATUS	0=OK, 1=Bus abort detected and processing halted (the NPU has reached IDLE state and does not start to process any more commands/AXI transactions). Can only be cleared by a reset. Default Value: 0
1	IRQ_RAISED	Raw IRQ status: 0 = IRQ not raised, 1 = IRQ raised. IRQ is cleared using command register bit 1. Default Value: 0
0	STATE	NPU state; 0 = Stopped, 1 = Running Default Value: 0

1.1.226 U550_CMD

Description: Command register, reads as last written command

Address: 0x44600008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved [7:4]				POWER_Q_ENABLE	CLOCK_Q_ENABLE	CLEAR_IRQ	TRANSITION_TO_RUNNING_STATE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	CLEAR_IRQ_HISTORY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	CLEAR_IRQ_HISTORY [31:24]							

Bits	Name	Description
31 : 16	CLEAR_IRQ_HISTORY	Clears the IRQ history mask. When bit k is set, then the corresponding bit k of the STATUS register (IRQ history) is cleared. Default Value: 0
3	POWER_Q_ENABLE	Write 1 to this bit to enable power off using the Power Q-interface. Default Value: 1
2	CLOCK_Q_ENABLE	Write 1 to this bit to enable clock off using the Clock Q-interface and enable the main clock gate. Default Value: 1
1	CLEAR_IRQ	Write 1 to clear the IRQ status in the STATUS register. Writing 0 has no effect. Default Value: 0
0	TRANSITION_TO_RUNNING_STATE	Write 1 to transition the NPU to running state. Writing 0 has no effect. Default Value: 0

1.1.227 U550_RESET

Description: Request Reset and new security mode

Address: 0x4460000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						RW	RW
Name	Reserved [7:2]						PEND-ING_CSL	PEND-ING_CPL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	PENDING_CSL	Current security level: 0=Secure (default), 1=Non secure Default Value: 0
0	PENDING_CPL	Current privilege level: 0=User (default), 1=Privileged Default Value: 0

1.1.228 U550_QBASE0

Description: Base address of Command-queue bits [31 downto 0]. The address is 4-byte-aligned

Address: 0x44600010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	QBASE0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	QBASE0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	QBASE0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	QBASE0 [31:24]							

Bits	Name	Description
31 : 0	QBASE0	The 4-byte-aligned lower bytes of the base address value for the command stream. Default Value: 0

1.1.229 U550_QBASE1

Description: Address extension bits [47 downto 32] for queue base

Address: 0x44600014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	QBASE1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	QBASE1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	QBASE1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	QBASE1 [31:24]							

Bits	Name	Description
31 : 0	QBASE1	The 4-byte-aligned upper bytes of the base address value for the command stream Default Value: 0

1.1.230 U550_QREAD

Description: Read offset in the command stream in bytes. Multiples of 4 in the range 0-16 MB

Address: 0x44600018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RO							
HW Access	RW							
Name	QREAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RO							
HW Access	RW							
Name	QREAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RO							
HW Access	RW							
Name	QREAD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RO							
HW Access	RW							
Name	QREAD [31:24]							

Bits	Name	Description
31 : 0	QREAD	The read offset of the current command under execution Default Value: 0

1.1.231 U550_QCONFIG

Description: AXI configuration for the command stream in the range 0-3. Same encoding as for REGIONCFG

Address: 0x4460001C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	QCONFIG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	QCONFIG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	QCONFIG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	QCONFIG [31:24]							

Bits	Name	Description
31 : 0	QCONFIG	AXI configuration for the command stream in the range 0-3 Default Value: 0

1.1.232 U550_QSIZE

Description: Size of the command stream in bytes. Multiples of 4 in the range 0-16 MB

Address: 0x44600020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	QSIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	QSIZE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	QSIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	QSIZE [31:24]							

Bits	Name	Description
31 : 0	QSIZE	Size of the next command stream to be executed by the NPU Default Value: 0

1.1.233 U550_PROT

Description: Protection level configured for the NPU when acting as an AXI master

Address: 0x44600024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						R	R
Name	Reserved [7:2]						ACTIVE_CSL	ACTIVE_CPL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	ACTIVE_CSL	Current security level. 0 = Secure 1 = Non-secure This is used as AxPROT[1] when the NPU is a master and set from Pending CSL after the reset is complete. - After a hard reset, this is set to Power-on-reset security level (PORSL), which allows for CPUs that do not support TrustZone. - After a soft reset, this is set to pending_CSL, if PPROT[1]==0, otherwise it is set to 1. For this to be effective, there must be a memory-protection controller included in the system. Depends on ROT_INIT.SECURITY_LEVEL Default Value: 1
0	ACTIVE_CPL	Current privilege level. 0 = User 1 = Privilege This is used as AxPROT[0] when the NPU is a master. - After hard reset, this is set to Power-on-reset privilege level (PORPL). - After soft reset, this is set to pending_CPL, if PPROT[0]==1, otherwise it is set to 0. For this to be effective, there must be a system-level MPU built for the system. Depends on ROT_INIT.PRIVILEGE_LEVEL Default Value: 0

1.1.234 U550_CONFIG

Description: RTL configuration

Address: 0x44600028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RO				RO			
HW Access	R				R			
Name	CMD_STREAM_VERSION [7:4]				MACS_PER_CC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RO							
HW Access	R							
Name	SHRAM_SIZE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RO				Reserved			
HW Access	R				Reserved			
Name	PRODUCT [31:28]				Reserved [27:24]			

Bits	Name	Description
31 : 28	PRODUCT	Product configuration (implementation defined) Default Value: 0
15 : 8	SHRAM_SIZE	Size in KB of SHRAM in the range 8-48. 0x10 = 16KB 0x18 = 24KB 0x30 = 48KB Default Value: 0x18
7 : 4	CMD_STREAM_VER-SION	Command stream version accepted by this NPU Default Value: 0
3 : 0	MACS_PER_CC	The log2(macs/clock cycle). Valid encoding range is 5-8 for 32-256 MACs/clock cycle. 5 = 2^5 MACS/cycle 6 = 2^6 MACS/cycle 7 = 2^7 MACS/cycle 8 = 2^8 MACS/cycle Default Value: 7

1.1.235 U550_LOCK

Description: Lock register. This register is designed for driver use and does not affect NPU functionality

Address: 0x4460002C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LOCK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOCK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	LOCK [31:24]							

Bits	Name	Description
31 : 0	LOCK	This register is designed for driver use and does not affect NPU functionality. Default Value: 0

1.1.236 U550_REGIONCFG

Description: Base pointer configuration. Bits[2*k+1 downto 2*k] give the memory type for REGION[k]

Address: 0x4460003C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	REGION3 [7:6]		REGION2 [5:4]		REGION1 [3:2]		REGION0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	REGION7 [15:14]		REGION6 [13:12]		REGION5 [11:10]		REGION4 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	REGION7	0 = AXI0 port, outstanding counter 0; AXI limits are set by the AXI_LIMIT0 register. 1 = AXI0 port, outstanding counter 1; AXI limits are set by the AXI_LIMIT1 register. 2 = AXI1 port, outstanding counter 2; AXI limits are set by the AXI_LIMIT2 register. 3 = AXI1 port, outstanding counter 3; AXI limits are set by the AXI_LIMIT3 register. Default Value: 0
13 : 12	REGION6	same description as REGION7 field. Default Value: 0
11 : 10	REGION5	same description as REGION7 field. Default Value: 0
9 : 8	REGION4	same description as REGION7 field. Default Value: 0
7 : 6	REGION3	same description as REGION7 field. Default Value: 0
5 : 4	REGION2	same description as REGION7 field. Default Value: 0
3 : 2	REGION1	same description as REGION7 field. Default Value: 0
1 : 0	REGION0	same description as REGION7 field. Default Value: 0

1.1.237 U550_AXI_LIMIT0

Description: AXI limits for port 0 counter 0

Address: 0x44600040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				Reserved		RW	
HW Access	R				Reserved		R	
Name	MEMTYPE [7:4]				Reserved [3:2]		MAX_BEATS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MAX_OUTSTANDING_READ_M1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MAX_OUTSTANDING_WRITE_M1 [31:24]							

Bits	Name	Description
31 : 24	MAX_OUTSTAND-ING_WRITE_M1	Maximum number of outstanding AXI write transactions, in range 0-15 Default Value: 0
23 : 16	MAX_OUTSTAND-ING_READ_M1	Maximum number of outstanding AXI read transactions, in range 0-15 Default Value: 0
7 : 4	MEMTYPE	Memtype. Default Value: 0
1 : 0	MAX_BEATS	Burst-split alignment: 0=64 bytes, 1=128 bytes, 2=256 bytes, 3=reserved Default Value: 0

1.1.238 U550_AXI_LIMIT1

Description: AXI limits for port 0 counter 1

Address: 0x44600044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				Reserved		RW	
HW Access	R				Reserved		R	
Name	MEMTYPE [7:4]				Reserved [3:2]		MAX_BEATS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MAX_OUTSTANDING_READ_M1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MAX_OUTSTANDING_WRITE_M1 [31:24]							

Bits	Name	Description
31 : 24	MAX_OUTSTAND-ING_WRITE_M1	Maximum number of outstanding AXI write transactions, in range 0-15 Default Value: 0
23 : 16	MAX_OUTSTAND-ING_READ_M1	Maximum number of outstanding AXI read transactions, in range 0-15 Default Value: 0
7 : 4	MEMTYPE	Memtype. Default Value: 0
1 : 0	MAX_BEATS	Burst-split alignment: 0=64 bytes, 1=128 bytes, 2=256 bytes, 3=reserved Default Value: 0

1.1.239 U550_AXI_LIMIT2

Description: AXI limits for port 1 counter 2

Address: 0x44600048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				Reserved		RW	
HW Access	R				Reserved		R	
Name	MEMTYPE [7:4]				Reserved [3:2]		MAX_BEATS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MAX_OUTSTANDING_READ_M1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MAX_OUTSTANDING_WRITE_M1 [31:24]							

Bits	Name	Description
31 : 24	MAX_OUTSTAND-ING_WRITE_M1	Maximum number of outstanding AXI write transactions, in range 0-15 Default Value: 0
23 : 16	MAX_OUTSTAND-ING_READ_M1	Maximum number of outstanding AXI read transactions, in range 0-15 Default Value: 0
7 : 4	MEMTYPE	Memtype. Default Value: 0
1 : 0	MAX_BEATS	Burst-split alignment: 0=64 bytes, 1=128 bytes, 2=256 bytes, 3=reserved Default Value: 0

1.1.240 U550_AXI_LIMIT3

Description: AXI limits for port 1 counter 3

Address: 0x4460004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				Reserved		RW	
HW Access	R				Reserved		R	
Name	MEMTYPE [7:4]				Reserved [3:2]		MAX_BEATS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MAX_OUTSTANDING_READ_M1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MAX_OUTSTANDING_WRITE_M1 [31:24]							

Bits	Name	Description
31 : 24	MAX_OUTSTAND-ING_WRITE_M1	Maximum number of outstanding AXI write transactions, in range 0-15 Default Value: 0
23 : 16	MAX_OUTSTAND-ING_READ_M1	Maximum number of outstanding AXI read transactions, in range 0-15 Default Value: 0
7 : 4	MEMTYPE	Memtype. Default Value: 0
1 : 0	MAX_BEATS	Burst-split alignment: 0=64 bytes, 1=128 bytes, 2=256 bytes, 3=reserved Default Value: 0

1.1.241 U550_BASEP0

Description: Lower 32 bits of the base pointer for region index 0

Address: 0x44600080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The low word of the 64-bit address Default Value: 0

1.1.242 U550_BASEP1

Description: Upper 32-bits of the base pointer for region index 0

Address: 0x44600084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The high word of the 64-bit address Default Value: 0

1.1.243 U550_BASEP2

Description: Lower 32 bits of the base pointer for region index 1

Address: 0x44600088

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The low word of the 64-bit address Default Value: 0

1.1.244 U550_BASEP3

Description: Upper 32-bits of the base pointer for region index 1

Address: 0x4460008C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The high word of the 64-bit address Default Value: 0

1.1.245 U550_BASEP4

Description: Lower 32 bits of the base pointer for region index 2

Address: 0x44600090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The low word of the 64-bit address Default Value: 0

1.1.246 U550_BASEP5

Description: Upper 32-bits of the base pointer for region index 2

Address: 0x44600094

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The high word of the 64-bit address Default Value: 0

1.1.247 U550_BASEP6

Description: Lower 32 bits of the base pointer for region index 3

Address: 0x44600098

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The low word of the 64-bit address Default Value: 0

1.1.248 U550_BASEP7

Description: Upper 32-bits of the base pointer for region index 3

Address: 0x4460009C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The high word of the 64-bit address Default Value: 0

1.1.249 U550_BASEP8

Description: Lower 32 bits of the base pointer for region index 4

Address: 0x446000A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The low word of the 64-bit address Default Value: 0

1.1.250 U550_BASEP9

Description: Upper 32-bits of the base pointer for region index 4

Address: 0x446000A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The high word of the 64-bit address Default Value: 0

1.1.251 U550_BASEP10

Description: Lower 32 bits of the base pointer for region index 5

Address: 0x446000A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The low word of the 64-bit address Default Value: 0

1.1.252 U550_BASEP11

Description: Upper 32-bits of the base pointer for region index 5

Address: 0x446000AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The high word of the 64-bit address Default Value: 0

1.1.253 U550_BASEP12

Description: Lower 32 bits of the base pointer for region index 6

Address: 0x446000B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The low word of the 64-bit address Default Value: 0

1.1.254 U550_BASEP13

Description: Upper 32-bits of the base pointer for region index 6

Address: 0x446000B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The high word of the 64-bit address Default Value: 0

1.1.255 U550_BASEP14

Description: Lower 32 bits of the base pointer for region index 7

Address: 0x446000B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The low word of the 64-bit address Default Value: 0

1.1.256 U550_BASEP15

Description: Upper 32-bits of the base pointer for region index 7

Address: 0x446000BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDR_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR_WORD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR_WORD [31:24]							

Bits	Name	Description
31 : 0	ADDR_WORD	The high word of the 64-bit address Default Value: 0

1.1.257 U550_PMCR

Description: PMU master control register

Address: 0x44600180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved [7:4]				MASK_EN	CY-CLE_CNT_RST	EVENT_CNT_RST	CNT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	R					Reserved		
HW Access						Reserved		
Name	NUM_EVENT_CNT [15:11]					Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 11	NUM_EVENT_CNT	Number of event counters available for performance measurement Default Value: 0x04
3	MASK_EN	PMU can be enabled/disabled by command stream operation NPU_OP_PMU_MASK Default Value: 0
2	CYCLE_CNT_RST	Reset cycle counter. Writing a 1 to this register resets the cycle counter. If the cycle counter is active, it will continue counting after reset. This register bit always reads a 0. Default Value: 0
1	EVENT_CNT_RST	Reset event counter. Writing a 1 to this field resets all event counters. If any counter is active, it will continue counting after reset. This register bit always reads a 0. Default Value: 0
0	CNT_EN	Enable counter. This is the master switch. When the switch is disabled, the PMU is always off. Default Value: 0

1.1.258 U550_PMCNTENSET

Description: Count-enable set register

Address: 0x44600184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				EVENT_CNT_3	EVENT_CNT_2	EVENT_CNT_1	EVENT_CNT_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	CY-CLE_CNT	Reserved [30:24]						

Bits	Name	Description
31	CYCLE_CNT	PMCCNTR enable bit. Enables the dedicated cycle counter, PMCCNTR. 0 (default) When read, it means the cycle counter is disabled. When written, it has no effect. 1 When read, it means the cycle counter is enabled. When written, it enables the cycle counter. Default Value: 0
3	EVENT_CNT_3	Event-counter enable bit for PMU_EVCNTRn, where n=3. 0 (default) When read, it means that PMU_EVCNTRn is disabled. When written, it has no effect. 1 When read, it means that PMU_EVCNTRn event counter is enabled. When written, it enables PMU_EVCNTRn. Default Value: 0
2	EVENT_CNT_2	Event-counter enable bit for PMU_EVCNTRn, where n=2. 0 (default) When read, it means that PMU_EVCNTRn is disabled. When written, it has no effect. 1 When read, it means that PMU_EVCNTRn event counter is enabled. When written, it enables PMU_EVCNTRn. Default Value: 0
1	EVENT_CNT_1	Event-counter enable bit for PMU_EVCNTRn, where n=1. 0 (default) When read, it means that PMU_EVCNTRn is disabled. When written, it has no effect. 1 When read, it means that PMU_EVCNTRn event counter is enabled. When written, it enables PMU_EVCNTRn. Default Value: 0

1.1.258 U550_PMCNTENSET (continued)

0	EVENT_CNT_0	Event-counter enable bit for PMU_EVCNTRn, where n=0. 0 (default) When read, it means that PMU_EVCNTRn is disabled. When written, it has no effect. 1 When read, it means that PMU_EVCNTRn event counter is enabled. When written, it enables PMU_EVCNTRn. Default Value: 0

1.1.259 U550_PMCNTENCLR

Description: Count-enable clear register

Address: 0x44600188

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				EVENT_CNT_3	EVENT_CNT_2	EVENT_CNT_1	EVENT_CNT_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	CY-CLE_CNT	Reserved [30:24]						

Bits	Name	Description
31	CYCLE_CNT	PMCCNTR disable bit. Disables the dedicated cycle counter, PMCCNTR. 0 (default) When read, it means the cycle counter is disabled. When written, it has no effect. 1 When read, it means the cycle counter is enabled. When written, it disables the cycle counter. Default Value: 0
3	EVENT_CNT_3	Event-counter disable bit for PMU_EVCNTRn, where n=3. 0 (default) When read, it means that PMU_EVCNTRn is disabled. When written, it has no effect. 1 When read, it means that PMU_EVCNTRn event counter is enabled. When written, it disables PMU_EVCNTRn. Default Value: 0
2	EVENT_CNT_2	Event-counter disable bit for PMU_EVCNTRn, where n=2. 0 (default) When read, it means that PMU_EVCNTRn is disabled. When written, it has no effect. 1 When read, it means that PMU_EVCNTRn event counter is enabled. When written, it disables PMU_EVCNTRn. Default Value: 0
1	EVENT_CNT_1	Event-counter disable bit for PMU_EVCNTRn, where n=1. 0 (default) When read, it means that PMU_EVCNTRn is disabled. When written, it has no effect. 1 When read, it means that PMU_EVCNTRn event counter is enabled. When written, it disables PMU_EVCNTRn. Default Value: 0

1.1.259 U550_PMCNTENCLR (continued)

0	EVENT_CNT_0	Event-counter disable bit for PMU_EVCNTRn, where n=0. 0 (default) When read, it means that PMU_EVCNTRn is disabled. When written, it has no effect. 1 When read, it means that PMU_EVCNTRn event counter is enabled. When written, it disables PMU_EVCNTRn. Default Value: 0

1.1.260 U550_PMOVSSET

Description: Overflow-flag status set register

Address: 0x4460018C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				RW	RW	RW	RW
Name	Reserved [7:4]				EVENT_CNT_3_OVF	EVENT_CNT_2_OVF	EVENT_CNT_1_OVF	EVENT_CNT_0_OVF

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	RW	Reserved						
Name	CYCLE_CNT_OVF	Reserved [30:24]						

Bits	Name	Description
31	CYCLE_CNT_OVF	Set PMCCNTR overflow Default Value: 0
3	EVENT_CNT_3_OVF	Event-counter overflow set bit for PMU_EVCNTR3. 0 (default) When read, it means the cycle counter has not overflowed. When written, it has no effect. 1 When read, it means the cycle counter has overflowed. When written, it sets the overflow bit to 1. Default Value: 0
2	EVENT_CNT_2_OVF	Event-counter overflow set bit for PMU_EVCNTR2. 0 (default) When read, it means the cycle counter has not overflowed. When written, it has no effect. 1 When read, it means the cycle counter has overflowed. When written, it sets the overflow bit to 1. Default Value: 0
1	EVENT_CNT_1_OVF	Event-counter overflow set bit for PMU_EVCNTR1. 0 (default) When read, it means the cycle counter has not overflowed. When written, it has no effect. 1 When read, it means the cycle counter has overflowed. When written, it sets the overflow bit to 1. Default Value: 0

1.1.260 U550_PMOVSSET (continued)

0	EVENT_CNT_0_OVF	Event-counter overflow set bit for PMU_EVCNTR0. 0 (default) When read, it means the cycle counter has not overflowed. When written, it has no effect. 1 When read, it means the cycle counter has overflowed. When written, it sets the overflow bit to 1. Default Value: 0

1.1.261 U550_PMOVSCLR

Description: Overflow-flag status clear register

Address: 0x44600190

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				RW	RW	RW	RW
Name	Reserved [7:4]				EVENT_CNT_3_OVF	EVENT_CNT_2_OVF	EVENT_CNT_1_OVF	EVENT_CNT_0_OVF

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	RW	Reserved						
Name	CYCLE_CNT_OVF	Reserved [30:24]						

Bits	Name	Description
31	CYCLE_CNT_OVF	Clear PMCCNTR overflow Default Value: 0
3	EVENT_CNT_3_OVF	Event-counter overflow clear bit for PMU_EVCNTR3. 0 (default) When read, it means the cycle counter has not overflowed. When written, it has no effect. 1 When read, it means the cycle counter has overflowed. When written, it clears the overflow bit to 0. Default Value: 0
2	EVENT_CNT_2_OVF	Event-counter overflow clear bit for PMU_EVCNTR2. 0 (default) When read, it means the cycle counter has not overflowed. When written, it has no effect. 1 When read, it means the cycle counter has overflowed. When written, it clears the overflow bit to 0. Default Value: 0
1	EVENT_CNT_1_OVF	Event-counter overflow clear bit for PMU_EVCNTR1. 0 (default) When read, it means the cycle counter has not overflowed. When written, it has no effect. 1 When read, it means the cycle counter has overflowed. When written, it clears the overflow bit to 0. Default Value: 0

1.1.261 U550_PMOVSCLR (continued)

0	EVENT_CNT_0_OVF	Event-counter overflow clear bit for PMU_EVCNTR0. 0 (default) When read, it means the cycle counter has not overflowed. When written, it has no effect. 1 When read, it means the cycle counter has overflowed. When written, it clears the overflow bit to 0. Default Value: 0

1.1.262 U550_PMINTSET

Description: Interrupt-enable set register

Address: 0x44600194

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved [7:4]				EVENT_CNT_3_INT	EVENT_CNT_2_INT	EVENT_CNT_1_INT	EVENT_CNT_0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access		Reserved						
Name	CYCLE_CNT_INT	Reserved [30:24]						

Bits	Name	Description
31	CYCLE_CNT_INT	PMCCNTR overflow interrupt-request enable bit 0 (default) When read, it means the cycle-counter overflow interrupt request is disabled. When written, it has no effect. 1 When read, it means the cycle-counter overflow interrupt request is enabled. When written, it enables the cycle count overflow interrupt request. Default Value: 0
3	EVENT_CNT_3_INT	Event-counter overflow interrupt-request enable bit for PMU_EVCNTR3 0 (default) When read, it means that the event-counter interrupt request is disabled. When written, it has no effect. 1 When read, it means that the event-counter interrupt request is enabled. When written, it enables theinterrupt request. Default Value: 0
2	EVENT_CNT_2_INT	Event-counter overflow interrupt-request enable bit for PMU_EVCNTR2 0 (default) When read, it means that the event-counter interrupt request is disabled. When written, it has no effect. 1 When read, it means that the event-counter interrupt request is enabled. When written, it enables theinterrupt request. Default Value: 0

1.1.262 U550_PMINTSET (continued)

1	EVENT_CNT_1_INT	Event-counter overflow interrupt-request enable bit for PMU_EVCNTR1 0 (default) When read, it means that the event-counter interrupt request is disabled. When written, it has no effect. 1 When read, it means that the event-counter interrupt request is enabled. When written, it enables theinterrupt request. Default Value: 0
0	EVENT_CNT_0_INT	Event-counter overflow interrupt-request enable bit for PMU_EVCNTR0 0 (default) When read, it means that the event-counter interrupt request is disabled. When written, it has no effect. 1 When read, it means that the event-counter interrupt request is enabled. When written, it enables theinterrupt request. Default Value: 0

1.1.263 U550_PMINTCLR

Description: Interrupt-enable clear register

Address: 0x44600198

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved [7:4]				EVENT_CNT_3_INT	EVENT_CNT_2_INT	EVENT_CNT_1_INT	EVENT_CNT_0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access		Reserved						
Name	CYCLE_CNT_INT	Reserved [30:24]						

Bits	Name	Description
31	CYCLE_CNT_INT	PMCCNTR overflow interrupt-request disable bit 0 (default) When read, it means the cycle-counter overflow interrupt request is disabled. When written, it has no effect. 1 When read, it means the cycle-counter overflow interrupt request is enabled. When written, it disables the cycle count overflow interrupt request. Default Value: 0
3	EVENT_CNT_3_INT	Event-counter overflow interrupt-request disable bit for PMU_EVCNTR3 0 (default) When read, it means that the event-counter interrupt request is disabled. When written, it has no effect. 1 When read, it means that the event-counter interrupt request is enabled. When written, it disables the interrupt request. Default Value: 0
2	EVENT_CNT_2_INT	Event-counter overflow interrupt-request disable bit for PMU_EVCNTR2 0 (default) When read, it means that the event-counter interrupt request is disabled. When written, it has no effect. 1 When read, it means that the event-counter interrupt request is enabled. When written, it disables the interrupt request. Default Value: 0

1.1.263 U550_PMINTCLR (continued)

1	EVENT_CNT_1_INT	Event-counter overflow interrupt-request disable bit for PMU_EVCNTR1 0 (default) When read, it means that the event-counter interrupt request is disabled. When written, it has no effect. 1 When read, it means that the event-counter interrupt request is enabled. When written, it disables the interrupt request. Default Value: 0
0	EVENT_CNT_0_INT	Event-counter overflow interrupt-request disable bit for PMU_EVCNTR0 0 (default) When read, it means that the event-counter interrupt request is disabled. When written, it has no effect. 1 When read, it means that the event-counter interrupt request is enabled. When written, it disables the interrupt request. Default Value: 0

1.1.264 U550_PMCCNTR_LO

Description: Performance-monitor cycle count low register

Address: 0x446001A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	CYCLE_CNT_LO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	CYCLE_CNT_LO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	CYCLE_CNT_LO [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	CYCLE_CNT_LO [31:24]							

Bits	Name	Description
31 : 0	CYCLE_CNT_LO	Performance-monitor cycle count low register. This represents the lower 32 bits of the dedicated 48-bit cycle counter, PMCCNTR. Default Value: 0

1.1.265 U550_PMCCNTR_HI

Description: Performance-monitor cycle count high register

Address: 0x446001A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	CYCLE_CNT_HI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	CYCLE_CNT_HI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	CYCLE_CNT_HI	Performance-monitor cycle count high register. This represents the higher 16 bits of the dedicated 48-bit cycle counter, PMCCNTR. Default Value: 0

1.1.266 U550_PMCCNTR_CFG

Description: Set start/stop event on the cycle counter.

Address: 0x446001A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	CYCLE_CNT_CFG_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [15:10]						CYCLE_CNT_CF-G_START [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	CYCLE_CNT_CFG_STOP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [31:26]						CYCLE_CNT_CFG_STOP [25:24]	

Bits	Name	Description
25 : 16	CYCLE_CNT_CFG_STOP	Cycle counter stop event Default Value: 0
9 : 0	CYCLE_CNT_CF-G_START	Cycle counter start event Default Value: 0

1.1.267 U550_PMCAXI_CHAN

Description: Set which AXI channel monitor

Address: 0x446001AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved							
Name	Reserved [7:4]				CH_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW	RW	
HW Access	Reserved							
Name	Reserved [15:11]					BW_CH_SEL_EN	AXI_CNT_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10	BW_CH_SEL_EN	Enable bandwidth channel selector: 0=AXI bw events measured for all channels, 1=AXI bw events measured for channel specified by CH_SEL Default Value: 0
9 : 8	AXI_CNT_SEL	Select AXI counter to monitor for latency measurements (0=AXI0 counter0, 1=AXI0 counter1, 2=AXI1 counter 2, 3=AXI1 counter3) Default Value: 0
3 : 0	CH_SEL	Specify the type of traffic for bandwidth or latency measurements (Read: 0=command traffic, 1=IFM traffic, 2=Weight traffic, 3=Scale+Bias, 4=Mem2Mem traffic - read direction; Write: 8=OFM traffic, 9=Mem2Mem traffic - write direction) Default Value: 0

1.1.268 U550_PMU_EVCNTR0

Description: Performance monitor event counters

Address: 0x44600300

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	SW							
HW Access								
Name	PMU_EVCNTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	SW							
HW Access								
Name	PMU_EVCNTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	SW							
HW Access								
Name	PMU_EVCNTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	SW							
HW Access								
Name	PMU_EVCNTR [31:24]							

Bits	Name	Description
31 : 0	PMU_EVCNTR	Performance-monitor event counters. PMU_EVCNTR[k]: these are the four 32-bit performance counters (k=0-3). Default Value: 0

1.1.269 U550_PMU_ENTYPER0

Description: Performance monitor event type control counters

Address: 0x44600380

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	EV_TYPE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [15:10]						EV_TYPE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description

1.1.269 U550_PMU_ENTYPER0 (continued)

9 : 0	EV_TYPE	Event type: 0x00 (default) no_event No event counted (the event never occurs) 0x11-0x5b - - 0x80 axi0_rd_trans_accepted AXI-0 read transfer accepted, arready & arvalid (number of read transfers) 0x81 - - 0x82 axi0_rd_data_beat_received AXI-0, rready & rvalid (read bandwidth) 0x83 axi0_rd_tran_req_stalled AXI-0, arvalid & ~arready (read stalls due memory system) 0x84 axi0_wr_trans_accepted AXI0, awready & awvalid (number write transfers) 0x85-0x86 - - 0x87 axi0_wr_data_beat_written AXI-0, wvalid wready (write bandwidth) 0x88 axi0_wr_tran_req_stalled AXI-0, awvalid & ~awready (write transfer stalls due to memory system) 0x89 axi0_wr_data_beat_stalled AXI-0, wvalid & ~wready (write beat stalls due to memory system) 0x8a-0x8b - - 0x8c axi0_enabled_cycles AXI-0, aclken_input (memory system frequency) 0x8d - - 0x8e axi0_rd_stall_limit AXI-0, check if read stalled due to AXI counter limit reached 0x8f axi0_wr_stall_limit AXI-0, check if write stalled due to AXI counter limit reached 0x180 axi1_rd_trans_accepted AXI-1 read transfer accepted, arready & arvalid (number of read transfers) 0x181 - - 0x182 axi1_rd_data_beat_received AXI-1, rready & rvalid (read bandwidth) 0x183 axi1_rd_tran_req_stalled AXI-1, arvalid & ~arready (read stalls due memory system) 0x184 axi1_wr_trans_accepted AXI-1, awready & awvalid (number write transfers) 0x185-0x186 - - 0x187 axi1_wr_data_beat_written AXI-1, wvalid & wready (write bandwidth) 0x188 axi1_wr_tran_req_stalled AXI-1, awvalid & ~awready (write transfer stalls due to memory system) 0x189 axi1_wr_data_beat_stalled AXI-1, wvalid & ~wready (write beat stalls due to memory system) 0x18a-0x18b - - 0x18c axi1_enabled_cycles AXI-1, aclken_input (memory system frequency) 0x18d - - 0x18e axi1_rd_stall_limit AXI-1, check if read stalled due to AXI counter limit reached 0x18f axi1_wr_stall_limit AXI-1, check if write stalled due to AXI counter limit reached 0xa0 axi_latency_any Any latency; measures the total number of transactions for the specified ID and interface 0xa1 axi_latency_32 Latency was >= 32 cycles 0xa2 axi_latency_64 Latency was >= 64 cycles 0xa3 axi_latency_128 Latency was >= 128 cycles 0xa4 axi_latency_256 Latency was >= 256 cycles 0xa5 axi_latency_512 Latency was >= 512 cycles 0xa6 axi_latency_1024 Latency was >= 1024 cycles Default Value: 0

1.1.270 U550_PID4

Description: Peripheral ID byte 4 (Arm = code 4)

Address: 0x44600FD0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PID4 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PID4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PID4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PID4 [31:24]							

Bits	Name	Description
31 : 0	PID4	Byte 4 of the Peripheral ID (Lower 8 bits valid) Default Value: 4

1.1.271 U550_PID5

Description: Peripheral ID byte 5. (reserved)

Address: 0x44600FD4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PID5 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PID5 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PID5 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PID5 [31:24]							

Bits	Name	Description
31 : 0	PID5	Byte 5 of the Peripheral ID (Lower 8 bits valid) Default Value: 0

1.1.272 U550_PID6

Description: Peripheral ID byte 6. (reserved)

Address: 0x44600FD8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PID6 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PID6 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PID6 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PID6 [31:24]							

Bits	Name	Description
31 : 0	PID6	Byte 6 of the Peripheral ID (Lower 8 bits valid) Default Value: 0

1.1.273 U550_PID7

Description: Peripheral ID byte 7. (reserved)

Address: 0x44600FDC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PID7 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PID7 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PID7 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PID7 [31:24]							

Bits	Name	Description
31 : 0	PID7	Byte 7 of the Peripheral ID (Lower 8 bits valid) Default Value: 0

1.1.274 U550_PID0

Description: Peripheral ID byte 0. This is bits[7 downto 0] of the part number.

Address: 0x44600FE0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PID0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PID0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PID0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PID0 [31:24]							

Bits	Name	Description
31 : 0	PID0	Byte 0 of the Peripheral ID (Lower 8 bits valid) Default Value: 0x80

1.1.275 U550_PID1

Description: Peripheral ID byte 1. This is bits[11 downto 8] of the part number in bits[3 downto 0], and bits[3 downto 0] of the Arm ID in bits[7 downto 4].

Address: 0x44600FE4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PID1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PID1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PID1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PID1 [31:24]							

Bits	Name	Description
31 : 0	PID1	Byte 1 of the Peripheral ID (Lower 8 bits valid) Default Value: 0xB5

1.1.276 U550_PID2

Description: Peripheral ID byte 2. This is bits[6 downto 4] of the Arm ID in bits[2 downto 0], and bit 3 indicates format B.

Address: 0x44600FE8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PID2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PID2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PID2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PID2 [31:24]							

Bits	Name	Description
31 : 0	PID2	Byte 2 of the Peripheral ID (Lower 8 bits valid) Default Value: 0x0B

1.1.277 U550_PID3

Description: Peripheral ID byte 3

Address: 0x44600FEC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PID3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PID3 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PID3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PID3 [31:24]							

Bits	Name	Description
31 : 0	PID3	Byte 3 of the Peripheral ID (Lower 8 bits valid) Default Value: 0

1.1.278 U550_CID0

Description: Component ID byte 0

Address: 0x44600FF0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	CID0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	CID0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	CID0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	CID0 [31:24]							

Bits	Name	Description
31 : 0	CID0	Byte 0 of the Component ID (Lower 8 bits valid) Default Value: 0x0D

1.1.279 U550_CID1

Description: Component ID byte 1

Address: 0x44600FF4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	CID1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	CID1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	CID1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	CID1 [31:24]							

Bits	Name	Description
31 : 0	CID1	Byte 1 of the Component ID (Lower 8 bits valid) Default Value: 0xF0

1.1.280 U550_CID2

Description: Component ID byte 2

Address: 0x44600FF8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	CID2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	CID2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	CID2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	CID2 [31:24]							

Bits	Name	Description
31 : 0	CID2	Byte 2 of the Component ID (Lower 8 bits valid) Default Value: 0x05

1.1.281 U550_CID3

Description: Component ID byte 3

Address: 0x44600FFC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	CID3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	CID3 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	CID3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	CID3 [31:24]							

Bits	Name	Description
31 : 0	CID3	Byte 3 of the Component ID (Lower 8 bits valid) Default Value: 0xB1

1.1.282 U550_ROT_INIT

Description: Initial settings

Address: 0x44601000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	Reserved
HW Access	Reserved					R	R	Reserved
Name	Reserved [7:3]					SECURI-TY_LEVEL	PRIVI-LEGE_LEV-EL	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	SECURITY_LEVEL	Initial security level after power-up. 0 = Secure 1 = Non-secure Default Value: 1
1	PRIVILEGE_LEVEL	Initial privilege level after power-up. 0 = User 1 = Privileged Default Value: 0

1.1.283 U550_ACG_CTL

Description: ACG Configuration of ARMU55 Bridge

Address: 0x44601004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							CF-G_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.284 U550_MXU55_PPU_PWPR

Description: Power Policy Register

Address: 0x44602000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			LOCK_EN	Reserved [11:9]			PWR_DY-N_EN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							OP_DY-N_EN

Bits	Name	Description
24	OP_DYN_EN	Reserved Default Value: 0x0
19 : 16	OP_POLICY	Reserved Default Value: 0x0
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. When this bit is set to 1 dynamic transitions are enabled for power modes, allowing transitions to be initiated by changes on power mode DEVACTIVE inputs. Default Value: 0x0
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x0

1.1.285 U550_MXU55_PPU_PMER

Description: Power Mode Emulation Register

Address: 0x44602004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							EMU_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	EMU_EN	Reserved Default Value: 0x0

1.1.286 U550_MXU55_PPU_PWSR

Description: Power Status Register

Address: 0x44602008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PWR_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved			R
HW Access	Reserved			RW	Reserved			RW
Name	Reserved [15:13]			LOCK_STA-TUS	Reserved [11:9]			PWR_DY-N_STATUS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [23:20]				OP_STATUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [31:25]							OP_DY-N_STATUS

Bits	Name	Description
24	OP_DYN_STATUS	Reserved Default Value: 0x0
19 : 16	OP_STATUS	Reserved Default Value: 0x0
12	LOCK_STATUS	Reserved Default Value: 0x0
8	PWR_DYN_STATUS	Power mode dynamic transition status. When set to 1 power mode dynamic transitions are enabled. There might be a delay in dynamic transitions becoming active or inactive if the PPU is transitioning when PWR_DYN_EN is programmed. Default Value: 0x0
3 : 0	PWR_STATUS	Power mode status. These bits reflect the current power mode of the PPU. See PPU_PWPR.PWR_POLICY for power mode enumeration. Default Value: 0x0

1.1.287 U550_MXU55_PPU_DISR

Description: Device Interface Input Current Status Register

Address: 0x44602010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PWR_DEVACTIVE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					R		
HW Access	Reserved					RW		
Name	Reserved [15:11]					PWR_DEVACTIVE_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	OP_DEVACTIVE_STATUS [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVE_STATUS	Reserved Default Value: 0x0
10 : 0	PWR_DEVACTIVE_STATUS	Status of the power mode DEVACTIVE inputs. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 0 is for Q-channel device 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0

1.1.288 U550_MXU55_PPU_MISR

Description: Miscellaneous Input Current Status Register

Address: 0x44602014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							PCSMPACCEPT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DEVACCEPT_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DEVDENY_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	DEVDENY_STATUS	Status of the device interface DEVDENY inputs. There is one bit for each device interface DEVQDENY. For example, bit 16 is for Q-Channel 0 DEVQDENY, and bit 17 for Q-Channel 1 DEVQDENY. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
15 : 8	DEVACCEPT_STATUS	Status of the device interface DEVACCEPT inputs. There is one bit for each device interface DEVQACCEPTn. For example, bit 8 is for Q-Channel 0 DEVQACCEPTn and bit 9 for Q-Channel 1 DEVQACCEPTn. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
0	PCSMPACCEPT_STATUS	The status of the PCSMPACCEPT input. Default Value: 0x0

1.1.289 U550_MXU55_PPU_STSR

Description: Stored Status Register

Address: 0x44602018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	STORED_DEVDENY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	STORED_DEVDENY	Reserved (this PPU has a single Q-channel) Default Value: 0x0

1.1.290 U550_MXU55_PPU_UNLK

Description: Unlock register

Address: 0x4460201C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							UNLOCK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	UNLOCK	Reserved Default Value: 0x0

1.1.291 U550_MXU55_PPU_PWCR

Description: Power Configuration Register

Address: 0x44602020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVREQEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PWR_DEVACTIVEEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_DEVACTIVEEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	OP_DEVACTIVEEN [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVEEN	Reserved Default Value: 0x0
18 : 8	PWR_DEVACTIVEEN	These bits enable the power mode DEVACTIVE inputs. When a bit is to 1 the related DEVACTIVE input is enabled, when set to 0 it is disabled. All available bits are reset to 1. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE, and bit 9 for the Q-Channel 1 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x007
7 : 0	DEVREQEN	When set to 1 enables the device interface handshake for transitions. All available bits are reset to 1. There is one bit for each device interface channel. For example, bit 0 is for Q-Channel 0, and bit 1 is for Q-Channel 1. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x07

1.1.292 U550_MXU55_PPU_PTCR

Description: Power Mode Transition Configuration Register

Address: 0x44602024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						DBG_RE-COV_POR ST_EN	WARM_RS T_DEVREQ EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	DBG_RE-COV_PORST_EN	Reserved Default Value: 0x0
0	WARM_RST_DEVREQEN	Transition behavior between ON and WARM_RST. This bit should not be modified when the PPU is in WARM_RST, or if the PPU is performing a transition, otherwise PPU behavior is UN-PREDICTABLE. 0: The PPU does not perform a device interface handshake when transitioning between ON and WARM_RST. 1: The PPU performs a device interface handshake when transitioning between ON and WARM_RST. This disables all Q-Channels for this transition. Default Value: 0x0

1.1.293 U550_MXU55_PPU_IMR

Description: Interrupt Mask Register

Address: 0x44602030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R	R	R	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		LOCKED_IRQ_MASK	EMU_DENY_IRQ_MASK	EMU_ACCEPT_IRQ_MASK	STA_DENY_IRQ_MASK	STA_ACCEPT_IRQ_MASK	STA_POLICY_TRN_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	LOCKED_IRQ_MASK	Reserved Default Value: 0x0
4	EMU_DENY_IRQ_MASK	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ_MASK	Reserved Default Value: 0x0
2	STA_DENY_IRQ_MASK	Static transition denial event mask. Default Value: 0x0
1	STA_ACCEPT_IRQ_MASK	Static transition acceptance event mask. Default Value: 0x1
0	STA_POLICY_TRN_IRQ_MASK	Static full policy transition completion event mask. Default Value: 0x0

1.1.294 U550_MXU55_PPU_AIMR

Description: Additional Interrupt Mask Register

Address: 0x44602034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R	R	RW	RW	RW
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ_MASK	STA_POLICY_PWR_IRQ_MASK	DYN_DENY_IRQ_MASK	DYN_ACCEPT_IRQ_MASK	UNSPT_POLICY_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ_MASK	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ_MASK	Reserved Default Value: 0x0
2	DYN_DENY_IRQ_MASK	Dynamic transition denial event mask. Default Value: 0x1
1	DYN_ACCEPT_IRQ_MASK	Dynamic transition acceptance event mask. Default Value: 0x1
0	UNSPT_POLICY_IRQ_MASK	Unsupported Policy event mask. Default Value: 0x0

1.1.295 U550_MXU55_PPU_ISR

Description: Interrupt Status Register

Address: 0x44602038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	Reserved	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	Reserved	R	R	R	R	R	R
Name	OTH-ER_IRQ	Reserved	LOCKED_IRQ	EMU_DE-NY_IRQ	EMU_AC-CEPT_IRQ	STA_DE-NY_IRQ	STA_AC-CEPT_IRQ	STA_POLI-CY_TRN_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	PWR_ACTIVE_EDGE_IRQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW1C		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_ACTIVE_EDGE_IRQ [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	OP_ACTIVE_EDGE_IRQ [31:24]							

Bits	Name	Description
31 : 24	OP_ACTIVE_EDGE_IRQ	Indicates which operating mode DEVPACTIVE inputs caused the input edge event. When operating modes are not supported this field is reserved. Default Value: 0x0
18 : 8	PWR_ACTIVE_EDGE_IRQ	Indicates which power mode DEVACTIVE inputs caused the input edge event. Bits for unused channels are the MSBs and are reserved. There is one bit for each device Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x00
7	OTHER_IRQ	Indicates there is an interrupt event pending in the Additional Interrupt Status Register (PPU_AISR). Default Value: 0x0
5	LOCKED_IRQ	Reserved Default Value: 0x0
4	EMU_DENY_IRQ	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ	Reserved Default Value: 0x0
2	STA_DENY_IRQ	Static transition denial event status. Default Value: 0x0
1	STA_ACCEPT_IRQ	Static transition acceptance event status. Default Value: 0x0

1.1.295 U550_MXU55_PPU_ISR (continued)

0	STA_POLICY_TRN_IRQ	Static full policy transition completion event status. Default Value: 0x0

1.1.296 U550_MXU55_PPU_AISR

Description: Additional Interrupt Status Register

Address: 0x4460203C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ	STA_POLICY_PWR_IRQ	DYN_DENY_IRQ	DYN_ACCEPT_IRQ	UNSPT_POLICY_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ	Reserved Default Value: 0x0
2	DYN_DENY_IRQ	Dynamic transition denial event status. Default Value: 0x0
1	DYN_ACCEPT_IRQ	Dynamic transition acceptance event status. Default Value: 0x0
0	UNSPT_POLICY_IRQ	Unsupported Policy event status. Default Value: 0x0

1.1.297 U550_MXU55_PPU_IESR

Description: Input Edge Sensitivity Register

Address: 0x44602040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE03_EDGE [7:6]		DEVACTIVE02_EDGE [5:4]		DEVACTIVE01_EDGE [3:2]		DEVACTIVE00_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE07_EDGE [15:14]		DEVACTIVE06_EDGE [13:12]		DEVACTIVE05_EDGE [11:10]		DEVACTIVE04_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		RW		RW	
HW Access	Reserved		R		R		R	
Name	Reserved [23:22]		DEVACTIVE10_EDGE [21:20]		DEVACTIVE09_EDGE [19:18]		DEVACTIVE08_EDGE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 20	DEVACTIVE10_EDGE	Reserved Default Value: 0x0
19 : 18	DEVACTIVE09_EDGE	Reserved Default Value: 0x0
17 : 16	DEVACTIVE08_EDGE	Reserved Default Value: 0x0
15 : 14	DEVACTIVE07_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE06_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE05_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE04_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE03_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE02_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE01_EDGE	Reserved Default Value: 0x0

1.1.297 U550_MXU55_PPU_IESR (continued)

1 : 0	DEVACTIVE00_EDGE	DEVACTIVE 0 edge sensitivity. Default Value: 0x0

1.1.298 U550_MXU55_PPU_OPSR

Description: Operating Mode Active Edge Sensitivity Register

Address: 0x44602044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE19_EDGE [7:6]		DEVACTIVE18_EDGE [5:4]		DEVACTIVE17_EDGE [3:2]		DEVACTIVE16_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE23_EDGE [15:14]		DEVACTIVE22_EDGE [13:12]		DEVACTIVE21_EDGE [11:10]		DEVACTIVE20_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	DEVACTIVE23_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE22_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE21_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE20_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE19_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE18_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE17_EDGE	Reserved Default Value: 0x0
1 : 0	DEVACTIVE16_EDGE	Reserved Default Value: 0x0

1.1.299 U550_MXU55_PPU_FUNRR

Description: Functional Retention RAM Configuration Register

Address: 0x44602050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FUNC_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FUNC_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.300 U550_MXU55_PPU_FULRR

Description: Full Retention RAM Configuration Register

Address: 0x44602054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FULL_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FULL_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.301 U550_MXU55_PPU_MEMRR

Description: Memory Retention RAM Configuration Register

Address: 0x44602058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	MEM_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.302 U550_MXU55_PPU_EDTR0

Description: Power Mode Entry Delay Register 0

Address: 0x44602160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOGIC_RET_DEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	FULL_RET_DEL [31:24]							

Bits	Name	Description
31 : 24	FULL_RET_DEL	Reserved Default Value: 0x00
23 : 16	LOGIC_RET_DEL	Reserved Default Value: 0x00
15 : 8	MEM_RET_DEL	Reserved Default Value: 0x00
7 : 0	OFF_DEL	Reserved Default Value: 0x00

1.1.303 U550_MXU55_PPU_EDTR1

Description: Power Mode Entry Delay Register 1

Address: 0x44602164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FUNC_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	FUNC_RET_DEL	Reserved Default Value: 0x00
7 : 0	MEM_OFF_DEL	Reserved Default Value: 0x00

1.1.304 U550_MXU55_PPU_DCDR0

Description: Device Control Delay Configuration Register 0

Address: 0x44602170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CLKEN_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ISO_CLKEN_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RST_HWSTAT_DLY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	RST_HWSTAT_DLY	Delay from clock enable assertion to reset de-assertion. Default Value: 0x1F
15 : 8	ISO_CLKEN_DLY	Reserved Default Value: 0x0
7 : 0	CLKEN_RST_DLY	Reserved Default Value: 0x0

1.1.305 U550_MXU55_PPU_DCDR1

Description: Device Control Delay Configuration Register 1

Address: 0x44602174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ISO_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CLKEN_ISO_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	CLKEN_ISO_DLY	Reserved Default Value: 0x0
7 : 0	ISO_RST_DLY	Reserved Default Value: 0x0

1.1.306 U550_MXU55_PPU_IDR0

Description: PPU Identification Register 0

Address: 0x44602FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	NUM_OPMODE [7:4]				DEVCHAN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	STA_-FUNC_RET_SPT	STA_-FULL_RET_SPT	STA_MEM_OFF_SPT	STA_LG-C_RET_SPT	STA_MEM_RET_EMU_SPT	STA_MEM_RET_SPT	STA_OFF_EMU_SPT	STA_OFF_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	Reserved	R	R	R
HW Access	RW	RW	RW	RW	Reserved	RW	RW	RW
Name	DY-N_MEM_RET_EMU_SPT	DY-N_MEM_RET_SPT	DY-N_OFF_EMU_SPT	DY-N_OFF_SPT	Reserved	STA_DB-G_RE-COV_SPT	STA_WRM_RST_SPT	STA_ON_SPT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [31:30]		DY-N_WRM_RST_SPT	DY-N_ON_SPT	DYN_-FUNC_RET_SPT	DYN_-FULL_RET_SPT	DY-N_MEM_OFF_SPT	DYN_LG-C_RET_SPT

Bits	Name	Description
29	DYN_WRM_RST_SPT	Dynamic WARM_RST support. Default Value: 0x0
28	DYN_ON_SPT	Dynamic ON support. Default Value: 0x1
27	DYN_FUNC_RET_SPT	Dynamic FUNC_RET support. Default Value: 0x0
26	DYN_FULL_RET_SPT	Dynamic FULL_RET support. Default Value: 0x0
25	DYN_MEM_OFF_SPT	Dynamic MEM_OFF support. Default Value: 0x0
24	DYN_LGC_RET_SPT	Dynamic LOGIC_RET support. Default Value: 0x0
23	DY-N_MEM_RET_EMU_SPT	Dynamic MEM_RET_EMU support Default Value: 0x0
22	DYN_MEM_RET_SPT	Dynamic MEM_RET support. Default Value: 0x0

1.1.306 U550_MXU55_PPU_IDR0 (continued)

21	DYN_OFF_EMU_SPT	Dynamic OFF_EMU support. Default Value: 0x0
20	DYN_OFF_SPT	Dynamic OFF support. Default Value: 0x1
18	STA_DBG_RECOV_SPT	DBG_RECOV support. Default Value: 0x0
17	STA_WRM_RST_SPT	WARM_RST support. Ignore this bit. Do not use WARM_RST. Default Value: 0x1
16	STA_ON_SPT	ON support. Default Value: 0x1
15	STA_FUNC_RET_SPT	FUNC_RET support. Default Value: 0x0
14	STA_FULL_RET_SPT	FULL_RET support. Default Value: 0x0
13	STA_MEM_OFF_SPT	MEM_OFF support. Default Value: 0x0
12	STA_LGC_RET_SPT	LOGIC_RET support. Default Value: 0x0
11	STA_MEM_RET_EMU_SPT	MEM_RET_EMU support. Default Value: 0x0
10	STA_MEM_RET_SPT	MEM_RET support. Default Value: 0x0
9	STA_OFF_EMU_SPT	OFF_EMU support. Default Value: 0x0
8	STA_OFF_SPT	OFF support. Default Value: 0x1
7 : 4	NUM_OPMODE	No. of operating modes supported is NUM_OPMODE + 1. Default Value: 0x0
3 : 0	DEVCHAN	No. of Device Interface Channels. The device enumeration is: Device 0: PDCM Device 1: U55 Device 2: U55 Sync-Down Bridge Default Value: 3

1.1.307 U550_MXU55_PPU_IDR1

Description: PPU Identification Register 1

Address: 0x44602FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	Reserved	R	R	R
HW Access	Reserved	RW	RW	RW	Reserved	RW	RW	RW
Name	Reserved	FUNC_RET_RAM_REG	FULL_RET_RAM_REG	MEM_RET_RAM_REG	Reserved	LOCK_SPT	SW_DEV_DEL_SPT	PWR_-MODE_EN-TRY_DEL_SPT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved	R	R	R
HW Access	Reserved			RW	Reserved	RW	RW	RW
Name	Reserved [15:13]			OFF_MEM_RET_TRANS	Reserved	OP_AC-TIVE	STA_POLI-CY_OP_IRQ_SPT	STA_POLI-CY_P-WR_IRQ_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	OFF_MEM_RET_TRANS	OFF to MEM_RET direct transition. Indicates if direct transitions from OFF to MEM_RET and from OFF_EMU to MEM_RET_EMU are supported. Default Value: 0x0
10	OP_ACTIVE	Reserved Default Value: 0x0
9	STA_POLI-CY_OP_IRQ_SPT	Operating policy transition completion event status. Default Value: 0x0
8	STA_POLICY_P-WR_IRQ_SPT	Power policy transition completion event status. Default Value: 0x0
6	FUNC_RET_RAM_REG	Indicates if the PPU_FUNRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
5	FULL_RET_RAM_REG	Indicates if the PPU_FULRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
4	MEM_RET_RAM_REG	Indicates if the PPU_MEMRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
2	LOCK_SPT	Lock and the lock interrupt event are supported. Default Value: 0x0

1.1.307 U550_MXU55_PPU_IDR1 (continued)

1	SW_DEV_DEL_SPT	Software device delay control configuration support. Default Value: 0x0
0	PWR_MODE_EN- TRY_DEL_SPT	Power mode entry delay support. Default Value: 0x0

1.1.308 U550_MXU55_PPU_IIDR

Description: Implementation Identification Register

Address: 0x44602FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IMPLEMENTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	REVISION [15:12]				IMPLEMENTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PRODUCT_ID [23:20]				VARIANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 20	PRODUCT_ID	PPU part identification. Default Value: 0x0B6
19 : 16	VARIANT	Major revision of the product. Default Value: 0x1
15 : 12	REVISION	Minor revision of the product. Default Value: 0
11 : 0	IMPLEMENTER	Implementer identification. [11:8] The JEP106 continuation code of the implementer. [7] Always 0. [6:0] The JEP106 identity code of the implementer. For an Arm implementation, bits [11:0] are 0x43B. Default Value: 0x43B

1.1.309 U550_MXU55_PPU_AIDR

Description: Architecture Identification Register

Address: 0x44602FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	ARCH_REV_MAJOR [7:4]				ARCH_REV_MINOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ARCH_REV_MAJOR	0x1 - PPU architecture major revision 1. Other Values - Reserved. Default Value: 0x1
3 : 0	ARCH_REV_MINOR	0x1 - PPU Architecture minor revision 1. Other Values - Reserved. Default Value: 0x1

1.1.310 U550_MXU55_PPU_PID4

Description: Implementation Defined Identification Register (PID4)

Address: 0x44602FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				IMPLEMENTER_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	IMPLEMENTER_11_8	The JEP106 continuation code of the implementer, which is 0x4 hardcoded value. Default Value: 0x4

1.1.311 U550_MXU55_PPU_PID0

Description: Implementation Defined Identification Register (PID0)

Address: 0x44602FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID_7_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PRODUCT_ID_7_0	PPU part identification bits [7:0]. Default Value: 0xB6

1.1.312 U550_MXU55_PPU_PID1

Description: Implementation Defined Identification Register (PID1)

Address: 0x44602FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	IMPLEMENTER_3_0 [7:4]				PRODUCT_ID_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	IMPLEMENTER_3_0	JEP106_ID bits [3:0] Default Value: 0xB
3 : 0	PRODUCT_ID_11_8	PPU part identification bits [11:8] Default Value: 0x0

1.1.313 U550_MXU55_PPU_PID2

Description: Implementation Defined Identification Register (PID2)

Address: 0x44602FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R	R		
HW Access	RW				RW	RW		
Name	REV [7:4]				JDEC	JEP106_ID_6_4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	REV	Revision identifier for the PCK-600 PPU: - 0x0 = r0p0. - 0x1 = r0p1, r0p2. Default Value: 0x1
3	JDEC	Indicates the use of a JEDEC-assigned ID value. Default Value: 0x1
2 : 0	JEP106_ID_6_4	JEDEC JEP106 ID code. See also PID1.JEP_ID[3:0] and the Standard Manufacturer's Identification Code. Default Value: 0x3

1.1.314 U550_MXU55_PPU_PID3

Description: Implementation Defined Identification Register (PID3)

Address: 0x44602FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PID3_REVISION [7:4]				PID3_REV_CONST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	PID3_REVISION	Minor revision of the product. Default Value: 0x0
3 : 0	PID3_REV_CONST	Constant LOW (4 bits) Default Value: 0x0

1.1.315 U550_MXU55_PPU_ID0

Description: Implementation Defined Identification Register (ID0)

Address: 0x44602FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID0	ID0 hard coded value Default Value: 0x0D

1.1.316 U550_MXU55_PPU_ID1

Description: Implementation Defined Identification Register (ID1)

Address: 0x44602FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID1	ID1 hardcoded value Default Value: 0xF0

1.1.317 U550_MXU55_PPU_ID2

Description: Implementation Defined Identification Register (ID2)

Address: 0x44602FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID2	ID2 hardcoded value Default Value: 0x05

1.1.318 U550_MXU55_PPU_ID3

Description: Implementation Defined Identification Register (ID3)

Address: 0x44602FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID3	ID3 hardcoded value Default Value: 0xB1

2 Inter Processor Communication (IPC) registers

This section discusses the IPC registers. It lists all the registers in mapping tables, in address order.

2.1 Register details

Register name	Address	Description
IPC0_STRUCT0_ACQUIRE	0x422A0000	IPC acquire
IPC0_STRUCT0_RELEASE	0x422A0004	IPC release
IPC0_STRUCT0_NOTIFY	0x422A0008	IPC notification
IPC0_STRUCT0_DATA0	0x422A000C	IPC data 0
IPC0_STRUCT0_DATA1	0x422A0010	IPC data 1
IPC0_STRUCT0_LOCK_STATUS	0x422A001C	IPC lock status
IPC0_STRUCT1_ACQUIRE	0x422A0020	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT1_RELEASE	0x422A0024	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT1_NOTIFY	0x422A0028	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT1_DATA0	0x422A002C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT1_DATA1	0x422A0030	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT1_LOCK_STATUS	0x422A003C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT2_ACQUIRE	0x422A0040	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT2_RELEASE	0x422A0044	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT2_NOTIFY	0x422A0048	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT2_DATA0	0x422A004C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT2_DATA1	0x422A0050	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT2_LOCK_STATUS	0x422A005C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT3_ACQUIRE	0x422A0060	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT3_RELEASE	0x422A0064	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT3_NOTIFY	0x422A0068	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC0_STRUCT3_DATA0	0x422A006C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT3_DATA1	0x422A0070	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT3_LOCK_STATUS	0x422A007C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT4_ACQUIRE	0x422A0080	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT4_RELEASE	0x422A0084	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT4_NOTIFY	0x422A0088	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT4_DATA0	0x422A008C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT4_DATA1	0x422A0090	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT4_LOCK_STATUS	0x422A009C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT5_ACQUIRE	0x422A00A0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT5_RELEASE	0x422A00A4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT5_NOTIFY	0x422A00A8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT5_DATA0	0x422A00AC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT5_DATA1	0x422A00B0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT5_LOCK_STATUS	0x422A00BC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT6_ACQUIRE	0x422A00C0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT6_RELEASE	0x422A00C4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT6_NOTIFY	0x422A00C8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT6_DATA0	0x422A00CC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT6_DATA1	0x422A00D0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT6_LOCK_STATUS	0x422A00DC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC0_STRUCT7_ACQUIRE	0x422A00E0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT7_RELEASE	0x422A00E4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT7_NOTIFY	0x422A00E8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT7_DATA0	0x422A00EC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT7_DATA1	0x422A00F0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT7_LOCK_STATUS	0x422A00FC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT8_ACQUIRE	0x422A0100	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT8_RELEASE	0x422A0104	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT8_NOTIFY	0x422A0108	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT8_DATA0	0x422A010C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT8_DATA1	0x422A0110	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT8_LOCK_STATUS	0x422A011C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT9_ACQUIRE	0x422A0120	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT9_RELEASE	0x422A0124	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT9_NOTIFY	0x422A0128	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT9_DATA0	0x422A012C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT9_DATA1	0x422A0130	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT9_LOCK_STATUS	0x422A013C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT10_ACQUIRE	0x422A0140	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT10_RELEASE	0x422A0144	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT10_NOTIFY	0x422A0148	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC0_STRUCT10_DATA0	0x422A014C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT10_DATA1	0x422A0150	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT10_LOCK_STATUS	0x422A015C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT11_ACQUIRE	0x422A0160	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT11_RELEASE	0x422A0164	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT11_NOTIFY	0x422A0168	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT11_DATA0	0x422A016C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT11_DATA1	0x422A0170	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT11_LOCK_STATUS	0x422A017C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT12_ACQUIRE	0x422A0180	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT12_RELEASE	0x422A0184	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT12_NOTIFY	0x422A0188	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT12_DATA0	0x422A018C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT12_DATA1	0x422A0190	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT12_LOCK_STATUS	0x422A019C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT13_ACQUIRE	0x422A01A0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT13_RELEASE	0x422A01A4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT13_NOTIFY	0x422A01A8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT13_DATA0	0x422A01AC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT13_DATA1	0x422A01B0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT13_LOCK_STATUS	0x422A01BC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC0_STRUCT14_ACQUIRE	0x422A01C0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT14_RELEASE	0x422A01C4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT14_NOTIFY	0x422A01C8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT14_DATA0	0x422A01CC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT14_DATA1	0x422A01D0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT14_LOCK_STATUS	0x422A01DC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_STRUCT15_ACQUIRE	0x422A01E0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC0_STRUCT15_RELEASE	0x422A01E4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC0_STRUCT15_NOTIFY	0x422A01E8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC0_STRUCT15_DATA0	0x422A01EC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC0_STRUCT15_DATA1	0x422A01F0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC0_STRUCT15_LOCK_STATUS	0x422A01FC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC0_INTR_STRUCT0_INTR	0x422A1000	Interrupt
IPC0_INTR_STRUCT0_INTR_SET	0x422A1004	Interrupt set
IPC0_INTR_STRUCT0_INTR_MASK	0x422A1008	Interrupt mask
IPC0_INTR_STRUCT0_INTR_MASKED	0x422A100C	Interrupt masked
IPC0_INTR_STRUCT1_INTR	0x422A1020	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC0_INTR_STRUCT1_INTR_SET	0x422A1024	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC0_INTR_STRUCT1_INTR_MASK	0x422A1028	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC0_INTR_STRUCT1_INTR_MASKED	0x422A102C	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC0_INTR_STRUCT2_INTR	0x422A1040	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC0_INTR_STRUCT2_INTR_SET	0x422A1044	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC0_INTR_STRUCT2_INTR_MASK	0x422A1048	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC0_INTR_STRUCT2_INTR_MASKED	0x422A104C	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC0_INTR_STRUCT3_INTR	0x422A1060	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC0_INTR_STRUCT3_INTR_SET	0x422A1064	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC0_INTR_STRUCT3_INTR_MASK	0x422A1068	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC0_INTR_STRUCT3_INTR_MASKED	0x422A106C	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC0_INTR_STRUCT4_INTR	0x422A1080	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC0_INTR_STRUCT4_INTR_SET	0x422A1084	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC0_INTR_STRUCT4_INTR_MASK	0x422A1088	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC0_INTR_STRUCT4_INTR_MASKED	0x422A108C	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC0_INTR_STRUCT5_INTR	0x422A10A0	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC0_INTR_STRUCT5_INTR_SET	0x422A10A4	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC0_INTR_STRUCT5_INTR_MASK	0x422A10A8	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC0_INTR_STRUCT5_INTR_MASKED	0x422A10AC	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC0_INTR_STRUCT6_INTR	0x422A10C0	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC0_INTR_STRUCT6_INTR_SET	0x422A10C4	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC0_INTR_STRUCT6_INTR_MASK	0x422A10C8	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC0_INTR_STRUCT6_INTR_MASKED	0x422A10CC	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC0_INTR_STRUCT7_INTR	0x422A10E0	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC0_INTR_STRUCT7_INTR_SET	0x422A10E4	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC0_INTR_STRUCT7_INTR_MASK	0x422A10E8	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC0_INTR_STRUCT7_INTR_MASKED	0x422A10EC	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC1_STRUCT0_ACQUIRE	0x441D0000	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT0_RELEASE	0x441D0004	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT0_NOTIFY	0x441D0008	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT0_DATA0	0x441D000C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT0_DATA1	0x441D0010	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT0_LOCK_STATUS	0x441D001C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT1_ACQUIRE	0x441D0020	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT1_RELEASE	0x441D0024	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT1_NOTIFY	0x441D0028	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT1_DATA0	0x441D002C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT1_DATA1	0x441D0030	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT1_LOCK_STATUS	0x441D003C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT2_ACQUIRE	0x441D0040	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT2_RELEASE	0x441D0044	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT2_NOTIFY	0x441D0048	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT2_DATA0	0x441D004C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT2_DATA1	0x441D0050	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT2_LOCK_STATUS	0x441D005C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC1_STRUCT3_ACQUIRE	0x441D0060	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT3_RELEASE	0x441D0064	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT3_NOTIFY	0x441D0068	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT3_DATA0	0x441D006C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT3_DATA1	0x441D0070	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT3_LOCK_STATUS	0x441D007C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT4_ACQUIRE	0x441D0080	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT4_RELEASE	0x441D0084	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT4_NOTIFY	0x441D0088	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT4_DATA0	0x441D008C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT4_DATA1	0x441D0090	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT4_LOCK_STATUS	0x441D009C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT5_ACQUIRE	0x441D00A0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT5_RELEASE	0x441D00A4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT5_NOTIFY	0x441D00A8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT5_DATA0	0x441D00AC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT5_DATA1	0x441D00B0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT5_LOCK_STATUS	0x441D00BC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT6_ACQUIRE	0x441D00C0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT6_RELEASE	0x441D00C4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT6_NOTIFY	0x441D00C8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC1_STRUCT6_DATA0	0x441D00CC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT6_DATA1	0x441D00D0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT6_LOCK_STATUS	0x441D00DC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT7_ACQUIRE	0x441D00E0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT7_RELEASE	0x441D00E4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT7_NOTIFY	0x441D00E8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT7_DATA0	0x441D00EC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT7_DATA1	0x441D00F0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT7_LOCK_STATUS	0x441D00FC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT8_ACQUIRE	0x441D0100	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT8_RELEASE	0x441D0104	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT8_NOTIFY	0x441D0108	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT8_DATA0	0x441D010C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT8_DATA1	0x441D0110	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT8_LOCK_STATUS	0x441D011C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT9_ACQUIRE	0x441D0120	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT9_RELEASE	0x441D0124	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT9_NOTIFY	0x441D0128	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT9_DATA0	0x441D012C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT9_DATA1	0x441D0130	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT9_LOCK_STATUS	0x441D013C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC1_STRUCT10_ACQUIRE	0x441D0140	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT10_RELEASE	0x441D0144	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT10_NOTIFY	0x441D0148	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT10_DATA0	0x441D014C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT10_DATA1	0x441D0150	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT10_LOCK_STATUS	0x441D015C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT11_ACQUIRE	0x441D0160	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT11_RELEASE	0x441D0164	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT11_NOTIFY	0x441D0168	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT11_DATA0	0x441D016C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT11_DATA1	0x441D0170	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT11_LOCK_STATUS	0x441D017C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT12_ACQUIRE	0x441D0180	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT12_RELEASE	0x441D0184	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT12_NOTIFY	0x441D0188	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT12_DATA0	0x441D018C	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT12_DATA1	0x441D0190	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT12_LOCK_STATUS	0x441D019C	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT13_ACQUIRE	0x441D01A0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT13_RELEASE	0x441D01A4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT13_NOTIFY	0x441D01A8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC1_STRUCT13_DATA0	0x441D01AC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT13_DATA1	0x441D01B0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT13_LOCK_STATUS	0x441D01BC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT14_ACQUIRE	0x441D01C0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT14_RELEASE	0x441D01C4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT14_NOTIFY	0x441D01C8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT14_DATA0	0x441D01CC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT14_DATA1	0x441D01D0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT14_LOCK_STATUS	0x441D01DC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_STRUCT15_ACQUIRE	0x441D01E0	IPC acquire. See IPC0_STRUCT0_ACQUIRE for the details of bit fields
IPC1_STRUCT15_RELEASE	0x441D01E4	IPC release. See IPC0_STRUCT0_RELEASE for the details of bit fields
IPC1_STRUCT15_NOTIFY	0x441D01E8	IPC notification. See IPC0_STRUCT0_NOTIFY for the details of bit fields
IPC1_STRUCT15_DATA0	0x441D01EC	IPC data 0. See IPC0_STRUCT0_DATA0 for the details of bit fields
IPC1_STRUCT15_DATA1	0x441D01F0	IPC data 1. See IPC0_STRUCT0_DATA1 for the details of bit fields
IPC1_STRUCT15_LOCK_STATUS	0x441D01FC	IPC lock status. See IPC0_STRUCT0_LOCK_STATUS for the details of bit fields
IPC1_INTR_STRUCT0_INTR	0x441D1000	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC1_INTR_STRUCT0_INTR_SET	0x441D1004	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC1_INTR_STRUCT0_INTR_MASK	0x441D1008	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC1_INTR_STRUCT0_INTR_MASKED	0x441D100C	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC1_INTR_STRUCT1_INTR	0x441D1020	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC1_INTR_STRUCT1_INTR_SET	0x441D1024	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC1_INTR_STRUCT1_INTR_MASK	0x441D1028	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC1_INTR_STRUCT1_INTR_MASKED	0x441D102C	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC1_INTR_STRUCT2_INTR	0x441D1040	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC1_INTR_STRUCT2_INTR_SET	0x441D1044	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC1_INTR_STRUCT2_INTR_MASK	0x441D1048	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC1_INTR_STRUCT2_INTR_MASKED	0x441D104C	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC1_INTR_STRUCT3_INTR	0x441D1060	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC1_INTR_STRUCT3_INTR_SET	0x441D1064	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC1_INTR_STRUCT3_INTR_MASK	0x441D1068	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC1_INTR_STRUCT3_INTR_MASKED	0x441D106C	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC1_INTR_STRUCT4_INTR	0x441D1080	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC1_INTR_STRUCT4_INTR_SET	0x441D1084	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC1_INTR_STRUCT4_INTR_MASK	0x441D1088	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC1_INTR_STRUCT4_INTR_MASKED	0x441D108C	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC1_INTR_STRUCT5_INTR	0x441D10A0	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC1_INTR_STRUCT5_INTR_SET	0x441D10A4	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC1_INTR_STRUCT5_INTR_MASK	0x441D10A8	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC1_INTR_STRUCT5_INTR_MASKED	0x441D10AC	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC1_INTR_STRUCT6_INTR	0x441D10C0	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields

Inter Processor Communication (IPC) registers

Register name	Address	Description
IPC1_INTR_STRUCT6_INTR_SET	0x441D10C4	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC1_INTR_STRUCT6_INTR_MASK	0x441D10C8	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC1_INTR_STRUCT6_INTR_MASKED	0x441D10CC	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields
IPC1_INTR_STRUCT7_INTR	0x441D10E0	Interrupt. See IPC0_INTR_STRUCT0_INTR for the details of bit fields
IPC1_INTR_STRUCT7_INTR_SET	0x441D10E4	Interrupt set. See IPC0_INTR_STRUCT0_INTR_SET for the details of bit fields
IPC1_INTR_STRUCT7_INTR_MASK	0x441D10E8	Interrupt mask. See IPC0_INTR_STRUCT0_INTR_MASK for the details of bit fields
IPC1_INTR_STRUCT7_INTR_MASKED	0x441D10EC	Interrupt masked. See IPC0_INTR_STRUCT0_INTR_MASKED for the details of bit fields

2.1.1 IPC0_STRUCT0_ACQUIRE

Description: IPC acquire

Address: 0x422A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved		R	R
HW Access	W				Reserved		W	W
Name	PC [7:4]				Reserved [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [15:14]		MS [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	SUCCESS	Reserved [30:24]						

Bits	Name	Description
31	SUCCESS	Specifies if the lock is successfully acquired or not (reading the ACQUIRE register can have affect on SUCCESS and LOCK_STATUS.ACQUIRED): '0': Not successfully acquired; i.e. the lock was already acquired by another read transaction and not released. The P, NS, PC and MS fields reflect the access attributes of the transaction that previously successfully acuired the lock; the fields are NOT affected by the current access. '1': Successfully acquired. The P, NS, PC and MS fields reflect the access attributes of the current access. Note that this field is NOT SW writable. A lock is released by writing to the associated RELEASE register (irrespective of the write value). Default Value: 0
13 : 8	MS	This field specifies the bus master identifier that successfully acquired the lock. Default Value: Undefined
7 : 4	PC	This field specifies the protection context that successfully acquired the lock. Default Value: Undefined
1	NS	Secure/non-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the access that successfully acquired the lock. Default Value: Undefined
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the access that successfully acquired the lock. Default Value: Undefined

2.1.2 IPC0_STRUCT0_RELEASE

Description: IPC release

Address: 0x422A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access								
Name	INTR_RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	INTR_RELEASE	Writing this field releases a lock and allows for the generation of release events to the IPC interrupt structures, but only when the lock is acquired (LOCK_STATUS.ACQUIRED is '1'). The IPC release cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_RELEASE[] is set to '1'. SW writes a '1' to the bit fields to generate a release event. Due to the transient nature of this event, SW always reads a '0' from this field. Default Value: 0

2.1.3 IPC0_STRUCT0_NOTIFY

Description: IPC notification

Address: 0x422A0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access								
Name	INTR_NOTIFY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	INTR_NOTIFY	This field allows for the generation of notification events to the IPC interrupt structures. The IPC notification cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_NOTIFY[] is set to '1'. SW writes a '1' to the bit fields to generate a notify event. Due to the transient nature of this event, SW always reads a '0' from this field. Default Value: 0

2.1.4 IPC0_STRUCT0_DATA0

Description: IPC data 0

Address: 0x422A000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This field holds a 32-bit data element that is associated with the IPC structure. Default Value: Undefined

2.1.5 IPC0_STRUCT0_DATA1

Description: IPC data 1

Address: 0x422A0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This field holds a 32-bit data element that is associated with the IPC structure. Default Value: Undefined

2.1.6 IPC0_STRUCT0_LOCK_STATUS

Description: IPC lock status

Address: 0x422A001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved		R	R
HW Access	W				Reserved		W	W
Name	PC [7:4]				Reserved [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	MS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	ACQUIRED	Reserved [30:24]						

Bits	Name	Description
31	ACQUIRED	Specifies if the lock is acquired. This field is set to '1', if a ACQUIRE read transfer successfully acquires the lock (the ACQUIRE read transfer returns ACQUIRE.SUCCESS as '1'). If zero, P, NS, PC, and MS are not valid. Default Value: 0
15 : 8	MS	This field specifies the bus master identifier that successfully acquired the lock. Default Value: Undefined
7 : 4	PC	This field specifies the protection context that successfully acquired the lock. Default Value: Undefined
1	NS	This field specifies the secure/non-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	This field specifies the user/privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

2.1.7 IPC0_INTR_STRUCT0_INTR

Description: Interrupt

Address: 0x422A1000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW1S							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW1S							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	These interrupt cause fields are activated (HW sets the field to '1') when a IPC notification event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. Default Value: 0
15 : 0	RELEASE	These interrupt cause fields are activated (HW sets the field to '1') when a IPC release event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. Default Value: 0

2.1.8 IPC0_INTR_STRUCT0_INTR_SET

Description: Interrupt set

Address: 0x422A1004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	A							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	A							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0
15 : 0	RELEASE	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

2.1.9 IPC0_INTR_STRUCT0_INTR_MASK

Description: Interrupt mask

Address: 0x422A1008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	Mask bit for corresponding field in the INTR register. Default Value: 0
15 : 0	RELEASE	Mask bit for corresponding field in the INTR register. Default Value: 0

2.1.10 IPC0_INTR_STRUCT0_INTR_MASKED

Description: Interrupt masked

Address: 0x422A100C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0
15 : 0	RELEASE	Logical and of corresponding request and mask bits. Default Value: 0

3 SRAM Controller registers

This section discusses the SRAM Controller registers. It lists all the registers in mapping tables, in address order.

3.1 Register details

Register name	Address	Description
RAMC0_CTL	0x42230000	Control
RAMC0_STATUS	0x42230008	Status
RAMC0_PWR_MACRO_CTL	0x42230200	SRAM power partition power control
RAMC0_PWR_MACRO_CTL_LOCK	0x42230240	SRAM power partition power control Lock
RAMC0_PWR_DELAY_CTL	0x42230280	SRAM power switch power up & sequence delay
RAMC0_MPC0_CFG	0x42234000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.
RAMC0_MPC0_CTRL	0x42234100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)
RAMC0_MPC0_BLK_MAX	0x42234104	Max value of block-based index register
RAMC0_MPC0_BLK_CFG	0x42234108	Block size & initialization in progress
RAMC0_MPC0_BLK_IDX	0x4223410C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)
RAMC0_MPC0_BLK_LUT	0x42234110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>
RAMC0_MPC0_ROT_CTRL	0x42234200	Control register with lock bit and auto-increment only
RAMC0_MPC0_ROT_BLK_MAX	0x42234208	Max value of block-based index register for ROT
RAMC0_MPC0_ROT_BLK_CFG	0x4223420C	Same as BLK_CFG
RAMC0_MPC0_ROT_BLK_IDX	0x42234210	Index of 8-block group accessed through ROT_BLK_LUT_*
RAMC0_MPC0_ROT_BLK_PC	0x42234214	Protection context of 8-block group accesses through ROT_BLK_LUT
RAMC0_MPC0_ROT_BLK_LUT	0x42234218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC
RAMC1_CTL	0x42240000	Control. See RAMC0_CTL for the details of bit fields.
RAMC1_STATUS	0x42240008	Status. See RAMC0_STATUS for the details of bit fields.
RAMC1_PWR_MACRO_CTL	0x42240200	SRAM power partition power control. See RAMC0_PWR_MACRO_CTL for the details of bit fields.
RAMC1_PWR_MACRO_CTL_LOCK	0x42240240	SRAM power partition power control Lock. See RAMC0_PWR_MACRO_CTL_LOCK for the details of bit fields.
RAMC1_PWR_DELAY_CTL	0x42240280	SRAM power switch power up & sequence delay. See RAMC0_PWR_DELAY_CTL for the details of bit fields.

SRAM Controller registers

Register name	Address	Description
RAMC1_MPC0_CFG	0x42244000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.. See RAMC0_MPC0_CFG for the details of bit fields.
RAMC1_MPC0_CTRL	0x42244100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc). See RAMC0_MPC0_CTRL for the details of bit fields.
RAMC1_MPC0_BLK_MAX	0x42244104	Max value of block-based index register. See RAMC0_MPC0_BLK_MAX for the details of bit fields.
RAMC1_MPC0_BLK_CFG	0x42244108	Block size & initialization in progress. See RAMC0_MPC0_BLK_CFG for the details of bit fields.
RAMC1_MPC0_BLK_IDX	0x4224410C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc). See RAMC0_MPC0_BLK_IDX for the details of bit fields.
RAMC1_MPC0_BLK_LUT	0x42244110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>. See RAMC0_MPC0_BLK_LUT for the details of bit fields.
RAMC1_MPC0_ROT_CTRL	0x42244200	Control register with lock bit and auto-increment only. See RAMC0_MPC0_ROT_CTRL for the details of bit fields.
RAMC1_MPC0_ROT_BLK_MAX	0x42244208	Max value of block-based index register for ROT. See RAMC0_MPC0_ROT_BLK_MAX for the details of bit fields.
RAMC1_MPC0_ROT_BLK_CFG	0x4224420C	Same as BLK_CFG. See RAMC0_MPC0_ROT_BLK_CFG for the details of bit fields.
RAMC1_MPC0_ROT_BLK_IDX	0x42244210	Index of 8-block group accessed through ROT_BLK_LUT_*. See RAMC0_MPC0_ROT_BLK_IDX for the details of bit fields.
RAMC1_MPC0_ROT_BLK_PC	0x42244214	Protection context of 8-block group accesses through ROT_BLK_LUT. See RAMC0_MPC0_ROT_BLK_PC for the details of bit fields.
RAMC1_MPC0_ROT_BLK_LUT	0x42244218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC. See RAMC0_MPC0_ROT_BLK_LUT for the details of bit fields.

3.1.1 RAMC0_CTL

Description: Control

Address: 0x42230000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						SRAM_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							CLOCK_-FORCE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	CLOCK_FORCE	Force EAM clock gating to be always ON. 0: Disabled 1: Enabled This bit provides fail safe mechanism for dynamic clock gating added on EAM block. Default Value: 0
1 : 0	SRAM_WS	Wait states. Default Value: 0 **0x0: WS_0 :** **0x1: WS_1 :** **0x2: WS_2 :** **0x3: WS_3 :**

3.1.2 RAMC0_STATUS

Description: Status

Address: 0x42230008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R	Reserved			
HW Access	Reserved			W	Reserved			
Name	Reserved [7:5]			PWR_-DONE	Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	PWR_DONE	After a PWR_MACRO_CTL.OFF change this flag indicates if the new power mode has taken effect or not. 1: Indicates change is effective; 0: Indicates change is in progress; Default Value: 1

3.1.3 RAMC0_PWR_MACRO_CTL

Description: SRAM power partition power control

Address: 0x42230200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	OFF	Each bit represent the individual RAM power partition power state. One bit for each macro of RAM controller when all 32 bits are populated as 32 independent power partitions. 0: Macros in power partion is to be powered-ON 1: Macros in power partion is to be powered-OFF Note 1: it is not allowed to disable a macro during access to its address range. Note 2: it is not allowed to disable few macros while enable others in the same AHB write transaction. It is mandatory to check for STATUS.PWR_DONE to become 1 once this PWR_MACRO_DTL register contents are changed to ensure SRAM mode transition is completed successfully. Default Value: 0

3.1.4 RAMC0_PWR_MACRO_CTL_LOCK

Description: SRAM power partition power control Lock

Address: 0x42230240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						A	
Name	Reserved [7:2]						PWR_MACRO_CT-L_LOCK [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	PWR_MACRO_CT-L_LOCK	Prohibits Read/Write access to PWR_MACRO_CTL register when this field is not equal to 0. Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. By default AHB reads/writes to PWR_MACRO_CTL register are locked. Default Value: 3 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0 **0x2: CLR1 :** Clears bit 1 **0x3: SET01 :** Sets both bits 0 and 1

3.1.5 RAMC0_PWR_DELAY_CTL

Description: SRAM power switch power up & sequence delay

Address: 0x42230280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SEQ0_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SEQ1_DELAY [31:24]							

Bits	Name	Description
31 : 24	SEQ1_DELAY	Number of IMO clock cycles delay needed for sequence-1 of SRAM power transition Default Value: 0x9
23 : 16	SEQ0_DELAY	Number of IMO clock cycles delay needed for sequence-0 of SRAM power transition Default Value: 0x2
9 : 0	UP	Number of IMO clock cycles delay needed after power domain power up Default Value: 0x9

3.1.6 RAMC0_MPC0_CFG

Description: Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.

Address: 0x42234000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			
HW Access	Reserved			R	Reserved			
Name	Reserved [7:5]			RE-SPONSE	Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	RESPONSE	Response Configuration for Security and PC violations 0: Read-Zero Write Ignore (RAZ/WI) 1: Bus Error Default Value: 0

3.1.7 RAMC0_MPC0_CTRL

Description: Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)

Address: 0x42234100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	Reserved						
HW Access	R	Reserved						
Name	LOCK	Reserved [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for this protection context. Software can set this bit but not clear it once set. When set, write operations to BLK_LUT are not possible from this protection context. Setting LOCK also blocks writes to CTRL itself (for that PC copy). All writes are ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for this protection context as a side effect of each read/write access to BLK_LUT Default Value: 1

3.1.8 RAMC0_MPC0_BLK_MAX

Description: Max value of block-based index register

Address: 0x42234104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	
HW Access	Reserved						R	
Name	Reserved [7:2]						VALUE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; See product datasheet for details on protection of external memories. Default Value: 3

3.1.9 RAMC0_MPC0_BLK_CFG

Description: Block size & initialization in progress

Address: 0x42234108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	INIT_IN_PROGRESS	Reserved [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to BLK_LUT is blocked (BLK_IDX increment is also ignored). The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ... up to 15: 1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 7

3.1.10 RAMC0_MPC0_BLK_IDX

Description: Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)

Address: 0x4223410C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						RW	
Name	Reserved [7:2]						VALUE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	VALUE	Index value for accessing block-based lookup table using BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

3.1.11 RAMC0_MPC0_BLK_LUT

Description: NS status for 32 blocks at BLK_IDX with PC=_pc>

Address: 0x42234110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS7	ATTR_NS6	ATTR_NS5	ATTR_NS4	ATTR_NS3	ATTR_NS2	ATTR_NS1	ATTR_NS0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	AT-TR_NS15	AT-TR_NS14	AT-TR_NS13	AT-TR_NS12	ATTR_NS11	AT-TR_NS10	ATTR_NS9	ATTR_NS8

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	AT-TR_NS23	AT-TR_NS22	AT-TR_NS21	AT-TR_NS20	AT-TR_NS19	AT-TR_NS18	AT-TR_NS17	AT-TR_NS16

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	AT-TR_NS31	AT-TR_NS30	AT-TR_NS29	AT-TR_NS28	AT-TR_NS27	AT-TR_NS26	AT-TR_NS25	AT-TR_NS24

Bits	Name	Description
31	ATTR_NS31	NS bit for block 31 based on BLK_IDX Default Value: 0
30	ATTR_NS30	NS bit for block 30 based on BLK_IDX Default Value: 0
29	ATTR_NS29	NS bit for block 29 based on BLK_IDX Default Value: 0
28	ATTR_NS28	NS bit for block 28 based on BLK_IDX Default Value: 0
27	ATTR_NS27	NS bit for block 27 based on BLK_IDX Default Value: 0
26	ATTR_NS26	NS bit for block 26 based on BLK_IDX Default Value: 0
25	ATTR_NS25	NS bit for block 25 based on BLK_IDX Default Value: 0
24	ATTR_NS24	NS bit for block 24 based on BLK_IDX Default Value: 0
23	ATTR_NS23	NS bit for block 23 based on BLK_IDX Default Value: 0
22	ATTR_NS22	NS bit for block 22 based on BLK_IDX Default Value: 0

3.1.11 RAMC0_MPC0_BLK_LUT (continued)

21	ATTR_NS21	NS bit for block 21 based on BLK_IDX Default Value: 0
20	ATTR_NS20	NS bit for block 20 based on BLK_IDX Default Value: 0
19	ATTR_NS19	NS bit for block 19 based on BLK_IDX Default Value: 0
18	ATTR_NS18	NS bit for block 18 based on BLK_IDX Default Value: 0
17	ATTR_NS17	NS bit for block 17 based on BLK_IDX Default Value: 0
16	ATTR_NS16	NS bit for block 16 based on BLK_IDX Default Value: 0
15	ATTR_NS15	NS bit for block 15 based on BLK_IDX Default Value: 0
14	ATTR_NS14	NS bit for block 14 based on BLK_IDX Default Value: 0
13	ATTR_NS13	NS bit for block 13 based on BLK_IDX Default Value: 0
12	ATTR_NS12	NS bit for block 12 based on BLK_IDX Default Value: 0
11	ATTR_NS11	NS bit for block 11 based on BLK_IDX Default Value: 0
10	ATTR_NS10	NS bit for block 10 based on BLK_IDX Default Value: 0
9	ATTR_NS9	NS bit for block 9 based on BLK_IDX Default Value: 0
8	ATTR_NS8	NS bit for block 8 based on BLK_IDX Default Value: 0
7	ATTR_NS7	NS bit for block 7 based on BLK_IDX Default Value: 0
6	ATTR_NS6	NS bit for block 6 based on BLK_IDX Default Value: 0
5	ATTR_NS5	NS bit for block 5 based on BLK_IDX Default Value: 0
4	ATTR_NS4	NS bit for block 4 based on BLK_IDX Default Value: 0
3	ATTR_NS3	NS bit for block 3 based on BLK_IDX Default Value: 0
2	ATTR_NS2	NS bit for block 2 based on BLK_IDX Default Value: 0
1	ATTR_NS1	NS bit for block 1 based on BLK_IDX Default Value: 0
0	ATTR_NS0	NS bit for block 0 based on BLK_IDX Default Value: 0

3.1.12 RAMC0_MPC0_ROT_CTRL

Description: Control register with lock bit and auto-increment only

Address: 0x42234200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	Reserved						
HW Access	R	Reserved						
Name	LOCK	Reserved [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for the root-of-trust configuration registers. Software can set this bit but not clear it once set. When set, write operations to ROT_BLK_LUT are not possible. Write is ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for each read/write of ROT_BLK_LUT Default Value: 1

3.1.13 RAMC0_MPC0_ROT_BLK_MAX

Description: Max value of block-based index register for ROT

Address: 0x42234208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				VALUE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 15

3.1.14 RAMC0_MPC0_ROT_BLK_CFG

Description: Same as BLK_CFG

Address: 0x4223420C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	INIT_IN_PROGRESS	Reserved [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to ROT_BLK_LUT is RAZWI. The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ...up to 15:1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 7

3.1.15 RAMC0_MPC0_ROT_BLK_IDX

Description: Index of 8-block group accessed through ROT_BLK_LUT_*

Address: 0x42234210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				RW			
Name	Reserved [7:4]				VALUE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	VALUE	Index value for accessing block-based lookup table using ROT_BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

3.1.16 RAMC0_MPC0_ROT_BLK_PC

Description: Protection context of 8-block group accesses through ROT_BLK_LUT

Address: 0x42234214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	PC	Specify PC values for ROT_BLK_IDX and ROT_BLK_LUT Default Value: 0

3.1.17 RAMC0_MPC0_ROT_BLK_LUT

Description: (R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC

Address: 0x42234218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR1 [6:4]			Reserved	ATTR0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR3 [14:12]			Reserved	ATTR2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR5 [22:20]			Reserved	ATTR4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR7 [30:28]			Reserved	ATTR6 [26:24]		

Bits	Name	Description
30 : 28	ATTR7	W/R/NS bits for block 7 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
26 : 24	ATTR6	W/R/NS bits for block 6 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
22 : 20	ATTR5	W/R/NS bits for block 5 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
18 : 16	ATTR4	W/R/NS bits for block 4 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
14 : 12	ATTR3	W/R/NS bits for block 3 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
10 : 8	ATTR2	W/R/NS bits for block 2 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
6 : 4	ATTR1	W/R/NS bits for block 1 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
2 : 0	ATTR0	W/R/NS bits for block 0 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0

4 System-on-Chip Memory (SoCMEM) registers

This section discusses the SoCMEM registers. It lists all the registers in mapping tables, in address order.

4.1 Register details

Register name	Address	Description
SOCMEM_CTL	0x44640000	Control
SOCMEM_STATUS	0x44640004	Status
SOCMEM_GK_CTL	0x44640008	Gate keeper control
SOCMEM_GK_STATUS	0x4464000C	Gate keeper status
SOCMEM_ARB_DYN_CTL0	0x44640010	Port arbitration control
SOCMEM_ARB_DYN_CTL1	0x44640014	Port arbitration control. See SOCMEM_ARB_DYN_CTL0 for the details of bit fields.
SOCMEM_ARB_DYN_CTL2	0x44640018	Port arbitration control. See SOCMEM_ARB_DYN_CTL0 for the details of bit fields.
SOCMEM_ARB_DYN_CTL3	0x4464001C	Port arbitration control. See SOCMEM_ARB_DYN_CTL0 for the details of bit fields.
SOCMEM_ARB_DYN_CTL4	0x44640020	Port arbitration control. See SOCMEM_ARB_DYN_CTL0 for the details of bit fields.
SOCMEM_MPC_READ_PORT_CTL	0x44640060	MPC MMIO read port index control
SOCMEM_WOUNDING	0x44640110	Wounding
SOCMEM_PWR_PARTITION_CTL0	0x44640200	SRAM partition power control
SOCMEM_PWR_PARTITION_CTL1	0x44640204	SRAM partition power control. See SOCMEM_PWR_PARTITION_CTL0 for the details of bit fields.
SOCMEM_PWR_PARTITION_CTL2	0x44640208	SRAM partition power control. See SOCMEM_PWR_PARTITION_CTL0 for the details of bit fields.
SOCMEM_PWR_PARTITION_CTL3	0x4464020C	SRAM partition power control. See SOCMEM_PWR_PARTITION_CTL0 for the details of bit fields.
SOCMEM_PWR_PARTITION_CTL4	0x44640210	SRAM partition power control. See SOCMEM_PWR_PARTITION_CTL0 for the details of bit fields.
SOCMEM_PWR_PARTITION_CTL5	0x44640214	SRAM partition power control. See SOCMEM_PWR_PARTITION_CTL0 for the details of bit fields.

System-on-Chip Memory (SoCMEM) registers

Register name	Address	Description
SOCMEM_PWR_PARTITION_CTL6	0x44640218	SRAM partition power control. See SOCMEM_PWR_PARTITION_CTL0 for the details of bit fields.
SOCMEM_PWR_PARTITION_CTL7	0x4464021C	SRAM partition power control. See SOCMEM_PWR_PARTITION_CTL0 for the details of bit fields.
SOCMEM_PWR_PARTITION_CTL8	0x44640220	SRAM partition power control. See SOCMEM_PWR_PARTITION_CTL0 for the details of bit fields.
SOCMEM_PWR_PARTITION_CTL9	0x44640224	SRAM partition power control. See SOCMEM_PWR_PARTITION_CTL0 for the details of bit fields.
SOCMEM_PWR_PARTITION_CTL_LOCK	0x44640280	SRAM power partition control Lock
SOCMEM_PWR_DELAY_CTL	0x44640284	SRAM power switch power up & sequence delay
SOCMEM_PWR_STATUS	0x44640288	SRAM power status
SOCMEM_SRAM_MPC0_CFG	0x44642000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.
SOCMEM_SRAM_MPC0_CTRL	0x44642100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)
SOCMEM_SRAM_MPC0_BLK_MAX	0x44642104	Max value of block-based index register
SOCMEM_SRAM_MPC0_BLK_CFG	0x44642108	Block size & initialization in progress
SOCMEM_SRAM_MPC0_BLK_IDX	0x4464210C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)
SOCMEM_SRAM_MPC0_BLK_LUT	0x44642110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>
SOCMEM_SRAM_MPC0_ROT_CTRL	0x44642200	Control register with lock bit and auto-increment only
SOCMEM_SRAM_MPC0_ROT_BLK_MAX	0x44642208	Max value of block-based index register for ROT
SOCMEM_SRAM_MPC0_ROT_BLK_CFG	0x4464220C	Same as BLK_CFG
SOCMEM_SRAM_MPC0_ROT_BLK_IDX	0x44642210	Index of 8-block group accessed through ROT_BLK_LUT_*
SOCMEM_SRAM_MPC0_ROT_BLK_PC	0x44642214	Protection context of 8-block group accesses through ROT_BLK_LUT
SOCMEM_SRAM_MPC0_ROT_BLK_LUT	0x44642218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC
SOCMEM_PATCH_STRUCT_CTL00	0x44650800	Patch structure control
SOCMEM_PATCH_STRUCT_CTL10	0x44651800	Patch structure control. See SOCMEM_PATCH_STRUCT_CTL00 for the details of bit fields.

System-on-Chip Memory (SoCMEM) registers

Register name	Address	Description
SOCMEM_PATCH_STRUCT_CTL20	0x44652800	Patch structure control. See SOCMEM_PATCH_STRUCT_CTL00 for the details of bit fields.
SOCMEM_PATCH_STRUCT_CTL30	0x44653800	Patch structure control. See SOCMEM_PATCH_STRUCT_CTL00 for the details of bit fields.
SOCMEM_PATCH_STRUCT_CTL40	0x44654800	Patch structure control. See SOCMEM_PATCH_STRUCT_CTL00 for the details of bit fields.
SOCMEM_PPU_SOCMEM_PWPR	0x44660000	Power Policy Register
SOCMEM_PPU_SOCMEM_PMER	0x44660004	Power Mode Emulation Register
SOCMEM_PPU_SOCMEM_PWSR	0x44660008	Power Status Register
SOCMEM_PPU_SOCMEM_DISR	0x44660010	Device Interface Input Current Status Register
SOCMEM_PPU_SOCMEM_MISR	0x44660014	Miscellaneous Input Current Status Register
SOCMEM_PPU_SOCMEM_STSR	0x44660018	Stored Status Register
SOCMEM_PPU_SOCMEM_UNLK	0x4466001C	Unlock register
SOCMEM_PPU_SOCMEM_PWCR	0x44660020	Power Configuration Register
SOCMEM_PPU_SOCMEM_PTCR	0x44660024	Power Mode Transition Configuration Register
SOCMEM_PPU_SOCMEM_IMR	0x44660030	Interrupt Mask Register
SOCMEM_PPU_SOCMEM_AIMR	0x44660034	Additional Interrupt Mask Register
SOCMEM_PPU_SOCMEM_ISR	0x44660038	Interrupt Status Register
SOCMEM_PPU_SOCMEM_AISR	0x4466003C	Additional Interrupt Status Register
SOCMEM_PPU_SOCMEM_IESR	0x44660040	Input Edge Sensitivity Register
SOCMEM_PPU_SOCMEM_OPSR	0x44660044	Operating Mode Active Edge Sensitivity Register
SOCMEM_PPU_SOCMEM_FUNRR	0x44660050	Functional Retention RAM Configuration Register
SOCMEM_PPU_SOCMEM_FULRR	0x44660054	Full Retention RAM Configuration Register
SOCMEM_PPU_SOCMEM_MEMRR	0x44660058	Memory Retention RAM Configuration Register
SOCMEM_PPU_SOCMEM_EDTR0	0x44660160	Power Mode Entry Delay Register 0
SOCMEM_PPU_SOCMEM_EDTR1	0x44660164	Power Mode Entry Delay Register 1
SOCMEM_PPU_SOCMEM_DCDR0	0x44660170	Device Control Delay Configuration Register 0
SOCMEM_PPU_SOCMEM_DCDR1	0x44660174	Device Control Delay Configuration Register 1
SOCMEM_PPU_SOCMEM_IDR0	0x44660FB0	PPU Identification Register 0
SOCMEM_PPU_SOCMEM_IDR1	0x44660FB4	PPU Identification Register 1
SOCMEM_PPU_SOCMEM_IIDR	0x44660FC8	Implementation Identification Register
SOCMEM_PPU_SOCMEM_AIDR	0x44660FCC	Architecture Identification Register
SOCMEM_PPU_SOCMEM_PID4	0x44660FD0	Implementation Defined Identification Register (PID4)
SOCMEM_PPU_SOCMEM_PID0	0x44660FE0	Implementation Defined Identification Register (PID0)

System-on-Chip Memory (SoCMEM) registers

Register name	Address	Description
SOCMEM_PPU_SOCMEM_PID1	0x44660FE4	Implementation Defined Identification Register (PID1)
SOCMEM_PPU_SOCMEM_PID2	0x44660FE8	Implementation Defined Identification Register (PID2)
SOCMEM_PPU_SOCMEM_PID3	0x44660FEC	Implementation Defined Identification Register (PID3)
SOCMEM_PPU_SOCMEM_ID0	0x44660FF0	Implementation Defined Identification Register (ID0)
SOCMEM_PPU_SOCMEM_ID1	0x44660FF4	Implementation Defined Identification Register (ID1)
SOCMEM_PPU_SOCMEM_ID2	0x44660FF8	Implementation Defined Identification Register (ID2)
SOCMEM_PPU_SOCMEM_ID3	0x44660FFC	Implementation Defined Identification Register (ID3)
SOCMEM_SOCMEM_PD_CTL	0x44661000	Power Domain Control
SOCMEM_SOCMEM_PD_PWR_UP_DELAY	0x44661004	Active switch weak enable to active switch strong enable delay

4.1.1 SOCMEM_CTL

Description: Control

Address: 0x44640000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW		Reserved		RW	
HW Access	Reserved		R		Reserved		R	
Name	Reserved [7:6]		SROM_WS [5:4]		Reserved [3:2]		SRAM_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							AUTO_GK

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	AUTO_GK	Automatic gate keeper control: '0': Disabled. '1': Enabled. Before every MMIO register write, ALL ports are automatically closed. After the MMIO register write, the gate keeper control defaults to GK_CTL.OPEN. Default Value: 1
5 : 4	SROM_WS	Wait states. Default Value: 3 **0x0: WS_0 :** **0x1: WS_1 :** **0x2: WS_2 :** **0x3: WS_3 :**
1 : 0	SRAM_WS	Wait states. Default Value: 3 **0x0: WS_0 :** **0x1: WS_1 :** **0x2: WS_2 :**

4.1.1 SOCMEM_CTL (continued)

0x3: WS_3 :

4.1.2 SOCMEM_STATUS

Description: Status

Address: 0x44640004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				WB_EMPTY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [23:17]							PORT_MP-C_INIT_-DONE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	PORT_MPC_INIT_DONE	Port MPC SRAM initialisation done. It is a combined single initialisation done for all the ports mpc sram. Default Value: 0
3 : 0	WB_EMPTY	Write buffer empty. This information is used when entering DEEPSLEEP or DEEPSLEEP_RAM system power modes: WB_EMPTY must be '1' before a transition to DEEPSLEEP or DEEPSLEEP_RAM system power modes. '0': Write buffer NOT empty. '1': Write buffer empty. Note: the SoCMEM controller write buffer is only used when ECC checking is enabled. (ECC_CTL.EN is '1'). Default Value: Undefined

4.1.3 SOCMEM_GK_CTL

Description: Gate keeper control

Address: 0x44640008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			OPEN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	OPEN	Port gate keeper control: '0': Close port request. Finishes ongoing AMBA transactions, but does not accept new AMBA transactions. '1': Open port request. Note: GK_CTL allows for the creation of atomic sequences (from the perspective of AMBA transactions) of MMIO register writes. Note: gate keeper control is used to change MMIO register settings in an active system (per TZC400). Default Value: 0

4.1.4 SOCMEM_GK_STATUS

Description: Gate keeper status

Address: 0x4464000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [7:5]			OPEN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	OPEN	Port gate keeper status '0': Port is closed. A port may be closed under SW MMIO control (GK_CTL) or under HW system control '1': Port is open. Note: gate keeper control is used to change MMIO register settings in an active system (per TZC400). Default Value: 0

4.1.5 SOCMEM_ARB_DYN_CTL0

Description: Port arbitration control

Address: 0x44640010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	CREDIT [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							LATENCY

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	LATENCY	Specifies if the port is latency sensitive. '0': Non latency sensitive or less latency sensitive (e.g. a DMA controller). '1': Latency sensitive (e.g. a CPU or a real-time master such as a sound or display controller). As described above, the scheduler favors latency sensitive masters over non latency sensitive masters. Default Value: 0

4.1.5 SOCMEM_ARB_DYN_CTL0 (continued)

6 : 0	CREDIT	Port account increment. Value in the range [0, 127]. Total available SRAM/SROM bank bandwidth is partitioned into 128 partitions. The CREDIT value specifies what guaranteed relative bandwidth is assigned to the port. E.g., when CREDIT is "32", 25% of the relative bandwidth is assigned to the port. Note that for absolute bandwidth, the SRAM/SROM frequency and wait states need to be taken into account as well. An arbiter/scheduler operation is performed when one or more port requests for a SRAM/SROM bank are present and the SRAM/SROM bank is available for a new request. Each SRAM/SROM bank has a dedicated scheduler. The scheduler uses port account values: 9-bit values in the range [0, 511]. The port account values identify: - Non credit-worthy ports (account value in the range [0, 255]). - Credit-worthy ports (account value in the range [256, 511]). In addition, each port is specified to be either non (less) latency sensitive or latency sensitive (LATENCY). A scheduler operation is defined as follows: IF ("Any requesting port is a credit-worthy, latency port") "Select port with lowest index from requesting, credit-worthy, latency ports" ELSE IF ("Any requesting port is a credit-worthy, non latency port") "Select port with lowest index from requesting, credit-worthy, non latency ports" ELSE IF ("Any requesting port is a non credit-worthy, latency port") "Select port with lowest index from requesting, non credit-worthy, latency ports" ELSE IF ("Any requesting port is a non credit-worthy, non latency port") "Select port with lowest index from requesting, non credit-worthy, non latency ports" After a scheduler operation, account values are updated: - The selected port's account is incremented by CREDIT and decremented with "128". If ECC is enabled AND the transaction was a partial write, an additional "128" is decremented, because two transactions (read-modify-write) are needed to change the ECC. Clipping to "0" is performed to prevent negative values. - Non-selected port account are increment by CREDIT, if the current account value is less than "256". Otherwise, the port account value is not updated. Default Value: 0

4.1.6 SOCMEM_MPC_READ_PORT_CTL

Description: MPC MMIO read port index control

Address: 0x44640060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				INDEX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	INDEX	specifies port index for any MPC read access using SOCMEM.SRAM_MPC/SROM_MPC. 0- Any SW MPC MMIO read through SOCMEM.SRAM/SROM_MPC is from port-0. 1- Any SW MPC MMIO read through SOCMEM.SRAM/SROM_MPC is from port-1. . . 15- Any SW MPC MMIO read through SOCMEM.SRAM/SROM_MPC is from port-15. Note that INDEX field value programmed by SW must be between 0 and one less than number of configured SOCMEM ports (number of ports is design time config option using parameter PORT_NR). IMPORTANT: When MPC.CTRL.AUTO_INC is 1, each read access will auto-increment MPC.BLK_IDX in the port specified by MPC_READ_PORT_CTL.INDEX; not all ports are updated. Each write access will auto-increment MPC.BLK_IDX.VALUE in all ports. When MPC.CTRL.AUTO_INC is 1, to ensure that all ports are initialized correctly, write to MPC.BLK_IDX.VALUE before any series of writes to MPC.BLK_LUT. Writing to MPC.BLK_IDX.VALUE sets the index in all ports to the same value. Default Value: 0

4.1.7 SOCMEM_WOUNDING

Description: Wounding

Address: 0x44640110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1S		
HW Access	Reserved					R		
Name	Reserved [7:3]					WOUND [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	WOUND	Indicates the amount of accessible SRAM in this device. The value in this field is effectively write-once (it is only possible to set bits to '1', not clear them to '0'). Accesses to non-accessible SRAM return a bus error. Wounding control is rounded to next power of two bytes. "0": entire memory accessible "1": first 1/2 of the memory accessible. "2": first 1/4 of the memory accessible. "3": first 1/8 of the memory accessible. "4": first 1/16 of the memory accessible. "5": first 1/32 of the memory accessible. "6": first 1/64 of the memory accessible. "7": first 1/128 of the memory accessible. Default Value: 0

4.1.8 SOCMEM_PWR_PARTITION_CTL0

Description: SRAM partition power control

Address: 0x44640200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						ACT_OFF [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						RET_OFF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 8	RET_OFF	This field defines the power state of each SRAM partition in DeepSleep/DeepSleep-RAM power modes. (Note that partition-0 can support upto two sub partitions within, when parameter SUB-_PARTITION_NR is set to 1 i.e. partition 0 is divided into partition-A and partition-B). 2'b00- sub partition-B is to be powered-ON and sub partition- A is to be powered-ON. 2'b01- sub partition-B is to be powered-ON and sub partition- A is to be powered-OFF. 2'b10- sub partition-B is to be powered-OFF and sub partition- A is to be powered-ON. 2'b11- sub partition-B is to be powered-OFF and sub partition- A is to be powered-OFF. (Note if a partition has a sub-partition, 2'b00,2'b01,2'b10,2'b11 are all valid values. If a partition doesn't have sub-partition, Only 2'b00, 2'b01 are valid values , 2'b10,2'b11 are reserved.) Notes: RET_OFF is exact replica of PWR_PARTITION_CTL.ACT_OFF, which enables independent SRAM partition granularity control in Active vs DeepSleep* modes and avoids SW reconfiguration of PWR_PARTITION_CTL register while switching power modes. Since this register field PWR_PARTITION_CTL.RET_OFF is applicable and used by HW only in retention mode, any update to this register field (PWR_PARTITION_CTL.RET_OFF) does not change status of PWR_STATUS.PWR_DONE. i.e. PWR_STATUS.PWR_DONE is not applicable for RET_OFF field SW programming. Default Value: 0

4.1.8 SOCMEM_PWR_PARTITION_CTL0 (continued)

1 : 0	ACT_OFF	This field defines the power state of each SRAM partition in Active power mode (Note that partition-0 can support upto two sub partitions within, when parameter SUB_PARTITION_NR is set to 1 i.e. partition 0 is divided into partition-A and partition-B). 2'b00- sub partition-B is to be powered-ON and sub partition- A is to be powered-ON. 2'b01- sub partition-B is to be powered-ON and sub partition- A is to be powered-OFF. 2'b10- sub partition-B is to be powered-OFF and sub partition- A is to be powered-ON. 2'b11- sub partition-B is to be powered-OFF and sub partition- A is to be powered-OFF. (Note if a partition has a sub-partition, 2'b00,2'b01,2'b10,2'b11 are all valid values. If a partition doesn't have sub-partition, Only 2'b00, 2'b01 are valid values , 2'b10,2'b11 are reserved.) It is mandatory to check for PWR_STATUS.PWR_DONE to become 1 once this PWR_PARTITION_CTL register contents are changed to ensure SRAM mode transition is completed successfully. Default Value: 0

4.1.9 SOCMEM_PWR_PARTITION_CTL_LOCK

Description: SRAM power partition control Lock

Address: 0x44640280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						A	
Name	Reserved [7:2]						PWR_PARTITION_CT-L_LOCK [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	PWR_PARTITION_CT-L_LOCK	Prohibits Read/Write access to PWR_PARTITION_CTL register when this field is not equal to 0. Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. By default AHB reads/writes to PWR_PARTITION_CTL register are locked. Default Value: 3 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0 **0x2: CLR1 :** Clears bit 1 **0x3: SET01 :** Sets both bits 0 and 1

4.1.10 SOCMEM_PWR_DELAY_CTL

Description: SRAM power switch power up & sequence delay

Address: 0x44640284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SEQ0_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SEQ1_DELAY [31:24]							

Bits	Name	Description
31 : 24	SEQ1_DELAY	Number of IMO clock cycles delay needed for sequence-1 of SRAM power transition Default Value: 0x9
23 : 16	SEQ0_DELAY	Number of IMO clock cycles delay needed for sequence-0 of SRAM power transition Default Value: 0x2
9 : 0	UP	Number of IMO clock cycles delay needed after power domain power up Default Value: 0x9

4.1.11 SOCMEM_PWR_STATUS

Description: SRAM power status

Address: 0x44640288

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							PWR_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	PWR_DONE	After a PWR_PARTITION_CTL.OFF change this flag indicates if the new power mode has taken effect or not. 1: Indicates change is effective; 0: Indicates change is in progress; Default Value: 1

4.1.12 SOCMEM_SRAM_MPC0_CFG

Description: Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.

Address: 0x44642000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			
HW Access	Reserved			R	Reserved			
Name	Reserved [7:5]			RE-SPONSE	Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	RESPONSE	Response Configuration for Security and PC violations 0: Read-Zero Write Ignore (RAZ/WI) 1: Bus Error Default Value: 0

4.1.13 SOCMEM_SRAM_MPC0_CTRL

Description: Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)

Address: 0x44642100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	Reserved						
HW Access	R	Reserved						
Name	LOCK	Reserved [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for this protection context. Software can set this bit but not clear it once set. When set, write operations to BLK_LUT are not possible from this protection context. Setting LOCK also blocks writes to CTRL itself (for that PC copy). All writes are ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for this protection context as a side effect of each read/write access to BLK_LUT Default Value: 1

4.1.14 SOCMEM_SRAM_MPC0_BLK_MAX

Description: Max value of block-based index register

Address: 0x44642104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R				
HW Access	Reserved			R				
Name	Reserved [7:5]			VALUE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; See product datasheet for details on protection of external memories. Default Value: 31

4.1.15 SOCMEM_SRAM_MPC0_BLK_CFG

Description: Block size & initialization in progress

Address: 0x44642108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	INIT_IN_PROGRESS	Reserved [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to BLK_LUT is blocked (BLK_IDX increment is also ignored). The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ... up to 15: 1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 8

4.1.16 SOCMEM_SRAM_MPC0_BLK_IDX

Description: Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)

Address: 0x4464210C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [7:5]			VALUE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	VALUE	Index value for accessing block-based lookup table using BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

4.1.17 SOCMEM_SRAM_MPC0_BLK_LUT

Description: NS status for 32 blocks at BLK_IDX with PC=_pc>

Address: 0x44642110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS7	ATTR_NS6	ATTR_NS5	ATTR_NS4	ATTR_NS3	ATTR_NS2	ATTR_NS1	ATTR_NS0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS15	ATTR_NS14	ATTR_NS13	ATTR_NS12	ATTR_NS11	ATTR_NS10	ATTR_NS9	ATTR_NS8

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS23	ATTR_NS22	ATTR_NS21	ATTR_NS20	ATTR_NS19	ATTR_NS18	ATTR_NS17	ATTR_NS16

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS31	ATTR_NS30	ATTR_NS29	ATTR_NS28	ATTR_NS27	ATTR_NS26	ATTR_NS25	ATTR_NS24

Bits	Name	Description
31	ATTR_NS31	NS bit for block 31 based on BLK_IDX Default Value: 0
30	ATTR_NS30	NS bit for block 30 based on BLK_IDX Default Value: 0
29	ATTR_NS29	NS bit for block 29 based on BLK_IDX Default Value: 0
28	ATTR_NS28	NS bit for block 28 based on BLK_IDX Default Value: 0
27	ATTR_NS27	NS bit for block 27 based on BLK_IDX Default Value: 0
26	ATTR_NS26	NS bit for block 26 based on BLK_IDX Default Value: 0
25	ATTR_NS25	NS bit for block 25 based on BLK_IDX Default Value: 0
24	ATTR_NS24	NS bit for block 24 based on BLK_IDX Default Value: 0
23	ATTR_NS23	NS bit for block 23 based on BLK_IDX Default Value: 0
22	ATTR_NS22	NS bit for block 22 based on BLK_IDX Default Value: 0

4.1.17 SOCMEM_SRAM_MPC0_BLK_LUT (continued)

21	ATTR_NS21	NS bit for block 21 based on BLK_IDX Default Value: 0
20	ATTR_NS20	NS bit for block 20 based on BLK_IDX Default Value: 0
19	ATTR_NS19	NS bit for block 19 based on BLK_IDX Default Value: 0
18	ATTR_NS18	NS bit for block 18 based on BLK_IDX Default Value: 0
17	ATTR_NS17	NS bit for block 17 based on BLK_IDX Default Value: 0
16	ATTR_NS16	NS bit for block 16 based on BLK_IDX Default Value: 0
15	ATTR_NS15	NS bit for block 15 based on BLK_IDX Default Value: 0
14	ATTR_NS14	NS bit for block 14 based on BLK_IDX Default Value: 0
13	ATTR_NS13	NS bit for block 13 based on BLK_IDX Default Value: 0
12	ATTR_NS12	NS bit for block 12 based on BLK_IDX Default Value: 0
11	ATTR_NS11	NS bit for block 11 based on BLK_IDX Default Value: 0
10	ATTR_NS10	NS bit for block 10 based on BLK_IDX Default Value: 0
9	ATTR_NS9	NS bit for block 9 based on BLK_IDX Default Value: 0
8	ATTR_NS8	NS bit for block 8 based on BLK_IDX Default Value: 0
7	ATTR_NS7	NS bit for block 7 based on BLK_IDX Default Value: 0
6	ATTR_NS6	NS bit for block 6 based on BLK_IDX Default Value: 0
5	ATTR_NS5	NS bit for block 5 based on BLK_IDX Default Value: 0
4	ATTR_NS4	NS bit for block 4 based on BLK_IDX Default Value: 0
3	ATTR_NS3	NS bit for block 3 based on BLK_IDX Default Value: 0
2	ATTR_NS2	NS bit for block 2 based on BLK_IDX Default Value: 0
1	ATTR_NS1	NS bit for block 1 based on BLK_IDX Default Value: 0
0	ATTR_NS0	NS bit for block 0 based on BLK_IDX Default Value: 0

4.1.18 SOCMEM_SRAM_MPC0_ROT_CTRL

Description: Control register with lock bit and auto-increment only

Address: 0x44642200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	Reserved						
HW Access	R	Reserved						
Name	LOCK	Reserved [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for the root-of-trust configuration registers. Software can set this bit but not clear it once set. When set, write operations to ROT_BLK_LUT are not possible. Write is ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for each read/write of ROT_BLK_LUT Default Value: 1

4.1.19 SOCMEM_SRAM_MPC0_ROT_BLK_MAX

Description: Max value of block-based index register for ROT

Address: 0x44642208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R						
HW Access	Reserved	R						
Name	Reserved	VALUE [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 127

4.1.20 SOCMEM_SRAM_MPC0_ROT_BLK_CFG

Description: Same as BLK_CFG

Address: 0x4464220C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	INIT_IN_PROGRESS	Reserved [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to ROT_BLK_LUT is RAZWI. The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ...up to 15:1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 8

4.1.21 SOCMEM_SRAM_MPC0_ROT_BLK_IDX

Description: Index of 8-block group accessed through ROT_BLK_LUT_*

Address: 0x44642210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	RW						
Name	Reserved	VALUE [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6 : 0	VALUE	Index value for accessing block-based lookup table using ROT_BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

4.1.22 SOCMEM_SRAM_MPC0_ROT_BLK_PC

Description: Protection context of 8-block group accesses through ROT_BLK_LUT

Address: 0x44642214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	PC	Specify PC values for ROT_BLK_IDX and ROT_BLK_LUT Default Value: 0

4.1.23 SOCMEM_SRAM_MPC0_ROT_BLK_LUT

Description: (R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC

Address: 0x44642218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR1 [6:4]			Reserved	ATTR0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR3 [14:12]			Reserved	ATTR2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR5 [22:20]			Reserved	ATTR4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR7 [30:28]			Reserved	ATTR6 [26:24]		

Bits	Name	Description
30 : 28	ATTR7	W/R/NS bits for block 7 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
26 : 24	ATTR6	W/R/NS bits for block 6 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
22 : 20	ATTR5	W/R/NS bits for block 5 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
18 : 16	ATTR4	W/R/NS bits for block 4 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
14 : 12	ATTR3	W/R/NS bits for block 3 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
10 : 8	ATTR2	W/R/NS bits for block 2 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
6 : 4	ATTR1	W/R/NS bits for block 1 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
2 : 0	ATTR0	W/R/NS bits for block 0 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0

4.1.24 SOCMEM_PATCH_STRUCT_CTL00

Description: Patch structure control

Address: 0x44650800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					Reserved		RW
HW Access	R					Reserved		R
Name	MATCH_ADDR [7:3]					Reserved [2:1]		VALID

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MATCH_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MATCH_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MATCH_ADDR [31:24]							

Bits	Name	Description
4098 : 3	MATCH_ADDR	Match address. SROM accesses are matched/compared to this address. An address match results into patching/redirection of the SROM access (if PATCH_CTL.ENABLED is '1'): the SROM access is redirected to an SRAM access. The PATCH_SRAM register and the "matching" patch structure index determine the SRAM access address. Specifically, given an index i, the SRAM access address is given by: PATCH_SRAM.ADDR + i * "patch size", where patch size is the number of Bytes that are patched by a single patch structure (2 ^ (3+CFG.PATCH_SIZE)). The MATCH_ADDR[] bit range is dependent on two design time configuration parameters: - The lowest index is determined by PATCH_SIZE. E.g., a 8 Byte patch size uses "3" as the lowest bit index, a 16 Byte patch size uses "4" as the lowest bit index, etc. Unused lower bit indices are '0'. - The highest index is determined by the SROM size as specified by SROM_MASK (the next power of two multiple of the SROM size). E.g., a 0xffff:0000 mask specifies a 64 KByte SROM size and uses "15" as the highest bit index, a 0xfff0:0000 mask specifies a 1 MByte SROM size and uses "19" as the highest bit index, etc. Unused higher bit indices reflect the SROM location in the address space. Default Value: Undefined
0	VALID	Patch structure validity: '0': Not valid. '1': Valid. Note: VALID uses the bit field "0" location, rather than the more typical bit field "31" location. This architecture decision was made to allow for SROM location anywhere in a 32-bit address space, and not require extensive address manipulation when accessing PATCH_CTL.MATCH_ADDR. Default Value: 0

4.1.25 SOCMEM_PPU_SOCMEM_PWPR

Description: Power Policy Register

Address: 0x44660000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			LOCK_EN	Reserved [11:9]			PWR_DY-N_EN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							OP_DY-N_EN

Bits	Name	Description
24	OP_DYN_EN	Reserved Default Value: 0x0
19 : 16	OP_POLICY	Reserved Default Value: 0x0
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. When this bit is set to 1 dynamic transitions are enabled for power modes, allowing transitions to be initiated by changes on power mode DEVACTIVE inputs. Default Value: 0x1
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), MEM_RET(2), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x8

4.1.26 SOCMEM_PPU_SOCMEM_PMER

Description: Power Mode Emulation Register

Address: 0x44660004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							EMU_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	EMU_EN	Reserved Default Value: 0x0

4.1.27 SOCMEM_PPU_SOCMEM_PWSR

Description: Power Status Register

Address: 0x44660008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PWR_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved			R
HW Access	Reserved			RW	Reserved			RW
Name	Reserved [15:13]			LOCK_STA-TUS	Reserved [11:9]			PWR_DY-N_STATUS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [23:20]				OP_STATUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [31:25]							OP_DY-N_STATUS

Bits	Name	Description
24	OP_DYN_STATUS	Reserved Default Value: 0x0
19 : 16	OP_STATUS	Reserved Default Value: 0x0
12	LOCK_STATUS	Reserved Default Value: 0x0
8	PWR_DYN_STATUS	Power mode dynamic transition status. When set to 1 power mode dynamic transitions are enabled. There might be a delay in dynamic transitions becoming active or inactive if the PPU is transitioning when PWR_DYN_EN is programmed. Default Value: 0x0
3 : 0	PWR_STATUS	Power mode status. These bits reflect the current power mode of the PPU. See PPU_PWPR.PWR_POLICY for power mode enumeration. Default Value: 0x0

4.1.28 SOCMEM_PPU_SOCMEM_DISR

Description: Device Interface Input Current Status Register

Address: 0x44660010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PWR_DEVACTIVE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					R		
HW Access	Reserved					RW		
Name	Reserved [15:11]					PWR_DEVACTIVE_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	OP_DEVACTIVE_STATUS [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVE_STATUS	Reserved Default Value: 0x0
10 : 0	PWR_DEVACTIVE_STATUS	Status of the power mode DEVACTIVE inputs. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 0 is for Q-channel device 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0

4.1.29 SOCMEM_PPU_SOCMEM_MISR

Description: Miscellaneous Input Current Status Register

Address: 0x44660014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							PCSMPACCEPT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DEVACCEPT_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DEVDENY_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	DEVDENY_STATUS	Status of the device interface DEVDENY inputs. There is one bit for each device interface DEVQDENY. For example, bit 16 is for Q-Channel 0 DEVQDENY, and bit 17 for Q-Channel 1 DEVQDENY. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
15 : 8	DEVACCEPT_STATUS	Status of the device interface DEVACCEPT inputs. There is one bit for each device interface DEVQACCEPTn. For example, bit 8 is for Q-Channel 0 DEVQACCEPTn and bit 9 for Q-Channel 1 DEVQACCEPTn. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
0	PCSMPACCEPT_STATUS	The status of the PCSMPACCEPT input. Default Value: 0x0

4.1.30 SOCMEM_PPU_SOCMEM_STSR

Description: Stored Status Register

Address: 0x44660018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	STORED_DEVDENY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	STORED_DEVDENY	Reserved (this PPU has a single Q-channel) Default Value: 0x0

4.1.31 SOCMEM_PPU_SOCMEM_UNLK

Description: Unlock register

Address: 0x4466001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							UNLOCK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	UNLOCK	Reserved Default Value: 0x0

4.1.32 SOCMEM_PPU_SOCMEM_PWCR

Description: Power Configuration Register

Address: 0x44660020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVREQEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PWR_DEVACTIVEEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_DEVACTIVEEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	OP_DEVACTIVEEN [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVEEN	Reserved Default Value: 0x0
18 : 8	PWR_DEVACTIVEEN	These bits enable the power mode DEVACTIVE inputs. When a bit is to 1 the related DEVACTIVE input is enabled, when set to 0 it is disabled. All available bits are reset to 1. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE, and bit 9 for the Q-Channel 1 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x003
7 : 0	DEVREQEN	When set to 1 enables the device interface handshake for transitions. All available bits are reset to 1. There is one bit for each device interface channel. For example, bit 0 is for Q-Channel 0, and bit 1 is for Q-Channel 1. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x03

4.1.33 SOCMEM_PPU_SOCMEM_PTCR

Description: Power Mode Transition Configuration Register

Address: 0x44660024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						DBG_RE-COV_POR ST_EN	WARM_RS T_DEVREQ EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	DBG_RE-COV_PORST_EN	Reserved Default Value: 0x0
0	WARM_RST_DEVREQEN	Transition behavior between ON and WARM_RST. This bit should not be modified when the PPU is in WARM_RST, or if the PPU is performing a transition, otherwise PPU behavior is UN-PREDICTABLE. 0: The PPU does not perform a device interface handshake when transitioning between ON and WARM_RST. 1: The PPU performs a device interface handshake when transitioning between ON and WARM_RST. This disables all Q-Channels for this transition. Default Value: 0x0

4.1.34 SOCMEM_PPU_SOCMEM_IMR

Description: Interrupt Mask Register

Address: 0x44660030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		LOCKED_IRQ_MASK	EMU_DENY_IRQ_MASK	EMU_ACCEPT_IRQ_MASK	STA_DENY_IRQ_MASK	STA_ACCEPT_IRQ_MASK	STA_POLICY_TRN_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	LOCKED_IRQ_MASK	Reserved Default Value: 0x1
4	EMU_DENY_IRQ_MASK	Reserved Default Value: 0x1
3	EMU_ACCEPT_IRQ_MASK	Reserved Default Value: 0x1
2	STA_DENY_IRQ_MASK	Static transition denial event mask. Default Value: 0x0
1	STA_ACCEPT_IRQ_MASK	Static transition acceptance event mask. Default Value: 0x1
0	STA_POLICY_TRN_IRQ_MASK	Static full policy transition completion event mask. Default Value: 0x0

4.1.35 SOCMEM_PPU_SOCMEM_AIMR

Description: Additional Interrupt Mask Register

Address: 0x44660034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	RW	RW	RW
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ_MASK	STA_POLICY_PWR_IRQ_MASK	DYN_DENY_IRQ_MASK	DYN_ACCEPT_IRQ_MASK	UNSPT_POLICY_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ_MASK	Reserved Default Value: 0x1
3	STA_POLICY_PWR_IRQ_MASK	Reserved Default Value: 0x1
2	DYN_DENY_IRQ_MASK	Dynamic transition denial event mask. Default Value: 0x1
1	DYN_ACCEPT_IRQ_MASK	Dynamic transition acceptance event mask. Default Value: 0x1
0	UNSPT_POLICY_IRQ_MASK	Unsupported Policy event mask. Default Value: 0x0

4.1.36 SOCMEM_PPU_SOCMEM_ISR

Description: Interrupt Status Register

Address: 0x44660038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	Reserved	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	Reserved	R	R	R	R	R	R
Name	OTH-ER_IRQ	Reserved	LOCKED_IRQ	EMU_DE-NY_IRQ	EMU_AC-CEPT_IRQ	STA_DE-NY_IRQ	STA_AC-CEPT_IRQ	STA_POLI-CY_TRN_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	PWR_ACTIVE_EDGE_IRQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW1C		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_ACTIVE_EDGE_IRQ [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	OP_ACTIVE_EDGE_IRQ [31:24]							

Bits	Name	Description
31 : 24	OP_ACTIVE_EDGE_IRQ	Indicates which operating mode DEVPACTIVE inputs caused the input edge event. When operating modes are not supported this field is reserved. Default Value: 0x0
18 : 8	PWR_ACTIVE_EDGE_IRQ	Indicates which power mode DEVACTIVE inputs caused the input edge event. Bits for unused channels are the MSBs and are reserved. There is one bit for each device Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x00
7	OTHER_IRQ	Indicates there is an interrupt event pending in the Additional Interrupt Status Register (PPU_AISR). Default Value: 0x0
5	LOCKED_IRQ	Reserved Default Value: 0x0
4	EMU_DENY_IRQ	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ	Reserved Default Value: 0x0
2	STA_DENY_IRQ	Static transition denial event status. Default Value: 0x0
1	STA_ACCEPT_IRQ	Static transition acceptance event status. Default Value: 0x0

4.1.36 SOCMEM_PPU_SOCMEM_ISR (continued)

0	STA_POLICY_TRN_IRQ	Static full policy transition completion event status. Default Value: 0x0

4.1.37 SOCMEM_PPU_SOCMEM_AISR

Description: Additional Interrupt Status Register

Address: 0x4466003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ	STA_POLICY_PWR_IRQ	DYN_DENY_IRQ	DYN_ACCEPT_IRQ	UNSPT_POLICY_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ	Reserved Default Value: 0x0
2	DYN_DENY_IRQ	Dynamic transition denial event status. Default Value: 0x0
1	DYN_ACCEPT_IRQ	Dynamic transition acceptance event status. Default Value: 0x0
0	UNSPT_POLICY_IRQ	Unsupported Policy event status. Default Value: 0x0

4.1.38 SOCMEM_PPU_SOCMEM_IESR

Description: Input Edge Sensitivity Register

Address: 0x44660040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE03_EDGE [7:6]		DEVACTIVE02_EDGE [5:4]		DEVACTIVE01_EDGE [3:2]		DEVACTIVE00_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE07_EDGE [15:14]		DEVACTIVE06_EDGE [13:12]		DEVACTIVE05_EDGE [11:10]		DEVACTIVE04_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		RW		RW	
HW Access	Reserved		R		R		R	
Name	Reserved [23:22]		DEVACTIVE10_EDGE [21:20]		DEVACTIVE09_EDGE [19:18]		DEVACTIVE08_EDGE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 20	DEVACTIVE10_EDGE	Reserved Default Value: 0x0
19 : 18	DEVACTIVE09_EDGE	Reserved Default Value: 0x0
17 : 16	DEVACTIVE08_EDGE	Reserved Default Value: 0x0
15 : 14	DEVACTIVE07_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE06_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE05_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE04_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE03_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE02_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE01_EDGE	DEVACTIVE 1 edge sensitivity. Default Value: 0x0

4.1.38 SOCMEM_PPU_SOCMEM_IESR (continued)

1 : 0	DEVACTIVE00_EDGE	DEVACTIVE 0 edge sensitivity. Default Value: 0x0

4.1.39 SOCMEM_PPU_SOCMEM_OPSR

Description: Operating Mode Active Edge Sensitivity Register

Address: 0x44660044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE19_EDGE [7:6]		DEVACTIVE18_EDGE [5:4]		DEVACTIVE17_EDGE [3:2]		DEVACTIVE16_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE23_EDGE [15:14]		DEVACTIVE22_EDGE [13:12]		DEVACTIVE21_EDGE [11:10]		DEVACTIVE20_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	DEVACTIVE23_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE22_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE21_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE20_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE19_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE18_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE17_EDGE	Reserved Default Value: 0x0
1 : 0	DEVACTIVE16_EDGE	Reserved Default Value: 0x0

4.1.40 SOCMEM_PPU_SOCMEM_FUNRR

Description: Functional Retention RAM Configuration Register

Address: 0x44660050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FUNC_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FUNC_RET_RAM_CFG	Reserved Default Value: 0x0

4.1.41 SOCMEM_PPU_SOCMEM_FULRR

Description: Full Retention RAM Configuration Register

Address: 0x44660054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FULL_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FULL_RET_RAM_CFG	Reserved Default Value: 0x0

4.1.42 SOCMEM_PPU_SOCMEM_MEMRR

Description: Memory Retention RAM Configuration Register

Address: 0x44660058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	MEM_RET_RAM_CFG	Reserved Default Value: 0x0

4.1.43 SOCMEM_PPU_SOCMEM_EDTR0

Description: Power Mode Entry Delay Register 0

Address: 0x44660160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOGIC_RET_DEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	FULL_RET_DEL [31:24]							

Bits	Name	Description
31 : 24	FULL_RET_DEL	Reserved Default Value: 0x00
23 : 16	LOGIC_RET_DEL	Reserved Default Value: 0x00
15 : 8	MEM_RET_DEL	Reserved Default Value: 0x00
7 : 0	OFF_DEL	Reserved Default Value: 0x00

4.1.44 SOCMEM_PPU_SOCMEM_EDTR1

Description: Power Mode Entry Delay Register 1

Address: 0x44660164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FUNC_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	FUNC_RET_DEL	Reserved Default Value: 0x00
7 : 0	MEM_OFF_DEL	Reserved Default Value: 0x00

4.1.45 SOCMEM_PPU_SOCMEM_DCDR0

Description: Device Control Delay Configuration Register 0

Address: 0x44660170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CLKEN_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ISO_CLKEN_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RST_HWSTAT_DLY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	RST_HWSTAT_DLY	Reserved Default Value: 0x0
15 : 8	ISO_CLKEN_DLY	Reserved Default Value: 0x0
7 : 0	CLKEN_RST_DLY	Reserved Default Value: 0x0

4.1.46 SOCMEM_PPU_SOCMEM_DCDR1

Description: Device Control Delay Configuration Register 1

Address: 0x44660174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ISO_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CLKEN_ISO_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	CLKEN_ISO_DLY	Reserved Default Value: 0x0
7 : 0	ISO_RST_DLY	Reserved Default Value: 0x0

4.1.47 SOCMEM_PPU_SOCMEM_IDR0

Description: PPU Identification Register 0

Address: 0x44660FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	NUM_OPMODE [7:4]				DEVCHAN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	STA_-FUNC_RET_SPT	STA_-FULL_RET_SPT	STA_MEM_OFF_SPT	STA_LG-C_RET_SPT	STA_MEM_RET_EMU_SPT	STA_MEM_RET_SPT	STA_OFF_EMU_SPT	STA_OFF_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	Reserved	R	R	R
HW Access	RW	RW	RW	RW	Reserved	RW	RW	RW
Name	DY-N_MEM_RET_EMU_SPT	DY-N_MEM_RET_SPT	DY-N_OFF_EMU_SPT	DY-N_OFF_SPT	Reserved	STA_DB-G_RE-COV_SPT	STA_WRM_RST_SPT	STA_ON_SPT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [31:30]		DY-N_WRM_RST_SPT	DY-N_ON_SPT	DYN_-FUNC_RET_SPT	DYN_-FULL_RET_SPT	DY-N_MEM_OFF_SPT	DYN_LG-C_RET_SPT

Bits	Name	Description
29	DYN_WRM_RST_SPT	Dynamic WARM_RST support. Default Value: 0x0
28	DYN_ON_SPT	Dynamic ON support. Default Value: 0x1
27	DYN_FUNC_RET_SPT	Dynamic FUNC_RET support. Default Value: 0x0
26	DYN_FULL_RET_SPT	Dynamic FULL_RET support. Default Value: 0x0
25	DYN_MEM_OFF_SPT	Dynamic MEM_OFF support. Default Value: 0x0
24	DYN_LGC_RET_SPT	Dynamic LOGIC_RET support. Default Value: 0x0
23	DY-N_MEM_RET_EMU_SPT	Dynamic MEM_RET_EMU support Default Value: 0x0
22	DYN_MEM_RET_SPT	Dynamic MEM_RET support. Default Value: 0x1

4.1.47 SOCMEM_PPU_SOCMEM_IDR0 (continued)

21	DYN_OFF_EMU_SPT	Dynamic OFF_EMU support. Default Value: 0x0
20	DYN_OFF_SPT	Dynamic OFF support. Default Value: 0x1
18	STA_DBG_RECOV_SPT	DBG_RECOV support. Default Value: 0x0
17	STA_WRM_RST_SPT	WARM_RST support. Ignore this bit. Do not use WARM_RST. Default Value: 0x1
16	STA_ON_SPT	ON support. Default Value: 0x1
15	STA_FUNC_RET_SPT	FUNC_RET support. Default Value: 0x0
14	STA_FULL_RET_SPT	FULL_RET support. Default Value: 0x0
13	STA_MEM_OFF_SPT	MEM_OFF support. Default Value: 0x0
12	STA_LGC_RET_SPT	LOGIC_RET support. Default Value: 0x0
11	STA_MEM_RET_EMU_SPT	MEM_RET_EMU support. Default Value: 0x0
10	STA_MEM_RET_SPT	MEM_RET support. Default Value: 0x1
9	STA_OFF_EMU_SPT	OFF_EMU support. Default Value: 0x0
8	STA_OFF_SPT	OFF support. Default Value: 0x1
7 : 4	NUM_OPMODE	No. of operating modes supported is NUM_OPMODE + 1. Default Value: 0x0
3 : 0	DEVCHAN	No. of Device Interface Channels. The device enumeration is: Device 0: SOCMEM SEQ between between SOCMEM MMIO, ports & Banks. Device 1: SRSS PDCM Default Value: 0x2

4.1.48 SOCMEM_PPU_SOCMEM_IDR1

Description: PPU Identification Register 1

Address: 0x44660FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	Reserved	R	R	R
HW Access	Reserved	RW	RW	RW	Reserved	RW	RW	RW
Name	Reserved	FUNC_RET_RAM_REG	FULL_RET_RAM_REG	MEM_RET_RAM_REG	Reserved	LOCK_SPT	SW_DEV_DEL_SPT	PWR_MODE_ENTRY_DEL_SPT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved	R	R	R
HW Access	Reserved			RW	Reserved	RW	RW	RW
Name	Reserved [15:13]			OFF_MEM_RET_TRANS	Reserved	OP_ACTIVE	STA_POLICY_OP_IRQ_SPT	STA_POLICY_PWR_IRQ_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	OFF_MEM_RET_TRANS	OFF to MEM_RET direct transition. Indicates if direct transitions from OFF to MEM_RET and from OFF_EMU to MEM_RET_EMU are supported. Default Value: 0x0
10	OP_ACTIVE	Reserved Default Value: 0x0
9	STA_POLICY_OP_IRQ_SPT	Operating policy transition completion event status. Default Value: 0x0
8	STA_POLICY_PWR_IRQ_SPT	Power policy transition completion event status. Default Value: 0x0
6	FUNC_RET_RAM_REG	Indicates if the PPU_FUNRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
5	FULL_RET_RAM_REG	Indicates if the PPU_FULRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
4	MEM_RET_RAM_REG	Indicates if the PPU_MEMRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x1
2	LOCK_SPT	Lock and the lock interrupt event are supported. Default Value: 0x0

4.1.48 SOCMEM_PPU_SOCMEM_IDR1 (continued)

1	SW_DEV_DEL_SPT	Software device delay control configuration support. Default Value: 0x0
0	PWR_MODE_EN-TRY_DEL_SPT	Power mode entry delay support. Default Value: 0x0

4.1.49 SOCMEM_PPU_SOCMEM_IIDR

Description: Implementation Identification Register

Address: 0x44660FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IMPLEMENTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	REVISION [15:12]				IMPLEMENTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PRODUCT_ID [23:20]				VARIANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 20	PRODUCT_ID	PPU part identification. Default Value: 0x0B6
19 : 16	VARIANT	Major revision of the product. Default Value: 0
15 : 12	REVISION	Minor revision of the product. Default Value: 0
11 : 0	IMPLEMENTER	Implementer identification. [11:8] The JEP106 continuation code of the implementer. [7] Always 0. [6:0] The JEP106 identity code of the implementer. For an Arm implementation, bits [11:0] are 0x43B. Default Value: 0x43B

4.1.50 SOCMEM_PPU_SOCMEM_AIDR

Description: Architecture Identification Register

Address: 0x44660FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	ARCH_REV_MAJOR [7:4]				ARCH_REV_MINOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ARCH_REV_MAJOR	0x1 - PPU architecture major revision 1. Other Values - Reserved. Default Value: 0x1
3 : 0	ARCH_REV_MINOR	0x1 - PPU Architecture minor revision 1. Other Values - Reserved. Default Value: 0x1

4.1.51 SOCMEM_PPU_SOCMEM_PID4

Description: Implementation Defined Identification Register (PID4)

Address: 0x44660FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				IMPLEMENTER_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	IMPLEMENTER_11_8	The JEP106 continuation code of the implementer, which is 0x4 hardcoded value. Default Value: 0x4

4.1.52 SOCMEM_PPU_SOCMEM_PID0

Description: Implementation Defined Identification Register (PID0)

Address: 0x44660FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID_7_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PRODUCT_ID_7_0	PPU part identification bits [7:0]. Default Value: 0xB6

4.1.53 SOCMEM_PPU_SOCMEM_PID1

Description: Implementation Defined Identification Register (PID1)

Address: 0x44660FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	IMPLEMENTER_3_0 [7:4]				PRODUCT_ID_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	IMPLEMENTER_3_0	JEP106_ID bits [3:0] Default Value: 0xB
3 : 0	PRODUCT_ID_11_8	PPU part identification bits [11:8] Default Value: 0x0

4.1.54 SOCMEM_PPU_SOCMEM_PID2

Description: Implementation Defined Identification Register (PID2)

Address: 0x44660FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R	R		
HW Access	RW				RW	RW		
Name	REV_CONST [7:4]				CON-ST_HIGH	IMPLEMENTER_6_4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	REV_CONST	Constant LOW Revision (4 bits) Default Value: 0x1
3	CONST_HIGH	Constant HIGH Default Value: 0x1
2 : 0	IMPLEMENTER_6_4	JEP106_ID bits [6:4] Default Value: 0x3

4.1.55 SOCMEM_PPU_SOCMEM_PID3

Description: Implementation Defined Identification Register (PID3)

Address: 0x44660FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PID3_REVISION [7:4]				PID3_REV_CONST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	PID3_REVISION	Minor revision of the product. Default Value: 0x0
3 : 0	PID3_REV_CONST	Constant LOW (4 bits) Default Value: 0x0

4.1.56 SOCMEM_PPU_SOCMEM_ID0

Description: Implementation Defined Identification Register (ID0)

Address: 0x44660FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID0	ID0 hard coded value Default Value: 0x0D

4.1.57 SOCMEM_PPU_SOCMEM_ID1

Description: Implementation Defined Identification Register (ID1)

Address: 0x44660FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID1	ID1 hardcoded value Default Value: 0xF0

4.1.58 SOCMEM_PPU_SOCMEM_ID2

Description: Implementation Defined Identification Register (ID2)

Address: 0x44660FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID2	ID2 hardcoded value Default Value: 0x05

4.1.59 SOCMEM_PPU_SOCMEM_ID3

Description: Implementation Defined Identification Register (ID3)

Address: 0x44660FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ID3	ID3 hardcoded value Default Value: 0xB1

4.1.60 SOCMEM_SOCMEM_PD_CTL

Description: Power Domain Control

Address: 0x44661000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							BLEED_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	BLEED_EN	Activates bleed feature for the controlled power domain Default Value: 0

4.1.61 SOCMEM_SOCMEM_PD_PWR_UP_DELAY

Description: Active switch weak enable to active switch strong enable delay

Address: 0x44661004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COUNT_LOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_COUNT_LOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	MEM_COUNT_LOAD	Load value for counter running on clk_pwr (10MHz) providing the timing from weak MEM switch enable to strong MEM switch enable. Default is 5 for ~500ns Default Value: 0
7 : 0	COUNT_LOAD	Load value for counter running on clk_pwr (10MHz) providing the timing from weak ACTIVE switch enable to strong ACTIVE switch enable. Default is 5 for ~500ns Default Value: 5

5 Non-Volatile Memory (NVM) registers

This section discusses the NVM registers. It lists all the registers in mapping tables, in address order.

5.1 Register details

Register name	Address	Description
RRAMC0_RRAM_EXTRA_AREA_GENERAL_OTP0	0x42204000	GENERAL_OTP subregion (5.5KB). This is the starting address of a register bank containing 1408 registers (RRAMC0_RRAM_EXTRA_AREA_GENERAL_OTP0 to RRAMC0_RRAM_EXTRA_AREA_GENERAL_OTP1407).
RRAMC0_RRAMC0_AHB_HRESP	0x42210000	RRAMC AHB HRESP
RRAMC0_RRAMC0_PC_MASK	0x42210020	PC acquisition and releasing
RRAMC0_RRAMC0_RRAM_PROTECTED_X	0x42210024	Size of PROTECTED_NVM subregion (8KB * X)
RRAMC0_RRAMC0_RRAM_SFLASH_Y	0x42210028	Size of SFLASH_NVM subregion (8KB * Y)
RRAMC0_RRAMC0_RRAM_WORK_Z	0x4221002C	Size of WORK_NVM subregion (8KB * Z)
RRAMC0_RRAMC0_RRAM_MAIN_N	0x42210030	Size of MAIN_NVM subregion (8KB * N)
RRAMC0_RRAMC0_RRAM_CTL	0x42210100	RRAM macro OSC control
RRAMC0_RRAMC0_PROTECTED_LOCKABLE_LOCK	0x42210104	PROTECTED_NVM lockable configuration
RRAMC0_RRAMC0_UDS_CTL	0x42210110	UDS control
RRAMC0_RRAMC0_RECLAIMED_MAIN_NVM_SIZE	0x42210114	Reclaimed size (KB) from upgradeable
RRAMC0_RRAMC0_TB_GATING_CTL	0x42210118	Turn-off Tagbit post-read gating control check
RRAMC0_MPC0_CFG	0x42211000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.
RRAMC0_MPC0_CTRL	0x42211100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)
RRAMC0_MPC0_BLK_MAX	0x42211104	Max value of block-based index register
RRAMC0_MPC0_BLK_CFG	0x42211108	Block size & initialization in progress
RRAMC0_MPC0_BLK_IDX	0x4221110C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)
RRAMC0_MPC0_BLK_LUT	0x42211110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>

Non-Volatile Memory (NVM) registers

Register name	Address	Description
RRAMC0_MPC0_ROT_CTRL	0x42211200	Control register with lock bit and auto-increment only
RRAMC0_MPC0_ROT_BLK_MAX	0x42211208	Max value of block-based index register for ROT
RRAMC0_MPC0_ROT_BLK_CFG	0x4221120C	Same as BLK_CFG
RRAMC0_MPC0_ROT_BLK_IDX	0x42211210	Index of 8-block group accessed through ROT_BLK_LUT_*
RRAMC0_MPC0_ROT_BLK_PC	0x42211214	Protection context of 8-block group accesses through ROT_BLK_LUT
RRAMC0_MPC0_ROT_BLK_LUT	0x42211218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC
RRAMC0_MPC1_CFG	0x42212000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.. See RRAMC0_MPC0_CFG for the details of bit fields.
RRAMC0_MPC1_CTRL	0x42212100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc). See RRAMC0_MPC0_CTRL for the details of bit fields.
RRAMC0_MPC1_BLK_MAX	0x42212104	Max value of block-based index register. See RRAMC0_MPC0_BLK_MAX for the details of bit fields.
RRAMC0_MPC1_BLK_CFG	0x42212108	Block size & initialization in progress. See RRAMC0_MPC0_BLK_CFG for the details of bit fields.
RRAMC0_MPC1_BLK_IDX	0x4221210C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc). See RRAMC0_MPC0_BLK_IDX for the details of bit fields.
RRAMC0_MPC1_BLK_LUT	0x42212110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>. See RRAMC0_MPC0_BLK_LUT for the details of bit fields.
RRAMC0_MPC1_ROT_CTRL	0x42212200	Control register with lock bit and auto-increment only. See RRAMC0_MPC0_ROT_CTRL for the details of bit fields.

Non-Volatile Memory (NVM) registers

Register name	Address	Description
RRAMC0_MPC1_ROT_BLK_MAX	0x42212208	Max value of block-based index register for ROT. See RRAMC0_MPC0_ROT_BLK_MAX for the details of bit fields.
RRAMC0_MPC1_ROT_BLK_CFG	0x4221220C	Same as BLK_CFG. See RRAMC0_MPC0_ROT_BLK_CFG for the details of bit fields.
RRAMC0_MPC1_ROT_BLK_IDX	0x42212210	Index of 8-block group accessed through ROT_BLK_LUT_*. See RRAMC0_MPC0_ROT_BLK_IDX for the details of bit fields.
RRAMC0_MPC1_ROT_BLK_PC	0x42212214	Protection context of 8-block group accesses through ROT_BLK_LUT. See RRAMC0_MPC0_ROT_BLK_PC for the details of bit fields.
RRAMC0_MPC1_ROT_BLK_LUT	0x42212218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC. See RRAMC0_MPC0_ROT_BLK_LUT for the details of bit fields.
RRAMC0_RRAM_SFR_NVM_STATUS	0x42213000	status register
RRAMC0_RRAM_SFR_NVM_PROG	0x42213004	programming control register
RRAMC0_RRAM_SFR_NVM_ADDR	0x42213008	address register
RRAMC0_RRAM_SFR_NVM_CONF1	0x4221300C	configuration register
RRAMC0_RRAM_SFR_NVM_HARDEN1	0x42213010	hardening configuration register
RRAMC0_RRAM_SFR_NVM_HARDADDR	0x42213014	hardening address register
RRAMC0_RRAM_SFR_NVM_HRESP	0x42213018	bus response register
RRAMC0_RRAM_SFR_NVM_ECCLOG	0x4221301C	ECC failure logging register
RRAMC0_RRAM_SFR_NVM_ECCLOGIR	0x42213020	ECC failure logging interrupt register
RRAMC0_RRAM_SFR_NVM_VMODE	0x42213024	voltage mode register

5.1.1 RRAMC0_RRAM_EXTRA_AREA_GENERAL_OTP0

Description: GENERAL_OTP subregion (5.5KB)

Address: 0x42204000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	GENERAL_OTP_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	GENERAL_OTP_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	GENERAL_OTP_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	GENERAL_OTP_VALUE [31:24]							

Bits	Name	Description
31 : 0	GENERAL_OTP_VALUE	GENERAL_OTP subregion (5.5KB) Default Value: 0

5.1.2 RRAMC0_RRAMC0_AHB_HRESP

Description: RRAMC AHB HRESP

Address: 0x42210000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				HRESP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	RW	Reserved						
Name	RE-SET_HRE-SP	Reserved [30:24]						

Bits	Name	Description
31	RESET_HRESP	0: No reset to AHB_HRESP 1: Triggering reset to AHB_HRESP by hardware after one clock cycle Default Value: 0

5.1.2 RRAMC0_RRAMC0_AHB_HRESP (continued)

3 : 0	HRESP	Logs RRAMC AHB bus errors/faults on the PROTECTED interface and SFR/MMIO PC acquisition/status violations. 4'b0000: No AHB bus error 4'b0001: OTP Tagbit[2:0] violation during write (the target OTP is tagged 3'b111) 4'b0010: Post-read check Tagbit[2:0] violation during read (when target NVM/OTP tagged other than 3'b000) 4'b0011: Post-read check address fault alarm 4'b0100: RARM IP AHB bus error (Needs to read RRAM SFR NVM_HRESP for causes of the error) 4'b0101: Incomplete write or 8/16 write on the protected interface 4'b0110: Indirect sequence where AHB write address mismatch with SFR NVM_ADDR on the protected interface or direct write target address not in defined range on the BISR interface 4'b0111: Programming PROTECTED_NVM lockable subsection when PROTECTED_LOCKABLE_LOCK.LOCK is locked (write-protected) 4'b1000: 4'b1001: Detecting UDS read access while UDS is locked 4'b1010: 4'b1011: 4'b1100: Executing indirect operation without a PC acquired 4'b1101: Transaction PC is different (or same PC but different HMASTER_ID) than the acquired PC or transaction PC is not PC0 in VIRGIN/SORT LCS 4'b1110: Executing forming or looped forming in SORT LCS 4'b1111: Protected interface MPC violation Default Value: 0

5.1.3 RRAMC0_RRAMC0_PC_MASK

Description: PC acquisition and releasing

Address: 0x42210020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	PC_LOCK [31:28]				Reserved [27:24]			

Bits	Name	Description
31 : 28	PC_LOCK	SW writes to PC_LOCK to acquire / release a PC. 4'b0000: Not locked, any PC can lock again 4'b1111: PC [3:0] locked PC_LOCK is redundantly implemented. Any other bit encoding besides the aforementioned two values during programming or at any instance in time causes an AHB bus error, resulting into a fault/interrupt to the system fault reporting infrastructure. Default Value: 0
3 : 0	PC	PC allowed for an indirect sequence 4'b0000: PC0 4'b0001: PC1 4'b0010: PC2 4'b0011: PC3 ... 4'b0111: PC7 Default Value: 0

5.1.4 RRAMC0_RRAMC0_RRAM_PROTECTED_X

Description: Size of PROTECTED_NVM subregion (8KB * X)

Address: 0x42210024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PROTECTED_X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	PROTECTED_X [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	PROTECTED_X [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PROTECTED_X [31:24]							

Bits	Name	Description
31 : 0	PROTECTED_X	Size of PROTECTED_NVM, same value as RTL parameter PROTECTED_X Default Value: 32

5.1.5 RRAMC0_RRAMC0_RRAM_SFLASH_Y

Description: Size of SFLASH_NVM subregion (8KB * Y)

Address: 0x42210028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	SFLASH_Y [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	SFLASH_Y [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	SFLASH_Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	SFLASH_Y [31:24]							

Bits	Name	Description
31 : 0	SFLASH_Y	Size of SFLASH_NVM, same value as RTL parameter SFLASH_Y Default Value: 0

5.1.6 RRAMC0_RRAMC0_RRAM_WORK_Z

Description: Size of WORK_NVM subregion (8KB * Z)

Address: 0x4221002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK_Z [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK_Z [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WORK_Z [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WORK_Z [31:24]							

Bits	Name	Description
31 : 0	WORK_Z	Size of WORK_NVM, same value as RTL parameter WORK_Z Default Value: 0

5.1.7 RRAMC0_RRAMC0_RRAM_MAIN_N

Description: Size of MAIN_NVM subregion (8KB * N)

Address: 0x42210030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MAIN_N [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MAIN_N [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MAIN_N [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MAIN_N [31:24]							

Bits	Name	Description
31 : 0	MAIN_N	Size of MAIN_NVM, same value as RTL parameter MAIN_N Default Value: 32

5.1.8 RRAMC0_RRAMC0_RRAM_CTL

Description: RRAM macro OSC control

Address: 0x42210100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		OSC_OUT_ON	OSC_EXKEEP_RUN	OSC_EXCLK10_EN	OSC_EXCLK40_EN	OSC_EXCLK80_EN	OSC_EXCLK160_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	OSC_OUT_ON	Enables the RRAM macro oscillator output after RRAM reset. Determines the reset value of NVM_OSCCONF.OSC_OUT Static signal of RRAM macro. 0: Disabled . 1: Enabled. Default Value: 0
4	OSC_EXKEEP_RUN	Keep internal oscillator running. If osc_exkeeprun_i is '0', and the FSM signals the internal oscillator to switch off, it is really switched off (without generating spikeson the clock signal). If osc_exkeeprun_i is '1' and the FSM signals the internal oscillator to switch off, it is not switched off. Instead it waits for osc_exkeeprun_i to become '0' and then isswitched off (without generating spikes on the clock signal). When osc_exkeeprun_i becomes'1', the internal oscillator is switched on again. Note: For NVM_OSCCONF.OSC_ON = '0', the oscillator is switched off independent of signal osc_exkeeprun_i. Default Value: 0
3	OSC_EXCLK10_EN	Enables the RRAM macro oscillator output with oscillator frequency/16. 0: Disabled . 1: Enabled. This is effective only when OSC_OUT_ON is 1. Default Value: 0
2	OSC_EXCLK40_EN	Enables the RRAM macro oscillator output with oscillator frequency/4. 0: Disabled . 1: Enabled. This is effective only when OSC_OUT_ON is 1. Default Value: 0

5.1.8 RRAMC0_RRAMC0_RRAM_CTL (continued)

1	OSC_EXCLK80_EN	Enables the RRAM macro oscillator output with oscillator frequency/2. 0: Disabled . 1: Enabled. This is effective only when OSC_OUT_ON is 1. Default Value: 0
0	OSC_EXCLK160_EN	Enables the RRAM macro oscillator output with default oscillator frequency. 0: Disabled . 1: Enabled. This is effective only when OSC_OUT_ON is 1. Default Value: 0

5.1.9 RRAMC0_RRAMC0_PROTECTED_LOCKABLE_LOCK

Description: PROTECTED_NVM lockable configuarion

Address: 0x42210104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PARTITION_SIZE_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PARTITION_SIZE_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S				Reserved			
HW Access	R				Reserved			
Name	LOCK [31:28]				Reserved [27:24]			

Bits	Name	Description
31 : 28	LOCK	4'b0000: Not locked, PARTITION_SIZE_0/1 changes and lockable programming are allowed 4'b1111: Locked, PARTITION_SIZE_0/1 changes and Lockable programming are NOT allowed except the topmost 1KB of lockable which is always writable regardless of "LOCK" status Any other bit encoding besides the aforementioned two values during programming or at any instance in time causes an AHB bus error, resulting into a fault/interrupt to the host (fault reporting infrastructure). Trying to program PROTECTED_NVM lockable subsection or program/change PARTITION_SIZE_0/1 during locked LOCK triggers AHB bus error. SW can write to PARTITION_SIZE and LOCK at the same transaction. Default Value: 0
15 : 8	PARTITION_SIZE_1	Redundant implementation of the size encoding If bit[7:0] and bit[15:8] are different during programming or at any instance in time, AHB bus error (while programming) is generated and fault/interrupt is triggered to the system fault reporting infrastructure SW must write both PARTITION_SIZE_0/1 at the same transaction Default Value: 0
7 : 0	PARTITION_SIZE_0	8'h00: 1KB lockable subsection in PROTECTED_NVM 8'h01: 2KB lockable subsection in PROTECTED_NVM 8'h02: 3KB lockable subsection in PROTECTED_NVM .. .. 8'hfd: 254KB lockable subsection in PROTECTED_NVM 8'hfe: 255KB lockable subsection in PROTECTED_NVM 8'hff: 256KB lockable subsection in PROTECTED_NVM In case size is larger than PROTECTERD_NVM, the entire PROTECTED_NVM is lockable, there is no upgradable subsection Default Value: 0

5.1.10 RRAMC0_RRAMC0_UDS_CTL

Description: UDS control

Address: 0x42210110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							CONFIG

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S				Reserved			
HW Access	R				Reserved			
Name	LOCK [31:28]				Reserved [27:24]			

Bits	Name	Description
31 : 28	LOCK	4'b0000: Not locked 4'b1111: Locked. No access to UDS_KEY. Once locked, cannot be changed till next reset Any other bit encoding besides the aforementioned two values during programming or at any instance in time causes an AHB bus error, resulting into a fault/interrupt to the host (fault reporting infrastructure). Default Value: 0
0	CONFIG	1'b0: When LOCKED, read access triggers "read-as-zero" and no error 1'b1: When LOCKED, read access triggers AHB bus error Default Value: 0

5.1.11 RRAMC0_RRAMC0_RECLAIMED_MAIN_NVM_SIZE

Description: Reclaimed size (KB) from upgradeable

Address: 0x42210114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	RECLAIMED_SIZE_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	RECLAIMED_SIZE_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	RECLAIMED_SIZE_1	Redundant implementation of RECLAIMED_SIZE encoding If bit[7:0] and bit[15:8] are different during programming or at any instance in time, AHB bus error (while programming) is generated and fault/interrupt is triggered to the system fault reporting infrastructure SW must write both RECLAIMED_SIZE_0/RECLAIMED_SIZE_1 at the same transaction Default Value: 0
7 : 0	RECLAIMED_SIZE_0	8'h00: 0KB upgradeable reclaimed from PROTECTED_NVM 8'h01: 1KB upgradeable reclaimed from PROTECTED_NVM 8'h02: 2KB upgradeable reclaimed from PROTECTED_NVM .. .. 8'hfd: 253KB upgradeable reclaimed from PROTECTED_NVM 8'hfe: 254KB upgradeable reclaimed from PROTECTED_NVM 8'hff: 255KB upgradeable reclaimed from PROTECTED_NVM In case the size of the reclaimed is larger than PROTECTERD_NVM, the entire PROTECTED_NVM is reclaimed, there is no PROTECTED_NVM Default Value: 0

5.1.12 RRAMC0_RRAMC0_TB_GATING_CTL

Description: Turn-off Tagbit post-read gating control check

Address: 0x42210118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C				Reserved			
HW Access	R				Reserved			
Name	TB_GATING_OFF [31:28]				Reserved [27:24]			

Bits	Name	Description
31 : 28	TB_GATING_OFF	4'b0000: Gating control on 4'b1111: Gating control off (in test mode) Any other bit encoding besides the aforementioned two values during programming or at any instance in time causes an AHB bus error, resulting into a fault/interrupt to the host (fault reporting infrastructure). Write 4'b1111 (once only) to clear to 4'b0000, write 4'b0000 is ignored (no error response/no fault) Default Value: 0xF

5.1.13 RRAMC0_MPC0_CFG

Description: Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.

Address: 0x42211000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			
HW Access	Reserved			R	Reserved			
Name	Reserved [7:5]			RE-SPONSE	Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	RESPONSE	Response Configuration for Security and PC violations 0: Read-Zero Write Ignore (RAZ/WI) 1: Bus Error Default Value: 0

5.1.14 RRAMC0_MPC0_CTRL

Description: Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)

Address: 0x42211100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	Reserved						
HW Access	R	Reserved						
Name	LOCK	Reserved [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for this protection context. Software can set this bit but not clear it once set. When set, write operations to BLK_LUT are not possible from this protection context. Setting LOCK also blocks writes to CTRL itself (for that PC copy). All writes are ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for this protection context as a side effect of each read/write access to BLK_LUT Default Value: 1

5.1.15 RRAMC0_MPC0_BLK_MAX

Description: Max value of block-based index register

Address: 0x42211104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	
HW Access	Reserved						R	
Name	Reserved [7:2]						VALUE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; See product datasheet for details on protection of external memories. Default Value: 3

5.1.16 RRAMC0_MPC0_BLK_CFG

Description: Block size & initialization in progress

Address: 0x42211108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	INIT_IN_PROGRESS	Reserved [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to BLK_LUT is blocked (BLK_IDX increment is also ignored). The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ... up to 15: 1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 7

5.1.17 RRAMC0_MPC0_BLK_IDX

Description: Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)

Address: 0x4221110C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						RW	
Name	Reserved [7:2]						VALUE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	VALUE	Index value for accessing block-based lookup table using BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

5.1.18 RRAMC0_MPC0_BLK_LUT

Description: NS status for 32 blocks at BLK_IDX with PC=_pc>

Address: 0x42211110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS7	ATTR_NS6	ATTR_NS5	ATTR_NS4	ATTR_NS3	ATTR_NS2	ATTR_NS1	ATTR_NS0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS15	ATTR_NS14	ATTR_NS13	ATTR_NS12	ATTR_NS11	ATTR_NS10	ATTR_NS9	ATTR_NS8

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS23	ATTR_NS22	ATTR_NS21	ATTR_NS20	ATTR_NS19	ATTR_NS18	ATTR_NS17	ATTR_NS16

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS31	ATTR_NS30	ATTR_NS29	ATTR_NS28	ATTR_NS27	ATTR_NS26	ATTR_NS25	ATTR_NS24

Bits	Name	Description
31	ATTR_NS31	NS bit for block 31 based on BLK_IDX Default Value: 0
30	ATTR_NS30	NS bit for block 30 based on BLK_IDX Default Value: 0
29	ATTR_NS29	NS bit for block 29 based on BLK_IDX Default Value: 0
28	ATTR_NS28	NS bit for block 28 based on BLK_IDX Default Value: 0
27	ATTR_NS27	NS bit for block 27 based on BLK_IDX Default Value: 0
26	ATTR_NS26	NS bit for block 26 based on BLK_IDX Default Value: 0
25	ATTR_NS25	NS bit for block 25 based on BLK_IDX Default Value: 0
24	ATTR_NS24	NS bit for block 24 based on BLK_IDX Default Value: 0
23	ATTR_NS23	NS bit for block 23 based on BLK_IDX Default Value: 0
22	ATTR_NS22	NS bit for block 22 based on BLK_IDX Default Value: 0

5.1.18 RRAMC0_MPC0_BLK_LUT (continued)

21	ATTR_NS21	NS bit for block 21 based on BLK_IDX Default Value: 0
20	ATTR_NS20	NS bit for block 20 based on BLK_IDX Default Value: 0
19	ATTR_NS19	NS bit for block 19 based on BLK_IDX Default Value: 0
18	ATTR_NS18	NS bit for block 18 based on BLK_IDX Default Value: 0
17	ATTR_NS17	NS bit for block 17 based on BLK_IDX Default Value: 0
16	ATTR_NS16	NS bit for block 16 based on BLK_IDX Default Value: 0
15	ATTR_NS15	NS bit for block 15 based on BLK_IDX Default Value: 0
14	ATTR_NS14	NS bit for block 14 based on BLK_IDX Default Value: 0
13	ATTR_NS13	NS bit for block 13 based on BLK_IDX Default Value: 0
12	ATTR_NS12	NS bit for block 12 based on BLK_IDX Default Value: 0
11	ATTR_NS11	NS bit for block 11 based on BLK_IDX Default Value: 0
10	ATTR_NS10	NS bit for block 10 based on BLK_IDX Default Value: 0
9	ATTR_NS9	NS bit for block 9 based on BLK_IDX Default Value: 0
8	ATTR_NS8	NS bit for block 8 based on BLK_IDX Default Value: 0
7	ATTR_NS7	NS bit for block 7 based on BLK_IDX Default Value: 0
6	ATTR_NS6	NS bit for block 6 based on BLK_IDX Default Value: 0
5	ATTR_NS5	NS bit for block 5 based on BLK_IDX Default Value: 0
4	ATTR_NS4	NS bit for block 4 based on BLK_IDX Default Value: 0
3	ATTR_NS3	NS bit for block 3 based on BLK_IDX Default Value: 0
2	ATTR_NS2	NS bit for block 2 based on BLK_IDX Default Value: 0
1	ATTR_NS1	NS bit for block 1 based on BLK_IDX Default Value: 0
0	ATTR_NS0	NS bit for block 0 based on BLK_IDX Default Value: 0

5.1.19 RRAMC0_MPC0_ROT_CTRL

Description: Control register with lock bit and auto-increment only

Address: 0x42211200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	Reserved						
HW Access	R	Reserved						
Name	LOCK	Reserved [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for the root-of-trust configuration registers. Software can set this bit but not clear it once set. When set, write operations to ROT_BLK_LUT are not possible. Write is ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for each read/write of ROT_BLK_LUT Default Value: 1

5.1.20 RRAMC0_MPC0_ROT_BLK_MAX

Description: Max value of block-based index register for ROT

Address: 0x42211208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				VALUE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 15

5.1.21 RRAMC0_MPC0_ROT_BLK_CFG

Description: Same as BLK_CFG

Address: 0x4221120C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	INIT_IN_PROGRESS	Reserved [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to ROT_BLK_LUT is RAZWI. The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ...up to 15:1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 7

5.1.22 RRAMC0_MPC0_ROT_BLK_IDX

Description: Index of 8-block group accessed through ROT_BLK_LUT_*

Address: 0x42211210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				RW			
Name	Reserved [7:4]				VALUE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	VALUE	Index value for accessing block-based lookup table using ROT_BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

5.1.23 RRAMC0_MPC0_ROT_BLK_PC

Description: Protection context of 8-block group accesses through ROT_BLK_LUT

Address: 0x42211214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	PC	Specify PC values for ROT_BLK_IDX and ROT_BLK_LUT Default Value: 0

5.1.24 RRAMC0_MPC0_ROT_BLK_LUT

Description: (R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC

Address: 0x42211218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR1 [6:4]			Reserved	ATTR0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR3 [14:12]			Reserved	ATTR2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR5 [22:20]			Reserved	ATTR4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR7 [30:28]			Reserved	ATTR6 [26:24]		

Bits	Name	Description
30 : 28	ATTR7	W/R/NS bits for block 7 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
26 : 24	ATTR6	W/R/NS bits for block 6 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
22 : 20	ATTR5	W/R/NS bits for block 5 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
18 : 16	ATTR4	W/R/NS bits for block 4 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
14 : 12	ATTR3	W/R/NS bits for block 3 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
10 : 8	ATTR2	W/R/NS bits for block 2 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
6 : 4	ATTR1	W/R/NS bits for block 1 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
2 : 0	ATTR0	W/R/NS bits for block 0 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0

5.1.25 RRAMC0_RRAM_SFR_NVM_STATUS

Description: status register

Address: 0x42213000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R			R	R
HW Access	W	W	W	W			W	W
Name	ECC1READ	RWWERR	WRPERR	VERR [4:2]			SLEEP	BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R				R	R	R	R
HW Access	W				W	W	W	W
Name	WBFILL [15:12]				ECCA-READ	ECC4READ	ECC3READ	ECC2READ

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			R	R	R	R	R
HW Access	Reserved			W	W	W	W	W
Name	Reserved [23:21]			ECCAMRD	ECC4MRD	ECC3MRD	ECC2MRD	ECC1MRD

Bits	31	30	29	28	27	26	25	24
SW Access	R	R		R	R	R		
HW Access	W	W		W	W	W		
Name	WSUSP	REREA [30:29]		HARDFLAG	OLRFLAG	CONFSTATE [26:24]		

Bits	Name	Description
31	WSUSP	0: NVM not in write suspended mode. 1: NVM in write suspended mode. Resume command expected. Default Value: 0
30 : 29	REREA	Information on number of re-reads triggered by uncorrectable ECC read failures in the last read operations (and the initial reading of existing data for an indirect write operation): 00: no re-read operation was performed 01: in maximum one re-read operation was performed 10: in maximum two consecutive re-read operations were performed 11: in maximum three consecutive re-read operations were performed REREA is updated every time an uncorrectable ECC read failure triggered re_x0002_read operation(s) and a higher number of consecutive re-reads was performed than is indicated so far. REREA is reset by hardware, when NVM_PROG.RSTECC is written. Note: REREA is not changed when a re-read is performed within thehardening operation. Note: Maximum number of consecutive re-reads is configured in NVM_SETUP1.REREAD. Default Value: 0
28	HARDFLAG	Information, if hardening operation has performed internal write operation: 0: no 1: yes HARDFLAG is reset by hardware, when NVM_PROG.RSTVERR is written. HARDFLAG is automatically reset, when write mode, verify-only mode, hardening mode, or forming mode are entered (writing NVM_PROG.ACTION "not equal" "0000"). HARDFLAG does not accumulate, i.e. HARDFLAG is updated every time (latest at the end of a write or hardening operation started with NVM_PROG.STARTOP = "11". Default Value: 0

5.1.25 RRAMC0_RRAM_SFR_NVM_STATUS (continued)

27	OLRFLAG	Information, if online-repair (OLR) was triggered by last direct or indirect write operation: 0: no 1: yes OLRFLAG is reset by hardware, when NVM_PROG.RSTVERR is written. OLRFLAG is automatically reset, when write mode, verify-only mode, hardening mode, or forming mode are entered (writing NVM_PROG.ACTION "not equal" "0000"). OLRFLAG does not accumulate, i.e. OLRFLAG is updated every time (latest at the end of a write or hardening operation started with NVM_PROG.STARTOP = "11"). Default Value: 0
26 : 24	CONFSTATE	Information, on configuration status: xx0: NVM_SYSCONF* are not configured xx1: NVM_SYSCONF* are configured x0x: not all SFRs (excluding NVM_SYSCONF* and NVM_ALGO*) are configured x1x: all SFRs (excluding NVM_SYSCONF* and NVM_ALGO*) are configured 0xx: NVM_ALGO* are not configured 1xx: NVM_ALGO* are configured Default Value: 0
20	ECCAMRD	0: No address mismatch ECC failure during the most recent memory read operation to a new block (or the initial reading of existing data for an indirect write operation). 1: An address mismatch ECC failure was detected during the most recent memory read operation to a new block (or the initial reading of existing data for an indirect write operation). ECCAMRD is only set, if NVM_TEST1.ECCOFFRD = "0x" . For NVM_TEST1.ECCOFFRD = "1x", ECCAMRD is reset. The flag does not accumulate but is updated with every new loading of the read-buffer. Default Value: 0
19	ECC4MRD	0: No ECC-uncorrectable multi-bit failure during the most recent memory read operation to a new block (or the initial reading of existing data for an indirect write operation). 1: An ECC-uncorrectable multi-bit failure was detected during the most recent memory read operation to a new block (or the initial reading of existing data for an indirect write operation). ECC4MRD is only set, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) still yields an ECC_x0002_uncorrectable multi-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC4MRD is reset. The flag does not accumulate but is updated with every new loading of the read-buffer. Default Value: 0
18	ECC3MRD	0: No ECC triple-bit failure during the most recent memory read operation to a new block (or the initial reading of existing data for an indirect write operation). 1: An ECC triple-bit failure was detected and corrected during the most recent memory read operation to a new block (or the initial reading of existing data for an indirect write operation). ECC3MRD is only set, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) yields an ECC triple-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC3MRD is reset. The flag does not accumulate but is updated with every new loading of the read-buffer. Default Value: 0
17	ECC2MRD	0" No ECC double-bit failure during the most recent memory read operation to a new block (or the initial reading of existing data for an indirect write operation). 1: An ECC double-bit failure was detected and corrected during the most recent memory read operation to a new block (or the initial reading of existing data for an indirect write operation). ECC2MRD is only set, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) yields an ECC double-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC2MRD is reset. The flag does not accumulate but is updated with every new loading of the read-buffer. Default Value: 0

5.1.25 RRAMC0_RRAM_SFR_NVM_STATUS (continued)

16	ECC1MRD	0: No ECC single-bit failure during the most recent memory read operation to a new block (or the initial reading of existing data for an indirect write operation). 1: An ECC single-bit failure was detected and corrected during the most recent memory read operation to a new block (or the initial reading of existing data for an indirect write operation). ECC1MRD is only set, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) yields an ECC single-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC1MRD is reset. The flag does not accumulate but is updated with every new loading of the read-buffer. Default Value: 0
15 : 12	WBFILL	Filling state for the write-buffer data words. E.g. WBFILL = 0000 (Write-Buffer invalid), WBFILL = 0011 (Write-Buffer intermediate), WBFILL = 1111 (Write-Buffer valid) The bits of WBFILL are set by the hardware, when write, verify-only, or forming data is written into the write-buffer. WBFILL is reset after each direct write, online-repair, or hardening operation. Default Value: 0
11	ECCAREAD	0: No address mismatch ECC failure during the last memory read operations (or the initial reading of existing data for an indirect write operation). 1: At least one address mismatch ECC failure was detected during the last memory read operations (or the initial reading of existing data for an indirect write operation). ECCAREAD is only set, if NVM_TEST1.ECCOFFRD = "0x". For NVM_TEST1.ECCOFFRD = "1x", ECCAREAD stays unchanged. The flag accumulates until it is reset by hardware when NVM_PROG.RSTECC is written, i.e. sticky version of ECCAMRD. Default Value: 0
10	ECC4READ	0: No ECC-uncorrectable multi-bit failure during the last memory read operations (or the initial reading of existing data for an indirect write operation). 1: At least one ECC-uncorrectable multi-bit failure was detected during the last memory read operations (or the initial reading of existing data for an indirect write operation). ECC4READ is only set, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) still yields an ECC-uncorrectable multi-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC4READ stays unchanged. The flag accumulates until it is reset by hardware when NVM_PROG.RSTECC is written, i.e. sticky version of ECC4MRD. Default Value: 0
9	ECC3READ	0: No ECC triple-bit failure during the last memory read operations (or the initial reading of existing data for an indirect write operation). 1: At least one ECC triple-bit failure was detected and corrected during the last memory read operations (or the initial reading of existing data for an indirect write operation). ECC3READ is only set, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) yields an ECC triple-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC3READ stays unchanged. The flag accumulates until it is reset by hardware when NVM_PROG.RSTECC is written, i.e. sticky version of ECC3MRD. Default Value: 0
8	ECC2READ	0: No ECC double-bit failure during the last memory read operations (or the initial reading of existing data for an indirect write operation) 1: At least one ECC double-bit failure was detected and corrected during the last memory read operations (or the initial reading of existing data for an indirect write operation). ECC2READ is only set, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) yields an ECC double-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC2READ stays unchanged. The flag accumulates until it is reset by hardware when NVM_PROG.RSTECC is written, i.e. sticky version of ECC2MRD Default Value: 0

5.1.25 RRAMC0_RRAM_SFR_NVM_STATUS (continued)

7	ECC1READ	0: No ECC single-bit failure during the last memory read operations (or the initial reading of existing data for an indirect write operation). 1: At least one ECC single-bit failure was detected and corrected during the last memory read operations (or the initial reading of existing data for an indirect write operation). ECC1READ is only set, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) yields an ECC single-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC1READ stays unchanged. The flag accumulates until it is reset by hardware when NVM_PROG.RSTECC is written, i.e. sticky version of ECC1MRD. Default Value: 0
6	RWWERR	0: No read operation was stalled because of write, verify-only, forming, or hardening operation active. 1: At least one read operation was stalled because of write, verify-only, forming, or hardening operation active. The flag accumulates until it is reset by hardware when NVM_PROG.RSTECC is written. Default Value: 0
5	WRPERR	0: No operation triggered by writing NVM_PROG.STARTOP was ignored because of write protection. 1: At least one operation triggered by writing NVM_PROG.STARTOP was ignored because of write protection. The flag accumulates until it is reset by hardware when NVM_PROG.RSTECC is written. Default Value: 0
4 : 2	VERR	Information on number of fail bits for a block after verify operations in indirect write, verify-only, and forming operations: 000: no fail bit. 001: single-bit fail. 010: double-bit fail. 011: triple-bit fail. 100: uncorrectable fail bits encountered. 101: address mismatch ECC failure encountered. 110: no configuration retrieved, since no marker word found. 111: no algorithm settings retrieved, since no marker word found. VERR is reset by hardware, when NVM_PROG.RSTVERR is written. VERR is automatically reset, when write mode, verify-only mode, hardening mode, forming mode, or 'retrieve configuration settings' are entered (writing NVM_PROG.ACTION "not equal" "0000"). VERR does not accumulate, i.e. VERR is updated every time (at the end of an operation started with NVM_PROG.STARTOP = "11".) Note: VERR is not changed by hardening or direct write operations, except for the case where these operations need to internally call the 'retrieve configuration settings' operation. Default Value: 0
1	SLEEP	0: NVM not in sleep mode, and no sleep or wake up procedure in progress. 1: NVM in sleep mode, or busy due to a sleep or wake up procedure. Default Value: 1
0	BUSY	0: NVM is not busy. Memory accesses and register write accesses are possible. 1: NVM is busy. Memory accesses and register write accesses are not possible. Default Value: 0

5.1.26 RRAMC0_RRAM_SFR_NVM_PROG

Description: programming control register

Address: 0x42213004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				ACTION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	RW	RW	RW	RW	RW
HW Access	W		W	W	W	W	W	W
Name	STARTOP [15:14]		RSTECC	RSTVERR	RBINVAL	RSTIR	RSTTRAP	SELRCS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		Reserved	RW		
HW Access	Reserved		W		Reserved	W		
Name	Reserved [23:22]		SELAL [21:20]		Reserved	OLREN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW				Reserved			RW
HW Access	W				Reserved			W
Name	TEMP [31:28]				Reserved [27:25]			RDWB

Bits	Name	Description
31 : 28	TEMP	actual junction temperature: 0000: invalid/unknown junction temperature value. others: junction temperature value to be used for voltage compensation in programming algorithms. Example for coding: 0001: Tj <= 50C 0010: 50C < Tj <= 85C 0100: 85C < Tj <= 100C 1000: 100C < Tj <= 110C 1010: 110C < Tj <=120C 1100: Tj > 120C Note: The coding has to use increasing values of TEMP for increasing temperatures and it has to match to the coding employed in NVM_COMPEN.TMIN*. Default Value: 0
24	RDWB	Read from write-buffer: 0: disabled. 1: enabled for memory bus reads with ACTION = ["0001", "0010", "1000", "1110", "0111"] and read address matching content of NVMADDR. RDWB is automatically reset, when the content of the write-buffer is invalidated or when ACTION is changed. Default Value: 0

5.1.26 RRAMC0_RRAM_SFR_NVM_PROG (continued)

21 : 20	SELAL	Select type of write algorithm: 00: Employ first (typically standard, 8 bit parallel) algorithm defined by NVM_SELALGO1.SEL*ALGO1. 01: Employ second (typically strong, 8 bit parallel) algorithm defined by NVM_SELALGO1.SEL*ALGO2. 1x: Employ third (typically standard, 1 bit parallel) algorithm defined by NVM_SELALGO2.SEL*ALGO3. Default Value: 0
18 : 16	OLREN	000: disable online-repair (OLR). 001: enable online-repair for >= single-bit write or forming fail in block. 010: enable online-repair for >= double-bit write or forming fail in block. 011: enable online-repair for>= triple-bit write or forming fail in block. 1xx: enable online-repair for > triple-bit write or forming fail in block. Default Value: 0
15 : 14	STARTOP	Can only be set by software, is reset automatically by hardware after one clock cycle. 00: No start of operation defined by ACTION. 11: Start operation defined by ACTION, if these are not changed with the same write operation that sets STARTOP. Others: Interpreted and stored in SFR as "00". Default Value: 0
13	RSTECC	Can only be set by software, is reset automatically by hardware after one clock cycle. 0: No reset of NVM_STATUS.ECC*READ, NVM_STATUS.REREA, NVM_STATUS.RWWERR, and NVM_STATUS.WRPERR. 1: Reset of NVM_STATUS.ECC*READ, NVM_STATUS.REREA, NVM_STATUS.RWWERR, and NVM_STATUS.WRPERR. Default Value: 0
12	RSTVERR	Can only be set by software, is reset automatically by hardware after one clock cycle. 0: No reset of NVM_STATUS.VERR, NVM_STATUS.HARDFLAG, and NVM_STATUS.OLRFLAG. 1: Reset of NVM_STATUS.VERR, NVM_STATUS.HARDFLAG, and NVM_STATUS.OLRFLAG. Default Value: 0
11	RBINVAL	Can only be set by software, is reset automatically by hardware after one clock cycle. 0: No invalidation of read-buffer content. 1: Invalidation of read-buffer content. Default Value: 0
10	RSTIR	Can only be set by software, is reset automatically by hardware after one clock cycle. 0: No reset of ECC logging interrupt on nvm_ir_ecclog_req_o. 1: Reset of ECC logging interrupt on nvm_ir_ecclog_req_o. Default Value: 0
9	RSTTRAP	Can only be set by software, is reset automatically by hardware after one clock cycle. 0: No reset of NVM ready trap on nvm_trap_req_o. 1: Reset of NVM ready trap on nvm_trap_req_o. Default Value: 0
8	SELRCS	Select parameter for operation 'retrieve configuration settings' from configuration space in extra area. 0: Retrieve SYSCONF information and configuration settings, but do not retrieve write algorithm information. 1: Retrieve SYSCONF information, configuration settings, and write algorithm information. Note: SELRCS only applies to the sequence explicitly started with ACTION = "1011", but not to the implicitly started sequences during wake-up and write sequences Default Value: 0

5.1.26 RRAMC0_RRAM_SFR_NVM_PROG (continued)

3 : 0	ACTION	Selects indirect write, verify-only, hardening or forming operations: 0000: Idle state, no action triggered. Writing "0000" exits current mode. 0001: Select indirect write operation, using algorithm selected by SELAL, NVM_SELALGO1/2.SEL*ALGO1/2/3, and NVM_SETUP1.FSMSEQ. 0010: Select verify-only: Written data is compared to array content. 0100: Select hardening: Existing data is verified and hardened/corrected if necessary. 1000: Select forming operation, using algorithm selected by NVM_SELALGO2.SELFALGO. 1110: Select looped write operation, using algorithm selected by SLSTRAL, NVM_SELALGO1/2.SEL*ALGO1/2/3, and NVM_SETUP1.FSMSEQ; cannot be set, if NVM_ACC.ACC2_EN = '0'. Note: Only to be used in production test flow. 0111: Select looped forming operation, using algorithm selected by NVM_SELALGO2.SELFALGO; cannot be set, if NVM_ACC.ACC2_EN = '0'. Note: Only to be used in production test flow. 1011: Select operation 'retrieve configuration settings' from configuration space in extra area; cannot be set, if NVM_ACC.ACC3_EN = '0'. Others: Interpreted and stored in SFR as "0000" The operation selected by ACTION is performed, when STARTOP = "11" is written while ACTION stays constant. NVM_ADDR defines the address for the operation. Verification results can be read at NVM_STATUS.VERR. ACTION can only be changed to a value other than "0000", if the current value of ACTION is "0000". Otherwise ACTION = "0000" is stored. Once ACTION is set to a value other than "0000", ACTION can only be written again with its current value; any other value leads to a reset of ACTION to "0000" Default Value: 0

5.1.27 RRAMC0_RRAM_SFR_NVM_ADDR

Description: address register

Address: 0x42213008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	ADDRWL [7:5]			ADDRB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [23:18]						ADDRS [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 8	ADDRS	sector address for operations started with NVM_PROG. Default Value: 0
7 : 5	ADDRWL	wordline address for operations started with NVM_PROG. Default Value: 0
4 : 0	ADDRB	block address for operations started with NVM_PROG. Default Value: 0

5.1.28 RRAMC0_RRAM_SFR_NVM_CONF1

Description: configuration register

Address: 0x4221300C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW			Reserved		RW	
HW Access	Reserved	R			Reserved		R	
Name	Reserved	DWVERR [6:4]			Reserved [3:2]		HRLEV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	Reserved					
HW Access	R	R	Reserved					
Name	NVM_ON	TRAP_ON	Reserved [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SECPROT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved					RW	
HW Access	R	Reserved					R	
Name	WPLCK	Reserved [30:26]					SECPROT [25:24]	

Bits	Name	Description
31	WPLCK	Locking of protection settings in SECPROT: 0: SECPROT can be changed. 1: SECPROT cannot be changed. WPLCK cannot be written by software, if it is '1'. Default Value: 0
25 : 16	SECPROT	number of write protected sectors, starting with sector 0. SECPROT cannot be changed, if WPLCK = '1'. Default Value: 0
15	NVM_ON	0: NVM is switched to or stays in NVM sleep mode. 1: NVM is switched to or stays in normal mode. Default Value: 1
14	TRAP_ON	0: no NVM ready traps are generated on nvm_trap_req_o. 1: NVM ready traps are generated when long lasting NVM actions (indirect write, hardening, forming, and wake-up) are finished Note: Direct write operations and verify-only operations never generate a ready trap. Default Value: 0
6 : 4	DWVERR	for direct write operations, defines the threshold for a verify error indication: 000: verify is pass only, if no fail bit. 001: verify is pass only, if at most a single-bit fail. 010: verify is pass only, if at most a double-bit fail. 011: verify is pass only, if at most a triple-bit fail. 1xx: verify is always pass, independent of any fail bits. Default Value: 0x2

5.1.28 RRAMC0_RRAM_SFR_NVM_CONF1 (continued)

1 : 0	HRLEV	defines single hardread level for verify-only operation started for NVM_PROG.ACTION = "0010": 00: normal read. 01: hardread reset. 1x: hardread set. Default Value: 0

5.1.29 RRAMC0_RRAM_SFR_NVM_HARDEN1

Description: hardening configuration register

Address: 0x42213010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BLOCKS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved						RW
HW Access	R	Reserved						R
Name	ALLMEM	Reserved [14:9]						BLOCKS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	ALLMEM	selected address range for hardening operation: 0: defined by NVM_ADDR and BLOCKS. 1: complete memory. Default Value: 0
8 : 0	BLOCKS	BLOCKS+1 defines number of blocks in address range selected for hardening: start of hardening address range = NVM_ADDR end of hardening address range = NVM_ADDR + BLOCKS only valid for ALLMEM = '0' Default Value: 0

5.1.30 RRAMC0_RRAM_SFR_NVM_HARDADDR

Description: hardening address register

Address: 0x42213014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	ADDRWL [7:5]			ADDRB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [23:18]						ADDRS [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 8	ADDRS	sector address for automatic hardening Default Value: 0
7 : 5	ADDRWL	wordline address for automatic hardening Default Value: 0
4 : 0	ADDRB	block address for automatic hardening Default Value: 0

5.1.31 RRAMC0_RRAM_SFR_NVM_HRESP

Description: bus response register

Address: 0x42213018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R		
HW Access	Reserved					W		
Name	Reserved [7:3]					HRESP [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved						
HW Access	W	Reserved						
Name	RSTHRESP	Reserved [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	RSTHRESP	reset of NVM_HRESP: 0: no reset of HRESP triggered trigger 1: reset of HRESP RSTHRESP is reset automatically by hardware after one clock cycle Default Value: 0
2 : 0	HRESP	Root cause for triggered AHB-HRESP response: 000: AHB-HRESP not triggered. 001: reserved. 010: AHB-HRESP triggered by an error in configuration read started by direct write access or hardening. 011: AHB-HRESP triggered by use of unsupported ahb_hsize_i size code or by an incorrectly aligned address during a memory access. 100: AHB-HRESP triggered by an uncorrectable ECC read error or by an address mismatch ECC error. 101: AHB-HRESP triggered by direct write accesses to write protected addresses. 110: AHB-HRESP triggered by unsuccessful direct write, i.e. caused by direct write access where the fail-bit count exceeds NVM_CONF1.DWVERR. 111: AHB-HRESP triggered by simultaneously activated select signals. HRESP can be reset by software by writing RSTHRESP = '1'. Default Value: 0

5.1.32 RRAMC0_RRAM_SFR_NVM_ECCLOG

Description: ECC failure logging register

Address: 0x4221301C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ECC1CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ECC1CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ECC2CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	ECC4CNT [31:28]				ECC3CNT [27:24]			

Bits	Name	Description
31 : 28	ECC4CNT	Number of ECC-uncorrectable multi-bit failures detected during the last memory read operations (or the initial reading of existing data for a write operation). ECC4CNT is only updated, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) still yields an ECC-uncorrectable multi-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC4CNT stays unchanged. Default Value: 0
27 : 24	ECC3CNT	Number of ECC triple-bit failures detected and corrected during the last memory read operations (or the initial reading of existing data for a write operation). ECC3CNT is only updated, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) yields an ECC triple-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC3CNT stays unchanged. Default Value: 0
23 : 16	ECC2CNT	Number of ECC double-bit failures detected and corrected during the last memory read operations (or the initial reading of existing data for a write operation). ECC2CNT is only updated, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) yields an ECC double-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC2CNT stays unchanged. Default Value: 0
15 : 0	ECC1CNT	Number of ECC single-bit failures detected and corrected during the last memory read operations (or the initial reading of existing data for a write operation). ECC1CNT is only updated, if NVM_TEST1.ECCOFFRD = "0x" and if even the last re-read operation (configured in NVM_SETUP1.REREAD) yields an ECC single-bit failure. For NVM_TEST1.ECCOFFRD = "1x", ECC1CNT stays unchanged. Default Value: 0

5.1.33 RRAMC0_RRAM_SFR_NVM_ECCLOGIR

Description: ECC failure logging interrupt register

Address: 0x42213020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	W							
Name	ECC1CNTIR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	W							
Name	ECC1CNTIR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	W							
Name	ECC2CNTIR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	W				W			
Name	ECC4CNTIR [31:28]				ECC3CNTIR [27:24]			

Bits	Name	Description
31 : 28	ECC4CNTIR	Interrupt threshold for number of ECC-uncorrectable multi-bit failures indicated in NVM_ECCLOG.ECC4CNT: If NVM_ECCLOG.ECC4CNT becomes larger than ECC4CNTIR, an ECC logging interrupt is triggered. Default Value: 0xF
27 : 24	ECC3CNTIR	Interrupt threshold for number of ECC triple-bit failures indicated in NVM_ECCLOG.ECC3CNT: If NVM_ECCLOG.ECC3CNT becomes larger than ECC3CNTIR, an ECC logging interrupt is triggered Default Value: 0xF
23 : 16	ECC2CNTIR	Interrupt threshold for number of ECC double-bit failures indicated in NVM_ECCLOG.ECC2CNT: If NVM_ECCLOG.ECC2CNT becomes larger than ECC2CNTIR, an ECC logging interrupt is triggered. Default Value: 0xFF
15 : 0	ECC1CNTIR	Interrupt threshold for number of ECC single-bit failures indicated in NVM_ECCLOG.ECC1CNT: If NVM_ECCLOG.ECC1CNT becomes larger than ECC1CNTIR, an ECC logging interrupt is triggered. Default Value: 0xFFFF

5.1.34 RRAMC0_RRAM_SFR_NVM_VMODE

Description: voltage mode register

Address: 0x42213024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						W	
Name	Reserved [7:2]						VMODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	VMODE	voltage/frequency mode for operations: 00: undefined / unknown 01: ULP mode 10: MF mode 11: LP mode Default Value: 0

6 Fault Monitoring registers

This section discusses the Fault Monitoring registers. It lists all the registers in mapping tables, in address order.

6.1 Register details

Register name	Address	Description
FAULT_STRUCT0_CTL	0x422B0000	Fault control
FAULT_STRUCT0_STATUS	0x422B000C	Fault status
FAULT_STRUCT0_DATA0	0x422B0010	Fault data
FAULT_STRUCT0_DATA1	0x422B0014	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_DATA2	0x422B0018	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_DATA3	0x422B001C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_PENDING0	0x422B0040	Fault pending 0
FAULT_STRUCT0_PENDING1	0x422B0044	Fault pending 1
FAULT_STRUCT0_PENDING2	0x422B0048	Fault pending 2
FAULT_STRUCT0_MASK0	0x422B0050	Fault mask 0
FAULT_STRUCT0_MASK1	0x422B0054	Fault mask 1
FAULT_STRUCT0_MASK2	0x422B0058	Fault mask 2
FAULT_STRUCT0_INTR	0x422B00C0	Interrupt
FAULT_STRUCT0_INTR_SET	0x422B00C4	Interrupt set
FAULT_STRUCT0_INTR_MASK	0x422B00C8	Interrupt mask
FAULT_STRUCT0_INTR_MASKED	0x422B00CC	Interrupt masked
FAULT_STRUCT1_CTL	0x422B0100	Fault control. See FAULT_STRUCT0_CTL for the details of bit fields.
FAULT_STRUCT1_STATUS	0x422B010C	Fault status. See FAULT_STRUCT0_STATUS for the details of bit fields.
FAULT_STRUCT1_DATA0	0x422B0110	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA1	0x422B0114	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA2	0x422B0118	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA3	0x422B011C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_PENDING0	0x422B0140	Fault pending 0. See FAULT_STRUCT0_PENDING0 for the details of bit fields.
FAULT_STRUCT1_PENDING1	0x422B0144	Fault pending 1. See FAULT_STRUCT0_PENDING1 for the details of bit fields.

Fault Monitoring registers

Register name	Address	Description
FAULT_STRUCT1_PENDING2	0x422B0148	Fault pending 2. See FAULT_STRUCT0_PENDING2 for the details of bit fields.
FAULT_STRUCT1_MASK0	0x422B0150	Fault mask 0. See FAULT_STRUCT0_MASK0 for the details of bit fields.
FAULT_STRUCT1_MASK1	0x422B0154	Fault mask 1. See FAULT_STRUCT0_MASK1 for the details of bit fields.
FAULT_STRUCT1_MASK2	0x422B0158	Fault mask 2. See FAULT_STRUCT0_MASK2 for the details of bit fields.
FAULT_STRUCT1_INTR	0x422B01C0	Interrupt. See FAULT_STRUCT0_INTR for the details of bit fields.
FAULT_STRUCT1_INTR_SET	0x422B01C4	Interrupt set. See FAULT_STRUCT0_INTR_SET for the details of bit fields.
FAULT_STRUCT1_INTR_MASK	0x422B01C8	Interrupt mask. See FAULT_STRUCT0_INTR_MASK for the details of bit fields.
FAULT_STRUCT1_INTR_MASKED	0x422B01CC	Interrupt masked. See FAULT_STRUCT0_INTR_MASKED for the details of bit fields.

6.1.1 FAULT_STRUCT0_CTL

Description: Fault control

Address: 0x422B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [7:3]					RE-SET_REQ_EN	OUT_EN	TR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	RESET_REQ_EN	Reset request enable: '0': Disabled. '1': Enabled. The output reset request signal "fault_reset_req" reflects STATUS.VALID. This reset causes a warm/soft/core reset. This warm/soft/core reset does not affect the fault logic STATUS, DATA0, ..., DATA3 registers (allowing for post soft reset failure analysis). The "fault_reset_req" signals of the individual fault report structures are combined (logically OR'd) into a single SRSS "fault_reset_req" signal. Default Value: 0
1	OUT_EN	IO output signal enable: '0': Disabled. The IO output signal "fault_out" is '0'. The IO output enable signal "fault_out_en" is '0'. '1': Enabled. The IO output signal "fault_out" reflects STATUS.VALID. The IO output enable signal "fault_out_en" is '1'. Default Value: 0
0	TR_EN	Trigger output enable: '0': Disabled. The trigger output "tr_fault" is '0'. '1': Enabled. The trigger output "tr_fault" reflects STATUS.VALID. The trigger can be used to initiate a Datawire transfer of the FAULT data (FAULT_DATA0 through FAULT_DATA3). Default Value: 0

6.1.2 FAULT_STRUCT0_STATUS

Description: Fault status

Address: 0x422B000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	W						
Name	Reserved	IDX [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	RW1S	Reserved						
Name	VALID	Reserved [30:24]						

Bits	Name	Description
31	VALID	Valid indication: '0': Invalid. '1': Valid. STATUS.IDX, DATA0, ..., DATA3 specify the fault. Note: Typically, HW sets this field to '1' (on an activated HW fault source that is "enabled" by the MASK registers) and SW clears this field to '0' (typically by boot code SW (after a warm system reset, when the fault is handled). In this typical use case scenario, the HW source fault data is simultaneously captured into DATA0, ..., DATA3 when the VALID field is set to '1'. An exceptional SW use case scenario is identified as well. In this scenario, SW sets this field to '1' with a fault source index different to one of the defined HW fault sources. SW update is not restricted by the MASK registers). In both use case scenarios, the following holds: - STATUS.IDX, DATA0, ..., DATA3 can only be written when STATUS.VALID is '0'; the fault structure is not in use yet. Writing STATUS.VALID to '1' effectively locks the fault structure (until SW clears STATUS.VALID to '0'). This restriction requires a SW update to sequentially update the DATA registers followed by an update of the STATUS register. Note: For the exceptional SW use case, sequential updates to the DATA and STATUS registers may be "interrupted" by a HW fault capture. In this case, the SW DATA register updates are over-written by the HW update (and the STATUS.IDX field will reflect the HW capture) Default Value: 0
6 : 0	IDX	The fault source index for which fault information is captured in DATA0 through DATA3. The fault information is fault source specific and described below. Note: this register field (and associated fault source data in DATA0 through DATA3) should only be considered valid, when VALID is '1'. The description of the encoded meaning of this field is comes from the Fault assignment in the Product TRM. Default Value: Undefined

6.1.3 FAULT_STRUCT0_DATA0

Description: Fault data

Address: 0x422B0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Captured fault source data. Note: the DATA registers can only be written when STATUS.VALID is '0'. Note: the fault source index STATUS.IDX specifies the format of the DATA registers. Default Value: Undefined

6.1.4 FAULT_STRUCT0_PENDING0

Description: Fault pending 0

Address: 0x422B0040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the fault source. The list of fault sources is in the product.xls in the "Faults" tab. Default Value: Undefined

6.1.5 FAULT_STRUCT0_PENDING1

Description: Fault pending 1

Address: 0x422B0044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0: Peripheral group 0 PPU. Bit 1: Peripheral group 1 PPU. Bit 2: Peripheral group 2 PPU. Bit 3: Peripheral group 3 PPU. Bit 4: Peripheral group 4 PPU. Bit 5: Peripheral group 5 PPU. Bit 6: Peripheral group 6 PPU. Bit 7: Peripheral group 7 PPU. ... Bit 15: Peripheral group 15 PPU. Bit 16 - 31: See STATUS register. Default Value: Undefined

6.1.6 FAULT_STRUCT0_PENDING2

Description: Fault pending 2

Address: 0x422B0048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0 - 31: See STATUS register. Default Value: Undefined

6.1.7 FAULT_STRUCT0_MASK0

Description: Fault mask 0

Address: 0x422B0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 31 to 0. Default Value: 0

6.1.8 FAULT_STRUCT0_MASK1

Description: Fault mask 1

Address: 0x422B0054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 63 to 32. Default Value: 0

6.1.9 FAULT_STRUCT0_MASK2

Description: Fault mask 2

Address: 0x422B0058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 95 to 64. Default Value: 0

6.1.10 FAULT_STRUCT0_INTR

Description: Interrupt

Address: 0x422B00C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1C
HW Access	Reserved							RW1S
Name	Reserved [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	FAULT	This interrupt cause field is activated (HW sets the field to '1') when an enabled (MASK0/MASK1/MASK2) pending fault source is captured: - STATUS.VALID is set to '1'. - STATUS.IDX specifies the fault source index. - DATA0 through DATA3 captures the fault source data. SW writes a '1' to this field to clear the interrupt cause to '0'. SW clear STATUS.VALID to '0' to enable capture of the next fault. Note that when there is an enabled pending fault source, the pending fault source is captured immediately and INTR.FAULT is immediately activated (set to '1'). Default Value: 0

6.1.11 FAULT_STRUCT0_INTR_SET

Description: Interrupt set

Address: 0x422B00C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	FAULT	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

6.1.12 FAULT_STRUCT0_INTR_MASK

Description: Interrupt mask

Address: 0x422B00C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	FAULT	Mask bit for corresponding field in the INTR register. Default Value: 0

6.1.13 FAULT_STRUCT0_INTR_MASKED

Description: Interrupt masked

Address: 0x422B00CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	FAULT	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

7 High Performance Direct Memory Access (HPDMA) registers

This section discusses the HPDMA registers. It lists all the registers in mapping tables, in address order.

7.1 Register details

Register name	Address	Description
SAXI_DMAC_CTL	0x441A0000	Control
SAXI_DMAC_STATUS	0x441A0004	Enabled channels
SAXI_DMAC_ACTIVE	0x441A0008	Active channels
SAXI_DMAC_CH0_CTL	0x441A1000	Channel control
SAXI_DMAC_CH0_STATUS	0x441A1004	Channel status
SAXI_DMAC_CH0_IDX	0x441A1010	Channel current X and Y indices
SAXI_DMAC_CH0_SRC	0x441A1014	Channel current source address
SAXI_DMAC_CH0_DST	0x441A1018	Channel current destination address
SAXI_DMAC_CH0_M_IDX	0x441A101C	Channel current M index
SAXI_DMAC_CH0_CURR	0x441A1020	Channel current descriptor pointer
SAXI_DMAC_CH0_TR_CMD	0x441A1028	Channel software trigger
SAXI_DMAC_CH0_DESCR_STATUS	0x441A1040	Channel descriptor status
SAXI_DMAC_CH0_DESCR_CTL	0x441A1050	Channel descriptor control
SAXI_DMAC_CH0_DESCR_SRC	0x441A1054	Channel descriptor source
SAXI_DMAC_CH0_DESCR_DST	0x441A1058	Channel descriptor destination
SAXI_DMAC_CH0_DESCR_M_SIZE	0x441A105C	Channel descriptor M size
SAXI_DMAC_CH0_DESCR_X_SIZE	0x441A1060	Channel descriptor X size
SAXI_DMAC_CH0_DESCR_X_INCR	0x441A1064	Channel descriptor X increment
SAXI_DMAC_CH0_DESCR_Y_SIZE	0x441A1068	Channel descriptor Y size
SAXI_DMAC_CH0_DESCR_Y_INCR	0x441A106C	Channel descriptor Y increment
SAXI_DMAC_CH0_DESCR_NEXT	0x441A1070	Channel descriptor next pointer
SAXI_DMAC_CH0_INTR	0x441A1080	Interrupt
SAXI_DMAC_CH0_INTR_SET	0x441A1084	Interrupt set
SAXI_DMAC_CH0_INTR_MASK	0x441A1088	Interrupt mask
SAXI_DMAC_CH0_INTR_MASKED	0x441A108C	Interrupt masked
SAXI_DMAC_CH1_CTL	0x441A1100	Channel control. See SAXI_DMAC_CH0_CTL for the details of bit fields
SAXI_DMAC_CH1_STATUS	0x441A1104	Channel status. See SAXI_DMAC_CH0_STATUS for the details of bit fields
SAXI_DMAC_CH1_IDX	0x441A1110	Channel current X and Y indices. See SAXI_DMAC_CH0_IDX for the details of bit fields
SAXI_DMAC_CH1_SRC	0x441A1114	Channel current source address. See SAXI_DMAC_CH0_SRC for the details of bit fields

High Performance Direct Memory Access (HPDMA) registers

Register name	Address	Description
SAXI_DMAC_CH1_DST	0x441A1118	Channel current destination address. See SAXI_DMAC_CH0_DST for the details of bit fields
SAXI_DMAC_CH1_M_IDX	0x441A111C	Channel current M index. See SAXI_DMAC_CH0_M_IDX for the details of bit fields
SAXI_DMAC_CH1_CURR	0x441A1120	Channel current descriptor pointer. See SAXI_DMAC_CH0_CURR for the details of bit fields
SAXI_DMAC_CH1_TR_CMD	0x441A1128	Channel software trigger. See SAXI_DMAC_CH0_TR_CMD for the details of bit fields
SAXI_DMAC_CH1_DESCR_STATUS	0x441A1140	Channel descriptor status. See SAXI_DMAC_CH0_DESCR_STATUS for the details of bit fields
SAXI_DMAC_CH1_DESCR_CTL	0x441A1150	Channel descriptor control. See SAXI_DMAC_CH0_DESCR_CTL for the details of bit fields
SAXI_DMAC_CH1_DESCR_SRC	0x441A1154	Channel descriptor source. See SAXI_DMAC_CH0_DESCR_SRC for the details of bit fields
SAXI_DMAC_CH1_DESCR_DST	0x441A1158	Channel descriptor destination. See SAXI_DMAC_CH0_DESCR_DST for the details of bit fields
SAXI_DMAC_CH1_DESCR_M_SIZE	0x441A115C	Channel descriptor M size. See SAXI_DMAC_CH0_DESCR_M_SIZE for the details of bit fields
SAXI_DMAC_CH1_DESCR_X_SIZE	0x441A1160	Channel descriptor X size. See SAXI_DMAC_CH0_DESCR_X_SIZE for the details of bit fields
SAXI_DMAC_CH1_DESCR_X_INCR	0x441A1164	Channel descriptor X increment. See SAXI_DMAC_CH0_DESCR_X_INCR for the details of bit fields
SAXI_DMAC_CH1_DESCR_Y_SIZE	0x441A1168	Channel descriptor Y size. See SAXI_DMAC_CH0_DESCR_Y_SIZE for the details of bit fields
SAXI_DMAC_CH1_DESCR_Y_INCR	0x441A116C	Channel descriptor Y increment. See SAXI_DMAC_CH0_DESCR_Y_INCR for the details of bit fields
SAXI_DMAC_CH1_DESCR_NEXT	0x441A1170	Channel descriptor next pointer. See SAXI_DMAC_CH0_DESCR_NEXT for the details of bit fields
SAXI_DMAC_CH1_INTR	0x441A1180	Interrupt. See SAXI_DMAC_CH0_INTR for the details of bit fields
SAXI_DMAC_CH1_INTR_SET	0x441A1184	Interrupt set. See SAXI_DMAC_CH0_INTR_SET for the details of bit fields
SAXI_DMAC_CH1_INTR_MASK	0x441A1188	Interrupt mask. See SAXI_DMAC_CH0_INTR_MASK for the details of bit fields
SAXI_DMAC_CH1_INTR_MASKED	0x441A118C	Interrupt masked. See SAXI_DMAC_CH0_INTR_MASKED for the details of bit fields

High Performance Direct Memory Access (HPDMA) registers

Register name	Address	Description
SAXI_DMAC_CH2_CTL	0x441A1200	Channel control. See SAXI_DMAC_CH0_CTL for the details of bit fields
SAXI_DMAC_CH2_STATUS	0x441A1204	Channel status. See SAXI_DMAC_CH0_STATUS for the details of bit fields
SAXI_DMAC_CH2_IDX	0x441A1210	Channel current X and Y indices. See SAXI_DMAC_CH0_IDX for the details of bit fields
SAXI_DMAC_CH2_SRC	0x441A1214	Channel current source address. See SAXI_DMAC_CH0_SRC for the details of bit fields
SAXI_DMAC_CH2_DST	0x441A1218	Channel current destination address. See SAXI_DMAC_CH0_DST for the details of bit fields
SAXI_DMAC_CH2_M_IDX	0x441A121C	Channel current M index. See SAXI_DMAC_CH0_M_IDX for the details of bit fields
SAXI_DMAC_CH2_CURR	0x441A1220	Channel current descriptor pointer. See SAXI_DMAC_CH0_CURR for the details of bit fields
SAXI_DMAC_CH2_TR_CMD	0x441A1228	Channel software trigger. See SAXI_DMAC_CH0_TR_CMD for the details of bit fields
SAXI_DMAC_CH2_DESCR_STATUS	0x441A1240	Channel descriptor status. See SAXI_DMAC_CH0_DESCR_STATUS for the details of bit fields
SAXI_DMAC_CH2_DESCR_CTL	0x441A1250	Channel descriptor control. See SAXI_DMAC_CH0_DESCR_CTL for the details of bit fields
SAXI_DMAC_CH2_DESCR_SRC	0x441A1254	Channel descriptor source. See SAXI_DMAC_CH0_DESCR_SRC for the details of bit fields
SAXI_DMAC_CH2_DESCR_DST	0x441A1258	Channel descriptor destination. See SAXI_DMAC_CH0_DESCR_DST for the details of bit fields
SAXI_DMAC_CH2_DESCR_M_SIZE	0x441A125C	Channel descriptor M size. See SAXI_DMAC_CH0_DESCR_M_SIZE for the details of bit fields
SAXI_DMAC_CH2_DESCR_X_SIZE	0x441A1260	Channel descriptor X size. See SAXI_DMAC_CH0_DESCR_X_SIZE for the details of bit fields
SAXI_DMAC_CH2_DESCR_X_INCR	0x441A1264	Channel descriptor X increment. See SAXI_DMAC_CH0_DESCR_X_INCR for the details of bit fields
SAXI_DMAC_CH2_DESCR_Y_SIZE	0x441A1268	Channel descriptor Y size. See SAXI_DMAC_CH0_DESCR_Y_SIZE for the details of bit fields
SAXI_DMAC_CH2_DESCR_Y_INCR	0x441A126C	Channel descriptor Y increment. See SAXI_DMAC_CH0_DESCR_Y_INCR for the details of bit fields
SAXI_DMAC_CH2_DESCR_NEXT	0x441A1270	Channel descriptor next pointer. See SAXI_DMAC_CH0_DESCR_NEXT for the details of bit fields

High Performance Direct Memory Access (HPDMA) registers

Register name	Address	Description
SAXI_DMAC_CH2_INTR	0x441A1280	Interrupt. See SAXI_DMAC_CH0_INTR for the details of bit fields
SAXI_DMAC_CH2_INTR_SET	0x441A1284	Interrupt set. See SAXI_DMAC_CH0_INTR_SET for the details of bit fields
SAXI_DMAC_CH2_INTR_MASK	0x441A1288	Interrupt mask. See SAXI_DMAC_CH0_INTR_MASK for the details of bit fields
SAXI_DMAC_CH2_INTR_MASKED	0x441A128C	Interrupt masked. See SAXI_DMAC_CH0_INTR_MASKED for the details of bit fields
SAXI_DMAC_CH3_CTL	0x441A1300	Channel control. See SAXI_DMAC_CH0_CTL for the details of bit fields
SAXI_DMAC_CH3_STATUS	0x441A1304	Channel status. See SAXI_DMAC_CH0_STATUS for the details of bit fields
SAXI_DMAC_CH3_IDX	0x441A1310	Channel current X and Y indices. See SAXI_DMAC_CH0_IDX for the details of bit fields
SAXI_DMAC_CH3_SRC	0x441A1314	Channel current source address. See SAXI_DMAC_CH0_SRC for the details of bit fields
SAXI_DMAC_CH3_DST	0x441A1318	Channel current destination address. See SAXI_DMAC_CH0_DST for the details of bit fields
SAXI_DMAC_CH3_M_IDX	0x441A131C	Channel current M index. See SAXI_DMAC_CH0_M_IDX for the details of bit fields
SAXI_DMAC_CH3_CURR	0x441A1320	Channel current descriptor pointer. See SAXI_DMAC_CH0_CURR for the details of bit fields
SAXI_DMAC_CH3_TR_CMD	0x441A1328	Channel software trigger. See SAXI_DMAC_CH0_TR_CMD for the details of bit fields
SAXI_DMAC_CH3_DESCR_STATUS	0x441A1340	Channel descriptor status. See SAXI_DMAC_CH0_DESCR_STATUS for the details of bit fields
SAXI_DMAC_CH3_DESCR_CTL	0x441A1350	Channel descriptor control. See SAXI_DMAC_CH0_DESCR_CTL for the details of bit fields
SAXI_DMAC_CH3_DESCR_SRC	0x441A1354	Channel descriptor source. See SAXI_DMAC_CH0_DESCR_SRC for the details of bit fields
SAXI_DMAC_CH3_DESCR_DST	0x441A1358	Channel descriptor destination. See SAXI_DMAC_CH0_DESCR_DST for the details of bit fields
SAXI_DMAC_CH3_DESCR_M_SIZE	0x441A135C	Channel descriptor M size. See SAXI_DMAC_CH0_DESCR_M_SIZE for the details of bit fields
SAXI_DMAC_CH3_DESCR_X_SIZE	0x441A1360	Channel descriptor X size. See SAXI_DMAC_CH0_DESCR_X_SIZE for the details of bit fields
SAXI_DMAC_CH3_DESCR_X_INCR	0x441A1364	Channel descriptor X increment. See SAXI_DMAC_CH0_DESCR_X_INCR for the details of bit fields

High Performance Direct Memory Access (HPDMA) registers

Register name	Address	Description
SAXI_DMAC_CH3_DESCR_Y_SIZE	0x441A1368	Channel descriptor Y size. See SAXI_DMAC_CH0_DESCR_Y_SIZE for the details of bit fields
SAXI_DMAC_CH3_DESCR_Y_INCR	0x441A136C	Channel descriptor Y increment. See SAXI_DMAC_CH0_DESCR_Y_INCR for the details of bit fields
SAXI_DMAC_CH3_DESCR_NEXT	0x441A1370	Channel descriptor next pointer. See SAXI_DMAC_CH0_DESCR_NEXT for the details of bit fields
SAXI_DMAC_CH3_INTR	0x441A1380	Interrupt. See SAXI_DMAC_CH0_INTR for the details of bit fields
SAXI_DMAC_CH3_INTR_SET	0x441A1384	Interrupt set. See SAXI_DMAC_CH0_INTR_SET for the details of bit fields
SAXI_DMAC_CH3_INTR_MASK	0x441A1388	Interrupt mask. See SAXI_DMAC_CH0_INTR_MASK for the details of bit fields
SAXI_DMAC_CH3_INTR_MASKED	0x441A138C	Interrupt masked. See SAXI_DMAC_CH0_INTR_MASKED for the details of bit fields

7.1.1 SAXI_DMAC_CTL

Description: Control

Address: 0x441A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. Clearing this field to '0' by software shuts down all channels by clearing their CH_CTL.ENABLED fields, unless all CH_STATUS.ENABLED fields are '0'. After all channels have completed their AXI transactions, all non-retention registers (command and status registers) are reset to their default value, and all retention registers retain their value. '1': Enabled. Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**

7.1.2 SAXI_DMAC_STATUS

Description: Enabled channels

Address: 0x441A0004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				CH_EN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	CH_EN	Specifies channels whose CH_STATUS.ENABLED = '1', i.e. channels that are either enabled, or are still completing their AXI transactions after being disabled. Default Value: 0

7.1.3 SAXI_DMAC_ACTIVE

Description: Active channels

Address: 0x441A0008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				ACTIVE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	ACTIVE	Specifies active channels; i.e. enabled channels whose trigger got activated. Default Value: 0

7.1.4 SAXI_DMAC_CH0_CTL

Description: Channel control

Address: 0x441A1000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				Reserved	RW	RW	RW
HW Access	R				Reserved	R	R	R
Name	PC [7:4]				Reserved	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	RW1C	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	Channel enable: '0': Disabled. The channel's trigger is ignored and the channel cannot be made active. If an active channel is disabled, the channel is de-activated: This field is set to '0' immediately, and CH_STATUS.ENABLED is set to '0' by HW after AXI bus transactions are completed. '1': Enabled. SW sets this field to '1' to enable a specific channel. HW sets this field to '0' in the following cases: - when an error interrupt cause is activated - when a descriptor has completed, if CH_DESCR_CTL.CH_DISABLE is '1' - when CTL.ENABLED is cleared to '0' by SW while the CH_STATUS.ENABLED field of at least one channel is '1' Default Value: 0
9 : 8	PRIO	Channel priority: "0": highest priority. "1" "2" "3": lowest priority. Channels with the same priority constitute a priority group. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority group with pending channels is identified. Second, within this priority group, roundrobin arbitration is applied. Roundrobin arbitration (within a priority group) gives the highest priority to the lower channel indices (within the priority group). Default Value: 0

7.1.4 SAXI_DMAC_CH0_CTL (continued)

7 : 4	PC	Protection Context This field can only be updated based on software write to this register. However, value of this field is set with the protection context of the transaction that writes this register; i.e. the 'write data' is ignored and instead the context is inherited from the write transaction All transactions for this channel uses the PC field for the protection context. Note: This is an exception as compared to other Registers, where the field value is inherited from the bus, instead of 'write data'. Default Value: 0
2	B	Non-bufferable/bufferable access control: '0': non-bufferable. '1': bufferable. This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data. All transactions for this channel uses the B field for the non-bufferable/bufferable access control ("acache[0]"). Default Value: 0
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field can only be updated based on software write to this register. However, value of this field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction ("hnonsec") All transactions for this channel use the NS field for the secure/non-secure access control ("aprot[1]"). Note: This is an exception as compared to other registers, where the field value is inherited from the bus, instead of 'write data'. Default Value: 1
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field can only be updated based on software write to this register. However, value of this field is set with the user/privileged access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction ("hprot[1]") All transactions for this channel use the P field for the user/privileged access control ("aprot[0]"). Note: This is an exception as compared to other registers, where the field value is inherited from the bus, instead of 'write data'. Default Value: 0

7.1.5 SAXI_DMAC_CH0_STATUS

Description: Channel status

Address: 0x441A1004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	Indicates the enable status of the channel. '0': Disabled. '1': Enabled. When CH_CTL.ENABLED is set to '0' by SW or by the activation of an error interrupt cause or by disabling the entire DMAC, HW sets this field to '0' after the channel has completed AXI transactions. When SW sets CH_CTL.ENABLED to '1' and this field is '0', it changes from '0' to '1' immediately (if the entire DMAC is still disabled by CTL.ENABLED, it changes from '0' to '1' after the DMAC gets enabled). If this field is '1' at the time CH_CTL_ENABLED is changed from '0' to '1', then this field is first set to '0' by HW after the channel has completed AXI transactions, and it is set to '1' after one clock cycle if CH_CTL.ENABLED is still '1'. This ensures that the channel is properly initialized (except the retained registers). Default Value: 0

7.1.6 SAXI_DMAC_CH0_IDX

Description: Channel current X and Y indices

Address: 0x441A1010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	X [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	Y [31:24]							

Bits	Name	Description
31 : 16	Y	Specifies the Y loop index. In the range of [0, Y_COUNT], with Y_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it loads a descriptor.. Default Value: Undefined
15 : 0	X	Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it loads a descriptor. Default Value: Undefined

7.1.7 SAXI_DMAC_CH0_SRC

Description: Channel current source address

Address: 0x441A1014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Current address of source location. Default Value: Undefined

7.1.8 SAXI_DMAC_CH0_DST

Description: Channel current destination address

Address: 0x441A1018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Current address of destination location. Default Value: Undefined

7.1.9 SAXI_DMAC_CH0_M_IDX

Description: Channel current M index

Address: 0x441A101C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	M [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 0	M	Specifies the M loop index. In the range of [0, M_COUNT], with M_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it loads a descriptor. Default Value: Undefined

7.1.10 SAXI_DMAC_CH0_CURR

Description: Channel current descriptor pointer

Address: 0x441A1020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					Reserved		
HW Access	RW					Reserved		
Name	PTR [7:3]					Reserved [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PTR [31:24]							

Bits	Name	Description
31 : 3	PTR	Address of current descriptor. When this field is "0", there is no valid descriptor. Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: When this field is "0", and the DMAC and the channel are enabled, and the channel is triggered, then this will raise the CURR_PTR_NULL interrupt, and initiate the disabling of the channel. If this field is changed to a value different from "0" afterwards, then the channel may start to fetch the descriptor before finally being disabled, and the ISR will find this field not being "0" although the CURR_PTR_NULL interrupt has been raised. Default Value: Undefined

7.1.11 SAXI_DMAC_CH0_TR_CMD

Description: Channel software trigger

Address: 0x441A1028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							ACTIVATE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	ACTIVATE	Software trigger. When written with '1', a trigger is generated which sets 'trigger pending' (only if the channel is enabled). A read always returns a 0. Default Value: 0

7.1.12 SAXI_DMAC_CH0_DESCR_STATUS

Description: Channel descriptor status

Address: 0x441A1040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	VALID	Reserved [30:24]						

Bits	Name	Description
31	VALID	Indicates whether the descriptor information present in DESCR_CTL, DESCR_SRC, DESCR_DST, DESCR_M_SIZE, DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE, DESCR_Y_INCR, DESCR_NEXT status registers is valid or not. 0: Valid 1: Not Valid Default Value: 0

7.1.13 SAXI_DMAC_CH0_DESCR_CTL

Description: Channel descriptor control

Address: 0x441A1050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	TR_IN_TYPE [7:6]		TR_OUT_TYPE [5:4]		INTR_TYPE [3:2]		WAIT_FOR_DEACT [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							DATA_PRE FETCH

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R		Reserved			R
HW Access	Reserved		W		Reserved			W
Name	Reserved [31:30]		DESCR_TYPE [29:28]		Reserved [27:25]			CH_DIS- ABLE

Bits	Name	Description
29 : 28	DESCR_TYPE	Default Value: Undefined
24	CH_DISABLE	Default Value: Undefined
8	DATA_PREFETCH	Default Value: Undefined
7 : 6	TR_IN_TYPE	Default Value: Undefined
5 : 4	TR_OUT_TYPE	Default Value: Undefined
3 : 2	INTR_TYPE	Default Value: Undefined
1 : 0	WAIT_FOR_DEACT	Default Value: Undefined

7.1.14 SAXI_DMAC_CH0_DESCR_SRC

Description: Channel descriptor source

Address: 0x441A1054

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Default Value: Undefined

7.1.15 SAXI_DMAC_CH0_DESCR_DST

Description: Channel descriptor destination

Address: 0x441A1058

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Default Value: Undefined

7.1.16 SAXI_DMAC_CH0_DESCR_M_SIZE

Description: Channel descriptor M size

Address: 0x441A105C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	M_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	M_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	M_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 0	M_COUNT	Default Value: Undefined

7.1.17 SAXI_DMAC_CH0_DESCR_X_SIZE

Description: Channel descriptor X size

Address: 0x441A1060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	X_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	X_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	X_COUNT	Default Value: Undefined

7.1.18 SAXI_DMAC_CH0_DESCR_X_INCR

Description: Channel descriptor X increment

Address: 0x441A1064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_X [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_X [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_X [31:24]							

Bits	Name	Description
31 : 16	DST_X	Default Value: Undefined
15 : 0	SRC_X	Default Value: Undefined

7.1.19 SAXI_DMAC_CH0_DESCR_Y_SIZE

Description: Channel descriptor Y size

Address: 0x441A1068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	Y_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	Y_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	Y_COUNT	Default Value: Undefined

7.1.20 SAXI_DMAC_CH0_DESCR_Y_INCR

Description: Channel descriptor Y increment

Address: 0x441A106C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_Y [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_Y [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_Y [31:24]							

Bits	Name	Description
31 : 16	DST_Y	Default Value: Undefined
15 : 0	SRC_Y	Default Value: Undefined

7.1.21 SAXI_DMAC_CH0_DESCR_NEXT

Description: Channel descriptor next pointer

Address: 0x441A1070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R					Reserved		
HW Access	W					Reserved		
Name	PTR [7:3]					Reserved [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	PTR [31:24]							

Bits	Name	Description
31 : 3	PTR	Default Value: Undefined

7.1.22 SAXI_DMAC_CH0_INTR

Description: Interrupt

Address: 0x441A1080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	Reserved	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	Reserved	RW1S	RW1S	RW1S	RW1S
Name	DE-SCR_BUS_ERROR	AC-TIVE_CH_-DISABLED	CUR-R_PTR_NULL	Reserved	INVALID_-DESCR_-TYPE	DST_BUS_ERROR	SRC_BUS_ERROR	COMPLE-TION

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Activated (set to '1') on a bus error for a load of the descriptor. Default Value: 0
6	ACTIVE_CH_DISABLED	Activated (set to '1') when the channel is disabled and the data transfer engine is busy, i.e there is a pending trigger. This flag is also set if an input trigger is received at the same time another error occurs (in this case, ACT_CH_DISABLED is set in addition to another error interrupt flag). Default Value: 0
5	CURR_PTR_NULL	Activated (set to '1') when the channel is enabled (CH_CTL.ENABLED is '1'), CH_CURR_PTR is "0", and the channel is triggered. Default Value: 0
3	INVALID_DESCR_TYPE	Activated (set to '1') when the descriptor type is invalid. Default Value: 0
2	DST_BUS_ERROR	Activated (set to '1') on a bus error for a store to the destination. Also activated when an AXI write response is received although there is no outstanding write transaction. Default Value: 0
1	SRC_BUS_ERROR	Activated (set to '1') on a bus error for a load from the source. Note that INTR.COMPLETION is not valid if it is activated along with INTR.SRC_BUS_ERROR. When INTR.SRC_BUS_ERROR status is activated, then destination data may be corrupted. Default Value: 0

7.1.22 SAXI_DMAC_CH0_INTR (continued)

0	COMPLETION	Activated (set to '1') on completion of data transfer(s) as specified by the descriptor's CH_DESCR_CTL.INTR_TYPE. Note that this flag is not valid if it is activated along with INTR.SRC_BUS_ERROR. In this case destination data corresponding to this completion flag may be corrupted. Default Value: 0

7.1.23 SAXI_DMAC_CH0_INTR_SET

Description: Interrupt set

Address: 0x441A1084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	Reserved	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	Reserved	A	A	A	A
Name	DE-SCR_BUS_ ERROR	AC-TIVE_CH_-DISABLED	CUR-R_PTR_NU LL	Reserved	INVALID_-DESCR_-TYPE	DST_BUS_ ERROR	SRC_BUS_ ERROR	COMPLE-TION

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Default Value: 0
6	ACTIVE_CH_DISABLED	Default Value: 0
5	CURR_PTR_NULL	Default Value: 0
3	INVALID_DESCR_TYPE	Default Value: 0
2	DST_BUS_ERROR	Default Value: 0
1	SRC_BUS_ERROR	Default Value: 0
0	COMPLETION	Write this field with '1' to set corresponding INTR field to '1' (a write of '0' has no effect). Default Value: 0

7.1.24 SAXI_DMAC_CH0_INTR_MASK

Description: Interrupt mask

Address: 0x441A1088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	Reserved	RW	RW	RW	RW
HW Access	R	R	R	Reserved	R	R	R	R
Name	DE-SCR_BUS_ERROR	AC-TIVE_CH_-DISABLED	CUR-R_PTR_NULL	Reserved	INVALID_-DESCR_-TYPE	DST_BUS_ERROR	SRC_BUS_ERROR	COMPLE-TION

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Default Value: 0
6	ACTIVE_CH_DISABLED	Default Value: 0
5	CURR_PTR_NULL	Default Value: 0
3	INVALID_DESCR_TYPE	Default Value: 0
2	DST_BUS_ERROR	Default Value: 0
1	SRC_BUS_ERROR	Default Value: 0
0	COMPLETION	Mask for corresponding field in INTR register. Default Value: 0

7.1.25 SAXI_DMAC_CH0_INTR_MASKED

Description: Interrupt masked

Address: 0x441A108C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	Reserved	R	R	R	R
HW Access	W	W	W	Reserved	W	W	W	W
Name	DE-SCR_BUS_ ERROR	AC-TIVE_CH_- DISABLED	CUR-R_PTR_NU LL	Reserved	INVALID_- DESCR_- TYPE	DST_BUS_ ERROR	SRC_BUS_ ERROR	COMPLE-TION

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Default Value: 0
6	ACTIVE_CH_DISABLED	Default Value: 0
5	CURR_PTR_NULL	Default Value: 0
3	INVALID_DESCR_TYPE	Default Value: 0
2	DST_BUS_ERROR	Default Value: 0
1	SRC_BUS_ERROR	Default Value: 0
0	COMPLETION	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

8 Direct Memory Access (DMA) registers

This section discusses the DMA registers. It lists all the registers in mapping tables, in address order.

8.1 Register details

Register name	Address	Description
DW0_CTL	0x42270000	Control
DW0_STATUS	0x42270004	Status
DW0_ACT_DESCR_CTL	0x42270020	Active descriptor control
DW0_ACT_DESCR_SRC	0x42270024	Active descriptor source
DW0_ACT_DESCR_DST	0x42270028	Active descriptor destination
DW0_ACT_DESCR_X_CTL	0x42270030	Active descriptor X loop control
DW0_ACT_DESCR_Y_CTL	0x42270034	Active descriptor Y loop control
DW0_ACT_DESCR_NEXT_PTR	0x42270038	Active descriptor next pointer
DW0_ACT_SRC	0x42270040	Active source
DW0_ACT_DST	0x42270044	Active destination
DW0_CRC_CTL	0x42270100	CRC control
DW0_CRC_DATA_CTL	0x42270110	CRC data control
DW0_CRC_POL_CTL	0x42270120	CRC polynomial control
DW0_CRC_LFSR_CTL	0x42270130	CRC LFSR control
DW0_CRC_REM_CTL	0x42270140	CRC remainder control
DW0_CRC_REM_RESULT	0x42270148	CRC remainder result
DW0_CH_STRUCT0_CH_CTL	0x42278000	Channel control
DW0_CH_STRUCT0_CH_STATUS	0x42278004	Channel status
DW0_CH_STRUCT0_CH_IDX	0x42278008	Channel current indices
DW0_CH_STRUCT0_CH_CURR_PTR	0x4227800C	Channel current descriptor pointer
DW0_CH_STRUCT0_INTR	0x42278010	Interrupt
DW0_CH_STRUCT0_INTR_SET	0x42278014	Interrupt set
DW0_CH_STRUCT0_INTR_MASK	0x42278018	Interrupt mask
DW0_CH_STRUCT0_INTR_MASKED	0x4227801C	Interrupt masked
DW0_CH_STRUCT0_TR_CMD	0x42278028	Channel software trigger
DW0_CH_STRUCT1_CH_CTL	0x42278040	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT1_CH_STATUS	0x42278044	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT1_CH_IDX	0x42278048	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT1_CH_CURR_PTR	0x4227804C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT1_INTR	0x42278050	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT1_INTR_SET	0x42278054	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT1_INTR_MASK	0x42278058	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT1_INTR_MASKED	0x4227805C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT1_TR_CMD	0x42278068	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT2_CH_CTL	0x42278080	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT2_CH_STATUS	0x42278084	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT2_CH_IDX	0x42278088	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT2_CH_CURR_PTR	0x4227808C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT2_INTR	0x42278090	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT2_INTR_SET	0x42278094	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT2_INTR_MASK	0x42278098	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT2_INTR_MASKED	0x4227809C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT2_TR_CMD	0x422780A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT3_CH_CTL	0x422780C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT3_CH_STATUS	0x422780C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT3_CH_IDX	0x422780C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT3_CH_CURR_PTR	0x422780CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT3_INTR	0x422780D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT3_INTR_SET	0x422780D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT3_INTR_MASK	0x422780D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT3_INTR_MASKED	0x422780DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT3_TR_CMD	0x422780E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT4_CH_CTL	0x42278100	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT4_CH_STATUS	0x42278104	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT4_CH_IDX	0x42278108	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT4_CH_CURR_PTR	0x4227810C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT4_INTR	0x42278110	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT4_INTR_SET	0x42278114	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT4_INTR_MASK	0x42278118	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT4_INTR_MASKED	0x4227811C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT4_TR_CMD	0x42278128	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT5_CH_CTL	0x42278140	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT5_CH_STATUS	0x42278144	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT5_CH_IDX	0x42278148	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Direct Memory Access (DMA) registers

Register name	Address	Description
DW0_CH_STRUCT5_CH_CURR_PTR	0x4227814C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT5_INTR	0x42278150	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT5_INTR_SET	0x42278154	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT5_INTR_MASK	0x42278158	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT5_INTR_MASKED	0x4227815C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT5_TR_CMD	0x42278168	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT6_CH_CTL	0x42278180	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT6_CH_STATUS	0x42278184	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT6_CH_IDX	0x42278188	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT6_CH_CURR_PTR	0x4227818C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT6_INTR	0x42278190	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT6_INTR_SET	0x42278194	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT6_INTR_MASK	0x42278198	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT6_INTR_MASKED	0x4227819C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT6_TR_CMD	0x422781A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT7_CH_CTL	0x422781C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT7_CH_STATUS	0x422781C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT7_CH_IDX	0x422781C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT7_CH_CURR_PTR	0x422781CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT7_INTR	0x422781D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT7_INTR_SET	0x422781D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT7_INTR_MASK	0x422781D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT7_INTR_MASKED	0x422781DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT7_TR_CMD	0x422781E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT8_CH_CTL	0x42278200	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT8_CH_STATUS	0x42278204	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT8_CH_IDX	0x42278208	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT8_CH_CURR_PTR	0x4227820C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT8_INTR	0x42278210	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT8_INTR_SET	0x42278214	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT8_INTR_MASK	0x42278218	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT8_INTR_MASKED	0x4227821C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT8_TR_CMD	0x42278228	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT9_CH_CTL	0x42278240	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT9_CH_STATUS	0x42278244	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT9_CH_IDX	0x42278248	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Direct Memory Access (DMA) registers

Register name	Address	Description
DW0_CH_STRUCT9_CH_CURR_PTR	0x4227824C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT9_INTR	0x42278250	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT9_INTR_SET	0x42278254	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT9_INTR_MASK	0x42278258	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT9_INTR_MASKED	0x4227825C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT9_TR_CMD	0x42278268	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT10_CH_CTL	0x42278280	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT10_CH_STATUS	0x42278284	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT10_CH_IDX	0x42278288	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT10_CH_CURR_PTR	0x4227828C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT10_INTR	0x42278290	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT10_INTR_SET	0x42278294	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT10_INTR_MASK	0x42278298	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT10_INTR_MASKED	0x4227829C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT10_TR_CMD	0x422782A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT11_CH_CTL	0x422782C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT11_CH_STATUS	0x422782C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT11_CH_IDX	0x422782C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Direct Memory Access (DMA) registers

Register name	Address	Description
DW0_CH_STRUCT11_CH_CURR_PTR	0x422782CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT11_INTR	0x422782D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT11_INTR_SET	0x422782D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT11_INTR_MASK	0x422782D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT11_INTR_MASKED	0x422782DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT11_TR_CMD	0x422782E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT12_CH_CTL	0x42278300	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT12_CH_STATUS	0x42278304	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT12_CH_IDX	0x42278308	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT12_CH_CURR_PTR	0x4227830C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT12_INTR	0x42278310	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT12_INTR_SET	0x42278314	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT12_INTR_MASK	0x42278318	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT12_INTR_MASKED	0x4227831C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT12_TR_CMD	0x42278328	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT13_CH_CTL	0x42278340	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT13_CH_STATUS	0x42278344	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT13_CH_IDX	0x42278348	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Direct Memory Access (DMA) registers

Register name	Address	Description
DW0_CH_STRUCT13_CH_CURR_PTR	0x4227834C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT13_INTR	0x42278350	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT13_INTR_SET	0x42278354	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT13_INTR_MASK	0x42278358	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT13_INTR_MASKED	0x4227835C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT13_TR_CMD	0x42278368	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT14_CH_CTL	0x42278380	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT14_CH_STATUS	0x42278384	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT14_CH_IDX	0x42278388	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT14_CH_CURR_PTR	0x4227838C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT14_INTR	0x42278390	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT14_INTR_SET	0x42278394	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT14_INTR_MASK	0x42278398	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT14_INTR_MASKED	0x4227839C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT14_TR_CMD	0x422783A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT15_CH_CTL	0x422783C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT15_CH_STATUS	0x422783C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT15_CH_IDX	0x422783C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Direct Memory Access (DMA) registers

Register name	Address	Description
DW0_CH_STRUCT15_CH_CURR_PTR	0x422783CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT15_INTR	0x422783D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT15_INTR_SET	0x422783D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT15_INTR_MASK	0x422783D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT15_INTR_MASKED	0x422783DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT15_TR_CMD	0x422783E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.

8.1.1 DW0_CTL

Description: Control

Address: 0x42270000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. Disabling the IP activates the IP's Active logic reset: Active logic and non-retention MMIO registers are reset (retention MMIO registers are not affected). Note that DW SRAM writes/reads are possible when ENABLED=0 also. '1': Enabled. Default Value: 0

8.1.2 DW0_STATUS

Description: Status

Address: 0x42270004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved	R	R	R
HW Access	RW				Reserved	RW	RW	RW
Name	PC [7:4]				Reserved	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R	Reserved	R	
HW Access	Reserved				W	Reserved	W	
Name	Reserved [15:12]				PREEMPT-ABLE	Reserved	PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [23:17]							CH_IDX

Bits	31	30	29	28	27	26	25	24
SW Access	R	R			Reserved			
HW Access	W	W			Reserved			
Name	ACTIVE	STATE [30:28]			Reserved [27:24]			

Bits	Name	Description
31	ACTIVE	Active channel present: '0': No. '1': Yes. Default Value: 0
30 : 28	STATE	State of the DW controller. "0": Default/inactive state. "1": Loading descriptor. "2": Loading data element from source location. "3": Storing data element to destination location. "4": CRC functionality (only used for CRC transfer descriptor type). "5": Update of active control information (e.g. source and destination addresses) and wait for trigger de-activation. "6": Error. Default Value: 0
16	CH_IDX	Active channel index. Default Value: Undefined
11	PREEMPTABLE	Active channel preemptable. Default Value: Undefined
9 : 8	PRIO	Active channel priority. Default Value: Undefined
7 : 4	PC	Active channel protection context. Default Value: Undefined

8.1.2 DW0_STATUS (continued)

2	B	Active channel, non-bufferable/bufferable access control: '0': non-bufferable '1': bufferable. Default Value: Undefined
1	NS	Active channel, secure/non-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	Active channel, user/privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

8.1.3 DW0_ACT_DESCR_CTL

Description: Active descriptor control

Address: 0x42270020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description

8.1.3 DW0_ACT_DESCR_CTL (continued)

31 : 0	DATA	Copy of DESCR_CTL of the currently active descriptor. [1:0] WAIT_FOR_DEACT Specifies whether the controller should wait for the input trigger to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller with the agent that generated the trigger. This field is ONLY used at the completion of the transfer as specified by TR_IN. E.g., a TX FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the controller AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW controller performance. "0": Do not wait for trigger de-activation (for pulse sensitive triggers). "1": Wait for up to 4 cycles. "2": Wait for up to 16 cycles. "3": Wait indefinitely. This option may result in controller lockup if the trigger is not de-activated. [3:2] INTR_TYPE Specifies the input trigger type (not to be confused with the descriptor type): "0": A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. "1": A trigger results in the execution of a single 1D transfer. - If the descriptor type is "single", the trigger results in the execution of a single transfer. - If the descriptor type is "1D" or "2D", the trigger results in the execution of a 1D transfer. "2": A trigger results in the execution of the current descriptor. "3": A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. [5:4] TR_OUT_TYPE Specifies when an output trigger is generated: "0": An output trigger is generated after a single transfer. "1": An output trigger is generated after a single 1D transfer. - If the descriptor type is "single", the output trigger is generated after a single transfer. - If the descriptor type is "1D", "CRC" or "2D", the output trigger is generated after the execution of a 1D transfer. "2": An output trigger is generated after the execution of the current descriptor. "3": An output trigger is generated after the execution of a descriptor list: after the execution of the current descriptor AND the current descriptor DESCR_NEXT_PTR.ADDR is '0'. [7:6] TR_IN_TYPE Specifies the input trigger type (not to be confused with the descriptor type): "0": A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. "1": A trigger results in the execution of a single 1D transfer. - If the descriptor type is "single", the trigger results in the execution of a single transfer. - If the descriptor type is "1D" or "2D", the trigger results in the execution of a 1D transfer. "2": A trigger results in the execution of the current descriptor. "3": A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. [24] CH_DISABLE Specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the DESCR_NEXT_PTR value): '0': Channel is not disabled. '1': Channel is disabled. Note: a disabled channel will ignore its input trigger. [26] SRC_TRANSFER_SIZE Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. [27] DST_TRANSFER_SIZE Specifies the bus transfer size to the destination location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. [29:28] DATA_SIZE Specifies the data element size: "0": Byte (8 bits). "1": Halfword (16 bits). "2": Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit. - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit. - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made "0"). - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made "0"). - DATA is 16 bit, SRC is 16 bit, DST is 16 bit. - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit. - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made "0"). - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made "0"). - DATA is 32 bit, SRC is 32 bit, DST is 32 bit. [31:30] DESCR_TYPE Specifies the descriptor type (not to be confused with the trigger type): "0": Single transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are not present and DESCR_NEXT_PTR is at offset 0x0c. "1": 1D transfer. The DESCR_X_CTL register is present, the DESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A 1D transfer consists out of DESCR_X_CTL.X_COUNT single transfers. "2": 2D transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are present and DESCR_NEXT_PTR is at offset 0x14. A 2D transfer consists of DESCR_X_CTL.X_COUNT*DESCR_Y_CTL.Y_COUNT single transfers. "3": CRC transfer. The DESCR_X_CTL register is present, theDESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A CRC transfer consists out of DESCR_X_CTL.X_COUNT single transfers. After the execution of the current descriptor, the DESCR_NEXT_PTR address is copied to the channel's CH_CURR_PTR address and CH_STATUS.X_IDX and CH_STATUS.Y_IDX are set to "0". Default Value: Undefined

8.1.4 DW0_ACT_DESCR_SRC

Description: Active descriptor source

Address: 0x42270024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_SRC of the currently active descriptor. Base address of source location. Default Value: Undefined

8.1.5 DW0_ACT_DESCR_DST

Description: Active descriptor destination

Address: 0x42270028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_DST of the currently active descriptor. Base address of destination location. Note: For a CRC transfer descriptor, this field should be programmed with the address of the CRC_LFSR_CTL register. The calculated CRC LFSR state is written to this address (through the CRYPTO AHB-Lite master interface) when the input trigger is processed. The write transfer will be submitted to the CPUSS and PERI protection schemes. Default Value: Undefined

8.1.6 DW0_ACT_DESCR_X_CTL

Description: Active descriptor X loop control

Address: 0x42270030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_X_CTL of the currently active descriptor. [11:0] SRC_X_INCR Specifies increment of source address for each X loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is "0", the source address is not incremented. This is useful for reading from RX FIFO structures. [23:12] DST_X_INCR Specifies increment of destination address for each X loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is "0", the destination address is not incremented. This is useful for writing to TX FIFO structures. Note: this field is not used for CRC transfer descriptors and must be set to "0". [31:24] X_COUNT Number of iterations (minus 1) of the "X loop" (X_COUNT+1 is the number of single transfers in a 1D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations. For a single transfer descriptor type, descriptor will not have X_CTL. Default Value: Undefined

8.1.7 DW0_ACT_DESCR_Y_CTL

Description: Active descriptor Y loop control

Address: 0x42270034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_Y_CTL of the currently active descriptor. [11:0] SRC_Y_INCR Specifies increment of source address for each Y loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. [23:12] DST_Y_INCR Specifies increment of destination address for each Y loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. [31:24] Y_COUNT Number of iterations (minus 1) of the "Y loop" (X_COUNT+1)*(Y_COUNT+1) is the number of single transfers in a 2D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations. For single, 1D and CRC transfer descriptor types, descriptor will not have Y_CTL. Default Value: Undefined

8.1.8 DW0_ACT_DESCR_NEXT_PTR

Description: Active descriptor next pointer

Address: 0x42270038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						Reserved	
HW Access	W						Reserved	
Name	ADDR [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 2	ADDR	Copy of DESCR_NEXT_PTR of the currently active descriptor. [31:2] ADDR Address of next descriptor in descriptor list. When this field is "0", this is the last descriptor in the descriptor list. Default Value: Undefined

8.1.9 DW0_ACT_SRC

Description: Active source

Address: 0x42270040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SRC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SRC_ADDR [31:24]							

Bits	Name	Description
31 : 0	SRC_ADDR	Current address of source location. Default Value: Undefined

8.1.10 DW0_ACT_DST

Description: Active destination

Address: 0x42270044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DST_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DST_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_ADDR [31:24]							

Bits	Name	Description
31 : 0	DST_ADDR	Current address of destination location. Default Value: Undefined

8.1.11 DW0_CRC_CTL

Description: CRC control

Address: 0x42270100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							DATA_REVERSE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							REM_REVERSE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	REM_REVERSE	Specifies whether the remainder is bit reversed (reversal is performed after XORing): '0': No. '1': Yes. Default Value: 0
0	DATA_REVERSE	Specifies the bit order in which a data Byte is processed (reversal is performed after XORing): '0': Most significant bit (bit 1) first. '1': Least significant bit (bit 0) first. Default Value: 0

8.1.12 DW0_CRC_DATA_CTL

Description: CRC data control

Address: 0x42270110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DATA_XOR	Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. Default Value: 0

8.1.13 DW0_CRC_POL_CTL

Description: CRC polynomial control

Address: 0x42270120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [31:24]							

Bits	Name	Description
31 : 0	POLYNOMIAL	CRC polynomial. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned/shifted such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials: - CRC32: POLYNOMIAL is 0x04c11db7 (x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1). - CRC16: POLYNOMIAL is 0x80050000 (x^16 + x^15 + x^2 + 1, shifted by 16 bit positions). - CRC16 CCITT: POLYNOMIAL is 0x10210000 (x^16 + x^12 + x^5 + 1, shifted by 16 bit positions). Default Value: 0

8.1.14 DW0_CRC_LFSR_CTL

Description: CRC LFSR control

Address: 0x42270130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description
31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value. The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's. Note that SW can write this field. This functionality can be used prevent information leakage (through either CRC_LFSR_CTL or CRC_REM_RESULT). Default Value: 0

8.1.15 DW0_CRC_REM_CTL

Description: CRC remainder control

Address: 0x42270140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REM_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REM_XOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	REM_XOR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	REM_XOR [31:24]							

Bits	Name	Description
31 : 0	REM_XOR	Specifies a mask with which the CRC_LFSR_CTL.LFSR32 register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. Default Value: 0

8.1.16 DW0_CRC_REM_RESULT

Description: CRC remainder result

Address: 0x42270148

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	REM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	REM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	REM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	REM [31:24]							

Bits	Name	Description
31 : 0	REM	Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE: '0': the more significant bits (bit 31 and down) contain the remainder. '1': the less significant bits (bit 0 and up) contain the remainder. Note: This field is combinatorially derived from CRC_LFSR_CTL.LFSR32, CRC_CTL.REM_REVERSE and CRC_REM_CTL.REM_XOR. Default Value: 0

8.1.17 DW0_CH_STRUCT0_CH_CTL

Description: Channel control

Address: 0x42278000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				Reserved	RW	RW	RW
HW Access	R				Reserved	R	R	R
Name	PC [7:4]				Reserved	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW	Reserved	RW	
HW Access	Reserved				R	Reserved	R	
Name	Reserved [15:12]				PREEMPT-ABLE	Reserved	PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	RW1C	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	Channel enable: '0': Disabled. The channel's trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed). '1': Enabled. SW sets this field to '1' to enable a specific channel. HW sets this field to '0' on an error interrupt cause (the specific error is specified by CH_STATUS.INTR_CAUSE). Default Value: 0
11	PREEMPTABLE	Specifies if the channel is preemptable. '0': Not preemptable. '1': Preemptable. This field allows higher priority pending channels (from a higher priority group; i.e. an active channel can NOT be preempted by a pending channel in the same priority group) to preempt the active channel in between "single transfers" (a 1D transfer consists out of X_COUNT single transfers; a 2D transfer consists out of X_COUNT*Y_COUNT single transfers). Preemption will NOT affect the pending status of channel. As a result, after completion of a higher priority activated channel, the current channel may be reactivated. Default Value: Undefined

8.1.17 DW0_CH_STRUCT0_CH_CTL (continued)

9 : 8	PRIO	Channel priority: "0": highest priority. "1" "2" "3": lowest priority. Channels with the same priority constitute a priority group. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority group with pending channels is identified. Second, within this priority group, round robin arbitration is applied. Round robin arbitration (within a priority group) gives the highest priority to the lower channel indices (within the priority group). Default Value: 0
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes this register; i.e. the 'write data' is ignored and instead the context is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel uses the PC field for the protection context. Note: protection context (PC) is routed on "hauser" bus of the AHB5 bus. Default Value: Undefined
2	B	Non-bufferable/bufferable access control: '0': non-bufferable. '1': bufferable. This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data. All transactions for this channel uses the B field for the non-bufferable/bufferable access control ("hprot[2]"). Default Value: Undefined
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the NS field for the secure/non-secure access control ("hnonsec"). Default Value: Undefined
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the P field for the user/privileged access control ("hprot[1]"). Default Value: Undefined

8.1.18 DW0_CH_STRUCT0_CH_STATUS

Description: Channel status

Address: 0x42278004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				INTR_CAUSE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	PENDING	Reserved [30:24]						

Bits	Name	Description
31	PENDING	Specifies pending DW channels; i.e. enabled channels whose trigger got activated. This field includes all channels that are in the pending state (not scheduled) or active state (scheduled and performing data transfer(s)). Default Value: 0
3 : 0	INTR_CAUSE	Specifies the source of the interrupt cause: "0": NO_INTR "1": COMPLETION "2": SRC_BUS_ERROR "3": DST_BUS_ERROR "4": SRC_MISAL "5": DST_MISAL "6": CURR_PTR_NULL "7": ACTIVE_CH_DISABLED "8": DESCR_BUS_ERROR "9"-"15": Not used. For error related interrupt causes (INTR_CAUSE is "2", "3", ..., "8"), the channel is disabled (HW sets CH_CTL.ENABLED to '0'). Default Value: Undefined

8.1.19 DW0_CH_STRUCT0_CH_IDX

Description: Channel current indices

Address: 0x42278008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	X_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	Y_IDX [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	Y_IDX	Specifies the Y loop index, with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to "0" when it updates CH_CURR_PTR. Default Value: Undefined
7 : 0	X_IDX	Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to "0" when it updates CH_CURR_PTR. Default Value: Undefined

8.1.20 DW0_CH_STRUCT0_CH_CURR_PTR

Description: Channel current descriptor pointer

Address: 0x4227800C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	
HW Access	RW						Reserved	
Name	ADDR [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 2	ADDR	Address of current descriptor. When this field is "0", there is no valid descriptor. Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: Typically, when SW updates the current descriptor pointer CH_CURR_PTR, it also sets CH_IDX.X_IDX and CH_IDX.Y_IDX to "0". Default Value: Undefined

8.1.21 DW0_CH_STRUCT0_INTR

Description: Interrupt

Address: 0x42278010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1C
HW Access	Reserved							RW1S
Name	Reserved [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CH	Set to '1', when event (as specified by CH_STATUS.INTR_CAUSE) is detected. Write INTR.CH field with '1', to clear bit. Write INTR_SET.CH field with '1', to set bit. Default Value: 0

8.1.22 DW0_CH_STRUCT0_INTR_SET

Description: Interrupt set

Address: 0x42278014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CH	Write INTR_SET field with '1' to set corresponding INTR.CH field (a write of '0' has no effect). Default Value: 0

8.1.23 DW0_CH_STRUCT0_INTR_MASK

Description: Interrupt mask

Address: 0x42278018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CH	Mask for corresponding field in INTR register. Default Value: 0

8.1.24 DW0_CH_STRUCT0_INTR_MASKED

Description: Interrupt masked

Address: 0x4227801C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CH	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

8.1.25 DW0_CH_STRUCT0_TR_CMD

Description: Channel software trigger

Address: 0x42278028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							ACTIVATE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	ACTIVATE	Software trigger. When written with '1', a trigger is generated which sets 'trigger pending' (only if the channel is enabled). A read always returns a 0. Default Value: 0

9 Trigger Multiplexer registers

This section discusses the Trigger Multiplexer registers. It lists all the registers in mapping tables, in address order.

9.1 Register details

Register name	Address	Description
PERI0_TIMEOUT_CTL	0x42000200	Timeout control
PERI0_TR_CMD	0x42002000	Trigger command
PERI0_INFRA_CLK_FORCE	0x42002004	Infrastructure clock force enable
PERI0_GR0_SL_CTL	0x42004010	Slave control
PERI0_GR0_SL_CTL2	0x42004014	Slave control2
PERI0_GR1_CLOCK_CTL	0x42004040	Clock control
PERI0_GR1_SL_CTL	0x42004050	Slave control
PERI0_GR1_SL_CTL2	0x42004054	Slave control2
PERI0_GR2_CLOCK_CTL	0x42004080	Clock control. See PERI0_GR1_CLOCK_CTL for the details of bit fields.
PERI0_GR2_SL_CTL	0x42004090	Slave control
PERI0_GR2_SL_CTL2	0x42004094	Slave control2
PERI0_GR3_CLOCK_CTL	0x420040C0	Clock control. See PERI0_GR1_CLOCK_CTL for the details of bit fields.
PERI0_GR3_SL_CTL	0x420040D0	Slave control
PERI0_GR3_SL_CTL2	0x420040D4	Slave control2
PERI0_GR4_SL_CTL	0x42004110	Slave control. See PERI0_GR3_SL_CTL for the details of bit fields.
PERI0_GR4_SL_CTL2	0x42004114	Slave control2. See PERI0_GR3_SL_CTL2 for the details of bit fields.
PERI0_GR5_CLOCK_CTL	0x42004140	Clock control. See PERI0_GR1_CLOCK_CTL for the details of bit fields.
PERI0_GR5_SL_CTL	0x42004150	Slave control. See PERI0_GR3_SL_CTL for the details of bit fields.
PERI0_GR5_SL_CTL2	0x42004154	Slave control2. See PERI0_GR3_SL_CTL2 for the details of bit fields.
PERI0_TR_GR0_TR_CTL0	0x42008000	Trigger control register
PERI0_TR_GR0_TR_CTL1	0x42008004	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL2	0x42008008	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL3	0x4200800C	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL4	0x42008010	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.

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PERI0_TR_GR0_TR_CTL5	0x42008014	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL6	0x42008018	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL7	0x4200801C	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL0	0x42008400	Trigger control register
PERI0_TR_GR1_TR_CTL1	0x42008404	Trigger control register. See PERI0_TR_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL0	0x42008800	Trigger control register
PERI0_TR_GR2_TR_CTL1	0x42008804	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL2	0x42008808	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL3	0x4200880C	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL4	0x42008810	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL5	0x42008814	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL6	0x42008818	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL7	0x4200881C	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL8	0x42008820	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL9	0x42008824	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL10	0x42008828	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL11	0x4200882C	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL12	0x42008830	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL13	0x42008834	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL14	0x42008838	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL15	0x4200883C	Trigger control register. See PERI0_TR_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_GR3_TR_CTL0	0x42008C00	Trigger control register. This is the starting address of a register bank containing 50 registers (PERI0_TR_GR3_TR_CTL0 to PERI0_TR_GR3_TR_CTL49).
PERI0_TR_GR4_TR_CTL0	0x42009000	Trigger control register

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PERI0_TR_GR4_TR_CTL1	0x42009004	Trigger control register. See PERI0_TR_GR4_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL0	0x42009400	Trigger control register
PERI0_TR_GR5_TR_CTL1	0x42009404	Trigger control register. See PERI0_TR_GR5_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL2	0x42009408	Trigger control register. See PERI0_TR_GR5_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL3	0x4200940C	Trigger control register. See PERI0_TR_GR5_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR0_TR_CTL0	0x4200C000	Trigger control register
PERI0_TR_1TO1_GR0_TR_CTL1	0x4200C004	Trigger control register. See PERI0_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR0_TR_CTL2	0x4200C008	Trigger control register. See PERI0_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR0_TR_CTL3	0x4200C00C	Trigger control register. See PERI0_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR0_TR_CTL4	0x4200C010	Trigger control register. See PERI0_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR0_TR_CTL5	0x4200C014	Trigger control register. See PERI0_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR0_TR_CTL6	0x4200C018	Trigger control register. See PERI0_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR0_TR_CTL7	0x4200C01C	Trigger control register. See PERI0_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI1_TIMEOUT_CTL	0x44000200	Timeout control. See PERI0_TIMEOUT_CTL for the details of bit fields.
PERI1_TR_CMD	0x44002000	Trigger command. See PERI0_TR_CMD for the details of bit fields.
PERI1_INFRA_CLK_FORCE	0x44002004	Infrastructure clock force enable. See PERI0_INFRA_CLK_FORCE for the details of bit fields.
PERI1_GR0_SL_CTL	0x44004010	Slave control
PERI1_GR0_SL_CTL2	0x44004014	Slave control2
PERI1_GR1_CLOCK_CTL	0x44004040	Clock control. See PERI0_GR1_CLOCK_CTL for the details of bit fields.
PERI1_GR1_SL_CTL	0x44004050	Slave control
PERI1_GR1_SL_CTL2	0x44004054	Slave control2
PERI1_GR2_SL_CTL	0x44004090	Slave control. See PERI0_GR2_SL_CTL for the details of bit fields.
PERI1_GR2_SL_CTL2	0x44004094	Slave control2. See PERI0_GR2_SL_CTL2 for the details of bit fields.
PERI1_GR3_CLOCK_CTL	0x440040C0	Clock control. See PERI0_GR1_CLOCK_CTL for the details of bit fields.
PERI1_GR3_SL_CTL	0x440040D0	Slave control

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PERI1_GR3_SL_CTL2	0x440040D4	Slave control2
PERI1_GR4_SL_CTL	0x44004110	Slave control. See PERI0_GR3_SL_CTL for the details of bit fields.
PERI1_GR4_SL_CTL2	0x44004114	Slave control2. See PERI0_GR3_SL_CTL2 for the details of bit fields.
PERI1_TR_GR0_TR_CTL0	0x44008000	Trigger control register
PERI1_TR_GR0_TR_CTL1	0x44008004	Trigger control register. See PERI1_TR_GR0_TR_CTL0 for the details of bit fields.
PERI1_TR_GR0_TR_CTL2	0x44008008	Trigger control register. See PERI1_TR_GR0_TR_CTL0 for the details of bit fields.
PERI1_TR_GR0_TR_CTL3	0x4400800C	Trigger control register. See PERI1_TR_GR0_TR_CTL0 for the details of bit fields.
PERI1_TR_GR0_TR_CTL4	0x44008010	Trigger control register. See PERI1_TR_GR0_TR_CTL0 for the details of bit fields.
PERI1_TR_GR0_TR_CTL5	0x44008014	Trigger control register. See PERI1_TR_GR0_TR_CTL0 for the details of bit fields.
PERI1_TR_GR1_TR_CTL0	0x44008400	Trigger control register
PERI1_TR_GR1_TR_CTL1	0x44008404	Trigger control register. See PERI1_TR_GR1_TR_CTL0 for the details of bit fields.
PERI1_TR_GR1_TR_CTL2	0x44008408	Trigger control register. See PERI1_TR_GR1_TR_CTL0 for the details of bit fields.
PERI1_TR_GR2_TR_CTL0	0x44008800	Trigger control register
PERI1_TR_GR2_TR_CTL1	0x44008804	Trigger control register. See PERI1_TR_GR2_TR_CTL0 for the details of bit fields.
PERI1_TR_GR2_TR_CTL2	0x44008808	Trigger control register. See PERI1_TR_GR2_TR_CTL0 for the details of bit fields.
PERI1_TR_GR2_TR_CTL3	0x4400880C	Trigger control register. See PERI1_TR_GR2_TR_CTL0 for the details of bit fields.
PERI1_TR_GR2_TR_CTL4	0x44008810	Trigger control register. See PERI1_TR_GR2_TR_CTL0 for the details of bit fields.
PERI1_TR_GR2_TR_CTL5	0x44008814	Trigger control register. See PERI1_TR_GR2_TR_CTL0 for the details of bit fields.

9.1.1 PERI0_TIMEOUT_CTL

Description: Timeout control

Address: 0x42000200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIMEOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIMEOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	HWRST_-DISABLE	Reserved [30:24]						

Bits	Name	Description
31	HWRST_DISABLE	This field provides control for HW to reset the slave that is causing the timeout to occur. 1 - no HW reset during timeout. 0 - HW resets the corresponding slave during timeout. This ensures the AHB bus not to be hung after a timeout has occurred. HW asserts the reset along with fault request (peri_gp'i'_mmio_timeout_vio_req) and holds it until fault acknowledge (mmio_peri_gp'i'_timeout_vio_ack) is received from centralized fault infrastructure. Note, SW needs to take care of the implication when clearing this bit when a HW reset has occurred as clearing this bit will cause HW reset de-assert. Note that peripheral group-0 slaves are excluded from timeout (Refer Timeout section in mxs-peri.1 BROS for more details). Default Value: 0
15 : 0	TIMEOUT	This field specifies a number of peripheral group root undivided (clk_group_root[i]) clock cycles. If an AHB-Lite bus transfer takes more than the specified number of cycles (timeout detection), the bus transfer is terminated with an AHB5 bus error and a timeout status is set. "0x0000"-"0xfffe": Number of peripheral group clock cycles. "0xffff": This value is the default/reset value and specifies that no timeout detection is performed: a bus transfer will never be terminated, and a interrupt will never be generated. Note that TIMEOUT_CTL.TIMEOUT[15:0] in clk_pclk0_root (clk_hf0) is used directly in peripheral group clock domain clk_group_root[i], even if clk_group_root[i] is async to clk_pclk0_root. This is on the assumption that this register is programmed once by SW, remain constant. Following SW programming restrictions apply to TIMEOUT_CTL.TIMEOUT[15:0]. SW should make sure that no other AHB transactions are initiated through PERI before programming this register. SW should make sure that write to TIMEOUT_CTL.TIMEOUT[15:0] is completed by doing a readback. Note that peripheral group-0 slaves are excluded from timeout (Refer Timeout section in mxs-peri.1 BROS for more details). Default Value: 0xFFFF

9.1.2 PERI0_TR_CMD

Description: Trigger command

Address: 0x42002000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			GROUP_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	Reserved				
HW Access	RW1C	R	R	Reserved				
Name	ACTIVATE	OUT_SEL	TR_EDGE	Reserved [28:24]				

Bits	Name	Description
31	ACTIVATE	SW sets this field to '1' to activate (set to '1') a trigger as identified by TR_SEL, TR_EDGE and OUT_SEL. HW sets this field to '0' for edge sensitive triggers AFTER the selected trigger is activated for two clk_peri cycles. Note: when ACTIVATE is '1', SW should not modify the other register fields. SW MUST NOT set ACTIVATE bit to '1' while updating the other register bits simultaneously. At first the SW MUST update the other register bits as needed, and then set ACTIVATE to '1' with a new register write. Default Value: 0
30	OUT_SEL	Specifies whether trigger activation is for a specific input or output trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_CTL.TR_SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer. Note: this field is not used for trigger 1-to-1 groups. Default Value: 0
29	TR_EDGE	Specifies if the activated trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. The trigger reflects TR_CMD.ACTIVATE. '1': edge sensitive trigger. The trigger is activated for two clk_peri cycles. Default Value: 0
12 : 8	GROUP_SEL	Specifies the trigger group: "0"-"15": trigger multiplexer groups. "16"-"31": trigger 1-to-1 groups. Default Value: 0

9.1.2 PERI0_TR_CMD (continued)

7 : 0	TR_SEL	Specifies the activated trigger when ACTIVATE is '1'. If the specified trigger is not present, the trigger activation has no effect. Default Value: 0

9.1.3 PERI0_INFRA_CLK_FORCE

Description: Infrastructure clock force enable

Address: 0x42002004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	ENABLED	Infrastructure clock force enable. 0: Disabled 1: Enabled Default Value: 0

9.1.4 PERI0_GR0_SL_CTL

Description: Slave control

Address: 0x42004010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						ENABLED [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Refer to the section "Peripheral Interconnect" within the "Bus Infrastructure" chapter of the PSOC™ Edge E8x2/E8x3/E8x5/E8x6 MCU architecture reference manual for the mapping between the SL_CTL.ENABLED bits and the MMIO slaves. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 1023

9.1.5 PERI0_GR0_SL_CTL2

Description: Slave control2

Address: 0x42004014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						RST [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

9.1.6 PERI0_GR1_CLOCK_CTL

Description: Clock control

Address: 0x42004040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Specifies a group clock divider (from the peripheral clock "clk_peri" to the group clock "clk_group[1/2/3/4/5/...15]"). Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

9.1.7 PERI0_GR1_SL_CTL

Description: Slave control

Address: 0x42004050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ENABLED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [23:18]						ENABLED [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Refer to the section "Peripheral Interconnect" within the "Bus Infrastructure" chapter of the PSOC™ Edge E8x2/E8x3/E8x5/E8x6 MCU architecture reference manual for the mapping between the SL_CTL.ENABLED bits and the MMIO slaves. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 0

9.1.8 PERI0_GR1_SL_CTL2

Description: Slave control2

Address: 0x42004054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RST [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [23:18]						RST [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

9.1.9 PERI0_GR2_SL_CTL

Description: Slave control

Address: 0x42004090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						ENABLED [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Refer to the section "Peripheral Interconnect" within the "Bus Infrastructure" chapter of the PSOC™ Edge E8x2/E8x3/E8x5/E8x6 MCU architecture reference manual for the mapping between the SL_CTL.ENABLED bits and the MMIO slaves. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 0

9.1.10 PERI0_GR2_SL_CTL2

Description: Slave control2

Address: 0x42004094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						RST [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

9.1.11 PERI0_GR3_SL_CTL

Description: Slave control

Address: 0x420040D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Refer to the section "Peripheral Interconnect" within the "Bus Infrastructure" chapter of the PSOC™ Edge E8x2/E8x3/E8x5/E8x6 MCU architecture reference manual for the mapping between the SL_CTL.ENABLED bits and the MMIO slaves. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 0

9.1.12 PERI0_GR3_SL_CTL2

Description: Slave control2

Address: 0x420040D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							RST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

9.1.13 PERI0_TR_GR0_TR_CTL0

Description: Trigger control register

Address: 0x42008000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved		RW	RW
HW Access	Reserved			R	Reserved		R	R
Name	Reserved [15:13]			DBG_-FREEZE_EN	Reserved [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

9.1.14 PERI0_TR_GR1_TR_CTL0

Description: Trigger control register

Address: 0x42008400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						TR_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved		RW	RW
HW Access	Reserved			R	Reserved		R	R
Name	Reserved [15:13]			DBG_-FREEZE_EN	Reserved [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
1 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

9.1.15 PERI0_TR_GR2_TR_CTL0

Description: Trigger control register

Address: 0x42008800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved		RW	RW
HW Access	Reserved			R	Reserved		R	R
Name	Reserved [15:13]			DBG_-FREEZE_EN	Reserved [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

9.1.16 PERI0_TR_GR3_TR_CTL0

Description: Trigger control register

Address: 0x42008C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			
HW Access	Reserved			R	Reserved			
Name	Reserved [15:13]			DBG_-FREEZE_EN	Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

9.1.17 PERI0_TR_GR4_TR_CTL0

Description: Trigger control register

Address: 0x42009000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:3]						TR_SEL [2:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved		RW	RW
HW Access	Reserved			R	Reserved		R	R
Name	Reserved [15:13]			DBG_-FREEZE_EN	Reserved [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
2 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

9.1.18 PERI0_TR_GR5_TR_CTL0

Description: Trigger control register

Address: 0x42009400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved		RW	RW
HW Access	Reserved			R	Reserved		R	R
Name	Reserved [15:13]			DBG_-FREEZE_EN	Reserved [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

9.1.19 PERI0_TR_1TO1_GR0_TR_CTL0

Description: Trigger control register

Address: 0x4200C000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved		RW	RW
HW Access	Reserved			R	Reserved		R	R
Name	Reserved [15:13]			DBG_-FREEZE_EN	Reserved [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

9.1.20 PERI1_GR0_SL_CTL

Description: Slave control

Address: 0x44004010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				ENABLED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Refer to the section "Peripheral Interconnect" within the "Bus Infrastructure" chapter of the PSOC™ Edge E8x2/E8x3/E8x5/E8x6 MCU architecture reference manual for the mapping between the SL_CTL.ENABLED bits and the MMIO slaves. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 15

9.1.21 PERI1_GR0_SL_CTL2

Description: Slave control2

Address: 0x44004014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				RST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

9.1.22 PERI1_GR1_SL_CTL

Description: Slave control

Address: 0x44004050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				ENABLED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Refer to the section "Peripheral Interconnect" within the "Bus Infrastructure" chapter of the PSOC™ Edge E8x2/E8x3/E8x5/E8x6 MCU architecture reference manual for the mapping between the SL_CTL.ENABLED bits and the MMIO slaves. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 0

9.1.23 PERI1_GR3_SL_CTL

Description: Slave control

Address: 0x440040D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		ENABLED [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Refer to the section "Peripheral Interconnect" within the "Bus Infrastructure" chapter of the PSOC™ Edge E8x2/E8x3/E8x5/E8x6 MCU architecture reference manual for the mapping between the SL_CTL.ENABLED bits and the MMIO slaves. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 0

9.1.24 PERI1_GR3_SL_CTL2

Description: Slave control2

Address: 0x440040D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		RST [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

9.1.25 PERI1_TR_GR1_TR_CTL0

Description: Trigger control register

Address: 0x44008400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						TR_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved		RW	RW
HW Access	Reserved			R	Reserved		R	R
Name	Reserved [15:13]			DBG_-FREEZE_EN	Reserved [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
1 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

9.1.26 PERI1_TR_GR2_TR_CTL0

Description: Trigger control register

Address: 0x44008800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved		RW	RW
HW Access	Reserved			R	Reserved		R	R
Name	Reserved [15:13]			DBG_-FREEZE_EN	Reserved [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
6 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10 Program and Debug Interface registers

This section discusses the Program and Debug Interface registers. It lists all the registers in mapping tables, in address order.

10.1 Register details

Register name	Address	Description
DEBUG600_VERSION	0x42430000	IP Version Information
CM33_SCS_ICTR	0xE000E004	Interrupt Controller Type Register
CM33_SCS_ACTLR	0xE000E008	Auxiliary Control Register
CM33_SCS_SYST_CSR	0xE000E010	SysTick Control and Status Register
CM33_SCS_SYST_RVR	0xE000E014	SysTick Reload Value Register
CM33_SCS_SYST_CVR	0xE000E018	SysTick Current Value Register
CM33_SCS_SYST_CALIB	0xE000E01C	SysTick Calibration value Register
CM33_SCS_NVIC_ISER0	0xE000E100	Interrupt Set-Enable Registers
CM33_SCS_NVIC_ISER1	0xE000E104	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER2	0xE000E108	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER3	0xE000E10C	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER4	0xE000E110	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER5	0xE000E114	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER6	0xE000E118	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER7	0xE000E11C	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER8	0xE000E120	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER9	0xE000E124	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER10	0xE000E128	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER11	0xE000E12C	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER12	0xE000E130	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER13	0xE000E134	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.

Program and Debug Interface registers

Register name	Address	Description
CM33_SCS_NVIC_ISER14	0xE000E138	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER15	0xE000E13C	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ICER0	0xE000E180	Interrupt Clear-Enable Registers
CM33_SCS_NVIC_ICER1	0xE000E184	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER2	0xE000E188	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER3	0xE000E18C	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER4	0xE000E190	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER5	0xE000E194	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER6	0xE000E198	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER7	0xE000E19C	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER8	0xE000E1A0	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER9	0xE000E1A4	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER10	0xE000E1A8	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER11	0xE000E1AC	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER12	0xE000E1B0	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER13	0xE000E1B4	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER14	0xE000E1B8	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER15	0xE000E1BC	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ISPR0	0xE000E200	Interrupt Set-Pending Registers
CM33_SCS_NVIC_ISPR1	0xE000E204	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR2	0xE000E208	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR3	0xE000E20C	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.

Program and Debug Interface registers

Register name	Address	Description
CM33_SCS_NVIC_ISPR4	0xE000E210	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR5	0xE000E214	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR6	0xE000E218	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR7	0xE000E21C	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR8	0xE000E220	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR9	0xE000E224	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR10	0xE000E228	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR11	0xE000E22C	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR12	0xE000E230	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR13	0xE000E234	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR14	0xE000E238	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR15	0xE000E23C	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR0	0xE000E280	Interrupt Clear-Pending Registers
CM33_SCS_NVIC_ICPR1	0xE000E284	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR2	0xE000E288	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR3	0xE000E28C	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR4	0xE000E290	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR5	0xE000E294	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR6	0xE000E298	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR7	0xE000E29C	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR8	0xE000E2A0	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR9	0xE000E2A4	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.

Program and Debug Interface registers

Register name	Address	Description
CM33_SCS_NVIC_ICPR10	0xE000E2A8	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR11	0xE000E2AC	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR12	0xE000E2B0	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR13	0xE000E2B4	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR14	0xE000E2B8	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR15	0xE000E2BC	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_IABR0	0xE000E300	Interrupt Active Bit Registers
CM33_SCS_NVIC_IABR1	0xE000E304	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR2	0xE000E308	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR3	0xE000E30C	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR4	0xE000E310	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR5	0xE000E314	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR6	0xE000E318	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR7	0xE000E31C	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR8	0xE000E320	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR9	0xE000E324	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR10	0xE000E328	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR11	0xE000E32C	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR12	0xE000E330	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR13	0xE000E334	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR14	0xE000E338	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR15	0xE000E33C	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.

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Register name	Address	Description
CM33_SCS_NVIC_ITNS0	0xE000E380	Interrupt Target Non-secure Registers
CM33_SCS_NVIC_ITNS1	0xE000E384	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS2	0xE000E388	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS3	0xE000E38C	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS4	0xE000E390	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS5	0xE000E394	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS6	0xE000E398	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS7	0xE000E39C	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS8	0xE000E3A0	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS9	0xE000E3A4	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS10	0xE000E3A8	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS11	0xE000E3AC	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS12	0xE000E3B0	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS13	0xE000E3B4	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS14	0xE000E3B8	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS15	0xE000E3BC	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_IPR0	0xE000E400	Interrupt Priority Registers. This is the starting address of a register bank containing 120 registers (CM33_SCS_NVIC_IPR0 to CM33_SCS_NVIC_IPR119).
CM33_SCS_CPUID	0xE000ED00	CPUID Base Register
CM33_SCS_VTOR	0xE000ED08	Vector Table Offset Register
CM33_SCS_AIRCR	0xE000ED0C	Application Interrupt and Reset Control Register
CM33_SCS_SCR	0xE000ED10	System Control Register
CM33_SCS_CCR	0xE000ED14	Configuration and Control Register
CM33_SCS_DFSR	0xE000ED30	Debug Fault Status Register
CM33_SCS_ID_PFR0	0xE000ED40	Processor Feature Register 0
CM33_SCS_ID_PFR1	0xE000ED44	Processor Feature Register 1

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Register name	Address	Description
CM33_SCS_ID_DFR0	0xE000ED48	Debug Feature Register 0
CM33_SCS_ID_AFR0	0xE000ED4C	Auxiliary Feature Register 0
CM33_SCS_ID_MMFR0	0xE000ED50	Memory Model Feature Register 0
CM33_SCS_ID_MMFR1	0xE000ED54	Memory Model Feature Register 1
CM33_SCS_ID_MMFR2	0xE000ED58	Memory Model Feature Register 2
CM33_SCS_ID_MMFR3	0xE000ED5C	Memory Model Feature Register 3
CM33_SCS_ID_ISAR0	0xE000ED60	Instruction Set Attributes Register 0
CM33_SCS_ID_ISAR1	0xE000ED64	Instruction Set Attributes Register 1
CM33_SCS_ID_ISAR2	0xE000ED68	Instruction Set Attributes Register 2
CM33_SCS_ID_ISAR3	0xE000ED6C	Instruction Set Attributes Register 3
CM33_SCS_ID_ISAR4	0xE000ED70	Instruction Set Attributes Register 4
CM33_SCS_CLIDR	0xE000ED78	Cache Level ID Register
CM33_SCS_CTR	0xE000ED7C	Cache Type Register
CM33_SCS_CPACR	0xE000ED88	Coprocessor Access Control Register
CM33_SCS_NSACR	0xE000ED8C	Non-secure Access Control Register
CM33_SCS_MPU_TYPE	0xE000ED90	MPU Type Register
CM33_SCS_MPU_CTRL	0xE000ED94	MPU Control Register
CM33_SCS_MPU_RNR	0xE000ED98	MPU Region Number Register
CM33_SCS_MPU_RBAR	0xE000ED9C	MPU Region Base Address Register
CM33_SCS_MPU_RLAR	0xE000EDA0	MPU Region Limit Address Register
CM33_SCS_MPU_RBAR_A1	0xE000EDA4	MPU alias registers
CM33_SCS_MPU_RLAR_A1	0xE000EDA8	MPU alias registers
CM33_SCS_MPU_RBAR_A2	0xE000EDAC	MPU alias registers
CM33_SCS_MPU_RLAR_A2	0xE000EDB0	MPU alias registers
CM33_SCS_MPU_RBAR_A3	0xE000EDB4	MPU alias registers
CM33_SCS_MPU_RLAR_A3	0xE000EDB8	MPU alias registers
CM33_SCS_MPU_MAIR0	0xE000EDC0	MPU Memory Attribute Indirection Register 0
CM33_SCS_MPU_MAIR1	0xE000EDC4	MPU Memory Attribute Indirection Register 1
CM33_SCS_SAU_CTRL	0xE000EDD0	SAU Control Register
CM33_SCS_SAU_TYPE	0xE000EDD4	SAU Type Register
CM33_SCS_SAU_RNR	0xE000EDD8	SAU Region Number Register
CM33_SCS_SAU_RBAR	0xE000EDDC	SAU Region Base Address Register
CM33_SCS_SAU_RLAR	0xE000EDE0	SAU Region Limit Address Register
CM33_SCS_DHCSR	0xE000EDF0	Debug Halting Control and Status Register
CM33_SCS_DCRSR	0xE000EDF4	Debug Core Register Selector Register
CM33_SCS_DCRDR	0xE000EDF8	Debug Core Register Data Register
CM33_SCS_DEMCR	0xE000EDFC	Debug Exception and Monitor Control Register
CM33_SCS_DAUTHCTRL	0xE000EE04	Debug Authentication Control Register
CM33_SCS_DSCSR	0xE000EE08	Debug Security Control and Status Register

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Register name	Address	Description
CM33_SCS_FPCCR	0xE000EF34	FP Context Control Register
CM33_SCS_FPCAR	0xE000EF38	FP Context Control Register
CM33_SCS_FPDSCR	0xE000EF3C	FP Context Control Register
CM33_SCS_MVFR0	0xE000EF40	Media and VFP Feature Register 0
CM33_SCS_MVFR1	0xE000EF44	Media and VFP Feature Register 1
CM33_SCS_MVFR2	0xE000EF48	Media and VFP Feature Register 2
CM33_SCS_DAUTHSTATUS	0xE000EFB8	Debug Authentication Status Register
CM33_SCS_DEVARCH	0xE000EFBC	CoreSight Device Architecture Register
CM33_SCS_PIDR4	0xE000EFD0	Peripheral Identification Register 4
CM33_SCS_PIDR5	0xE000EFD4	Peripheral Identification Register 5
CM33_SCS_PIDR6	0xE000EFD8	Peripheral Identification Register 6
CM33_SCS_PIDR7	0xE000EFDC	Peripheral Identification Register 7
CM33_SCS_PIDR0	0xE000EFE0	Peripheral Identification Register 0
CM33_SCS_PIDR1	0xE000EFE4	Peripheral Identification Register 1
CM33_SCS_PIDR2	0xE000EFE8	Peripheral Identification Register 2
CM33_SCS_PIDR3	0xE000EFEC	Peripheral Identification Register 3
CM33_SCS_CIDR0	0xE000EFF0	Component Identification Register 0
CM33_SCS_CIDR1	0xE000EFF4	Component Identification Register 1
CM33_SCS_CIDR2	0xE000EFF8	Component Identification Register 2
CM33_SCS_CIDR3	0xE000EFFC	Component Identification Register 3
CM33_TRC_CTI_CTICONTROL	0xE0080000	CTI Control Register
CM33_TRC_CTI_CTIINTACK	0xE0080010	CTI Interrupt Acknowledge Register
CM33_TRC_CTI_CTIAPPSET	0xE0080014	CTI Application Trigger Set Register
CM33_TRC_CTI_CTIAPPCLEAR	0xE0080018	CTI Application Trigger Clear Register
CM33_TRC_CTI_CTIAPPPULSE	0xE008001C	CTI Application Pulse Register
CM33_TRC_CTI_CTIINEN0	0xE0080020	CTI Trigger to Channel Enable Registers
CM33_TRC_CTI_CTIINEN1	0xE0080024	CTI Trigger to Channel Enable Registers. See CM33_TRC_CTI_CTIINEN0 for the details of bit fields.
CM33_TRC_CTI_CTIINEN2	0xE0080028	CTI Trigger to Channel Enable Registers. See CM33_TRC_CTI_CTIINEN0 for the details of bit fields.
CM33_TRC_CTI_CTIINEN3	0xE008002C	CTI Trigger to Channel Enable Registers. See CM33_TRC_CTI_CTIINEN0 for the details of bit fields.
CM33_TRC_CTI_CTIINEN4	0xE0080030	CTI Trigger to Channel Enable Registers. See CM33_TRC_CTI_CTIINEN0 for the details of bit fields.
CM33_TRC_CTI_CTIINEN5	0xE0080034	CTI Trigger to Channel Enable Registers. See CM33_TRC_CTI_CTIINEN0 for the details of bit fields.
CM33_TRC_CTI_CTIINEN6	0xE0080038	CTI Trigger to Channel Enable Registers. See CM33_TRC_CTI_CTIINEN0 for the details of bit fields.
CM33_TRC_CTI_CTIINEN7	0xE008003C	CTI Trigger to Channel Enable Registers. See CM33_TRC_CTI_CTIINEN0 for the details of bit fields.

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Register name	Address	Description
CM33_TRC_CTI_CTIOUTEN0	0xE00800A0	CTI Channel to Trigger Enable Registers
CM33_TRC_CTI_CTIOUTEN1	0xE00800A4	CTI Channel to Trigger Enable Registers. See CM33_TRC_CTI_CTIOUTEN0 for the details of bit fields.
CM33_TRC_CTI_CTIOUTEN2	0xE00800A8	CTI Channel to Trigger Enable Registers. See CM33_TRC_CTI_CTIOUTEN0 for the details of bit fields.
CM33_TRC_CTI_CTIOUTEN3	0xE00800AC	CTI Channel to Trigger Enable Registers. See CM33_TRC_CTI_CTIOUTEN0 for the details of bit fields.
CM33_TRC_CTI_CTIOUTEN4	0xE00800B0	CTI Channel to Trigger Enable Registers. See CM33_TRC_CTI_CTIOUTEN0 for the details of bit fields.
CM33_TRC_CTI_CTIOUTEN5	0xE00800B4	CTI Channel to Trigger Enable Registers. See CM33_TRC_CTI_CTIOUTEN0 for the details of bit fields.
CM33_TRC_CTI_CTIOUTEN6	0xE00800B8	CTI Channel to Trigger Enable Registers. See CM33_TRC_CTI_CTIOUTEN0 for the details of bit fields.
CM33_TRC_CTI_CTIOUTEN7	0xE00800BC	CTI Channel to Trigger Enable Registers. See CM33_TRC_CTI_CTIOUTEN0 for the details of bit fields.
CM33_TRC_CTI_CTITRIGINSTATUS	0xE0080130	CTI Trigger In Status Register
CM33_TRC_CTI_CTITRIGOUTSTATUS	0xE0080134	CTI Trigger Out Status Register
CM33_TRC_CTI_CTICHINSTATUS	0xE0080138	CTI Channel In Status Register
CM33_TRC_CTI_CTICHOUTSTATUS	0xE008013C	CTI Channel Out Status Register
CM33_TRC_CTI_CTIGATE	0xE0080140	Enable CTI Channel Gate Register
CM33_TRC_CTI_ASICCTL	0xE0080144	External Multiplexor Control Register
CM33_TRC_CTI_ITCHINACK	0xE0080EDC	ITCHINACK Register
CM33_TRC_CTI_ITTRIGINACK	0xE0080EE0	ITTRIGINACK Register
CM33_TRC_CTI_ITCHOUT	0xE0080EE4	ITCHOUT Register
CM33_TRC_CTI_ITTRIGOUT	0xE0080EE8	ITTRIGOUT Register
CM33_TRC_CTI_ITCHOUTACK	0xE0080EEC	ITCHOUTACK Register
CM33_TRC_CTI_ITTRIGOUTACK	0xE0080EF0	ITTRIGOUTACK Register
CM33_TRC_CTI_ITCHIN	0xE0080EF4	ITCHIN Register
CM33_TRC_CTI_ITTRIGIN	0xE0080EF8	ITTRIGIN Register
CM33_TRC_CTI_ITCTRL	0xE0080F00	Integration Mode Control Register
CM33_TRC_CTI_CLAIMSET	0xE0080FA0	Claim Tag Set Register
CM33_TRC_CTI_CLAIMCLR	0xE0080FA4	Claim Tag Clear Register
CM33_TRC_CTI_LAR	0xE0080FB0	Lock Access Register
CM33_TRC_CTI_LSR	0xE0080FB4	Lock Status Register
CM33_TRC_CTI_AUTHSTATUS	0xE0080FB8	Authentication Status Register
CM33_TRC_CTI_DEVID	0xE0080FC8	Device Configuration Register
CM33_TRC_CTI_DEVTYPE	0xE0080FCC	Device Type Identifier Register
CM33_TRC_CTI_PIDR4	0xE0080FD0	Peripheral Identification Register 4
CM33_TRC_CTI_PIDR5	0xE0080FD4	Peripheral Identification Register 5

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Register name	Address	Description
CM33_TRC_CTI_PIDR6	0xE0080FD8	Peripheral Identification Register 6
CM33_TRC_CTI_PIDR7	0xE0080FDC	Peripheral Identification Register 7
CM33_TRC_CTI_PIDR0	0xE0080FE0	Peripheral Identification Register 0
CM33_TRC_CTI_PIDR1	0xE0080FE4	Peripheral Identification Register 1
CM33_TRC_CTI_PIDR2	0xE0080FE8	Peripheral Identification Register 2
CM33_TRC_CTI_PIDR3	0xE0080FEC	Peripheral Identification Register 3
CM33_TRC_CTI_CIDR0	0xE0080FF0	Component Identification Register 0
CM33_TRC_CTI_CIDR1	0xE0080FF4	Component Identification Register 1
CM33_TRC_CTI_CIDR2	0xE0080FF8	Component Identification Register 2
CM33_TRC_CTI_CIDR3	0xE0080FFC	Component Identification Register 3
CM33_CSTF_FUNNELCONTROL	0xE0088000	Funnel Control Register
CM33_CSTF_PRIORITYCONTROL	0xE0088004	Priority Control Register
CM33_CSTF_ITATBDATA0	0xE0088EEC	Integration Register
CM33_CSTF_ITATBCTR3	0xE0088EF0	Integration Register
CM33_CSTF_ITATBCTR2	0xE0088EF4	Integration Register
CM33_CSTF_ITATBCTR1	0xE0088EF8	Integration Register
CM33_CSTF_ITATBCTR0	0xE0088EFC	Integration Register
CM33_CSTF_ITCTRL	0xE0088F00	Integration Mode Control Register
CM33_CSTF_CLAIMSET	0xE0088FA0	Claim Tag Set Register
CM33_CSTF_CLAIMCLR	0xE0088FA4	Claim Tag Clear Register
CM33_CSTF_DEVAFF0	0xE0088FB0	Device Affinity Register0
CM33_CSTF_DEVAFF1	0xE0088FB4	Device Affinity Register1
CM33_CSTF_AUTHSTATUS	0xE0088FB8	Authentication Status Register
CM33_CSTF_DEVARCH	0xE0088FBC	Device Architecture Register
CM33_CSTF_DEVID2	0xE0088FC0	Device Configuration Register 2
CM33_CSTF_DEVID1	0xE0088FC4	Device Configuration Register 1
CM33_CSTF_DEVID	0xE0088FC8	Device Configuration Register
CM33_CSTF_DEVTYPE	0xE0088FCC	Device Type Identifier Register
CM33_CSTF_PIDR4	0xE0088FD0	Peripheral Identification Register 4
CM33_CSTF_PIDR5	0xE0088FD4	Peripheral Identification Register 5
CM33_CSTF_PIDR6	0xE0088FD8	Peripheral Identification Register 6
CM33_CSTF_PIDR7	0xE0088FDC	Peripheral Identification Register 7
CM33_CSTF_PIDR0	0xE0088FE0	Peripheral Identification Register 0
CM33_CSTF_PIDR1	0xE0088FE4	Peripheral Identification Register 1
CM33_CSTF_PIDR2	0xE0088FE8	Peripheral Identification Register 2
CM33_CSTF_PIDR3	0xE0088FEC	Peripheral Identification Register 3
CM33_CSTF_CIDR1	0xE0088FF4	Component Identification Register 1
CM33_CSTF_CIDR2	0xE0088FF8	Component Identification Register 2
CM33_CSTF_CIDR3	0xE0088FFC	Component Identification Register 3

Program and Debug Interface registers

Register name	Address	Description
CM33_ETF_RSZ	0xE008D004	RAM Size register
CM33_ETF_STS	0xE008D00C	Status Register
CM33_ETF_RRD	0xE008D010	RAM Read Data Register
CM33_ETF_RRP	0xE008D014	RAM Read Pointer Register
CM33_ETF_RWP	0xE008D018	RAM Write Pointer Register
CM33_ETF_TRG	0xE008D01C	Trigger Counter Register
CM33_ETF_CTL	0xE008D020	Control Register
CM33_ETF_RWD	0xE008D024	RAM Write Data Register
CM33_ETF_MODE	0xE008D028	Mode Register
CM33_ETF_LBUFLEVEL	0xE008D02C	Latched Buffer Fill Level
CM33_ETF_CBUFLEVEL	0xE008D030	Current Buffer Fill Level
CM33_ETF_BUFWM	0xE008D034	Buffer Level Water Mark
CM33_ETF_FFSR	0xE008D300	Formatter and Flush Status Register
CM33_ETF_FFCR	0xE008D304	Formatter and Flush Control Register
CM33_ETF_PSCR	0xE008D308	Periodic Synchronization Counter Register
CM33_ETF_ITATBMDATA0	0xE008DED0	Integration Test ATB Master Data 0 Register
CM33_ETF_ITATBMCTR2	0xE008DED4	Integration Test ATB Master Interface Control 2 Register
CM33_ETF_ITATBMCTR1	0xE008DED8	Integration Test ATB Master Interface Control 1 Register
CM33_ETF_ITATBMCTR0	0xE008DEDC	Integration Test ATB Master Interface Control 0 Registe
CM33_ETF_ITEVTINTR	0xE008DEE0	Integration Test Event & Interrupt Status Register
CM33_ETF_ITTRFLIN	0xE008DEE8	Integration Test Trigger In and Flush In Register
CM33_ETF_ITATBDATA0	0xE008DEEC	Integration Test ATB Data 0 Register
CM33_ETF_ITATBCTR2	0xE008DEF0	Integration Test ATB Control 2 Register
CM33_ETF_ITATBCTR1	0xE008DEF4	Integration Test ATB Control 1 Register
CM33_ETF_ITATBCTR0	0xE008DEF8	Integration Test ATB Control 0 Register
CM33_ETF_ITCTRL	0xE008DF00	Integration Mode Control Register
CM33_ETF_CLAIMSET	0xE008DFA0	Claim Tag Set Register
CM33_ETF_CLAIMCLR	0xE008DFA4	Claim Tag Clear Register
CM33_ETF_AUTHSTATUS	0xE008DFB8	Authentication Status Register
CM33_ETF_DEVID1	0xE008DFC4	Device Configuration Register 1
CM33_ETF_DEVID	0xE008DFC8	Device Configuration Register
CM33_ETF_DEVTYPE	0xE008DFCC	Device Type Identifier Register
CM33_ETF_PIDR4	0xE008DFD0	Peripheral Identification Register 4
CM33_ETF_PIDR5	0xE008DFD4	Peripheral Identification Register 5
CM33_ETF_PIDR6	0xE008DFD8	Peripheral Identification Register 6
CM33_ETF_PIDR7	0xE008DFDC	Peripheral Identification Register 7
CM33_ETF_PIDR0	0xE008DFE0	Peripheral Identification Register 0
CM33_ETF_PIDR1	0xE008DFE4	Peripheral Identification Register 1
CM33_ETF_PIDR2	0xE008DFE8	Peripheral Identification Register 2

Program and Debug Interface registers

Register name	Address	Description
CM33_ETF_PIDR3	0xE008DFEC	Peripheral Identification Register 3
CM33_ETF_CIDR0	0xE008DFF0	Component Identification Register 0
CM33_ETF_CIDR1	0xE008DFF4	Component Identification Register 1
CM33_ETF_CIDR2	0xE008DFF8	Component Identification Register 2
CM33_ETF_CIDR3	0xE008DFFC	Component Identification Register 3
CM33_CSS600_TPIU_TPIU_SSPSR	0xE008E000	Supported Parallel Port Size Register
CM33_CSS600_TPIU_TPIU_CSPSR	0xE008E004	Current Parallel Port Size Register
CM33_CSS600_TPIU_TPIU_STMR	0xE008E100	Supported Trigger Model Register
CM33_CSS600_TPIU_TPIU_TCVR	0xE008E104	Trigger Counter Value Register
CM33_CSS600_TPIU_TPIU_TCMR	0xE008E108	Trigger Counter Multiplier Register
CM33_CSS600_TPIU_TPIU_STPMR	0xE008E200	Supported Test Patterns Modes Register
CM33_CSS600_TPIU_TPIU_CTPMR	0xE008E204	Current Test Patterns Modes Register
CM33_CSS600_TPIU_TPIU_TPRCR	0xE008E208	Test Pattern Repeat Counter Register
CM33_CSS600_TPIU_TPIU_FFSR	0xE008E300	Formatter and Flush Status Register
CM33_CSS600_TPIU_TPIU_FFCR	0xE008E304	Formatter and Flush Control Register
CM33_CSS600_TPIU_TPIU_FSCR	0xE008E308	Formatter Synchronization Count Register
CM33_CSS600_TPIU_TPIU_EXTCTLIN	0xE008E400	External Control Port In Register
CM33_CSS600_TPIU_TPIU_EXTCTLOUT	0xE008E404	External Control Port Out Register
CM33_CSS600_TPIU_ITTRFLIN	0xE008EEE8	Integration Test Trigger In Flush In Register
CM33_CSS600_TPIU_ITATBDATA0	0xE008EEEC	Integration Test ATB Data Register0
CM33_CSS600_TPIU_ITATBCTR2	0xE008EEF0	Integration Test ATB Control Register 2
CM33_CSS600_TPIU_ITATBCTR1	0xE008EEF4	Integration Test ATB Control Register 1
CM33_CSS600_TPIU_ITATBCTR0	0xE008EEF8	Integration Test ATB Control Register 0
CM33_CSS600_TPIU_ITOUTCTR	0xE008EEFC	Integration Test Output Control Register
CM33_CSS600_TPIU_ITCTRL	0xE008EF00	Integration Mode Control Register
CM33_CSS600_TPIU_CLAIMSET	0xE008EFA0	Claim Tag Set Register
CM33_CSS600_TPIU_CLAIMCLR	0xE008EFA4	Claim Tag Clear Register
CM33_CSS600_TPIU_AUTHSTATUS	0xE008EFB8	Authentication Status Register
CM33_CSS600_TPIU_DEVARCH	0xE008EFBC	Device Architecture Register
CM33_CSS600_TPIU_DEVID	0xE008EFC8	Device ID
CM33_CSS600_TPIU_DEVTYPE	0xE008EFCC	Device Type Identifier Register
CM33_CSS600_TPIU_PIDR4	0xE008EFD0	Peripheral Identification Register 4
CM33_CSS600_TPIU_PIDR5	0xE008EFD4	Peripheral Identification Register 5
CM33_CSS600_TPIU_PIDR6	0xE008EFD8	Peripheral Identification Register 6
CM33_CSS600_TPIU_PIDR7	0xE008EFDC	Peripheral Identification Register 7
CM33_CSS600_TPIU_PIDR0	0xE008EFE0	Peripheral Identification Register 0
CM33_CSS600_TPIU_PIDR1	0xE008EFE4	Peripheral Identification Register 1

Program and Debug Interface registers

Register name	Address	Description
CM33_CSS600_TPIU_PIDR2	0xE008EFE8	Peripheral Identification Register 2
CM33_CSS600_TPIU_PIDR3	0xE008EFEC	Peripheral Identification Register 3
CM33_CSS600_TPIU_CIDR0	0xE008EFF0	Component Identification Register 0
CM33_CSS600_TPIU_CIDR1	0xE008EFF4	Component Identification Register 1
CM33_CSS600_TPIU_CIDR2	0xE008EFF8	Component Identification Register 2
CM33_CSS600_TPIU_CIDR3	0xE008EFFC	Component Identification Register 3
SYSAP_ROMTABLE_DID	0xE00BEFCC	Device Type Identifier register.
SYSAP_ROMTABLE_PID4	0xE00BEFD0	Peripheral Identification Register 4.
SYSAP_ROMTABLE_PID5	0xE00BEFD4	Peripheral Identification Register 5.
SYSAP_ROMTABLE_PID6	0xE00BEFD8	Peripheral Identification Register 6.
SYSAP_ROMTABLE_PID7	0xE00BEFDC	Peripheral Identification Register 7.
SYSAP_ROMTABLE_PID0	0xE00BEFE0	Peripheral Identification Register 0.
SYSAP_ROMTABLE_PID1	0xE00BEFE4	Peripheral Identification Register 1.
SYSAP_ROMTABLE_PID2	0xE00BEFE8	Peripheral Identification Register 2.
SYSAP_ROMTABLE_PID3	0xE00BEFEC	Peripheral Identification Register 3.
SYSAP_ROMTABLE_CID0	0xE00BEFF0	Component Identification Register 0.
SYSAP_ROMTABLE_CID1	0xE00BEFF4	Component Identification Register 1.
SYSAP_ROMTABLE_CID2	0xE00BEFF8	Component Identification Register 2.
SYSAP_ROMTABLE_CID3	0xE00BEFFC	Component Identification Register 3.
CM33_ROMTABLE_TRC_CTI	0xE00BF000	CM33 CoreSight ROM Table Peripheral #0
CM33_ROMTABLE_TRC_ETB_CSTF	0xE00BF004	CM33 CoreSight ROM Table Peripheral #1
CM33_ROMTABLE_TRC_ETB	0xE00BF008	CM33 CoreSight ROM Table Peripheral #2
CM33_ROMTABLE_TRC_TPIU	0xE00BF00C	CM33 CoreSight ROM Table Peripheral #3
CM33_ROMTABLE_TRC_ETM_CSTF	0xE00BF010	CM33 CoreSight ROM Table Peripheral #4
CM33_ROMTABLE_TRC_ITM_CSTF	0xE00BF014	CM33 CoreSight ROM Table Peripheral #5
CM33_ROMTABLE_CM33	0xE00BF018	CM33 CoreSight ROM Table Peripheral #6
CM33_ROMTABLE_CSMT	0xE00BFFCC	CM33 CoreSight ROM Table Memory Type
CM33_ROMTABLE_PID4	0xE00BFFD0	CM33 CoreSight ROM Table Peripheral ID #4
CM33_ROMTABLE_PID0	0xE00BFFE0	CM33 CoreSight ROM Table Peripheral ID #0
CM33_ROMTABLE_PID1	0xE00BFFE4	CM33 CoreSight ROM Table Peripheral ID #1
CM33_ROMTABLE_PID2	0xE00BFFE8	CM33 CoreSight ROM Table Peripheral ID #2
CM33_ROMTABLE_PID3	0xE00BFFEC	CM33 CoreSight ROM Table Peripheral ID #3
CM33_ROMTABLE_CID0	0xE00BFFF0	CM33 CoreSight ROM Table Component ID #0
CM33_ROMTABLE_CID1	0xE00BFFF4	CM33 CoreSight ROM Table Component ID #1
CM33_ROMTABLE_CID2	0xE00BFFF8	CM33 CoreSight ROM Table Component ID #2
CM33_ROMTABLE_CID3	0xE00BFFFC	CM33 CoreSight ROM Table Component ID #3
CM33_ROM_SCS	0xE00FF000	CM33 CoreSight ROM Table Peripheral #0
CM33_ROM_DWT	0xE00FF004	CM33 CoreSight ROM Table Peripheral #1
CM33_ROM_FPB	0xE00FF008	CM33 CoreSight ROM Table Peripheral #2

Program and Debug Interface registers

Register name	Address	Description
CM33_ROM_ITM	0xE00FF00C	CM33 CoreSight ROM Table Peripheral #3
CM33_ROM_ETM	0xE00FF014	CM33 CoreSight ROM Table Peripheral #4
CM33_ROM_CTI	0xE00FF018	CM33 CoreSight ROM Table Peripheral #5
CM33_ROM_MTB	0xE00FF01C	CM33 CoreSight ROM Table Peripheral #6
CM33_ROM_CSMT	0xE00FFFCC	CM33 CoreSight ROM Table Memory Type
CM33_ROM_PID4	0xE00FFFD0	CM33 CoreSight ROM Table Peripheral ID #4
CM33_ROM_PID0	0xE00FFFE0	CM33 CoreSight ROM Table Peripheral ID #0
CM33_ROM_PID1	0xE00FFFE4	CM33 CoreSight ROM Table Peripheral ID #1
CM33_ROM_PID2	0xE00FFFE8	CM33 CoreSight ROM Table Peripheral ID #2
CM33_ROM_PID3	0xE00FFFEC	CM33 CoreSight ROM Table Peripheral ID #3
CM33_ROM_CID0	0xE00FFFF0	CM33 CoreSight ROM Table Component ID #0
CM33_ROM_CID1	0xE00FFFF4	CM33 CoreSight ROM Table Component ID #1
CM33_ROM_CID2	0xE00FFFF8	CM33 CoreSight ROM Table Component ID #2
CM33_ROM_CID3	0xE00FFFFC	CM33 CoreSight ROM Table Component ID #3

10.1.1 DEBUG600_VERSION

Description: IP Version Information

Address: 0x42430000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	MINOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	MAJOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	MAJOR	IP Major Revision Number Default Value: Undefined
7 : 0	MINOR	IP Minor Revision Number Default Value: Undefined

10.1.2 CM33_SCS_ICTR

Description: Interrupt Controller Type Register

Address: 0xE000E004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Shows the number of interrupt lines that the NVIC supports Total number of interrupt lines in groups of 32: 0b0000 = 1...32 0b0001 = 33...64 0b0010 = 65...96 0b0011 = 97...128 0b0100 = 129...160 0b0101 = 161...192 0b0110 = 193...224 0b0111 = 225...256 0b1000 = 257...288 0b1001 = 289...320 0b1010 = 321...352 0b1011 = 353...384 0b1100 = 385...416 0b1101 = 417...448 0b1110 = 449...480 Default Value: 0x0000000X

10.1.3 CM33_SCS_ACTLR

Description: Auxiliary Control Register

Address: 0xE000E008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer the following ARM documents for details about CPU register descriptions: ARMv8-M : https://developer.arm.com/documentation/ddi0553/latest/ CM33 TRM - ACTLR : https://developer.arm.com/documentation/100230/0100/System-Control/Auxiliary-Control-Register Default Value: 0

10.1.4 CM33_SCS_SYST_CSR

Description: SysTick Control and Status Register

Address: 0xE000E010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.189 SYST_CSR, SysTick Control and Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.5 CM33_SCS_SYST_RVR

Description: SysTick Reload Value Register

Address: 0xE000E014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.191 SYST_RVR, SysTick Reload Value Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.6 CM33_SCS_SYST_CVR

Description: SysTick Current Value Register

Address: 0xE000E018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.190 SYST_CVR, SysTick Current Value Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.7 CM33_SCS_SYST_CALIB

Description: SysTick Calibration value Register

Address: 0xE000E01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.188 SYST_CALIB, SysTick Calibration Value Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.8 CM33_SCS_NVIC_ISER0

Description: Interrupt Set-Enable Registers

Address: 0xE000E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.165 NVIC_ISER, Interrupt Set Enable Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.9 CM33_SCS_NVIC_ICER0

Description: Interrupt Clear-Enable Registers

Address: 0xE000E180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.162 NVIC_ICER, Interrupt Clear Enable Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.10 CM33_SCS_NVIC_ISPR0

Description: Interrupt Set-Pending Registers

Address: 0xE000E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.166 NVIC_ISPR, Interrupt Set Pending Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.11 CM33_SCS_NVIC_ICPR0

Description: Interrupt Clear-Pending Registers

Address: 0xE000E280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.163 NVIC_ICPR, Interrupt Clear Pending Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.12 CM33_SCS_NVIC_IABR0

Description: Interrupt Active Bit Registers

Address: 0xE000E300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.161 NVIC_IABR, Interrupt Active Bit Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.13 CM33_SCS_NVIC_ITNS0

Description: Interrupt Target Non-secure Registers

Address: 0xE000E380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.167 NVIC_ITNS, Interrupt Target Non-secure Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.14 CM33_SCS_NVIC_IPR0

Description: Interrupt Priority Registers

Address: 0xE000E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.164 NVIC_IPR, Interrupt Priority Register, n = 0 - 123" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.15 CM33_SCS_CPUID

Description: CPUID Base Register

Address: 0xE000ED00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM33 TRM - CPUID: https://developer.arm.com/documentation/100230/0100/System-Control/CPUID-Base-Register Default Value: 0x410FD214

10.1.16 CM33_SCS_VTOR

Description: Vector Table Offset Register

Address: 0xE000ED08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Table offset. Bits [31:7] of the vector table address for the selected Security state. It is IMPLEMENTATION DEFINED whether any of the TBLOFF bits are WI. This field resets to an IMPLEMENTATION DEFINED value on a Warm reset. Default Value: 0

10.1.17 CM33_SCS_AIRCR

Description: Application Interrupt and Reset Control Register

Address: 0xE000ED0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.3 AIRCR, Application Interrupt and Reset Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.18 CM33_SCS_SCR

Description: System Control Register

Address: 0xE000ED10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.178 SCR, System Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.19 CM33_SCS_CCR

Description: Configuration and Control Register

Address: 0xE000ED14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.9 CCR, Configuration and Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.20 CM33_SCS_DFSR

Description: Debug Fault Status Register

Address: 0xE000ED30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.37 DFSR, Debug Fault Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.21 CM33_SCS_ID_PFR0

Description: Processor Feature Register 0

Address: 0xE000ED40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.120 ID_PFR0, Processor Feature Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000030

10.1.22 CM33_SCS_ID_PFR1

Description: Processor Feature Register 1

Address: 0xE000ED44

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.121 ID_PFR1, Processor Feature Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x000002X0

10.1.23 CM33_SCS_ID_DFR0

Description: Debug Feature Register 0

Address: 0xE000ED48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.109 ID_DFR0, Debug Feature Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00200000

10.1.24 CM33_SCS_ID_AFR0

Description: Auxiliary Feature Register 0

Address: 0xE000ED4C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.108 ID_AFR0, Auxiliary Feature Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.25 CM33_SCS_ID_MMFR0

Description: Memory Model Feature Register 0

Address: 0xE000ED50

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.116 ID_MMFR0, Memory Model Feature Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00101F40

10.1.26 CM33_SCS_ID_MMFR1

Description: Memory Model Feature Register 1

Address: 0xE000ED54

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.117 ID_MMFR1, Memory Model Feature Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.27 CM33_SCS_ID_MMFR2

Description: Memory Model Feature Register 2

Address: 0xE000ED58

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.118 ID_MMFR2, Memory Model Feature Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x01000000

10.1.28 CM33_SCS_ID_MMFR3

Description: Memory Model Feature Register 3

Address: 0xE000ED5C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.119 ID_MMFR3, Memory Model Feature Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.29 CM33_SCS_ID_ISAR0

Description: Instruction Set Attributes Register 0

Address: 0xE000ED60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.110 ID_ISAR0, Instruction Set Attribute Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x011X1110

10.1.30 CM33_SCS_ID_ISAR1

Description: Instruction Set Attributes Register 1

Address: 0xE000ED64

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.111 ID_ISAR1, Instruction Set Attribute Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0221X000

10.1.31 CM33_SCS_ID_ISAR2

Description: Instruction Set Attributes Register 2

Address: 0xE000ED68

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.112 ID_ISAR2, Instruction Set Attribute Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x20XX2232

10.1.32 CM33_SCS_ID_ISAR3

Description: Instruction Set Attributes Register 3

Address: 0xE000ED6C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.113 ID_ISAR3, Instruction Set Attribute Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x011111XX

10.1.33 CM33_SCS_ID_ISAR4

Description: Instruction Set Attributes Register 4

Address: 0xE000ED70

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.114 ID_ISAR4, Instruction Set Attribute Register 4" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x01310132

10.1.34 CM33_SCS_CLIDR

Description: Cache Level ID Register

Address: 0xE000ED78

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.12 CLIDR, Cache Level ID Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.35 CM33_SCS_CTR

Description: Cache Type Register

Address: 0xE000ED7C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.18 CTR, Cache Type Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x8000C000

10.1.36 CM33_SCS_CPACR

Description: Coprocessor Access Control Register

Address: 0xE000ED88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.14 CPACR, Coprocessor Access Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.37 CM33_SCS_NSACR

Description: Non-secure Access Control Register

Address: 0xE000ED8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.160 NSACR, Non-secure Access Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.38 CM33_SCS_MPU_TYPE

Description: MPU Type Register

Address: 0xE000ED90

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.155 MPU_TYPE, MPU Type Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0000XX00

10.1.39 CM33_SCS_MPU_CTRL

Description: MPU Control Register

Address: 0xE000ED94

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.147 MPU_CTRL, MPU Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.40 CM33_SCS_MPU_RNR

Description: MPU Region Number Register

Address: 0xE000ED98

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.154 MPU_RNR, MPU Region Number Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.41 CM33_SCS_MPU_RBAR

Description: MPU Region Base Address Register

Address: 0xE000ED9C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.150 MPU_RBAR, MPU Region Base Address Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.42 CM33_SCS_MPU_RLAR

Description: MPU Region Limit Address Register

Address: 0xE000EDA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.152 MPU_RLAR, MPU Region Limit Address Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.43 CM33_SCS_MPU_RBAR_A1

Description: MPU alias registers

Address: 0xE000EDA4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.151 MPU_RBAR_A, MPU Region Base Address Register Alias, n = 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.44 CM33_SCS_MPU_RLAR_A1

Description: MPU alias registers

Address: 0xE000EDA8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.153 MPU_RLAR_A, MPU Region Limit Address Register Alias, n = 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.45 CM33_SCS_MPU_RBAR_A2

Description: MPU alias registers

Address: 0xE000EDAC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.151 MPU_RBAR_A, MPU Region Base Address Register Alias, n = 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.46 CM33_SCS_MPU_RLAR_A2

Description: MPU alias registers

Address: 0xE000EDB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.153 MPU_RLAR_A, MPU Region Limit Address Register Alias, n = 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.47 CM33_SCS_MPU_RBAR_A3

Description: MPU alias registers

Address: 0xE000EDB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.151 MPU_RBAR_A, MPU Region Base Address Register Alias, n = 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.48 CM33_SCS_MPU_RLAR_A3

Description: MPU alias registers

Address: 0xE000EDB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.153 MPU_RLAR_A, MPU Region Limit Address Register Alias, n = 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.49 CM33_SCS_MPU_MAIR0

Description: MPU Memory Attribute Indirection Register 0

Address: 0xE000EDC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.148 MPU_MAIR0, MPU Memory Attribute Indirection Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.50 CM33_SCS_MPU_MAIR1

Description: MPU Memory Attribute Indirection Register 1

Address: 0xE000EDC4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.149 MPU_MAIR1, MPU Memory Attribute Indirection Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.51 CM33_SCS_SAU_CTRL

Description: SAU Control Register

Address: 0xE000EDD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.173 SAU_CTRL, SAU Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.52 CM33_SCS_SAU_TYPE

Description: SAU Type Register

Address: 0xE000EDD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.177 SAU_TYPE, SAU Type Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000008

10.1.53 CM33_SCS_SAU_RNR

Description: SAU Region Number Register

Address: 0xE000EDD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.176 SAU_RNR, SAU Region Number Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.54 CM33_SCS_SAU_RBAR

Description: SAU Region Base Address Register

Address: 0xE000EDDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.174 SAU_RBAR, SAU Region Base Address Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.55 CM33_SCS_SAU_RLAR

Description: SAU Region Limit Address Register

Address: 0xE000EDE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.175 SAU_RLAR, SAU Region Limit Address Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.56 CM33_SCS_DHCSR

Description: Debug Halting Control and Status Register

Address: 0xE000EDF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.38 DHCSR, Debug Halting Control and Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.57 CM33_SCS_DCRSR

Description: Debug Core Register Selector Register

Address: 0xE000EDF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.33 DCRSR, Debug Core Register Select Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.58 CM33_SCS_DCRDR

Description: Debug Core Register Data Register

Address: 0xE000EDF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.32 DCRDR, Debug Core Register Data Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.59 CM33_SCS_DEMCR

Description: Debug Exception and Monitor Control Register

Address: 0xE000EDFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.36 DEMCR, Debug Exception and Monitor Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.60 CM33_SCS_DAUTHCTRL

Description: Debug Authentication Control Register

Address: 0xE000EE04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.19 DAUTHCTRL, Debug Authentication Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.61 CM33_SCS_DSCSR

Description: Debug Security Control and Status Register

Address: 0xE000EE08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.49 DSCSR, Debug Security Control and Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.62 CM33_SCS_FPCCR

Description: FP Context Control Register

Address: 0xE000EF34

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.81 FPCCR, Floating-Point Context Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0xC0000004

10.1.63 CM33_SCS_FPCAR

Description: FP Context Control Register

Address: 0xE000EF38

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.80 FPCAR, Floating-Point Context Address Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.64 CM33_SCS_FPDSCR

Description: FP Context Control Register

Address: 0xE000EF3C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.82 FPDSCR, Floating-Point Default Status Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.65 CM33_SCS_MVFR0

Description: Media and VFP Feature Register 0

Address: 0xE000EF40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.157 MVFR0, Media and VFP Feature Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x10110021

10.1.66 CM33_SCS_MVFR1

Description: Media and VFP Feature Register 1

Address: 0xE000EF44

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.158 MVFR1, Media and VFP Feature Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x11000011

10.1.67 CM33_SCS_MVFR2

Description: Media and VFP Feature Register 2

Address: 0xE000EF48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.159 MVFR2, Media and VFP Feature Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000040

10.1.68 CM33_SCS_DAUTHSTATUS

Description: Debug Authentication Status Register

Address: 0xE000EFB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.20 DAUTHSTATUS, Debug Authentication Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

10.1.69 CM33_SCS_DEVARCH

Description: CoreSight Device Architecture Register

Address: 0xE000EFBC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.34 DDEVARCH, SCS Device Architecture Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x47702A04

10.1.70 CM33_SCS_PIDR4

Description: Peripheral Identification Register 4

Address: 0xE000EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.45 DPIDR4, SCS Peripheral Identification Register 4" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000004

10.1.71 CM33_SCS_PIDR5

Description: Peripheral Identification Register 5

Address: 0xE000EFD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.46 DPIDR5, SCS Peripheral Identification Register 5" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.72 CM33_SCS_PIDR6

Description: Peripheral Identification Register 6

Address: 0xE000EFD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.47 DPIDR5, SCS Peripheral Identification Register 6" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.73 CM33_SCS_PIDR7

Description: Peripheral Identification Register 7

Address: 0xE000EFDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.48 DPIDR7, SCS Peripheral Identification Register 7" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.74 CM33_SCS_PIDR0

Description: Peripheral Identification Register 0

Address: 0xE000EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.41 DPIDR0, SCS Peripheral Identification Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000021

10.1.75 CM33_SCS_PIDR1

Description: Peripheral Identification Register 1

Address: 0xE000EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.42 DPIDR1, SCS Peripheral Identification Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x000000BD

10.1.76 CM33_SCS_PIDR2

Description: Peripheral Identification Register 2

Address: 0xE000EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.43 DPIDR2, SCS Peripheral Identification Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0000000B

10.1.77 CM33_SCS_PIDR3

Description: Peripheral Identification Register 3

Address: 0xE000EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.44 DPIDR3, SCS Peripheral Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

10.1.78 CM33_SCS_CIDR0

Description: Component Identification Register 0

Address: 0xE000EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.26 DCIDR0, SCS Component Identification Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0000000D

10.1.79 CM33_SCS_CIDR1

Description: Component Identification Register 1

Address: 0xE000EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.27 DCIDR1, SCS Component Identification Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000090

10.1.80 CM33_SCS_CIDR2

Description: Component Identification Register 2

Address: 0xE000EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.28 DCIDR2, SCS Component Identification Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000005

10.1.81 CM33_SCS_CIDR3

Description: Component Identification Register 3

Address: 0xE000EFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.29 DCIDR3, SCS Component Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x000000B1

10.1.82 CM33_TRC_CTI_CTICONTROL

Description: CTI Control Register

Address: 0xE0080000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							GLBEN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	GLBEN	Enables or disables the ECT: 0 = disabled (reset) 1 = enabled. When disabled, all cross triggering mapping logic functionality is disabled for this processor. Default Value: 0

10.1.83 CM33_TRC_CTI_CTIINTACK

Description: CTI Interrupt Acknowledge Register

Address: 0xE0080010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	INTACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	INTACK	Acknowledges the corresponding CTITRIGOUT output: 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect. There is one bit of the register for each CTITRIGOUT output. Default Value: 0

10.1.84 CM33_TRC_CTI_CTIAPPSET

Description: CTI Application Trigger Set Register

Address: 0xE0080014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				APPSET [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	APPSET	Setting a bit HIGH generates a channel event for the selected channel. Read: 0 = application trigger inactive (reset) 1 = application trigger active. Write: 0 = no effect 1 = generate channel event. There is one bit of the register for each channel. Default Value: 0

10.1.85 CM33_TRC_CTI_CTIAPPCLEAR

Description: CTI Application Trigger Clear Register

Address: 0xE0080018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				W			
HW Access	Reserved				R			
Name	Reserved [7:4]				APPCLEAR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	APPCLEAR	Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect. There is one bit of the register for each channel. Default Value: 0

10.1.86 CM33_TRC_CTI_CTIAPPPULSE

Description: CTI Application Pulse Register

Address: 0xE008001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				W			
HW Access	Reserved				R			
Name	Reserved [7:4]				APPULSE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	APPULSE	Setting a bit HIGH generates a channel event pulse for the selected channel. Write: 1 = channel event pulse generated for one CTICLK period 0 = no effect. There is one bit of the register for each channel. Default Value: 0

10.1.87 CM33_TRC_CTI_CTIINEN0

Description: CTI Trigger to Channel Enable Registers

Address: 0xE0080020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				TRIGINEN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	TRIGINEN	Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated. 1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM. There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0. 0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. Default Value: 0

10.1.88 CM33_TRC_CTI_CTIOUTEN0

Description: CTI Channel to Trigger Enable Registers

Address: 0xE00800A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				TRIGOUTEN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	TRIGOUTEN	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output: 0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. Default Value: 0

10.1.89 CM33_TRC_CTI_CTITRIGINSTATUS

Description: CTI Trigger In Status Register

Address: 0xE0080130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRIGINSTATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	TRIGINSTATUS	Shows the status of the CTITRIGIN inputs: 1 = CTITRIGIN is active 0 = CTITRIGIN is inactive. Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. Default Value: 0

10.1.90 CM33_TRC_CTI_CTITRIGOUTSTATUS

Description: CTI Trigger Out Status Register

Address: 0xE0080134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRIGOUTSTATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	TRIGOUTSTATUS	Shows the status of the CTITRIGOUT outputs. 1 = CTITRIGOUT is active 0 = CTITRIGOUT is inactive (reset). There is one bit of the register for each trigger output. Default Value: 0

10.1.91 CM33_TRC_CTI_CTICHINSTATUS

Description: CTI Channel In Status Register

Address: 0xE0080138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				CTICHINSTATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	CTICHINSTATUS	Shows the status of the CTICHIN inputs: 1 = CTICHIN is active 0 = CTICHIN is inactive. Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. Default Value: 0

10.1.92 CM33_TRC_CTI_CTICHOUTSTATUS

Description: CTI Channel Out Status Register

Address: 0xE008013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				CTICHOUTSTATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	CTICHOUTSTATUS	Shows the status of the CTICHOUT outputs. 1 = CTICHOUT is active 0 = CTICHOUT is inactive (reset). There is one bit of the register for each channel output. Default Value: 0

10.1.93 CM33_TRC_CTI_CTIGATE

Description: Enable CTI Channel Gate Register

Address: 0xE0080140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				CTIGA-TEEN3	CTIGA-TEEN2	CTIGA-TEEN1	CTIGA-TEEN0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	CTIGATEEN3	Enable CTICHOUT3. Set to 0 to disable channel propagation. Default Value: 1
2	CTIGATEEN2	Enable CTICHOUT2. Set to 0 to disable channel propagation. Default Value: 1
1	CTIGATEEN1	Enable CTICHOUT1. Set to 0 to disable channel propagation. Default Value: 1
0	CTIGATEEN0	Enable CTICHOUT0. Set to 0 to disable channel propagation. Default Value: 1

10.1.94 CM33_TRC_CTI_ASICCTL

Description: External Multiplexor Control Register

Address: 0xE0080144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ASICCTL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	ASICCTL	Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on page 4-28. Default Value: 0

10.1.95 CM33_TRC_CTI_ITCHINACK

Description: ITCHINACK Register

Address: 0xE0080EDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				W			
HW Access	Reserved				R			
Name	Reserved [7:4]				CTCHINACK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	CTCHINACK	Set the value of the CTCHINACK outputs Default Value: 0

10.1.96 CM33_TRC_CTI_ITTRIGINACK

Description: ITTRIGINACK Register

Address: 0xE0080EE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	CTTRIGINACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	CTTRIGINACK	Set the value of the CTTRIGINACK outputs Default Value: 0

10.1.97 CM33_TRC_CTI_ITCHOUT

Description: ITCHOUT Register

Address: 0xE0080EE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				W			
HW Access	Reserved				R			
Name	Reserved [7:4]				CTCHOUT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	CTCHOUT	Set the value of the CTCHOUT outputs Default Value: 0

10.1.98 CM33_TRC_CTI_ITTRIGOUT

Description: ITTRIGOUT Register

Address: 0xE0080EE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	CTTRIGOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	CTTRIGOUT	Set the value of the CTTRIGOUT outputs Default Value: 0

10.1.99 CM33_TRC_CTI_ITCHOUTACK

Description: ITCHOUTACK Register

Address: 0xE0080EEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				CTCHOUTACK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	CTCHOUTACK	Read the values of the CTCHOUTACK inputs Default Value: 0

10.1.100 CM33_TRC_CTI_ITTRIGOUTACK

Description: ITTRIGOUTACK Register

Address: 0xE0080EF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CTTRIGOUTACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	CTTRIGOUTACK	Read the values of the CTTRIGOUTACK inputs Default Value: 0

10.1.101 CM33_TRC_CTI_ITCHIN

Description: ITCHIN Register

Address: 0xE0080EF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				CTCHIN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	CTCHIN	Read the values of the CTCHIN inputs Default Value: 0

10.1.102 CM33_TRC_CTI_ITTRIGIN

Description: ITTRIGIN Register

Address: 0xE0080EF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CTTRIGIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	CTTRIGIN	Read the values of the CTTRIGIN inputs Default Value: 0

10.1.103 CM33_TRC_CTI_ITCTRL

Description: Integration Mode Control Register

Address: 0xE0080F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							MODE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	MODE	When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. Default Value: 0

10.1.104 CM33_TRC_CTI_CLAIMSET

Description: Claim Tag Set Register

Address: 0xE0080FA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1S			
HW Access	Reserved				R			
Name	Reserved [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. Default Value: 0xF

10.1.105 CM33_TRC_CTI_CLAIMCLR

Description: Claim Tag Clear Register

Address: 0xE0080FA4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1C			
HW Access	Reserved				R			
Name	Reserved [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank that is zero at reset. Default Value: 0

10.1.106 CM33_TRC_CTI_LAR

Description: Lock Access Register

Address: 0xE0080FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LSR[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. Default Value: 0

10.1.107 CM33_TRC_CTI_LSR

Description: Lock Status Register

Address: 0xE0080FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R	R	R
HW Access	Reserved					W	W	W
Name	Reserved [7:3]					nTT	SLK	SLI

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	nTT	This component implements an 32-bit Lock Access Register. Default Value: 0
1	SLK	The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted Default Value: 1
0	SLI	Indicates that a lock control mechanism exists for this device Default Value: 1

10.1.108 CM33_TRC_CTI_AUTHSTATUS

Description: Authentication Status Register

Address: 0xE0080FB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	SNIDBG [7:6]		SIDBG [5:4]		NSNIDBG [3:2]		NSIDBG [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 6	SNIDBG	Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
5 : 4	SIDBG	Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
3 : 2	NSNIDBG	Non-Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
1 : 0	NSIDBG	Non-Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0

10.1.109 CM33_TRC_CTI_DEVID

Description: Device Configuration Register

Address: 0xE0080FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R				
HW Access	Reserved			R				
Name	Reserved [7:5]			EXTMUXNUM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	NUMTRIG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [23:20]				NUMCH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 16	NUMCH	Number of ECT channels available. Default Value: 4
15 : 8	NUMTRIG	Number of ECT triggers available. Default Value: 8
4 : 0	EXTMUXNUM	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. Default Value: 0

10.1.110 CM33_TRC_CTI_DEVTYPE

Description: Device Type Identifier Register

Address: 0xE0080FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	SUB_TYPE [7:4]				CLASS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	SUB_TYPE	cross trigger Default Value: 0x1
3 : 0	CLASS	debug control logic component Default Value: 0x4

10.1.111 CM33_TRC_CTI_PIDR4

Description: Peripheral Identification Register 4

Address: 0xE0080FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000004

10.1.112 CM33_TRC_CTI_PIDR5

Description: Peripheral Identification Register 5

Address: 0xE0080FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000000

10.1.113 CM33_TRC_CTI_PIDR6

Description: Peripheral Identification Register 6

Address: 0xE0080FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000000

10.1.114 CM33_TRC_CTI_PIDR7

Description: Peripheral Identification Register 7

Address: 0xE0080FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000000

10.1.115 CM33_TRC_CTI_PIDR0

Description: Peripheral Identification Register 0

Address: 0xE0080FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000006

10.1.116 CM33_TRC_CTI_PIDR1

Description: Peripheral Identification Register 1

Address: 0xE0080FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x000000B9

10.1.117 CM33_TRC_CTI_PIDR2

Description: Peripheral Identification Register 2

Address: 0xE0080FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x0000005B

10.1.118 CM33_TRC_CTI_PIDR3

Description: Peripheral Identification Register 3

Address: 0xE0080FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved			
HW Access	R				Reserved			
Name	ECOREVNUM [7:4]				Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	ECO revision for MTB Default Value: 0x0

10.1.119 CM33_TRC_CTI_CIDR0

Description: Component Identification Register 0

Address: 0xE0080FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x0000000D

10.1.120 CM33_TRC_CTI_CIDR1

Description: Component Identification Register 1

Address: 0xE0080FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000090

10.1.121 CM33_TRC_CTI_CIDR2

Description: Component Identification Register 2

Address: 0xE0080FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000005

10.1.122 CM33_TRC_CTI_CIDR3

Description: Component Identification Register 3

Address: 0xE0080FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x000000B1

10.1.123 CM33_CSTF_FUNNELCONTROL

Description: Funnel Control Register

Address: 0xE0088000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.1 css600_atbfunnel Funnel Control register, FUNNELCONTROL" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000300

10.1.124 CM33_CSTF_PRIORITYCONTROL

Description: Priority Control Register

Address: 0xE0088004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.2 css600_atbfunnel Priority Control register, PRIORITYCONTROL" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.125 CM33_CSTF_ITATBDATA0

Description: Integration Register

Address: 0xE0088EEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.3 css600_atbfunnel Integration test data register, ITATBDATA0" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.126 CM33_CSTF_ITATBCTR3

Description: Integration Register

Address: 0xE0088EF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.4 css600_atbfunnel Integration test control register 3, ITATBCTR3" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.127 CM33_CSTF_ITATBCTR2

Description: Integration Register

Address: 0xE0088EF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.5 css600_atbfunnel Integration test control register 2, ITATBCTR2" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.128 CM33_CSTF_ITATBCTR1

Description: Integration Register

Address: 0xE0088EF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.6 css600_atbfunnel Integration test control register 1, ITATBCTR1" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.129 CM33_CSTF_ITATBCTR0

Description: Integration Register

Address: 0xE0088EFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.7 css600_atbfunnel Integration test control register 0, ITATBCTR0" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.130 CM33_CSTF_ITCTRL

Description: Integration Mode Control Register

Address: 0xE0088F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.8 css600_atbfunnel Integration Mode Control Register, ITCTRL" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.131 CM33_CSTF_CLAIMSET

Description: Claim Tag Set Register

Address: 0xE0088FA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.9 css600_atbfunnel Claim Tag Set Register, CLAIMSET" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0xF

10.1.132 CM33_CSTF_CLAIMCLR

Description: Claim Tag Clear Register

Address: 0xE0088FA4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.10 css600_atbfunnel Claim Tag Clear Register, CLAIMCLR" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.133 CM33_CSTF_DEVAFF0

Description: Device Affinity Register0

Address: 0xE0088FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.11 css600_atbfunnel Device Affinity register 0, DEVAFF0" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.134 CM33_CSTF_DEVAFF1

Description: Device Affinity Register1

Address: 0xE0088FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.12 css600_atbfunnel Device Affinity register 1, DEVAFF1" in ARM Core-Sight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x3

10.1.135 CM33_CSTF_AUTHSTATUS

Description: Authentication Status Register

Address: 0xE0088FB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.13 css600_atbfunnel Authentication Status Register, AUTHSTATUS" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.136 CM33_CSTF_DEVARCH

Description: Device Architecture Register

Address: 0xE0088FBC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.14 css600_atbfunnel Device Architecture Register, DEVARCH" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

10.1.137 CM33_CSTF_DEVID2

Description: Device Configuration Register 2

Address: 0xE0088FC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.15 css600_atbfunnel Device Configuration Register 2, DEVID2" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000000

10.1.138 CM33_CSTF_DEVID1

Description: Device Configuration Register 1

Address: 0xE0088FC4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.16 css600_atbfunnel Device Configuration Register 1, DEVID1" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000000

10.1.139 CM33_CSTF_DEVID

Description: Device Configuration Register

Address: 0xE0088FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.17 css600_atbfunnel Device Configuration Register, DEVID" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x0000003X

10.1.140 CM33_CSTF_DEVTYPE

Description: Device Type Identifier Register

Address: 0xE0088FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.18 css600_atbfunnel Device Type Identifier Register, DEVTYPE" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000012

10.1.141 CM33_CSTF_PIDR4

Description: Peripheral Identification Register 4

Address: 0xE0088FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.19 css600_atbfunnel Peripheral Identification Register 4, PIDR4" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000004

10.1.142 CM33_CSTF_PIDR5

Description: Peripheral Identification Register 5

Address: 0xE0088FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.20 css600_atbfunnel Peripheral Identification Register 5, PIDR5" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000000

10.1.143 CM33_CSTF_PIDR6

Description: Peripheral Identification Register 6

Address: 0xE0088FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.21 css600_atbfunnel Peripheral Identification Register 6, PIDR6" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000000

10.1.144 CM33_CSTF_PIDR7

Description: Peripheral Identification Register 7

Address: 0xE0088FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.22 css600_atbfunnel Peripheral Identification Register 7, PIDR7" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000000

10.1.145 CM33_CSTF_PIDR0

Description: Peripheral Identification Register 0

Address: 0xE0088FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.23 css600_atbfunnel Peripheral Identification Register 0, PIDR0" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x000000EB

10.1.146 CM33_CSTF_PIDR1

Description: Peripheral Identification Register 1

Address: 0xE0088FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.24 css600_atbfunnel Peripheral Identification Register 1, PIDR1" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x000000B9

10.1.147 CM33_CSTF_PIDR2

Description: Peripheral Identification Register 2

Address: 0xE0088FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.25 css600_atbfunnel Peripheral Identification Register 2, PIDR2" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x0000002B

10.1.148 CM33_CSTF_PIDR3

Description: Peripheral Identification Register 3

Address: 0xE0088FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved			
HW Access	R				Reserved			
Name	ECOREVNUM [7:4]				Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer "10.11.2.26 css600_atbfunnel Peripheral Identification Register 3, PIDR3" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x0

10.1.149 CM33_CSTF_CIDR1

Description: Component Identification Register 1

Address: 0xE0088FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.28 css600_atbfunnel Component Identification Register 1, CIDR1" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000090

10.1.150 CM33_CSTF_CIDR2

Description: Component Identification Register 2

Address: 0xE0088FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.29 css600_atbfunnel Component Identification Register 2, CIDR2" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000005

10.1.151 CM33_CSTF_CIDR3

Description: Component Identification Register 3

Address: 0xE0088FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.30 css600_atbfunnel Component Identification Register 3, CIDR3" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x000000B1

10.1.152 CM33_ETF_RSZ

Description: RAM Size register

Address: 0xE008D004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE0 [31:24]							

Bits	Name	Description
31 : 0	VALUE0	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.153 CM33_ETF_STS

Description: Status Register

Address: 0xE008D00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE1 [31:24]							

Bits	Name	Description
31 : 0	VALUE1	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.154 CM33_ETF_RRD

Description: RAM Read Data Register

Address: 0xE008D010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE2 [31:24]							

Bits	Name	Description
31 : 0	VALUE2	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.155 CM33_ETF_RRP

Description: RAM Read Pointer Register

Address: 0xE008D014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE3 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE3 [31:24]							

Bits	Name	Description
31 : 0	VALUE3	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.156 CM33_ETF_RWP

Description: RAM Write Pointer Register

Address: 0xE008D018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE4 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE4 [31:24]							

Bits	Name	Description
31 : 0	VALUE4	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.157 CM33_ETF_TRG

Description: Trigger Counter Register

Address: 0xE008D01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE5 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE5 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE5 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE5 [31:24]							

Bits	Name	Description
31 : 0	VALUE5	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.158 CM33_ETF_CTL

Description: Control Register

Address: 0xE008D020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE6 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE6 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE6 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE6 [31:24]							

Bits	Name	Description
31 : 0	VALUE6	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.159 CM33_ETF_RWD

Description: RAM Write Data Register

Address: 0xE008D024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE7 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE7 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE7 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE7 [31:24]							

Bits	Name	Description
31 : 0	VALUE7	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.160 CM33_ETF_MODE

Description: Mode Register

Address: 0xE008D028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE8 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE8 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE8 [31:24]							

Bits	Name	Description
31 : 0	VALUE8	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.161 CM33_ETF_LBUFLEVEL

Description: Latched Buffer Fill Level

Address: 0xE008D02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE9 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE9 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE9 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE9 [31:24]							

Bits	Name	Description
31 : 0	VALUE9	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.162 CM33_ETF_CBUFLEVEL

Description: Current Buffer Fill Level

Address: 0xE008D030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE10 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE10 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE10 [31:24]							

Bits	Name	Description
31 : 0	VALUE10	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.163 CM33_ETF_BUFWM

Description: Buffer Level Water Mark

Address: 0xE008D034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE11 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE11 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE11 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE11 [31:24]							

Bits	Name	Description
31 : 0	VALUE11	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.164 CM33_ETF_FFSR

Description: Formatter and Flush Status Register

Address: 0xE008D300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE12 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE12 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE12 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE12 [31:24]							

Bits	Name	Description
31 : 0	VALUE12	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.165 CM33_ETF_FFCR

Description: Formatter and Flush Control Register

Address: 0xE008D304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE13 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE13 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE13 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE13 [31:24]							

Bits	Name	Description
31 : 0	VALUE13	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.166 CM33_ETF_PSCR

Description: Periodic Synchronization Counter Register

Address: 0xE008D308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE14 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE14 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE14 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE14 [31:24]							

Bits	Name	Description
31 : 0	VALUE14	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x0000000A

10.1.167 CM33_ETF_ITATBMDATA0

Description: Integration Test ATB Master Data 0 Register

Address: 0xE008DED0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE15 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE15 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE15 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE15 [31:24]							

Bits	Name	Description
31 : 0	VALUE15	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.168 CM33_ETF_ITATBMCTR2

Description: Integration Test ATB Master Interface Control 2 Register

Address: 0xE008DED4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE16 [31:24]							

Bits	Name	Description
31 : 0	VALUE16	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.169 CM33_ETF_ITATBMCTR1

Description: Integration Test ATB Master Interface Control 1 Register

Address: 0xE008DED8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE17 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE17 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE17 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE17 [31:24]							

Bits	Name	Description
31 : 0	VALUE17	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.170 CM33_ETF_ITATBMCTR0

Description: Integration Test ATB Master Interface Control 0 Registe

Address: 0xE008DEDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE18 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE18 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE18 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE18 [31:24]							

Bits	Name	Description
31 : 0	VALUE18	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.171 CM33_ETF_ITEVTINTR

Description: Integration Test Event & Interrupt Status Register

Address: 0xE008DEE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE19 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE19 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE19 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE19 [31:24]							

Bits	Name	Description
31 : 0	VALUE19	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.172 CM33_ETF_ITTRFLIN

Description: Integration Test Trigger In and Flush In Register

Address: 0xE008DEE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE20 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE20 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE20 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE20 [31:24]							

Bits	Name	Description
31 : 0	VALUE20	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.173 CM33_ETF_ITATBDATA0

Description: Integration Test ATB Data 0 Register

Address: 0xE008DEEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE21 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE21 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE21 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE21 [31:24]							

Bits	Name	Description
31 : 0	VALUE21	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.174 CM33_ETF_ITATBCTR2

Description: Integration Test ATB Control 2 Register

Address: 0xE008DEF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE22 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE22 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE22 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE22 [31:24]							

Bits	Name	Description
31 : 0	VALUE22	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.175 CM33_ETF_ITATBCTR1

Description: Integration Test ATB Control 1 Register

Address: 0xE008DEF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE23 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE23 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE23 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE23 [31:24]							

Bits	Name	Description
31 : 0	VALUE23	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.176 CM33_ETF_ITATBCTR0

Description: Integration Test ATB Control 0 Register

Address: 0xE008DEF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE24 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE24 [31:24]							

Bits	Name	Description
31 : 0	VALUE24	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.177 CM33_ETF_ITCTRL

Description: Integration Mode Control Register

Address: 0xE008DF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE25 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE25 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE25 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE25 [31:24]							

Bits	Name	Description
31 : 0	VALUE25	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.178 CM33_ETF_CLAIMSET

Description: Claim Tag Set Register

Address: 0xE008DFA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RAZWI				RW1S			
HW Access	R				R			
Name	VALUE26 [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RAZWI							
HW Access	R							
Name	VALUE26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RAZWI							
HW Access	R							
Name	VALUE26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RAZWI							
HW Access	R							
Name	VALUE26 [31:24]							

Bits	Name	Description
31 : 4	VALUE26	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0
3 : 0	TAG	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0xF

10.1.179 CM33_ETF_CLAIMCLR

Description: Claim Tag Clear Register

Address: 0xE008DFA4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RAZWI				RW1C			
HW Access	R				R			
Name	VALUE27 [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RAZWI							
HW Access	R							
Name	VALUE27 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RAZWI							
HW Access	R							
Name	VALUE27 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RAZWI							
HW Access	R							
Name	VALUE27 [31:24]							

Bits	Name	Description
31 : 4	VALUE27	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0
3 : 0	TAG	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

10.1.180 CM33_ETF_AUTHSTATUS

Description: Authentication Status Register

Address: 0xE008DFB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	SNIDBG [7:6]		SIDBG [5:4]		NSNIDBG [3:2]		NSIDBG [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R				R		R	
HW Access	R				W		W	
Name	RES0_1 [15:12]				HNIDBG [11:10]		HIDBG [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RES0_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RES0_1 [31:24]							

Bits	Name	Description
31 : 12	RES0_1	RESERVED Default Value: 0
11 : 10	HNIDBG	Hypervisor non-invasive debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
9 : 8	HIDBG	Hypervisor invasive debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
7 : 6	SNIDBG	Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
5 : 4	SIDBG	Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0

10.1.180 CM33_ETF_AUTHSTATUS (continued)

3 : 2	NSNIDBG	Non-Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
1 : 0	NSIDBG	Non-Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0

10.1.181 CM33_ETF_DEVID1

Description: Device Configuration Register 1

Address: 0xE008DFC4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							R
HW Access	R							R
Name	RES0_2 [7:1]							RMC

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	RES0_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RES0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RES0_2 [31:24]							

Bits	Name	Description
31 : 1	RES0_2	RESERVED Default Value: 0
0	RMC	Registr Management mode Default Value: 1

10.1.182 CM33_ETF_DEVID

Description: Device Configuration Register

Address: 0xE008DFC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R	R				
HW Access	R		R	R				
Name	CONFIGTYPE [7:6]		CLKSCHEME	ATBINPORTCOUNT [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R					R		
HW Access	R					R		
Name	RES0_3 [15:11]					MEMWIDTH [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RES0_3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RES0_3 [31:24]							

Bits	Name	Description
31 : 11	RES0_3	RESERVED Default Value: 0
10 : 8	MEMWIDTH	This value is twice ATB_DATA_WIDTH. 0x3 Memory interface databus is 64-bits wide. (ATB_-DATA_WIDTH= 32bit) 0x4 Memory interface databus is 128-bits wide. (ATB_DATA_WIDTH= 64bit) 0x5 Memory interface databus is 256-bits wide. (ATB_DATA_WIDTH= 128bit) Default Value: 0
7 : 6	CONFIGTYPE	Returns 0x2, indicating ETF configuration Default Value: 0x2
5	CLKSCHEME	RAM Clocking Scheme. This value indicates the TMC RAM clocking scheme used, that is, whether the TMC RAM operates synchronously or asynchronously to the TMC clock. Fixed to 0 indicating that TMC RAM clock is synchronous to the clk input Default Value: 0
4 : 0	ATBINPORTCOUNT	Hidden Level of ATB input multiplexing. This value indicates the type/ number of ATB multiplex-ing present on the input ATB. Fixed to 0x00 indicating that no multiplexing is present. Default Value: 0

10.1.183 CM33_ETF_DEVTYPE

Description: Device Type Identifier Register

Address: 0xE008DFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	SUB_TYPE [7:4]				MAJOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	RES0_4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RES0_4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RES0_4 [31:24]							

Bits	Name	Description
31 : 8	RES0_4	Reserved Default Value: 0
7 : 4	SUB_TYPE	Minor classification. Returns 0x3, indicating this component is a FIFO Default Value: 0x3
3 : 0	MAJOR	Major classification. Returns 0x2, indicating this component is a Trace Link Default Value: 0x2

10.1.184 CM33_ETF_PIDR4

Description: Peripheral Identification Register 4

Address: 0xE008DFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE28 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE28 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE28 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE28 [31:24]							

Bits	Name	Description
31 : 0	VALUE28	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000004

10.1.185 CM33_ETF_PIDR5

Description: Peripheral Identification Register 5

Address: 0xE008DFD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE29 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE29 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE29 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE29 [31:24]							

Bits	Name	Description
31 : 0	VALUE29	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000000

10.1.186 CM33_ETF_PIDR6

Description: Peripheral Identification Register 6

Address: 0xE008DFD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE30 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE30 [31:24]							

Bits	Name	Description
31 : 0	VALUE30	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000000

10.1.187 CM33_ETF_PIDR7

Description: Peripheral Identification Register 7

Address: 0xE008DFDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE31 [31:24]							

Bits	Name	Description
31 : 0	VALUE31	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000000

10.1.188 CM33_ETF_PIDR0

Description: Peripheral Identification Register 0

Address: 0xE008DFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE32 [31:24]							

Bits	Name	Description
31 : 0	VALUE32	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x000000EA

10.1.189 CM33_ETF_PIDR1

Description: Peripheral Identification Register 1

Address: 0xE008DFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE33 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE33 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE33 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE33 [31:24]							

Bits	Name	Description
31 : 0	VALUE33	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x000000B9

10.1.190 CM33_ETF_PIDR2

Description: Peripheral Identification Register 2

Address: 0xE008DFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE34 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE34 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE34 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE34 [31:24]							

Bits	Name	Description
31 : 0	VALUE34	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x0000004B

10.1.191 CM33_ETF_PIDR3

Description: Peripheral Identification Register 3

Address: 0xE008DFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved			
HW Access	R				Reserved			
Name	ECOREVNUM [7:4]				Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x0

10.1.192 CM33_ETF_CIDR0

Description: Component Identification Register 0

Address: 0xE008DFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE35 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE35 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE35 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE35 [31:24]							

Bits	Name	Description
31 : 0	VALUE35	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x000000D

10.1.193 CM33_ETF_CIDR1

Description: Component Identification Register 1

Address: 0xE008DFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE36 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE36 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE36 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE36 [31:24]							

Bits	Name	Description
31 : 0	VALUE36	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000090

10.1.194 CM33_ETF_CIDR2

Description: Component Identification Register 2

Address: 0xE008DFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE37 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE37 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE37 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE37 [31:24]							

Bits	Name	Description
31 : 0	VALUE37	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000005

10.1.195 CM33_ETF_CIDR3

Description: Component Identification Register 3

Address: 0xE008DFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE38 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE38 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE38 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE38 [31:24]							

Bits	Name	Description
31 : 0	VALUE38	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x000000B1

10.1.196 CM33_CSS600_TPIU_TPIU_SSPSR

Description: Supported Parallel Port Size Register

Address: 0xE008E000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.213 TPIU_SSPSR, TPIU Supported Parallel Port Sizes Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: X

10.1.197 CM33_CSS600_TPIU_TPIU_CSPSR

Description: Current Parallel Port Size Register

Address: 0xE008E004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.197 TPIU_CSPSR, TPIU Current Parallel Port Sizes Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x1

10.1.198 CM33_CSS600_TPIU_TPIU_STMR

Description: Supported Trigger Model Register

Address: 0xE008E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	0: MULT2 1: MULT4 2: MULT6 3: MULT256 4: MULT64K 7:5 : RES0 8: TCOUNT8 15:9: RES0 16: TRIGGERED 17: TrgRun 31:18: RES0 Default Value: 0x0000011F

10.1.199 CM33_CSS600_TPIU_TPIU_TCVR

Description: Trigger Counter Value Register

Address: 0xE008E104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	7:0 : TrigCount 31:8 : RES0 Default Value: 0x00000000

10.1.200 CM33_CSS600_TPIU_TPIU_TCMR

Description: Trigger Counter Multiplier Register

Address: 0xE008E108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	7:0 : TrigCount 31:8 : RES0 Default Value: 0x00000000

10.1.201 CM33_CSS600_TPIU_TPIU_STPMR

Description: Supported Test Patterns Modes Register

Address: 0xE008E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	0 : MULT2 1 : MULT4 2 : MULT16 3 : MULT256 4 : MULT64K 31:5 : RES0 Default Value: 0x00000000

10.1.202 CM33_CSS600_TPIU_TPIU_CTPMR

Description: Current Test Patterns Modes Register

Address: 0xE008E204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	0 : PATW1 1 : PATW0 2 : PATA5 3 : PATAF0 15:4 :RES0 16 : PTIMEEN 17 : PCONTEN 31:18 : RES0 Default Value: 0x00000000

10.1.203 CM33_CSS600_TPIU_TPIU_TPRCR

Description: Test Pattern Repeat Counter Register

Address: 0xE008E208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

10.1.204 CM33_CSS600_TPIU_TPIU_FFSR

Description: Formatter and Flush Status Register

Address: 0xE008E300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.200 TPIU_FFSR, TPIU Formatter and Flush Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: X

10.1.205 CM33_CSS600_TPIU_TPIU_FFCR

Description: Formatter and Flush Control Register

Address: 0xE008E304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.199 TPIU_FFCR, TPIU Formatter and Flush Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00001000

10.1.206 CM33_CSS600_TPIU_TPIU_FSCR

Description: Formatter Synchronization Count Register

Address: 0xE008E308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.211 TPIU_PSCR, TPIU Periodic Synchronization Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000040

10.1.207 CM33_CSS600_TPIU_TPIU_EXTCTLIN

Description: External Control Port In Register

Address: 0xE008E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000XX

10.1.208 CM33_CSS600_TPIU_TPIU_EXTCTLOUT

Description: External Control Port Out Register

Address: 0xE008E404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

10.1.209 CM33_CSS600_TPIU_ITTRFLIN

Description: Integration Test Trigger In Flush In Register

Address: 0xE008EEE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0

10.1.210 CM33_CSS600_TPIU_ITATBDATA0

Description: Integration Test ATB Data Register0

Address: 0xE008EEEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 0	VALUE0	Default Value: 0

10.1.211 CM33_CSS600_TPIU_ITATBCTR2

Description: Integration Test ATB Control Register 2

Address: 0xE008EEF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0

10.1.212 CM33_CSS600_TPIU_ITATBCTR1

Description: Integration Test ATB Control Register 1

Address: 0xE008EEF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0

10.1.213 CM33_CSS600_TPIU_ITATBCTR0

Description: Integration Test ATB Control Register 0

Address: 0xE008EEF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0

10.1.214 CM33_CSS600_TPIU_ITOUTCTR

Description: Integration Test Output Control Register

Address: 0xE008EEFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0

10.1.215 CM33_CSS600_TPIU_ITCTRL

Description: Integration Mode Control Register

Address: 0xE008EF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	MODE	Specifies the current mode for the TPIU: 0b00 Normal mode. 0b01 Integration test mode. 0b10 Integration data test mode. 0b11 Reserved. In integration data test mode, the trace output is disabled, and data can be read directly from each input port using the integration data registers. Default Value: 0

10.1.216 CM33_CSS600_TPIU_CLAIMSET

Description: Claim Tag Set Register

Address: 0xE008EFA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1S			
HW Access	Reserved				R			
Name	Reserved [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. Default Value: 0xF

10.1.217 CM33_CSS600_TPIU_CLAIMCLR

Description: Claim Tag Clear Register

Address: 0xE008EFA4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1C			
HW Access	Reserved				R			
Name	Reserved [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank that is zero at reset Default Value: 0

10.1.218 CM33_CSS600_TPIU_AUTHSTATUS

Description: Authentication Status Register

Address: 0xE008EFB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	TAG	Default Value: 0

10.1.219 CM33_CSS600_TPIU_DEVARCH

Description: Device Architecture Register

Address: 0xE008EFBC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	TAG	Default Value: 0

10.1.220 CM33_CSS600_TPIU_DEVID

Description: Device ID

Address: 0xE008EFC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "B.3.10 Device Configuration Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000020

10.1.221 CM33_CSS600_TPIU_DEVTYPE

Description: Device Type Identifier Register

Address: 0xE008EFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "B.3.11 Device Type Identifier Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x11

10.1.222 CM33_CSS600_TPIU_PIDR4

Description: Peripheral Identification Register 4

Address: 0xE008EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.207 TPIU_PIDR4, TPIU Peripheral Identification Register 4" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000004

10.1.223 CM33_CSS600_TPIU_PIDR5

Description: Peripheral Identification Register 5

Address: 0xE008EFD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.208 TPIU_PIDR5, TPIU Peripheral Identification Register 5" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000000

10.1.224 CM33_CSS600_TPIU_PIDR6

Description: Peripheral Identification Register 6

Address: 0xE008EFD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

10.1.225 CM33_CSS600_TPIU_PIDR7

Description: Peripheral Identification Register 7

Address: 0xE008EFDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.210 TPIU_PIDR7, TPIU Peripheral Identification Register 7" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000000

10.1.226 CM33_CSS600_TPIU_PIDR0

Description: Peripheral Identification Register 0

Address: 0xE008EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.203 TPIU_PIDR0, TPIU Peripheral Identification Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x000000E7

10.1.227 CM33_CSS600_TPIU_PIDR1

Description: Peripheral Identification Register 1

Address: 0xE008EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.204 TPIU_PIDR1, TPIU Peripheral Identification Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000089

10.1.228 CM33_CSS600_TPIU_PIDR2

Description: Peripheral Identification Register 2

Address: 0xE008EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.205 TPIU_PIDR2, TPIU Peripheral Identification Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0000002B

10.1.229 CM33_CSS600_TPIU_PIDR3

Description: Peripheral Identification Register 3

Address: 0xE008EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved			
HW Access	R				Reserved			
Name	ECOREVNUM [7:4]				Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer "D2.2.206 TPIU_PIDR3, TPIU Peripheral Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000000

10.1.230 CM33_CSS600_TPIU_CIDR0

Description: Component Identification Register 0

Address: 0xE008EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.206 TPIU_PIDR3, TPIU Peripheral Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0000008D

10.1.231 CM33_CSS600_TPIU_CIDR1

Description: Component Identification Register 1

Address: 0xE008EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.206 TPIU_PIDR3, TPIU Peripheral Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000090

10.1.232 CM33_CSS600_TPIU_CIDR2

Description: Component Identification Register 2

Address: 0xE008EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.195 TPIU_CIDR2, TPIU Component Identification Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000005

10.1.233 CM33_CSS600_TPIU_CIDR3

Description: Component Identification Register 3

Address: 0xE008EFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.196 TPIU_CIDR3, TPIU Component Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x000000B1

10.1.234 SYSAP_ROMTABLE_DID

Description: Device Type Identifier register.

Address: 0xE00BEFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Identifies the classification of the debug component. Default Value: 0x00000001

10.1.235 SYSAP_ROMTABLE_PID4

Description: Peripheral Identification Register 4.

Address: 0xE00BEFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	COUNT	Size of ROM Table is 2^COUNT * 4 KByte. Default Value: 0
3 : 0	JEP_CONTINUATION	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. Default Value: Undefined

10.1.236 SYSAP_ROMTABLE_PID5

Description: Peripheral Identification Register 5.

Address: 0xE00BEFD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Reserved Default Value: 0

10.1.237 SYSAP_ROMTABLE_PID6

Description: Peripheral Identification Register 6.

Address: 0xE00BEFD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Reserved Default Value: 0

10.1.238 SYSAP_ROMTABLE_PID7

Description: Peripheral Identification Register 7.

Address: 0xE00BEFDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Reserved Default Value: 0

10.1.239 SYSAP_ROMTABLE_PID0

Description: Peripheral Identification Register 0.

Address: 0xE00BEFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PN_MIN	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. Default Value: Undefined

10.1.240 SYSAP_ROMTABLE_PID1

Description: Peripheral Identification Register 1.

Address: 0xE00BEFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	JEPID_MIN	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. Default Value: Undefined
3 : 0	PN_MAJ	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. Default Value: Undefined

10.1.241 SYSAP_ROMTABLE_PID2

Description: Peripheral Identification Register 2.

Address: 0xE00BEFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved	R		
HW Access	R				Reserved	R		
Name	REV [7:4]				Reserved	JEPID_MAJ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	REV	Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is incremented on subsequent tape outs. Default Value: Undefined
2 : 0	JEPID_MAJ	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. Default Value: Undefined

10.1.242 SYSAP_ROMTABLE_PID3

Description: Peripheral Identification Register 3.

Address: 0xE00BEFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	REV_AND	Minor REVision number (chip specific). For first tape out: 0x1. This field is incremented on subsequent tape outs. Default Value: Undefined
3 : 0	CM	Customer modified field. This field is used to track modifications to the original component design as a result of component IP reuse. Default Value: 0

10.1.243 SYSAP_ROMTABLE_CID0

Description: Component Identification Register 0.

Address: 0xE00BEFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 0 of 4-byte component identification 0xB105:100D. Default Value: 0x0000000D

10.1.244 SYSAP_ROMTABLE_CID1

Description: Component Identification Register 1.

Address: 0xE00BEFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: "ROM Table". Default Value: 0x00000010

10.1.245 SYSAP_ROMTABLE_CID2

Description: Component Identification Register 2.

Address: 0xE00BEFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 2 of 4-byte component identification 0xB105:100D. Default Value: 0x00000005

10.1.246 SYSAP_ROMTABLE_CID3

Description: Component Identification Register 3.

Address: 0xE00BEFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 3 of 4-byte component identification 0xB105:100D. Default Value: 0x000000B1

10.1.247 CM33_ROMTABLE_TRC_CTI

Description: CM33 CoreSight ROM Table Peripheral #0

Address: 0xE00BF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to TRC_CTI component Default Value: 0xFFFC1003

10.1.248 CM33_ROMTABLE_TRC_ETB_CSTF

Description: CM33 CoreSight ROM Table Peripheral #1

Address: 0xE00BF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ETB funnel component Note that this entry is present only for the products which has ETB. For the products that has no ETB, this field read as 0xffffd002. Default Value: 0xFFFFD003

10.1.249 CM33_ROMTABLE_TRC_ETB

Description: CM33 CoreSight ROM Table Peripheral #2

Address: 0xE00BF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ETB component. Note that this entry is present only for the products which has ETB. For the products that has no ETB, this field read as 0xfffce002. Default Value: 0xFFFCE003

10.1.250 CM33_ROMTABLE_TRC_TPIU

Description: CM33 CoreSight ROM Table Peripheral #3

Address: 0xE00BF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to TPIU component. For the products that doesn't have TPIU, this field reads as 0xfffcf002. Default Value: 0xFFFCF003

10.1.251 CM33_ROMTABLE_TRC_ETM_CSTF

Description: CM33 CoreSight ROM Table Peripheral #4

Address: 0xE00BF010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ETM funnel component. Note that this entry is present only for the products which does not have 2nd CM33 (i.e. CM33_1). This field read as 0xfffca002 for products without CM33_1. Default Value: 0xFFFCA003

10.1.252 CM33_ROMTABLE_TRC_ITM_CSTF

Description: CM33 CoreSight ROM Table Peripheral #5

Address: 0xE00BF014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ITM funnel component. Note that this entry is present only for the products which does not have 2nd CM33 (i.e. CM33_1). This field read as 0xfffc9002 for products without CM33_1. Default Value: 0xFFFC9003

10.1.253 CM33_ROMTABLE_CM33

Description: CM33 CoreSight ROM Table Peripheral #6

Address: 0xE00BF018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to CM33_0 internal ROM Table (i.e. CM33_ROM) Default Value: 0x00040003

10.1.254 CM33_ROMTABLE_CSMT

Description: CM33 CoreSight ROM Table Memory Type

Address: 0xE00BFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

10.1.255 CM33_ROMTABLE_PID4

Description: CM33 CoreSight ROM Table Peripheral ID #4

Address: 0xE00BFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 0x00000004

10.1.256 CM33_ROMTABLE_PID0

Description: CM33 CoreSight ROM Table Peripheral ID #0

Address: 0xE00BFFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 0x000000C0

10.1.257 CM33_ROMTABLE_PID1

Description: CM33 CoreSight ROM Table Peripheral ID #1

Address: 0xE00BFFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 0x000000B4

10.1.258 CM33_ROMTABLE_PID2

Description: CM33 CoreSight ROM Table Peripheral ID #2

Address: 0xE00BFFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 0x0000000B

10.1.259 CM33_ROMTABLE_PID3

Description: CM33 CoreSight ROM Table Peripheral ID #3

Address: 0xE00BFFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

10.1.260 CM33_ROMTABLE_CID0

Description: CM33 CoreSight ROM Table Component ID #0

Address: 0xE00BFFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 0x0000000D

10.1.261 CM33_ROMTABLE_CID1

Description: CM33 CoreSight ROM Table Component ID #1

Address: 0xE00BFFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 0x00000010

10.1.262 CM33_ROMTABLE_CID2

Description: CM33 CoreSight ROM Table Component ID #2

Address: 0xE00BFFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 0x00000005

10.1.263 CM33_ROMTABLE_CID3

Description: CM33 CoreSight ROM Table Component ID #3

Address: 0xE00BFFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 0x000000B1

10.1.264 CM33_ROM_SCS

Description: CM33 CoreSight ROM Table Peripheral #0

Address: 0xE00FF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to SCS ROM Table Default Value: 0xFFF0F003

10.1.265 CM33_ROM_DWT

Description: CM33 CoreSight ROM Table Peripheral #1

Address: 0xE00FF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to DWT ROM Table. Reads as 0xfff02002 if DWT is not present in system. Default Value: 0xFFF02003

10.1.266 CM33_ROM_FPB

Description: CM33 CoreSight ROM Table Peripheral #2

Address: 0xE00FF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to BPU ROM Table. Reads as 0xfff03002 if BPU is not present. Default Value: 0xFFF03003

10.1.267 CM33_ROM_ITM

Description: CM33 CoreSight ROM Table Peripheral #3

Address: 0xE00FF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ITM ROM Table. Reads as 0xfff01002 if ITM is not present. Default Value: 0xFFF01003

10.1.268 CM33_ROM_ETM

Description: CM33 CoreSight ROM Table Peripheral #4

Address: 0xE00FF014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ETM ROM Table. Reads as 0xfff42002 if ETM is not present. Default Value: 0xFFF42003

10.1.269 CM33_ROM_CTI

Description: CM33 CoreSight ROM Table Peripheral #5

Address: 0xE00FF018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to CTI ROM Table. Reads as 0xfff43002 if CTI is not present. Default Value: 0xFFF43003

10.1.270 CM33_ROM_MTB

Description: CM33 CoreSight ROM Table Peripheral #6

Address: 0xE00FF01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to MTB ROM Table. Reads as 0xfff42002 if MTB is not present. Default Value: 0xFFF44002

10.1.271 CM33_ROM_CSMT

Description: CM33 CoreSight ROM Table Memory Type

Address: 0xE00FFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

10.1.272 CM33_ROM_PID4

Description: CM33 CoreSight ROM Table Peripheral ID #4

Address: 0xE00FFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 0x00000004

10.1.273 CM33_ROM_PID0

Description: CM33 CoreSight ROM Table Peripheral ID #0

Address: 0xE00FFFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 0x000000C0

10.1.274 CM33_ROM_PID1

Description: CM33 CoreSight ROM Table Peripheral ID #1

Address: 0xE00FFFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 0x000000B4

10.1.275 CM33_ROM_PID2

Description: CM33 CoreSight ROM Table Peripheral ID #2

Address: 0xE00FFFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 0x0000000B

10.1.276 CM33_ROM_PID3

Description: CM33 CoreSight ROM Table Peripheral ID #3

Address: 0xE00FFFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

10.1.277 CM33_ROM_CID0

Description: CM33 CoreSight ROM Table Component ID #0

Address: 0xE00FFFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 0x0000000D

10.1.278 CM33_ROM_CID1

Description: CM33 CoreSight ROM Table Component ID #1

Address: 0xE00FFFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 0x00000010

10.1.279 CM33_ROM_CID2

Description: CM33 CoreSight ROM Table Component ID #2

Address: 0xE00FFFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 0x00000005

10.1.280 CM33_ROM_CID3

Description: CM33 CoreSight ROM Table Component ID #3

Address: 0xE00FFFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 0x000000B1

11 Protection Units registers

This section discusses the Peripheral Protection Control (PPC) registers. It lists all the registers in mapping tables, in address order.

For more details on Memory Protection Controller (MPC) registers of different memories present in the MCU, see the following chapters:

- **SRAM Controller registers**
- **System-on-Chip Memory (SoCMEM) registers**
- **Non-Volatile Memory (NVM) registers**
- **Serial Memory Interface (SMIF) registers**

For details on Master Control and Protection Context registers, see the following chapter:

- **CPU Sub System (CPUSS) registers**

11.1 Register details

Register name	Address	Description
PPC0_PPC_CTL	0x42020000	PPC Control Registers
PPC0_PPC_LOCK_MASK	0x4202000C	Locked Mask
PPC0_PPC_PC_MASK0	0x42021000	Protection Context Mask. This is the starting address of a register bank containing 319 registers (PPC0_PPC_PC_MASK0 to PPC0_PPC_PC_MASK318).
PPC0_PPC_NS_ATT0	0x42022000	Non-secure attribute
PPC0_PPC_NS_ATT1	0x42022004	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT2	0x42022008	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT3	0x4202200C	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT4	0x42022010	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT5	0x42022014	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT6	0x42022018	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT7	0x4202201C	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT8	0x42022020	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT9	0x42022024	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT0	0x42022400	Secure Privilege Attribute

Protection Units registers

Register name	Address	Description
PPC0_PPC_S_P_ATT1	0x42022404	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT2	0x42022408	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT3	0x4202240C	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT4	0x42022410	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT5	0x42022414	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT6	0x42022418	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT7	0x4202241C	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT8	0x42022420	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT9	0x42022424	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT0	0x42024000	Non-secure Privilege Attribute
PPC0_PPC_NS_P_ATT1	0x42024004	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT2	0x42024008	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT3	0x4202400C	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT4	0x42024010	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT5	0x42024014	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT6	0x42024018	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT7	0x4202401C	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT8	0x42024020	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT9	0x42024024	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_R_ADDR0	0x42025000	Region Address

Protection Units registers

Register name	Address	Description
PPC0_PPC_R_ADDR1	0x42025004	Region Address
PPC0_PPC_R_ADDR2	0x42025008	Region Address
PPC0_PPC_R_ADDR3	0x4202500C	Region Address
PPC0_PPC_R_ADDR4	0x42025010	Region Address
PPC0_PPC_R_ADDR5	0x42025014	Region Address
PPC0_PPC_R_ADDR6	0x42025018	Region Address
PPC0_PPC_R_ADDR7	0x4202501C	Region Address
PPC0_PPC_R_ADDR8	0x42025020	Region Address
PPC0_PPC_R_ADDR9	0x42025024	Region Address
PPC0_PPC_R_ADDR10	0x42025028	Region Address
PPC0_PPC_R_ADDR11	0x4202502C	Region Address
PPC0_PPC_R_ADDR12	0x42025030	Region Address
PPC0_PPC_R_ADDR13	0x42025034	Region Address
PPC0_PPC_R_ADDR14	0x42025038	Region Address
PPC0_PPC_R_ADDR15	0x4202503C	Region Address
PPC0_PPC_R_ADDR16	0x42025040	Region Address
PPC0_PPC_R_ADDR17	0x42025044	Region Address
PPC0_PPC_R_ADDR18	0x42025048	Region Address
PPC0_PPC_R_ADDR19	0x4202504C	Region Address
PPC0_PPC_R_ADDR20	0x42025050	Region Address
PPC0_PPC_R_ADDR21	0x42025054	Region Address
PPC0_PPC_R_ADDR22	0x42025058	Region Address
PPC0_PPC_R_ADDR23	0x4202505C	Region Address
PPC0_PPC_R_ADDR24	0x42025060	Region Address
PPC0_PPC_R_ADDR25	0x42025064	Region Address
PPC0_PPC_R_ADDR26	0x42025068	Region Address
PPC0_PPC_R_ADDR27	0x4202506C	Region Address
PPC0_PPC_R_ADDR28	0x42025070	Region Address
PPC0_PPC_R_ADDR29	0x42025074	Region Address
PPC0_PPC_R_ADDR30	0x42025078	Region Address
PPC0_PPC_R_ADDR31	0x4202507C	Region Address
PPC0_PPC_R_ADDR32	0x42025080	Region Address
PPC0_PPC_R_ADDR33	0x42025084	Region Address
PPC0_PPC_R_ADDR34	0x42025088	Region Address
PPC0_PPC_R_ADDR35	0x4202508C	Region Address
PPC0_PPC_R_ADDR36	0x42025090	Region Address

Protection Units registers

Register name	Address	Description
PPC0_PPC_R_ADDR37	0x42025094	Region Address
PPC0_PPC_R_ADDR38	0x42025098	Region Address
PPC0_PPC_R_ADDR39	0x4202509C	Region Address
PPC0_PPC_R_ADDR40	0x420250A0	Region Address
PPC0_PPC_R_ADDR41	0x420250A4	Region Address
PPC0_PPC_R_ADDR42	0x420250A8	Region Address
PPC0_PPC_R_ADDR43	0x420250AC	Region Address
PPC0_PPC_R_ADDR44	0x420250B0	Region Address
PPC0_PPC_R_ADDR45	0x420250B4	Region Address
PPC0_PPC_R_ADDR46	0x420250B8	Region Address
PPC0_PPC_R_ADDR47	0x420250BC	Region Address
PPC0_PPC_R_ADDR48	0x420250C0	Region Address
PPC0_PPC_R_ADDR49	0x420250C4	Region Address
PPC0_PPC_R_ADDR50	0x420250C8	Region Address
PPC0_PPC_R_ADDR51	0x420250CC	Region Address
PPC0_PPC_R_ADDR52	0x420250D0	Region Address
PPC0_PPC_R_ADDR53	0x420250D4	Region Address
PPC0_PPC_R_ADDR54	0x420250D8	Region Address
PPC0_PPC_R_ADDR55	0x420250DC	Region Address
PPC0_PPC_R_ADDR56	0x420250E0	Region Address
PPC0_PPC_R_ADDR57	0x420250E4	Region Address
PPC0_PPC_R_ADDR58	0x420250E8	Region Address
PPC0_PPC_R_ADDR59	0x420250EC	Region Address
PPC0_PPC_R_ADDR60	0x420250F0	Region Address
PPC0_PPC_R_ADDR61	0x420250F4	Region Address
PPC0_PPC_R_ADDR62	0x420250F8	Region Address
PPC0_PPC_R_ADDR63	0x420250FC	Region Address
PPC0_PPC_R_ADDR64	0x42025100	Region Address
PPC0_PPC_R_ADDR65	0x42025104	Region Address
PPC0_PPC_R_ADDR66	0x42025108	Region Address
PPC0_PPC_R_ADDR67	0x4202510C	Region Address
PPC0_PPC_R_ADDR68	0x42025110	Region Address
PPC0_PPC_R_ADDR69	0x42025114	Region Address
PPC0_PPC_R_ADDR70	0x42025118	Region Address
PPC0_PPC_R_ADDR71	0x4202511C	Region Address
PPC0_PPC_R_ADDR72	0x42025120	Region Address

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Register name	Address	Description
PPC0_PPC_R_ADDR73	0x42025124	Region Address
PPC0_PPC_R_ADDR74	0x42025128	Region Address
PPC0_PPC_R_ADDR75	0x4202512C	Region Address
PPC0_PPC_R_ADDR76	0x42025130	Region Address
PPC0_PPC_R_ADDR77	0x42025134	Region Address
PPC0_PPC_R_ADDR78	0x42025138	Region Address
PPC0_PPC_R_ADDR79	0x4202513C	Region Address
PPC0_PPC_R_ADDR80	0x42025140	Region Address
PPC0_PPC_R_ADDR81	0x42025144	Region Address
PPC0_PPC_R_ADDR82	0x42025148	Region Address
PPC0_PPC_R_ADDR83	0x4202514C	Region Address
PPC0_PPC_R_ADDR84	0x42025150	Region Address
PPC0_PPC_R_ADDR85	0x42025154	Region Address
PPC0_PPC_R_ADDR86	0x42025158	Region Address
PPC0_PPC_R_ADDR87	0x4202515C	Region Address
PPC0_PPC_R_ADDR88	0x42025160	Region Address
PPC0_PPC_R_ADDR89	0x42025164	Region Address
PPC0_PPC_R_ADDR90	0x42025168	Region Address
PPC0_PPC_R_ADDR91	0x4202516C	Region Address
PPC0_PPC_R_ADDR92	0x42025170	Region Address
PPC0_PPC_R_ADDR93	0x42025174	Region Address
PPC0_PPC_R_ADDR94	0x42025178	Region Address
PPC0_PPC_R_ADDR95	0x4202517C	Region Address
PPC0_PPC_R_ADDR96	0x42025180	Region Address
PPC0_PPC_R_ADDR97	0x42025184	Region Address
PPC0_PPC_R_ADDR98	0x42025188	Region Address
PPC0_PPC_R_ADDR99	0x4202518C	Region Address
PPC0_PPC_R_ADDR100	0x42025190	Region Address
PPC0_PPC_R_ADDR101	0x42025194	Region Address
PPC0_PPC_R_ADDR102	0x42025198	Region Address
PPC0_PPC_R_ADDR103	0x4202519C	Region Address
PPC0_PPC_R_ADDR104	0x420251A0	Region Address
PPC0_PPC_R_ADDR105	0x420251A4	Region Address
PPC0_PPC_R_ADDR106	0x420251A8	Region Address
PPC0_PPC_R_ADDR107	0x420251AC	Region Address
PPC0_PPC_R_ADDR108	0x420251B0	Region Address

Protection Units registers

Register name	Address	Description
PPC0_PPC_R_ADDR109	0x420251B4	Region Address
PPC0_PPC_R_ADDR110	0x420251B8	Region Address
PPC0_PPC_R_ADDR111	0x420251BC	Region Address
PPC0_PPC_R_ADDR112	0x420251C0	Region Address
PPC0_PPC_R_ADDR113	0x420251C4	Region Address
PPC0_PPC_R_ADDR114	0x420251C8	Region Address
PPC0_PPC_R_ADDR115	0x420251CC	Region Address
PPC0_PPC_R_ADDR116	0x420251D0	Region Address
PPC0_PPC_R_ADDR117	0x420251D4	Region Address
PPC0_PPC_R_ADDR118	0x420251D8	Region Address
PPC0_PPC_R_ADDR119	0x420251DC	Region Address
PPC0_PPC_R_ADDR120	0x420251E0	Region Address
PPC0_PPC_R_ADDR121	0x420251E4	Region Address
PPC0_PPC_R_ADDR122	0x420251E8	Region Address
PPC0_PPC_R_ADDR123	0x420251EC	Region Address
PPC0_PPC_R_ADDR124	0x420251F0	Region Address
PPC0_PPC_R_ADDR125	0x420251F4	Region Address
PPC0_PPC_R_ADDR126	0x420251F8	Region Address
PPC0_PPC_R_ADDR127	0x420251FC	Region Address
PPC0_PPC_R_ADDR128	0x42025200	Region Address
PPC0_PPC_R_ADDR129	0x42025204	Region Address
PPC0_PPC_R_ADDR130	0x42025208	Region Address
PPC0_PPC_R_ADDR131	0x4202520C	Region Address
PPC0_PPC_R_ADDR132	0x42025210	Region Address
PPC0_PPC_R_ADDR133	0x42025214	Region Address
PPC0_PPC_R_ADDR134	0x42025218	Region Address
PPC0_PPC_R_ADDR135	0x4202521C	Region Address
PPC0_PPC_R_ADDR136	0x42025220	Region Address
PPC0_PPC_R_ADDR137	0x42025224	Region Address
PPC0_PPC_R_ADDR138	0x42025228	Region Address
PPC0_PPC_R_ADDR139	0x4202522C	Region Address
PPC0_PPC_R_ADDR140	0x42025230	Region Address
PPC0_PPC_R_ADDR141	0x42025234	Region Address
PPC0_PPC_R_ADDR142	0x42025238	Region Address
PPC0_PPC_R_ADDR143	0x4202523C	Region Address
PPC0_PPC_R_ADDR144	0x42025240	Region Address

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Register name	Address	Description
PPC0_PPC_R_ADDR145	0x42025244	Region Address
PPC0_PPC_R_ADDR146	0x42025248	Region Address
PPC0_PPC_R_ADDR147	0x4202524C	Region Address
PPC0_PPC_R_ADDR148	0x42025250	Region Address
PPC0_PPC_R_ADDR149	0x42025254	Region Address
PPC0_PPC_R_ADDR150	0x42025258	Region Address
PPC0_PPC_R_ADDR151	0x4202525C	Region Address
PPC0_PPC_R_ADDR152	0x42025260	Region Address
PPC0_PPC_R_ADDR153	0x42025264	Region Address
PPC0_PPC_R_ADDR154	0x42025268	Region Address
PPC0_PPC_R_ADDR155	0x4202526C	Region Address
PPC0_PPC_R_ADDR156	0x42025270	Region Address
PPC0_PPC_R_ADDR157	0x42025274	Region Address
PPC0_PPC_R_ADDR158	0x42025278	Region Address
PPC0_PPC_R_ADDR159	0x4202527C	Region Address
PPC0_PPC_R_ADDR160	0x42025280	Region Address
PPC0_PPC_R_ADDR161	0x42025284	Region Address
PPC0_PPC_R_ADDR162	0x42025288	Region Address
PPC0_PPC_R_ADDR163	0x4202528C	Region Address
PPC0_PPC_R_ADDR164	0x42025290	Region Address
PPC0_PPC_R_ADDR165	0x42025294	Region Address
PPC0_PPC_R_ADDR166	0x42025298	Region Address
PPC0_PPC_R_ADDR167	0x4202529C	Region Address
PPC0_PPC_R_ADDR168	0x420252A0	Region Address
PPC0_PPC_R_ADDR169	0x420252A4	Region Address
PPC0_PPC_R_ADDR170	0x420252A8	Region Address
PPC0_PPC_R_ADDR171	0x420252AC	Region Address
PPC0_PPC_R_ADDR172	0x420252B0	Region Address
PPC0_PPC_R_ADDR173	0x420252B4	Region Address
PPC0_PPC_R_ADDR174	0x420252B8	Region Address
PPC0_PPC_R_ADDR175	0x420252BC	Region Address
PPC0_PPC_R_ADDR176	0x420252C0	Region Address
PPC0_PPC_R_ADDR177	0x420252C4	Region Address
PPC0_PPC_R_ADDR178	0x420252C8	Region Address
PPC0_PPC_R_ADDR179	0x420252CC	Region Address
PPC0_PPC_R_ADDR180	0x420252D0	Region Address

Protection Units registers

Register name	Address	Description
PPC0_PPC_R_ADDR181	0x420252D4	Region Address
PPC0_PPC_R_ADDR182	0x420252D8	Region Address
PPC0_PPC_R_ADDR183	0x420252DC	Region Address
PPC0_PPC_R_ADDR184	0x420252E0	Region Address
PPC0_PPC_R_ADDR185	0x420252E4	Region Address
PPC0_PPC_R_ADDR186	0x420252E8	Region Address
PPC0_PPC_R_ADDR187	0x420252EC	Region Address
PPC0_PPC_R_ADDR188	0x420252F0	Region Address
PPC0_PPC_R_ADDR189	0x420252F4	Region Address
PPC0_PPC_R_ADDR190	0x420252F8	Region Address
PPC0_PPC_R_ADDR191	0x420252FC	Region Address
PPC0_PPC_R_ADDR192	0x42025300	Region Address
PPC0_PPC_R_ADDR193	0x42025304	Region Address
PPC0_PPC_R_ADDR194	0x42025308	Region Address
PPC0_PPC_R_ADDR195	0x4202530C	Region Address
PPC0_PPC_R_ADDR196	0x42025310	Region Address
PPC0_PPC_R_ADDR197	0x42025314	Region Address
PPC0_PPC_R_ADDR198	0x42025318	Region Address
PPC0_PPC_R_ADDR199	0x4202531C	Region Address
PPC0_PPC_R_ADDR200	0x42025320	Region Address
PPC0_PPC_R_ADDR201	0x42025324	Region Address
PPC0_PPC_R_ADDR202	0x42025328	Region Address
PPC0_PPC_R_ADDR203	0x4202532C	Region Address
PPC0_PPC_R_ADDR204	0x42025330	Region Address
PPC0_PPC_R_ADDR205	0x42025334	Region Address
PPC0_PPC_R_ADDR206	0x42025338	Region Address
PPC0_PPC_R_ADDR207	0x4202533C	Region Address
PPC0_PPC_R_ADDR208	0x42025340	Region Address
PPC0_PPC_R_ADDR209	0x42025344	Region Address
PPC0_PPC_R_ADDR210	0x42025348	Region Address
PPC0_PPC_R_ADDR211	0x4202534C	Region Address
PPC0_PPC_R_ADDR212	0x42025350	Region Address
PPC0_PPC_R_ADDR213	0x42025354	Region Address
PPC0_PPC_R_ADDR214	0x42025358	Region Address
PPC0_PPC_R_ADDR215	0x4202535C	Region Address
PPC0_PPC_R_ADDR216	0x42025360	Region Address

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Register name	Address	Description
PPC0_PPC_R_ADDR217	0x42025364	Region Address
PPC0_PPC_R_ADDR218	0x42025368	Region Address
PPC0_PPC_R_ADDR219	0x4202536C	Region Address
PPC0_PPC_R_ADDR220	0x42025370	Region Address
PPC0_PPC_R_ADDR221	0x42025374	Region Address
PPC0_PPC_R_ADDR222	0x42025378	Region Address
PPC0_PPC_R_ADDR223	0x4202537C	Region Address
PPC0_PPC_R_ADDR224	0x42025380	Region Address
PPC0_PPC_R_ADDR225	0x42025384	Region Address
PPC0_PPC_R_ADDR226	0x42025388	Region Address
PPC0_PPC_R_ADDR227	0x4202538C	Region Address
PPC0_PPC_R_ADDR228	0x42025390	Region Address
PPC0_PPC_R_ADDR229	0x42025394	Region Address
PPC0_PPC_R_ADDR230	0x42025398	Region Address
PPC0_PPC_R_ADDR231	0x4202539C	Region Address
PPC0_PPC_R_ADDR232	0x420253A0	Region Address
PPC0_PPC_R_ADDR233	0x420253A4	Region Address
PPC0_PPC_R_ADDR234	0x420253A8	Region Address
PPC0_PPC_R_ADDR235	0x420253AC	Region Address
PPC0_PPC_R_ADDR236	0x420253B0	Region Address
PPC0_PPC_R_ADDR237	0x420253B4	Region Address
PPC0_PPC_R_ADDR238	0x420253B8	Region Address
PPC0_PPC_R_ADDR239	0x420253BC	Region Address
PPC0_PPC_R_ADDR240	0x420253C0	Region Address
PPC0_PPC_R_ADDR241	0x420253C4	Region Address
PPC0_PPC_R_ADDR242	0x420253C8	Region Address
PPC0_PPC_R_ADDR243	0x420253CC	Region Address
PPC0_PPC_R_ADDR244	0x420253D0	Region Address
PPC0_PPC_R_ADDR245	0x420253D4	Region Address
PPC0_PPC_R_ADDR246	0x420253D8	Region Address
PPC0_PPC_R_ADDR247	0x420253DC	Region Address
PPC0_PPC_R_ADDR248	0x420253E0	Region Address
PPC0_PPC_R_ADDR249	0x420253E4	Region Address
PPC0_PPC_R_ADDR250	0x420253E8	Region Address
PPC0_PPC_R_ADDR251	0x420253EC	Region Address
PPC0_PPC_R_ADDR252	0x420253F0	Region Address

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Register name	Address	Description
PPC0_PPC_R_ADDR253	0x420253F4	Region Address
PPC0_PPC_R_ADDR254	0x420253F8	Region Address
PPC0_PPC_R_ADDR255	0x420253FC	Region Address
PPC0_PPC_R_ADDR256	0x42025400	Region Address
PPC0_PPC_R_ADDR257	0x42025404	Region Address
PPC0_PPC_R_ADDR258	0x42025408	Region Address
PPC0_PPC_R_ADDR259	0x4202540C	Region Address
PPC0_PPC_R_ADDR260	0x42025410	Region Address
PPC0_PPC_R_ADDR261	0x42025414	Region Address
PPC0_PPC_R_ADDR262	0x42025418	Region Address
PPC0_PPC_R_ADDR263	0x4202541C	Region Address
PPC0_PPC_R_ADDR264	0x42025420	Region Address
PPC0_PPC_R_ADDR265	0x42025424	Region Address
PPC0_PPC_R_ADDR266	0x42025428	Region Address
PPC0_PPC_R_ADDR267	0x4202542C	Region Address
PPC0_PPC_R_ADDR268	0x42025430	Region Address
PPC0_PPC_R_ADDR269	0x42025434	Region Address
PPC0_PPC_R_ADDR270	0x42025438	Region Address
PPC0_PPC_R_ADDR271	0x4202543C	Region Address
PPC0_PPC_R_ADDR272	0x42025440	Region Address
PPC0_PPC_R_ADDR273	0x42025444	Region Address
PPC0_PPC_R_ADDR274	0x42025448	Region Address
PPC0_PPC_R_ADDR275	0x4202544C	Region Address
PPC0_PPC_R_ADDR276	0x42025450	Region Address
PPC0_PPC_R_ADDR277	0x42025454	Region Address
PPC0_PPC_R_ADDR278	0x42025458	Region Address
PPC0_PPC_R_ADDR279	0x4202545C	Region Address
PPC0_PPC_R_ADDR280	0x42025460	Region Address
PPC0_PPC_R_ADDR281	0x42025464	Region Address
PPC0_PPC_R_ADDR282	0x42025468	Region Address
PPC0_PPC_R_ADDR283	0x4202546C	Region Address
PPC0_PPC_R_ADDR284	0x42025470	Region Address
PPC0_PPC_R_ADDR285	0x42025474	Region Address
PPC0_PPC_R_ADDR286	0x42025478	Region Address
PPC0_PPC_R_ADDR287	0x4202547C	Region Address
PPC0_PPC_R_ADDR288	0x42025480	Region Address

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Register name	Address	Description
PPC0_PPC_R_ADDR289	0x42025484	Region Address
PPC0_PPC_R_ADDR290	0x42025488	Region Address
PPC0_PPC_R_ADDR291	0x4202548C	Region Address
PPC0_PPC_R_ADDR292	0x42025490	Region Address
PPC0_PPC_R_ADDR293	0x42025494	Region Address
PPC0_PPC_R_ADDR294	0x42025498	Region Address
PPC0_PPC_R_ADDR295	0x4202549C	Region Address
PPC0_PPC_R_ADDR296	0x420254A0	Region Address
PPC0_PPC_R_ADDR297	0x420254A4	Region Address
PPC0_PPC_R_ADDR298	0x420254A8	Region Address
PPC0_PPC_R_ADDR299	0x420254AC	Region Address
PPC0_PPC_R_ADDR300	0x420254B0	Region Address
PPC0_PPC_R_ADDR301	0x420254B4	Region Address
PPC0_PPC_R_ADDR302	0x420254B8	Region Address
PPC0_PPC_R_ADDR303	0x420254BC	Region Address
PPC0_PPC_R_ADDR304	0x420254C0	Region Address
PPC0_PPC_R_ADDR305	0x420254C4	Region Address
PPC0_PPC_R_ADDR306	0x420254C8	Region Address
PPC0_PPC_R_ADDR307	0x420254CC	Region Address
PPC0_PPC_R_ADDR308	0x420254D0	Region Address
PPC0_PPC_R_ADDR309	0x420254D4	Region Address
PPC0_PPC_R_ADDR310	0x420254D8	Region Address
PPC0_PPC_R_ADDR311	0x420254DC	Region Address
PPC0_PPC_R_ADDR312	0x420254E0	Region Address
PPC0_PPC_R_ADDR313	0x420254E4	Region Address
PPC0_PPC_R_ADDR314	0x420254E8	Region Address
PPC0_PPC_R_ADDR315	0x420254EC	Region Address
PPC0_PPC_R_ADDR316	0x420254F0	Region Address
PPC0_PPC_R_ADDR317	0x420254F4	Region Address
PPC0_PPC_R_ADDR318	0x420254F8	Region Address
PPC0_PPC_R_ATT0	0x42026000	Region Attribute
PPC0_PPC_R_ATT1	0x42026004	Region Attribute
PPC0_PPC_R_ATT2	0x42026008	Region Attribute. This is the starting address of a register bank containing 33 registers (PPC0_PPC_R_ATT2 to PPC0_PPC_R_ATT215).

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Register name	Address	Description
PPC0_PPC_R_ATT5	0x42026014	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT7	0x4202601C	Region Attribute. This is the starting address of a register bank containing 71 registers (PPC0_PPC_R_ATT7 to PPC0_PPC_R_ATT261).
PPC0_PPC_R_ATT13	0x42026034	Region Attribute
PPC0_PPC_R_ATT14	0x42026038	Region Attribute. See PPC0_PPC_R_ATT0 for the details of bit fields.
PPC0_PPC_R_ATT15	0x4202603C	Region Attribute. See PPC0_PPC_R_ATT0 for the details of bit fields.
PPC0_PPC_R_ATT16	0x42026040	Region Attribute
PPC0_PPC_R_ATT17	0x42026044	Region Attribute
PPC0_PPC_R_ATT18	0x42026048	Region Attribute. See PPC0_PPC_R_ATT17 for the details of bit fields.
PPC0_PPC_R_ATT19	0x4202604C	Region Attribute
PPC0_PPC_R_ATT20	0x42026050	Region Attribute
PPC0_PPC_R_ATT30	0x42026078	Region Attribute. This is the starting address of a register bank containing 79 registers (PPC0_PPC_R_ATT30 to PPC0_PPC_R_ATT268).
PPC0_PPC_R_ATT31	0x4202607C	Region Attribute
PPC0_PPC_R_ATT32	0x42026080	Region Attribute
PPC0_PPC_R_ATT33	0x42026084	Region Attribute
PPC0_PPC_R_ATT34	0x42026088	Region Attribute
PPC0_PPC_R_ATT35	0x4202608C	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT36	0x42026090	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT39	0x4202609C	Region Attribute
PPC0_PPC_R_ATT40	0x420260A0	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC0_PPC_R_ATT47	0x420260BC	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC0_PPC_R_ATT50	0x420260C8	Region Attribute. This is the starting address of a register bank containing 41 registers (PPC0_PPC_R_ATT50 to PPC0_PPC_R_ATT301).
PPC0_PPC_R_ATT55	0x420260DC	Region Attribute
PPC0_PPC_R_ATT96	0x42026180	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.

Protection Units registers

Register name	Address	Description
PPC0_PPC_R_ATT98	0x42026188	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT121	0x420261E4	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT138	0x42026228	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT139	0x4202622C	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT140	0x42026230	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT141	0x42026234	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT142	0x42026238	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT143	0x4202623C	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT144	0x42026240	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT145	0x42026244	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT146	0x42026248	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC0_PPC_R_ATT147	0x4202624C	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC0_PPC_R_ATT148	0x42026250	Region Attribute. See PPC0_PPC_R_ATT55 for the details of bit fields.
PPC0_PPC_R_ATT150	0x42026258	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT152	0x42026260	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC0_PPC_R_ATT153	0x42026264	Region Attribute. See PPC0_PPC_R_ATT17 for the details of bit fields.
PPC0_PPC_R_ATT155	0x4202626C	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT157	0x42026274	Region Attribute. See PPC0_PPC_R_ATT13 for the details of bit fields.
PPC0_PPC_R_ATT159	0x4202627C	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.

Protection Units registers

Register name	Address	Description
PPC0_PPC_R_ATT160	0x42026280	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT164	0x42026290	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT165	0x42026294	Region Attribute. See PPC0_PPC_R_ATT55 for the details of bit fields.
PPC0_PPC_R_ATT166	0x42026298	Region Attribute. See PPC0_PPC_R_ATT32 for the details of bit fields.
PPC0_PPC_R_ATT167	0x4202629C	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC0_PPC_R_ATT170	0x420262A8	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC0_PPC_R_ATT171	0x420262AC	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT172	0x420262B0	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT173	0x420262B4	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT174	0x420262B8	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT175	0x420262BC	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT176	0x420262C0	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT177	0x420262C4	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT178	0x420262C8	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT179	0x420262CC	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT180	0x420262D0	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT181	0x420262D4	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT182	0x420262D8	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT183	0x420262DC	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.

Protection Units registers

Register name	Address	Description
PPC0_PPC_R_ATT184	0x420262E0	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT185	0x420262E4	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT186	0x420262E8	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT187	0x420262EC	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT188	0x420262F0	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT189	0x420262F4	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT190	0x420262F8	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT191	0x420262FC	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT192	0x42026300	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT216	0x42026360	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT240	0x420263C0	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT243	0x420263CC	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT263	0x4202641C	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT264	0x42026420	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC0_PPC_R_ATT265	0x42026424	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC0_PPC_R_ATT266	0x42026428	Region Attribute. See PPC0_PPC_R_ATT19 for the details of bit fields.
PPC0_PPC_R_ATT267	0x4202642C	Region Attribute. See PPC0_PPC_R_ATT19 for the details of bit fields.
PPC0_PPC_R_ATT269	0x42026434	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT302	0x420264B8	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.

Protection Units registers

Register name	Address	Description
PPC0_PPC_R_ATT303	0x420264BC	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT304	0x420264C0	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT305	0x420264C4	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT306	0x420264C8	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT307	0x420264CC	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT308	0x420264D0	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT309	0x420264D4	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT310	0x420264D8	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT311	0x420264DC	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT312	0x420264E0	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT313	0x420264E4	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT314	0x420264E8	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT315	0x420264EC	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT316	0x420264F0	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC0_PPC_R_ATT317	0x420264F4	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC0_PPC_R_ATT318	0x420264F8	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC1_PPC_CTL	0x44020000	PPC Control Registers. See PPC0_PPC_CTL for the details of bit fields.
PPC1_PPC_LOCK_MASK	0x4402000C	Locked Mask. See PPC0_PPC_LOCK_MASK for the details of bit fields.

Protection Units registers

Register name	Address	Description
PPC1_PPC_PC_MASK0	0x44021000	Protection Context Mask. This is the starting address of a register bank containing 164 registers (PPC1_PPC_PC_MASK0 to PPC1_PPC_PC_MASK163).
PPC1_PPC_NS_ATT0	0x44022000	Non-secure attribute
PPC1_PPC_NS_ATT1	0x44022004	Non-secure attribute. See PPC1_PPC_NS_ATT0 for the details of bit fields.
PPC1_PPC_NS_ATT2	0x44022008	Non-secure attribute. See PPC1_PPC_NS_ATT0 for the details of bit fields.
PPC1_PPC_NS_ATT3	0x4402200C	Non-secure attribute. See PPC1_PPC_NS_ATT0 for the details of bit fields.
PPC1_PPC_NS_ATT4	0x44022010	Non-secure attribute. See PPC1_PPC_NS_ATT0 for the details of bit fields.
PPC1_PPC_NS_ATT5	0x44022014	Non-secure attribute. See PPC1_PPC_NS_ATT0 for the details of bit fields.
PPC1_PPC_S_P_ATT0	0x44022400	Secure Privilege Attribute
PPC1_PPC_S_P_ATT1	0x44022404	Secure Privilege Attribute. See PPC1_PPC_S_P_ATT0 for the details of bit fields.
PPC1_PPC_S_P_ATT2	0x44022408	Secure Privilege Attribute. See PPC1_PPC_S_P_ATT0 for the details of bit fields.
PPC1_PPC_S_P_ATT3	0x4402240C	Secure Privilege Attribute. See PPC1_PPC_S_P_ATT0 for the details of bit fields.
PPC1_PPC_S_P_ATT4	0x44022410	Secure Privilege Attribute. See PPC1_PPC_S_P_ATT0 for the details of bit fields.
PPC1_PPC_S_P_ATT5	0x44022414	Secure Privilege Attribute. See PPC1_PPC_S_P_ATT0 for the details of bit fields.
PPC1_PPC_NS_P_ATT0	0x44024000	Non-secure Privilege Attribute
PPC1_PPC_NS_P_ATT1	0x44024004	Non-secure Privilege Attribute. See PPC1_PPC_NS_P_ATT0 for the details of bit fields.
PPC1_PPC_NS_P_ATT2	0x44024008	Non-secure Privilege Attribute. See PPC1_PPC_NS_P_ATT0 for the details of bit fields.
PPC1_PPC_NS_P_ATT3	0x4402400C	Non-secure Privilege Attribute. See PPC1_PPC_NS_P_ATT0 for the details of bit fields.
PPC1_PPC_NS_P_ATT4	0x44024010	Non-secure Privilege Attribute. See PPC1_PPC_NS_P_ATT0 for the details of bit fields.
PPC1_PPC_NS_P_ATT5	0x44024014	Non-secure Privilege Attribute. See PPC1_PPC_NS_P_ATT0 for the details of bit fields.
PPC1_PPC_R_ADDR0	0x44025000	Region Address
PPC1_PPC_R_ADDR1	0x44025004	Region Address

Protection Units registers

Register name	Address	Description
PPC1_PPC_R_ADDR2	0x44025008	Region Address
PPC1_PPC_R_ADDR3	0x4402500C	Region Address
PPC1_PPC_R_ADDR4	0x44025010	Region Address
PPC1_PPC_R_ADDR5	0x44025014	Region Address
PPC1_PPC_R_ADDR6	0x44025018	Region Address
PPC1_PPC_R_ADDR7	0x4402501C	Region Address
PPC1_PPC_R_ADDR8	0x44025020	Region Address
PPC1_PPC_R_ADDR9	0x44025024	Region Address
PPC1_PPC_R_ADDR10	0x44025028	Region Address
PPC1_PPC_R_ADDR11	0x4402502C	Region Address
PPC1_PPC_R_ADDR12	0x44025030	Region Address
PPC1_PPC_R_ADDR13	0x44025034	Region Address
PPC1_PPC_R_ADDR14	0x44025038	Region Address
PPC1_PPC_R_ADDR15	0x4402503C	Region Address
PPC1_PPC_R_ADDR16	0x44025040	Region Address
PPC1_PPC_R_ADDR17	0x44025044	Region Address
PPC1_PPC_R_ADDR18	0x44025048	Region Address
PPC1_PPC_R_ADDR19	0x4402504C	Region Address
PPC1_PPC_R_ADDR20	0x44025050	Region Address
PPC1_PPC_R_ADDR21	0x44025054	Region Address
PPC1_PPC_R_ADDR22	0x44025058	Region Address
PPC1_PPC_R_ADDR23	0x4402505C	Region Address
PPC1_PPC_R_ADDR24	0x44025060	Region Address
PPC1_PPC_R_ADDR25	0x44025064	Region Address
PPC1_PPC_R_ADDR26	0x44025068	Region Address
PPC1_PPC_R_ADDR27	0x4402506C	Region Address
PPC1_PPC_R_ADDR28	0x44025070	Region Address
PPC1_PPC_R_ADDR29	0x44025074	Region Address
PPC1_PPC_R_ADDR30	0x44025078	Region Address
PPC1_PPC_R_ADDR31	0x4402507C	Region Address
PPC1_PPC_R_ADDR32	0x44025080	Region Address
PPC1_PPC_R_ADDR33	0x44025084	Region Address
PPC1_PPC_R_ADDR34	0x44025088	Region Address
PPC1_PPC_R_ADDR35	0x4402508C	Region Address
PPC1_PPC_R_ADDR36	0x44025090	Region Address
PPC1_PPC_R_ADDR37	0x44025094	Region Address

Protection Units registers

Register name	Address	Description
PPC1_PPC_R_ADDR38	0x44025098	Region Address
PPC1_PPC_R_ADDR39	0x4402509C	Region Address
PPC1_PPC_R_ADDR40	0x440250A0	Region Address
PPC1_PPC_R_ADDR41	0x440250A4	Region Address
PPC1_PPC_R_ADDR42	0x440250A8	Region Address
PPC1_PPC_R_ADDR43	0x440250AC	Region Address
PPC1_PPC_R_ADDR44	0x440250B0	Region Address
PPC1_PPC_R_ADDR45	0x440250B4	Region Address
PPC1_PPC_R_ADDR46	0x440250B8	Region Address
PPC1_PPC_R_ADDR47	0x440250BC	Region Address
PPC1_PPC_R_ADDR48	0x440250C0	Region Address
PPC1_PPC_R_ADDR49	0x440250C4	Region Address
PPC1_PPC_R_ADDR50	0x440250C8	Region Address
PPC1_PPC_R_ADDR51	0x440250CC	Region Address
PPC1_PPC_R_ADDR52	0x440250D0	Region Address
PPC1_PPC_R_ADDR53	0x440250D4	Region Address
PPC1_PPC_R_ADDR54	0x440250D8	Region Address
PPC1_PPC_R_ADDR55	0x440250DC	Region Address
PPC1_PPC_R_ADDR56	0x440250E0	Region Address
PPC1_PPC_R_ADDR57	0x440250E4	Region Address
PPC1_PPC_R_ADDR58	0x440250E8	Region Address
PPC1_PPC_R_ADDR59	0x440250EC	Region Address
PPC1_PPC_R_ADDR60	0x440250F0	Region Address
PPC1_PPC_R_ADDR61	0x440250F4	Region Address
PPC1_PPC_R_ADDR62	0x440250F8	Region Address
PPC1_PPC_R_ADDR63	0x440250FC	Region Address
PPC1_PPC_R_ADDR64	0x44025100	Region Address
PPC1_PPC_R_ADDR65	0x44025104	Region Address
PPC1_PPC_R_ADDR66	0x44025108	Region Address
PPC1_PPC_R_ADDR67	0x4402510C	Region Address
PPC1_PPC_R_ADDR68	0x44025110	Region Address
PPC1_PPC_R_ADDR69	0x44025114	Region Address
PPC1_PPC_R_ADDR70	0x44025118	Region Address
PPC1_PPC_R_ADDR71	0x4402511C	Region Address
PPC1_PPC_R_ADDR72	0x44025120	Region Address
PPC1_PPC_R_ADDR73	0x44025124	Region Address

Protection Units registers

Register name	Address	Description
PPC1_PPC_R_ADDR74	0x44025128	Region Address
PPC1_PPC_R_ADDR75	0x4402512C	Region Address
PPC1_PPC_R_ADDR76	0x44025130	Region Address
PPC1_PPC_R_ADDR77	0x44025134	Region Address
PPC1_PPC_R_ADDR78	0x44025138	Region Address
PPC1_PPC_R_ADDR79	0x4402513C	Region Address
PPC1_PPC_R_ADDR80	0x44025140	Region Address
PPC1_PPC_R_ADDR81	0x44025144	Region Address
PPC1_PPC_R_ADDR82	0x44025148	Region Address
PPC1_PPC_R_ADDR83	0x4402514C	Region Address
PPC1_PPC_R_ADDR84	0x44025150	Region Address
PPC1_PPC_R_ADDR85	0x44025154	Region Address
PPC1_PPC_R_ADDR86	0x44025158	Region Address
PPC1_PPC_R_ADDR87	0x4402515C	Region Address
PPC1_PPC_R_ADDR88	0x44025160	Region Address
PPC1_PPC_R_ADDR89	0x44025164	Region Address
PPC1_PPC_R_ADDR90	0x44025168	Region Address
PPC1_PPC_R_ADDR91	0x4402516C	Region Address
PPC1_PPC_R_ADDR92	0x44025170	Region Address
PPC1_PPC_R_ADDR93	0x44025174	Region Address
PPC1_PPC_R_ADDR94	0x44025178	Region Address
PPC1_PPC_R_ADDR95	0x4402517C	Region Address
PPC1_PPC_R_ADDR96	0x44025180	Region Address
PPC1_PPC_R_ADDR97	0x44025184	Region Address
PPC1_PPC_R_ADDR98	0x44025188	Region Address
PPC1_PPC_R_ADDR99	0x4402518C	Region Address
PPC1_PPC_R_ADDR100	0x44025190	Region Address
PPC1_PPC_R_ADDR101	0x44025194	Region Address
PPC1_PPC_R_ADDR102	0x44025198	Region Address
PPC1_PPC_R_ADDR103	0x4402519C	Region Address
PPC1_PPC_R_ADDR104	0x440251A0	Region Address
PPC1_PPC_R_ADDR105	0x440251A4	Region Address
PPC1_PPC_R_ADDR106	0x440251A8	Region Address
PPC1_PPC_R_ADDR107	0x440251AC	Region Address
PPC1_PPC_R_ADDR108	0x440251B0	Region Address
PPC1_PPC_R_ADDR109	0x440251B4	Region Address

Protection Units registers

Register name	Address	Description
PPC1_PPC_R_ADDR110	0x440251B8	Region Address
PPC1_PPC_R_ADDR111	0x440251BC	Region Address
PPC1_PPC_R_ADDR112	0x440251C0	Region Address
PPC1_PPC_R_ADDR113	0x440251C4	Region Address
PPC1_PPC_R_ADDR114	0x440251C8	Region Address
PPC1_PPC_R_ADDR115	0x440251CC	Region Address
PPC1_PPC_R_ADDR116	0x440251D0	Region Address
PPC1_PPC_R_ADDR117	0x440251D4	Region Address
PPC1_PPC_R_ADDR118	0x440251D8	Region Address
PPC1_PPC_R_ADDR119	0x440251DC	Region Address
PPC1_PPC_R_ADDR120	0x440251E0	Region Address
PPC1_PPC_R_ADDR121	0x440251E4	Region Address
PPC1_PPC_R_ADDR122	0x440251E8	Region Address
PPC1_PPC_R_ADDR123	0x440251EC	Region Address
PPC1_PPC_R_ADDR124	0x440251F0	Region Address
PPC1_PPC_R_ADDR125	0x440251F4	Region Address
PPC1_PPC_R_ADDR126	0x440251F8	Region Address
PPC1_PPC_R_ADDR127	0x440251FC	Region Address
PPC1_PPC_R_ADDR128	0x44025200	Region Address
PPC1_PPC_R_ADDR129	0x44025204	Region Address
PPC1_PPC_R_ADDR130	0x44025208	Region Address
PPC1_PPC_R_ADDR131	0x4402520C	Region Address
PPC1_PPC_R_ADDR132	0x44025210	Region Address
PPC1_PPC_R_ADDR133	0x44025214	Region Address
PPC1_PPC_R_ADDR134	0x44025218	Region Address
PPC1_PPC_R_ADDR135	0x4402521C	Region Address
PPC1_PPC_R_ADDR136	0x44025220	Region Address
PPC1_PPC_R_ADDR137	0x44025224	Region Address
PPC1_PPC_R_ADDR138	0x44025228	Region Address
PPC1_PPC_R_ADDR139	0x4402522C	Region Address
PPC1_PPC_R_ADDR140	0x44025230	Region Address
PPC1_PPC_R_ADDR141	0x44025234	Region Address
PPC1_PPC_R_ADDR142	0x44025238	Region Address
PPC1_PPC_R_ADDR143	0x4402523C	Region Address
PPC1_PPC_R_ADDR144	0x44025240	Region Address
PPC1_PPC_R_ADDR145	0x44025244	Region Address

Protection Units registers

Register name	Address	Description
PPC1_PPC_R_ADDR146	0x44025248	Region Address
PPC1_PPC_R_ADDR147	0x4402524C	Region Address
PPC1_PPC_R_ADDR148	0x44025250	Region Address
PPC1_PPC_R_ADDR149	0x44025254	Region Address
PPC1_PPC_R_ADDR150	0x44025258	Region Address
PPC1_PPC_R_ADDR151	0x4402525C	Region Address
PPC1_PPC_R_ADDR152	0x44025260	Region Address
PPC1_PPC_R_ADDR153	0x44025264	Region Address
PPC1_PPC_R_ADDR154	0x44025268	Region Address
PPC1_PPC_R_ADDR155	0x4402526C	Region Address
PPC1_PPC_R_ADDR156	0x44025270	Region Address
PPC1_PPC_R_ADDR157	0x44025274	Region Address
PPC1_PPC_R_ADDR158	0x44025278	Region Address
PPC1_PPC_R_ADDR159	0x4402527C	Region Address
PPC1_PPC_R_ADDR160	0x44025280	Region Address
PPC1_PPC_R_ADDR161	0x44025284	Region Address
PPC1_PPC_R_ADDR162	0x44025288	Region Address
PPC1_PPC_R_ADDR163	0x4402528C	Region Address
PPC1_PPC_R_ATT0	0x44026000	Region Attribute. See PPC0_PPC_R_ATT0 for the details of bit fields.
PPC1_PPC_R_ATT1	0x44026004	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT2	0x44026008	Region Attribute. This is the starting address of a register bank containing 30 registers (PPC1_PPC_R_ATT2 to PPC1_PPC_R_ATT154). See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC1_PPC_R_ATT3	0x4402600C	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT5	0x44026014	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT6	0x44026018	Region Attribute. This is the starting address of a register bank containing 43 registers (PPC1_PPC_R_ATT6 to PPC1_PPC_R_ATT149). See PPC0_PPC_R_ATT7 for the details of bit fields.
PPC1_PPC_R_ATT11	0x4402602C	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.

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Register name	Address	Description
PPC1_PPC_R_ATT12	0x44026030	Region Attribute. See PPC0_PPC_R_ATT0 for the details of bit fields.
PPC1_PPC_R_ATT13	0x44026034	Region Attribute. See PPC0_PPC_R_ATT0 for the details of bit fields.
PPC1_PPC_R_ATT14	0x44026038	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.
PPC1_PPC_R_ATT15	0x4402603C	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC1_PPC_R_ATT16	0x44026040	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT20	0x44026050	Region Attribute. See PPC0_PPC_R_ATT55 for the details of bit fields.
PPC1_PPC_R_ATT21	0x44026054	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT22	0x44026058	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT23	0x4402605C	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT24	0x44026060	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT25	0x44026064	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT26	0x44026068	Region Attribute. This is the starting address of a register bank containing 5 registers (PPC1_PPC_R_ATT26 to PPC1_PPC_R_ATT146). See PPC0_PPC_R_ATT50 for the details of bit fields.
PPC1_PPC_R_ATT28	0x44026070	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT29	0x44026074	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT57	0x440260E4	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT74	0x44026128	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT75	0x4402612C	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT76	0x44026130	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.

Protection Units registers

Register name	Address	Description
PPC1_PPC_R_ATT77	0x44026134	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT78	0x44026138	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT79	0x4402613C	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT80	0x44026140	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT81	0x44026144	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT82	0x44026148	Region Attribute. See PPC0_PPC_R_ATT19 for the details of bit fields.
PPC1_PPC_R_ATT83	0x4402614C	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT84	0x44026150	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT85	0x44026154	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT86	0x44026158	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT87	0x4402615C	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT88	0x44026160	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT89	0x44026164	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT90	0x44026168	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT91	0x4402616C	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT92	0x44026170	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT93	0x44026174	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC1_PPC_R_ATT94	0x44026178	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC1_PPC_R_ATT103	0x4402619C	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.

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Register name	Address	Description
PPC1_PPC_R_ATT104	0x440261A0	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT105	0x440261A4	Region Attribute. See PPC0_PPC_R_ATT19 for the details of bit fields.
PPC1_PPC_R_ATT106	0x440261A8	Region Attribute. See PPC0_PPC_R_ATT19 for the details of bit fields.
PPC1_PPC_R_ATT107	0x440261AC	Region Attribute. This is the starting address of a register bank containing 17 registers (PPC1_PPC_R_ATT107 to PPC1_PPC_R_ATT161). See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC1_PPC_R_ATT109	0x440261B4	Region Attribute. See PPC0_PPC_R_ATT19 for the details of bit fields.
PPC1_PPC_R_ATT110	0x440261B8	Region Attribute. See PPC0_PPC_R_ATT19 for the details of bit fields.
PPC1_PPC_R_ATT117	0x440261D4	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT118	0x440261D8	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT119	0x440261DC	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT120	0x440261E0	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT121	0x440261E4	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT122	0x440261E8	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT123	0x440261EC	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT124	0x440261F0	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC1_PPC_R_ATT139	0x4402622C	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT140	0x44026230	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC1_PPC_R_ATT141	0x44026234	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC1_PPC_R_ATT144	0x44026240	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.

Protection Units registers

Register name	Address	Description
PPC1_PPC_R_ATT148	0x44026250	Region Attribute. See PPC0_PPC_R_ATT39 for the details of bit fields.
PPC1_PPC_R_ATT152	0x44026260	Region Attribute. See PPC0_PPC_R_ATT13 for the details of bit fields.
PPC1_PPC_R_ATT153	0x44026264	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC1_PPC_R_ATT155	0x4402626C	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC1_PPC_R_ATT156	0x44026270	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC1_PPC_R_ATT157	0x44026274	Region Attribute. See PPC0_PPC_R_ATT17 for the details of bit fields.
PPC1_PPC_R_ATT158	0x44026278	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC1_PPC_R_ATT159	0x4402627C	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC1_PPC_R_ATT160	0x44026280	Region Attribute. See PPC0_PPC_R_ATT20 for the details of bit fields.
PPC1_PPC_R_ATT162	0x44026288	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.
PPC1_PPC_R_ATT163	0x4402628C	Region Attribute. See PPC0_PPC_R_ATT33 for the details of bit fields.

11.2 Registers default values

The table lists the address order of the default values of PPC0_PPC_R_ADDRx and PPC1_PPC_R_ADDRx register corresponding to the various PPC instances in the MCU.

Register Name	Address of the register	Default value of register
PPC0_PPC_R_ADDR0	0x42025000	0x10800000
PPC0_PPC_R_ADDR1	0x42025004	0x10801004
PPC0_PPC_R_ADDR2	0x42025008	0x10801010
PPC0_PPC_R_ADDR3	0x4202500C	0x10801020
PPC0_PPC_R_ADDR4	0x42025010	0x10801030
PPC0_PPC_R_ADDR5	0x42025014	0x10801044
PPC0_PPC_R_ADDR6	0x42025018	0x10801050
PPC0_PPC_R_ADDR7	0x4202501C	0x10801008
PPC0_PPC_R_ADDR8	0x42025020	0x10801018
PPC0_PPC_R_ADDR9	0x42025024	0x10801028
PPC0_PPC_R_ADDR10	0x42025028	0x10801038
PPC0_PPC_R_ADDR11	0x4202502C	0x10801048
PPC0_PPC_R_ADDR12	0x42025030	0x10801058
PPC0_PPC_R_ADDR13	0x42025034	0x10802000
PPC0_PPC_R_ADDR14	0x42025038	0x10808000
PPC0_PPC_R_ADDR15	0x4202503C	0x10809000
PPC0_PPC_R_ADDR16	0x42025040	0x10810000
PPC0_PPC_R_ADDR17	0x42025044	0x10880000
PPC0_PPC_R_ADDR18	0x42025048	0x10881000
PPC0_PPC_R_ADDR19	0x4202504C	0x10882000
PPC0_PPC_R_ADDR20	0x42025050	0x10882400
PPC0_PPC_R_ADDR21	0x42025054	0x10884000
PPC0_PPC_R_ADDR22	0x42025058	0x10884008
PPC0_PPC_R_ADDR23	0x4202505C	0x10884040
PPC0_PPC_R_ADDR24	0x42025060	0x10884400
PPC0_PPC_R_ADDR25	0x42025064	0x10884800
PPC0_PPC_R_ADDR26	0x42025068	0x10884440
PPC0_PPC_R_ADDR27	0x4202506C	0x10884840
PPC0_PPC_R_ADDR28	0x42025070	0x10884480
PPC0_PPC_R_ADDR29	0x42025074	0x10884880
PPC0_PPC_R_ADDR30	0x42025078	0x10884C00
PPC0_PPC_R_ADDR31	0x4202507C	0x10884C10
PPC0_PPC_R_ADDR32	0x42025080	0x10884E00
PPC0_PPC_R_ADDR33	0x42025084	0x10888000

Register Name	Address of the register	Default value of register
PPC0_PPC_R_ADDR34	0x42025088	0x10B80000
PPC0_PPC_R_ADDR35	0x4202508C	0x1088C000
PPC0_PPC_R_ADDR36	0x42025090	0x10890000
PPC0_PPC_R_ADDR37	0x42025094	0x1088C040
PPC0_PPC_R_ADDR38	0x42025098	0x10890040
PPC0_PPC_R_ADDR39	0x4202509C	0x1088C080
PPC0_PPC_R_ADDR40	0x420250A0	0x10890080
PPC0_PPC_R_ADDR41	0x420250A4	0x1088D000
PPC0_PPC_R_ADDR42	0x420250A8	0x10891000
PPC0_PPC_R_ADDR43	0x420250AC	0x1088D040
PPC0_PPC_R_ADDR44	0x420250B0	0x10891040
PPC0_PPC_R_ADDR45	0x420250B4	0x1088D080
PPC0_PPC_R_ADDR46	0x420250B8	0x10891080
PPC0_PPC_R_ADDR47	0x420250BC	0x10898000
PPC0_PPC_R_ADDR48	0x420250C0	0x10898400
PPC0_PPC_R_ADDR49	0x420250C4	0x10898401
PPC0_PPC_R_ADDR50	0x420250C8	0x10898800
PPC0_PPC_R_ADDR51	0x420250CC	0x10898840
PPC0_PPC_R_ADDR52	0x420250D0	0x10898850
PPC0_PPC_R_ADDR53	0x420250D4	0x10898860
PPC0_PPC_R_ADDR54	0x420250D8	0x10898870
PPC0_PPC_R_ADDR55	0x420250DC	0x1089A000
PPC0_PPC_R_ADDR56	0x420250E0	0x1089C000
PPC0_PPC_R_ADDR57	0x420250E4	0x108A0000
PPC0_PPC_R_ADDR58	0x420250E8	0x1089C040
PPC0_PPC_R_ADDR59	0x420250EC	0x108A0040
PPC0_PPC_R_ADDR60	0x420250F0	0x1089E000
PPC0_PPC_R_ADDR61	0x420250F4	0x1089E010
PPC0_PPC_R_ADDR62	0x420250F8	0x1089E020
PPC0_PPC_R_ADDR63	0x420250FC	0x1089E030
PPC0_PPC_R_ADDR64	0x42025100	0x1089E040
PPC0_PPC_R_ADDR65	0x42025104	0x1089E050
PPC0_PPC_R_ADDR66	0x42025108	0x1089E060
PPC0_PPC_R_ADDR67	0x4202510C	0x1089E070
PPC0_PPC_R_ADDR68	0x42025110	0x1089E080
PPC0_PPC_R_ADDR69	0x42025114	0x1089E090
PPC0_PPC_R_ADDR70	0x42025118	0x1089E0A0
PPC0_PPC_R_ADDR71	0x4202511C	0x1089E0B0
PPC0_PPC_R_ADDR72	0x42025120	0x1089E0C0

Register Name	Address of the register	Default value of register
PPC0_PPC_R_ADDR73	0x42025124	0x1089E0D0
PPC0_PPC_R_ADDR74	0x42025128	0x1089E0E0
PPC0_PPC_R_ADDR75	0x4202512C	0x1089E0F0
PPC0_PPC_R_ADDR76	0x42025130	0x108A2000
PPC0_PPC_R_ADDR77	0x42025134	0x108A2010
PPC0_PPC_R_ADDR78	0x42025138	0x108A2020
PPC0_PPC_R_ADDR79	0x4202513C	0x108A2030
PPC0_PPC_R_ADDR80	0x42025140	0x108A2040
PPC0_PPC_R_ADDR81	0x42025144	0x108A2050
PPC0_PPC_R_ADDR82	0x42025148	0x108A2060
PPC0_PPC_R_ADDR83	0x4202514C	0x108A2070
PPC0_PPC_R_ADDR84	0x42025150	0x108A2080
PPC0_PPC_R_ADDR85	0x42025154	0x108A2090
PPC0_PPC_R_ADDR86	0x42025158	0x108A20A0
PPC0_PPC_R_ADDR87	0x4202515C	0x108A20B0
PPC0_PPC_R_ADDR88	0x42025160	0x108A20C0
PPC0_PPC_R_ADDR89	0x42025164	0x108A20D0
PPC0_PPC_R_ADDR90	0x42025168	0x108A20E0
PPC0_PPC_R_ADDR91	0x4202516C	0x108A20F0
PPC0_PPC_R_ADDR92	0x42025170	0x108A4000
PPC0_PPC_R_ADDR93	0x42025174	0x108A4020
PPC0_PPC_R_ADDR94	0x42025178	0x108A4040
PPC0_PPC_R_ADDR95	0x4202517C	0x108A4048
PPC0_PPC_R_ADDR96	0x42025180	0x108A4080
PPC0_PPC_R_ADDR97	0x42025184	0x108A4400
PPC0_PPC_R_ADDR98	0x42025188	0x108A4800
PPC0_PPC_R_ADDR99	0x4202518C	0x108A5000
PPC0_PPC_R_ADDR100	0x42025190	0x108A5010
PPC0_PPC_R_ADDR101	0x42025194	0x108A5014
PPC0_PPC_R_ADDR102	0x42025198	0x108A5018
PPC0_PPC_R_ADDR103	0x4202519C	0x108A501C
PPC0_PPC_R_ADDR104	0x420251A0	0x108A5020
PPC0_PPC_R_ADDR105	0x420251A4	0x108A5024
PPC0_PPC_R_ADDR106	0x420251A8	0x108A5028
PPC0_PPC_R_ADDR107	0x420251AC	0x108A502C
PPC0_PPC_R_ADDR108	0x420251B0	0x108A5074
PPC0_PPC_R_ADDR109	0x420251B4	0x108A507C
PPC0_PPC_R_ADDR110	0x420251B8	0x108A5400
PPC0_PPC_R_ADDR111	0x420251BC	0x108A5418

Register Name	Address of the register	Default value of register
PPC0_PPC_R_ADDR112	0x420251C0	0x108A5424
PPC0_PPC_R_ADDR113	0x420251C4	0x108A542C
PPC0_PPC_R_ADDR114	0x420251C8	0x108A547C
PPC0_PPC_R_ADDR115	0x420251CC	0x108A5401
PPC0_PPC_R_ADDR116	0x420251D0	0x108A5419
PPC0_PPC_R_ADDR117	0x420251D4	0x108A5425
PPC0_PPC_R_ADDR118	0x420251D8	0x108A542D
PPC0_PPC_R_ADDR119	0x420251DC	0x108A547D
PPC0_PPC_R_ADDR120	0x420251E0	0x108A5800
PPC0_PPC_R_ADDR121	0x420251E4	0x108A6000
PPC0_PPC_R_ADDR122	0x420251E8	0x108A8000
PPC0_PPC_R_ADDR123	0x420251EC	0x108A8008
PPC0_PPC_R_ADDR124	0x420251F0	0x108A8010
PPC0_PPC_R_ADDR125	0x420251F4	0x108A8018
PPC0_PPC_R_ADDR126	0x420251F8	0x108A8020
PPC0_PPC_R_ADDR127	0x420251FC	0x108A8028
PPC0_PPC_R_ADDR128	0x42025200	0x108A8030
PPC0_PPC_R_ADDR129	0x42025204	0x108A8038
PPC0_PPC_R_ADDR130	0x42025208	0x108A8040
PPC0_PPC_R_ADDR131	0x4202520C	0x108A8048
PPC0_PPC_R_ADDR132	0x42025210	0x108A8050
PPC0_PPC_R_ADDR133	0x42025214	0x108A8058
PPC0_PPC_R_ADDR134	0x42025218	0x108A8060
PPC0_PPC_R_ADDR135	0x4202521C	0x108A8068
PPC0_PPC_R_ADDR136	0x42025220	0x108A8070
PPC0_PPC_R_ADDR137	0x42025224	0x108A8078
PPC0_PPC_R_ADDR138	0x42025228	0x108A8400
PPC0_PPC_R_ADDR139	0x4202522C	0x108A8408
PPC0_PPC_R_ADDR140	0x42025230	0x108A8410
PPC0_PPC_R_ADDR141	0x42025234	0x108A8418
PPC0_PPC_R_ADDR142	0x42025238	0x108A8420
PPC0_PPC_R_ADDR143	0x4202523C	0x108A8428
PPC0_PPC_R_ADDR144	0x42025240	0x108A8430
PPC0_PPC_R_ADDR145	0x42025244	0x108A8438
PPC0_PPC_R_ADDR146	0x42025248	0x108AC000
PPC0_PPC_R_ADDR147	0x4202524C	0x108AC040
PPC0_PPC_R_ADDR148	0x42025250	0x10900000
PPC0_PPC_R_ADDR149	0x42025254	0x10900100
PPC0_PPC_R_ADDR150	0x42025258	0x10900228

Register Name	Address of the register	Default value of register
PPC0_PPC_R_ADDR151	0x4202525C	0x10900240
PPC0_PPC_R_ADDR152	0x42025260	0x10900400
PPC0_PPC_R_ADDR153	0x42025264	0x10900800
PPC0_PPC_R_ADDR154	0x42025268	0x10901000
PPC0_PPC_R_ADDR155	0x4202526C	0x10903000
PPC0_PPC_R_ADDR156	0x42025270	0x10903400
PPC0_PPC_R_ADDR157	0x42025274	0x10904000
PPC0_PPC_R_ADDR158	0x42025278	0x10908000
PPC0_PPC_R_ADDR159	0x4202527C	0x10908400
PPC0_PPC_R_ADDR160	0x42025280	0x10908404
PPC0_PPC_R_ADDR161	0x42025284	0x10908408
PPC0_PPC_R_ADDR162	0x42025288	0x1090C000
PPC0_PPC_R_ADDR163	0x4202528C	0x1090C040
PPC0_PPC_R_ADDR164	0x42025290	0x1090C060
PPC0_PPC_R_ADDR165	0x42025294	0x10910000
PPC0_PPC_R_ADDR166	0x42025298	0x10910400
PPC0_PPC_R_ADDR167	0x4202529C	0x10910800
PPC0_PPC_R_ADDR168	0x420252A0	0x10910840
PPC0_PPC_R_ADDR169	0x420252A4	0x10910848
PPC0_PPC_R_ADDR170	0x420252A8	0x10912000
PPC0_PPC_R_ADDR171	0x420252AC	0x10A00000
PPC0_PPC_R_ADDR172	0x420252B0	0x10A00004
PPC0_PPC_R_ADDR173	0x420252B4	0x10A00008
PPC0_PPC_R_ADDR174	0x420252B8	0x10A0000C
PPC0_PPC_R_ADDR175	0x420252BC	0x10A00010
PPC0_PPC_R_ADDR176	0x420252C0	0x10A00014
PPC0_PPC_R_ADDR177	0x420252C4	0x10A00018
PPC0_PPC_R_ADDR178	0x420252C8	0x10A0001C
PPC0_PPC_R_ADDR179	0x420252CC	0x10A00020
PPC0_PPC_R_ADDR180	0x420252D0	0x10A00024
PPC0_PPC_R_ADDR181	0x420252D4	0x10A00028
PPC0_PPC_R_ADDR182	0x420252D8	0x10A0002C
PPC0_PPC_R_ADDR183	0x420252DC	0x10A00030
PPC0_PPC_R_ADDR184	0x420252E0	0x10A00034
PPC0_PPC_R_ADDR185	0x420252E4	0x10A00038
PPC0_PPC_R_ADDR186	0x420252E8	0x10A0003C
PPC0_PPC_R_ADDR187	0x420252EC	0x10A00040
PPC0_PPC_R_ADDR188	0x420252F0	0x10A00044
PPC0_PPC_R_ADDR189	0x420252F4	0x10A00048

Register Name	Address of the register	Default value of register
PPC0_PPC_R_ADDR190	0x420252F8	0x10A0004C
PPC0_PPC_R_ADDR191	0x420252FC	0x10A00050
PPC0_PPC_R_ADDR192	0x42025300	0x10A00054
PPC0_PPC_R_ADDR193	0x42025304	0x10A00400
PPC0_PPC_R_ADDR194	0x42025308	0x10A00404
PPC0_PPC_R_ADDR195	0x4202530C	0x10A00408
PPC0_PPC_R_ADDR196	0x42025310	0x10A0040C
PPC0_PPC_R_ADDR197	0x42025314	0x10A00410
PPC0_PPC_R_ADDR198	0x42025318	0x10A00414
PPC0_PPC_R_ADDR199	0x4202531C	0x10A00418
PPC0_PPC_R_ADDR200	0x42025320	0x10A0041C
PPC0_PPC_R_ADDR201	0x42025324	0x10A00420
PPC0_PPC_R_ADDR202	0x42025328	0x10A00424
PPC0_PPC_R_ADDR203	0x4202532C	0x10A00428
PPC0_PPC_R_ADDR204	0x42025330	0x10A0042C
PPC0_PPC_R_ADDR205	0x42025334	0x10A00430
PPC0_PPC_R_ADDR206	0x42025338	0x10A00434
PPC0_PPC_R_ADDR207	0x4202533C	0x10A00438
PPC0_PPC_R_ADDR208	0x42025340	0x10A0043C
PPC0_PPC_R_ADDR209	0x42025344	0x10A00440
PPC0_PPC_R_ADDR210	0x42025348	0x10A00444
PPC0_PPC_R_ADDR211	0x4202534C	0x10A00448
PPC0_PPC_R_ADDR212	0x42025350	0x10A0044C
PPC0_PPC_R_ADDR213	0x42025354	0x10A00450
PPC0_PPC_R_ADDR214	0x42025358	0x10A00454
PPC0_PPC_R_ADDR215	0x4202535C	0x10A00800
PPC0_PPC_R_ADDR216	0x42025360	0x10A00880
PPC0_PPC_R_ADDR217	0x42025364	0x10A04000
PPC0_PPC_R_ADDR218	0x42025368	0x10A04020
PPC0_PPC_R_ADDR219	0x4202536C	0x10A04040
PPC0_PPC_R_ADDR220	0x42025370	0x10A04060
PPC0_PPC_R_ADDR221	0x42025374	0x10A04080
PPC0_PPC_R_ADDR222	0x42025378	0x10A040A0
PPC0_PPC_R_ADDR223	0x4202537C	0x10A040C0
PPC0_PPC_R_ADDR224	0x42025380	0x10A040E0
PPC0_PPC_R_ADDR225	0x42025384	0x10A04100
PPC0_PPC_R_ADDR226	0x42025388	0x10A04120
PPC0_PPC_R_ADDR227	0x4202538C	0x10A04140
PPC0_PPC_R_ADDR228	0x42025390	0x10A04160

Register Name	Address of the register	Default value of register
PPC0_PPC_R_ADDR229	0x42025394	0x10A04180
PPC0_PPC_R_ADDR230	0x42025398	0x10A041A0
PPC0_PPC_R_ADDR231	0x4202539C	0x10A041C0
PPC0_PPC_R_ADDR232	0x420253A0	0x10A041E0
PPC0_PPC_R_ADDR233	0x420253A4	0x10A04200
PPC0_PPC_R_ADDR234	0x420253A8	0x10A04220
PPC0_PPC_R_ADDR235	0x420253AC	0x10A04240
PPC0_PPC_R_ADDR236	0x420253B0	0x10A04260
PPC0_PPC_R_ADDR237	0x420253B4	0x10A04280
PPC0_PPC_R_ADDR238	0x420253B8	0x10A042A0
PPC0_PPC_R_ADDR239	0x420253BC	0x10A04010
PPC0_PPC_R_ADDR240	0x420253C0	0x10A04030
PPC0_PPC_R_ADDR241	0x420253C4	0x10A04050
PPC0_PPC_R_ADDR242	0x420253C8	0x10A04070
PPC0_PPC_R_ADDR243	0x420253CC	0x10A04090
PPC0_PPC_R_ADDR244	0x420253D0	0x10A040B0
PPC0_PPC_R_ADDR245	0x420253D4	0x10A040D0
PPC0_PPC_R_ADDR246	0x420253D8	0x10A040F0
PPC0_PPC_R_ADDR247	0x420253DC	0x10A04110
PPC0_PPC_R_ADDR248	0x420253E0	0x10A04130
PPC0_PPC_R_ADDR249	0x420253E4	0x10A04150
PPC0_PPC_R_ADDR250	0x420253E8	0x10A04170
PPC0_PPC_R_ADDR251	0x420253EC	0x10A04190
PPC0_PPC_R_ADDR252	0x420253F0	0x10A041B0
PPC0_PPC_R_ADDR253	0x420253F4	0x10A041D0
PPC0_PPC_R_ADDR254	0x420253F8	0x10A041F0
PPC0_PPC_R_ADDR255	0x420253FC	0x10A04210
PPC0_PPC_R_ADDR256	0x42025400	0x10A04230
PPC0_PPC_R_ADDR257	0x42025404	0x10A04250
PPC0_PPC_R_ADDR258	0x42025408	0x10A04270
PPC0_PPC_R_ADDR259	0x4202540C	0x10A04290
PPC0_PPC_R_ADDR260	0x42025410	0x10A042B0
PPC0_PPC_R_ADDR261	0x42025414	0x10A05C00
PPC0_PPC_R_ADDR262	0x42025418	0x10A06000
PPC0_PPC_R_ADDR263	0x4202541C	0x10A06400
PPC0_PPC_R_ADDR264	0x42025420	0x10A082C0
PPC0_PPC_R_ADDR265	0x42025424	0x10A08440
PPC0_PPC_R_ADDR266	0x42025428	0x10A10000
PPC0_PPC_R_ADDR267	0x4202542C	0x10A10080

Register Name	Address of the register	Default value of register
PPC0_PPC_R_ADDR268	0x42025430	0x10A10400
PPC0_PPC_R_ADDR269	0x42025434	0x10A14000
PPC0_PPC_R_ADDR270	0x42025438	0x10A18000
PPC0_PPC_R_ADDR271	0x4202543C	0x10A18020
PPC0_PPC_R_ADDR272	0x42025440	0x10A18040
PPC0_PPC_R_ADDR273	0x42025444	0x10A18060
PPC0_PPC_R_ADDR274	0x42025448	0x10A18080
PPC0_PPC_R_ADDR275	0x4202544C	0x10A180A0
PPC0_PPC_R_ADDR276	0x42025450	0x10A180C0
PPC0_PPC_R_ADDR277	0x42025454	0x10A180E0
PPC0_PPC_R_ADDR278	0x42025458	0x10A1A000
PPC0_PPC_R_ADDR279	0x4202545C	0x10A1A020
PPC0_PPC_R_ADDR280	0x42025460	0x10A1A040
PPC0_PPC_R_ADDR281	0x42025464	0x10A1A060
PPC0_PPC_R_ADDR282	0x42025468	0x10A1A080
PPC0_PPC_R_ADDR283	0x4202546C	0x10A1A0A0
PPC0_PPC_R_ADDR284	0x42025470	0x10A1A0C0
PPC0_PPC_R_ADDR285	0x42025474	0x10A1A0E0
PPC0_PPC_R_ADDR286	0x42025478	0x10A1A100
PPC0_PPC_R_ADDR287	0x4202547C	0x10A1A120
PPC0_PPC_R_ADDR288	0x42025480	0x10A1A140
PPC0_PPC_R_ADDR289	0x42025484	0x10A1A160
PPC0_PPC_R_ADDR290	0x42025488	0x10A1A180
PPC0_PPC_R_ADDR291	0x4202548C	0x10A1A1A0
PPC0_PPC_R_ADDR292	0x42025490	0x10A1A1C0
PPC0_PPC_R_ADDR293	0x42025494	0x10A1A1E0
PPC0_PPC_R_ADDR294	0x42025498	0x10A1A200
PPC0_PPC_R_ADDR295	0x4202549C	0x10A1A220
PPC0_PPC_R_ADDR296	0x420254A0	0x10A1A240
PPC0_PPC_R_ADDR297	0x420254A4	0x10A1A260
PPC0_PPC_R_ADDR298	0x420254A8	0x10A1A280
PPC0_PPC_R_ADDR299	0x420254AC	0x10A1A2A0
PPC0_PPC_R_ADDR300	0x420254B0	0x10A1A2C0
PPC0_PPC_R_ADDR301	0x420254B4	0x10A1A2E0
PPC0_PPC_R_ADDR302	0x420254B8	0x10A20000
PPC0_PPC_R_ADDR303	0x420254BC	0x10A64000
PPC0_PPC_R_ADDR304	0x420254C0	0x10A68000
PPC0_PPC_R_ADDR305	0x420254C4	0x10A6C000
PPC0_PPC_R_ADDR306	0x420254C8	0x10A70000

Register Name	Address of the register	Default value of register
PPC0_PPC_R_ADDR307	0x420254CC	0x10A74000
PPC0_PPC_R_ADDR308	0x420254D0	0x10A78000
PPC0_PPC_R_ADDR309	0x420254D4	0x10A7C000
PPC0_PPC_R_ADDR310	0x420254D8	0x10A80000
PPC0_PPC_R_ADDR311	0x420254DC	0x10A84000
PPC0_PPC_R_ADDR312	0x420254E0	0x10A88000
PPC0_PPC_R_ADDR313	0x420254E4	0x10A8C000
PPC0_PPC_R_ADDR314	0x420254E8	0x10B40000
PPC0_PPC_R_ADDR315	0x420254EC	0x10A94000
PPC0_PPC_R_ADDR316	0x420254F0	0x10B00000
PPC0_PPC_R_ADDR317	0x420254F4	0x10B04000
PPC0_PPC_R_ADDR318	0x420254F8	0x10B60000
PPC1_PPC_R_ADDR0	0x44025000	0x11000000
PPC1_PPC_R_ADDR1	0x44025004	0x11001004
PPC1_PPC_R_ADDR2	0x44025008	0x11001010
PPC1_PPC_R_ADDR3	0x4402500C	0x11001024
PPC1_PPC_R_ADDR4	0x44025010	0x11001030
PPC1_PPC_R_ADDR5	0x44025014	0x11001044
PPC1_PPC_R_ADDR6	0x44025018	0x11001008
PPC1_PPC_R_ADDR7	0x4402501C	0x11001018
PPC1_PPC_R_ADDR8	0x44025020	0x11001028
PPC1_PPC_R_ADDR9	0x44025024	0x11001038
PPC1_PPC_R_ADDR10	0x44025028	0x11001048
PPC1_PPC_R_ADDR11	0x4402502C	0x11002000
PPC1_PPC_R_ADDR12	0x44025030	0x11008000
PPC1_PPC_R_ADDR13	0x44025034	0x11009000
PPC1_PPC_R_ADDR14	0x44025038	0x11010000
PPC1_PPC_R_ADDR15	0x4402503C	0x11040000
PPC1_PPC_R_ADDR16	0x44025040	0x11058000
PPC1_PPC_R_ADDR17	0x44025044	0x11058400
PPC1_PPC_R_ADDR18	0x44025048	0x11058401
PPC1_PPC_R_ADDR19	0x4402504C	0x11058830
PPC1_PPC_R_ADDR20	0x44025050	0x1105A000
PPC1_PPC_R_ADDR21	0x44025054	0x11068000
PPC1_PPC_R_ADDR22	0x44025058	0x11068400
PPC1_PPC_R_ADDR23	0x4402505C	0x11068440
PPC1_PPC_R_ADDR24	0x44025060	0x11068480
PPC1_PPC_R_ADDR25	0x44025064	0x110684C0
PPC1_PPC_R_ADDR26	0x44025068	0x11070000

Register Name	Address of the register	Default value of register
PPC1_PPC_R_ADDR27	0x4402506C	0x11070048
PPC1_PPC_R_ADDR28	0x44025070	0x11070080
PPC1_PPC_R_ADDR29	0x44025074	0x110700C0
PPC1_PPC_R_ADDR30	0x44025078	0x11070400
PPC1_PPC_R_ADDR31	0x4402507C	0x11071034
PPC1_PPC_R_ADDR32	0x44025080	0x11071038
PPC1_PPC_R_ADDR33	0x44025084	0x1107103C
PPC1_PPC_R_ADDR34	0x44025088	0x1107104C
PPC1_PPC_R_ADDR35	0x4402508C	0x1107105C
PPC1_PPC_R_ADDR36	0x44025090	0x11071064
PPC1_PPC_R_ADDR37	0x44025094	0x11071068
PPC1_PPC_R_ADDR38	0x44025098	0x1107106C
PPC1_PPC_R_ADDR39	0x4402509C	0x11071070
PPC1_PPC_R_ADDR40	0x440250A0	0x11071434
PPC1_PPC_R_ADDR41	0x440250A4	0x11071438
PPC1_PPC_R_ADDR42	0x440250A8	0x1107143C
PPC1_PPC_R_ADDR43	0x440250AC	0x1107144C
PPC1_PPC_R_ADDR44	0x440250B0	0x11071464
PPC1_PPC_R_ADDR45	0x440250B4	0x11071468
PPC1_PPC_R_ADDR46	0x440250B8	0x1107146C
PPC1_PPC_R_ADDR47	0x440250BC	0x11071470
PPC1_PPC_R_ADDR48	0x440250C0	0x11071435
PPC1_PPC_R_ADDR49	0x440250C4	0x11071439
PPC1_PPC_R_ADDR50	0x440250C8	0x1107143D
PPC1_PPC_R_ADDR51	0x440250CC	0x1107144D
PPC1_PPC_R_ADDR52	0x440250D0	0x11071465
PPC1_PPC_R_ADDR53	0x440250D4	0x11071469
PPC1_PPC_R_ADDR54	0x440250D8	0x1107146D
PPC1_PPC_R_ADDR55	0x440250DC	0x11071471
PPC1_PPC_R_ADDR56	0x440250E0	0x11071800
PPC1_PPC_R_ADDR57	0x440250E4	0x11072000
PPC1_PPC_R_ADDR58	0x440250E8	0x11074000
PPC1_PPC_R_ADDR59	0x440250EC	0x11074008
PPC1_PPC_R_ADDR60	0x440250F0	0x11074010
PPC1_PPC_R_ADDR61	0x440250F4	0x11074018
PPC1_PPC_R_ADDR62	0x440250F8	0x11074020
PPC1_PPC_R_ADDR63	0x440250FC	0x11074028
PPC1_PPC_R_ADDR64	0x44025100	0x11074030
PPC1_PPC_R_ADDR65	0x44025104	0x11074038

Register Name	Address of the register	Default value of register
PPC1_PPC_R_ADDR66	0x44025108	0x11074040
PPC1_PPC_R_ADDR67	0x4402510C	0x11074048
PPC1_PPC_R_ADDR68	0x44025110	0x11074050
PPC1_PPC_R_ADDR69	0x44025114	0x11074058
PPC1_PPC_R_ADDR70	0x44025118	0x11074060
PPC1_PPC_R_ADDR71	0x4402511C	0x11074068
PPC1_PPC_R_ADDR72	0x44025120	0x11074070
PPC1_PPC_R_ADDR73	0x44025124	0x11074078
PPC1_PPC_R_ADDR74	0x44025128	0x11074400
PPC1_PPC_R_ADDR75	0x4402512C	0x11074408
PPC1_PPC_R_ADDR76	0x44025130	0x11074410
PPC1_PPC_R_ADDR77	0x44025134	0x11074418
PPC1_PPC_R_ADDR78	0x44025138	0x11074420
PPC1_PPC_R_ADDR79	0x4402513C	0x11074428
PPC1_PPC_R_ADDR80	0x44025140	0x11074430
PPC1_PPC_R_ADDR81	0x44025144	0x11074438
PPC1_PPC_R_ADDR82	0x44025148	0x11100000
PPC1_PPC_R_ADDR83	0x4402514C	0x11102000
PPC1_PPC_R_ADDR84	0x44025150	0x11102040
PPC1_PPC_R_ADDR85	0x44025154	0x11102080
PPC1_PPC_R_ADDR86	0x44025158	0x111020C0
PPC1_PPC_R_ADDR87	0x4402515C	0x11102100
PPC1_PPC_R_ADDR88	0x44025160	0x11102140
PPC1_PPC_R_ADDR89	0x44025164	0x11106000
PPC1_PPC_R_ADDR90	0x44025168	0x11106080
PPC1_PPC_R_ADDR91	0x4402516C	0x11106040
PPC1_PPC_R_ADDR92	0x44025170	0x111060C0
PPC1_PPC_R_ADDR93	0x44025174	0x11114000
PPC1_PPC_R_ADDR94	0x44025178	0x11124000
PPC1_PPC_R_ADDR95	0x4402517C	0x11114800
PPC1_PPC_R_ADDR96	0x44025180	0x11124800
PPC1_PPC_R_ADDR97	0x44025184	0x11115000
PPC1_PPC_R_ADDR98	0x44025188	0x11125000
PPC1_PPC_R_ADDR99	0x4402518C	0x11115040
PPC1_PPC_R_ADDR100	0x44025190	0x11125040
PPC1_PPC_R_ADDR101	0x44025194	0x11115080
PPC1_PPC_R_ADDR102	0x44025198	0x11125080
PPC1_PPC_R_ADDR103	0x4402519C	0x11118000
PPC1_PPC_R_ADDR104	0x440251A0	0x11128000

Register Name	Address of the register	Default value of register
PPC1_PPC_R_ADDR105	0x440251A4	0x11118080
PPC1_PPC_R_ADDR106	0x440251A8	0x11128080
PPC1_PPC_R_ADDR107	0x440251AC	0x111181F0
PPC1_PPC_R_ADDR108	0x440251B0	0x111281F0
PPC1_PPC_R_ADDR109	0x440251B4	0x11118200
PPC1_PPC_R_ADDR110	0x440251B8	0x11128200
PPC1_PPC_R_ADDR111	0x440251BC	0x11118C00
PPC1_PPC_R_ADDR112	0x440251C0	0x11128C00
PPC1_PPC_R_ADDR113	0x440251C4	0x11118C40
PPC1_PPC_R_ADDR114	0x440251C8	0x11128C40
PPC1_PPC_R_ADDR115	0x440251CC	0x11118C80
PPC1_PPC_R_ADDR116	0x440251D0	0x11128C80
PPC1_PPC_R_ADDR117	0x440251D4	0x11119000
PPC1_PPC_R_ADDR118	0x440251D8	0x11119004
PPC1_PPC_R_ADDR119	0x440251DC	0x11119008
PPC1_PPC_R_ADDR120	0x440251E0	0x11129000
PPC1_PPC_R_ADDR121	0x440251E4	0x11129004
PPC1_PPC_R_ADDR122	0x440251E8	0x11129008
PPC1_PPC_R_ADDR123	0x440251EC	0x11119880
PPC1_PPC_R_ADDR124	0x440251F0	0x11129880
PPC1_PPC_R_ADDR125	0x440251F4	0x1111C000
PPC1_PPC_R_ADDR126	0x440251F8	0x1111C020
PPC1_PPC_R_ADDR127	0x440251FC	0x1111C040
PPC1_PPC_R_ADDR128	0x44025200	0x1112C000
PPC1_PPC_R_ADDR129	0x44025204	0x1112C020
PPC1_PPC_R_ADDR130	0x44025208	0x1112C040
PPC1_PPC_R_ADDR131	0x4402520C	0x1111C010
PPC1_PPC_R_ADDR132	0x44025210	0x1111C030
PPC1_PPC_R_ADDR133	0x44025214	0x1111C050
PPC1_PPC_R_ADDR134	0x44025218	0x1112C010
PPC1_PPC_R_ADDR135	0x4402521C	0x1112C030
PPC1_PPC_R_ADDR136	0x44025220	0x1112C050
PPC1_PPC_R_ADDR137	0x44025224	0x1111E000
PPC1_PPC_R_ADDR138	0x44025228	0x1112E000
PPC1_PPC_R_ADDR139	0x4402522C	0x1111E400
PPC1_PPC_R_ADDR140	0x44025230	0x1112E400
PPC1_PPC_R_ADDR141	0x44025234	0x11180000
PPC1_PPC_R_ADDR142	0x44025238	0x11180400
PPC1_PPC_R_ADDR143	0x4402523C	0x11180401

Register Name	Address of the register	Default value of register
PPC1_PPC_R_ADDR144	0x44025240	0x11180800
PPC1_PPC_R_ADDR145	0x44025244	0x11180C00
PPC1_PPC_R_ADDR146	0x44025248	0x11190000
PPC1_PPC_R_ADDR147	0x4402524C	0x11190044
PPC1_PPC_R_ADDR148	0x44025250	0x11190080
PPC1_PPC_R_ADDR149	0x44025254	0x11190800
PPC1_PPC_R_ADDR150	0x44025258	0x11190840
PPC1_PPC_R_ADDR151	0x4402525C	0x11190880
PPC1_PPC_R_ADDR152	0x44025260	0x11194000
PPC1_PPC_R_ADDR153	0x44025264	0x11198000
PPC1_PPC_R_ADDR154	0x44025268	0x11198400
PPC1_PPC_R_ADDR155	0x4402526C	0x11200000
PPC1_PPC_R_ADDR156	0x44025270	0x11200400
PPC1_PPC_R_ADDR157	0x44025274	0x11200800
PPC1_PPC_R_ADDR158	0x44025278	0x11204000
PPC1_PPC_R_ADDR159	0x4402527C	0x11208000
PPC1_PPC_R_ADDR160	0x44025280	0x11240000
PPC1_PPC_R_ADDR161	0x44025284	0x11250000
PPC1_PPC_R_ADDR162	0x44025288	0x12000000
PPC1_PPC_R_ADDR163	0x4402528C	0x12010000

11.3.1 PPC0_PPC_CTL

Description: PPC Control Registers

Address: 0x42020000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							RESP_CFG

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	RESP_CFG	Response Configuration. This field configures the security violation response. 0 - Read-Zero Write Ignore (RZWI) 1 - Bus Error Default Value: 0

11.3.2 PPC0_PPC_LOCK_MASK

Description: Locked Mask

Address: 0x4202000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	LOCK_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	LOCK_MASK	A mask that indicates which protection contexts are 'locked'. Once locked, a protection context cannot be unlocked until the next reset or power cycle. Bit i specifies the locked status for protection context i. 0: The protection context is unlocked. 1: The protection context is locked. When a PC is locked, the PPC_PC_MASK, PPC_NS_ATT and PPC_S_P_ATT register bits for peripheral regions to which this PC has access can no longer be modified (PPC_NS_P_ATT is not subject to these restrictions). The one exception to this is that PPC_PC_MASK bits associated with other protection contexts that are not themselves locked can still be cleared (but not set). Default Value: 0

11.3.3 PPC0_PPC_PC_MASK0

Description: Protection Context Mask

Address: 0x42021000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PC_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PC_MASK	A mask that indicates which protection contexts have access to a peripheral region. Bit i specifies the access for protection context i. 0: The protection context has no access to this region. 1: The protection context has access to this region, subject to secure and privilege attribute constraints setup in PPC_NS_ATT, PPC_S_P_ATT, PPC_NS_P_ATT registers) Default Value: 255

11.3.4 PPC0_PPC_NS_ATT0

Description: Non-secure attribute

Address: 0x42022000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	NS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	NS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	NS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	NS [31:24]							

Bits	Name	Description
31 : 0	NS	Non-Secure. Each bit indicates whether access to a peripheral region must be secure or non-secure: IF SECURITY_AWARE=0 0 - allow only secure access to respective peripheral region. 1 - allow only non-secure access to respective peripheral region. IF SECURITY_AWARE=1 0 - allow only secure access to respective peripheral region. 1 - allows both secure and non-secure access to respective peripheral region. (Note that, depending on this setting the privilege access requirement for this region is specified in the corresponding PPC_S_P_ATT or PPC_NS_P_ATT register) Default Value: 0

11.3.5 PPC0_PPC_S_P_ATT0

Description: Secure Privilege Attribute

Address: 0x42022400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	S_P [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	S_P [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	S_P [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	S_P [31:24]							

Bits	Name	Description
31 : 0	S_P	Secure Privilege. Each bit indicates whether access to a secure peripheral region requires privilege: 0 - allow only secure privileged access to respective peripheral region. 1 - allow only secure unprivileged or privileged access to respective peripheral region. Default Value: 0

11.3.6 PPC0_PPC_NS_P_ATT0

Description: Non-secure Privilege Attribute

Address: 0x42024000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	NS_P [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	NS_P [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	NS_P [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	NS_P [31:24]							

Bits	Name	Description
31 : 0	NS_P	Non-Secure Privilege. Each bit indicates whether access to a non-secure peripheral region requires privilege: 0 - allow only non-secure privileged access to respective peripheral region. 1 - allow only non-secure unprivileged or privileged access to respective peripheral region. Default Value: 0

11.3.7 PPC0_PPC_R_ADDR0

Description: Region Address

Address: 0x42025000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						Reserved	
HW Access	W						Reserved	
Name	R_ADDR [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276824064

11.3.8 PPC0_PPC_R_ATT0

Description: Region Attribute

Address: 0x42026000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.8 PPC0_PPC_R_ATT0 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 13

11.3.9 PPC0_PPC_R_ATT1

Description: Region Attribute

Address: 0x42026004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.9 PPC0_PPC_R_ATT1 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 2

11.3.10 PPC0_PPC_R_ATT2

Description: Region Attribute

Address: 0x42026008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.10 PPC0_PPC_R_ATT2 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 4

11.3.11 PPC0_PPC_R_ATT7

Description: Region Attribute

Address: 0x4202601C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.11 PPC0_PPC_R_ATT7 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 1

11.3.12 PPC0_PPC_R_ATT13

Description: Region Attribute

Address: 0x42026034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.12 PPC0_PPC_R_ATT13 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 14

11.3.13 PPC0_PPC_R_ATT16

Description: Region Attribute

Address: 0x42026040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.13 PPC0_PPC_R_ATT16 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 16

11.3.14 PPC0_PPC_R_ATT17

Description: Region Attribute

Address: 0x42026044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.14 PPC0_PPC_R_ATT17 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 12

11.3.15 PPC0_PPC_R_ATT19

Description: Region Attribute

Address: 0x4202604C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.15 PPC0_PPC_R_ATT19 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 8

11.3.16 PPC0_PPC_R_ATT20

Description: Region Attribute

Address: 0x42026050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.16 PPC0_PPC_R_ATT20 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 11

11.3.17 PPC0_PPC_R_ATT30

Description: Region Attribute

Address: 0x42026078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.17 PPC0_PPC_R_ATT30 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 5

11.3.18 PPC0_PPC_R_ATT31

Description: Region Attribute

Address: 0x4202607C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.18 PPC0_PPC_R_ATT31 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 3

11.3.19 PPC0_PPC_R_ATT32

Description: Region Attribute

Address: 0x42026080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.19 PPC0_PPC_R_ATT32 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 10

11.3.20 PPC0_PPC_R_ATT33

Description: Region Attribute

Address: 0x42026084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.20 PPC0_PPC_R_ATT33 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 15

11.3.21 PPC0_PPC_R_ATT34

Description: Region Attribute

Address: 0x42026088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.21 PPC0_PPC_R_ATT34 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 19

11.3.22 PPC0_PPC_R_ATT39

Description: Region Attribute

Address: 0x4202609C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.22 PPC0_PPC_R_ATT39 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 7

11.3.23 PPC0_PPC_R_ATT50

Description: Region Attribute

Address: 0x420260C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.23 PPC0_PPC_R_ATT50 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 6

11.3.24 PPC0_PPC_R_ATT55

Description: Region Attribute

Address: 0x420260DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			R_SIZE [28:24]				

Bits	Name	Description

11.3.24 PPC0_PPC_R_ATT55 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 9

11.3.25 PPC1_PPC_PC_MASK0

Description: Protection Context Mask

Address: 0x44021000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PC_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PC_MASK	A mask that indicates which protection contexts have access to a peripheral region. Bit i specifies the access for protection context i. 0: The protection context has no access to this region. 1: The protection context has access to this region, subject to secure and privilege attribute constraints setup in PPC_NS_ATT, PPC_S_P_ATT, PPC_NS_P_ATT registers) Default Value: 255

11.3.26 PPC1_PPC_NS_ATT0

Description: Non-secure attribute

Address: 0x44022000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	NS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	NS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	NS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	NS [31:24]							

Bits	Name	Description
31 : 0	NS	Non-Secure. Each bit indicates whether access to a peripheral region must be secure or non-secure: IF SECURITY_AWARE=0 0 - allow only secure access to respective peripheral region. 1 - allow only non-secure access to respective peripheral region. IF SECURITY_AWARE=1 0 - allow only secure access to respective peripheral region. 1 - allows both secure and non-secure access to respective peripheral region. (Note that, depending on this setting the privilege access requirement for this region is specified in the corresponding PPC_S_P_ATT or PPC_NS_P_ATT register) Default Value: 0

11.3.27 PPC1_PPC_S_P_ATT0

Description: Secure Privilege Attribute

Address: 0x44022400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	S_P [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	S_P [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	S_P [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	S_P [31:24]							

Bits	Name	Description
31 : 0	S_P	Secure Privilege. Each bit indicates whether access to a secure peripheral region requires privilege: 0 - allow only secure privileged access to respective peripheral region. 1 - allow only secure unprivileged or privileged access to respective peripheral region. Default Value: 0

11.3.28 PPC1_PPC_NS_P_ATT0

Description: Non-secure Privilege Attribute

Address: 0x44024000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	NS_P [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	NS_P [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	NS_P [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	NS_P [31:24]							

Bits	Name	Description
31 : 0	NS_P	Non-Secure Privilege. Each bit indicates whether access to a non-secure peripheral region requires privilege: 0 - allow only non-secure privileged access to respective peripheral region. 1 - allow only non-secure unprivileged or privileged access to respective peripheral region. Default Value: 0

11.1.29 PPC1_PPC_R_ADDR0

Description: Region Address

Address: 0x44025000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						Reserved	
HW Access	W						Reserved	
Name	R_ADDR [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 285212672

12 Cryptographic Accelerator registers

This section discusses the CRYPTO registers. It lists all the registers in mapping tables, in address order.

12.1 Register details

Register name	Address	Description
CRYPTO_CTL	0x42440000	Control
CRYPTO_RAM_PWR_CTL	0x42440008	SRAM power control
CRYPTO_RAM_PWR_DELAY_CTL	0x4244000C	SRAM power delay control
CRYPTO_ERROR_STATUS0	0x42440020	Error status 0
CRYPTO_ERROR_STATUS1	0x42440024	Error status 1
CRYPTO_INTR	0x42440100	Interrupt register
CRYPTO_INTR_SET	0x42440104	Interrupt set register
CRYPTO_INTR_MASK	0x42440108	Interrupt mask register
CRYPTO_INTR_MASKED	0x4244010C	Interrupt masked register
CRYPTO_PR_LFSR_CTL0	0x42440200	Pseudo random LFSR control 0
CRYPTO_PR_LFSR_CTL1	0x42440204	Pseudo random LFSR control 1
CRYPTO_PR_LFSR_CTL2	0x42440208	Pseudo random LFSR control 2
CRYPTO_PR_MAX_CTL	0x4244020C	Pseudo random maximum control
CRYPTO_PR_CMD	0x42440210	Pseudo random command
CRYPTO_PR_RESULT	0x42440218	Pseudo random result
CRYPTO_TR_CTL0	0x42440280	True random control 0
CRYPTO_TR_CTL1	0x42440284	True random control 1
CRYPTO_TR_CTL2	0x42440288	True random control 2
CRYPTO_TR_STATUS	0x4244028C	True random status
CRYPTO_TR_CMD	0x42440290	True random command
CRYPTO_TR_RESULT	0x42440298	True random result
CRYPTO_TR_GARO_CTL	0x424402A0	True random GARO control
CRYPTO_TR_FIRO_CTL	0x424402A4	True random FIRO control
CRYPTO_TR_MON_CTL	0x424402C0	True random monitor control
CRYPTO_TR_MON_CMD	0x424402C8	True random monitor command
CRYPTO_TR_MON_RC_CTL	0x424402D0	True random monitor RC control
CRYPTO_TR_MON_RC_STATUS0	0x424402D8	True random monitor RC status 0
CRYPTO_TR_MON_RC_STATUS1	0x424402DC	True random monitor RC status 1
CRYPTO_TR_MON_AP_CTL	0x424402E0	True random monitor AP control
CRYPTO_TR_MON_AP_STATUS0	0x424402E8	True random monitor AP status 0
CRYPTO_TR_MON_AP_STATUS1	0x424402EC	True random monitor AP status 1
CRYPTO_STATUS	0x42441004	Status
CRYPTO_INSTR_FF_CTL	0x42441040	Instruction FIFO control

Cryptographic Accelerator registers

Register name	Address	Description
CRYPTO_INSTR_FF_STATUS	0x42441044	Instruction FIFO status
CRYPTO_INSTR_FF_WR	0x42441048	Instruction FIFO write
CRYPTO_LOAD0_FF_STATUS	0x424410C0	Load 0 FIFO status
CRYPTO_LOAD1_FF_STATUS	0x424410D0	Load 1 FIFO status
CRYPTO_STORE_FF_STATUS	0x424410F0	Store FIFO status
CRYPTO_AES_CTL	0x42441100	AES control
CRYPTO_RESULT	0x42441180	Result
CRYPTO_CRC_CTL	0x42441400	CRC control
CRYPTO_CRC_DATA_CTL	0x42441410	CRC data control
CRYPTO_CRC_POL_CTL	0x42441420	CRC polynomial control
CRYPTO_CRC_REM_CTL	0x42441440	CRC remainder control
CRYPTO_CRC_REM_RESULT	0x42441448	CRC remainder result
CRYPTO_VU_CTL0	0x42441480	Vector unit control 0
CRYPTO_VU_CTL1	0x42441484	Vector unit control 1
CRYPTO_VU_CTL2	0x42441488	Vector unit control 2
CRYPTO_VU_STATUS	0x42441490	Vector unit status
CRYPTO_VU_RF_DATA0	0x424414C0	Vector unit register-file
CRYPTO_VU_RF_DATA1	0x424414C4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA2	0x424414C8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA3	0x424414CC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA4	0x424414D0	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA5	0x424414D4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA6	0x424414D8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA7	0x424414DC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA8	0x424414E0	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA9	0x424414E4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA10	0x424414E8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA11	0x424414EC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA12	0x424414F0	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.

Cryptographic Accelerator registers

Register name	Address	Description
CRYPTO_VU_RF_DATA13	0x424414F4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA14	0x424414F8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA15	0x424414FC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_DEV_KEY_ADDR0_CTL	0x42442000	Device key address 0 control
CRYPTO_DEV_KEY_ADDR0	0x42442004	Device key address 0
CRYPTO_DEV_KEY_ADDR1_CTL	0x42442020	Device key address 1 control
CRYPTO_DEV_KEY_ADDR1	0x42442024	Device key address 1 control
CRYPTO_DEV_KEY_STATUS	0x42442080	Device key status
CRYPTO_DEV_KEY_CTL0	0x42442100	Device key control 0
CRYPTO_DEV_KEY_CTL1	0x42442120	Device key control 1
CRYPTO_MEM_BUFF0	0x42448000	Memory buffer. This is the starting address of a register bank containing 1024 registers (CRYPTO_MEM_BUFF0 to CRYPTO_MEM_BUFF1023).

12.1.1 CRYPTO_CTL

Description: Control

Address: 0x42440000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				Reserved		RW	RW
HW Access	R				Reserved		R	R
Name	PC [7:4]				Reserved [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. All non-retention registers (command and status registers, instruct FIFO, internal component state machines) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. When the IP is enabled, the IP register buffer is set to "0". Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes this register; i.e. the context is inherited from the write transaction and not specified by the transaction write data. All IP master transactions use the PC field for the protection context. There is one exception: the LOAD_DEV_KEY instruction IP master transactions are always performed with protection context "0". Default Value: 0
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All IP master transactions use the NS field for the secure/non-secure access control ("hprot[4]"). Default Value: 1

12.1.1 CRYPTO_CTL (continued)

0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All IP master transactions use the P field for the user/privileged access control ("hprot[1]"). Default Value: 0

12.1.2 CRYPTO_RAM_PWR_CTL

Description: SRAM power control

Address: 0x42440008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	PWR_MODE	Set power mode for memory buffer SRAM. Default Value: 3 **0x0: OFF :** Turn OFF the SRAM. This will turn OFF both array and periphery power of the SRAM and SRAM memory contents are lost. **0x1: RESERVED :** undefined **0x2: RETAINED :** Keep SRAM in Retained mode. This will turn OFF the SRAM periphery power, but array power is ON to retain memory contents. The SRAM contents will be retained in DeepSleep/DeepSleep-RAM system power mode. **0x3: ENABLED :** Enable SRAM for regular operation. The SRAM contents will be retained in DeepSleep/DeepSleep-RAM system power mode.

12.1.3 CRYPTO_RAM_PWR_DELAY_CTL

Description: SRAM power delay control

Address: 0x4244000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	UP	Number clock cycles delay needed after power domain power up Default Value: 0x96

12.1.4 CRYPTO_ERROR_STATUS0

Description: Error status 0

Address: 0x42440020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Specifies error description information. - For INSTR_OPC_ERROR/ INSTR_CC_ERROR/ INSTR_DEV_KEY_ERROR: - Violating instruction (from instruction FIFO). - For BUS_ERROR: - Violating transfer, address. Default Value: Undefined

12.1.5 CRYPTO_ERROR_STATUS1

Description: Error status 1

Address: 0x42440024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DATA24 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DATA24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DATA24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved				R		
HW Access	RW	Reserved				RW		
Name	VALID	Reserved [30:27]				IDX [26:24]		

Bits	Name	Description
31	VALID	Specifies if ERROR_STATUS0 and ERROR_STATUS1 specify valid error information. No new error information is captured as long as VALID is '1'; i.e. the error information of the first detected error is NOT overwritten. Default Value: 0
26 : 24	IDX	Error source: "0": INSTR_OPC_ERROR (instruction FIFO decoder error). "1": INSTR_CC_ERROR (instruction FIFO decoder, VU CC error). "2": BUS_ERROR (bus master interface AHB-Lite bus error). "3": TR_AP_DETECT_ERROR. "4": TR_RC_DETECT_ERROR. "5": INSTR_DEV_KEY_ERROR. "6"-"7": Undefined. Default Value: Undefined
23 : 0	DATA24	Specifies error description information. - For BUS_ERROR: - Violating transfer, read attribute (DATA[0]). - Violating transfer, size attribute (DATA[5:4]). "0": 8-bit transfer, "1": 16 bits transfer, "2": 32-bit transfer. Default Value: Undefined

12.1.6 CRYPTO_INTR

Description: Interrupt register

Address: 0x42440100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved			RW1S	RW1S	RW1S	RW1S	RW1S
Name	Reserved [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	Reserved [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_-DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	This interrupt cause is activated (HW sets the field to '1') when the LOAD_DEV_KEY instruction tries to load a device key whose DEV_KEY_ADDR_CTL.VALID or DEV_KEY_CTL.ALLOWED is set to '0'. Default Value: 0
20	TR_RC_DETECT_ERROR	This interrupt cause is activated (HW sets the field to '1') when the true random number generator monitor adaptive proportion test detects a disproportionate occurrence of a specific bit value. Default Value: 0
19	TR_AP_DETECT_ERROR	This interrupt cause is activated (HW sets the field to '1') when the true random number generator monitor adaptive proportion test detects a repetition of a specific bit value. Default Value: 0
18	BUS_ERROR	This interrupt cause is activated (HW sets the field to '1') when a AHB-Lite bus error is observed on the AHB-Lite master interface. When the interrupt cause is activated, HW sets INSTR_FF_CTL.CLEAR to '1'. Default Value: 0
17	INSTR_CC_ERROR	This interrupt cause is activated (HW sets the field to '1') when the instruction decoder encounters an instruction with a non-defined condition code. This error is only generated for VU instructions. When the interrupt cause is activated, HW sets INSTR_FF_CTL.CLEAR to '1'. Default Value: 0

12.1.6 CRYPTO_INTR (continued)

16	INSTR_OPC_ERROR	This interrupt cause is activated (HW sets the field to '1') when the instruction decoder encounters an instruction with a non-defined operation code (opcode). When the interrupt cause is activated, HW sets INSTR_FF_CTL.CLEAR to '1'. Default Value: 0
4	PR_DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when the pseudo random number generator has generated a data value. Default Value: 0
3	TR_DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when the true random number generator has generated a data value of the specified bit size. Default Value: 0
2	TR_INITIALIZED	This interrupt cause is activated (HW sets the field to '1') when the true random number generator is initialized. Default Value: 0
1	INSTR_FF_OVERFLOW	This interrupt cause is activated (HW sets the field to '1') when the instruction FIFO overflows (an attempt is made to write to a full FIFO). Default Value: 0
0	INSTR_FF_LEVEL	This interrupt cause is activated (HW sets the field to '1') when the instruction FIFO event is activated. Default Value: 0

12.1.7 CRYPTO_INTR_SET

Description: Interrupt set register

Address: 0x42440104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	Reserved			A	A	A	A	A
Name	Reserved [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	Reserved		A	A	A	A	A	A
Name	Reserved [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_-DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
20	TR_RC_DETECT_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
19	TR_AP_DETECT_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
18	BUS_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
17	INSTR_CC_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
16	INSTR_OPC_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
4	PR_DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
3	TR_DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
2	TR_INITIALIZED	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

12.1.7 CRYPTO_INTR_SET (continued)

1	INSTR_FF_OVERFLOW	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
0	INSTR_FF_LEVEL	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

12.1.8 CRYPTO_INTR_MASK

Description: Interrupt mask register

Address: 0x42440108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	RW	RW	RW
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_-DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
20	TR_RC_DETECT_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
19	TR_AP_DETECT_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
18	BUS_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
17	INSTR_CC_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
16	INSTR_OPC_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
4	PR_DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0
3	TR_DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0
2	TR_INITIALIZED	Mask bit for corresponding field in interrupt request register. Default Value: 0

12.1.8 CRYPTO_INTR_MASK (continued)

1	INSTR_FF_OVERFLOW	Mask bit for corresponding field in interrupt request register. Default Value: 0
0	INSTR_FF_LEVEL	Mask bit for corresponding field in interrupt request register. Default Value: 0

12.1.9 CRYPTO_INTR_MASKED

Description: Interrupt masked register

Address: 0x4244010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R	R	R	R	R
HW Access	Reserved			W	W	W	W	W
Name	Reserved [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		W	W	W	W	W	W
Name	Reserved [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_-DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
20	TR_RC_DETECT_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
19	TR_AP_DETECT_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
18	BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
17	INSTR_CC_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
16	INSTR_OPC_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	PR_DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0
3	TR_DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0
2	TR_INITIALIZED	Logical and of corresponding request and mask bits. Default Value: 0

12.1.9 CRYPTO_INTR_MASKED (continued)

1	INSTR_FF_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
0	INSTR_FF_LEVEL	Logical and of corresponding request and mask bits. Default Value: 0

12.1.10 CRYPTO_PR_LFSR_CTL0

Description: Pseudo random LFSR control 0

Address: 0x42440200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description
31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. This register needs to be initialized by SW. The initialization value should be different from "0". The three PR_LFSR_CTL registers represents the state of a 32-bit, 31-bit and 29-bit LFSR. Individually, these LFSRs generate a pseudo random bit sequence that repeats itself after (2^32)-1, (2^31)-1 and (2^29)-1 bits. The numbers (2^32)-1, (2^31)-1 and (2^29)-1 are relatively prime (their greatest common denominator is "1"). The three bit sequence are combined (XOR'd) into a single bitstream to create a pseudo random bit sequence that repeats itself after ((2^32)-1) * ((2^31)-1) * ((2*29)-1) bits. The following polynomials are used: - 32-bit irreducible polynomial: x^32+x^30+x^26+x^25+1. - 31-bit irreducible polynomial: x^31+x^28+1. - 29-bit irreducible polynomial: x^29+x^27+1. Default Value: 0xD8959BC9

12.1.11 CRYPTO_PR_LFSR_CTL1

Description: Pseudo random LFSR control 1

Address: 0x42440204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW						
HW Access	Reserved	RW						
Name	Reserved	LFSR31 [30:24]						

Bits	Name	Description
30 : 0	LFSR31	State of a 31-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. See PR_LFSR_CTL0. Default Value: 0x2BB911F8

12.1.12 CRYPTO_PR_LFSR_CTL2

Description: Pseudo random LFSR control 2

Address: 0x42440208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR29 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR29 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR29 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [31:29]			LFSR29 [28:24]				

Bits	Name	Description
28 : 0	LFSR29	State of a 29-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. See PR_LFSR_CTL0. Default Value: 0x060C31B7

12.1.13 CRYPTO_PR_MAX_CTL

Description: Pseudo random maximum control

Address: 0x4244020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Maximum value of to be generated random number Default Value: 0xFFFFFFFF

12.1.14 CRYPTO_PR_CMD

Description: Pseudo random command

Address: 0x42440210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							RW1C
Name	Reserved [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	START	Pseudo random command. On a generated number, HW sets this field to '0' and sets INTR.PR_-DATA_AVAILABLE to '1. Default Value: 0

12.1.15 CRYPTO_PR_RESULT

Description: Pseudo random result

Address: 0x42440218

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Result of a pseudo random number generation operation. The resulting value DATA is in the range [0, PR_MAX_CTL.DATA32]. The PR_DATA_AVAILABLE interrupt cause is activated when the number is generated. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

12.1.16 CRYPTO_TR_CTL0

Description: True random control 0

Address: 0x42440280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_CLOCK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RED_CLOCK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INIT_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	Reserved			RW
HW Access	Reserved		R	R	Reserved			R
Name	Reserved [31:30]		STOP_ON_RC_DETECT	STOP_ON_AP_DETECT	Reserved [27:25]			VON_NEUMANN_CORR

Bits	Name	Description
29	STOP_ON_RC_DETECT	Specifies if TRNG functionality is stopped on a repetition count test detection (when HW sets INTR.TR_RC_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TR_CTL1 fields are set to '0' by HW). Default Value: 0
28	STOP_ON_AP_DETECT	Specifies if TRNG functionality is stopped on an adaptive proportion test detection (when HW sets INTR.TR_AP_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TR_CTL1 fields are set to '0' by HW). Default Value: 0
24	VON_NEUMANN_CORR	Specifies if the "von Neumann corrector" is disabled or enabled: '0': disabled. '1': enabled. The "von Neumann corrector" post-processes the reduced bits to remove a '0' or '1' bias. The corrector operates on reduced bit pairs ("oldest bit, newest bit"): "00": no bit is produced. "01": '0' bit is produced (oldest bit). "10": '1' bit is produced (oldest bit). "11": no bit is produced. Note that the corrector produces bits at a random pace and at a frequency that is 1/4 of the reduced bit frequency (reduced bits are processed in pairs, and half of the pairs do NOT produce a bit). Default Value: 0

12.1.16 CRYPTO_TR_CTL0 (continued)

23 : 16	INIT_DELAY	Specifies an initialization delay: number of removed/dropped samples before reduced bits are generated. This field should be programmed in the range [1, 255]. After starting the oscillators, at least the first 2 samples should be removed/dropped to clear the state of internal synchronizers. In addition, it is advised to drop at least the second 2 samples from the oscillators (to circumvent the semi-predictable oscillator startup behavior). This result in the default field value of "3". Field encoding is as follows: "0": 1 sample is dropped. "1": 2 samples are dropped. ... "255": 256 samples are dropped. The TR_INITIALIZED interrupt cause is set to '1', when the initialization delay is passed. Default Value: 3
15 : 8	RED_CLOCK_DIV	Specifies the clock divider that is used to produce reduced bits. "0": 1 reduced bit is produced for each sample. "1": 1 reduced bit is produced for each 2 samples. ... "255": 1 reduced bit is produced for each 256 samples. The reduced bits are considered random bits and shifted into TR_RESULT0.DATA32. Default Value: 0
7 : 0	SAMPLE_CLOCK_DIV	Specifies the clock divider that is used to sample oscillator data. This clock divider is wrt. "clk_sys". "0": sample clock is "clk_sys". "1": sample clock is "clk_sys"/2. ... "255": sample clock is "clk_sys"/256. Default Value: 0

12.1.17 CRYPTO_TR_CTL1

Description: True random control 1

Address: 0x42440284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	Reserved [7:6]		FIRO31_EN	FIRO15_EN	GA-RO31_EN	GA-RO15_EN	RO15_EN	RO11_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	FIRO31_EN	FW sets this field to '1' to enable the programmable Fibonacci ring oscillator with up to 31 inverters. The TR_FIRO_CTL register specifies the programmable polynomial. Default Value: 0
4	FIRO15_EN	FW sets this field to '1' to enable the fixed Fibonacci ring oscillator with 15 inverters. Default Value: 0
3	GARO31_EN	FW sets this field to '1' to enable the programmable Galois ring oscillator with up to 31 inverters. The TR_GARO_CTL register specifies the programmable polynomial. Default Value: 0
2	GARO15_EN	FW sets this field to '1' to enable the fixed Galois ring oscillator with 15 inverters. Default Value: 0
1	RO15_EN	FW sets this field to '1' to enable the ring oscillator with 15 inverters. Default Value: 0
0	RO11_EN	FW sets this field to '1' to enable the ring oscillator with 11 inverters. Default Value: 0

12.1.18 CRYPTO_TR_CTL2

Description: True random control 2

Address: 0x42440288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		SIZE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	SIZE	Bit size of generated random number in TR_RESULT. Legal range is in [0, 32]. Default Value: 0

12.1.19 CRYPTO_TR_STATUS

Description: True random status

Address: 0x4244028C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							INITIAL-IZED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	INITIALIZED	Reflects the state of the true random number generator: '0': Not initialized (TR_CTL0.INIT_DELAY has NOT passed). '1': Initialized (TR_CTL0.INIT_DELAY has passed). Default Value: 0

12.1.20 CRYPTO_TR_CMD

Description: True random command

Address: 0x42440290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							RW1C
Name	Reserved [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	START	True random command. On completion of the command, HW sets this field to '0' and sets INTR.TR_DATA_AVAILABLE to '1 when: - A random number is generated in TR_RESULT. - All ring oscillators are off (per TR_CTL1). - A repetition count (RC) or adaptive proportion (AP) error is detected during the random number generation (INTR.TR_RC/AP_DETECT_ERROR). Note: On completion of the command, SW should check TR_CTL1 and INTR.TR_RC/AP_DETECT_ERROR to ensure that no unexpected error occurred during random number generation. Default Value: 0

12.1.21 CRYPTO_TR_RESULT

Description: True random result

Address: 0x42440298

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Generated true random number. HW generates the number in the least significant bit positions (TR_CTL2.SIZE) of this field. The TR_DATA_AVAILABLE interrupt cause is activated when the number is generated. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

12.1.22 CRYPTO_TR_GARO_CTL

Description: True random GARO control

Address: 0x424402A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Galois ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

12.1.23 CRYPTO_TR_FIRO_CTL

Description: True random FIRO control

Address: 0x424402A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Fibonacci ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

12.1.24 CRYPTO_TR_MON_CTL

Description: True random monitor control

Address: 0x424402C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						BITSTREAM_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	BITSTREAM_SEL	Selection of the bitstream: "0": DAS bitstream. "1": RED bitstream. "2": TR bitstream. "3": Undefined. Default Value: 2

12.1.25 CRYPTO_TR_MON_CMD

Description: True random monitor command

Address: 0x424402C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						RW1C	RW1C
Name	Reserved [7:2]						START_RC	START_AP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	START_RC	Repetition count (RC) test enable: '0': Disabled. '1': Enabled. On a RC detection, HW sets this field to '0' and sets INTR.TR_RC_DETECT to '1. Default Value: 0
0	START_AP	Adaptive proportion (AP) test enable: '0': Stopped. '1': Started. On a AP detection, HW sets this field to '0' and sets INTR.TR_AP_DETECT to '1. Default Value: 0

12.1.26 CRYPTO_TR_MON_RC_CTL

Description: True random monitor RC control

Address: 0x424402D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	CUTOFF_COUNT8	Cutoff count (legal range is [1, 255]): "0": Illegal. "1": 1 repetition. ... "255": 255 repetitions. Default Value: 255

12.1.27 CRYPTO_TR_MON_RC_STATUS0

Description: True random monitor RC status 0

Address: 0x424402D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TR_MON_RC_STATUS1.REP_COUNT is NOT equal to "0". Default Value: 0

12.1.28 CRYPTO_TR_MON_RC_STATUS1

Description: True random monitor RC status 1

Address: 0x424402DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	REP_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	REP_COUNT	Number of repetitions of the current active bit counter: "0": 0 repetitions. ... "255": 255 repetitions. Default Value: 0

12.1.29 CRYPTO_TR_MON_AP_CTL

Description: True random monitor AP control

Address: 0x424402E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [31:24]							

Bits	Name	Description
31 : 16	WINDOW_SIZE	Window size (minus 1) : "0": 1 bit. ... "65535": 65536 bits. Default Value: 65535
15 : 0	CUTOFF_COUNT16	Cutoff count (legal range is [1, 65535]). "0": Illegal. "1": 1 occurrence. ... "65535": 65535 occurrences. Default Value: 65535

12.1.30 CRYPTO_TR_MON_AP_STATUS0

Description: True random monitor AP status 0

Address: 0x424402E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TR_MON_AP_STATUS1.OCC_COUNT is NOT equal to "0". Default Value: 0

12.1.31 CRYPTO_TR_MON_AP_STATUS1

Description: True random monitor AP status 1

Address: 0x424402EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [31:24]							

Bits	Name	Description
31 : 16	WINDOW_INDEX	Counter to keep track of the current index in the window (counts from "0" to TR_MON_AP_CTL.WINDOW_SIZE to "0"). Default Value: 0
15 : 0	OCC_COUNT	Number of occurrences of the current active bit counter: "0": 0 occurrences ... "65535": 65535 occurrences Default Value: 0

12.1.32 CRYPTO_STATUS

Description: Status

Address: 0x42441004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	BUSY	Reserved [30:24]						

Bits	Name	Description
31	BUSY	Reflects the state of the IP: '0': Idle/no busy. '1': Busy: - Instruction is pending in the instruction FIFO. - Instruction is busy in a IP component (e.g. SHA1, SHA2, SHA3, DES, TDES, AES, CHACHA, ...). - Store FIFO is busy. - TR or PR command is busy. Default Value: 0

12.1.33 CRYPTO_INSTR_FF_CTL

Description: Instruction FIFO control

Address: 0x42441040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					EVENT_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	RW
HW Access	Reserved						R	RW1S
Name	Reserved [23:18]						BLOCK	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17	BLOCK	This field specifies the behavior when an instruction is written to a full FIFO (INSTR_FIFO_WR MMIO register): '0': The write is ignored/dropped and the INTR.INSTR_FF_OVERFLOW interrupt cause is set to '1'. '1': The write is blocked, resulting in AHB-Lite wait states and the INTR.INSTR_FF_OVERFLOW interrupt cause is set to '1' (this cause may be masked out). The instruction is written to the FIFO as soon as a FIFO entry becomes available. The maximum time is roughly the time of the execution of the slowest/longest instruction. Note that this setting may "lock up" /stall the CPU. When the CPU is "locked up"/stalled it can not respond to any system interrupts. As a result, the interrupt latency is increased. Note that this may not be an issue if the associated CPU is only performing cryptography functionality, e.g. the CM0+ during boot time. Default Value: 1
16	CLEAR	When '1', the instruction FIFO is cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. HW sets this field to '1' on when a INSTR_OPC_ERROR, INSTR_CC_ERROR or BUS_ERROR interrupt cause is activated. Default Value: 0
2 : 0	EVENT_LEVEL	Event level. When the number of entries in the instruction FIFO is less than the amount of this field, an event is generated: - "event" = INSTR_FF_STATUS.USED < EVENT_LEVEL. Default Value: 0

12.1.34 CRYPTO_INSTR_FF_STATUS

Description: Instruction FIFO status

Address: 0x42441044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				USED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [23:17]							EVENT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	EVENT	Instruction FIFO event. Default Value: 0
3 : 0	USED	Number of instructions in the instruction FIFO. The value of this field ranges from 0 to 8. Default Value: 0

12.1.35 CRYPTO_INSTR_FF_WR

Description: Instruction FIFO write

Address: 0x42441048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Instruction or instruction operand data that is written to the instruction FIFO. Default Value: 0

12.1.36 CRYPTO_LOAD0_FF_STATUS

Description: Load 0 FIFO status

Address: 0x424410C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [7:5]			USED5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	BUSY	Reserved [30:24]						

Bits	Name	Description
31	BUSY	Reflects the state of the FIFO: '0': FIFO load engine is idle and a new FIFO instruction can be accepted. '1': FIFO load engine is busy and NO new FIFO instruction can be accepted. Default Value: 0
4 : 0	USED5	Number of Bytes in the FIFO. The value of this field is in the range [0, 19]. Default Value: 0

12.1.37 CRYPTO_LOAD1_FF_STATUS

Description: Load 1 FIFO status

Address: 0x424410D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [7:5]			USED5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	BUSY	Reserved [30:24]						

Bits	Name	Description
31	BUSY	See LOAD1_FF_STATUS.BUSY. Default Value: 0
4 : 0	USED5	See LOAD1_FF_STATUS.USED. Default Value: 0

12.1.38 CRYPTO_STORE_FF_STATUS

Description: Store FIFO status

Address: 0x424410F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [7:5]			USED5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	BUSY	Reserved [30:24]						

Bits	Name	Description
31	BUSY	Reflects the state of the FIFO: '0': FIFO store engine is idle and a new FIFO instruction can be accepted (USED is "0"). '1': FIFO store engine is busy and NO new FIFO instruction can be accepted. Default Value: 0
4 : 0	USED5	Number of Bytes in the FIFO. The value of this field is in the range [0, 16]. Default Value: 0

12.1.39 CRYPTO_AES_CTL

Description: AES control

Address: 0x42441100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						KEY_SIZE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	KEY_SIZE	AES key size: "0": 128-bit key, 10 rounds AES (inverse) cipher operation. "1": 192-bit key, 12 rounds AES (inverse) cipher operation. "2": 256-bit key, 14 rounds AES (inverse) cipher operation. "3": Undefined Default Value: 0 **0x0: AES128 :** **0x1: AES192 :** **0x2: AES256 :**

12.1.40 CRYPTO_RESULT

Description: Result

Address: 0x42441180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	BLOCK_CMP operation (DATA[0]): "0": source 0 equals source 1. "1": source 0 does NOT equal source 1. CRC operation (DATA[31:0]). State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value. The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

12.1.41 CRYPTO_CRC_CTL

Description: CRC control

Address: 0x42441400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							DATA_REVERSE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							REM_REVERSE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	REM_REVERSE	Specifies whether the remainder is bit reversed (reversal is performed after XORing): '0': No. '1': Yes. Default Value: 0
0	DATA_REVERSE	Specifies the bit order in which a data Byte is processed (reversal is performed after XORing): '0': Most significant bit (bit 1) first. '1': Least significant bit (bit 0) first. Default Value: 0

12.1.42 CRYPTO_CRC_DATA_CTL

Description: CRC data control

Address: 0x42441410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DATA_XOR	Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. Default Value: 0

12.1.43 CRYPTO_CRC_POL_CTL

Description: CRC polynomial control

Address: 0x42441420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [31:24]							

Bits	Name	Description
31 : 0	POLYNOMIAL	CRC polynomial. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned/shifted such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials: - CRC32: POLYNOMIAL is 0x04c11db7 (x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1). - CRC16: POLYNOMIAL is 0x80050000 (x^16 + x^15 + x^2 + 1, shifted by 16 bit positions). - CRC16 CCITT: POLYNOMIAL is 0x10210000 (x^16 + x^12 + x^5 + 1, shifted by 16 bit positions). Default Value: 0

12.1.44 CRYPTO_CRC_REM_CTL

Description: CRC remainder control

Address: 0x42441440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REM_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REM_XOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	REM_XOR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	REM_XOR [31:24]							

Bits	Name	Description
31 : 0	REM_XOR	Specifies a mask with which the CRC_LFSR_CTL.LFSR32 register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. Default Value: 0

12.1.45 CRYPTO_CRC_REM_RESULT

Description: CRC remainder result

Address: 0x42441448

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	REM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	REM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	REM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	REM [31:24]							

Bits	Name	Description
31 : 0	REM	Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE: '0': the more significant bits (bit 31 and down) contain the remainder. '1': the less significant bits (bit 0 and up) contain the remainder. Note: This field is combinatorially derived from CRC_LFSR_CTL.LFSR32, CRC_REM_CTL0.REM_REVERSE and CRC_REM_CTL1.REM_XOR. Default Value: 0

12.1.46 CRYPTO_VU_CTL0

Description: Vector unit control 0

Address: 0x42441480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							ALWAYS_EXECUTE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	ALWAYS_EXECUTE	Specifies if a conditional instruction is executed or not, when its condition code evaluates to false/'0'. '0': The instruction is NOT executed. As a result, the instruction may be handled faster than when it is executed. '1': The instruction is executed, but the execution result (including status field information) is not reflected in the IP. The instruction is handled just as fast as when it is executed. Note: a conditional instruction with a condition code that evaluates to false/'0' does not affect the architectural state: VU_STATUS fields, memory or register-file data. Note: Always execution is useful to prevent/complicate differential timing and differential power attacks. Default Value: 0

12.1.47 CRYPTO_VU_CTL1

Description: Vector unit control 1

Address: 0x42441484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	Specifies the memory address for the vector unit operand memory region. The register-file registers provide 13-bit word offsets within this memory region. Given ADDR[31:8], VU_VTL2.MASK[14:8] and a 13-bit word offset offset[14:2], a vector operand memory address VU_OPERAND_ADDR[31:0] is calculated as follows: - VU_OPERAND_ADDR[31:15] = ADDR[31:15] - VU_OPERAND_ADDR[14:8] = (ADDR[14:8] & MASK[14:8]) | (offset[14:8] & ~MASK[14:8]) - VU_OPERAND_ADDR[7:2] = offset[7:2] - VU_OPERAND_ADDR[1:0] = 0 (always word aligned) The vector unit operand memory region uses either the IP's memory buffer or system memory. For best performance, the IP's memory buffer should be used and ADDR should be set to MEM_BUFF and MASK should specify the IP memory buffer size. If a vector operand memory address is mapped on a memory hole, read accesses return a "0" and write accesses are ignored Note: The base address of the IP internal memory buffer is equal to IP_ADDR + MEM_BUFF where. - IP_ADDR is the top-level design time parameter. - MEM_BUFF is address offset value for MEM_BUFF MMIO register.. Default Value: 0

12.1.48 CRYPTO_VU_CTL2

Description: Vector unit control 2

Address: 0x42441488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	MASK [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14 : 8	MASK	Specifies the size of the vector operand memory region. Legal values: "0b0000000": 32 KB memory region (VU_VTL1.ADDR[14:8] ignored). "0b1000000": 16 KB memory region (VU_VTL1.ADDR[13:8] ignored). "0b1100000": 8 KB memory region (VU_VTL1.ADDR[12:8] ignored). "0b1110000": 4 KB memory region (VU_VTL1.ADDR[11:8] ignored). "0b1111000": 2 KB memory region (VU_VTL1.ADDR[10:8] ignored). "0b1111100": 1 KB memory region (VU_VTL1.ADDR[9:8] ignored). "0b1111110": 512 B memory region (VU_VTL1.ADDR[8] ignored). "0b1111111": 256 B memory region. Note: the default specifies a 256 B memory region. Default Value: 0x7F

12.1.49 CRYPTO_VU_STATUS

Description: Vector unit status

Address: 0x42441490

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [7:4]				ONE	ZERO	EVEN	CARRY

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	ONE	STATUS ONE field. Default Value: 0
2	ZERO	STATUS ZERO field. Default Value: 0
1	EVEN	STATUS EVEN field. Default Value: 0
0	CARRY	STATUS CARRY field. Default Value: 0

12.1.50 CRYPTO_VU_RF_DATA0

Description: Vector unit register-file

Address: 0x424414C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Vector unit register-file data. A register-file register has the following layout: DATA[28:16]: data (typically used as a word offset in vector unit operand memory). DATA[12:0]: bit size minus 1. Default Value: 0

12.1.51 CRYPTO_DEV_KEY_ADDR0_CTL

Description: Device key address 0 control

Address: 0x42442000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	VALID	Reserved [30:24]						

Bits	Name	Description
31	VALID	Specifies if the address in the associated DEV_KEY_ADDR0 is valid: '0': Address not valid; i.e. no device key specified. '1': Address valid; i.e. device key specified. Note: A LOAD_DEV_KEY instruction requires that the device key's valid field is '1'. Default Value: 0

12.1.52 CRYPTO_DEV_KEY_ADDR0

Description: Device key address 0

Address: 0x42442004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR32 [31:24]							

Bits	Name	Description
31 : 0	ADDR32	Specifies the memory address of the device key in memory. A LOAD_DEV_KEY instruction uses this address to load a device key from memory into the IP register buffer blocks 4 and 5. Default Value: 0

12.1.53 CRYPTO_DEV_KEY_ADDR1_CTL

Description: Device key address 1 control

Address: 0x42442020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	VALID	Reserved [30:24]						

Bits	Name	Description
31	VALID	See DEV_KEY_ADDR0_CTL. Default Value: 0

12.1.54 CRYPTO_DEV_KEY_ADDR1

Description: Device key address 1 control

Address: 0x42442024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR32 [31:24]							

Bits	Name	Description
31 : 0	ADDR32	See DEV_KEY_ADDR0. Default Value: 0

12.1.55 CRYPTO_DEV_KEY_STATUS

Description: Device key status

Address: 0x42442080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							LOADED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	LOADED	Specifies if a device key is present in the IP register buffer blocks 4 and 5. HW sets this field to '1' on successful completion of a LOAD_DEV_KEY instruction. HW clears this field to '0' when a CLEAR instruction is executed (the CLEAR instruction also sets the IP register buffer to "0"). Default Value: 0

12.1.56 CRYPTO_DEV_KEY_CTL0

Description: Device key control 0

Address: 0x42442100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							ALLOWED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	ALLOWED	Specifies if a LOAD_DEV_KEY instruction is allowed to use the device key in memory: '0': Not allowed. '1': Allowed. Note: For successful completion of a LOAD_DEV_KEY instruction, both the associated DEV_KEY_ADDR_CTL.VALID and DEV_KEY_CTL.ALLOWED fields must be '1'. On successful instruction completion, DEV_KEY_STATUS.LOADED is set to '1'. On unsuccessful completion, the instruction FIFO is cleared and the IP is locked; an Active reset or an IP reset (CTL.ENABLED), which reinitializes the IP, is required. Note: A LOAD_DEV_KEY loads the device key from memory with protection context "0". Default Value: 0

12.1.57 CRYPTO_DEV_KEY_CTL1

Description: Device key control 1

Address: 0x42442120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							ALLOWED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	ALLOWED	See DEV_KEY_CTL0. Default Value: 0

12.1.58 CRYPTO_MEM_BUFF0

Description: Memory buffer

Address: 0x42448000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: Undefined

13 Device Power Modes registers

This section discusses the Device power modes registers. It lists all the registers in mapping tables, in address order.

13.1 Register details

Register name	Address	Description
PWRMODE_PD0_PD_SENSE	0x42410000	Dependency Sense Register
PWRMODE_PD0_PD_SPT	0x42410004	Dependency Support Register
PWRMODE_PD1_PD_SENSE	0x42410010	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD1_PD_SPT	0x42410014	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD2_PD_SENSE	0x42410020	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD2_PD_SPT	0x42410024	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD3_PD_SENSE	0x42410030	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD3_PD_SPT	0x42410034	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD4_PD_SENSE	0x42410040	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD4_PD_SPT	0x42410044	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD5_PD_SENSE	0x42410050	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD5_PD_SPT	0x42410054	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD6_PD_SENSE	0x42410060	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD6_PD_SPT	0x42410064	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD7_PD_SENSE	0x42410070	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD7_PD_SPT	0x42410074	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD8_PD_SENSE	0x42410080	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD8_PD_SPT	0x42410084	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD9_PD_SENSE	0x42410090	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.

Device Power Modes registers

Register name	Address	Description
PWRMODE_PD9_PD_SPT	0x42410094	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD10_PD_SENSE	0x424100A0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD10_PD_SPT	0x424100A4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD11_PD_SENSE	0x424100B0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD11_PD_SPT	0x424100B4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD12_PD_SENSE	0x424100C0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD12_PD_SPT	0x424100C4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD13_PD_SENSE	0x424100D0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD13_PD_SPT	0x424100D4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD14_PD_SENSE	0x424100E0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD14_PD_SPT	0x424100E4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD15_PD_SENSE	0x424100F0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD15_PD_SPT	0x424100F4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PPU_MAIN_PPU_PWPR	0x42411000	Power Policy Register
PWRMODE_PPU_MAIN_PPU_PMER	0x42411004	Power Mode Emulation Register
PWRMODE_PPU_MAIN_PPU_PWSR	0x42411008	Power Status Register
PWRMODE_PPU_MAIN_PPU_DISR	0x42411010	Device Interface Input Current Status Register
PWRMODE_PPU_MAIN_PPU_MISR	0x42411014	Miscellaneous Input Current Status Register
PWRMODE_PPU_MAIN_PPU_STSR	0x42411018	Stored Status Register
PWRMODE_PPU_MAIN_PPU_UNLK	0x4241101C	Unlock register
PWRMODE_PPU_MAIN_PPU_PWCR	0x42411020	Power Configuration Register
PWRMODE_PPU_MAIN_PPU_PTCR	0x42411024	Power Mode Transition Configuration Register
PWRMODE_PPU_MAIN_PPU_IMR	0x42411030	Interrupt Mask Register
PWRMODE_PPU_MAIN_PPU_AIMR	0x42411034	Additional Interrupt Mask Register
PWRMODE_PPU_MAIN_PPU_ISR	0x42411038	Interrupt Status Register
PWRMODE_PPU_MAIN_PPU_AISR	0x4241103C	Additional Interrupt Status Register
PWRMODE_PPU_MAIN_PPU_IESR	0x42411040	Input Edge Sensitivity Register
PWRMODE_PPU_MAIN_PPU_OPSR	0x42411044	Operating Mode Active Edge Sensitivity Register

Device Power Modes registers

Register name	Address	Description
PWRMODE_PPU_MAIN_PPU_FUNRR	0x42411050	Functional Retention RAM Configuration Register
PWRMODE_PPU_MAIN_PPU_FULRR	0x42411054	Full Retention RAM Configuration Register
PWRMODE_PPU_MAIN_PPU_MEMRR	0x42411058	Memory Retention RAM Configuration Register
PWRMODE_PPU_MAIN_PPU_EDTR0	0x42411160	Power Mode Entry Delay Register 0
PWRMODE_PPU_MAIN_PPU_EDTR1	0x42411164	Power Mode Entry Delay Register 1
PWRMODE_PPU_MAIN_PPU_DCDR0	0x42411170	Device Control Delay Configuration Register 0
PWRMODE_PPU_MAIN_PPU_DCDR1	0x42411174	Device Control Delay Configuration Register 1
PWRMODE_PPU_MAIN_PPU_IDR0	0x42411FB0	PPU Identification Register 0
PWRMODE_PPU_MAIN_PPU_IDR1	0x42411FB4	PPU Identification Register 1
PWRMODE_PPU_MAIN_PPU_IIDR	0x42411FC8	Implementation Identification Register
PWRMODE_PPU_MAIN_PPU_AIDR	0x42411FCC	Architecture Identification Register
PWRMODE_CLK_SELECT	0x42412000	Clock Selection for Power Mode Components
PWRMODE_PDCM_HWSTAT_IN	0x42412004	PPU Status input
PWRMODE_PDCM_PD_PRESENT	0x42412008	Mask for whether a PD is present in the PDCM
PWRMODE_PPU_PD1_PWPR	0x42413000	Power Policy Register
PWRMODE_PPU_PD1_PMER	0x42413004	Power Mode Emulation Register. See PWRMODE_PPU_MAIN_PPU_PMER for the details of bit fields.
PWRMODE_PPU_PD1_PWSR	0x42413008	Power Status Register. See PWRMODE_PPU_MAIN_PPU_PWSR for the details of bit fields.
PWRMODE_PPU_PD1_DISR	0x42413010	Device Interface Input Current Status Register. See PWRMODE_PPU_MAIN_PPU_DISR for the details of bit fields.
PWRMODE_PPU_PD1_MISR	0x42413014	Miscellaneous Input Current Status Register. See PWRMODE_PPU_MAIN_PPU_MISR for the details of bit fields.
PWRMODE_PPU_PD1_STSR	0x42413018	Stored Status Register. See PWRMODE_PPU_MAIN_PPU_STSR for the details of bit fields.
PWRMODE_PPU_PD1_UNLK	0x4241301C	Unlock register. See PWRMODE_PPU_MAIN_PPU_UNLK for the details of bit fields.
PWRMODE_PPU_PD1_PWCR	0x42413020	Power Configuration Register. See PWRMODE_PPU_MAIN_PPU_PWCR for the details of bit fields.
PWRMODE_PPU_PD1_PTCR	0x42413024	Power Mode Transition Configuration Register. See PWRMODE_PPU_MAIN_PPU_PTCR for the details of bit fields.
PWRMODE_PPU_PD1_IMR	0x42413030	Interrupt Mask Register. See PWRMODE_PPU_MAIN_PPU_IMR for the details of bit fields.

Device Power Modes registers

Register name	Address	Description
PWRMODE_PPU_PD1_AIMR	0x42413034	Additional Interrupt Mask Register. See PWRMODE_PPU_MAIN_PPU_AIMR for the details of bit fields.
PWRMODE_PPU_PD1_ISR	0x42413038	Interrupt Status Register. See PWRMODE_PPU_MAIN_PPU_ISR for the details of bit fields.
PWRMODE_PPU_PD1_AISR	0x4241303C	Additional Interrupt Status Register. See PWRMODE_PPU_MAIN_PPU_AISR for the details of bit fields.
PWRMODE_PPU_PD1_IESR	0x42413040	Input Edge Sensitivity Register. See PWRMODE_PPU_MAIN_PPU_IESR for the details of bit fields.
PWRMODE_PPU_PD1_OPSR	0x42413044	Operating Mode Active Edge Sensitivity Register. See PWRMODE_PPU_MAIN_PPU_OPSR for the details of bit fields.
PWRMODE_PPU_PD1_FUNRR	0x42413050	Functional Retention RAM Configuration Register. See PWRMODE_PPU_MAIN_PPU_FUNRR for the details of bit fields.
PWRMODE_PPU_PD1_FULRR	0x42413054	Full Retention RAM Configuration Register. See PWRMODE_PPU_MAIN_PPU_FULRR for the details of bit fields.
PWRMODE_PPU_PD1_MEMRR	0x42413058	Memory Retention RAM Configuration Register. See PWRMODE_PPU_MAIN_PPU_MEMRR for the details of bit fields.
PWRMODE_PPU_PD1_EDTR0	0x42413160	Power Mode Entry Delay Register 0. See PWRMODE_PPU_MAIN_PPU_EDTR0 for the details of bit fields.
PWRMODE_PPU_PD1_EDTR1	0x42413164	Power Mode Entry Delay Register 1. See PWRMODE_PPU_MAIN_PPU_EDTR1 for the details of bit fields.
PWRMODE_PPU_PD1_DCDR0	0x42413170	Device Control Delay Configuration Register 0. See PWRMODE_PPU_MAIN_PPU_DCDR0 for the details of bit fields.
PWRMODE_PPU_PD1_DCDR1	0x42413174	Device Control Delay Configuration Register 1. See PWRMODE_PPU_MAIN_PPU_DCDR1 for the details of bit fields.
PWRMODE_PPU_PD1_IDR0	0x42413FB0	PPU Identification Register 0. See PWRMODE_PPU_MAIN_PPU_IDR0 for the details of bit fields.
PWRMODE_PPU_PD1_IDR1	0x42413FB4	PPU Identification Register 1. See PWRMODE_PPU_MAIN_PPU_IDR1 for the details of bit fields.
PWRMODE_PPU_PD1_IIDR	0x42413FC8	Implementation Identification Register. See PWRMODE_PPU_MAIN_PPU_IIDR for the details of bit fields.

Device Power Modes registers

Register name	Address	Description
PWRMODE_PPU_PD1_AIDR	0x42413FCC	Architecture Identification Register. See PWRMODE_PPU_MAIN_PPU_AIDR for the details of bit fields.
PWRMODE_PD0_CTRL_PD_CTL	0x42414000	Power Domain Control
PWRMODE_PD0_CTRL_PD_PWR_UP_DELAY	0x42414004	Active switch weak enable to active switch strong enable delay
PWRMODE_PD1_CTRL_PD_CTL	0x42415000	Power Domain Control. See PWRMODE_PD0_CTRL_PD_CTL for the details of bit fields.
PWRMODE_PD1_CTRL_PD_PWR_UP_DELAY	0x42415004	Active switch weak enable to active switch strong enable delay. See PWRMODE_PD0_CTRL_PD_PWR_UP_DELAY for the details of bit fields.

13.1.1 PWRMODE_PD0_PD_SENSE

Description: Dependency Sense Register

Address: 0x42410000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	PD_ON [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	PD_ON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	PD_ON	Each bit *indicates whether PD is directly kept on when PD is on. Indirect dependency is still possible if multiple direct dependencies work together to create a transitive relationship. For example, if PD1 depends upon PD2; and PD2 dpends upon PD3; then PD1 indirectly depends upon PD3 regardless of whether there is a direct dependency from PD3 to PD1. Some bits are implemented as constants, and some bits are implemented as user-configurable registers. Refer to PD_SPT register to see how each bit is implemented. Default Value: X*

13.1.2 PWRMODE_PD0_PD_SPT

Description: Dependency Support Register

Address: 0x42410004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PD_FORCE_ON [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	PD_FORCE_ON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	PD_CONFIG_ON [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PD_CONFIG_ON [31:24]							

Bits	Name	Description
31 : 16	PD_CONFIG_ON	Each bit *indicates whether PD can be configured on when PD is on. Default Value: X*
15 : 0	PD_FORCE_ON	Each bit *indicates whether PD is always kept on when PD is on for sense bits that are not configurable. For configurable bits, this indicates the reset value of the configurable bit. Default Value: X*

13.1.3 PWRMODE_PPU_MAIN_PPU_PWPR

Description: Power Policy Register

Address: 0x42411000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			LOCK_EN	Reserved [11:9]			PWR_DY-N_EN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							OP_DY-N_EN

Bits	Name	Description
24	OP_DYN_EN	Reserved Default Value: 0x0
19 : 16	OP_POLICY	Reserved Default Value: 0x0
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. For main PPU, keep this bit 1. Default Value: 0x1
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), MEM_RET(2), FULL_RET(5), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x8

13.1.4 PWRMODE_PPU_MAIN_PPU_PMER

Description: Power Mode Emulation Register

Address: 0x42411004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							EMU_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	EMU_EN	Reserved Default Value: 0x0

13.1.5 PWRMODE_PPU_MAIN_PPU_PWSR

Description: Power Status Register

Address: 0x42411008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [7:4]				PWR_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved			R
HW Access	Reserved			RW	Reserved			RW
Name	Reserved [15:13]			LOCK_STA-TUS	Reserved [11:9]			PWR_DY-N_STATUS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R			
HW Access	Reserved				RW			
Name	Reserved [23:20]				OP_STATUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [31:25]							OP_DY-N_STATUS

Bits	Name	Description
24	OP_DYN_STATUS	Reserved Default Value: 0x0
19 : 16	OP_STATUS	Reserved Default Value: 0x0
12	LOCK_STATUS	Reserved Default Value: 0x0
8	PWR_DYN_STATUS	Power mode dynamic transition status. When set to 1 power mode dynamic transitions are enabled. There might be a delay in dynamic transitions becoming active or inactive if the PPU is transitioning when PWR_DYN_EN is programmed. Default Value: 0x0
3 : 0	PWR_STATUS	Power mode status. These bits reflect the current power mode of the PPU. See PPU_PWPR.PWR_POLICY for power mode enumeration. Default Value: 0x0

13.1.6 PWRMODE_PPU_MAIN_PPU_DISR

Description: Device Interface Input Current Status Register

Address: 0x42411010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PWR_DEVACTIVE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					R		
HW Access	Reserved					RW		
Name	Reserved [15:11]					PWR_DEVACTIVE_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	OP_DEVACTIVE_STATUS [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVE_STATUS	Reserved Default Value: 0x0
10 : 0	PWR_DEVACTIVE_STATUS	Status of the power mode DEVACTIVE inputs. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 0 is for Q-channel device 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0

13.1.7 PWRMODE_PPU_MAIN_PPU_MISR

Description: Miscellaneous Input Current Status Register

Address: 0x42411014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							PCSMPAC-CEPT_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DEVACCEPT_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DEVDENY_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	DEVDENY_STATUS	Status of the device interface DEVDENY inputs. There is one bit for each device interface DEVQDENY. For example, bit 16 is for Q-Channel 0 DEVQDENY, and bit 17 for Q-Channel 1 DEVQDENY. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
15 : 8	DEVACCEPT_STATUS	Status of the device interface DEVACCEPT inputs. There is one bit for each device interface DEVQACCEPTn. For example, bit 8 is for Q-Channel 0 DEVQACCEPTn and bit 9 for Q-Channel 1 DEVQACCEPTn. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
0	PCSMPACCEPT_STA-TUS	The status of the PCSMPACCEPT input. Default Value: 0x0

13.1.8 PWRMODE_PPU_MAIN_PPU_STSR

Description: Stored Status Register

Address: 0x42411018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	STORED_DEVDENY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	STORED_DEVDENY	Status of the DEVDENY signals from the last device interface Q-Channel transition. For Q-Channel: There is one bit for each device interface DEVQDENY. For example, bit 0 is for Q-Channel 0 DEVQDENY, and bit 1 for Q-Channel 1 DEVQDENY. Refer to PPU_DISR.PWR_DEVACTIVE_STATUS for device enumeration. Default Value: 0x0

13.1.9 PWRMODE_PPU_MAIN_PPU_UNLK

Description: Unlock register

Address: 0x4241101C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							UNLOCK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	UNLOCK	Reserved Default Value: 0x0

13.1.10 PWRMODE_PPU_MAIN_PPU_PWCR

Description: Power Configuration Register

Address: 0x42411020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVREQEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PWR_DEVACTIVEEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_DEVACTIVEEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	OP_DEVACTIVEEN [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVEEN	Reserved Default Value: 0x00
18 : 8	PWR_DEVACTIVEEN	These bits enable the power mode DEVACTIVE inputs. When a bit is to 1 the related DEVACTIVE input is enabled, when set to 0 it is disabled. All available bits are reset to 1. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE, and bit 9 for the Q-Channel 1 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x001
7 : 0	DEVREQEN	When set to 1 enables the device interface handshake for transitions. All available bits are reset to 1. There is one bit for each device interface channel. For example, bit 0 is for Q-Channel 0, and bit 1 is for Q-Channel 1. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x01

13.1.11 PWRMODE_PPU_MAIN_PPU_PTCR

Description: Power Mode Transition Configuration Register

Address: 0x42411024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						DBG_RE-COV_POR ST_EN	WARM_RS T_DEVREQ EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	DBG_RE-COV_PORST_EN	Reserved Default Value: 0x0
0	WARM_RST_DEVREQEN	Transition behavior between ON and WARM_RST. This bit should not be modified when the PPU is in WARM_RST, or if the PPU is performing a transition, otherwise PPU behavior is UN-PREDICTABLE. 0: The PPU does not perform a device interface handshake when transitioning between ON and WARM_RST. 1: The PPU performs a device interface handshake when transitioning between ON and WARM_RST. This disables all Q-Channels for this transition. Default Value: 0x0

13.1.12 PWRMODE_PPU_MAIN_PPU_IMR

Description: Interrupt Mask Register

Address: 0x42411030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		LOCKED_IRQ_MASK	EMU_DENY_IRQ_MASK	EMU_ACCEPT_IRQ_MASK	STA_DENY_IRQ_MASK	STA_ACCEPT_IRQ_MASK	STA_POLICY_TRN_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	LOCKED_IRQ_MASK	Reserved Default Value: 0x0
4	EMU_DENY_IRQ_MASK	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ_MASK	Reserved Default Value: 0x0
2	STA_DENY_IRQ_MASK	Static transition denial event mask. Default Value: 0x0
1	STA_ACCEPT_IRQ_MASK	Static transition acceptance event mask. For main PPU, keep this bit 1 to mask the event, otherwise the interrupt may trigger a wakeup. Default Value: 0x1
0	STA_POLICY_TRN_IRQ_MASK	Static full policy transition completion event mask. For main PPU, this bit has no function because no static transitions are supported (see PWPR.PWR_DYN_EN). Default Value: 0x0

13.1.13 PWRMODE_PPU_MAIN_PPU_AIMR

Description: Additional Interrupt Mask Register

Address: 0x42411034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	RW	RW	RW
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ_MASK	STA_POLICY_PWR_IRQ_MASK	DYN_DENY_IRQ_MASK	DYN_ACCEPT_IRQ_MASK	UNSPT_POLICY_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ_MASK	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ_MASK	Reserved Default Value: 0x0
2	DYN_DENY_IRQ_MASK	Dynamic transition denial event mask. Default Value: 0x1
1	DYN_ACCEPT_IRQ_MASK	Dynamic transition acceptance event mask. For main PPU, keep this bit 1 to mask the event, otherwise the interrupt that occurs when entering a low power mode may trigger a wakeup. Default Value: 0x1
0	UNSPT_POLICY_IRQ_MASK	Unsupported Policy event mask. Default Value: 0x0

13.1.14 PWRMODE_PPU_MAIN_PPU_ISR

Description: Interrupt Status Register

Address: 0x42411038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	Reserved	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	Reserved	R	R	R	R	R	R
Name	OTH-ER_IRQ	Reserved	LOCKED_IRQ	EMU_DE-NY_IRQ	EMU_AC-CEPT_IRQ	STA_DE-NY_IRQ	STA_AC-CEPT_IRQ	STA_POLI-CY_TRN_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	PWR_ACTIVE_EDGE_IRQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW1C		
HW Access	Reserved					R		
Name	Reserved [23:19]					PWR_ACTIVE_EDGE_IRQ [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	OP_ACTIVE_EDGE_IRQ [31:24]							

Bits	Name	Description
31 : 24	OP_ACTIVE_EDGE_IRQ	Indicates which operating mode DEVPACTIVE inputs caused the input edge event. When operating modes are not supported this field is reserved. Default Value: 0x0
18 : 8	PWR_ACTIVE_EDGE_IRQ	Indicates which power mode DEVACTIVE inputs caused the input edge event. Bits for unused channels are the MSBs and are reserved. There is one bit for each device Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x00
7	OTHER_IRQ	Indicates there is an interrupt event pending in the Additional Interrupt Status Register (PPU_AISR). Default Value: 0x0
5	LOCKED_IRQ	Reserved Default Value: 0x0
4	EMU_DENY_IRQ	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ	Reserved Default Value: 0x0
2	STA_DENY_IRQ	Static transition denial event status. Default Value: 0x0
1	STA_ACCEPT_IRQ	Static transition acceptance event status. Default Value: 0x0

13.1.14 PWRMODE_PPU_MAIN_PPU_ISR (continued)

0	STA_POLICY_TRN_IRQ	Static full policy transition completion event status. Default Value: 0x0

13.1.15 PWRMODE_PPU_MAIN_PPU_AISR

Description: Additional Interrupt Status Register

Address: 0x4241103C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved			R	R	R	R	R
Name	Reserved [7:5]			STA_POLICY_OP_IRQ	STA_POLICY_PWR_IRQ	DYN_DENY_IRQ	DYN_ACCEPT_IRQ	UNSPT_POLICY_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ	Reserved Default Value: 0x0
2	DYN_DENY_IRQ	Dynamic transition denial event status. Default Value: 0x0
1	DYN_ACCEPT_IRQ	Dynamic transition acceptance event status. Default Value: 0x0
0	UNSPT_POLICY_IRQ	Unsupported Policy event status. Default Value: 0x0

13.1.16 PWRMODE_PPU_MAIN_PPU_IESR

Description: Input Edge Sensitivity Register

Address: 0x42411040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE03_EDGE [7:6]		DEVACTIVE02_EDGE [5:4]		DEVACTIVE01_EDGE [3:2]		DEVACTIVE00_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE07_EDGE [15:14]		DEVACTIVE06_EDGE [13:12]		DEVACTIVE05_EDGE [11:10]		DEVACTIVE04_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		RW		RW	
HW Access	Reserved		R		R		R	
Name	Reserved [23:22]		DEVACTIVE10_EDGE [21:20]		DEVACTIVE09_EDGE [19:18]		DEVACTIVE08_EDGE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 20	DEVACTIVE10_EDGE	Reserved Default Value: 0x0
19 : 18	DEVACTIVE09_EDGE	Reserved Default Value: 0x0
17 : 16	DEVACTIVE08_EDGE	Reserved Default Value: 0x0
15 : 14	DEVACTIVE07_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE06_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE05_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE04_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE03_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE02_EDGE	DEVACTIVE 2 edge sensitivity. Default Value: 0x0
3 : 2	DEVACTIVE01_EDGE	DEVACTIVE 1 edge sensitivity. Default Value: 0x0

13.1.16 PWRMODE_PPU_MAIN_PPU_IESR (continued)

1 : 0	DEVACTIVE00_EDGE	DEVACTIVE 0 edge sensitivity. Default Value: 0x0

13.1.17 PWRMODE_PPU_MAIN_PPU_OPSR

Description: Operating Mode Active Edge Sensitivity Register

Address: 0x42411044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE19_EDGE [7:6]		DEVACTIVE18_EDGE [5:4]		DEVACTIVE17_EDGE [3:2]		DEVACTIVE16_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE23_EDGE [15:14]		DEVACTIVE22_EDGE [13:12]		DEVACTIVE21_EDGE [11:10]		DEVACTIVE20_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	DEVACTIVE23_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE22_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE21_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE20_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE19_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE18_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE17_EDGE	Reserved Default Value: 0x0
1 : 0	DEVACTIVE16_EDGE	Reserved Default Value: 0x0

13.1.18 PWRMODE_PPU_MAIN_PPU_FUNRR

Description: Functional Retention RAM Configuration Register

Address: 0x42411050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FUNC_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FUNC_RET_RAM_CFG	Reserved Default Value: 0x0

13.1.19 PWRMODE_PPU_MAIN_PPU_FULRR

Description: Full Retention RAM Configuration Register

Address: 0x42411054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FULL_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	FULL_RET_RAM_CFG	Reserved Default Value: 0x0

13.1.20 PWRMODE_PPU_MAIN_PPU_MEMRR

Description: Memory Retention RAM Configuration Register

Address: 0x42411058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	MEM_RET_RAM_CFG	Reserved Default Value: 0x0

13.1.21 PWRMODE_PPU_MAIN_PPU_EDTR0

Description: Power Mode Entry Delay Register 0

Address: 0x42411160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOGIC_RET_DEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	FULL_RET_DEL [31:24]							

Bits	Name	Description
31 : 24	FULL_RET_DEL	Reserved Default Value: 0x00
23 : 16	LOGIC_RET_DEL	Reserved Default Value: 0x00
15 : 8	MEM_RET_DEL	Reserved Default Value: 0x00
7 : 0	OFF_DEL	Reserved Default Value: 0x00

13.1.22 PWRMODE_PPU_MAIN_PPU_EDTR1

Description: Power Mode Entry Delay Register 1

Address: 0x42411164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FUNC_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	FUNC_RET_DEL	Reserved Default Value: 0x00
7 : 0	MEM_OFF_DEL	Reserved Default Value: 0x00

13.1.23 PWRMODE_PPU_MAIN_PPU_DCDR0

Description: Device Control Delay Configuration Register 0

Address: 0x42411170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CLKEN_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ISO_CLKEN_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RST_HWSTAT_DLY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	RST_HWSTAT_DLY	Reserved Default Value: 0x0
15 : 8	ISO_CLKEN_DLY	Reserved Default Value: 0x0
7 : 0	CLKEN_RST_DLY	Reserved Default Value: 0x0

13.1.24 PWRMODE_PPU_MAIN_PPU_DCDR1

Description: Device Control Delay Configuration Register 1

Address: 0x42411174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ISO_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CLKEN_ISO_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	CLKEN_ISO_DLY	Reserved Default Value: 0x0
7 : 0	ISO_RST_DLY	Reserved Default Value: 0x0

13.1.25 PWRMODE_PPU_MAIN_PPU_IDR0

Description: PPU Identification Register 0

Address: 0x42411FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	NUM_OPMODE [7:4]				DEVCHAN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	STA_-FUNC_RET_SPT	STA_-FULL_RET_SPT	STA_MEM_OFF_SPT	STA_LG-C_RET_SPT	STA_MEM_RET_EMU_SPT	STA_MEM_RET_SPT	STA_OFF_EMU_SPT	STA_OFF_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	Reserved	R	R	R
HW Access	RW	RW	RW	RW	Reserved	RW	RW	RW
Name	DY-N_MEM_RET_EMU_SPT	DY-N_MEM_RET_SPT	DY-N_OFF_EMU_SPT	DY-N_OFF_SPT	Reserved	STA_DB-G_RE-COV_SPT	STA_WRM_RST_SPT	STA_ON_SPT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [31:30]		DY-N_WRM_RST_SPT	DY-N_ON_SPT	DYN_-FUNC_RET_SPT	DYN_-FULL_RET_SPT	DY-N_MEM_OFF_SPT	DYN_LG-C_RET_SPT

Bits	Name	Description
29	DYN_WRM_RST_SPT	Dynamic WARM_RST support. Default Value: 0x0
28	DYN_ON_SPT	Dynamic ON support. Default Value: 0x1
27	DYN_FUNC_RET_SPT	Dynamic FUNC_RET support. Default Value: 0x0
26	DYN_FULL_RET_SPT	Dynamic FULL_RET support. Default Value: 0x1
25	DYN_MEM_OFF_SPT	Dynamic MEM_OFF support. Default Value: 0x0
24	DYN_LGC_RET_SPT	Dynamic LOGIC_RET support. Default Value: 0x0
23	DY-N_MEM_RET_EMU_SPT	Dynamic MEM_RET_EMU support Default Value: 0x0
22	DYN_MEM_RET_SPT	Dynamic MEM_RET support. Default Value: 0x1

13.1.25 PWRMODE_PPU_MAIN_PPU_IDR0 (continued)

21	DYN_OFF_EMU_SPT	Dynamic OFF_EMU support. Default Value: 0x0
20	DYN_OFF_SPT	Dynamic OFF support. Default Value: 0x1
18	STA_DBG_RECOV_SPT	DBG_RECOV support. Default Value: 0x0
17	STA_WRM_RST_SPT	WARM_RST support. Ignore this bit. Do not use WARM_RST. Default Value: 0x1
16	STA_ON_SPT	ON support. Default Value: 0x1
15	STA_FUNC_RET_SPT	FUNC_RET support. Default Value: 0x0
14	STA_FULL_RET_SPT	FULL_RET support. Default Value: 0x1
13	STA_MEM_OFF_SPT	MEM_OFF support. Default Value: 0x0
12	STA_LGC_RET_SPT	LOGIC_RET support. Default Value: 0x0
11	STA_MEM_RET_EMU_SPT	MEM_RET_EMU support. Default Value: 0x0
10	STA_MEM_RET_SPT	MEM_RET support. Default Value: 0x1
9	STA_OFF_EMU_SPT	OFF_EMU support. Default Value: 0x0
8	STA_OFF_SPT	OFF support. Default Value: 0x1
7 : 4	NUM_OPMODE	No. of operating modes supported is NUM_OPMODE + 1. Default Value: 0x0
3 : 0	DEVCHAN	No. of Device Interface Channels. 0: This is a P-Channel PPU. Refer to PPU_IDR1.OP_ACTIVE for the number of DEVPACTIVE inputs and their meaning. non-zero: The value is the number of Q-Channels. The device enumeration is: Device 0: PDCM Default Value: 0x1

13.1.26 PWRMODE_PPU_MAIN_PPU_IDR1

Description: PPU Identification Register 1

Address: 0x42411FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	Reserved	R	R	R
HW Access	Reserved	RW	RW	RW	Reserved	RW	RW	RW
Name	Reserved	FUNC_RET_RAM_REG	FULL_RET_RAM_REG	MEM_RET_RAM_REG	Reserved	LOCK_SPT	SW_DEV_DEL_SPT	PWR_-MODE_EN-TRY_DEL_SPT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved	R	R	R
HW Access	Reserved			RW	Reserved	RW	RW	RW
Name	Reserved [15:13]			OFF_MEM_RET_TRANS	Reserved	OP_AC-TIVE	STA_POLI-CY_OP_IRQ_SPT	STA_POLI-CY_P-WR_IRQ_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	OFF_MEM_RET_TRANS	OFF to MEM_RET direct transition. Indicates if direct transitions from OFF to MEM_RET and from OFF_EMU to MEM_RET_EMU are supported. Default Value: 0x0
10	OP_ACTIVE	Operating mode use model for dynamic transitions. 0: Ladder use model. 1: Independent use model. When operating modes are not supported (PPU_IDR0.NUM_OPMODE==0), this field is reserved. Default Value: 0x0
9	STA_POLI-CY_OP_IRQ_SPT	Operating policy transition completion event status. Default Value: 0x0
8	STA_POLICY_P-WR_IRQ_SPT	Power policy transition completion event status. Default Value: 0x0
6	FUNC_RET_RAM_REG	Indicates if the PPU_FUNRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
5	FULL_RET_RAM_REG	Indicates if the PPU_FULRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
4	MEM_RET_RAM_REG	Indicates if the PPU_MEMRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0

13.1.26 PWRMODE_PPU_MAIN_PPU_IDR1 (continued)

2	LOCK_SPT	Lock and the lock interrupt event are supported. Default Value: 0x0
1	SW_DEV_DEL_SPT	Software device delay control configuration support. Default Value: 0x0
0	PWR_MODE_EN-TRY_DEL_SPT	Power mode entry delay support. Default Value: 0x0

13.1.27 PWRMODE_PPU_MAIN_PPU_IIDR

Description: Implementation Identification Register

Address: 0x42411FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IMPLEMENTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	REVISION [15:12]				IMPLEMENTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PRODUCT_ID [23:20]				VARIANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 20	PRODUCT_ID	PPU part identification. Default Value: 0x0B5
19 : 16	VARIANT	Major revision of the product. Default Value: 0
15 : 12	REVISION	Minor revision of the product. Default Value: 0
11 : 0	IMPLEMENTER	Implementer identification. [11:8] The JEP106 continuation code of the implementer. [7] Always 0. [6:0] The JEP106 identity code of the implementer. For an Arm implementation, bits [11:0] are 0x43B. Default Value: 0x43B

13.1.28 PWRMODE_PPU_MAIN_PPU_AIDR

Description: Architecture Identification Register

Address: 0x42411FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	ARCH_REV_MAJOR [7:4]				ARCH_REV_MINOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	ARCH_REV_MAJOR	0x1 - PPU architecture major revision 1. Other Values - Reserved. Default Value: 0x1
3 : 0	ARCH_REV_MINOR	0x1 - PPU Architecture minor revision 1. Other Values - Reserved. Default Value: 0x1

13.1.29 PWRMODE_CLK_SELECT

Description: Clock Selection for Power Mode Components

Address: 0x42412000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLK_PWR_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [23:18]						CLK_PWR_MUX [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 16	CLK_PWR_MUX	Selects a source for the clock used by power control components. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0 **0x0: IHO :** IHO - Internal High-speed Oscillator **0x1: IMO :** IMO - Internal R/C Oscillator **0x2: RESERVED :** reserved
7 : 0	CLK_PWR_DIV	clk_pwr is generated by dividing the CLK_PWR_MUX selection by (CLK_PWR_DIV+1). Default Value: 4

13.1.30 PWRMODE_PDCM_HWSTAT_IN

Description: PPU Status input

Address: 0x42412004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PPU_HWSTAT_ON [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	PPU_HWSTAT_ON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	PPU_HWSTAT_ON	Each bit represents the PPU 'ON' Status of connected PPU. 1: PPU is ON Default Value: x

13.1.31 PWRMODE_PDCM_PD_PRESENT

Description: Mask for whether a PD is present in the PDCM

Address: 0x42412008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PRESENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	PRESENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	PRESENT	Mask for whether a PD is present in the PDCM Default Value: x

13.1.32 PWRMODE_PPU_PD1_PWPR

Description: Power Policy Register

Address: 0x42413000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			LOCK_EN	Reserved [11:9]			PWR_DYN_EN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							OP_DYN_EN

Bits	Name	Description
24	OP_DYN_EN	Reserved Default Value: 0x0
19 : 16	OP_POLICY	Reserved Default Value: 0x0
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. For main PPU, keep this bit 1. Default Value: 0x1
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), MEM_RET(2), FULL_RET(5), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x0

13.1.33 PWRMODE_PD0_CTRL_PD_CTL

Description: Power Domain Control

Address: 0x42414000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							BLEED_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	BLEED_EN	Activates bleed feature for the controlled power domain Default Value: 0

13.1.34 PWRMODE_PD0_CTRL_PD_PWR_UP_DELAY

Description: Active switch weak enable to active switch strong enable delay

Address: 0x42414004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COUNT_LOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_COUNT_LOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	MEM_COUNT_LOAD	Load value for counter running on clk_pwr (10MHz) providing the timing from weak MEM switch enable to strong MEM switch enable. Default is 5 for ~500ns Default Value: 0
7 : 0	COUNT_LOAD	Load value for counter running on clk_pwr (10MHz) providing the timing from weak ACTIVE switch enable to strong ACTIVE switch enable. Default is 5 for ~500ns Default Value: 5

14 System Resources Subsystem (SRSS) registers

This section discusses the SRSS registers. It lists all the registers in mapping tables, in address order.

14.1 Register details

Register name	Address	Description
CLK_DSI_SELECT0	0x42400100	Clock DSI Select Register
CLK_DSI_SELECT1	0x42400104	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT2	0x42400108	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT3	0x4240010C	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT4	0x42400110	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT5	0x42400114	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_OUTPUT_FAST	0x42400140	Fast Clock Output Select Register
CLK_OUTPUT_SLOW	0x42400144	Slow Clock Output Select Register
CLK_CAL_CNT1	0x42400148	Clock Calibration Counter 1
CLK_CAL_CNT2	0x4240014C	Clock Calibration Counter 2
SRSS_INTR	0x42400200	SRSS Interrupt Register
SRSS_INTR_SET	0x42400204	SRSS Interrupt Set Register
SRSS_INTR_MASK	0x42400208	SRSS Interrupt Mask Register
SRSS_INTR_MASKED	0x4240020C	SRSS Interrupt Masked Register
SRSS_AINTR	0x42400300	SRSS Additional Interrupt Register
SRSS_AINTR_SET	0x42400304	SRSS Additional Interrupt Set Register
SRSS_AINTR_MASK	0x42400308	SRSS Additional Interrupt Mask Register
SRSS_AINTR_MASKED	0x4240030C	SRSS Additional Interrupt Masked Register
PWR_LVD_STATUS	0x42400340	High Voltage / Low Voltage Detector (HVLVD) Status Register
BOOT_DLM_CTL	0x42400404	Debug Control Register
BOOT_DLM_CTL2	0x42400408	Debug Control Register 2
BOOT_DLM_STATUS	0x4240040C	Debug Status Register
RES_SOFT_CTL	0x42400410	Soft Reset Trigger Register
BOOT_STATUS	0x42400418	Boot Execution Status Register
BOOT_ENTRY	0x42400430	Warm Boot Entry Address
PWR_HIB_DATA0	0x42400800	Hibernate Data Register. This is the starting address of a register bank containing 32 registers (PWR_HIB_DATA0 to PWR_HIB_DATA31).
PWR_HIB_WAKE_CTL	0x424008A0	Hibernate Wakeup Mask Register
PWR_HIB_WAKE_CTL2	0x424008A4	Hibernate Wakeup Polarity Register

System Resources Subsystem (SRSS) registers

Register name	Address	Description
PWR_HIB_WAKE_CAUSE	0x424008AC	Hibernate Wakeup Cause Register
TST_XRES_SECURE	0x42400914	SECURE TEST and FIRMWARE TEST Key control register
PWR_CTL	0x42401000	Power Mode Control
PWR_CTL2	0x42401004	Power Mode Control 2
PWR_HIBERNATE	0x42401008	HIBERNATE Mode Register
PWR_LVD_CTL	0x42401020	High Voltage / Low Voltage Detector (HVLVD) Configuration Register
CLK_PATH_SELECT0	0x42401200	Clock Path Select Register
CLK_PATH_SELECT1	0x42401204	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT2	0x42401208	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT3	0x4240120C	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT4	0x42401210	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT5	0x42401214	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT0	0x42401240	Clock Root Select Register
CLK_ROOT_SELECT1	0x42401244	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT2	0x42401248	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT3	0x4240124C	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT4	0x42401250	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT5	0x42401254	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT6	0x42401258	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT7	0x4240125C	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT8	0x42401260	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT9	0x42401264	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT10	0x42401268	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT11	0x4240126C	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.

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Register name	Address	Description
CLK_ROOT_SELECT12	0x42401270	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT13	0x42401274	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT0	0x42401280	Clock Root Direct Select Register
CLK_DIRECT_SELECT1	0x42401284	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT2	0x42401288	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT3	0x4240128C	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT4	0x42401290	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT5	0x42401294	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT6	0x42401298	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT7	0x4240129C	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT8	0x424012A0	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT9	0x424012A4	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT10	0x424012A8	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT11	0x424012AC	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT12	0x424012B0	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT13	0x424012B4	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_SELECT	0x42401300	Clock selection register
CLK_MF_SELECT	0x42401304	Medium Frequency Clock Select Register
CLK_ECO_PRESCALE	0x42401320	ECO Prescaler Configuration Register
CLK_IHO_CONFIG	0x42401344	IHO Configuration Register
CLK_ECO_CONFIG	0x42401360	ECO Configuration Register
CLK_ECO_CONFIG2	0x42401364	ECO Configuration Register 2
CLK_ECO_STATUS	0x42401368	ECO Status Register
CLK_PILO_CONFIG	0x42401370	Precision ILO Configuration Register
CLK_PILO_STATUS	0x42401374	Precision ILO Status Register
CLK_WCO_CONFIG	0x42401390	WCO Configuration Register
CLK_WCO_STATUS	0x42401394	WCO Status Register

System Resources Subsystem (SRSS) registers

Register name	Address	Description
CSV_HF_CSV0_REF_CTL	0x42401400	Clock Supervision Reference Control
CSV_HF_CSV0_REF_LIMIT	0x42401404	Clock Supervision Reference Limits
CSV_HF_CSV0_MON_CTL	0x42401408	Clock Supervision Monitor Control
CSV_HF_CSV1_REF_CTL	0x42401410	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV1_REF_LIMIT	0x42401414	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV1_MON_CTL	0x42401418	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV2_REF_CTL	0x42401420	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV2_REF_LIMIT	0x42401424	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV2_MON_CTL	0x42401428	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV3_REF_CTL	0x42401430	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV3_REF_LIMIT	0x42401434	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV3_MON_CTL	0x42401438	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV4_REF_CTL	0x42401440	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV4_REF_LIMIT	0x42401444	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV4_MON_CTL	0x42401448	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV5_REF_CTL	0x42401450	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV5_REF_LIMIT	0x42401454	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV5_MON_CTL	0x42401458	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV6_REF_CTL	0x42401460	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV6_REF_LIMIT	0x42401464	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV6_MON_CTL	0x42401468	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV7_REF_CTL	0x42401470	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV7_REF_LIMIT	0x42401474	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.

Register name	Address	Description
CSV_HF_CSV7_MON_CTL	0x42401478	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV8_REF_CTL	0x42401480	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV8_REF_LIMIT	0x42401484	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV8_MON_CTL	0x42401488	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV9_REF_CTL	0x42401490	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV9_REF_LIMIT	0x42401494	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV9_MON_CTL	0x42401498	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV10_REF_CTL	0x424014A0	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV10_REF_LIMIT	0x424014A4	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV10_MON_CTL	0x424014A8	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV11_REF_CTL	0x424014B0	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV11_REF_LIMIT	0x424014B4	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV11_MON_CTL	0x424014B8	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV12_REF_CTL	0x424014C0	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV12_REF_LIMIT	0x424014C4	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV12_MON_CTL	0x424014C8	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV13_REF_CTL	0x424014D0	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV13_REF_LIMIT	0x424014D4	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV13_MON_CTL	0x424014D8	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_REF_SEL	0x42401500	Select CSV Reference clock for Active domain
CSV_REF_CSV_REF_CTL	0x42401510	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_REF_CSV_REF_LIMIT	0x42401514	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.

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Register name	Address	Description
CSV_REF_CSV_MON_CTL	0x42401518	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_LF_REF_SEL	0x42401520	Select CSV Reference clock for LF clock
CSV_LF_CSV_REF_CTL	0x42401530	Clock Supervision Reference Control
CSV_LF_CSV_REF_LIMIT	0x42401534	Clock Supervision Reference Limits
CSV_LF_CSV_MON_CTL	0x42401538	Clock Supervision Monitor Control
CLK_DPLL_LP0_CONFIG	0x42401600	DPLL_LP Configuration Register
CLK_DPLL_LP0_CONFIG2	0x42401604	DPLL_LP Configuration Register 2
CLK_DPLL_LP0_CONFIG3	0x42401608	DPLL_LP Configuration Register 3
CLK_DPLL_LP0_CONFIG4	0x4240160C	DPLL_LP Configuration Register 4
CLK_DPLL_LP0_CONFIG5	0x42401610	DPLL_LP Configuration Register 5
CLK_DPLL_LP0_STATUS	0x42401614	DPLL_LP Status Register
CLK_DPLL_LP1_CONFIG	0x42401620	DPLL_LP Configuration Register. See CLK_DPLL_LP0_CONFIG for the details of bit fields.
CLK_DPLL_LP1_CONFIG2	0x42401624	DPLL_LP Configuration Register 2. See CLK_DPLL_LP0_CONFIG2 for the details of bit fields.
CLK_DPLL_LP1_CONFIG3	0x42401628	DPLL_LP Configuration Register 3. See CLK_DPLL_LP0_CONFIG3 for the details of bit fields.
CLK_DPLL_LP1_CONFIG4	0x4240162C	DPLL_LP Configuration Register 4. See CLK_DPLL_LP0_CONFIG4 for the details of bit fields.
CLK_DPLL_LP1_CONFIG5	0x42401630	DPLL_LP Configuration Register 5. See CLK_DPLL_LP0_CONFIG5 for the details of bit fields.
CLK_DPLL_LP1_STATUS	0x42401634	DPLL_LP Status Register. See CLK_DPLL_LP0_STATUS for the details of bit fields.
CLK_DPLL_HP0_CONFIG	0x42401800	DPLL_HP Configuration Register
CLK_DPLL_HP0_CONFIG2	0x42401804	DPLL_HP Configuration Register 2
CLK_DPLL_HP0_CONFIG3	0x42401808	DPLL_HP Configuration Register 3
CLK_DPLL_HP0_CONFIG4	0x4240180C	DPLL_HP Configuration Register 4
CLK_DPLL_HP0_CONFIG5	0x42401810	DPLL_HP Configuration Register 5
CLK_DPLL_HP0_TRIGMOD	0x42401814	DPLL_HP Trigmod SSCG Register
CLK_DPLL_HP0_TRIGMOD2	0x42401818	DPLL_HP Trigmod2 SSCG Register
CLK_DPLL_HP0_STATUS	0x4240181C	DPLL_HP Status Register
CLK_DPLL_HP0_DUTYCAL_CTRL	0x42401820	DPLL_HP_User DUTYCAL Control Register
RES_CAUSE	0x42401BD0	Reset Cause Observation Register
RES_CAUSE2	0x42401BD4	Reset Cause Observation Register 2
RES_PXRES_CTL	0x42401BE4	Programmable XRES Control Register
RES_CAUSE_EXTEND	0x42401C04	Extended Reset Cause Observation Register
PWR_CBUCK_CTL	0x42401C10	Core Buck Control Register
PWR_CBUCK_CTL2	0x42401C14	Core Buck Control Register 2
PWR_CBUCK_DPSLP_CTL	0x42401C1C	Core Buck Deepsleep Control Register

System Resources Subsystem (SRSS) registers

Register name	Address	Description
PWR_CBUCK_STATUS	0x42401C20	Core Buck Status Register
PWR_RETLDO_CTL	0x42401C24	RETLDO Control Register
PWR_SRAMLDO_CTL	0x42401C28	SRAMLDO Control Register
PWR_MISCLDO_CTL	0x42401C30	MISCLDO Control Register
DECODED_LCS_DATA	0x42401D00	Decoded Life Cycle Stage Data Register
PWR_TRIM_PMU_CTL0	0x42402110	PMU Trim Register 0
CLK_TRIM_ECO_CTL	0x42403020	ECO Trim Register
RAM_TRIM_TRIM_RAM_CTL0	0x42404000	Trim Register for RAM Type 0
RAM_TRIM_TRIM_RAM_CTL1	0x42404004	Trim Register for RAM Type 0. See RAM_TRIM_TRIM_RAM_CTL0 for the details of bit fields.
RAM_TRIM_TRIM_RAM_CTL2	0x42404008	Trim Register for RAM Type 0
RAM_TRIM_TRIM_RAM_CTL3	0x4240400C	Trim Register for RAM Type 0. See RAM_TRIM_TRIM_RAM_CTL2 for the details of bit fields.
RAM_TRIM_TRIM_RAM_CTL4	0x42404010	Trim Register for RAM Type 0. See RAM_TRIM_TRIM_RAM_CTL2 for the details of bit fields.
RAM_TRIM_TRIM_RAM_CTL5	0x42404014	Trim Register for RAM Type 0. See RAM_TRIM_TRIM_RAM_CTL2 for the details of bit fields.
RAM_TRIM_TRIM_RAM_CTL6	0x42404018	Trim Register for RAM Type 0
RAM_TRIM_TRIM_RAM_CTL7	0x4240401C	Trim Register for RAM Type 0. See RAM_TRIM_TRIM_RAM_CTL6 for the details of bit fields.
RAM_TRIM_TRIM_RAM_CTL8	0x42404020	Trim Register for RAM Type 0
WDT_CTL	0x4240C000	Watchdog Counter Control Register (Type A)
WDT_CNT	0x4240C004	Watchdog Counter Count Register (Type A)
WDT_MATCH	0x4240C008	Watchdog Counter Match Register (Type A)
WDT_MATCH2	0x4240C00C	Watchdog Counter Match Register 2 (Type A)
MCWDT_CNTLOW0	0x4240D004	Multi-Counter Watchdog Sub-counters 0/1
MCWDT_CNTHIGH0	0x4240D008	Multi-Counter Watchdog Sub-counter 2
MCWDT_MATCH0	0x4240D00C	Multi-Counter Watchdog Counter Match Register
MCWDT_CONFIG0	0x4240D010	Multi-Counter Watchdog Counter Configuration
MCWDT_CTL0	0x4240D014	Multi-Counter Watchdog Counter Control
MCWDT_INTR0	0x4240D018	Multi-Counter Watchdog Counter Interrupt Register
MCWDT_INTR_SET0	0x4240D01C	Multi-Counter Watchdog Counter Interrupt Set Register
MCWDT_INTR_MASK0	0x4240D020	Multi-Counter Watchdog Counter Interrupt Mask Register
MCWDT_INTR_MASKED0	0x4240D024	Multi-Counter Watchdog Counter Interrupt Masked Register
MCWDT_LOCK0	0x4240D028	Multi-Counter Watchdog Counter Lock Register
MCWDT_LOWER_LIMIT0	0x4240D02C	Multi-Counter Watchdog Counter Lower Limit Register
PERI_PCLK1_GR1_DIV_CMD	0x4240D044	Multi-Counter Watchdog Sub-counters 0/1. See MCWDT_CNTLOW0 for the details of bit fields.
PERI_PCLK1_GR1_CLOCK_CTL0	0x4240D048	Multi-Counter Watchdog Sub-counter 2. See MCWDT_CNTHIGH0 for the details of bit fields.

Register name	Address	Description
MCWDT_MATCH1	0x4240D04C	Multi-Counter Watchdog Counter Match Register. See MCWDT_MATCH0 for the details of bit fields.
MCWDT_CONFIG1	0x4240D050	Multi-Counter Watchdog Counter Configuration. See MCWDT_CONFIG0 for the details of bit fields.
MCWDT_CTL1	0x4240D054	Multi-Counter Watchdog Counter Control. See MCWDT_CTL0 for the details of bit fields.
MCWDT_INTR1	0x4240D058	Multi-Counter Watchdog Counter Interrupt Register. See MCWDT_INTR0 for the details of bit fields.
MCWDT_INTR_SET1	0x4240D05C	Multi-Counter Watchdog Counter Interrupt Set Register. See MCWDT_INTR_SET0 for the details of bit fields.
MCWDT_INTR_MASK1	0x4240D060	Multi-Counter Watchdog Counter Interrupt Mask Register. See MCWDT_INTR_MASK0 for the details of bit fields.
MCWDT_INTR_MASKED1	0x4240D064	Multi-Counter Watchdog Counter Interrupt Masked Register. See MCWDT_INTR_MASKED0 for the details of bit fields.
MCWDT_LOCK1	0x4240D068	Multi-Counter Watchdog Counter Lock Register. See MCWDT_LOCK0 for the details of bit fields.
MCWDT_LOWER_LIMIT1	0x4240D06C	Multi-Counter Watchdog Counter Lower Limit Register. See MCWDT_LOWER_LIMIT0 for the details of bit fields.
PERI_PCLK1_GR1_DIV_CMD	0x44042000	Divider command
PERI_PCLK1_GR1_CLOCK_CTL0	0x44042C00	Clock control
PERI_PCLK1_GR1_CLOCK_CTL1	0x44042C04	Clock control. See PERI_PCLK1_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK1_GR1_CLOCK_CTL2	0x44042C08	Clock control. See PERI_PCLK1_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK1_GR1_DIV_16_5_CTL0	0x44043800	Divider control (for 16.5 divider)
PERI_PCLK1_GR1_DIV_16_5_CTL1	0x44043804	Divider control (for 16.5 divider). See PERI_PCLK1_GR1_DIV_16_5_CTL0 for the details of bit fields.
PERI_PCLK1_GR1_DIV_16_5_CTL2	0x44043808	Divider control (for 16.5 divider). See PERI_PCLK1_GR1_DIV_16_5_CTL0 for the details of bit fields.
PERI_PCLK1_GR2_DIV_CMD	0x44044000	Divider command. See PERI_PCLK1_GR1_DIV_CMD for the details of bit fields.
PERI_PCLK1_GR2_CLOCK_CTL0	0x44044C00	Clock control
PERI_PCLK1_GR2_DIV_8_CTL0	0x44045000	Divider control (for 8.0 divider)
PERI_PCLK1_GR3_DIV_CMD	0x44046000	Divider command. See PERI_PCLK1_GR1_DIV_CMD for the details of bit fields.
PERI_PCLK1_GR3_CLOCK_CTL0	0x44046C00	Clock control. See PERI_PCLK1_GR2_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK1_GR3_DIV_8_CTL0	0x44047000	Divider control (for 8.0 divider). See PERI_PCLK1_GR2_DIV_8_CTL0 for the details of bit fields.

14.1.1 CLK_DSI_SELECT0

Description: Clock DSI Select Register

Address: 0x42400100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			DSI_MUX [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	DSI_MUX	Selects a DSI source or low frequency clock for use in a clock path. The output of this mux can be selected for clock PATH *using CLK_SELECT_PATH register. Using the output of this mux as HFCLK source will result in undefined behavior. It can be used to clocks to DSI or as reference inputs for the FLL/PLL, subject to the frequency limits of those circuits. This mux is not glitch free, so do not change the selection while it is an actively selected clock. Default Value: 0* **0x0: DSI_OUT0 :** DSI0 - dsi_out[0] **0x1: DSI_OUT1 :** DSI1 - dsi_out[1] **0x2: DSI_OUT2 :** DSI2 - dsi_out[2] **0x3: DSI_OUT3 :** DSI3 - dsi_out[3] **0x4: DSI_OUT4 :** DSI4 - dsi_out[4]

14.1.1 CLK_DSI_SELECT0 (continued)

0x5: DSI_OUT5 :

DSI5 - dsi_out[5]

0x6: DSI_OUT6 :

DSI6 - dsi_out[6]

0x7: DSI_OUT7 :

DSI7 - dsi_out[7]

0x8: DSI_OUT8 :

DSI8 - dsi_out[8]

0x9: DSI_OUT9 :

DSI9 - dsi_out[9]

0xa: DSI_OUT10 :

DSI10 - dsi_out[10]

0xb: DSI_OUT11 :

DSI11 - dsi_out[11]

0xc: DSI_OUT12 :

DSI12 - dsi_out[12]

0xd: DSI_OUT13 :

DSI13 - dsi_out[13]

0xe: DSI_OUT14 :

DSI14 - dsi_out[14]

0xf: DSI_OUT15 :

DSI15 - dsi_out[15]

0x10: ILO :

ILO - Internal Low-speed Oscillator #0

0x11: WCO :

WCO - Watch-Crystal Oscillator

0x12: ALTLF :

ALTLF - Alternate Low-Frequency Clock

14.1.1 CLK_DSI_SELECT0 (continued)

0x13: PILO :

PILO - Precision Internal Low-speed Oscillator

14.1.2 CLK_OUTPUT_FAST

Description: Fast Clock Output Select Register

Address: 0x42400140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PATH_SEL0 [7:4]				FAST_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				HFCLK_SEL0 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	PATH_SEL1 [23:20]				FAST_SEL1 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				HFCLK_SEL1 [27:24]			

Bits	Name	Description
27 : 24	HFCLK_SEL1	Selects a HFCLK tree for use in fast clock output #1 logic Default Value: 0
23 : 20	PATH_SEL1	Selects a clock path to use in fast clock output #1 logic. Default Value: 0
19 : 16	FAST_SEL1	Select signal for fast clock output #1 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL1 and HFCLK_SEL1. **0x1: HFSRC_0 :** IHO - Internal High-speed Oscillator **0x2: HFSRC_1 :** EXTCLK - External Clock Pin **0x3: HFSRC_2 :** ECO - External-Crystal Oscillator (Product Specific)

14.1.2 CLK_OUTPUT_FAST (continued)

0x4: HFSRC_3 :

IMO - Internal R/C Oscillator (Product Specific)

0x5: HFSRC_4 :

ALTHF0 - Alternate High-Frequency clock input (product-specific clock)

0x6: HFSRC_5 :

ALTHF1 - Alternate High-Frequency clock input (product-specific clock)

0x7: HFSRC_6 :

Reserved

0x8: TIMERCLK :

Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse.

0x9: PATH_SEL1 :

Selects the clock path chosen by PATH_SEL1 field

0xa: HFCLK_SEL1 :

Selects the output of the HFCLK_SEL1 mux

0xb: SLOW_SEL1 :

Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL1

0xc: PWR :

clk_pwr: used for PPU and related components

11 : 8	HFCLK_SEL0	Selects a HFCLK tree for use in fast clock output #0 Default Value: 0
7 : 4	PATH_SEL0	Selects a clock path to use in fast clock output #0 logic. Default Value: 0
3 : 0	FAST_SEL0	Select signal for fast clock output #0 Default Value: 0

0x0: NC :

Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL0 and HFCLK_SEL0.

0x1: HFSRC_0 :

IHO - Internal High-speed Oscillator

0x2: HFSRC_1 :

EXTCLK - External Clock Pin

14.1.2 CLK_OUTPUT_FAST (continued)

0x3: HFSRC_2 :

ECO - External-Crystal Oscillator (Product Specific)

0x4: HFSRC_3 :

IMO - Internal R/C Oscillator (Product Specific)

0x5: HFSRC_4 :

ALTHF0 - Alternate High-Frequency clock input (product-specific clock)

0x6: HFSRC_5 :

ALTHF1 - Alternate High-Frequency clock input (product-specific clock)

0x7: HFSRC_6 :

Reserved

0x8: TIMERCLK :

Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse.

0x9: PATH_SEL0 :

Selects the clock path chosen by PATH_SEL0 field

0xa: HFCLK_SEL0 :

Selects the output of the HFCLK_SEL0 mux

0xb: SLOW_SEL0 :

Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL0

0xc: PWR :

clk_pwr: used for PPU and related components

14.1.3 CLK_OUTPUT_SLOW

Description: Slow Clock Output Select Register

Address: 0x42400144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SLOW_SEL1 [7:4]				SLOW_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	SLOW_SEL1	Select signal for slow clock output #1 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes. **0x1: ILO :** Internal Low Speed Oscillator (ILO) **0x2: WCO :** Watch-Crystal Oscillator (WCO) **0x3: CLK_RTC :** Root of the RTC clock tree **0x4: ALTLF :** Alternate low-frequency clock input to SRSS (ALTLF)

14.1.3 CLK_OUTPUT_SLOW (continued)

0x5: LFCLK :

Root of the low-speed clock tree (LFCLK)

0x6: IMO :

Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x7: SLPCTRL :

Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x8: PILO :

Precision Internal Low Speed Oscillator (PILO)

0x9: ECO_PRESCALER :

ECO Prescaler (ECO_PRESCALER)

0xa: MF :

Medium Frequency clock tree (MF)

0xb: Reserved1 :

Reserved

0xc: Reserved2 :

Reserved

0xd: Reserved3 :

Reserved

3 : 0	SLOW_SEL0	Select signal for slow clock output #0 Default Value: 0

0x0: NC :

Disabled - output is 0. For power savings, clocks are blocked before entering any muxes.

0x1: ILO :

Internal Low Speed Oscillator (ILO)

0x2: WCO :

Watch-Crystal Oscillator (WCO)

0x3: CLK_RTC :

Root of the RTC clock tree

14.1.3 CLK_OUTPUT_SLOW (continued)

0x4: ALTLF :

Alternate low-frequency clock input to SRSS (ALTLF)

0x5: LFCLK :

Root of the low-speed clock tree (LFCLK)

0x6: IMO :

Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x7: SLPCTRL :

Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x8: PILO :

Precision Internal Low Speed Oscillator (PILO)

0x9: ECO_PRESCALER :

ECO Prescaler (ECO_PRESCALER)

0xa: MF :

Medium Frequency clock tree (MF)

0xb: Reserved1 :

Reserved

0xc: Reserved2 :

Reserved

0xd: Reserved3 :

Reserved

14.1.4 CLK_CAL_CNT1

Description: Clock Calibration Counter 1

Address: 0x42400148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	RW	Reserved				
HW Access	W	W	R	Reserved				
Name	CAL_COUNTER_DONE	CAL_CLK1_PRESENT	CAL_RESET	Reserved [28:24]				

Bits	Name	Description
31	CAL_COUNTER_DONE	Status bit indicating that the internal counter #1 is finished counting and CLK_CAL_CNT2.COUNTER stopped counting up Default Value: 1
30	CAL_CLK1_PRESENT	Status bit indicating that a posedge was detected by counter #1 (does not apply when CLK_CAL_TEST.CAL_WINDOW_SEL = 1). If this bit never asserts, there is no clock on counter #1 and CAL_COUNTER_DONE will stay low indefinitely. This can be recovered with CAL_RESET. Default Value: 0
29	CAL_RESET	Reset clock calibration logic for window mode. This can be used to recover from unexpected conditions, such as no clock present on counter #1. When entering window mode, set this bit, then set CLK_CAL_TEST.CAL_WINDOW_SEL=1, then clear this bit. It takes 3 clock cycles for this reset to propagate. A new calibration cannot start during this time. Default Value: 0
23 : 0	CAL_COUNTER1	Down-counter clocked on fast clock output #0 (see CLK_OUTPUT_FAST). This register always reads as zero. Counting starts internally when this register is written with a nonzero value. CAL_COUNTER_DONE goes immediately low to indicate that the counter has started and will be asserted when the counters are done. Do not write this field unless CAL_COUNTER_DONE==1. Both clocks must be running or the measurement will not complete, and this case can be recovered using CAL_RESET. Default Value: 0

14.1.5 CLK_CAL_CNT2

Description: Clock Calibration Counter 2

Address: 0x4240014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 0	CAL_COUNTER2	Up-counter clocked on fast clock output #1 (see CLK_OUTPUT_FAST). When CLK_-CAL_CNT1.CAL_COUNTER_DONE==1, the counter is stopped and can be read by SW. Do not read this value unless CAL_COUNTER_DONE==1. The expected final value is related to the ratio of clock frequencies used for the two counters and the value loaded into counter 1: CLK_-CAL_CNT2.COUNTER=(F_cnt2/F_cnt1)*(CLK_CAL_CNT1.COUNTER) Default Value: 0

14.1.6 SRSS_INTR

Description: SRSS Interrupt Register

Address: 0x42400200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW1C	Reserved				RW1C
HW Access	Reserved		A	Reserved				A
Name	Reserved [7:6]		CLK_CAL	Reserved [4:1]				WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [15:9]							CSV_LF

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	AINTR	Reserved [30:24]						

Bits	Name	Description
31	AINTR	See additional interrupts in SRSS_AINTR. Default Value: 0
8	CSV_LF	CSV_LF Interrupt Request. This bit is set when LFCLK is below or above the expected limit Default Value: 0
5	CLK_CAL	Clock calibration counter is done. This field is reset during DEEPSLEEP mode. Default Value: 0
0	WDT_MATCH	WDT Interrupt Request. This bit is set each time WDT_COUNTR==WDT_MATCH. W1C also feeds the watch dog. Missing 2 interrupts in a row will generate a reset. Due to internal synchronization, it takes 2 SYSCLK cycles to update after a W1C. Default Value: 0

14.1.7 SRSS_INTR_SET

Description: SRSS Interrupt Set Register

Address: 0x42400204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW1S	Reserved				RW1S
HW Access	Reserved		A	Reserved				A
Name	Reserved [7:6]		CLK_CAL	Reserved [4:1]				WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							CSV_LF

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	CSV_LF	Set interrupt for CSV_LF Default Value: 0
5	CLK_CAL	Set interrupt for clock calibration counter done. This field is reset during DEEPSLEEP mode. Default Value: 0
0	WDT_MATCH	Set interrupt for low voltage detector WDT_MATCH Default Value: 0

14.1.8 SRSS_INTR_MASK

Description: SRSS Interrupt Mask Register

Address: 0x42400208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	Reserved				RW
HW Access	Reserved		R	Reserved				R
Name	Reserved [7:6]		CLK_CAL	Reserved [4:1]				WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							CSV_LF

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	CSV_LF	Mask for interrupt for CSV_LF Default Value: 0
5	CLK_CAL	Mask for clock calibration done Default Value: 0
0	WDT_MATCH	Mask for watchdog timer. Clearing this bit will not forward the interrupt to the CPU. It will not, however, disable the WDT reset generation on 2 missed interrupts. When WDT resets the chip, it also internally pends an interrupt that survives the reset. To prevent unintended ISR execution, clear SRSS_INTR.WDT_MATCH before setting this bit. Default Value: 0

14.1.9 SRSS_INTR_MASKED

Description: SRSS Interrupt Masked Register

Address: 0x4240020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R	Reserved				R
HW Access	Reserved		RW	Reserved				RW
Name	Reserved [7:6]		CLK_CAL	Reserved [4:1]				WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [15:9]							CSV_LF

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	AINTR	Reserved [30:24]						

Bits	Name	Description
31	AINTR	See additional MASKED bits in SRSS_AINTR_MASKED.ADDITIONAL Default Value: 0
8	CSV_LF	Logical and of corresponding request and mask bits. Default Value: 0
5	CLK_CAL	Logical and of corresponding request and mask bits. Default Value: 0
0	WDT_MATCH	Logical and of corresponding request and mask bits. Default Value: 0

14.1.10 SRSS_AINTR

Description: SRSS Additional Interrupt Register

Address: 0x42400300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1C	RW1C
HW Access	Reserved						A	A
Name	Reserved [7:2]						HVLVD	OVDVCCD

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	HVLVD	Interrupt for low voltage detector HVLVD Default Value: 0
0	OVDVCCD	Interrupt for low voltage detector OVDVCCD. The OVD status should be cleared in PWR_SSV_STATUS before clearing this interrupt. Default Value: 0

14.1.11 SRSS_AINTR_SET

Description: SRSS Additional Interrupt Set Register

Address: 0x42400304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1S	RW1S
HW Access	Reserved						A	A
Name	Reserved [7:2]						HVLVD	OVDVCCD

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	HVLVD	Set interrupt for low voltage detector HVLVD. Note that the PWR_LVD_CTL.HVLVD_ACTION must be set to Interrupt for this SET functionality to work. Default Value: 0
0	OVDVCCD	Set interrupt for low voltage detector OVDVCCD. Note that the PWR_OVD_CTL.OVDVC-CD_ACTION must be set to Interrupt for this SET functionality to work. Default Value: 0

14.1.12 SRSS_AINTR_MASK

Description: SRSS Additional Interrupt Mask Register

Address: 0x42400308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						HVLVD	OVDVCCD

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	HVLVD	Mask for low voltage detector HVLVD Default Value: 0
0	OVDVCCD	Mask for low voltage detector OVDVCCD Default Value: 0

14.1.13 SRSS_AINTR_MASKED

Description: SRSS Additional Interrupt Masked Register

Address: 0x4240030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						RW	RW
Name	Reserved [7:2]						HVLVD	OVDVCCD

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	HVLVD	Logical and of corresponding request and mask bits. Default Value: 0
0	OVDVCCD	Logical and of corresponding request and mask bits. Default Value: 0

14.1.14 PWR_LVD_STATUS

Description: High Voltage / Low Voltage Detector (HVLVD) Status Register

Address: 0x42400340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							HVLVD_OK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	HVLVD_OK	HVLVD output. 0: below voltage threshold 1: above voltage threshold Default Value: 0

14.1.15 BOOT_DLM_CTL

Description: Debug Control Register

Address: 0x42400404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				A			
Name	Reserved [7:4]				REQUEST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	Reserved				
HW Access	A	A	A	Reserved				
Name	WFA	RESET	IN-PUT_AVAIL	Reserved [28:24]				

Bits	Name	Description
31	WFA	Wait for Action. Set by BootROM when it waits for application or debug certificate to be loaded into the RAM. The bit must be cleared to continue BootROM operation. It is used by the Sys-AP. Default Value: 0
30	RESET	Request the device reset after RAM application complete input parameters processing. This bit is analyzed with APP_INPUT_AVAIL so to take effect write both. 0 - No action, the device waits for input parameters. 1 - Reset the device after input parameters processing complete. Default Value: 0
29	INPUT_AVAIL	Notify RAM application that input parameters are valid for processing: 0 - the input parameters are not available. 1 - the input parameters are available (ready) for processing. Default Value: 0

14.1.15 BOOT_DLM_CTL (continued)

3 : 0	REQUEST	Set by Sys-AP or the user application to request BootROM for to execute the request after software reset (this encoding assumes singe request). This field survives some resets, including a system reset: 0x0: There is no request to BootROM (default value). The BootROM follows regular boot flow. 0x1: BootROM set DEBUG_WFA and waits for RAM application and input parameters (optional) in system RAM. After DEBUG_WFA is cleared the BootROM validate RAM application. If validation completed successfully BootROM launches RAM application, otherwise BootROM reports error in TST_DEBUG_STATUS register and continue boot. 0x2: BootROM set DEBUG_WFA and and waits for debug certificate in system RAM. After DEBUG_WFA is cleared the BootROM validates debug certificate. If validation completed successfully BootROM applies AP_CLT setting from certificate, otherwise BootROM reports error in TST_DEBUG_STATUS register. The boot continue independently from certificate validation result. 0x3: BootROM copies RAM application from the staging area and validates it. If validation completed successfully BootROM launches RAM application, otherwise BootROM reports error in TST_DEBUG_STATUS register and continue boot. 0x4: BootROM copies debug certificate from the staging area and validates it. If validation completed successfully BootROM applies AP_CLT setting from certificate, otherwise BootROM reports error in TST_DEBUG_STATUS register. The boot continue independently from certificate validation status. 0x5: Reserved (keep BWC with cyw208289). There is support for opening RAM application debug in PC=0 using certificate. 0x6: Request to higher level firmware (launched upon BootROM completion) to stage RAM application into the staging area. This request is ignored by the BootROM. Others reserved for future use. If set BootROM reports error. Default Value: 0

14.1.16 BOOT_DLM_CTL2

Description: Debug Control Register 2

Address: 0x42400408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	APP_CTL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	APP_CTL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	APP_CTL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	APP_CTL [31:24]							

Bits	Name	Description
31 : 0	APP_CTL	Address of application descriptor or debug certificate depends on DEBUG_TST_CTL.REQUEST. The application descriptor provides info about RAM application and its parameters layout in the staging area to BootROM and RAM application itself Default Value: 0

14.1.17 BOOT_DLM_STATUS

Description: Debug Status Register

Address: 0x4240040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [31:24]							

Bits	Name	Description
31 : 0	DEBUG_STATUS	RAM application execution status or debug certificate validation status depends on DEBUG_TST_CTL.REQUEST. This status can be read by the debugger using Sys-AP or user application when RAM application completes with system reset. This field survives some resets, including a system reset Default Value: 0

14.1.18 RES_SOFT_CTL

Description: Soft Reset Trigger Register

Address: 0x42400410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							R
Name	Reserved [7:1]							TRIGGER_-SOFT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	TRIGGER_SOFT	Triggers a soft reset. The reset clears this bit. Default Value: 0

14.1.19 BOOT_STATUS

Description: Boot Execution Status Register

Address: 0x42400418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [31:24]							

Bits	Name	Description
31 : 0	DEBUG_STATUS	Boot execution status. This status register can be used for communication between ROM_BOOT and User Application. This status can be read by the debugger using Sys-AP or User Application. This field survives some resets, including a system reset. It specifies if the Boot SW launched next application successfully. Following are the BOOT status codes: - Boot Success status: 0x0D50B002 - OEM Policy HASH Invalid : 0xBAF0002B - DLM Package Invalid : 0xBAF00073 - Debug Token Valid : 0x0D500081 - Debug Token Invalid : 0xBAF00082 - Debug Policy Invalid : 0xBAF00083 - OEM Policy Invalid : 0xBAF00085 - Extended Boot Image Invalid : 0xBAF00090 - BASE_RT_SERVICE Invalid : 0xBAF00091 - SE_RT_SERVICE Invalid : 0xBAF00092 Default Value: 0

14.1.20 BOOT_ENTRY

Description: Warm Boot Entry Address

Address: 0x42400430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WARM_BOOT_ENTRY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WARM_BOOT_ENTRY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WARM_BOOT_ENTRY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WARM_BOOT_ENTRY [31:24]							

Bits	Name	Description
31 : 0	WARM_BOOT_ENTRY	Warm boot entry point. This status register can be used for communication between 2 software application before/after DS-RAM or soft reset. This field survives low voltage resets, including a system reset. Default Value: 0

14.1.21 DECODED_LCS_DATA

Description: Decoded Life Cycle Stage Data Register

Address: 0x42400440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	RW		RW		RW		RW	
Name	N_CODE [7:6]		S_CODE [5:4]		P_CODE [3:2]		K_CODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R		R	
HW Access	Reserved				RW		RW	
Name	Reserved [15:12]				B_CODE [11:10]		R_CODE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11 : 10	B_CODE	Indicates status of LCS "B" bit. 00=Unprogrammed, 11=Valid, 10/01=Invalid Default Value: 2
9 : 8	R_CODE	Indicates status of LCS "R" bit. 00=Unprogrammed, 11=Valid, 10/01=Invalid Default Value: 2
7 : 6	N_CODE	Indicates status of LCS "N" bit*. 00=Unprogrammed, 11=Valid, 10/01=Invalid. Will be '00' if R_CODE is set in RMA LCS Default Value: 2
5 : 4	S_CODE	Indicates status of LCS "S" bit*. 00=Unprogrammed, 11=Valid, 10/01=Invalid. Will be '11' if R_CODE is set in RMA LCS Default Value: 2
3 : 2	P_CODE	Indicates status of LCS "P" bit*. 00=Unprogrammed, 11=Valid, 10/01=Invalid. Will be '11' if R_CODE is set in RMA LCS Default Value: 2
1 : 0	K_CODE	Indicates status of LCS "K" bit. 00=Unprogrammed, 11=Valid, 10/01=Invalid Default Value: 2

14.1.22 PWR_HIB_WAKE_CTL

Description: Hibernate Wakeup Mask Register

Address: 0x424008A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				A			
Name	Reserved [7:4]				HIB_WAKE_SRC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved					
HW Access	A	A	Reserved					
Name	HIB_WAKE_WDT	HIB_WAKE_RTC	Reserved [29:24]					

Bits	Name	Description
31	HIB_WAKE_WDT	When set, HIBERNATE will wakeup for a pending WDT interrupt. Default Value: 0
30	HIB_WAKE_RTC	When set, HIBERNATE will wakeup for a pending RTC interrupt. Default Value: 0
3 : 0	HIB_WAKE_SRC	When set, HIBERNATE will wakeup for the assigned source The number and assignment of HIBERNATE wakeup sources are product-specific. Default Value: 0

14.1.23 PWR_HIB_WAKE_CTL2

Description: Hibernate Wakeup Polarity Register

Address: 0x424008A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				A			
Name	Reserved [7:4]				HIB_WAKE_SRC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	HIB_WAKE_SRC	Each bit selects the polarity for the corresponding HIBERNATE wakeup source. The number and assignment of wakeup sources are product-specific. 0: Wakes when unmasked input is 0. 1: Wakes when unmasked input is 1. Default Value: 0

14.1.24 PWR_HIB_WAKE_CAUSE

Description: Hibernate Wakeup Cause Register

Address: 0x424008AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1C			
HW Access	Reserved				A			
Name	Reserved [7:4]				HIB_WAKE_SRC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	RW1C	Reserved					
HW Access	A	A	Reserved					
Name	HIB_WAKE_WDT	HIB_WAKE_RTC	Reserved [29:24]					

Bits	Name	Description
31	HIB_WAKE_WDT	Indicates WDT wakeup cause. The WDT interrupt must be cleared before this bit can be cleared. Default Value: 0
30	HIB_WAKE_RTC	Indicates RTC wakeup cause. The RTC interrupt must be cleared before this bit can be cleared. Default Value: 0
3 : 0	HIB_WAKE_SRC	Each bit indicates a HIBERNATE wakeup cause. The number and assigment of wakeup sources are product-specific. For each bit, writing a 1 clears the cause flag. Default Value: 0

14.1.25 TST_XRES_SECURE

Description: SECURE TEST and FIRMWARE TEST Key control register

Address: 0x42400914

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				FW_WR [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				SECURE_WR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	R	R	Reserved				
HW Access	R	RW	RW	Reserved				
Name	SECURE_-DISABLE	SE-CURE_KEY_OK	FW_KEY_OK	Reserved [28:24]				

Bits	Name	Description
31	SECURE_DISABLE	Disables the SECURE TEST key entry capability until next reset. Must not be set in the same write when any of the above *_WR bits are set or toggling. Default Value: 0
30	SECURE_KEY_OK	Indicates that the 32-bit SECURE TEST key is observing the correct key. Secure key is not reset, but it will establish low after a deep power cycle that causes it to lose its written state. Default Value: 0
29	FW_KEY_OK	Indicates that the 32-bit FIRMWARE TEST key is observing the correct key. Firmware key is re-set by (A)XRES and STRUCT_XRES. Default Value: 0
19 : 16	SECURE_WR	Latch enables for each of the 4 bytes in the 32-bit SECURE TEST key. Must be toggled high and then low while keeping DATA8 to the correct value. Default Value: 0
11 : 8	FW_WR	Latch enables for each of the 4 bytes in the 32-bit FIRMWARE TEST key. Must be toggled high and then low while keeping DATA8 to the correct value. Default Value: 0
7 : 0	DATA8	Data byte to be set into either SECURE TEST or FIRMWARE TEST key. Must not be changed in the same write that is toggling any of the *_WR bits below, Default Value: 0

14.1.26 PWR_CTL

Description: Power Mode Control

Address: 0x42401000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R	R	Reserved			
HW Access	Reserved		RW	RW	Reserved			
Name	Reserved [7:6]		LP-M_READY	DEBUG_-SESSION	Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	LPM_READY	Indicates whether certain low power functions are ready. The low current circuits take longer to startup after XRES, HIBERNATE wakeup, or supply supervision reset wakeup than the normal mode circuits. HIBERNATE mode may be entered regardless of this bit. 0: If a low power circuit operation is requested, it will stay in its normal operating mode until it is ready. If DEEPSLEEP is requested by all processors WFI/WFE, the device will instead enter SLEEP. When low power circuits are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP and low power circuits operate as requested in other registers. Default Value: 0
4	DEBUG_SESSION	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) Default Value: 0 **0x0: NO_SESSION :** No debug session active **0x1: SESSION_ACTIVE :** Debug session is active. Power modes behave differently to keep the debug session active, and current consumption may be higher than datasheet specification.

14.1.27 PWR_CTL2

Description: Power Mode Control 2

Address: 0x42401004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R	RW	Reserved		R	Reserved
HW Access	Reserved		RW	A	Reserved		RW	Reserved
Name	Reserved [23:22]		REFSYS-_VREF-BUF_OK	REFSYS-_VBUF_DIS	Reserved [19:18]		REFSYS-_VREF_OK	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	RW1C	Reserved	RW	RW	Reserved	R	Reserved
HW Access	A	A	Reserved	A	A	Reserved	RW	Reserved
Name	FREEZE_DPSLP_PD1	FREEZE_DPSLP	Reserved	BGREF_LPMODE	POR-BOD_LP-MODE	Reserved	REFSYS-_IREF_OK	Reserved

Bits	Name	Description
31	FREEZE_DPSLP_PD1	Controls whether mode and state of GPIOs and SIOs in Power Domain 1 are frozen. This is intended to be used as part of the DEEPSLEEP-RAM and DEEPSLEEP-OFF entry and exit sequences. It is set by HW when PD1 enters DEEPSLEEP-RAM and DEEPSLEEP-OFF modes. Writing a 1 clears freeze and GPIOs and SIOs resume normal operation. Default Value: 1
30	FREEZE_DPSLP	Controls whether mode and state of GPIOs and SIOs in Power Domain 0 are frozen. This is intended to be used as part of the DEEPSLEEP-RAM and DEEPSLEEP-OFF entry and exit sequences. It is set by HW when PD0 enters DEEPSLEEP-RAM and DEEPSLEEP-OFF modes. Writing a 1 clears freeze and GPIOs and SIOs resume normal operation. Default Value: 0
28	BGREF_LPMODE	Control the circuit-level power mode of the Bandgap Reference circuits for DEEPSLEEP. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. This requires CLK_LF to be operating properly, and it is SW's responsibility to ensure CLK_LF is correctly configured. Note that CLK_LF may be sourced from WCO, ILO, or PILO. When changing back to continuous operation, keep CLK_LF enabled for at least 5 cycles after clearing this bit to allow for internal synchronization. The setting is ignored during ACTIVE mode. 0: Bandgap Reference uses the normal settings. 1: Bandgap Reference uses the low power sample and hold circuits. Default Value: 0

14.1.27 PWR_CTL2 (continued)

27	PORBOD_LPMODE	Control the power mode of the POR/BOD circuits in DEEPSLEEP modes. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: POR/BOD circuits operate in normal mode during DEEPSLEEP. 1: POR/BOD circuits operate in low power mode during DEEPSLEEP. Response time is reduced to save current. Default Value: 0
25	REFSYS_IREF_OK	Indicates that the current reference is ready. Due to synchronization delays, it may take two IHO clock cycles for hardware to clear this bit after asserting REFI_DIS=1. Default Value: 0
21	REFSYS_VREFBUF_OK	Indicates that the voltage reference buffer is ready. Due to synchronization delays, it may take two IHO clock cycles for hardware to clear this bit after asserting REFVBUF_DIS=1. Default Value: 0
20	REFSYS_VBUF_DIS	Disable the voltage reference buffer. Firmware should only disable the buffer when there is no connected circuit that is using it. SRSS circuits that require it are the DPLL and ECO. A particular product may have circuits outside the SRSS that use the buffer. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. Default Value: 0
17	REFSYS_VREF_OK	Indicates that the normal mode of the voltage reference is ready. Default Value: 0

14.1.28 PWR_HIBERNATE

Description: HIBERNATE Mode Register

Address: 0x42401008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TOKEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	RW	RW	Reserved
HW Access	A				A	A	A	Reserved
Name	POLARITY_HIBPIN [23:20]				MASK_HIB-WDT	MASK_HI-BALARM	FREEZE	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW1S	RW	Reserved	RW			
HW Access	A	R	A	Reserved	A			
Name	HIBER-NATE	HIBER-NATE_DIS-ABLE	SENSE_-MODE	Reserved	MASK_HIBPIN [27:24]			

Bits	Name	Description
31	HIBERNATE	Firmware sets this bit to enter HIBERNATE mode. The system will enter HIBERNATE mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP. Both UNLOCK and FREEZE must have been set correctly in a previous write operations. Otherwise, it will not enter HIBERNATE. External supplies must have been stable for 250us before entering HIBERNATE mode. Default Value: 0
30	HIBERNATE_DISABLE	Hibernate disable bit. 0: Normal operation, HIBERNATE works as described 1: Further writes to this register are ignored Note: This bit is a write-once bit until the next reset. Avoid changing any other bits in this register while disabling HIBERNATE mode. Also, it is recommended to clear the UNLOCK code, if it was previously written.. Default Value: 0
29	SENSE_MODE	Power mode when wakeups are sensitive. The default of this field is 0 for software compatibility with other products. It is recommended to set this field to 1 for new/updated software. 0: Wakeups are sensitive only during HIBERNATE mode. A wakeup pulse that comes just before HIBERNATE entry may be missed. Backward compatible. 1: Wakeups are sensitive in HIBERNATE and higher modes. Before entering HIBERNATE, software must clear all unmasked, pending wakeups in PWR_HIB_WAKE_CAUSE register. An unmasked, pending wakeup causes HIBERNATE wakeup, even if it was pending from before HIBERNATE entry. This prevents missed wakeups. Default Value: 0

14.1.28 PWR_HIBERNATE (continued)

27 : 24	MASK_HIBPIN	Reserved. Default Value: 0
23 : 20	POLARITY_HIBPIN	Reserved. Default Value: 0
19	MASK_HIBWDT	Reserved. Default Value: 0
18	MASK_HIBALARM	Reserved. Default Value: 0
17	FREEZE	Controls whether mode and state of GPIOs and SIOs in the system are frozen. This is intended to be used as part of the HIBERNATE entry and exit sequences. When entering HIBERNATE mode, the first write instructs DEEPSLEEP peripherals that they cannot ignore the upcoming freeze command. This occurs even in the illegal condition where UNLOCK is not set. If UNLOCK and HIBERNATE are properly set, the IOs actually freeze on the second write. Supply supervision is disabled during HIBERNATE mode. HIBERNATE peripherals ignore resets (excluding XRES) while FREEZE==1. Default Value: 0
15 : 8	UNLOCK	This byte must be set to 0x3A for FREEZE or HIBERNATE fields to operate. Any other value in this register will cause FREEZE/HIBERNATE to have no effect, except as noted in the FREEZE description. Default Value: 0
7 : 0	TOKEN	Contains a 8-bit token that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from HIBERNATE using XRES,or a WDT reset will reset this register. Default Value: 0

14.1.29 PWR_LVD_CTL

Description: High Voltage / Low Voltage Detector (HVLVD) Configuration Register

Address: 0x42401020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	Reserved		RW			
HW Access	R	R	Reserved		R			
Name	HVLVD_EN	HVLVD_D-PSLP_EN	Reserved [5:4]		HVLVD_TRIPSEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [23:19]					HVLVD_AC-TION	HVLVD_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	HVLVD_ACTION	Action taken when the threshold is crossed in the programmed directions(s) Default Value: 0 **0x0: INTERRUPT :** Generate an interrupt **0x1: FAULT :** Generate a fault
17 : 16	HVLVD_EDGE_SEL	Sets which edge(s) will trigger an action when the threshold is crossed. Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge

14.1.29 PWR_LVD_CTL (continued)

		0x2: FALLING : Falling edge **0x3: BOTH :** Both rising and falling edges
7	HVLVD_EN	Enable HVLVD voltage monitor. Do not change other HVLVD settings when enabled. Default Value: 0
6	HVLVD_DPSLP_EN	1 = Enable HVLVD voltage monitor during Deepsleep if HVLVD_EN=1, but the response will be slowed to save power. 0 = HVLVD does not function during DEEPSLEEP, but it automatically returns to its configured setting after DEEPSLEEP wakeup. Default Value: 0
3 : 0	HVLVD_TRIPSEL	Threshold selection for HVLVD. Disable the detector (HVLVD_EN=0) before changing the threshold. 0: rise=2.78V (nom), fall=2.75V (nom) 1: rise=2.88V (nom), fall=2.85V (nom) 2: rise=2.98V (nom), fall=2.95V (nom) 3: rise=3.08V (nom), fall=3.05V (nom) 4: rise=3.18V (nom), fall=3.15V (nom) Default Value: 0

14.1.30 CLK_PATH_SELECT0

Description: Clock Path Select Register

Address: 0x42401200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					PATH_MUX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	PATH_MUX	Selects a source for clock PATH. *Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0* **0x0: HFSRC_0 :** IHO - Internal High-speed Oscillator **0x1: HFSRC_1 :** EXTCLK - External Clock Pin **0x2: HFSRC_2 :** ECO - External-Crystal Oscillator (Product Specific) **0x3: HFSRC_3 :** IMO - Internal R/C Oscillator (Product Specific) **0x4: HFSRC_4 :** ALTHF0 - Alternate High-Frequency clock input (product-specific clock)

14.1.30 CLK_PATH_SELECT0 (continued)

0x5: HFSRC_5 :

ALTHF1 - Alternate High-Frequency clock input (product-specific clock)

0x6: HFSRC_6 :

Reserved

0x7: HFSRC_7 :

DSI_MUX - Output of DSI mux for this path. Using a DSI source directly as root of HFCLK will result in undefined behavior.

14.1.31 CLK_ROOT_SELECT0

Description: Clock Root Select Register

Address: 0x42401240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				ROOT_MUX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				ROOT_DIV [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	A	Reserved						
Name	ENABLE	Reserved [30:24]						

Bits	Name	Description
31	ENABLE	Enable for this clock root. All clock roots default to disabled (ENABLE==0) except HFCLK0, which cannot be disabled. Default Value: 0
11 : 8	ROOT_DIV	Selects predivider value for this clock root and DSI input. This divider is after DIRECT_MUX. For products with DSI, the output of this mux is routed to DSI for use as a signal. For products with clock supervision, the output of this mux is the monitored clock for CSV_HF. Default Value: 0 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2 :** Divide selected clock source by 2 **0x2: DIV_BY_3 :** Divide selected clock source by 3 **0x3: DIV_BY_4 :** Divide selected clock source by 4

14.1.31 CLK_ROOT_SELECT0 (continued)

0x4: DIV_BY_5 :

Divide selected clock source by 5

0x5: DIV_BY_6 :

Divide selected clock source by 6

0x6: DIV_BY_7 :

Divide selected clock source by 7

0x7: DIV_BY_8 :

Divide selected clock source by 8

0x8: DIV_BY_9 :

Divide selected clock source by 9

0x9: DIV_BY_10 :

Divide selected clock source by 10

0xa: DIV_BY_11 :

Divide selected clock source by 11

0xb: DIV_BY_12 :

Divide selected clock source by 12

0xc: DIV_BY_13 :

Divide selected clock source by 13

0xd: DIV_BY_14 :

Divide selected clock source by 14

0xe: DIV_BY_15 :

Divide selected clock source by 15

0xf: DIV_BY_16 :

Divide selected clock source by 16

14.1.31 CLK_ROOT_SELECT0 (continued)

3 : 0	ROOT_MUX	Selects a clock path for HFCLK and SRSS DSI input . The output of this mux goes to the direct mux (see CLK_DIRECT_SELECT). Use CLK_SELECT_PATH[i] to configure the desired path. The number of clock paths is product-specific, and selecting an unimplemented path is not supported. Some paths may have PLL available (product-specific), and the control and bypass mux selections of these are in other registers. Configure a PLL using the related CLK_PLL_CONFIG[k] register. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. When switching to a different clock source, ensure that the ROOT_DIV is set to an appropriate value BEFORE changing the ROOT_MUX to avoid a temporary over/under-shoot in clock frequency that will occur if both fields are changed at the same time. Default Value: 0 **0x0: PATH0 :** Select PATH0 **0x1: PATH1 :** Select PATH1 **0x2: PATH2 :** Select PATH2 **0x3: PATH3 :** Select PATH3 **0x4: PATH4 :** Select PATH4 **0x5: PATH5 :** Select PATH5 **0x6: PATH6 :** Select PATH6 **0x7: PATH7 :** Select PATH7 **0x8: PATH8 :** Select PATH8 **0x9: PATH9 :** Select PATH9 **0xa: PATH10 :** Select PATH10

14.1.31 CLK_ROOT_SELECT0 (continued)

0xb: PATH11 :

Select PATH11

0xc: PATH12 :

Select PATH12

0xd: PATH13 :

Select PATH13

0xe: PATH14 :

Select PATH14

0xf: PATH15 :

Select PATH15

14.1.32 CLK_DIRECT_SELECT0

Description: Clock Root Direct Select Register

Address: 0x42401280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							A
Name	Reserved [15:9]							DIRECT_MUX

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	DIRECT_MUX	Direct selection mux that allows IHO to bypass most of the clock mux structure. For products with multiple regulators, this mux can be used to reduce current without requiring significant reconfiguration of the clocking network. The default value of HFCLK<0>==ROOT_MUX, and the default value for other clock trees is product-specific. Default Value: 1 **0x0: IHO :** Select IHO **0x1: ROOT_MUX :** Select ROOT_MUX selection

14.1.33 CLK_SELECT

Description: Clock selection register

Address: 0x42401300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					A		
Name	Reserved [7:3]					LFCLK_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	LFCLK_SEL	Select source for LFCLK. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0 **0x0: PILO :** PILO - Precision ILO, if present. **0x1: WCO :** WCO - Watch-Crystal Oscillator. Requires properly configured (including external watch crystal, if used), if present **0x2: ALTLF :** ALTLF - Alternate Low-Frequency Clock. Capability is product-specific **0x3: ECO_PRESCALER :** ECO_PRESCALER - External-Crystal Oscillator after prescaling, if present. Does not work in DEEPSLEEP or HIBERNATE modes. Intended for applications that operate in ACTIVE/SLEEP modes only. This option is only valid when ECO is present in the product. User must ensure that the CLK_ECO_PRESCALE is configured to generate a 32KHz clock when using this option.

14.1.33 CLK_SELECT (continued)

0x4: ILO :

ILO - Internal Low-speed Oscillator, if present

14.1.34 CLK_MF_SELECT

Description: Medium Frequency Clock Select Register

Address: 0x42401304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					MFCLK_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MFCLK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLE	Reserved [30:24]						

Bits	Name	Description
31	ENABLE	Enable for MFCLK (clk_mf). When disabling clk_mf, do not disable the source until after 5 clk_mf periods. clk_mf continues to operate in DEEPSLEEP for compatible sources. Firmware must disable clk_mf before entering DEEPSLEEP if the source is not compatible with DEEPSLEEP mode. Default Value: 0
15 : 8	MFCLK_DIV	Divide selected clock source by (1+MFCLK_DIV). The output of this divider is MFCLK (clk_mf). Allows for integer divisions in the range [1, 256]. Do not change this setting while ENABLE==1. Default Value: 0
2 : 0	MFCLK_SEL	Select source for MFCLK (clk_mf). Note that not all products support all clock sources. Selecting a clock source that is not supported results in undefined behavior. Default Value: 4 **0x0: IMO :** Internal Main Oscillator (IMO). DEEPSLEEP compatibility is product-specific. See CLK_IMO_CONFIG for capability of this product. **0x1: ILO :** ILO - Internal Low-speed Oscillator. **0x2: WCO :** WCO - Watch-Crystal Oscillator, if present.

14.1.34 CLK_MF_SELECT (continued)

0x3: ALTLF :

ALTLF - Alternate Low-Frequency Clock. Capability is product-specific

0x4: PILO :

PILO - Precision ILO, if present.

0x5: ECO_PRESCALER :

ECO_PRESCALER - External-Crystal Oscillator, if present, after prescaling in CLK_ECO_PRESCALE. Intended for applications that operate in ACTIVE/SLEEP modes only. Does not work in DEEPSLEEP mode.

0x6: IHO :

IHO clock. MFCLK_DIV should be >0 to achieve MF frequency. DEEPSLEEP compatibility is product-specific. See CLK_IHO_CONFIG for capability of this product.

0x7: RESERVED2 :

Reserved

14.1.35 CLK_ECO_PRESCALE

Description: ECO Prescaler Configuration Register

Address: 0x42401320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							ECO_DIV_ ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ECO_FRAC_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ECO_INT_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [31:26]						ECO_INT_DIV [25:24]	

Bits	Name	Description
25 : 16	ECO_INT_DIV	10-bit integer value allows for ECO frequencies up to 33.55MHz. Subtract one from the desired divide value when writing this field. For example, to divide by 1, write ECO_INT_DIV=0. Do not change this setting when ECO Prescaler is enabled. Default Value: 0
15 : 8	ECO_FRAC_DIV	8-bit fractional value, sufficient to get prescaler output within the +/-65ppm calibration range. Do not change this setting when ECO Prescaler is enabled. Default Value: 0
0	ECO_DIV_ENABLED	ECO prescaler enabled. HW sets this field to '1' as a result of an CLK_ECO_CONFIG.ECO_DIV_ENABLE command. HW sets this field to '0' as a result on a CLK_ECO_CONFIG.ECO_DIV_DISABLE command. ECO prescaler is incompatible with DEEPSLEEP modes, and firmware must disable it before entering DEEPSLEEP. Default Value: 0

14.1.36 CLK_IHO_CONFIG

Description: IHO Configuration Register

Address: 0x42401344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IHO_TRIM_FREQ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [15:11]					IHO_TRIM_FREQ [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW	Reserved					
HW Access	Reserved	R	Reserved					
Name	Reserved	DPS-LP_EN-ABLE	Reserved [29:24]					

Bits	Name	Description
30	DPSLP_ENABLE	Enable for IHO during DEEPSLEEP. This bit configures IHO behavior during DEEPSLEEP: 0: IHO is automatically disabled during DEEPSLEEP and enables upon wakeup; 1: IHO is kept enabled throughout DEEPSLEEP Default Value: 0
10 : 0	IHO_TRIM_FREQ	IHO frequency trim Default Value: 0x42E

14.1.37 CLK_ECO_CONFIG

Description: ECO Configuration Register

Address: 0x42401360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved		RW	RW	Reserved		
HW Access	R	Reserved		RW1C	RW1C	Reserved		
Name	ECO_EN	Reserved [30:29]		ECO_DIV_ENABLE	ECO_DIV_-DISABLE	Reserved [26:24]		

Bits	Name	Description
31	ECO_EN	Master enable for ECO oscillator. Configure the settings in CLK_ECO_CONFIG2 to work with the selected crystal, before enabling ECO. Default Value: 0
28	ECO_DIV_ENABLE	ECO prescaler enable command (mutually exclusive with ECO_DIV_DISABLE). ECO Prescaler only works in ACTIVE and SLEEP modes. SW sets this field to '1' to enable the divider and HW sets this field to '0' to indicate that divider enabling has completed. When the divider is enabled, its integer and fractional counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the ECO_DIV_DISABLE field. 1: Configure CLK_ECO_PRESCALE registers. 2: Enable the divider using the ECO_DIV_ENABLE field. HW sets the ECO_DIV_ENABLE field to '0' when the enabling is performed and HW set CLK_ECO_PRESCALER.ENABLED to '1' when the enabling is performed. Default Value: 0
27	ECO_DIV_DISABLE	ECO prescaler disable command (mutually exclusive with ECO_DIV_ENABLE). SW sets this field to '1' and HW sets this field to '0'. HW sets ECO_DIV_DISABLE field to '0' immediately and HW sets CLK_ECO_PRESCALE.ECO_DIV_EN field to '0' immediately. Default Value: 0

14.1.38 CLK_ECO_CONFIG2

Description: ECO Configuration Register 2

Address: 0x42401364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			A				
Name	Reserved [7:5]			ECO_TRIM_CL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				A			
Name	Reserved [15:12]				ECO_TRIM_GAIN [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							A
Name	Reserved [23:17]							ECO_C-TRL_AMP-DETEN

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	ECO_CTRL_AMPDETEN	Amplifer detect enable Default Value: 0
11 : 8	ECO_TRIM_GAIN	Gain trim Default Value: 0x6
4 : 0	ECO_TRIM_CL	Crystal load cap configuration trim Default Value: 0x1B

14.1.39 CLK_ECO_STATUS

Description: ECO Status Register

Address: 0x42401368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						ECO_READY	ECO_OK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	ECO_READY	Indicates the ECO internal oscillator circuit power has had enough time to fully stabilize and the CLK_EN can be set. The ECO_OK bit should be used to determine that the ECO is ready for use. Default Value: 0
0	ECO_OK	Indicates the ECO internal oscillator circuit has sufficient amplitude. It may not meet the PPM accuracy or duty cycle spec. Default Value: 0

14.1.40 CLK_PILO_CONFIG

Description: Precision ILO Configuration Register

Address: 0x42401370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	A	Reserved						
Name	PILO_EN	Reserved [30:24]						

Bits	Name	Description
31	PILO_EN	Enable PILO. If the PILO is the selected source for WDT, writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. To save power FW must disable PILO upon entry to Hibernate if it is not used as a Hibernate clock source. PILO will continue to run in XRES if enabled. Default Value: 1

14.1.41 CLK_PILO_STATUS

Description: Precision ILO Status Register

Address: 0x42401374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							PILO_OK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	PILO_OK	Indicates the PILO is running. Default Value: 0

14.1.42 CLK_WCO_CONFIG

Description: WCO Configuration Register

Address: 0x42401390

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	Reserved		
HW Access	Reserved				A	Reserved		
Name	Reserved [7:4]				WCO_EN	Reserved [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW		Reserved	RW		
HW Access	Reserved		A		Reserved	A		
Name	Reserved [15:14]		PRESCALER [13:12]		Reserved	CLK_RTC_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW				Reserved			RW
HW Access	A				Reserved			A
Name	WCO_TRIM_GAIN [23:20]				Reserved [19:17]			WCO_BY-PASS

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved						A	
Name	Reserved [31:26]						WCO_CTRL_PWRMOD [25:24]	

Bits	Name	Description
25 : 24	WCO_CTRL_PWRMOD	If the BAK (RTC) is the selected source for WDT, Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. WCO power mode control: 00: low power mode(agc on); 01: high power mode (agc off) ; 10: reserved 11: high power startup mode (agc_off intially then turns on) Default Value: 0
23 : 20	WCO_TRIM_GAIN	main amplifier gain control. Please use S22SRSSA_WCO_CALCULATOR to obtain appropriate value for the attached crystal. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register Default Value: 0xC
16	WCO_BYPASS	Configures the WCO for different board-level connections to the WCO pins. For example, this can be used to connect an external watch crystal oscillator instead of a watch crystal. In all cases, the two related GPIO pins (WCO input and output pins) must be configured as analog connections using GPIO registers, and they must be hooked at the board level as described below. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. Also if the BAK (RTC) is the selected source for WDT, Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. 0: Watch crystal. Connect a 32.768 kHz watch crystal between WCO input and output pins. 1: Clock signal, either a square wave or sine wave. See PRESCALER field for connection information. Default Value: 0

14.1.42 CLK_WCO_CONFIG (continued)

13 : 12	PRESCALER	Prescaler for real time clock used when WCO_BYPASS=1 and CLK_SEL = WCO. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. Also if the BAK (RTC) is the selected source for WDT, Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. 0: 32768 Hz square wave. Connect a 32768 Hz square wave to WCO input pin (XIP). Do not connect WCO output pin (XOP). 1: 60 Hz sine wave. Connect an AC-coupled sine wave to WCO input pin. Do not connect the WCO output pin at the board level. 2: 50 Hz sine wave. Connect an AC-couple sine wave to WCO input pin. Do not connect the WCO output pin at the board level. 3: reserved Default Value: 0
10 : 8	CLK_RTC_SEL	Clock select for RTC clock. If the BAK (RTC) is the selected source for WDT, Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. Selecting a clock that is not running results in unpredictable behavior. Default Value: 0 **0x0: WCO :** Watch-crystal oscillator input, available in Active, DeepSleep and Hibernate. **0x1: ALTBAK :** This allows to use the LFCLK selection as an alternate backup domain clock. Note that LFCLK is only available in Active and DeepSleep power modes. Note that LFCLK clock glitches can propagate into the RTC logic when the clock is stopped. For this reason, if the WCO, PILO or ILO is intended as the clock source then choose it directly instead of routing through LFCLK. **0x2: ILO :** Internal Low frequency Oscillator, available in Active, DeepSleep, and Hibernate. With this option selected, ILO reset is suppressed in XRES/Hibernate modes. **0x3: PILO :** Precision internal low-speed oscillator, available in Active, DeepSleep, and Hibernate. With this option selected, PILO reset is suppressed in XRES/Hibernate modes. **0x4: RESERVED :** Reserved
3	WCO_EN	Watch-crystal oscillator (WCO) enable. If there is an RTC write in progress and WCO is the clock source for clk_rtc when this bit is cleared, the WCO will be internally kept on until the write completes. After enabling the WCO software must wait until CLK_WCO_STATUS.WCO_OK=1 before configuring any component that depends on clk_lf/clk_rtc, like for example RTC or WDTs. If the BAK (RTC) is the selected source for WDT, writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. Default Value: 0

14.1.43 CLK_WCO_STATUS

Description: WCO Status Register

Address: 0x42401394

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R	Reserved	
HW Access	Reserved					W	Reserved	
Name	Reserved [7:3]					WCO_OK	Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	WCO_OK	Indicates that output has transitioned. Default Value: 0

14.1.44 CSV_HF_CSV0_REF_CTL

Description: Clock Supervision Reference Control

Address: 0x42401400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CSV_STARTUP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CSV_STARTUP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved					
HW Access	R	R	Reserved					
Name	CSV_EN	CSV_ACTION	Reserved [29:24]					

Bits	Name	Description
31	CSV_EN	Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup. A CSV error detection is reported to the Fault structure, or instead it can generate a power reset. Default Value: 0
30	CSV_ACTION	Specifies the action taken when an anomaly is detected on the monitored clock. CSV in DeepSleep domain always do a Fault report (which also wakes up the system). Default Value: 0 **0x0: FAULT :** Generate a fault **0x1: RESET :** Cause a power reset. This should only be used for clk_hf0.

14.1.44 CSV_HF_CSV0_REF_CTL (continued)

15 : 0	CSV_STARTUP	Startup delay time -1 (in reference clock cycles), after enable or DeepSleep wakeup, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. Default Value: 0

14.1.45 CSV_HF_CSV0_REF_LIMIT

Description: Clock Supervision Reference Limits

Address: 0x42401404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CSV_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CSV_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CSV_UPPER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CSV_UPPER [31:24]							

Bits	Name	Description
31 : 16	CSV_UPPER	Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. Default Value: 0
15 : 0	CSV_LOWER	Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. Default Value: 0

14.1.46 CSV_HF_CSV0_MON_CTL

Description: Clock Supervision Monitor Control

Address: 0x42401408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CSV_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CSV_PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	CSV_PERIOD	Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens. PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency) In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1 Additionally margin must be added for accuracy of both clocks. Default Value: 0

14.1.47 CSV_REF_SEL

Description: Select CSV Reference clock for Active domain

Address: 0x42401500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					REF_MUX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	REF_MUX	Selects a source for clock clk_ref_hf. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 4 **0x0: IMO :** IMO - Internal R/C Oscillator (product specific) **0x1: EXTCLK :** EXTCLK - External Clock Pin **0x2: ECO :** ECO - External-Crystal Oscillator **0x3: ALTHF0 :** ALTHF0 - Alternate High-Frequency clock input (product-specific clock) **0x4: IHO :** IHO - Internal High-speed Oscillator

14.1.47 CSV_REF_SEL (continued)

0x5: ALTHF1 :

ALTHF1 - Alternate High-Frequency clock input (product-specific clock)

14.1.48 CSV_LF_REF_SEL

Description: Select CSV Reference clock for LF clock

Address: 0x42401520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						LF_REF_MUX [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	LF_REF_MUX	Selects a source for clock clk_ref_lf. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Same clcok sources are also souce for clk_lf. Do not select the same clock. Default Value: 0 **0x0: PILO :** Precision internal low-speed oscillator, available in Active, DeepSleep, and Hibernate. (Product Specific) **0x1: ILO :** Internal Low frequency Oscillator, available in Active, DeepSleep, and Hibernate. (Product Specific) **0x2: WCO :** Watch-crystal oscillator input, available in Active, DeepSleep, and Hibernate. (Product Specific) **0x3: TIMERCLK :** Timer clock. Divided clock from IHO set to 1MHz. Available only during Active mode. If this clock is selected as reference, CSV will be disabled by hardware when entering lower power modes (DPSLP) and re-enabled back in Active.

14.1.49 CSV_LF_CSV_REF_CTL

Description: Clock Supervision Reference Control

Address: 0x42401530

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CSV_STARTUP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	CSV_EN	Reserved [30:24]						

Bits	Name	Description
31	CSV_EN	Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup. CSV in Backup domain: Clock supervision operates during Hibernate mode, can be configured to wake from Hibernate, and continues operating during reboot. A CSV error detection is reported to the Fault structure. Default Value: 0
7 : 0	CSV_STARTUP	Startup delay time -1 (in reference clock cycles), after enable, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. Default Value: 0

14.1.50 CSV_LF_CSV_REF_LIMIT

Description: Clock Supervision Reference Limits

Address: 0x42401534

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CSV_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CSV_UPPER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	CSV_UPPER	Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. Default Value: 0
7 : 0	CSV_LOWER	Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. Default Value: 0

14.1.51 CSV_LF_CSV_MON_CTL

Description: Clock Supervision Monitor Control

Address: 0x42401538

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CSV_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	CSV_PERIOD	Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens. PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency) In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1 Additionally margin must be added for accuracy of both clocks. Default Value: 0

14.1.52 CLK_DPLL_LP0_CONFIG

Description: DPLL_LP Configuration Register

Address: 0x42401600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FEEDBACK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			REFERENCE_DIV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [23:21]			OUTPUT_DIV [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved	RW		RW	Reserved		
HW Access	R	Reserved	R		R	Reserved		
Name	ENABLE	Reserved	BYPASS_SEL [29:28]		PLL_DCO_-MODE	Reserved [26:24]		

Bits	Name	Description
31	ENABLE	Master enable for PLL. Setup FEEDBACK_DIV, REFERENCE_DIV, and OUTPUT_DIV at least one cycle before setting ENABLE=1. fOUT = (FEEDBACK_DIV + FRAC_EN*FRAC_DIV/2^24) * (fREF / REFERENCE_DIV) / (OUT-PUT_DIV) 0: Block is disabled. When the PLL disables, hardware controls the bypass mux as described in BYPASS_SEL, before disabling the PLL circuit. 1: Block is enabled Default Value: 0
29 : 28	BYPASS_SEL	Bypass mux located just after PLL output. This selection is glitch-free and can be changed while the PLL is running. When changing BYPASS_SEL, do not turn off the reference clock or PLL clock for five cycles (whichever is slower). Default Value: 0 **0x0: AUTO :** Automatic using lock indicator. When unlocked, automatically selects PLL reference input (by-pass mode). When locked, automatically selects PLL output. If ENABLE=0, automatically selects PLL reference input. **0x1: LOCKED_OR_NOTHING :** Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock su-pervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running. If ENABLE=0, no clock is output.

14.1.52 CLK_DPLL_LP0_CONFIG (continued)

		0x2: PLL_BYPASS : Select PLL reference input (bypass mode). Ignores lock indicator **0x3: PLL_OUT :** Select PLL output. Ignores lock indicator. If ENABLE=0, no clock is output.
27	PLL_DCO_MODE	dco_mode='0' DCO freq 160-310MHz , '1' - DCO freq 310-480MHz Default Value: 0
20 : 16	OUTPUT_DIV	Control bits for Output divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: divide by 1. Suitable for direct usage as HFCLK source. 2: divide by 2. Suitable for direct usage as HFCLK source. ... 16: divide by 16. Suitable for direct usage as HFCLK source. >16: illegal (undefined behavior) Default Value: 2
12 : 8	REFERENCE_DIV	Control bits for reference divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 16: divide by 16 others: illegal (undefined behavior) Default Value: 1
7 : 0	FEEDBACK_DIV	Control bits for feedback divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0-15: illegal (undefined behavior) 16: divide by 16 ... 200: divide by 200 >200: illegal (undefined behavior) Default Value: 22

14.1.53 CLK_DPLL_LP0_CONFIG2

Description: DPLL_LP Configuration Register 2

Address: 0x42401604

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	FRAC_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	FRAC_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	FRAC_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			Reserved			
HW Access	R	R			Reserved			
Name	FRAC_EN	FRAC_DITHER_EN [30:28]			Reserved [27:24]			

Bits	Name	Description
31	FRAC_EN	Enables fractional division mode. Default Value: 0
30 : 28	FRAC_DITHER_EN	Enables dithering during fractional operation. 3'b000: disables dithering; 3'b001: enables dithering; others: reserved Default Value: 0
23 : 0	FRAC_DIV	Control bits for fractional divider. This value is interpreted as a fraction of the PFD frequency, i.e. fPFD * (FRAC_DIV/2^24). This field can be dynamically updated within the 1000ppm control limit. It takes up to 115 AHB cycles to transfer the setting to the PLL, and writes that occur faster may be silently ignored and require the application to write again after the previous update has finished. Reading the register returns the accepted value. The PLL will start targeting the new value, but it may take significant time (milliseconds) to stabilize at the new average value. Do not change the FRAC_DIV setting while the PLL is initially locking. Default Value: 0

14.1.54 CLK_DPLL_LP0_CONFIG3

Description: DPLL_LP Configuration Register 3

Address: 0x42401608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SSCG_DEPTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						SSCG_DEPTH [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					SSCG_RATE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved		RW	Reserved			RW
HW Access	R	Reserved		R	Reserved			R
Name	SSCG_EN	Reserved [30:29]		SSCG_-MODE	Reserved [27:25]			SSC-G_DITH-ER_EN

Bits	Name	Description
31	SSCG_EN	Enables spreading mode. When SSCG mode is enabled, DPLL_LP_TEST4.PLL_DIS_FAST_LOCK should be set to 1 to disable fast re-lock. Default Value: 0
28	SSCG_MODE	Reserved. Write zero always. Default Value: 0
24	SSCG_DITHER_EN	Reserved. Default Value: 0
18 : 16	SSCG_RATE	Control bits for SSCG modulation rate as a factor of fPFD clock frequency. Audio applications should choose a setting that results in a modulation rate that is greater than 20kHz, so fPFD/512 or fPFD/256 is recommended. Note: All modulation rate trims are valid as long as the fPFD/_number> is less than 32KHz, which is the max modulation rate defined at spec. 0: Modulation rate = fPFD/4096, 1: Modulation rate = fPFD/2048, 2: Modulation rate = fPFD/1024, 3: Modulation rate = fPFD/512, 4: Modulation rate = fPFD/256, 5: Modulation rate = pPFD/128, 6: Modulation rate = pPFD/744 others: reserved Default Value: 0

14.1.54 CLK_DPLL_LP0_CONFIG3 (continued)

9 : 0	SSCG_DEPTH	Control bits for SSCG modulation depth as a percentage of the non-modulated clock. The following choices are supported, and all others are reserved: 10'h029: -0.5% (down-spread), 10'h052: -1% (down-spread), 10'h0a4: -2% (down-spread), 10'h0f6: -3% (down-spread), 10'h148: -4% (down-spread), 10'h19a: -5% (down-spread) Default Value: 0

14.1.55 CLK_DPLL_LP0_CONFIG4

Description: DPLL_LP Configuration Register 4

Address: 0x4240160C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCO_CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW	Reserved		RW		
HW Access	Reserved		R	Reserved		R		
Name	Reserved [15:14]		PLL_CS_PB2_DIS	Reserved [12:11]		DCO_CODE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		Reserved			
HW Access	Reserved		R		Reserved			
Name	Reserved [23:22]		PLL_TG [21:20]		Reserved [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							PLL_SP

Bits	Name	Description
24	PLL_SP	Reserved Default Value: 0
21 : 20	PLL_TG	This value is a number of PFD clocks in relation to the DCO count. Can change the number of counts, set by p_div in integer mode, by the values of -1, +1, or +2. 0: 0 1: -1 2: +1 3: +2 In integer and SSCG mode, PLL_TG must be set to 0. If in fractional mode, PLL_TG must be 0 if frac_ratio <= 0.5 (pll_frac <= 2^23), PLL_TG must be 2 if frac_ratio > 0.5 (pll_frac > 2^23). Default Value: 0
13	PLL_CS_PB2_DIS	disable internal bias Default Value: 0x0
10 : 0	DCO_CODE	Initial DCO code. It is recommended to leave this at the default setting. This setting only has effect in open loop mode. See DPLL BROS regarding test modes. Default Value: 0xF

14.1.56 CLK_DPLL_LP0_CONFIG5

Description: DPLL_LP Configuration Register 5

Address: 0x42401610

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved	RW					
HW Access	R	Reserved	R					
Name	KP_INT	Reserved	KI_INT [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		Reserved	RW				
HW Access	R		Reserved	R				
Name	KI_ACC_INT [15:14]		Reserved	KP_INT [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW			Reserved	RW			
HW Access	R			Reserved	R			
Name	KP_ACC_INT [23:21]			Reserved	KI_ACC_INT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	R			Reserved	R		
Name	Reserved	PWRUP_ACC_INT [30:28]			Reserved	KP_ACC_INT [26:24]		

Bits	Name	Description
30 : 28	PWRUP_ACC_INT	Power Up Accleration Coefficient for INT operation Default Value: 0
26 : 21	KP_ACC_INT	Gain of P/I loop filter integrator path during cold start for INT operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x23
19 : 14	KI_ACC_INT	Gain of P/I loop filter integrator path during cold start for INT operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x27
12 : 7	KP_INT	Gain of P/I loop filter integrator path for INT operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x20
5 : 0	KI_INT	Gain of P/I loop filter integrator path for INT operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x28

14.1.57 CLK_DPLL_LP0_CONFIG6

Description: DPLL_LP Configuration Register 6

Address: 0x42401614

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved	RW					
HW Access	R	Reserved	R					
Name	KP_FRACT	Reserved	KI_FRACT [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		Reserved	RW				
HW Access	R		Reserved	R				
Name	KI_ACC_FRACT [15:14]		Reserved	KP_FRACT [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW			Reserved	RW			
HW Access	R			Reserved	R			
Name	KP_ACC_FRACT [23:21]			Reserved	KI_ACC_FRACT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	R			Reserved	R		
Name	Reserved	PWRUP_ACC_FRACT [30:28]			Reserved	KP_ACC_FRACT [26:24]		

Bits	Name	Description
30 : 28	PWRUP_ACC_FRACT	Power Up Accleration Coefficient for FRACT operation Default Value: 0
26 : 21	KP_ACC_FRACT	Gain of P/I loop filter integrator path during cold start for FRACT operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x1C
19 : 14	KI_ACC_FRACT	Gain of P/I loop filter integrator path during cold start for FRACT operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x27
12 : 7	KP_FRACT	Gain of P/I loop filter proportional path for FRACT operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x24
5 : 0	KI_FRACT	Gain of P/I loop filter proportional path for FRACT operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x2C

14.1.58 CLK_DPLL_LP0_CONFIG7

Description: DPLL_LP Configuration Register 7

Address: 0x42401618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved	RW					
HW Access	R	Reserved	R					
Name	KP_SSCG	Reserved	KI_SSCG [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		Reserved	RW				
HW Access	R		Reserved	R				
Name	KI_ACC_SSCG [15:14]		Reserved	KP_SSCG [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW			Reserved	RW			
HW Access	R			Reserved	R			
Name	KP_ACC_SSCG [23:21]			Reserved	KI_ACC_SSCG [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	R			Reserved	R		
Name	Reserved	PWRUP_ACC_SSCG [30:28]			Reserved	KP_ACC_SSCG [26:24]		

Bits	Name	Description
30 : 28	PWRUP_ACC_SSCG	Power Up Accleration Coefficient for SSCG operation Default Value: 0
26 : 21	KP_ACC_SSCG	Gain of P/I loop filter integrator path during cold start for SSCG operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x23
19 : 14	KI_ACC_SSCG	Gain of P/I loop filter integrator path during cold start for SSCG operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x27
12 : 7	KP_SSCG	Gain of P/I loop filter proportional path for SSCG operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x1C
5 : 0	KI_SSCG	Gain of P/I loop filter proportional path for SSCG operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x1C

14.1.59 CLK_DPLL_LP0_STATUS

Description: DPLL_LP Status Register

Address: 0x4240161C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1C	R
HW Access	Reserved						A	W
Name	Reserved [7:2]						UN-LOCK_OC-CURRED	LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	UNLOCK_OCCURRED	This bit sets whenever the PLL Lock bit goes low, and stays set until cleared by firmware. Note: When disabling DPLL via register write, UNLOCK_OCCURRED will set. Therefore, after enabling DPLL and DPLL successfully locks, FW should clear UNLOCK_OCCURRED flag to prevent a false positive that would indicate that DPLL erroneously unlocked. Default Value: 0
0	LOCKED	PLL Lock Indicator Default Value: 0

14.1.60 CLK_DPLL_HP0_CONFIG

Description: DPLL_HP Configuration Register

Address: 0x42401800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PLL_FREQ_NDIV_INT_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	R			Reserved	R		
Name	Reserved	PLL_FREQ_KDIV_SEL [14:12]			Reserved	PLL_FREQ_PDIV_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved	RW		Reserved			
HW Access	R	Reserved	R		Reserved			
Name	ENABLE	Reserved	BYPASS_SEL [29:28]		Reserved [27:24]			

Bits	Name	Description
31	ENABLE	Master enable for PLL. Setup PLL for integer, fract or SCSG at least one cycle before setting ENABLE=1. 0: Block is disabled. When the PLL disables, hardware controls the bypass mux as described in BYPASS_SEL, before disabling the PLL circuit. 1: Block is enabled Default Value: 0
29 : 28	BYPASS_SEL	Bypass mux located just after PLL output. This selection is glitch-free and can be changed while the PLL is running. When changing BYPASS_SEL, do not turn off the reference clock or PLL clock for five cycles (whichever is slower). Default Value: 0 **0x0: AUTO :** Automatic using lock indicator. When unlocked, automatically selects PLL reference input (bypass mode). When locked, automatically selects PLL output. If ENABLE=0, automatically selects PLL reference input. **0x1: LOCKED_OR_NOTHING :** Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock supervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running. If ENABLE=0, no clock is output. **0x2: PLL_BYPASS :** Select PLL reference input (bypass mode). Ignores lock indicator

14.1.60 CLK_DPLL_HP0_CONFIG (continued)

		0x3: PLL_OUT : Select PLL output. Ignores lock indicator. If ENABLE=0, no clock is output.
14 : 12	PLL_FREQ_KDIV_SEL	K-divider division factor (K = kdiv_sel_i + 1) Default Value: 1
10 : 8	PLL_FREQ_PDIV_SEL	P-divider division factor (P = pdiv_sel_i + 1) (Cannot be changed on the fly when the PLL is enabled) Default Value: 0
7 : 0	PLL_FREQ_NDIV_INT_SEL	N-divider division factor (N = ndiv_sel_i + 1) (Cannot be changed on the fly when the PLL is enabled) Default Value: 19

14.1.61 CLK_DPLL_HP0_CONFIG2

Description: DPLL_HP Configuration Register 2

Address: 0x42401804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PLL_FREQ_NDIV_FRACT_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PLL_FREQ_NDIV_FRACT_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW				
HW Access	R			R				
Name	PLL_FREQ_MODE_SEL [23:21]			PLL_FREQ_NDIV_FRACT_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				PLL_IVR_TRIM [27:24]			

Bits	Name	Description
27 : 24	PLL_IVR_TRIM	control word for trimming the regulated voltage that is internally generated from the 1v8 supply (default value = '10') (Cannot be changed on the fly when the PLL is enabled) Default Value: 0x8
23 : 21	PLL_FREQ_MODE_SEL	selects the waiting time for Power Initialization sequence, based on the PLL running frequency (Cannot be changed on the fly when the PLL is enabled) Default Value: 7
20 : 0	PLL_FREQ_NDIV_-FRACT_SEL	N-divider division factor (N = ndiv_sel_i + 1) (Cannot be changed on the fly when the PLL is enabled) Default Value: 0

14.1.62 CLK_DPLL_HP0_CONFIG3

Description: DPLL_HP Configuration Register 3

Address: 0x42401808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							PLL_-CLKR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	Reserved				
HW Access	Reserved		R	Reserved				
Name	Reserved [31:30]		PLL_FDS-M_SEL	Reserved [28:24]				

Bits	Name	Description
29	PLL_FDSM_SEL	DSM clock division select (Cannot be changed on the fly when the PLL is enabled) Default Value: 0 **0x0: DIV_BY_4 :** Divide output by 4 **0x1: DIV_BY_2 :** Divide output by 2
0	PLL_CLKR_SEL	Select retimed reference clock (Cannot be changed on the fly when the PLL is enabled) Default Value: 1

14.1.63 CLK_DPLL_HP0_CONFIG4

Description: DPLL_HP Configuration Register 4

Address: 0x4240180C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	PLL_LF_LC_BETA [7:5]			PLL_LF_LC_ALPHA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW			Reserved	RW	
HW Access	Reserved		R			Reserved	R	
Name	Reserved [15:14]		PLL_FLOCK_EN_THRESH [13:11]			Reserved	PLL_LF_LC_BETA [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	PLL_-FLOCK_LK_WAITPER	PLL_FLOCK_LK_THRESH [22:20]			PLL_FLOCK_WAITPER [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW				RW		
HW Access	Reserved	R				R		
Name	Reserved	PLL_FLOCK_OBSWIN [30:27]				PLL_FLOCK_LK_WAITPER [26:24]		

Bits	Name	Description
30 : 27	PLL_FLOCK_OBSWIN	Period over which PQDIFF is computed/observed. If 0 = use HW computed window. Supported values: 0-4 and 8 (Cannot be changed on the fly when the PLL is enabled) Default Value: 0
26 : 23	PLL_FLOCK_LK_WAIT-PER	Period over which flock_en_thresh must be met in order for Freq Locking. Supported values: 0-8 (Cannot be changed on the fly when the PLL is enabled) Default Value: 0x4
22 : 20	PLL_FLOCK_LK_-THRESH	PQDIFF threshold under which DLL asserts Freq LOCK (Cannot be changed on the fly when the PLL is enabled) Default Value: 0x7
19 : 16	PLL_FLOCK_WAITPER	Period over which flock_en_thresh must be met in order for FINE Filtering enabling. Supported values: 0-8 (Cannot be changed on the fly when the PLL is enabled) Default Value: 0x6
13 : 11	PLL_FLOCK_EN_-THRESH	PQDIFF threshold under which FINE Filtering gets enabled (Cannot be changed on the fly when the PLL is enabled) CONFIG.PLL_FREQ_NDIV_INT_SEL >= 20 -> PLL_FLOCK_EN_THRESH == 0x7; CONFIG.PLL_FREQ_NDIV_INT_SEL < 20 -> PLL_FLOCK_EN_THRESH == 0x3; Default Value: 0x3
9 : 5	PLL_LF_LC_BETA	Beta value of the coarse filter (Cannot be changed on the fly when the PLL is enabled) Default Value: 0x5
4 : 0	PLL_LF_LC_ALPHA	Alpha value of the coarse filter (Cannot be changed on the fly when the PLL is enabled) Default Value: 0xC

14.1.64 CLK_DPLL_HP0_CONFIG5

Description: DPLL_HP Configuration Register 5

Address: 0x42401810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	PLL_LF_BETA [7:5]			PLL_LF_ALPHA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved		RW	
HW Access	Reserved			R	Reserved		R	
Name	Reserved [15:13]			PLL_LF_SET_PARAMS	Reserved [11:10]		PLL_LF_BETA [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	PLL_DT_CAL_DIG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			PLL_DT_CAL_DIG [28:24]				

Bits	Name	Description
28 : 16	PLL_DT_CAL_DIG	FW should read pll_dutycal_dig_o only when pll_dutycal_ok is high to know the status of DUTY CAL circuit. Default Value: 0x0
12	PLL_LF_SET_PARAMS	enable for external loop filter control (alpha and beta values) (Cannot be changed on the fly when the PLL is enabled) Default Value: 0x1
9 : 5	PLL_LF_BETA	External beta value (Cannot be changed on the fly when the PLL is enabled) Fref/(pdiv_sel_i+1) >= 25MHz -> PLL_LF_BETA == 0x14 Fref/(pdiv_sel_i+1) < 25MHz -> PLL_LF_BETA == 0x10 Default Value: 0x14
4 : 0	PLL_LF_ALPHA	External alpha value (Cannot be changed on the fly when the PLL is enabled) Default Value: 0x14

14.1.65 CLK_DPLL_HP0_TRIGMOD

Description: DPLL_HP Trigmod SSCG Register

Address: 0x42401814

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PLL_TRIMOD_FREQ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PLL_TRIMOD_FREQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PLL_TRIMOD_GRD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PLL_TRIMOD_GRD [31:24]							

Bits	Name	Description
31 : 16	PLL_TRIMOD_GRD	Triangular-Frequency Modulation: modulation gradient. See formula in the BROS (word file) (Can be changed when PLL is enabled but cannot be changed on the fly when pll_trimod_en_i=1) Default Value: 0
15 : 0	PLL_TRIMOD_FREQ	Triangular-Frequency Modulation: modulation frequency. See formula in the BROS (word file) (Can be changed when PLL is enabled but cannot be changed on the fly when pll_trimod_en_i=1) Default Value: 0

14.1.66 CLK_DPLL_HP0_TRIGMOD2

Description: DPLL_HP Trigmod2 SSCG Register

Address: 0x42401818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PLL_TRIMOD_RATE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PLL_TRIMOD_RATE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW	Reserved	RW		
HW Access	Reserved			R	Reserved	R		
Name	Reserved [23:21]			PLL_TRI-MOD_EN	Reserved	PLL_TRIMOD_RATE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							PLL_TRI-MOD_STP

Bits	Name	Description
24	PLL_TRIMOD_STP	Triangular-Frequency Modulation stop Default Value: 0
20	PLL_TRIMOD_EN	Triangular-Frequency Modulation enable Default Value: 0
18 : 0	PLL_TRIMOD_RATE	triangular frequency modulation: trimod_rate = mod_grad_i * 16/mod_freq_i (Cannot be changed on the fly when the PLL is enabled) Default Value: 0

14.1.67 CLK_DPLL_HP0_STATUS

Description: DPLL_HP Status Register

Address: 0x4240181C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1C	R
HW Access	Reserved						A	W
Name	Reserved [7:2]						UN-LOCK_OC-CURRED	LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			R	Reserved			RW
HW Access	Reserved			RW	Reserved			R
Name	Reserved [23:21]			PLL_LOCK-DE-T_RES_ACK	Reserved [19:17]			PLL_LOCK-DET_RES

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20	PLL_LOCKDE-T_RES_ACK	acknowledgement for lock detection restart Default Value: 0
16	PLL_LOCKDET_RES	Restart lock detector Default Value: 0
1	UNLOCK_OCCURRED	This bit sets whenever the PLL Lock bit goes low, and stays set until cleared by firmware. Default Value: 0
0	LOCKED	PLL Lock Indicator Default Value: 0

14.1.68 CLK_DPLL_HP0_DUTYCAL_CTRL

Description: DPLL_HP_User DUTYCAL Control Register

Address: 0x42401820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R	R	RW		
HW Access	Reserved			W	W	R		
Name	Reserved [7:5]			PLL_DUTY_CAL_OK	PLL_DUTY_CAL_RATIO_OK	PLL_DUTYCAL_DELTA [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PLL_DUTYCAL_TARGET [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved	RW	RW				
HW Access	R	Reserved	R	R				
Name	PLL_DUTY_CAL_EN	Reserved	PLL_DUTY_CAL_CTRL_RG_EN	PLL_DUTYCAL_TARGET [28:24]				

Bits	Name	Description
31	PLL_DUTYCAL_EN	dutycal: enables duty cycle calibration (Cannot be changed on the fly when the PLL is enabled) Default Value: 1
29	PLL_DUTYCAL_CTRL_RG_EN	dutycal: enables ring oscillator for duty cycle digitization (Cannot be changed on the fly when the PLL is enabled) Default Value: 0
28 : 16	PLL_DUTYCAL_TARGET	duty cycle target (Cannot be changed on the fly when the PLL is enabled) Default Value: 0
4	PLL_DUTY_CAL_OK	Status of the duty calibration ok Default Value: 0
3	PLL_DUTY_CAL_RATIO_OK	Status of the duty calibration ratio ok Default Value: 0
2 : 0	PLL_DUTYCAL_DELTA	dutycal: margins for the duty cycle calibration error (Cannot be changed on the fly when the PLL is enabled) Default Value: 0

14.1.69 RES_CAUSE

Description: Reset Cause Observation Register

Address: 0x42401BD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved	A	A	A	A	A	A	A
Name	Reserved	RESET_SOFT2	RESET_SOFT1	RESET_SOFT	RESET_TC_DBGRESET	RESET_DPSLP_FAULT	RESET_ACT_FAULT	RESET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW1C	RW1C	RW1C	RW1C
HW Access	Reserved				A	A	A	A
Name	Reserved [15:12]				RESET_MCWDT3	RESET_MCWDT2	RESET_MCWDT1	RESET_MCWDT0

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	RESET_MCWDT3	Multi-Counter Watchdog timer reset #3. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
10	RESET_MCWDT2	Multi-Counter Watchdog timer reset #2. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
9	RESET_MCWDT1	Multi-Counter Watchdog timer reset #1. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
8	RESET_MCWDT0	Multi-Counter Watchdog timer reset #0. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
6	RESET_SOFT2	CPU[2] requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
5	RESET_SOFT1	CPU[1] requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0

14.1.69 RES_CAUSE (continued)

4	RESET_SOFT	CPU[0] requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
3	RESET_TC_DBGRESET	Test controller or debugger asserted reset. This asserts low-voltage resets including the debug domain. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
2	RESET_DPSLP_FAULT	Reserved Default Value: 0
1	RESET_ACT_FAULT	Fault logging system requested a reset from its Active logic. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
0	RESET_WDT	A basic WatchDog Timer (WDT) reset has occurred since last power cycle. ULP products: This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). For products that support high-voltage cause detection, this bit blocks recording of other high-voltage cause bits, except RESET_PORVDDD, or *XRES. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. Default Value: 0

14.1.70 RES_CAUSE2

Description: Reset Cause Observation Register 2

Address: 0x42401BD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [23:17]							RESET_CSV_REF

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	RESET_CSV_REF	Clock supervision logic requested a reset due to loss or frequency violation of the reference clock source that is used to monitor the other HF clock sources. Default Value: 0
15 : 0	RESET_CSV_HF	Clock supervision logic requested a reset due to loss or frequency violation of a high-frequency clock. Each bit index K corresponds to a HFCLK. Unimplemented clock bits return zero. Default Value: 0

14.1.71 RES_PXRES_CTL

Description: Programmable XRES Control Register

Address: 0x42401BE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							W1S
HW Access	Reserved							R
Name	Reserved [7:1]							PX-RES_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	PXRES_TRIGGER	Triggers PXRES. This causes a full-scope reset and reboot. Default Value: 0

14.1.72 RES_CAUSE_EXTEND

Description: Extended Reset Cause Observation Register

Address: 0x42401C04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW1C	Reserved	RW1C	RW1C	Reserved	RW1C	RW1C
HW Access	Reserved	A	Reserved	A	A	Reserved	A	A
Name	Reserved	RESET_OVDVCCD	Reserved	RESET_BODVBAT	RESET_BODVCCD	Reserved	RESET_BODVDDD	RESET_XRES

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW1C	RW1C	RW1C	Reserved			
HW Access	Reserved	A	A	A	Reserved			
Name	Reserved	RESET_PORVDDD	RESET_STRUCT_XRES	RESET_PXRES	Reserved [27:24]			

Bits	Name	Description
30	RESET_PORVDDD	Indicator that a POR occurred. This is a high-voltage cause bit, and hardware clears the other bits when this one is set. It does not block further recording of other high-voltage causes. Default Value: 1
29	RESET_STRUCT_XRES	Structural reset was asserted. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD, *XRES, or WDT. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. Default Value: 0
28	RESET_PXRES	PXRES triggered. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD, *XRES, or WDT. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. Default Value: 0
22	RESET_OVDVCCD	Overvoltage detection on the internal core VCCD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD, *XRES, or WDT. Hardware clears this bit during POR. Default Value: 0
20	RESET_BODVBAT	External VBAT supply crossed brown-out limit. Note that this cause will only be observable as long as the VDDD supply does not go below the POR (power on reset) detection limit. Below this limit it is not possible to reliably retain information in the device. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD, *XRES, or WDT. Hardware clears this bit during POR. Default Value: 0

14.1.72 RES_CAUSE_EXTEND (continued)

19	RESET_BODVCCD	Internal VCCD core supply crossed the brown-out limit. Note that this detector will detect gross issues with the internal core supply, but may not catch all brown-out conditions. Functional and timing supervision (CSV, WDT) is provided to create fully failsafe internal crash detection. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD, *XRES, or WDT. Hardware clears this bit during POR. Default Value: 0
17	RESET_BODVDDD	External VDDD supply crossed brown-out limit. Note that this cause will only be observable as long as the VDDD supply does not go below the POR (power on reset) detection limit. Below this limit it is not possible to reliably retain information in the device. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD, *XRES, or WDT. Hardware clears this bit during POR. Default Value: 0
16	RESET_XRES	External XRES pin was asserted. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD, or WDT. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. Default Value: 0

14.1.73 PWR_CBUCK_CTL

Description: Core Buck Control Register

Address: 0x42401C10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			A				
Name	Reserved [7:5]			CBUCK_VSEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			A				
Name	Reserved [15:13]			CBUCK_MODE [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12 : 8	CBUCK_MODE	CBUCK mode. Low ripple (high power) modes are intended for analog that needs low ripple. Low power mode is suitable for digital processing. The CBUCK mode is defined as = {mode*_sr_mode, mode*_sr_hp_submode[1:0], mode*_sr_lp_submode[1:0]} The actual CBUCK mode is the maximum of this setting and the settings of all enabled step-down regulators. 0x11: HP,Hysteretic PFM, High-Low (default Active) 0x01: LP,Hysteretic PFM, High-Low (default DeepSleep) Default Value: 1
4 : 0	CBUCK_VSEL	Voltage output selection. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. The actual CBUCK voltage is the maximum of this setting and the settings for selected mode (see PWR_BUCK_CTL.MODE). These settings follow the formula (0.58+0.02*CBUCK_VSEL). 0: 0.58V, 1: 0.60V, 2: 0.62V, 3: 0.64V, 4: 0.66V, 5: 0.68V, 6: 0.70V, 7: 0.72V, 8: 0.74V, 9: 0.76V, 10: 0.78V, 11: 0.80V, 12: 0.82V, 13: 0.84V, 14: 0.86V, 15: 0.88V, 16: 0.90V, 17: 0.92V, 18: 0.94V, 19: 0.96V, 20: 0.98V, 21: 1.00V, 22: 1.02V, 23: 1.04V, 24: 1.06V, 25: 1.08V, 26: 1.10V, 27: 1.12V, 28: 1.14V, 29: 1.16V, 30: 1.18V, 31: 1.20V. Default Value: 11

14.1.74 PWR_CBUCK_CTL2

Description: Core Buck Control Register 2

Address: 0x42401C14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						CBUCK_PROFILE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW1C	Reserved					
HW Access	R	A	Reserved					
Name	RE-SERVED_CTL	RE-SERVED_CTL2	Reserved [29:24]					

Bits	Name	Description
31	RESERVED_CTL	Reserved. Set to 0. Default Value: 0
30	RESERVED_CTL2	Reserved. Set to 0. Default Value: 0
1 : 0	CBUCK_PROFILE	Selects between CBUCK mode profiles. When CBUCK_USE_SETTING=1, PWR_CBUCK_CTL settings are included in the harmonization and the maximum of the respective mode is used. 00: Mode0: VSEL=0.8V; MODE= HP,Hysteretic PFM, High-Low (17) 01: Mode1: VSEL=0.7V; MODE=17 10: Mode2: VSEL=0.9V; MODE=17 11: Forces the CBUCK to use the settings in PWR_CBUCK_CTL register, ignoring the other hardware requests. This can be used as part of a firmware algorithm to change the voltage of an regulator. This bit is cleared by any reset]. Default Value: 0

14.1.75 PWR_CBUCK_DPSLP_CTL

Description: Core Buck Deepsleep Control Register

Address: 0x42401C1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			A				
Name	Reserved [7:5]			CBUCK_DPSLP_VSEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			A				
Name	Reserved [15:13]			CBUCK_DPSLP_MODE [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	CBUCK_DPSLP_OVERRIDE	Reserved [30:24]						

Bits	Name	Description
31	CBUCK_DPSLP_OVERRIDE	Causes the settings in CBUCK_DPSLP_VSEL and CBUCK_DPSLP_MODE in this register to be used during DEEPSLEEP. Can be used to override the normal hardware voltage behavior of 0.7V and LP, LP,Hysteretic PFM, High-Low (default DeepSleep) Default Value: 0
12 : 8	CBUCK_DPSLP_MODE	CBUCK mode. Low ripple (high power) modes are intended for analog that needs low ripple. Low power mode is suitable for digital processing. The CBUCK mode is defined as = {mode*_sr_mode, mode*_sr_hp_submode[1:0], mode*_sr_lp_submode[1:0]} CBUCK_DPSLP_OVERRIDE=1 will casue these settings to be used during DEEPSLEEP mode. 0x11: HP,Hysteretic PFM, High-Low (default Active) 0x01: LP,Hysteretic PFM, High-Low (default DeepSleep) Default Value: 1
4 : 0	CBUCK_DPSLP_VSEL	Voltage output selection for DEEPSLEEP. CBUCK_DPSLP_OVERRIDE=1 will casue these settings to be used during DEEPSLEEP mode. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. These settings follow the formula (0.58+0.02*CBUCK_VSEL). 0: 0.58V, 1: 0.60V, 2: 0.62V, 3: 0.64V, 4: 0.66V, 5: 0.68V, 6: 0.70V, 7: 0.72V, 8: 0.74V, 9: 0.76V, 10: 0.78V, 11: 0.80V, 12: 0.82V, 13: 0.84V, 14: 0.86V, 15: 0.88V, 16: 0.90V, 17: 0.92V, 18: 0.94V, 19: 0.96V, 20: 0.98V, 21: 1.00V, 22: 1.02V, 23: 1.04V, 24: 1.06V, 25: 1.08V, 26: 1.10V, 27: 1.12V, 28: 1.14V, 29: 1.16V, 30: 1.18V, 31: 1.20V. Default Value: 11

14.1.76 PWR_CBUCK_STATUS

Description: Core Buck Status Register

Address: 0x42401C20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						RW	RW
Name	Reserved [7:2]						SRAM-LDO_SW_ON	SRAM-LDO_DONE

Bits	15	14	13	12	11	10	9	8
SW Access	R	Reserved						R
HW Access	RW	Reserved						RW
Name	MISCLDO_-DONE	Reserved [14:9]						RETLDO_-DONE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved				R		
HW Access	RW	Reserved				RW		
Name	PMU_-DONE	Reserved [30:27]				SR_CUR_MODE [26:24]		

Bits	Name	Description
31	PMU_DONE	Indicates the power management unit is finished with a transition. 0: PMU busy 1: PMU done Default Value: 0
26 : 24	SR_CUR_MODE	Indicates the switching regulator current operating mode Default Value: 0
15	MISCLDO_DONE	Indicates the MISCLDO is finished with a transition. 0: MISCLDO busy 1: MISCLDO done Default Value: 0
8	RETLDO_DONE	Indicates the RETLDO is finished with a transition. 0: RETLDO busy 1: RETLDO done Default Value: 0
1	SRAMLDO_SW_ON	Indicates the state of the SRAMLDO bypass switch 0: SRAMLDO enabled 1: SRAMLDO bypassed Default Value: 0

14.1.76 PWR_CBUCK_STATUS (continued)

0	SRAMLDO_DONE	Indicates the SRAMLDO is finished with a transition. 0: SRAMLDO busy 1: SRAMLDO done Default Value: 0

14.1.77 PWR_RETLDO_CTL

Description: RETLDO Control Register

Address: 0x42401C24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW				
HW Access	Reserved		A	A				
Name	Reserved [7:6]		RET-LDO_GAIN	RETLDO_LVL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW	RW				
HW Access	Reserved		A	A				
Name	Reserved [15:14]		RET-LDO_GAIN_DPSLP	RETLDO_LVL_DPSLP [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
13	RETLDO_GAIN_DPSLP	RETLDO Gain during Deepslp modes 0: 2.00 1: 2.47 Default Value: 0x0

14.1.77 PWR_RETLDO_CTL (continued)

12 : 8	RETLDO_LVL_DPSLP	RETLDO output voltage during DEEPSLEEP modes retldo_gain=0retldo_gain=1 retref_lvlTemp Temp 25C-125CTemp Temp 25C-125C <4:0>-40C-40C 000000.61500.5500.75950.679 000010.62620.5600.77330.691 000100.63740.5700.78710.704 000110.64850.5800.80100.716 001000.65970.5900.81480.728 001010.67090.6000.82860.741 001100.68210.6100.84240.753 001110.69330.6200.85620.765 010000.70450.6300.87000.778 010010.70450.6300.87000.778 010100.70450.6300.87000.778 010110.70450.6300.87000.778 011000.70450.6300.87000.778 011010.70450.6300.87000.778 011100.70450.6300.87000.778 011110.70450.6300.87000.778 100000.43610.3900.53860.481 100010.44730.4000.55240.494 100100.45850.4100.56620.506 100110.46960.4200.58000.519 101000.48080.4300.59380.531 101010.49200.4400.60760.543 101100.50320.4500.62140.556 101110.51440.4600.63520.568 110000.52550.4700.64900.580 110010.53670.4800.66290.593 110100.54790.4900.67670.605 110110.55910.5000.69050.617 111000.57030.5100.70430.630 111010.58150.5200.71810.642 111100.59260.5300.73190.654 111110.60380.5400.74570.667 Default Value: 0x0
5	RETLDO_GAIN	RETLDO Gain During Active mode 0: 2.00 1: 2.47 Default Value: 0x0

14.1.77 PWR_RETLDO_CTL (continued)

4 : 0	RETLDO_LVL	RETLDO output voltage during DEEPSLEEP modes retldo_gain=0retldo_gain=1 retref_lvlTemp Temp 25C-125CTemp Temp 25C-125C <4:0>-40C-40C 000000.61500.5500.75950.679 000010.62620.5600.77330.691 000100.63740.5700.78710.704 000110.64850.5800.80100.716 001000.65970.5900.81480.728 001010.67090.6000.82860.741 001100.68210.6100.84240.753 001110.69330.6200.85620.765 010000.70450.6300.87000.778 010010.70450.6300.87000.778 010100.70450.6300.87000.778 010110.70450.6300.87000.778 011000.70450.6300.87000.778 011010.70450.6300.87000.778 011100.70450.6300.87000.778 011110.70450.6300.87000.778 100000.43610.3900.53860.481 100010.44730.4000.55240.494 100100.45850.4100.56620.506 100110.46960.4200.58000.519 101000.48080.4300.59380.531 101010.49200.4400.60760.543 101100.50320.4500.62140.556 101110.51440.4600.63520.568 110000.52550.4700.64900.580 110010.53670.4800.66290.593 110100.54790.4900.67670.605 110110.55910.5000.69050.617 111000.57030.5100.70430.630 111010.58150.5200.71810.642 111100.59260.5300.73190.654 111110.60380.5400.74570.667 Default Value: 0x0

14.1.78 PWR_SRAMLDO_CTL

Description: SRAMLDO Control Register

Address: 0x42401C28

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW					RW	RW
HW Access	Reserved	A					A	A
Name	Reserved	SRAMLDO_VOUT [6:2]					SRAM-LDO_DPS-LP_EN	SRAM-LDO_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6 : 2	SRAMLDO_VOUT	SRAMLDO output voltage Setting Voltage(V) Setting Voltage(V) 00000 0.58 10000 0.90 00001 0.60 10001 0.92 00001 0.60 10001 0.92 00010 0.62 10010 0.94 00011 0.64 10011 0.96 00100 0.66 10100 0.98 00101 0.68 10101 1.00 00110 0.70 10110 1.02 00111 0.72 10111 1.04 01000 0.74 11000 1.06 01001 0.76 11001 1.08 01010 0.78 11010 1.10 01011 0.80 11011 1.12 01100 0.82 11100 1.14 01101 0.84 11101 1.16 01110 0.86 11110 1.18 01111 0.88 11111 1.20 Default Value: 0xB
1	SRAMLDO_DPSLP_EN	Enable SRAMLDO during deepsleep modes for fast wakeup time versus power savings. Default Value: 0x0

14.1.78 PWR_SRAMLDO_CTL (continued)

0	SRAMLDO_EN	SRAM LDO enable 0: Disabled (switch VCCD->VCCSRAM enabled) 1: Enabled (switch VCCD->VCCSRAM disabled) Default Value: 0x0

14.1.79 PWR_MISCLDO_CTL

Description: MISCLDO Control Register

Address: 0x42401C30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW					RW	RW
HW Access	A	A					A	A
Name	MISCLDO_VCCACT_TRIM	MISCLDO_VOUT [6:2]					MISCLDO_MODE	MISCLDO_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved					A		
Name	Reserved [15:11]					MISCLDO_VCCACT_TRIM [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10 : 7	MISCLDO_VCCACT_TRIM	MISCLDO VCCACT_MISC trim adjustment. Proportional to VCCACT_MISC, numbers below at 0.9V. Setting Adj @0.9V 0111 35mV 0110 30mV 0101 25mV 0100 20mV 0011 15mV 0010 10mV 0001 5mV 0000 0mV 1111 -5mV 1110 -10mV 1110 -10mV 1101 -15mV 1100 -20mV 1011 -25mV 1010 -30mV 1001 -35mV 1000 -40mV Default Value: 0x0

14.1.79 PWR_MISCLDO_CTL (continued)

6 : 2	MISCLDO_VOUT	MISCLDO output voltage Setting Voltage(V) Setting Voltage(V) 00000 0.58 10000 0.90 00001 0.60 10001 0.92 00010 0.62 10010 0.94 00011 0.64 10011 0.96 00100 0.66 10100 0.98 00101 0.68 10101 1.00 00110 0.70 10110 1.02 00111 0.72 10111 1.04 01000 0.74 11000 1.06 01001 0.76 11001 1.08 01010 0.78 11010 1.10 01011 0.80 11011 1.12 01100 0.82 11100 1.14 01101 0.84 11101 1.16 01110 0.86 11110 1.18 01111 0.88 11111 1.20 Default Value: 0x10
1	MISCLDO_MODE	MISCLDO voltage mode 0: MISCLDO output follows VCCACT_MISC 1: MISCLDO output follows miscldo_vout<4:0> Default Value: 0x0
0	MISCLDO_EN	MISCLDO enable Default Value: 0x0

14.1.80 PWR_TRIM_PMU_CTL0

Description: PMU Trim Register 0

Address: 0x42402110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW				
HW Access	A		A	A				
Name	HPBG_CHOP_DELAY [7:6]		HPB-G_DIS_CH OP	LP_BUF_TRIM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	A				A			
Name	HPBG_RCTAT_ADJ [15:12]				HPBG_TRIM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OSC_-CAL_MAN-UAL_4M	OSC_-CAL_MAN-UAL_8M	OSC_-CAL_STAR T	OSC_-CAL_RE-SET	OSC_-CAL_FRE-Q_SEL	OSC4M_-FREQ_SEL	OSC4M_-FORCE_EN	OSC8M_-FORCE_EN

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			A				
Name	Reserved [31:29]			OSC_CAL_CODE_8M [28:24]				

Bits	Name	Description
28 : 24	OSC_CAL_CODE_8M	Manual trim code to apply to 8MHz oscillator. Only used if osc_cal_manual_8M=1. Default Value: 0x0
23	OSC_CAL_MANUAL_4M	Set to use manual cal code for 3.2/4MHz oscillator 0 Use calibration result 1 Use osc_cal_code_4M<4:0> Default Value: 0x0
22	OSC_CAL_MANUAL_8M	Set to use manual cal code for 8MHz oscillator 0 Use calibration result 1 Use osc_cal_code_8M<4:0> Default Value: 0x0
21	OSC_CAL_START	Start oscillator calibration Default Value: 0x0
20	OSC_CAL_RESET	Reset osc cal codes and cal_done signal Default Value: 0x0
19	OSC_CAL_FREQ_SEL	Select oscillator to calibrate 0: 8MHz 1: 3.2M/4MHz Default Value: 0x0

14.1.80 PWR_TRIM_PMU_CTL0 (continued)

18	OSC4M_FREQ_SEL	PWM oscillator frequency select 0: 4.0MHz 1 : 3.2MHz Default Value: 0x1
17	OSC4M_FORCE_EN	3.2/4MHz (PWM) oscillator enable - use for Calibration 0: Auto (powerup when used) 1: Enabled (3.2/4MHz always on) Default Value: 0x0
16	OSC8M_FORCE_EN	8MHz oscillator enable - use for Calibration 0: Auto (powerup when used) 1: Enabled (8MHz always on) Default Value: 0x0
15 : 12	HPBG_RCTAT_ADJ	High power bandgap adjust for 0TC (TTTT,50C) Default Value: 0x0
11 : 8	HPBG_TRIM	High power bandgap reference voltage trim Setting VOUT @1.16V VOUT % 0111 41mV +3.4% 0110 35mV +2.9% 0101 29mV +2.4% 0100 23mV +1.9% 0011 18mV +1.5% 0010 12mV +1.0% 0001 6mV +0.5% 0000 0mV 0.0% 1111 -5mV -0.4% 1110 -11mV -1.0% 1101 -16mV -1.4% 1100 -22mV -1.9% 1011 -27mV -2.4% 1010 -32mV -2.8% 1001 -38mV -3.4% 1000 -43mV -3.9% Default Value: 0x0
7 : 6	HPBG_CHOP_DELAY	HPBG chopping delay Setting Delay 00 16us 01 32us 10 64us 11 128us Default Value: 0x0
5	HPBG_DIS_CHOP	HPBG disable chop Default Value: 0x0
4 : 0	LP_BUF_TRIM	LP buffer voltage trim, 2's compliment format Setting Vref(V) Setting Vref(V) 00000 0.600 10000 0.520 (-13.3%) 00001 0.605 (+0.83%) 10001 0.525 (-12.5%) 00010 0.610 (+1.67%) 10010 0.530 (-11.7%) 00011 0.615 (+2.50%) 10011 0.535 (-10.8%) 00100 0.620 (+3.33%) 10100 0.540 (-10.0%) 00101 0.625 (+4.17%) 10101 0.545 (-9.17%) 00110 0.630 (+5.00%) 10110 0.550 (-8.33%) 00111 0.635 (+5.83%) 10111 0.555 (-7.50%) 01000 0.640 (+6.67%) 11000 0.560 (-6.67%) 01001 0.645 (+7.50%) 11001 0.565 (-5.83%) 01010 0.650 (+8.33%) 11010 0.570 (-5.00%) 01011 0.655 (+9.17%) 11011 0.575 (-4.17%) 01100 0.660 (+10.0%) 11100 0.580 (-3.33%) 01101 0.665 (+10.8%) 11101 0.585 (-2.50%) 01110 0.670 (+11.7%) 11110 0.590 (-1.67%) 01111 0.675 (+12.5%) 11111 0.595 (-0.83%) Default Value: 0x0

14.1.81 CLK_TRIM_ECO_CTL

Description: ECO Trim Register

Address: 0x42403020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [7:5]			ECO_CTRL_CPBOOST	Reserved [3:1]			ECO_CTRL_IBOOSTEN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							ECO_CTRL_WDBOOST

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW		RW	
HW Access	R				R		R	
Name	ECO_TRIM_IREF [23:20]				ECO_TRIM_WDHYST [19:18]		ECO_TRIM_FBK [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							ECO_TRIM_IREF

Bits	Name	Description
24 : 20	ECO_TRIM_IREF	Current bias trim input pin Default Value: 0x8
19 : 18	ECO_TRIM_WDHYST	Watchdog hysteresis trim Default Value: 0
17 : 16	ECO_TRIM_FBK	Feedback resistance trim Default Value: 0
8	ECO_CTRL_WDBOOST	Watchdog trim Default Value: 0
4	ECO_CTRL_CPBOOST	Amplitude trim Default Value: 0
0	ECO_CTRL_IBOOSTEN	Current boost enable input pin Default Value: 0

14.1.82 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL

Description: DPLL LP Trim Register

Address: 0x42403200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SAR_CYCLE_STOP_FAST [7:4]				SAR_CYCLE_STOP_COLD [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW			Reserved	RW	RW	RW
HW Access	Reserved	R			Reserved	R	R	R
Name	Reserved	LDO_DCO_TRIM [14:12]			Reserved	PLL_SAR_FSM_EN	SAR_DIS_-FAST	SAR_DIS_COLD

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW			Reserved	RW	
HW Access	R		R			Reserved	R	
Name	PLL_FRAC_ORDER [23:22]		LDO_PERI_TRIM [21:19]			Reserved	PLL_DCO_SD_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						RW
HW Access	R	R						R
Name	EN-ABLE_CNT	ISOLATE_CNT [30:25]						ISOLATE_N

Bits	Name	Description
31	ENABLE_CNT	Enable for the PLL hardware sequencer. 0: Disables the hardware sequencer. When disabling the PLL, first deselect it using .BYPASS_-SEL=PLL_REF, wait at least six PLL clock cycles, and then disable it with .ENABLE=0. Before entering DEEPSLEEP, firmware must switch to another clock source and disable the PLL. 1: Enables the hardware sequencer. The sequencer handles all PLL enable/disable transitions, including around DEEPSLEEP entry/exit. Default Value: 1
30 : 25	ISOLATE_CNT	Terminal count for the stabilization counter handles PLL_ISOLATE_N Default Value: 0x7
24	ISOLATE_N	Manual isolation control for PLL . This field is ignored when ENABLE_CNT==1. When controlling manually, de-assert >= 3us after ENABLE=1. Assertion can happen in cycle just before EN-ABLE=0. 0: Isolate outputs 1: Do not isolate outputs Default Value: 0
23 : 22	PLL_FRAC_ORDER	Order of the delta-sigma modulator used for fractional mode. 00: 4th order 01: 3rd order 10: 2nd order 11: 1st order Default Value: 0x3

14.1.82 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL (continued)

21 : 19	LDO_PERI_TRIM	pll ldo peripheri voltage trim 0 0.906V 1 0.786V 2 0.846V 3 0.876V 4 0.936V 5 0.966V 6: 0.995V 7: 1.05V Default Value: 0
17 : 16	PLL_DCO_SD_SEL	00': disable, '01' first order SigmaDelta enabled;'10' third order SigmaDelta enabled;'11' Sigma delta first order enable - with dco_clk/4 Default Value: 0
14 : 12	LDO_DCO_TRIM	Trim for PLL local regulator for DCO 0 0.906V 1 0.786V 2 0.846V 3 0.876V 4 0.936V 5 0.966V 6: 0.995V 7: 1.05V Default Value: 0
10	PLL_SAR_FSM_EN	SAR FSM enable. Always set to 1 for functional mode. This register was kept in the design (and moved to hidden trim register) to increase coverage on the hard IP, and could be removed once the hard IP input is removed. Default Value: 0x1
9	SAR_DIS_FAST	Disable Successive Approximation Register during locking for fast lock, used when code write=1. 0: Use SAR. 1: Disable SAR. Default Value: 0
8	SAR_DIS_COLD	Disable Successive Approximation Register during locking for cold lock, used when code write=0. 0: Use SAR. 1: Disable SAR. Default Value: 0
7 : 4	SAR_CYCLE_STOP_-FAST	Successive Approximation Register (SAR) configuration for fast lock, used when code write=1. Ignored when SAR_DIS==1. 0x1...0xB: Number of cycles until SAR stops. others: illegal Default Value: 0x1
3 : 0	SAR_CY-CLE_STOP_COLD	Successive Approximation Register (SAR) configuration for cold lock, used when code write=0. Ignored when SAR_DIS==1. 0x1...0xB: Number of cycles until SAR stops. others: illegal Default Value: 0x3

14.1.83 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL3

Description: DPLL LP Trim Register 3

Address: 0x42403208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PHASE_ACC_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							PHASE_ACC_CNT

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PHASE_ACC_CNT_SSCG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							PHASE_ACC_CNT_SSCG

Bits	Name	Description
24 : 16	PHASE_ACC_CNT_SS-CG	counter for phase accelerate cycles during PLL wakeup SSCG mode Optimal settings: 4 --> 5 MHz: 127 5-->6 MHz: 157 6-->7 MHz: 187 7-->8 MHz: 217 8-->9 MHz: 248 9-->10 MHz: 279 Default Value: 0x1
8 : 0	PHASE_ACC_CNT	counter for phase accelerate cycles during PLL wakeup for INT and FRAC modes Optimal settings: 4 --> 5 MHz: 127 5-->6 MHz: 157 6-->7 MHz: 187 7-->8 MHz: 217 8-->9 MHz: 255 9-->10 MHz: 286 Default Value: 0x7F

14.1.84 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL4

Description: DPLL LP Trim Register 4

Address: 0x4240320C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				Reserved		RW	
HW Access	R				Reserved		R	
Name	LOCK_WAIT_RISE_COLD [7:4]				Reserved [3:2]		LOCK_WAIT_FALL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				LOCK_WAIT_RISE_COLD [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	LOCK_WAIT_RISE_FAST [23:20]				Reserved [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				LOCK_WAIT_RISE_FAST [27:24]			

Bits	Name	Description
27 : 20	LOCK_WAIT_RISE_FAST	Wait time from when static phase error is within the lock window until lock signal asserts, for fast lock, used when code write=1. 0: Illegal 1: 1 PFD clocks 2: 2 PFD clocks ... 255: 255 PFD clocks Optimal settings f, MHz Wait Time, clocks --------- ---------- 4-->5 16 5-->6 17 6-->7 16 7-->8 13 8-->9 17 9-->10 21 Default Value: 0x3

14.1.84 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL4 (continued)

11 : 4	LOCK_WAIT_RISE_COLD	Wait time from when static phase error is within the lock window until lock signal asserts, for cold lock, used when code write=0. 0: Illegal 1: 1 PFD clocks 2: 2 PFD clocks ... 255: 255 PFD clocks Optimal settings f, MHz Wait Time, clocks --------- ---------- 4-->5 53 5-->6 73 6-->7 85 7-->8 91 8-->9 104 9-->10 117 Notes: For initial DPLL locking or when DPLL Fast Lock is disabled (PLL_DIS_FAST_LOCK=1), user must program DPLL_CTL4.LOCK_WAIT_RISE using appropriate value for "Without Code Write" for corresponding frequency range. Default Value: 0x8
1 : 0	LOCK_WAIT_FALL	Wait time from when static phase error is within the lock window until lock signal asserts. 0: 0 PFD clocks 1: 2 PFD clocks 2: 3 PFD clocks 3: 4 PFD clocks Default Value: 0

14.1.85 CLK_TRIM_DPLL_LP0_DPLL_LP_TEST4

Description: DPLL LP Test Register 4

Address: 0x4240321C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	PLL_USER_DCO_CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	Reserved			RW		
HW Access	A	R	Reserved			A		
Name	PLL_READ_EN	PLL_DIS_-FAST_LOCK	Reserved [13:11]			PLL_USER_DCO_CODE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	Reserved	RW					
HW Access	R	Reserved	R					
Name	PHASE_ACC_US-ER_WRITE_FRACT	Reserved	PHASE_ACC_USER_WRITE_INT [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [31:29]			PHASE_ACC_USER_WRITE_FRACT [28:24]				

Bits	Name	Description
28 : 23	PHASE_ACC_US-ER_WRITE_FRACT	reduce KI,KP coefficient during PLL deepsleep wakeup fract. Default Value: 0x10
21 : 16	PHASE_ACC_US-ER_WRITE_INT	Reduce KI,KP coefficient during PLL deepsleep wakeup integer. Default Value: 0x10
15	PLL_READ_EN	This bit is a self clear bit. The FW writes 1 to get an updated value in PLL_USER_D-CO_CODE.HW will self clear this bit to indicate that the PLL_USER_DCO_CODE be read. Default Value: 0
14	PLL_DIS_FAST_LOCK	0: Enables DPLL Fast Lock 1: Disables DPLL Fast Lock When PLL_DIS_FAST_LOCK=0, if DPLL successfully locks prior to a DEEPSLEEP entry: - HW will read the DCO code before DEEPSLEEP entry, then write the DCO code upon DEEP-SLEEP exit, to reduce DPLL lock time. - FW must follow the procedure described under DPLL_LP_CTL4.LOCK_WAIT_RISE Notes: 2 Default Value: 0
10 : 0	PLL_USER_DCO_CODE	FW can read the code saved by the DPLL before deepsleep.Use PLL_READ_EN to get updated DCO_CODE from the DPLL: To read properly please refer to PLL_USER_D-CO_CODE_RD_EN/PLL_READ_EN. Before any read, FW should check first that PLL_READ_EN is 0. To account for Clock Domain Crossings, FW should wait at least 3 CLK_IMO cycles (3*125ns=375ns) between SW write and SW read operation. Default Value: 0

14.1.86 RAM_TRIM_TRIM_RAM_CTL0

Description: Trim Register for RAM Type 0

Address: 0x42404000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	TRIM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	TRIM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	TRIM [31:24]							

Bits	Name	Description
31 : 0	TRIM	Trim value for RAM Type 0 Default Value: 1859

14.1.87 RAM_TRIM_TRIM_RAM_CTL2

Description: Trim Register for RAM Type 0

Address: 0x42404008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	TRIM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	TRIM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	TRIM [31:24]							

Bits	Name	Description
31 : 0	TRIM	Trim value for RAM Type 0 Default Value: 1540

14.1.88 RAM_TRIM_TRIM_RAM_CTL6

Description: Trim Register for RAM Type 0

Address: 0x42404018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	TRIM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	TRIM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	TRIM [31:24]							

Bits	Name	Description
31 : 0	TRIM	Trim value for RAM Type 0 Default Value: 557

14.1.89 RAM_TRIM_TRIM_RAM_CTL8

Description: Trim Register for RAM Type 0

Address: 0x42404020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	TRIM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	TRIM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	TRIM [31:24]							

Bits	Name	Description
31 : 0	TRIM	Trim value for RAM Type 0 Default Value: 11

14.1.90 WDT_CTL

Description: Watchdog Counter Control Register (Type A)

Address: 0x4240C000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW		Reserved			RW
HW Access	Reserved		A		Reserved			A
Name	Reserved [7:6]		WDT_CLK_SEL [5:4]		Reserved [3:1]			WDT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		Reserved					
HW Access	A		Reserved					
Name	WDT_LOCK [31:30]		Reserved [29:24]					

Bits	Name	Description
31 : 30	WDT_LOCK	Prohibits writing to WDT_*, CLK_ILO_CONFIG, CLK_SELECT.LFCLK_SEL, and CLK_TRIM_ILO_CTL registers when not equal 0. Requires at least two different writes to unlock. A change in WDT_LOCK takes effect beginning with the next write cycle. Note that this field is 2 bits to force multiple writes only. It represents only a single write protect signal protecting all those registers at the same time. WDT will lock on any reset. This field is not retained during DEEPSLEEP or HIBERNATE mode, so the WDT will be locked after wakeup from these modes. Default Value: 3 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0 **0x2: CLR1 :** Clears bit 1 **0x3: SET01 :** Sets both bits 0 and 1

14.1.90 WDT_CTL (continued)

5 : 4	WDT_CLK_SEL	Select source for WDT. Not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Writes to this field are ignored unless the WDT is unlock using WDT_LOCK register. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 1 **0x0: ILO :** ILO - Internal Low-speed Oscillator, if present. With this option selected, ILO reset is suppressed in Hibernate mode. **0x1: PILO :** PILO - Precision ILO. If present. With this option selected, PILO reset is suppressed in Hibernate mode. **0x2: RTC :** RTC - Selected clk_rtc source, if present. This choice is not recommended for applications that rely upon the watchdog timer for safety or security, unless the product supports clock supervision of clk_rtc (CSV_RTC). Generation of clk_rtc is not protected by WDT_LOCK and is in a different memory region with potentially different security attributes.
0	WDT_EN	Enable this watchdog timer. This field is retained during DEEPSLEEP and HIBERNATE modes. Default Value: 1

14.1.91 WDT_CNT

Description: Watchdog Counter Count Register (Type A)

Address: 0x4240C004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW					
HW Access	Reserved		A					
Name	Reserved [23:22]		COUNTER [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 0	COUNTER	Current value of WDT Counter. The write feature of this register is for verification purpose, have no synchronization, and can only be applied when the WDT is fully off. When writing, the value is updated immediately in the WDT counter, but it will read back as the old value until this register resynchronizes just after the negedge of selected WDT clock. Writes will be ignored if they occur when the WDT is enabled. Default Value: 0

14.1.92 WDT_MATCH

Description: Watchdog Counter Match Register (Type A)

Address: 0x4240C008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW					
HW Access	Reserved		A					
Name	Reserved [23:22]		MATCH [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 0	MATCH	Match value for Watchdog counter. Every time WDT_COUNTER reaches MATCH an interrupt is generated. Two unserviced interrupts will lead to a system reset (i.e. at the third match). Default Value: 4096

14.1.93 WDT_MATCH2

Description: Watchdog Counter Match Register 2 (Type A)

Address: 0x4240C00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			A				
Name	Reserved [7:5]			IGNORE_BITS_ABOVE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	IGNORE_BITS_ABOVE	The number of bits to be considered for matching starting from LSb of the register. Bit indices above this setting are NOT checked against MATCH. This value provides control over the time-to-reset of the watchdog (which happens after 3 successive matches). The four LSBs cannot be ignored for matching. Settings <3 behave like a setting of 3. If the setting is higher than the number of bits in the WDT counter, all actual bits in the counter are matched. Default Value: 31

14.1.94 MCWDT_CNTLOW0

Description: Multi-Counter Watchdog Sub-counters 0/1

Address: 0x4240D004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WDT_CTR0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WDT_CTR0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WDT_CTR1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WDT_CTR1 [31:24]							

Bits	Name	Description
31 : 16	WDT_CTR1	Current value of sub-counter 1 for this MCWDT. Software writes are ignored when the sub-counter is enabled Default Value: 0
15 : 0	WDT_CTR0	Current value of sub-counter 0 for this MCWDT. Software writes are ignored when the sub-counter is enabled. Default Value: 0

14.1.95 MCWDT_CNTHIGH0

Description: Multi-Counter Watchdog Sub-counter 2

Address: 0x4240D008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [31:24]							

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of sub-counter 2 for this MCWDT. Software writes are ignored when the sub-counter is enabled Default Value: 0

14.1.96 MCWDT_MATCH0

Description: Multi-Counter Watchdog Counter Match Register

Address: 0x4240D00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [31:24]							

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for sub-counter 1 of this MCWDT Default Value: 0
15 : 0	WDT_MATCH0	Match value for sub-counter 0 of this MCWDT Default Value: 0

14.1.97 MCWDT_CONFIG0

Description: Multi-Counter Watchdog Counter Configuration

Address: 0x4240D010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	WDT_-MATCH0_1	WDT_CAR-RY0_1	WDT_LOWER_MODE0 [5:4]		WDT_CAS-CADE0_1	WDT_-CLEAR0	WDT_MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	WDT_-MATCH1_2	WDT_CAR-RY1_2	WDT_LOWER_MODE1 [13:12]		WDT_CAS-CADE1_2	WDT_-CLEAR1	WDT_MODE1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							WDT_-MODE2

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [31:29]			WDT_BITS2 [28:24]				

Bits	Name	Description
28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert after bit0 of WDT_CTR2 toggles (one int every tick) ... 31: Assert after bit31 of WDT_CTR2 toggles (one int every 2^31 ticks) Default Value: 0
16	WDT_MODE2	Watchdog Counter 2 Mode. Default Value: 0 **0x0: NOTHING :** Free running counter with no interrupt requests **0x1: INT :** Free running counter with interrupt request that occurs one LFCLK cycle after the specified bit in CTR2 toggles (see WDT_BITS2).
15	WDT_MATCH1_2	Specifies matching behavior when WDT_CASCADE1_2==1. When WDT_CASCADE1_2==0, this bit is not used and match is based on counter 2 alone. 0: Match based on counter 2 alone. 1: Match based on counter 2 and counter 1 matching simultaneously. Default Value: 0

14.1.97 MCWDT_CONFIG0 (continued)

14	WDT_CARRY1_2	Carry out behavior that applies when WDT_CASCADE1_2==1. This bit is not used when WDT_-CASCADE1_2==0. 0: carry out on counter 1 match. 1: carry out on counter 1 roll-over. Default Value: 0
13 : 12	WDT_LOWER_MODE1	Watchdog Counter Action on service before lower limit. The lower limit action for counter 1 is ignored if this counter is cascaded into counter 2 (WDT_CASCADE1_2 = 1) Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset
11	WDT_CASCADE1_2	Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_-MATCH1. It is allowed to cascade all three WDT counters. 0: Independent counters 1: Cascaded counters. When cascading all three counters, WDT_CLEAR1 must be 1. Default Value: 0
10	WDT_CLEAR1	Clear Watchdog Counter when WDT_CTR1==WDT_MATCH1. In other words WDT_CTR1 divides LFCLK by (WDT_MATCH1+1). 0: Free running counter 1: Clear on match. In this mode, the minimum legal setting of WDT_MATCH1 is 1. Default Value: 0
9 : 8	WDT_MODE1	Watchdog Counter Action on Match. Action is taken on the next increment after the values match (WDT_CTR1=WDT_MATCH1). Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset **0x3: INT_THEN_RESET :** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt
7	WDT_MATCH0_1	Specifies matching behavior when WDT_CASCADE0_1==1. When WDT_CASCADE0_1==0, this bit is not used and match is based on counter 1 alone. 0: Match based on counter 1 alone. 1: Match based on counter 1 and counter 0 matching simultaneously. Default Value: 0

14.1.97 MCWDT_CONFIG0 (continued)

6	WDT_CARRY0_1	Carry out behavior that applies when WDT_CASCADE0_1==1. This bit is not used when WDT_-CASCADE0_1==0. 0: carry out on counter 0 match. 1: carry out on counter 0 roll-over. Default Value: 0
5 : 4	WDT_LOWER_MODE0	Watchdog Counter Action on service before lower limit. Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset
3	WDT_CASCADE0_1	Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_-MATCH0. 0: Independent counters 1: Cascaded counters Default Value: 0
2	WDT_CLEAR0	Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 divides LFCLK by (WDT_MATCH0+1). 0: Free running counter 1: Clear on match. In this mode, the minimum legal setting of WDT_MATCH0 is 1. Default Value: 0
1 : 0	WDT_MODE0	Watchdog Counter Action on Match. Action is taken on the next increment after the values match (WDT_CTR0=WDT_MATCH0). Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset **0x3: INT_THEN_RESET :** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt

14.1.98 MCWDT_CTL0

Description: Multi-Counter Watchdog Counter Control

Address: 0x4240D014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1S	Reserved	R	RW
HW Access	Reserved				RW0C	Reserved	RW	R
Name	Reserved [7:4]				WDT_RESET0	Reserved	WDT_ENABLED0	WDT_ENABLE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW1S	Reserved	R	RW
HW Access	Reserved				RW0C	Reserved	RW	R
Name	Reserved [15:12]				WDT_RESET1	Reserved	WDT_ENABLED1	WDT_ENABLE1

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW1S	Reserved	R	RW
HW Access	Reserved				RW0C	Reserved	RW	R
Name	Reserved [23:20]				WDT_RESET2	Reserved	WDT_ENABLED2	WDT_ENABLE2

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to two LFCLK cycles. Default Value: 0
16	WDT_ENABLE2	Enable subcounter 2. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0
11	WDT_RESET1	Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0
9	WDT_ENABLED1	Indicates actual state of counter. May lag WDT_ENABLE1 by up to two LFCLK cycles. Default Value: 0
8	WDT_ENABLE1	Enable subcounter 1. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0
3	WDT_RESET0	Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0

14.1.98 MCWDT_CTL0 (continued)

1	WDT_ENABLED0	Indicates actual state of counter. May lag WDT_ENABLE0 by up to two LFCLK cycles. Default Value: 0
0	WDT_ENABLE0	Enable subcounter 0. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0

14.1.99 MCWDT_INTR0

Description: Multi-Counter Watchdog Counter Interrupt Register

Address: 0x4240D018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1C	RW1C	RW1C
HW Access	Reserved					A	A	A
Name	Reserved [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	MCWDT_INT2	MCWDT Interrupt Request for sub-counter 2. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE2=3. Default Value: 0
1	MCWDT_INT1	MCWDT Interrupt Request for sub-counter 1. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE1=3. Default Value: 0
0	MCWDT_INT0	MCWDT Interrupt Request for sub-counter 0. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE0=3. Default Value: 0

14.1.100 MCWDT_INTR_SET0

Description: Multi-Counter Watchdog Counter Interrupt Set Register

Address: 0x4240D01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1S	RW1S	RW1S
HW Access	Reserved					A	A	A
Name	Reserved [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Set interrupt for MCWDT_INT2 Default Value: 0
1	MCWDT_INT1	Set interrupt for MCWDT_INT1 Default Value: 0
0	MCWDT_INT0	Set interrupt for MCWDT_INT0 Default Value: 0

14.1.101 MCWDT_INTR_MASK0

Description: Multi-Counter Watchdog Counter Interrupt Mask Register

Address: 0x4240D020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Mask for sub-counter 2. This controls if the interrupt is forwarded to the CPU. 0: Interrupt is masked (not forwarded). 1: Interrupt is forwarded. Default Value: 0
1	MCWDT_INT1	Mask for sub-counter 1. This controls if the interrupt is forwarded to the CPU. 0: Interrupt is masked (not forwarded). 1: Interrupt is forwarded. Default Value: 0
0	MCWDT_INT0	Mask for sub-counter 0. This controls if the interrupt is forwarded to the CPU. 0: Interrupt is masked (not forwarded). 1: Interrupt is forwarded. Default Value: 0

14.1.102 MCWDT_INTR_MASKED0

Description: Multi-Counter Watchdog Counter Interrupt Masked Register

Address: 0x4240D024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R	R	R
HW Access	Reserved					RW	RW	RW
Name	Reserved [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Logical and of corresponding request and mask bits. Default Value: 0
1	MCWDT_INT1	Logical and of corresponding request and mask bits. Default Value: 0
0	MCWDT_INT0	Logical and of corresponding request and mask bits. Default Value: 0

14.1.103 MCWDT_LOCK0

Description: Multi-Counter Watchdog Counter Lock Register

Address: 0x4240D028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		Reserved					
HW Access	A		Reserved					
Name	MCWDT_LOCK [31:30]		Reserved [29:24]					

Bits	Name	Description
31 : 30	MCWDT_LOCK	Prohibits writing control and configuration registers related to this MCWDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. Each MCWDT has a separate local lock. LFCLK settings are locked by the global WDT_LOCK register, and this register has no effect on that. Default Value: 0 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0 **0x2: CLR1 :** Clears bit 1 **0x3: SET01 :** Sets both bits 0 and 1

14.1.104 MCWDT_LOWER_LIMIT0

Description: Multi-Counter Watchdog Counter Lower Limit Register

Address: 0x4240D02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_LOWER_LIMIT0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_LOWER_LIMIT0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_LOWER_LIMIT1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_LOWER_LIMIT1 [31:24]							

Bits	Name	Description
31 : 16	WDT_LOWER_LIMIT1	Lower limit for sub-counter 1 of this MCWDT Default Value: 0
15 : 0	WDT_LOWER_LIMIT0	Lower limit for sub-counter 0 of this MCWDT Default Value: 0

14.1.105 PERI_PCLK1_GR1_DIV_CMD

Description: Divider command

Address: 0x44042000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DIV_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PA_DIV_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved				RW	
HW Access	RW1C	RW1C	Reserved				R	
Name	ENABLE	DISABLE	Reserved [29:26]				PA_TYPE_SEL [25:24]	

Bits	Name	Description
31	ENABLE	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The DIV_SEL and TYPE_SEL fields specify which divider is to be enabled. The enabled divider may be phase aligned to either "clk_pclk_root[i]" (typical usage) or to ANY enabled divider. The PA_DIV_SEL and PA_TYPE_SEL fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of "clk_pclk_root[i]"/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to "clk_pclk_root[i]" takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. Default Value: 0

14.1.105 PERI_PCLK1_GR1_DIV_CMD (continued)

30	DISABLE	Clock divider disable command (mutually exclusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The DIV_SEL and TYPE_SEL fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. Default Value: 0
25 : 24	PA_TYPE_SEL	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
23 : 16	PA_DIV_SEL	(PA_TYPE_SEL, PA_DIV_SEL) specifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_DIV_SEL is "255" and PA_TYPE_SEL is "3", "clk_pclk_root[i]" is used as reference. Default Value: 255
9 : 8	TYPE_SEL	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
7 : 0	DIV_SEL	(TYPE_SEL, DIV_SEL) specifies the divider on which the command (DISABLE/ENABLE) is performed. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock signal(s) are generated. Default Value: 255

14.1.106 PERI_PCLK1_GR1_CLOCK_CTL0

Description: Clock control

Address: 0x44042C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						DIV_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 8	TYPE_SEL	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
1 : 0	DIV_SEL	Specifies one of the dividers of the divider type specified by TYPE_SEL. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out-of-phase dividers, spurious clock control signals may be generated for one "clk_pclk_root[i]" cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (DIV_SEL is "255" and TYPE_SEL is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 3

14.1.107 PERI_PCLK1_GR1_DIV_16_5_CTL0

Description: Divider control (for 16.5 divider)

Address: 0x44043800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					Reserved		R
HW Access	R					Reserved		RW
Name	FRAC5_DIV [7:3]					Reserved [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_pclk_-root[i]" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

14.1.108 PERI_PCLK1_GR2_CLOCK_CTL0

Description: Clock control

Address: 0x44044C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						DIV_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 8	TYPE_SEL	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
1 : 0	DIV_SEL	Specifies one of the dividers of the divider type specified by TYPE_SEL. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out-of-phase dividers, spurious clock control signals may be generated for one "clk_pclk_root[i]" cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (DIV_SEL is "255" and TYPE_SEL is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 3

14.1.109 PERI_PCLK1_GR2_DIV_8_CTL0

Description: Divider control (for 8.0 divider)

Address: 0x44045000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 256]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 256]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

15 Real-Time Clock (RTC) registers

This section discusses the RTC registers. It lists all the registers in mapping tables, in address order.

15.1 Register details

Register name	Address	Description
RTC_RTC_RW	0x42420008	RTC Read Write register
RTC_CAL_CTL	0x4242000C	Oscillator calibration for absolute frequency
RTC_STATUS	0x42420010	Status
RTC_RTC_TIME	0x42420014	Calendar Seconds, Minutes, Hours, Day of Week
RTC_RTC_DATE	0x42420018	Calendar Day of Month, Month, Year
RTC_ALM1_TIME	0x4242001C	Alarm 1 Seconds, Minute, Hours, Day of Week
RTC_ALM1_DATE	0x42420020	Alarm 1 Day of Month, Month
RTC_ALM2_TIME	0x42420024	Alarm 2 Seconds, Minute, Hours, Day of Week
RTC_ALM2_DATE	0x42420028	Alarm 2 Day of Month, Month
RTC_INTR	0x4242002C	Interrupt request register
RTC_INTR_SET	0x42420030	Interrupt set request register
RTC_INTR_MASK	0x42420034	Interrupt mask register
RTC_INTR_MASKED	0x42420038	Interrupt masked request register
RTC_RESET	0x42420048	RTC reset register
RTC_BREG_SET00	0x42421000	Backup register region 0
RTC_BREG_SET01	0x42421004	Backup register region 0. See RTC_BREG_SET00 for the details of bit fields.
RTC_BREG_SET02	0x42421008	Backup register region 0. See RTC_BREG_SET00 for the details of bit fields.
RTC_BREG_SET03	0x4242100C	Backup register region 0. See RTC_BREG_SET00 for the details of bit fields.
RTC_BREG_SET10	0x42421010	Backup register region 1
RTC_BREG_SET11	0x42421014	Backup register region 1. See RTC_BREG_SET10 for the details of bit fields.
RTC_BREG_SET12	0x42421018	Backup register region 1. See RTC_BREG_SET10 for the details of bit fields.
RTC_BREG_SET13	0x4242101C	Backup register region 1. See RTC_BREG_SET10 for the details of bit fields.
RTC_BREG_SET20	0x42421020	Backup register region 2
RTC_BREG_SET21	0x42421024	Backup register region 2. See RTC_BREG_SET20 for the details of bit fields.
RTC_BREG_SET22	0x42421028	Backup register region 2. See RTC_BREG_SET20 for the details of bit fields.
RTC_BREG_SET23	0x4242102C	Backup register region 2. See RTC_BREG_SET20 for the details of bit fields.

Real-Time Clock (RTC) registers

Register name	Address	Description
RTC_BREG_SET24	0x42421030	Backup register region 2. See RTC_BREG_SET20 for the details of bit fields.
RTC_BREG_SET25	0x42421034	Backup register region 2. See RTC_BREG_SET20 for the details of bit fields.
RTC_BREG_SET26	0x42421038	Backup register region 2. See RTC_BREG_SET20 for the details of bit fields.
RTC_BREG_SET27	0x4242103C	Backup register region 2. See RTC_BREG_SET20 for the details of bit fields.

15.1.1 RTC_RTC_RW

Description: RTC Read Write register

Address: 0x42420008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						A	A
Name	Reserved [7:2]						WRITE	READ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	WRITE	Write bit Only when this bit is set can the RTC registers be written to (otherwise writes are ignored). This bit cannot be set if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Read bit is set or getting set. The user writes to the RTC user registers, when the Write bit is cleared by the user then the user registers content is copied to the actual RTC registers. Only user RTC registers that were written to will get copied, others will not be affected. When the SECONDS field is updated then TICKS will also be reset (WDT is not affected). When the Write bit is cleared by a reset (brown out/DeepSleep) then the RTC update will be ignored/lost. Do not set the Write bit if the RTC if the RTC is still busy with a previous update (see RTC_BUSY). Do not set the Write bit at the same time that the Read bit is cleared. Default Value: 0
0	READ	Read bit When this bit is set the RTC registers will be copied to user registers and frozen so that a coherent RTC value can safely be read. The RTC will keep on running. Do not set the read bit if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Write bit is set. Do not set the Read bit at the same time that the Write bit is cleared. Default Value: 0

15.1.2 RTC_CAL_CTL

Description: Oscillator calibration for absolute frequency

Address: 0x4242000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW					
HW Access	Reserved	A	A					
Name	Reserved	CALIB_-SIGN	CALIB_VAL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	
HW Access	Reserved						A	
Name	Reserved [23:18]						CAL_COMP_PER_MIN [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved	RW		Reserved			
HW Access	A	Reserved	A		Reserved			
Name	CAL_OUT	Reserved	CAL_SEL [29:28]		Reserved [27:24]			

Bits	Name	Description
31	CAL_OUT	Output enable for wave signal for calibration. This allows calibration wave to be used to calculate required CALIB_VAL to be written. Default Value: 0
29 : 28	CAL_SEL	Select calibration wave output signal Default Value: 0 **0x0: CAL512 :** 512Hz wave, not affected by calibration setting (not supported for 50/60Hz input clock: CTL.PRESCALER!=0) **0x1: RESERVED :** reserved **0x2: CAL2 :** 2Hz wave, includes the effect of the calibration setting, (not supported for 50/60Hz input clock: CTL.PRESCALER!=0) **0x3: CAL1 :** 1Hz wave, includes the effect of the calibration setting (supported for all input clocks)

15.1.2 RTC_CAL_CTL (continued)

17 : 16	CAL_COMP_PER_MIN	Select how many time calibration is performed per minute per step of 64 , each time a 64 step is added or substracted one unit 2/4/8/16*CALIB_VAL is substracted. Default Value: 0 **0x0: 2 :** Calibration of 64 each is performed twice per minute for 2*CALIB_VAL per hour **0x1: 4 :** Calibration of 64 each is performed four times per minute for 2*CALIB_VAL per hour **0x2: 8 :** Calibration of 64 each is performed eight times per minute for 2*CALIB_VAL per hour **0x3: 16 :** Ca6libration of 64 each is performed sixteen times per minute for 2*CALIB_VAL per hour
6	CALIB_SIGN	Calibration sign: 0= Negative sign: remove pulses (it takes more clock ticks to count one second) 1= Positive sign: add pulses (it takes less clock ticks to count one second) Default Value: 0
5 : 0	CALIB_VAL	Calibration value for absolute frequency (at a fixed temperature). Each step causes 128 ticks to be added or removed each hour. Effectively that means that each step is 1.085ppm (= 128/(60*60*32,768)) when CAL_COMP_PER_MIN is set at default value. Positive values 0x01-0x3c (1..60) add pulses, negative values remove pulses, thus giving a range of +/-65.1 ppm (limited by 60 minutes per hour, not the range of this field) when CAL_-COMP_PER_MIN is set at default value . Calibration is performed hourly, starting at 59 minutes and 59 seconds, and applied as 64 ticks every 30 seconds until there have been 2*CALIB_VAL adjustments when CAL_COM-P_PER_MIN is set at default value . Default Value: 0

15.1.3 RTC_STATUS

Description: Status

Address: 0x42420010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							RTC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	RTC_BUSY	Pending RTC write Default Value: 0

15.1.4 RTC_RTC_TIME

Description: Calendar Seconds, Minutes, Hours, Day of Week

Address: 0x42420014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		A					
Name	Reserved [7:6]		RTC_SEC [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		A					
Name	Reserved [15:14]		RTC_MIN [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW	Reserved	RW				
HW Access	Reserved	A	Reserved	A				
Name	Reserved	CTRL_12HR	Reserved	RTC_HOUR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					A		
Name	Reserved [31:27]					RTC_DAY [26:24]		

Bits	Name	Description
26 : 24	RTC_DAY	Calendar Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
22	CTRL_12HR	Select 12/24HR mode: 1=12HR, 0=24HR Default Value: 0
20 : 16	RTC_HOUR	Calendar hours, value depending on 12/24HR mode 0=24HR: [20:16]=0-23 1=12HR: [20]:0=AM, 1=PM, [19:16]=1-12 Default Value: 0
13 : 8	RTC_MIN	Calendar minutes, 0-59 Default Value: 0
5 : 0	RTC_SEC	Calendar seconds, 0-59 Default Value: 0

15.1.5 RTC_RTC_DATE

Description: Calendar Day of Month, Month, Year

Address: 0x42420018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			A				
Name	Reserved [7:5]			RTC_DATE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				A			
Name	Reserved [15:12]				RTC_MON [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW						
HW Access	Reserved	A						
Name	Reserved	RTC_YEAR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
22 : 16	RTC_YEAR	Calendar year, 0-99 Default Value: 0
11 : 8	RTC_MON	Calendar Month, 1-12 Default Value: 1
4 : 0	RTC_DATE	Calendar Day of the Month, 1-31 Automatic Leap Year Correction Default Value: 1

15.1.6 RTC_ALM1_TIME

Description: Alarm 1 Seconds, Minute, Hours, Day of Week

Address: 0x4242001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved	RW					
HW Access	A	Reserved	A					
Name	ALM_SEC_EN	Reserved	ALM_SEC [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved	RW					
HW Access	A	Reserved	A					
Name	ALM_MIN_EN	Reserved	ALM_MIN [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW	Reserved		RW				
HW Access	A	Reserved		A				
Name	ALM_HOUR_EN	Reserved [22:21]		ALM_HOUR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved				RW		
HW Access	A	Reserved				A		
Name	ALM_-DAY_EN	Reserved [30:27]				ALM_DAY [26:24]		

Bits	Name	Description
31	ALM_DAY_EN	Alarm Day of the Week enable: 0=ignore, 1=match Default Value: 0
26 : 24	ALM_DAY	Alarm Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
23	ALM_HOUR_EN	Alarm hour enable: 0=ignore, 1=match Default Value: 0
20 : 16	ALM_HOUR	Alarm hours, value depending on 12/24HR mode 24HR: [4:0]=0-23 12HR: [4]:0=AM, 1=PM, [3:0]=1-12 Default Value: 0
15	ALM_MIN_EN	Alarm minutes enable: 0=ignore, 1=match Default Value: 0
13 : 8	ALM_MIN	Alarm minutes, 0-59 Default Value: 0
7	ALM_SEC_EN	Alarm second enable: 0=ignore, 1=match Default Value: 0
5 : 0	ALM_SEC	Alarm seconds, 0-59 Default Value: 0

15.1.7 RTC_ALM1_DATE

Description: Alarm 1 Day of Month, Month

Address: 0x42420020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved		RW				
HW Access	A	Reserved		A				
Name	ALM_-DATE_EN	Reserved [6:5]		ALM_DATE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved			RW			
HW Access	A	Reserved			A			
Name	ALM_MON_EN	Reserved [14:12]			ALM_MON [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	A	Reserved						
Name	ALM_EN	Reserved [30:24]						

Bits	Name	Description
31	ALM_EN	Master enable for alarm 1. 0: Alarm 1 is disabled. Fields for date and time are ignored. 1: Alarm 1 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. Default Value: 0
15	ALM_MON_EN	Alarm Month enable: 0=ignore, 1=match Default Value: 0
11 : 8	ALM_MON	Alarm Month, 1-12 Default Value: 1
7	ALM_DATE_EN	Alarm Day of the Month enable: 0=ignore, 1=match Default Value: 0
4 : 0	ALM_DATE	Alarm Day of the Month, 1-31 Leap Year corrected Default Value: 1

15.1.8 RTC_ALM2_TIME

Description: Alarm 2 Seconds, Minute, Hours, Day of Week

Address: 0x42420024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved	RW					
HW Access	A	Reserved	A					
Name	ALM_SEC_EN	Reserved	ALM_SEC [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved	RW					
HW Access	A	Reserved	A					
Name	ALM_MIN_EN	Reserved	ALM_MIN [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW	Reserved		RW				
HW Access	A	Reserved		A				
Name	ALM_HOUR_EN	Reserved [22:21]		ALM_HOUR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved				RW		
HW Access	A	Reserved				A		
Name	ALM_-DAY_EN	Reserved [30:27]				ALM_DAY [26:24]		

Bits	Name	Description
31	ALM_DAY_EN	Alarm Day of the Week enable: 0=ignore, 1=match Default Value: 0
26 : 24	ALM_DAY	Alarm Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
23	ALM_HOUR_EN	Alarm hour enable: 0=ignore, 1=match Default Value: 0
20 : 16	ALM_HOUR	Alarm hours, value depending on 12/24HR mode 24HR: [4:0]=0-23 12HR: [4]:0=AM, 1=PM, [3:0]=1-12 Default Value: 0
15	ALM_MIN_EN	Alarm minutes enable: 0=ignore, 1=match Default Value: 0
13 : 8	ALM_MIN	Alarm minutes, 0-59 Default Value: 0
7	ALM_SEC_EN	Alarm second enable: 0=ignore, 1=match Default Value: 0
5 : 0	ALM_SEC	Alarm seconds, 0-59 Default Value: 0

15.1.9 RTC_ALM2_DATE

Description: Alarm 2 Day of Month, Month

Address: 0x42420028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved		RW				
HW Access	A	Reserved		A				
Name	ALM_-DATE_EN	Reserved [6:5]		ALM_DATE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved			RW			
HW Access	A	Reserved			A			
Name	ALM_MON_EN	Reserved [14:12]			ALM_MON [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	A	Reserved						
Name	ALM_EN	Reserved [30:24]						

Bits	Name	Description
31	ALM_EN	Master enable for alarm 2. 0: Alarm 2 is disabled. Fields for date and time are ignored. 1: Alarm 2 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. Default Value: 0
15	ALM_MON_EN	Alarm Month enable: 0=ignore, 1=match Default Value: 0
11 : 8	ALM_MON	Alarm Month, 1-12 Default Value: 1
7	ALM_DATE_EN	Alarm Day of the Month enable: 0=ignore, 1=match Default Value: 0
4 : 0	ALM_DATE	Alarm Day of the Month, 1-31 Leap Year corrected Default Value: 1

15.1.10 RTC_INTR

Description: Interrupt request register

Address: 0x4242002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1C	RW1C	RW1C
HW Access	Reserved					RW1S	RW1S	RW1S
Name	Reserved [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	CENTURY	Century overflow interrupt Default Value: 0
1	ALARM2	Alarm 2 Interrupt Default Value: 0
0	ALARM1	Alarm 1 Interrupt Default Value: 0

15.1.11 RTC_INTR_SET

Description: Interrupt set request register

Address: 0x42420030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1S	RW1S	RW1S
HW Access	Reserved					A	A	A
Name	Reserved [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	CENTURY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	ALARM2	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	ALARM1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

15.1.12 RTC_INTR_MASK

Description: Interrupt mask register

Address: 0x42420034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	CENTURY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	ALARM2	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	ALARM1	Mask bit for corresponding bit in interrupt request register. Default Value: 0

15.1.13 RTC_INTR_MASKED

Description: Interrupt masked request register

Address: 0x42420038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R	R	R
HW Access	Reserved					RW	RW	RW
Name	Reserved [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	CENTURY	Logical and of corresponding request and mask bits. Default Value: 0
1	ALARM2	Logical and of corresponding request and mask bits. Default Value: 0
0	ALARM1	Logical and of corresponding request and mask bits. Default Value: 0

15.1.14 RTC_RESET

Description: RTC reset register

Address: 0x42420048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	Reserved						
HW Access	A	Reserved						
Name	RESET	Reserved [30:24]						

Bits	Name	Description
31	RESET	Writing 1 to this register resets the backup logic. Hardware clears it when the reset is complete. After setting this register, firmware should confirm it reads as 0 before attempting to write other backup registers. Default Value: 0

15.1.15 RTC_BREG_SET00

Description: Backup register region 0

Address: 0x42421000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	BREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	BREG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	BREG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	BREG [31:24]							

Bits	Name	Description
31 : 0	BREG	Backup memory that contains application-specific data. Memory is retained on VDDD supply. Default Value: 0

15.1.16 RTC_BREG_SET10

Description: Backup register region 1

Address: 0x42421010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	BREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	BREG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	BREG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	BREG [31:24]							

Bits	Name	Description
31 : 0	BREG	Backup memory that contains application-specific data. Memory is retained on VDDD supply. Default Value: 0

15.1.17 RTC_BREG_SET20

Description: Backup register region 2

Address: 0x42421020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	BREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	BREG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	BREG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	BREG [31:24]							

Bits	Name	Description
31 : 0	BREG	Backup memory that contains application-specific data. Memory is retained on VDDD supply. Default Value: 0

16 I/O Subsystem registers

This section discusses the I/O Subsystem registers. It lists all the registers in mapping tables, in address order.

16.1 Register details

Register name	Address	Description
HSIOM_PRT0_PORT_SEL0	0x42800000	Port selection 0
HSIOM_PRT1_PORT_SEL0	0x42800010	Port selection 0
HSIOM_PRT1_PORT_SEL1	0x42800014	Port selection 1
HSIOM_PRT2_PORT_SEL0	0x42800020	Port selection 0
HSIOM_PRT3_PORT_SEL0	0x42800030	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT4_PORT_SEL0	0x42800040	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT4_PORT_SEL1	0x42800044	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT5_PORT_SEL0	0x42800050	Port selection 0. See HSIOM_PRT2_PORT_SEL0 for the details of bit fields.
HSIOM_PRT6_PORT_SEL0	0x42800060	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT6_PORT_SEL1	0x42800064	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT7_PORT_SEL0	0x42800070	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT7_PORT_SEL1	0x42800074	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT8_PORT_SEL0	0x42800080	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT8_PORT_SEL1	0x42800084	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT9_PORT_SEL0	0x42800090	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT10_PORT_SEL0	0x428000A0	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT10_PORT_SEL1	0x428000A4	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT11_PORT_SEL0	0x428000B0	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT11_PORT_SEL1	0x428000B4	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT12_PORT_SEL0	0x428000C0	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.

Register name	Address	Description
HSIOM_PRT12_PORT_SEL1	0x428000C4	Port selection 1
HSIOM_PRT13_PORT_SEL0	0x428000D0	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT13_PORT_SEL1	0x428000D4	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT14_PORT_SEL0	0x428000E0	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT14_PORT_SEL1	0x428000E4	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT15_PORT_SEL0	0x428000F0	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT15_PORT_SEL1	0x428000F4	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT16_PORT_SEL0	0x42800100	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT16_PORT_SEL1	0x42800104	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT17_PORT_SEL0	0x42800110	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT17_PORT_SEL1	0x42800114	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT18_PORT_SEL0	0x42800120	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT19_PORT_SEL0	0x42800130	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT20_PORT_SEL0	0x42800140	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT20_PORT_SEL1	0x42800144	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_PRT21_PORT_SEL0	0x42800150	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT21_PORT_SEL1	0x42800154	Port selection 1. See HSIOM_PRT1_PORT_SEL1 for the details of bit fields.
HSIOM_SECURE_PRT0_NONSECURE_MASK	0x42801000	Non-Secure Mask
HSIOM_SECURE_PRT1_NONSECURE_MASK	0x42801010	Non-Secure Mask
HSIOM_SECURE_PRT2_NONSECURE_MASK	0x42801020	Non-Secure Mask
HSIOM_SECURE_PRT3_NONSECURE_MASK	0x42801030	Non-Secure Mask. See HSIOM_SECURE_PRT0_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT4_NONSECURE_MASK	0x42801040	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.

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Register name	Address	Description
HSIOM_SECURE_PRT5_NONSECURE_MASK	0x42801050	Non-Secure Mask. See HSIOM_SECURE_PRT2_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT6_NONSECURE_MASK	0x42801060	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT7_NONSECURE_MASK	0x42801070	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT8_NONSECURE_MASK	0x42801080	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT9_NONSECURE_MASK	0x42801090	Non-Secure Mask
HSIOM_SECURE_PRT10_NONSECURE_MASK	0x428010A0	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT11_NONSECURE_MASK	0x428010B0	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT12_NONSECURE_MASK	0x428010C0	Non-Secure Mask
HSIOM_SECURE_PRT13_NONSECURE_MASK	0x428010D0	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT14_NONSECURE_MASK	0x428010E0	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT15_NONSECURE_MASK	0x428010F0	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT16_NONSECURE_MASK	0x42801100	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT17_NONSECURE_MASK	0x42801110	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT18_NONSECURE_MASK	0x42801120	Non-Secure Mask. See HSIOM_SECURE_PRT0_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT19_NONSECURE_MASK	0x42801130	Non-Secure Mask. See HSIOM_SECURE_PRT0_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT20_NONSECURE_MASK	0x42801140	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.

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Register name	Address	Description
HSIOM_SECURE_PRT21_NONSECURE_MASK	0x42801150	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL0	0x42802000	AMUX splitter cell control
HSIOM_AMUX_SPLIT_CTL1	0x42802004	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL2	0x42802008	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL3	0x4280200C	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL4	0x42802010	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL5	0x42802014	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL6	0x42802018	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
GPIO_PRT0_OUT	0x42810000	Port output data register
GPIO_PRT0_OUT_CLR	0x42810004	Port output data clear register
GPIO_PRT0_OUT_SET	0x42810008	Port output data set register
GPIO_PRT0_OUT_INV	0x4281000C	Port output data invert register
GPIO_PRT0_IN	0x42810010	Port input state register
GPIO_PRT0_INTR	0x42810014	Port interrupt status register
GPIO_PRT0_INTR_MASK	0x42810018	Port interrupt mask register
GPIO_PRT0_INTR_MASKED	0x4281001C	Port interrupt masked status register
GPIO_PRT0_INTR_SET	0x42810020	Port interrupt set register
GPIO_PRT0_INTR_CFG	0x42810040	Port interrupt configuration register
GPIO_PRT0_CFG	0x42810044	Port configuration register
GPIO_PRT0_CFG_IN	0x42810048	Port input buffer configuration register
GPIO_PRT0_CFG_OUT	0x4281004C	Port output buffer configuration register
GPIO_PRT0_CFG_SLEW_EXT	0x42810064	Port output buffer slew extension configuration register
GPIO_PRT0_CFG_DRIVE_EXT0	0x42810068	Port output buffer drive sel extension configuration register
GPIO_PRT0_CFG_DRIVE_EXT1	0x4281006C	Port output buffer drive sel extension configuration register
GPIO_PRT0_CFG_OUT3	0x42810070	Port output buffer configuration register 3

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Register name	Address	Description
GPIO_PRT1_OUT	0x42810080	Port output data register
GPIO_PRT1_OUT_CLR	0x42810084	Port output data clear register
GPIO_PRT1_OUT_SET	0x42810088	Port output data set register
GPIO_PRT1_OUT_INV	0x4281008C	Port output data invert register
GPIO_PRT1_IN	0x42810090	Port input state register
GPIO_PRT1_INTR	0x42810094	Port interrupt status register
GPIO_PRT1_INTR_MASK	0x42810098	Port interrupt mask register
GPIO_PRT1_INTR_MASKED	0x4281009C	Port interrupt masked status register
GPIO_PRT1_INTR_SET	0x428100A0	Port interrupt set register
GPIO_PRT1_INTR_CFG	0x428100C0	Port interrupt configuration register
GPIO_PRT1_CFG	0x428100C4	Port configuration register
GPIO_PRT2_OUT	0x42810100	Port output data register
GPIO_PRT2_OUT_CLR	0x42810104	Port output data clear register
GPIO_PRT2_OUT_SET	0x42810108	Port output data set register
GPIO_PRT2_OUT_INV	0x4281010C	Port output data invert register
GPIO_PRT2_IN	0x42810110	Port input state register
GPIO_PRT2_INTR	0x42810114	Port interrupt status register
GPIO_PRT2_INTR_MASK	0x42810118	Port interrupt mask register
GPIO_PRT2_INTR_MASKED	0x4281011C	Port interrupt masked status register
GPIO_PRT2_INTR_SET	0x42810120	Port interrupt set register
GPIO_PRT2_INTR_CFG	0x42810140	Port interrupt configuration register
GPIO_PRT2_CFG	0x42810144	Port configuration register
GPIO_PRT2_CFG_IN	0x42810148	Port input buffer configuration register
GPIO_PRT2_CFG_OUT	0x4281014C	Port output buffer configuration register
GPIO_PRT2_CFG_SLEW_EXT	0x42810164	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT2_CFG_DRIVE_EXT0	0x42810168	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT2_CFG_DRIVE_EXT1	0x4281016C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT2_CFG_OUT3	0x42810170	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT3_OUT	0x42810180	Port output data register. See GPIO_PRT0_OUT for the details of bit fields.

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Register name	Address	Description
GPIO_PRT3_OUT_CLR	0x42810184	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT3_OUT_SET	0x42810188	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT3_OUT_INV	0x4281018C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT3_IN	0x42810190	Port input state register. See GPIO_PRT0_IN for the details of bit fields.
GPIO_PRT3_INTR	0x42810194	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT3_INTR_MASK	0x42810198	Port interrupt mask register. See GPIO_PRT0_INTR_MASK for the details of bit fields.
GPIO_PRT3_INTR_MASKED	0x4281019C	Port interrupt masked status register. See GPIO_PRT0_INTR_MASKED for the details of bit fields.
GPIO_PRT3_INTR_SET	0x428101A0	Port interrupt set register. See GPIO_PRT0_INTR_SET for the details of bit fields.
GPIO_PRT3_INTR_CFG	0x428101C0	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT3_CFG	0x428101C4	Port configuration register. See GPIO_PRT0_CFG for the details of bit fields.
GPIO_PRT3_CFG_IN	0x428101C8	Port input buffer configuration register. See GPIO_PRT0_CFG_IN for the details of bit fields.
GPIO_PRT3_CFG_OUT	0x428101CC	Port output buffer configuration register
GPIO_PRT3_CFG_SLEW_EXT	0x428101E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT3_CFG_DRIVE_EXT0	0x428101E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT3_CFG_DRIVE_EXT1	0x428101EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT3_CFG_OUT3	0x428101F0	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT3_CFG_RES	0x428101F4	Port resistor configuration register 3
GPIO_PRT4_OUT	0x42810200	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT4_OUT_CLR	0x42810204	Port output data clear register. See GPIO_PRT1_OUT_CLR for the details of bit fields.

I/O Subsystem registers

Register name	Address	Description
GPIO_PRT4_OUT_SET	0x42810208	Port output data set register. See GPIO_PRT1_OUT_SET for the details of bit fields.
GPIO_PRT4_OUT_INV	0x4281020C	Port output data invert register. See GPIO_PRT1_OUT_INV for the details of bit fields.
GPIO_PRT4_IN	0x42810210	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT4_INTR	0x42810214	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT4_INTR_MASK	0x42810218	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT4_INTR_MASKED	0x4281021C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT4_INTR_SET	0x42810220	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT4_INTR_CFG	0x42810240	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT4_CFG	0x42810244	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT5_OUT	0x42810280	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT5_OUT_CLR	0x42810284	Port output data clear register. See GPIO_PRT2_OUT_CLR for the details of bit fields.
GPIO_PRT5_OUT_SET	0x42810288	Port output data set register. See GPIO_PRT2_OUT_SET for the details of bit fields.
GPIO_PRT5_OUT_INV	0x4281028C	Port output data invert register. See GPIO_PRT2_OUT_INV for the details of bit fields.
GPIO_PRT5_IN	0x42810290	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT5_INTR	0x42810294	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT5_INTR_MASK	0x42810298	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT5_INTR_MASKED	0x4281029C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT5_INTR_SET	0x428102A0	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT5_INTR_CFG	0x428102C0	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.

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Register name	Address	Description
GPIO_PRT5_CFG	0x428102C4	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT5_CFG_IN	0x428102C8	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT5_CFG_OUT	0x428102CC	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT5_CFG_SLEW_EXT	0x428102E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT5_CFG_DRIVE_EXT0	0x428102E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT5_CFG_DRIVE_EXT1	0x428102EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT5_CFG_OUT3	0x428102F0	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT6_OUT	0x42810300	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT6_OUT_CLR	0x42810304	Port output data clear register. See GPIO_PRT1_OUT_CLR for the details of bit fields.
GPIO_PRT6_OUT_SET	0x42810308	Port output data set register. See GPIO_PRT1_OUT_SET for the details of bit fields.
GPIO_PRT6_OUT_INV	0x4281030C	Port output data invert register. See GPIO_PRT1_OUT_INV for the details of bit fields.
GPIO_PRT6_IN	0x42810310	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT6_INTR	0x42810314	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT6_INTR_MASK	0x42810318	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT6_INTR_MASKED	0x4281031C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT6_INTR_SET	0x42810320	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT6_INTR_CFG	0x42810340	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT6_CFG	0x42810344	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.

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Register name	Address	Description
GPIO_PRT6_CFG_IN	0x42810348	Port input buffer configuration register
GPIO_PRT6_CFG_OUT	0x4281034C	Port output buffer configuration register
GPIO_PRT6_CFG_SLEW_EXT	0x42810364	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT6_CFG_DRIVE_EXT0	0x42810368	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT6_CFG_DRIVE_EXT1	0x4281036C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT6_CFG_OUT3	0x42810370	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT7_OUT	0x42810380	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT7_OUT_CLR	0x42810384	Port output data clear register. See GPIO_PRT1_OUT_CLR for the details of bit fields.
GPIO_PRT7_OUT_SET	0x42810388	Port output data set register. See GPIO_PRT1_OUT_SET for the details of bit fields.
GPIO_PRT7_OUT_INV	0x4281038C	Port output data invert register. See GPIO_PRT1_OUT_INV for the details of bit fields.
GPIO_PRT7_IN	0x42810390	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT7_INTR	0x42810394	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT7_INTR_MASK	0x42810398	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT7_INTR_MASKED	0x4281039C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT7_INTR_SET	0x428103A0	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT7_INTR_CFG	0x428103C0	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT7_CFG	0x428103C4	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT7_CFG_IN	0x428103C8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT7_CFG_OUT	0x428103CC	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.

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Register name	Address	Description
GPIO_PRT7_CFG_SLEW_EXT	0x428103E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT7_CFG_DRIVE_EXT0	0x428103E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT7_CFG_DRIVE_EXT1	0x428103EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT7_CFG_OUT3	0x428103F0	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT8_OUT	0x42810400	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT8_OUT_CLR	0x42810404	Port output data clear register. See GPIO_PRT1_OUT_CLR for the details of bit fields.
GPIO_PRT8_OUT_SET	0x42810408	Port output data set register. See GPIO_PRT1_OUT_SET for the details of bit fields.
GPIO_PRT8_OUT_INV	0x4281040C	Port output data invert register. See GPIO_PRT1_OUT_INV for the details of bit fields.
GPIO_PRT8_IN	0x42810410	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT8_INTR	0x42810414	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT8_INTR_MASK	0x42810418	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT8_INTR_MASKED	0x4281041C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT8_INTR_SET	0x42810420	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT8_INTR_CFG	0x42810440	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT8_CFG	0x42810444	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT8_CFG_IN	0x42810448	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT8_CFG_OUT	0x4281044C	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.

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Register name	Address	Description
GPIO_PRT8_CFG_SLEW_EXT	0x42810464	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT8_CFG_DRIVE_EXT0	0x42810468	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT8_CFG_DRIVE_EXT1	0x4281046C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT8_CFG_OUT3	0x42810470	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT9_OUT	0x42810480	Port output data register
GPIO_PRT9_OUT_CLR	0x42810484	Port output data clear register
GPIO_PRT9_OUT_SET	0x42810488	Port output data set register
GPIO_PRT9_OUT_INV	0x4281048C	Port output data invert register
GPIO_PRT9_IN	0x42810490	Port input state register
GPIO_PRT9_INTR	0x42810494	Port interrupt status register
GPIO_PRT9_INTR_MASK	0x42810498	Port interrupt mask register
GPIO_PRT9_INTR_MASKED	0x4281049C	Port interrupt masked status register
GPIO_PRT9_INTR_SET	0x428104A0	Port interrupt set register
GPIO_PRT9_INTR_CFG	0x428104C0	Port interrupt configuration register
GPIO_PRT9_CFG	0x428104C4	Port configuration register
GPIO_PRT9_CFG_IN	0x428104C8	Port input buffer configuration register
GPIO_PRT9_CFG_OUT	0x428104CC	Port output buffer configuration register
GPIO_PRT9_CFG_SLEW_EXT	0x428104E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT9_CFG_DRIVE_EXT0	0x428104E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT9_CFG_DRIVE_EXT1	0x428104EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT9_CFG_OUT3	0x428104F0	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT10_OUT	0x42810500	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.

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Register name	Address	Description
GPIO_PRT10_OUT_CLR	0x42810504	Port output data clear register. See GPIO_PRT1_OUT_CLR for the details of bit fields.
GPIO_PRT10_OUT_SET	0x42810508	Port output data set register. See GPIO_PRT1_OUT_SET for the details of bit fields.
GPIO_PRT10_OUT_INV	0x4281050C	Port output data invert register. See GPIO_PRT1_OUT_INV for the details of bit fields.
GPIO_PRT10_IN	0x42810510	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT10_INTR	0x42810514	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT10_INTR_MASK	0x42810518	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT10_INTR_MASKED	0x4281051C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT10_INTR_SET	0x42810520	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT10_INTR_CFG	0x42810540	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT10_CFG	0x42810544	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT10_CFG_IN	0x42810548	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT10_CFG_OUT	0x4281054C	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT10_CFG_SLEW_EXT	0x42810564	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT10_CFG_DRIVE_EXT0	0x42810568	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT10_CFG_DRIVE_EXT1	0x4281056C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT10_CFG_OUT3	0x42810570	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT11_OUT	0x42810580	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT11_OUT_CLR	0x42810584	Port output data clear register. See GPIO_PRT1_OUT_CLR for the details of bit fields.

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Register name	Address	Description
GPIO_PRT11_OUT_SET	0x42810588	Port output data set register. See GPIO_PRT1_OUT_SET for the details of bit fields.
GPIO_PRT11_OUT_INV	0x4281058C	Port output data invert register. See GPIO_PRT1_OUT_INV for the details of bit fields.
GPIO_PRT11_IN	0x42810590	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT11_INTR	0x42810594	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT11_INTR_MASK	0x42810598	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT11_INTR_MASKED	0x4281059C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT11_INTR_SET	0x428105A0	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT11_INTR_CFG	0x428105C0	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT11_CFG	0x428105C4	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT11_CFG_IN	0x428105C8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT11_CFG_OUT	0x428105CC	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT11_CFG_SLEW_EXT	0x428105E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT11_CFG_DRIVE_EXT0	0x428105E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT11_CFG_DRIVE_EXT1	0x428105EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT11_CFG_OUT3	0x428105F0	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT12_OUT	0x42810600	Port output data register
GPIO_PRT12_OUT_CLR	0x42810604	Port output data clear register
GPIO_PRT12_OUT_SET	0x42810608	Port output data set register
GPIO_PRT12_OUT_INV	0x4281060C	Port output data invert register
GPIO_PRT12_IN	0x42810610	Port input state register

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Register name	Address	Description
GPIO_PRT12_INTR	0x42810614	Port interrupt status register
GPIO_PRT12_INTR_MASK	0x42810618	Port interrupt mask register
GPIO_PRT12_INTR_MASKED	0x4281061C	Port interrupt masked status register
GPIO_PRT12_INTR_SET	0x42810620	Port interrupt set register
GPIO_PRT12_INTR_CFG	0x42810640	Port interrupt configuration register
GPIO_PRT12_CFG	0x42810644	Port configuration register
GPIO_PRT12_CFG_IN	0x42810648	Port input buffer configuration register
GPIO_PRT12_CFG_OUT	0x4281064C	Port output buffer configuration register
GPIO_PRT12_CFG_SLEW_EXT	0x42810664	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT12_CFG_DRIVE_EXT0	0x42810668	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT12_CFG_DRIVE_EXT1	0x4281066C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT12_CFG_OUT3	0x42810670	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT13_OUT	0x42810680	Port output data register
GPIO_PRT13_OUT_CLR	0x42810684	Port output data clear register
GPIO_PRT13_OUT_SET	0x42810688	Port output data set register
GPIO_PRT13_OUT_INV	0x4281068C	Port output data invert register
GPIO_PRT13_IN	0x42810690	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT13_INTR	0x42810694	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT13_INTR_MASK	0x42810698	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT13_INTR_MASKED	0x4281069C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT13_INTR_SET	0x428106A0	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT13_INTR_CFG	0x428106C0	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT13_CFG	0x428106C4	Port configuration register

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Register name	Address	Description
GPIO_PRT13_CFG_IN	0x428106C8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT13_CFG_OUT	0x428106CC	Port output buffer configuration register
GPIO_PRT13_CFG_SLEW_EXT	0x428106E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT13_CFG_DRIVE_EXT0	0x428106E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT13_CFG_DRIVE_EXT1	0x428106EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT13_CFG_OUT3	0x428106F0	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT14_OUT	0x42810700	Port output data register. See GPIO_PRT13_OUT for the details of bit fields.
GPIO_PRT14_OUT_CLR	0x42810704	Port output data clear register. See GPIO_PRT13_OUT_CLR for the details of bit fields.
GPIO_PRT14_OUT_SET	0x42810708	Port output data set register. See GPIO_PRT13_OUT_SET for the details of bit fields.
GPIO_PRT14_OUT_INV	0x4281070C	Port output data invert register. See GPIO_PRT13_OUT_INV for the details of bit fields.
GPIO_PRT14_IN	0x42810710	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT14_INTR	0x42810714	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT14_INTR_MASK	0x42810718	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT14_INTR_MASKED	0x4281071C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT14_INTR_SET	0x42810720	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT14_INTR_CFG	0x42810740	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT14_CFG	0x42810744	Port configuration register. See GPIO_PRT13_CFG for the details of bit fields.

Register name	Address	Description
GPIO_PRT14_CFG_IN	0x42810748	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT14_CFG_OUT	0x4281074C	Port output buffer configuration register. See GPIO_PRT13_CFG_OUT for the details of bit fields.
GPIO_PRT14_CFG_SLEW_EXT	0x42810764	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT14_CFG_DRIVE_EXT0	0x42810768	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT14_CFG_DRIVE_EXT1	0x4281076C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT14_CFG_OUT3	0x42810770	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT15_OUT	0x42810780	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT15_OUT_CLR	0x42810784	Port output data clear register. See GPIO_PRT13_OUT_CLR for the details of bit fields.
GPIO_PRT15_OUT_SET	0x42810788	Port output data set register. See GPIO_PRT13_OUT_SET for the details of bit fields.
GPIO_PRT15_OUT_INV	0x4281078C	Port output data invert register. See GPIO_PRT13_OUT_INV for the details of bit fields.
GPIO_PRT15_IN	0x42810790	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT15_INTR	0x42810794	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT15_INTR_MASK	0x42810798	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT15_INTR_MASKED	0x4281079C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT15_INTR_SET	0x428107A0	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT15_INTR_CFG	0x428107C0	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.

I/O Subsystem registers

Register name	Address	Description
GPIO_PRT15_CFG	0x428107C4	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT15_CFG_IN	0x428107C8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT15_CFG_OUT	0x428107CC	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT15_CFG_SLEW_EXT	0x428107E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT15_CFG_DRIVE_EXT0	0x428107E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT15_CFG_DRIVE_EXT1	0x428107EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT15_CFG_OUT3	0x428107F0	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT16_OUT	0x42810800	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT16_OUT_CLR	0x42810804	Port output data clear register. See GPIO_PRT13_OUT_CLR for the details of bit fields.
GPIO_PRT16_OUT_SET	0x42810808	Port output data set register. See GPIO_PRT13_OUT_SET for the details of bit fields.
GPIO_PRT16_OUT_INV	0x4281080C	Port output data invert register. See GPIO_PRT13_OUT_INV for the details of bit fields.
GPIO_PRT16_IN	0x42810810	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT16_INTR	0x42810814	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT16_INTR_MASK	0x42810818	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT16_INTR_MASKED	0x4281081C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT16_INTR_SET	0x42810820	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT16_INTR_CFG	0x42810840	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.

I/O Subsystem registers

Register name	Address	Description
GPIO_PRT16_CFG	0x42810844	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT16_CFG_IN	0x42810848	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT16_CFG_OUT	0x4281084C	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT16_CFG_SLEW_EXT	0x42810864	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT16_CFG_DRIVE_EXT0	0x42810868	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT16_CFG_DRIVE_EXT1	0x4281086C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT16_CFG_OUT3	0x42810870	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT17_OUT	0x42810880	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT17_OUT_CLR	0x42810884	Port output data clear register. See GPIO_PRT13_OUT_CLR for the details of bit fields.
GPIO_PRT17_OUT_SET	0x42810888	Port output data set register. See GPIO_PRT13_OUT_SET for the details of bit fields.
GPIO_PRT17_OUT_INV	0x4281088C	Port output data invert register. See GPIO_PRT13_OUT_INV for the details of bit fields.
GPIO_PRT17_IN	0x42810890	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT17_INTR	0x42810894	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT17_INTR_MASK	0x42810898	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT17_INTR_MASKED	0x4281089C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT17_INTR_SET	0x428108A0	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT17_INTR_CFG	0x428108C0	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.

I/O Subsystem registers

Register name	Address	Description
GPIO_PRT17_CFG	0x428108C4	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT17_CFG_IN	0x428108C8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT17_CFG_OUT	0x428108CC	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT17_CFG_SLEW_EXT	0x428108E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT17_CFG_DRIVE_EXT0	0x428108E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT17_CFG_DRIVE_EXT1	0x428108EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT17_CFG_OUT3	0x428108F0	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT18_IN	0x42810910	Port input state register. See GPIO_PRT0_IN for the details of bit fields.
GPIO_PRT18_INTR	0x42810914	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT18_INTR_MASK	0x42810918	Port interrupt mask register. See GPIO_PRT0_INTR_MASK for the details of bit fields.
GPIO_PRT18_INTR_MASKED	0x4281091C	Port interrupt masked status register. See GPIO_PRT0_INTR_MASKED for the details of bit fields.
GPIO_PRT18_INTR_SET	0x42810920	Port interrupt set register. See GPIO_PRT0_INTR_SET for the details of bit fields.
GPIO_PRT18_INTR_CFG	0x42810940	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT18_CFG	0x42810944	Port configuration register
GPIO_PRT18_CFG_IN	0x42810948	Port input buffer configuration register. See GPIO_PRT0_CFG_IN for the details of bit fields.
GPIO_PRT18_CFG_SLEW_EXT	0x42810964	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT18_CFG_DRIVE_EXT0	0x42810968	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.

I/O Subsystem registers

Register name	Address	Description
GPIO_PRT18_CFG_DRIVE_EXT1	0x4281096C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT18_CFG_OUT3	0x42810970	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT19_IN	0x42810990	Port input state register. See GPIO_PRT0_IN for the details of bit fields.
GPIO_PRT19_INTR	0x42810994	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT19_INTR_MASK	0x42810998	Port interrupt mask register. See GPIO_PRT0_INTR_MASK for the details of bit fields.
GPIO_PRT19_INTR_MASKED	0x4281099C	Port interrupt masked status register. See GPIO_PRT0_INTR_MASKED for the details of bit fields.
GPIO_PRT19_INTR_SET	0x428109A0	Port interrupt set register. See GPIO_PRT0_INTR_SET for the details of bit fields.
GPIO_PRT19_INTR_CFG	0x428109C0	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT19_CFG	0x428109C4	Port configuration register. See GPIO_PRT18_CFG for the details of bit fields.
GPIO_PRT19_CFG_IN	0x428109C8	Port input buffer configuration register. See GPIO_PRT0_CFG_IN for the details of bit fields.
GPIO_PRT19_CFG_SLEW_EXT	0x428109E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT19_CFG_DRIVE_EXT0	0x428109E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT19_CFG_DRIVE_EXT1	0x428109EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT19_CFG_OUT3	0x428109F0	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT20_OUT	0x42810A00	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT20_OUT_CLR	0x42810A04	Port output data clear register. See GPIO_PRT1_OUT_CLR for the details of bit fields.

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Register name	Address	Description
GPIO_PRT20_OUT_SET	0x42810A08	Port output data set register. See GPIO_PRT1_OUT_SET for the details of bit fields.
GPIO_PRT20_OUT_INV	0x42810A0C	Port output data invert register. See GPIO_PRT1_OUT_INV for the details of bit fields.
GPIO_PRT20_IN	0x42810A10	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT20_INTR	0x42810A14	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT20_INTR_MASK	0x42810A18	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT20_INTR_MASKED	0x42810A1C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT20_INTR_SET	0x42810A20	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT20_INTR_CFG	0x42810A40	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT20_CFG	0x42810A44	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT20_CFG_IN	0x42810A48	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT20_CFG_OUT	0x42810A4C	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT20_CFG_SLEW_EXT	0x42810A64	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT20_CFG_DRIVE_EXT0	0x42810A68	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT20_CFG_DRIVE_EXT1	0x42810A6C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT20_CFG_OUT3	0x42810A70	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3 for the details of bit fields.
GPIO_PRT21_OUT	0x42810A80	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT21_OUT_CLR	0x42810A84	Port output data clear register. See GPIO_PRT1_OUT_CLR for the details of bit fields.
GPIO_PRT21_OUT_SET	0x42810A88	Port output data set register. See GPIO_PRT1_OUT_SET for the details of bit fields.

I/O Subsystem registers

Register name	Address	Description
GPIO_PRT21_OUT_INV	0x42810A8C	Port output data invert register. See GPIO_PRT1_OUT_INV for the details of bit fields.
GPIO_PRT21_IN	0x42810A90	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT21_INTR	0x42810A94	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT21_INTR_MASK	0x42810A98	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT21_INTR_MASKED	0x42810A9C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT21_INTR_SET	0x42810AA0	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT21_INTR_CFG	0x42810AC0	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT21_CFG	0x42810AC4	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT21_CFG_IN	0x42810AC8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT21_CFG_OUT	0x42810ACC	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT21_CFG_SLEW_EXT	0x42810AE4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT21_CFG_DRIVE_EXT0	0x42810AE8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT21_CFG_DRIVE_EXT1	0x42810AEC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT21_CFG_OUT3	0x42810AF0	Port output buffer configuration register 3. See GPIO_PRT0_CFG_OUT3_ for the details of bit fields.
GPIO_SEC_INTR_CAUSE0	0x42817000	Secure Interrupt port cause register 0
GPIO_INTR_CAUSE0	0x42818000	Interrupt port cause register 0
GPIO_VDD_ACTIVE	0x42818010	Extern power supply detection register
GPIO_VDD_INTR	0x42818014	Supply detection interrupt register
GPIO_VDD_INTR_MASK	0x42818018	Supply detection interrupt mask register
GPIO_VDD_INTR_MASKED	0x4281801C	Supply detection interrupt masked register
GPIO_VDD_INTR_SET	0x42818020	Supply detection interrupt set register

I/O Subsystem registers

Register name	Address	Description
GPIO_VDD_MODE_SEL	0x42818024	Supply mode select for 3.3V domains
SMARTIO_PRT11_CTL	0x42820B00	Control register
SMARTIO_PRT11_SYNC_CTL	0x42820B10	Synchronization control register
SMARTIO_PRT11_LUT_SEL0	0x42820B20	LUT component input selection
SMARTIO_PRT11_LUT_SEL1	0x42820B24	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT11_LUT_SEL2	0x42820B28	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT11_LUT_SEL3	0x42820B2C	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT11_LUT_SEL4	0x42820B30	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT11_LUT_SEL5	0x42820B34	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT11_LUT_SEL6	0x42820B38	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT11_LUT_SEL7	0x42820B3C	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT11_LUT_CTL0	0x42820B40	LUT component control register
SMARTIO_PRT11_LUT_CTL1	0x42820B44	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT11_LUT_CTL2	0x42820B48	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT11_LUT_CTL3	0x42820B4C	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT11_LUT_CTL4	0x42820B50	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT11_LUT_CTL5	0x42820B54	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT11_LUT_CTL6	0x42820B58	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.

I/O Subsystem registers

Register name	Address	Description
SMARTIO_PRT11_LUT_CTL7	0x42820B5C	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT11_DU_SEL	0x42820BC0	Data unit component input selection
SMARTIO_PRT11_DU_CTL	0x42820BC4	Data unit component control register
SMARTIO_PRT11_DATA	0x42820BF0	Data register
SMARTIO_PRT17_CTL	0x42821100	Control register. See SMARTIO_PRT11_CTL for the details of bit fields.
SMARTIO_PRT17_SYNC_CTL	0x42821110	Synchronization control register. See SMARTIO_PRT11_SYNC_CTL for the details of bit fields.
SMARTIO_PRT17_LUT_SEL0	0x42821120	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL1	0x42821124	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL2	0x42821128	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL3	0x4282112C	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL4	0x42821130	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL5	0x42821134	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL6	0x42821138	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL7	0x4282113C	LUT component input selection. See SMARTIO_PRT11_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL0	0x42821140	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL1	0x42821144	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL2	0x42821148	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.

I/O Subsystem registers

Register name	Address	Description
SMARTIO_PRT17_LUT_CTL3	0x4282114C	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL4	0x42821150	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL5	0x42821154	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL6	0x42821158	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL7	0x4282115C	LUT component control register. See SMARTIO_PRT11_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_DU_SEL	0x428211C0	Data unit component input selection. See SMARTIO_PRT11_DU_SEL for the details of bit fields.
SMARTIO_PRT17_DU_CTL	0x428211C4	Data unit component control register. See SMARTIO_PRT11_DU_CTL for the details of bit fields.
SMARTIO_PRT17_DATA	0x428211F0	Data register. See SMARTIO_PRT11_DATA for the details of bit fields.

16.1.1 HSIOM_PRT0_PORT_SEL0

Description: Port selection 0

Address: 0x42800000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12 : 8	IO1_SEL	Selects connection for IO pin 1 route. Default Value: 0
4 : 0	IO0_SEL	Selects connection for IO pin 0 route. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable" **0x3: DSI_GPIO :** DSI controls "out", GPIO controls "output enable" **0x4: AMUXA :** Analog mux bus A

16.1.1 HSIOM_PRT0_PORT_SEL0 (continued)

0x5: AMUXB :

Analog mux bus B

0x6: AMUXA_DSI :

Analog mux bus A, DSI control

0x7: AMUXB_DSI :

Analog mux bus B, DSI control

0x8: ACT_0 :

Active functionality 0

0x9: ACT_1 :

Active functionality 1

0xa: ACT_2 :

Active functionality 2

0xb: ACT_3 :

Active functionality 3

0xc: DS_0 :

DeepSleep functionality 0

0xd: DS_1 :

DeepSleep functionality 1

0xe: DS_2 :

DeepSleep functionality 2

0xf: DS_3 :

DeepSleep functionality 3

0x10: ACT_4 :

Active functionality 4

0x11: ACT_5 :

Active functionality 5

0x12: ACT_6 :

Active functionality 6

16.1.1 HSIOM_PRT0_PORT_SEL0 (continued)

0x13: ACT_7 :

Active functionality 7

0x14: ACT_8 :

Active functionality 8

0x15: ACT_9 :

Active functionality 9

0x16: ACT_10 :

Active functionality 10

0x17: ACT_11 :

Active functionality 11

0x18: ACT_12 :

Active functionality 12

0x19: ACT_13 :

Active functionality 13

0x1a: ACT_14 :

Active functionality 14

0x1b: ACT_15 :

Active functionality 15

0x1c: DS_4 :

DeepSleep functionality 4

0x1d: DS_5 :

DeepSleep functionality 5

0x1e: DS_6 :

DeepSleep functionality 6

0x1f: DS_7 :

DeepSleep functionality 7

16.1.2 HSIOM_PRT1_PORT_SEL0

Description: Port selection 0

Address: 0x42800010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [23:21]			IO2_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [31:29]			IO3_SEL [28:24]				

Bits	Name	Description
28 : 24	IO3_SEL	Selects connection for IO pin 3 route. Default Value: 0
20 : 16	IO2_SEL	Selects connection for IO pin 2 route. Default Value: 0
12 : 8	IO1_SEL	Selects connection for IO pin 1 route. Default Value: 0
4 : 0	IO0_SEL	Selects connection for IO pin 0 route. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable" **0x3: DSI_GPIO :** DSI controls "out", GPIO controls "output enable"

16.1.2 HSIOM_PRT1_PORT_SEL0 (continued)

0x4: AMUXA :

Analog mux bus A

0x5: AMUXB :

Analog mux bus B

0x6: AMUXA_DSI :

Analog mux bus A, DSI control

0x7: AMUXB_DSI :

Analog mux bus B, DSI control

0x8: ACT_0 :

Active functionality 0

0x9: ACT_1 :

Active functionality 1

0xa: ACT_2 :

Active functionality 2

0xb: ACT_3 :

Active functionality 3

0xc: DS_0 :

DeepSleep functionality 0

0xd: DS_1 :

DeepSleep functionality 1

0xe: DS_2 :

DeepSleep functionality 2

0xf: DS_3 :

DeepSleep functionality 3

0x10: ACT_4 :

Active functionality 4

0x11: ACT_5 :

Active functionality 5

16.1.2 HSIOM_PRT1_PORT_SEL0 (continued)

0x12: ACT_6 :

Active functionality 6

0x13: ACT_7 :

Active functionality 7

0x14: ACT_8 :

Active functionality 8

0x15: ACT_9 :

Active functionality 9

0x16: ACT_10 :

Active functionality 10

0x17: ACT_11 :

Active functionality 11

0x18: ACT_12 :

Active functionality 12

0x19: ACT_13 :

Active functionality 13

0x1a: ACT_14 :

Active functionality 14

0x1b: ACT_15 :

Active functionality 15

0x1c: DS_4 :

DeepSleep functionality 4

0x1d: DS_5 :

DeepSleep functionality 5

0x1e: DS_6 :

DeepSleep functionality 6

0x1f: DS_7 :

DeepSleep functionality 7

16.1.3 HSIOM_PRT1_PORT_SEL1

Description: Port selection 1

Address: 0x42800014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [23:21]			IO6_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [31:29]			IO7_SEL [28:24]				

Bits	Name	Description
28 : 24	IO7_SEL	Selects connection for IO pin 7 route. Default Value: 0
20 : 16	IO6_SEL	Selects connection for IO pin 6 route. Default Value: 0
12 : 8	IO5_SEL	Selects connection for IO pin 5 route. Default Value: 0
4 : 0	IO4_SEL	Selects connection for IO pin 4 route. See PORT_SEL0 for connection details. Default Value: 0

16.1.4 HSIOM_PRT2_PORT_SEL0

Description: Port selection 0

Address: 0x42800020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	IO0_SEL	Selects connection for IO pin 0 route. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable" **0x3: DSI_GPIO :** DSI controls "out", GPIO controls "output enable" **0x4: AMUXA :** Analog mux bus A

16.1.4 HSIOM_PRT2_PORT_SEL0 (continued)

0x5: AMUXB :

Analog mux bus B

0x6: AMUXA_DSI :

Analog mux bus A, DSI control

0x7: AMUXB_DSI :

Analog mux bus B, DSI control

0x8: ACT_0 :

Active functionality 0

0x9: ACT_1 :

Active functionality 1

0xa: ACT_2 :

Active functionality 2

0xb: ACT_3 :

Active functionality 3

0xc: DS_0 :

DeepSleep functionality 0

0xd: DS_1 :

DeepSleep functionality 1

0xe: DS_2 :

DeepSleep functionality 2

0xf: DS_3 :

DeepSleep functionality 3

0x10: ACT_4 :

Active functionality 4

0x11: ACT_5 :

Active functionality 5

0x12: ACT_6 :

Active functionality 6

16.1.4 HSIOM_PRT2_PORT_SEL0 (continued)

0x13: ACT_7 :

Active functionality 7

0x14: ACT_8 :

Active functionality 8

0x15: ACT_9 :

Active functionality 9

0x16: ACT_10 :

Active functionality 10

0x17: ACT_11 :

Active functionality 11

0x18: ACT_12 :

Active functionality 12

0x19: ACT_13 :

Active functionality 13

0x1a: ACT_14 :

Active functionality 14

0x1b: ACT_15 :

Active functionality 15

0x1c: DS_4 :

DeepSleep functionality 4

0x1d: DS_5 :

DeepSleep functionality 5

0x1e: DS_6 :

DeepSleep functionality 6

0x1f: DS_7 :

DeepSleep functionality 7

16.1.5 HSIOM_PRT12_PORT_SEL1

Description: Port selection 1

Address: 0x428000C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12 : 8	IO5_SEL	Selects connection for IO pin 5 route. Default Value: 0
4 : 0	IO4_SEL	Selects connection for IO pin 4 route. See PORT_SEL0 for connection details. Default Value: 0

16.1.6 HSIOM_SECURE_PRT0_NONSECURE_MASK

Description: Non-Secure Mask

Address: 0x42801000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						RW	RW
Name	Reserved [7:2]						NONSE-CURE1	NONSE-CURE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	NONSECURE1	Non-secure attribute for IO1. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
0	NONSECURE0	Non-secure attribute for IO0. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

16.1.7 HSIOM_SECURE_PRT1_NONSECURE_MASK

Description: Non-Secure Mask

Address: 0x42801010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	NONSE-CURE7	NONSE-CURE6	NONSE-CURE5	NONSE-CURE4	NONSE-CURE3	NONSE-CURE2	NONSE-CURE1	NONSE-CURE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	NONSECURE7	Non-secure attribute for IO7. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
6	NONSECURE6	Non-secure attribute for IO6. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
5	NONSECURE5	Non-secure attribute for IO5. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
4	NONSECURE4	Non-secure attribute for IO4. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
3	NONSECURE3	Non-secure attribute for IO3. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
2	NONSECURE2	Non-secure attribute for IO2. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

16.1.7 HSIOM_SECURE_PRT1_NONSECURE_MASK (continued)

1	NONSECURE1	Non-secure attribute for IO1. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
0	NONSECURE0	Non-secure attribute for IO0. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

16.1.8 HSIOM_SECURE_PRT2_NONSECURE_MASK

Description: Non-Secure Mask

Address: 0x42801020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							RW
Name	Reserved [7:1]							NONSE-CURE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	NONSECURE0	Non-secure attribute for IO0. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

16.1.9 HSIOM_SECURE_PRT9_NONSECURE_MASK

Description: Non-Secure Mask

Address: 0x42801090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				RW	RW	RW	RW
Name	Reserved [7:4]				NONSE-CURE3	NONSE-CURE2	NONSE-CURE1	NONSE-CURE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	NONSECURE3	Non-secure attribute for IO3. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
2	NONSECURE2	Non-secure attribute for IO2. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
1	NONSECURE1	Non-secure attribute for IO1. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
0	NONSECURE0	Non-secure attribute for IO0. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

16.1.10 HSIOM_SECURE_PRT12_NONSECURE_MASK

Description: Non-Secure Mask

Address: 0x428010C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [7:6]		NONSE-CURE5	NONSE-CURE4	NONSE-CURE3	NONSE-CURE2	NONSE-CURE1	NONSE-CURE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	NONSECURE5	Non-secure attribute for IO5. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
4	NONSECURE4	Non-secure attribute for IO4. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
3	NONSECURE3	Non-secure attribute for IO3. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
2	NONSECURE2	Non-secure attribute for IO2. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
1	NONSECURE1	Non-secure attribute for IO1. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
0	NONSECURE0	Non-secure attribute for IO0. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

16.1.11 HSIOM_AMUX_SPLIT_CTL0

Description: AMUX splitter cell control

Address: 0x42802000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	Reserved	RW	RW	RW
HW Access	Reserved	R	R	R	Reserved	R	R	R
Name	Reserved	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	Reserved	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0
0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

16.1.12 GPIO_PRT0_OUT

Description: Port output data register

Address: 0x42810000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						RW	RW
Name	Reserved [7:2]						OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

16.1.13 GPIO_PRT0_OUT_CLR

Description: Port output data clear register

Address: 0x42810004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						A	A
Name	Reserved [7:2]						OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	OUT1	IO clear output for pin 1 Default Value: 0
0	OUT0	IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. Default Value: 0

16.1.14 GPIO_PRT0_OUT_SET

Description: Port output data set register

Address: 0x42810008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						A	A
Name	Reserved [7:2]						OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	OUT1	IO set output for pin 1 Default Value: 0
0	OUT0	IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. Default Value: 0

16.1.15 GPIO_PRT0_OUT_INV

Description: Port output data invert register

Address: 0x4281000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						A	A
Name	Reserved [7:2]						OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	OUT1	IO invert output for pin 1 Default Value: 0
0	OUT0	IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.16 GPIO_PRT0_IN

Description: Port input state register

Address: 0x42810010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

16.1.17 GPIO_PRT0_INTR

Description: Port interrupt status register

Address: 0x42810014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1C	RW1C
HW Access	Reserved						A	A
Name	Reserved [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [23:18]						IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

16.1.18 GPIO_PRT0_INTR_MASK

Description: Port interrupt mask register

Address: 0x42810018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

16.1.19 GPIO_PRT0_INTR_MASKED

Description: Port interrupt masked status register

Address: 0x4281001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.20 GPIO_PRT0_INTR_SET

Description: Port interrupt set register

Address: 0x42810020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1S	RW1S
HW Access	Reserved						A	A
Name	Reserved [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16.1.21 GPIO_PRT0_INTR_CFG

Description: Port interrupt configuration register

Address: 0x42810040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW		RW	
HW Access	Reserved				R		R	
Name	Reserved [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW			RW	
HW Access	Reserved			R			R	
Name	Reserved [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0

16.1.21 GPIO_PRT0_INTR_CFG (continued)

0x0: DISABLE :

Disabled

0x1: RISING :

Rising edge

0x2: FALLING :

Falling edge

0x3: BOTH :

Both rising and falling edges

16.1.22 GPIO_PRT0_CFG

Description: Port configuration register

Address: 0x42810044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**

16.1.22 GPIO_PRT0_CFG (continued)

3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: CFG3_EN :** Enables CFG_OUT3.bit[3:0] to control Port Pin 0 drive mode configuration. **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance **0x2: PULLUP :** Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up

16.1.22 GPIO_PRT0_CFG (continued)

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

16.1.22 GPIO_PRT0_CFG (continued)

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

16.1.23 GPIO_PRT0_CFG_IN

Description: Port input buffer configuration register

Address: 0x42810048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** Input buffer compatible with CMOS and I2C interfaces **0x1: TTL :** Input buffer compatible with TTL and MediaLB interfaces

16.1.24 GPIO_PRT0_CFG_OUT

Description: Port output buffer configuration register

Address: 0x4281004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW		RW	
HW Access	Reserved				R		R	
Name	Reserved [23:20]				DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 (Not using these register for PSOC™ Edge devices. CFG_DRIVE_EXT0 & CFG_DRIVE_EXT1 are used for drive strength settings) Default Value: 0 **0x0: DRIVE_SEL_ZERO :** **0x1: DRIVE_SEL_ONE :** **0x2: DRIVE_SEL_TWO :** **0x3: DRIVE_SEL_THREE :**

16.1.25 GPIO_PRT0_CFG_SLEW_EXT

Description: Port output buffer slew extension configuration register

Address: 0x42810064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [7:5]			SLEW1	Reserved [3:1]			SLEW0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			SLEW3	Reserved [11:9]			SLEW2

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [23:21]			SLEW5	Reserved [19:17]			SLEW4

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [31:29]			SLEW7	Reserved [27:25]			SLEW6

Bits	Name	Description
28	SLEW7	Slew rate for IO pin 7 Default Value: 0
24	SLEW6	Slew rate for IO pin 6 Default Value: 0
20	SLEW5	Slew rate for IO pin 5 Default Value: 0
16	SLEW4	Slew rate for IO pin 4 Default Value: 0
12	SLEW3	Slew rate for IO pin 3 Default Value: 0
8	SLEW2	Slew rate for IO pin 2 Default Value: 0
4	SLEW1	Slew rate for IO pin 1 Default Value: 0
0	SLEW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate CFG_SLEW_EXT register is used for slew settings when CFG.SLOWx = 0. Default Value: 0

16.1.26 GPIO_PRT0_CFG_DRIVE_EXT0

Description: Port output buffer drive sel extension configuration register

Address: 0x42810068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					DRIVE_SEL_EXT0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [15:11]					DRIVE_SEL_EXT1 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					DRIVE_SEL_EXT2 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					DRIVE_SEL_EXT3 [26:24]		

Bits	Name	Description
26 : 24	DRIVE_SEL_EXT3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
18 : 16	DRIVE_SEL_EXT2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
10 : 8	DRIVE_SEL_EXT1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
2 : 0	DRIVE_SEL_EXT0	Sets the GPIO drive strength for IO pin 0(only first 3 bits of DRIVE_SEL_EXTx are used, remaining 2 bits are reserved for future use) Default Value: 0 **0x0: DRIVE_SEL_ZERO :** low drive strength (Ex: 1mA) **0x1: DRIVE_SEL_ONE :** drive strength (Ex: 2mA) **0x2: DRIVE_SEL_TWO :** drive strength (Ex: 3mA)

16.1.26 GPIO_PRT0_CFG_DRIVE_EXT0 (continued)

0x3: DRIVE_SEL_THREE :

drive strength (Ex: 4mA)

0x4: DRIVE_SEL_FOUR :

drive strength (Ex: 5mA)

0x5: DRIVE_SEL_FIVE :

drive strength (Ex: 6mA)

0x6: DRIVE_SEL_SIX :

drive strength (Ex: 7mA)

0x7: DRIVE_SEL_SEVEN :

High Drive strength (Ex: 8mA)

16.1.27 GPIO_PRT0_CFG_DRIVE_EXT1

Description: Port output buffer drive sel extension configuration register

Address: 0x4281006C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					DRIVE_SEL_EXT4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [15:11]					DRIVE_SEL_EXT5 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					DRIVE_SEL_EXT6 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					DRIVE_SEL_EXT7 [26:24]		

Bits	Name	Description
26 : 24	DRIVE_SEL_EXT7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
18 : 16	DRIVE_SEL_EXT6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
10 : 8	DRIVE_SEL_EXT5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
2 : 0	DRIVE_SEL_EXT4	Sets the GPIO drive strength for IO pin 4 Default Value: 0

16.1.28 GPIO_PRT0_CFG_OUT3

Description: Port output buffer configuration register 3

Address: 0x42810070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DRIVEMODE_EXT1 [7:4]				DRIVEMODE_EXT0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	DRIVEMODE_EXT3 [15:12]				DRIVEMODE_EXT2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	DRIVEMODE_EXT5 [23:20]				DRIVEMODE_EXT4 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	DRIVEMODE_EXT7 [31:28]				DRIVEMODE_EXT6 [27:24]			

Bits	Name	Description
31 : 28	DRIVEMODE_EXT7	Sets the Drive mode for pin 7. Default Value: 0
27 : 24	DRIVEMODE_EXT6	Sets the Drive mode for pin 6. Default Value: 0
23 : 20	DRIVEMODE_EXT5	Sets the Drive mode for pin 5. Default Value: 0
19 : 16	DRIVEMODE_EXT4	Sets the Drive mode for pin 4. Default Value: 0
15 : 12	DRIVEMODE_EXT3	Sets the Drive mode for pin 3. Default Value: 0
11 : 8	DRIVEMODE_EXT2	Sets the Drive mode for pin 2. Default Value: 0
7 : 4	DRIVEMODE_EXT1	Sets the Drive mode for pin 1. Default Value: 0
3 : 0	DRIVEMODE_EXT0	Sets the Drive mode for pin 0. This fields are valid only if CFG.DRIVE_MODE0=0. See the bit value definitions below for functions. Default Value: 0 **0x0: HIGHZ :** Hi Z data_out_en=1: data_out=X-> HIZ, data_out_en=0, data_out=X-> HiZ

16.1.28 GPIO_PRT0_CFG_OUT3 (continued)

0x1: PUPD :

Strong drive 0/1 when enabled - else pull_up and pull_down both enabled
data_out_en=1: data_out=1/0->Strong 1/0, data_out_en=0, data_out=X-> Pull Up & Pull Down

0x2: PULLUP :

Strong drive 0/1 when enabled - else pull_up enabled
data_out_en=1: data_out= 1/0->Strong 1/0, data_out_en=0, data_out=X-> Pull Up

0x3: PULLDOWN :

Strong drive 0/1 when enabled - else pull_down enabled
data_out_en=1: data_out=1/0->Strong 1/0 , data_out_en=0, data_out=X-> Pull Down

0x4: OE0_HIZHIZ_0 :

Strong drive 0/1 when enabled - else HIZ
data_out_en=1: data_out=1/0-> Strong 1/0, data_out_en=0, data_out=X-> HiZ

0x5: OE0_HIZHIZ_1 :

Strong drive 0/1 when enabled - else HIZ
data_out_en=1: data_out=1/0-> Strong 1/0, data_out_en=0, data_out=X-> HiZ

0x6: OE0_HIZHIZ_2 :

Strong drive 0/1 when enabled - else HIZ
data_out_en=1: data_out=1/0-> Strong 1/0, data_out_en=0, data_out=X-> HiZ

0x7: OE0_PUPD :

Strong drive 0/1 when enabled else data_out driven by pull_up or pull _down following data_out
data_out_en=1: data_out=1/0-> Strong 1/0, data_out_en=0, data_out=0-> pull_down,
data_out_en=0,data_out=1->pull_up

0x8: OE0_PUHIZ :

Strong drive 0/1 when enabled else data_out driven by pull_up or HiZ following data_out
data_out_en=1: data_out=1/0-> Strong 1/0, data_out_en=0, data_out=0-> pull_down,
data_out_en=0,data_out=1->pull_up

16.1.29 GPIO_PRT1_OUT

Description: Port output data register

Address: 0x42810080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

16.1.30 GPIO_PRT1_OUT_CLR

Description: Port output data clear register

Address: 0x42810084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO clear output for pin 7 Default Value: 0
6	OUT6	IO clear output for pin 6 Default Value: 0
5	OUT5	IO clear output for pin 5 Default Value: 0
4	OUT4	IO clear output for pin 4 Default Value: 0
3	OUT3	IO clear output for pin 3 Default Value: 0
2	OUT2	IO clear output for pin 2 Default Value: 0
1	OUT1	IO clear output for pin 1 Default Value: 0
0	OUT0	IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. Default Value: 0

16.1.31 GPIO_PRT1_OUT_SET

Description: Port output data set register

Address: 0x42810088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO set output for pin 7 Default Value: 0
6	OUT6	IO set output for pin 6 Default Value: 0
5	OUT5	IO set output for pin 5 Default Value: 0
4	OUT4	IO set output for pin 4 Default Value: 0
3	OUT3	IO set output for pin 3 Default Value: 0
2	OUT2	IO set output for pin 2 Default Value: 0
1	OUT1	IO set output for pin 1 Default Value: 0
0	OUT0	IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. Default Value: 0

16.1.32 GPIO_PRT1_OUT_INV

Description: Port output data invert register

Address: 0x4281008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO invert output for pin 7 Default Value: 0
6	OUT6	IO invert output for pin 6 Default Value: 0
5	OUT5	IO invert output for pin 5 Default Value: 0
4	OUT4	IO invert output for pin 4 Default Value: 0
3	OUT3	IO invert output for pin 3 Default Value: 0
2	OUT2	IO invert output for pin 2 Default Value: 0
1	OUT1	IO invert output for pin 1 Default Value: 0
0	OUT0	IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.33 GPIO_PRT1_IN

Description: Port input state register

Address: 0x42810090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
6	IN6	IO pin state for pin 6 Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

16.1.34 GPIO_PRT1_INTR

Description: Port interrupt status register

Address: 0x42810094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN_IN7	IN_IN6	IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
22	IN_IN6	IO pin state for pin 6 Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detect for IO pin 7 Default Value: 0

16.1.34 GPIO_PRT1_INTR (continued)

6	EDGE6	Edge detect for IO pin 6 Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

16.1.35 GPIO_PRT1_INTR_MASK

Description: Port interrupt mask register

Address: 0x42810098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
6	EDGE6	Masks edge interrupt on IO pin 6 Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

16.1.36 GPIO_PRT1_INTR_MASKED

Description: Port interrupt masked status register

Address: 0x4281009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
6	EDGE6	Edge detected and masked on IO pin 6 Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.37 GPIO_PRT1_INTR_SET

Description: Port interrupt set register

Address: 0x428100A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
6	EDGE6	Sets edge detect interrupt for IO pin 6 Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16.1.38 GPIO_PRT1_INTR_CFG

Description: Port interrupt configuration register

Address: 0x428100C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW			RW	
HW Access	Reserved			R			R	
Name	Reserved [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pin 6 Default Value: 0

16.1.38 GPIO_PRT1_INTR_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

16.1.39 GPIO_PRT1_CFG

Description: Port configuration register

Address: 0x428100C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0

16.1.39 GPIO_PRT1_CFG (continued)

26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :**

16.1.39 GPIO_PRT1_CFG (continued)

		0x4: OD_DRIVESLOW :
		0x5: OD_DRIVESHIGH :
		0x6: STRONG :
		0x7: PULLUP_DOWN :
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
		0x0: CFG3_EN :
		0x1: RESERVED :
		0x2: PULLUP :
		0x3: PULLDOWN :
		0x4: OD_DRIVESLOW :
		0x5: OD_DRIVESHIGH :
		0x6: STRONG :
		0x7: PULLUP_DOWN :
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
		0x0: CFG3_EN :
		0x1: RESERVED :
		0x2: PULLUP :
		0x3: PULLDOWN :
		0x4: OD_DRIVESLOW :
		0x5: OD_DRIVESHIGH :
		0x6: STRONG :
		0x7: PULLUP_DOWN :
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0

16.1.39 GPIO_PRT1_CFG (continued)

6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: CFG3_EN :** Enables CFG_OUT3.bit[3:0] to control Port Pin 0 drive mode configuration. **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

16.1.39 GPIO_PRT1_CFG (continued)

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

16.1.39 GPIO_PRT1_CFG (continued)

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': High Impedance
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
 GPIO_DSI_OUT = '0': Weak/resistive pull down
 GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Weak/resistive pull up

16.1.40 GPIO_PRT2_OUT

Description: Port output data register

Address: 0x42810100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							RW
Name	Reserved [7:1]							OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

16.1.41 GPIO_PRT2_OUT_CLR

Description: Port output data clear register

Address: 0x42810104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							A
Name	Reserved [7:1]							OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	OUT0	IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. Default Value: 0

16.1.42 GPIO_PRT2_OUT_SET

Description: Port output data set register

Address: 0x42810108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							A
Name	Reserved [7:1]							OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	OUT0	IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. Default Value: 0

16.1.43 GPIO_PRT2_OUT_INV

Description: Port output data invert register

Address: 0x4281010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							A
Name	Reserved [7:1]							OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	OUT0	IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.44 GPIO_PRT2_IN

Description: Port input state register

Address: 0x42810110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							IN0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

16.1.45 GPIO_PRT2_INTR

Description: Port interrupt status register

Address: 0x42810114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [7:1]							EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [23:17]							IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

16.1.46 GPIO_PRT2_INTR_MASK

Description: Port interrupt mask register

Address: 0x42810118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

16.1.47 GPIO_PRT2_INTR_MASKED

Description: Port interrupt masked status register

Address: 0x4281011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.48 GPIO_PRT2_INTR_SET

Description: Port interrupt set register

Address: 0x42810120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16.1.49 GPIO_PRT2_INTR_CFG

Description: Port interrupt configuration register

Address: 0x42810140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW			RW	
HW Access	Reserved			R			R	
Name	Reserved [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0

16.1.49 GPIO_PRT2_INTR_CFG (continued)

0x0: DISABLE :

Disabled

0x1: RISING :

Rising edge

0x2: FALLING :

Falling edge

0x3: BOTH :

Both rising and falling edges

16.1.50 GPIO_PRT2_CFG

Description: Port configuration register

Address: 0x42810144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW		
HW Access	Reserved				R	R		
Name	Reserved [7:4]				IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: CFG3_EN :** Enables CFG_OUT3.bit[3:0] to control Port Pin 0 drive mode configuration.

16.1.50 GPIO_PRT2_CFG (continued)

0x1: RESERVED :

This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases.
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

16.1.50 GPIO_PRT2_CFG (continued)

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

16.1.50 GPIO_PRT2_CFG (continued)

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

16.1.51 GPIO_PRT2_CFG_IN

Description: Port input buffer configuration register

Address: 0x42810148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** Input buffer compatible with CMOS and I2C interfaces **0x1: TTL :** Input buffer compatible with TTL and MediaLB interfaces

16.1.52 GPIO_PRT2_CFG_OUT

Description: Port output buffer configuration register

Address: 0x4281014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [23:18]						DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 (Not using these register for PSOC™ Edge devices. CFG_DRIVE_EXT0 & CFG_DRIVE_EXT1 are used for drive strength settings) Default Value: 0 **0x0: DRIVE_SEL_ZERO :** **0x1: DRIVE_SEL_ONE :** **0x2: DRIVE_SEL_TWO :** **0x3: DRIVE_SEL_THREE :**

16.1.53 GPIO_PRT3_CFG_OUT

Description: Port output buffer configuration register

Address: 0x428101CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW		RW	
HW Access	Reserved				R		R	
Name	Reserved [23:20]				DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 (Not using these register for PSOC™ Edge devices. CFG_DRIVE_EXT0 & CFG_DRIVE_EXT1 are used for drive strength settings) Default Value: 0 **0x0: DRIVE_SEL_ZERO :** **0x1: DRIVE_SEL_ONE :** **0x2: DRIVE_SEL_TWO :** **0x3: DRIVE_SEL_THREE :**
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Slow represents speed of operation. Slow = 0. Normal operation with 10 to 50 MHz. CFG_SLEW_EXT register is used for slew settings when slow = 0. Slow =1. I2C fast mode operation Default Value: 0

16.1.54 GPIO_PRT3_CFG_RES

Description: Port resistor configuration register 3

Address: 0x428101F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	R			Reserved	R		
Name	Reserved	RESISTOR_CFG1 [6:4]			Reserved	RESISTOR_CFG0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	R			Reserved	R		
Name	Reserved	RESISTOR_CFG3 [14:12]			Reserved	RESISTOR_CFG2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	R			Reserved	R		
Name	Reserved	RESISTOR_CFG5 [22:20]			Reserved	RESISTOR_CFG4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	R			Reserved	R		
Name	Reserved	RESISTOR_CFG7 [30:28]			Reserved	RESISTOR_CFG6 [26:24]		

Bits	Name	Description
30 : 28	RESISTOR_CFG7	Sets resistor value in IO cell for pin 1. Default Value: 0
26 : 24	RESISTOR_CFG6	Sets resistor value in IO cell for pin 1. Default Value: 0
22 : 20	RESISTOR_CFG5	Sets resistor value in IO cell for pin 1. Default Value: 0
18 : 16	RESISTOR_CFG4	Sets resistor value in IO cell for pin 1. Default Value: 0
14 : 12	RESISTOR_CFG3	Sets resistor value in IO cell for pin 1. Default Value: 0
10 : 8	RESISTOR_CFG2	Sets resistor value in IO cell for pin 1. Default Value: 0
6 : 4	RESISTOR_CFG1	Sets resistor value in IO cell for pin 1. Default Value: 0
2 : 0	RESISTOR_CFG0	Sets resistor value in IO cell for pin 1. - 50K pullup is NOT controlled by these bits. Used in conjuntion with CFG_OUT3[N]=OE0_PUHIZ (8). Default Value: 0 **0x0: I3C_PU_DISABLE :** Disable additional Pull-ups

16.1.54 GPIO_PRT3_CFG_RES (continued)

0x7: I3C_PU_570 :

Pull-up 570 ohms

0x6: I3C_PU_940 :

Pull-up 940 Ohms

0x5: I3C_PU_980 :

Pull-up 980 Ohms

0x3: I3C_PU_1150 :

Pull-up 1150 Ohms

0x4: I3C_PU_1650 :

Pull-up 1650 Ohms

0x2: I3C_PU_2190 :

Pull-up 2190 Ohms

0x1: I3C_PU_2800 :

Pull-up 2800 Ohms

16.1.55 GPIO_PRT6_CFG_IN

Description: Port input buffer configuration register

Address: 0x42810348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VTRIP_-SEL7_0	VTRIP_-SEL6_0	VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
6	VTRIP_SEL6_0	Configures the pin 6 input buffer mode (trip points and hysteresis) Default Value: 0
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0
		0x0: CMOS : Input buffer compatible with CMOS and I2C interfaces

16.1.55 GPIO_PRT6_CFG_IN (continued)

0x1: TTL :

Input buffer compatible with TTL and MediaLB interfaces

16.1.56 GPIO_PRT6_CFG_OUT

Description: Port output buffer configuration register

Address: 0x4281034C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLOW7	SLOW6	SLOW5	SLOW4	SLOW3	SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 (Not using these register for PSOC™ Edge devices. CFG_DRIVE_EXT0 & CFG_DRIVE_EXT1 are used for drive strength settings) Default Value: 0 **0x0: DRIVE_SEL_ZERO :** **0x1: DRIVE_SEL_ONE :**

16.1.56 GPIO_PRT6_CFG_OUT (continued)

0x2: DRIVE_SEL_TWO :

0x3: DRIVE_SEL_THREE :

7	SLOW7	Enables slow slew rate for IO pin 7 Default Value: 0
6	SLOW6	Enables slow slew rate for IO pin 6 Default Value: 0
5	SLOW5	Enables slow slew rate for IO pin 5 Default Value: 0
4	SLOW4	Enables slow slew rate for IO pin 4 Default Value: 0
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Slow represents speed of operation. Slow = 0. Normal operation with 10 to 50 MHz. CFG_SLEW_EXT register is used for slew settings when slow = 0. Slow =1. I2C fast mode operation Default Value: 0

16.1.57 GPIO_PRT9_OUT

Description: Port output data register

Address: 0x42810480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				RW	RW	RW	RW
Name	Reserved [7:4]				OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

16.1.58 GPIO_PRT9_OUT_CLR

Description: Port output data clear register

Address: 0x42810484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				A	A	A	A
Name	Reserved [7:4]				OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	OUT3	IO clear output for pin 3 Default Value: 0
2	OUT2	IO clear output for pin 2 Default Value: 0
1	OUT1	IO clear output for pin 1 Default Value: 0
0	OUT0	IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. Default Value: 0

16.1.59 GPIO_PRT9_OUT_SET

Description: Port output data set register

Address: 0x42810488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				A	A	A	A
Name	Reserved [7:4]				OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	OUT3	IO set output for pin 3 Default Value: 0
2	OUT2	IO set output for pin 2 Default Value: 0
1	OUT1	IO set output for pin 1 Default Value: 0
0	OUT0	IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. Default Value: 0

16.1.60 GPIO_PRT9_OUT_INV

Description: Port output data invert register

Address: 0x4281048C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				A	A	A	A
Name	Reserved [7:4]				OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	OUT3	IO invert output for pin 3 Default Value: 0
2	OUT2	IO invert output for pin 2 Default Value: 0
1	OUT1	IO invert output for pin 1 Default Value: 0
0	OUT0	IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.61 GPIO_PRT9_IN

Description: Port input state register

Address: 0x42810490

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [7:4]				IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

16.1.62 GPIO_PRT9_INTR

Description: Port interrupt status register

Address: 0x42810494

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1C	RW1C	RW1C	RW1C
HW Access	Reserved				A	A	A	A
Name	Reserved [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [23:20]				IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

16.1.63 GPIO_PRT9_INTR_MASK

Description: Port interrupt mask register

Address: 0x42810498

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

16.1.64 GPIO_PRT9_INTR_MASKED

Description: Port interrupt masked status register

Address: 0x4281049C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.65 GPIO_PRT9_INTR_SET

Description: Port interrupt set register

Address: 0x428104A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1S	RW1S	RW1S	RW1S
HW Access	Reserved				A	A	A	A
Name	Reserved [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16.1.66 GPIO_PRT9_INTR_CFG

Description: Port interrupt configuration register

Address: 0x428104C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW			RW	
HW Access	Reserved			R			R	
Name	Reserved [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0

16.1.66 GPIO_PRT9_INTR_CFG (continued)

3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

16.1.67 GPIO_PRT9_CFG

Description: Port configuration register

Address: 0x428104C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0

16.1.67 GPIO_PRT9_CFG (continued)

10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0

16.1.67 GPIO_PRT9_CFG (continued)

0x0: CFG3_EN :

Enables CFG_OUT3.bit[3:0] to control Port Pin 0 drive mode configuration.

0x1: RESERVED :

This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases.
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

16.1.67 GPIO_PRT9_CFG (continued)

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

16.1.67 GPIO_PRT9_CFG (continued)

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

16.1.68 GPIO_PRT9_CFG_IN

Description: Port input buffer configuration register

Address: 0x428104C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** Input buffer compatible with CMOS and I2C interfaces **0x1: TTL :** Input buffer compatible with TTL and MediaLB interfaces

16.1.69 GPIO_PRT9_CFG_OUT

Description: Port output buffer configuration register

Address: 0x428104CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				SLOW3	SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 (Not using these register for PSOC™ Edge devices. CFG_DRIVE_EXT0 & CFG_DRIVE_EXT1 are used for drive strength settings) Default Value: 0 **0x0: DRIVE_SEL_ZERO :** **0x1: DRIVE_SEL_ONE :** **0x2: DRIVE_SEL_TWO :** **0x3: DRIVE_SEL_THREE :**
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0

16.1.69 GPIO_PRT9_CFG_OUT (continued)

1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Slow represents speed of operation. Slow = 0. Normal operation with 10 to 50 MHz. CFG_SLEW_EXT register is used for slew settings when slow = 0. Slow =1. I2C fast mode operation Default Value: 0

16.1.70 GPIO_PRT12_OUT

Description: Port output data register

Address: 0x42810600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [7:6]		OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

16.1.71 GPIO_PRT12_OUT_CLR

Description: Port output data clear register

Address: 0x42810604

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		A	A	A	A	A	A
Name	Reserved [7:6]		OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	OUT5	IO clear output for pin 5 Default Value: 0
4	OUT4	IO clear output for pin 4 Default Value: 0
3	OUT3	IO clear output for pin 3 Default Value: 0
2	OUT2	IO clear output for pin 2 Default Value: 0
1	OUT1	IO clear output for pin 1 Default Value: 0
0	OUT0	IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. Default Value: 0

16.1.72 GPIO_PRT12_OUT_SET

Description: Port output data set register

Address: 0x42810608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		A	A	A	A	A	A
Name	Reserved [7:6]		OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	OUT5	IO set output for pin 5 Default Value: 0
4	OUT4	IO set output for pin 4 Default Value: 0
3	OUT3	IO set output for pin 3 Default Value: 0
2	OUT2	IO set output for pin 2 Default Value: 0
1	OUT1	IO set output for pin 1 Default Value: 0
0	OUT0	IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. Default Value: 0

16.1.73 GPIO_PRT12_OUT_INV

Description: Port output data invert register

Address: 0x4281060C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		A	A	A	A	A	A
Name	Reserved [7:6]		OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	OUT5	IO invert output for pin 5 Default Value: 0
4	OUT4	IO invert output for pin 4 Default Value: 0
3	OUT3	IO invert output for pin 3 Default Value: 0
2	OUT2	IO invert output for pin 2 Default Value: 0
1	OUT1	IO invert output for pin 1 Default Value: 0
0	OUT0	IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.74 GPIO_PRT12_IN

Description: Port input state register

Address: 0x42810610

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		W	W	W	W	W	W
Name	Reserved [7:6]		IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

16.1.75 GPIO_PRT12_INTR

Description: Port interrupt status register

Address: 0x42810614

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved		A	A	A	A	A	A
Name	Reserved [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		W	W	W	W	W	W
Name	Reserved [23:22]		IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0

16.1.75 GPIO_PRT12_INTR (continued)

2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

16.1.76 GPIO_PRT12_INTR_MASK

Description: Port interrupt mask register

Address: 0x42810618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

16.1.77 GPIO_PRT12_INTR_MASKED

Description: Port interrupt masked status register

Address: 0x4281061C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		W	W	W	W	W	W
Name	Reserved [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.78 GPIO_PRT12_INTR_SET

Description: Port interrupt set register

Address: 0x42810620

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	Reserved		A	A	A	A	A	A
Name	Reserved [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16.1.79 GPIO_PRT12_INTR_CFG

Description: Port interrupt configuration register

Address: 0x42810640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW		RW	
HW Access	Reserved				R		R	
Name	Reserved [15:12]				EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW			RW	
HW Access	Reserved			R			R	
Name	Reserved [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0

16.1.79 GPIO_PRT12_INTR_CFG (continued)

7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

16.1.80 GPIO_PRT12_CFG

Description: Port configuration register

Address: 0x42810644

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0

16.1.80 GPIO_PRT12_CFG (continued)

18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :**

16.1.80 GPIO_PRT12_CFG (continued)

		0x4: OD_DRIVESLOW :
		0x5: OD_DRIVESHIGH :
		0x6: STRONG :
		0x7: PULLUP_DOWN :
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
		0x0: CFG3_EN :
		0x1: RESERVED :
		0x2: PULLUP :
		0x3: PULLDOWN :
		0x4: OD_DRIVESLOW :
		0x5: OD_DRIVESHIGH :
		0x6: STRONG :
		0x7: PULLUP_DOWN :
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: CFG3_EN : Enables CFG_OUT3.bit[3:0] to control Port Pin 0 drive mode configuration.

16.1.80 GPIO_PRT12_CFG (continued)

0x1: RESERVED :

This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases.
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

16.1.80 GPIO_PRT12_CFG (continued)

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

16.1.80 GPIO_PRT12_CFG (continued)

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

16.1.81 GPIO_PRT12_CFG_IN

Description: Port input buffer configuration register

Address: 0x42810648

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** Input buffer compatible with CMOS and I2C interfaces **0x1: TTL :** Input buffer compatible with TTL and MediaLB interfaces

16.1.82 GPIO_PRT12_CFG_OUT

Description: Port output buffer configuration register

Address: 0x4281064C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		SLOW5	SLOW4	SLOW3	SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW		RW	
HW Access	Reserved				R		R	
Name	Reserved [31:28]				DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 (Not using these register for PSOC™ Edge devices. CFG_DRIVE_EXT0 & CFG_DRIVE_EXT1 are used for drive strength settings) Default Value: 0 **0x0: DRIVE_SEL_ZERO :** **0x1: DRIVE_SEL_ONE :** **0x2: DRIVE_SEL_TWO :** **0x3: DRIVE_SEL_THREE :**

16.1.82 GPIO_PRT12_CFG_OUT (continued)

5	SLOW5	Enables slow slew rate for IO pin 5 Default Value: 0
4	SLOW4	Enables slow slew rate for IO pin 4 Default Value: 0
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Slow represents speed of operation. Slow = 0. Normal operation with 10 to 50 MHz. CFG_SLEW_EXT register is used for slew settings when slow = 0. Slow =1. I2C fast mode operation Default Value: 0

16.1.83 GPIO_PRT13_OUT

Description: Port output data register

Address: 0x42810680

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	Reserved	RW	RW	RW	RW	Reserved
HW Access	RW	RW	Reserved	RW	RW	RW	RW	Reserved
Name	OUT7	OUT6	Reserved	OUT4	OUT3	OUT2	OUT1	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0

16.1.84 GPIO_PRT13_OUT_CLR

Description: Port output data clear register

Address: 0x42810684

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	Reserved	RW	RW	RW	RW	Reserved
HW Access	A	A	Reserved	A	A	A	A	Reserved
Name	OUT7	OUT6	Reserved	OUT4	OUT3	OUT2	OUT1	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO clear output for pin 7 Default Value: 0
6	OUT6	IO clear output for pin 6 Default Value: 0
4	OUT4	IO clear output for pin 4 Default Value: 0
3	OUT3	IO clear output for pin 3 Default Value: 0
2	OUT2	IO clear output for pin 2 Default Value: 0
1	OUT1	IO clear output for pin 1 Default Value: 0

16.1.85 GPIO_PRT13_OUT_SET

Description: Port output data set register

Address: 0x42810688

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	Reserved	RW	RW	RW	RW	Reserved
HW Access	A	A	Reserved	A	A	A	A	Reserved
Name	OUT7	OUT6	Reserved	OUT4	OUT3	OUT2	OUT1	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO set output for pin 7 Default Value: 0
6	OUT6	IO set output for pin 6 Default Value: 0
4	OUT4	IO set output for pin 4 Default Value: 0
3	OUT3	IO set output for pin 3 Default Value: 0
2	OUT2	IO set output for pin 2 Default Value: 0
1	OUT1	IO set output for pin 1 Default Value: 0

16.1.86 GPIO_PRT13_OUT_INV

Description: Port output data invert register

Address: 0x4281068C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	Reserved	RW	RW	RW	RW	Reserved
HW Access	A	A	Reserved	A	A	A	A	Reserved
Name	OUT7	OUT6	Reserved	OUT4	OUT3	OUT2	OUT1	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO invert output for pin 7 Default Value: 0
6	OUT6	IO invert output for pin 6 Default Value: 0
4	OUT4	IO invert output for pin 4 Default Value: 0
3	OUT3	IO invert output for pin 3 Default Value: 0
2	OUT2	IO invert output for pin 2 Default Value: 0
1	OUT1	IO invert output for pin 1 Default Value: 0

16.1.87 GPIO_PRT13_CFG

Description: Port configuration register

Address: 0x428106C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	Reserved		
HW Access	R	R			R	Reserved		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	Reserved [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	Reserved			RW	RW		
HW Access	R	Reserved			R	R		
Name	IN_EN5	Reserved [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0

16.1.87 GPIO_PRT13_CFG (continued)

26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :** **0x3: PULLDOWN :** **0x4: OD_DRIVESLOW :** **0x5: OD_DRIVESHIGH :** **0x6: STRONG :** **0x7: PULLUP_DOWN :**
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0 **0x0: CFG3_EN :** **0x1: RESERVED :** **0x2: PULLUP :**

16.1.87 GPIO_PRT13_CFG (continued)

		0x3: PULLDOWN :
		0x4: OD_DRIVESLOW :
		0x5: OD_DRIVESHIGH :
		0x6: STRONG :
		0x7: PULLUP_DOWN :
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
		0x0: CFG3_EN :
		0x1: RESERVED :
		0x2: PULLUP :
		0x3: PULLDOWN :
		0x4: OD_DRIVESLOW :
		0x5: OD_DRIVESHIGH :
		0x6: STRONG :
		0x7: PULLUP_DOWN :
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
		0x0: CFG3_EN :
		0x1: RESERVED :
		0x2: PULLUP :
		0x3: PULLDOWN :
		0x4: OD_DRIVESLOW :
		0x5: OD_DRIVESHIGH :
		0x6: STRONG :
		0x7: PULLUP_DOWN :

16.1.87 GPIO_PRT13_CFG (continued)

3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0

16.1.88 GPIO_PRT13_CFG_OUT

Description: Port output buffer configuration register

Address: 0x428106CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	Reserved	RW	RW	RW	RW	Reserved
HW Access	R	R	Reserved	R	R	R	R	Reserved
Name	SLOW7	SLOW6	Reserved	SLOW4	SLOW3	SLOW2	SLOW1	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		Reserved	
HW Access	R		R		R		Reserved	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		Reserved [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		Reserved		RW	
HW Access	R		R		Reserved		R	
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		Reserved [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
7	SLOW7	Enables slow slew rate for IO pin 7 Default Value: 0
6	SLOW6	Enables slow slew rate for IO pin 6 Default Value: 0
4	SLOW4	Enables slow slew rate for IO pin 4 Default Value: 0
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0

16.1.88 GPIO_PRT13_CFG_OUT (continued)

1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0

16.1.89 GPIO_PRT18_CFG

Description: Port configuration register

Address: 0x42810944

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved			RW	Reserved		
HW Access	R	Reserved			R	Reserved		
Name	IN_EN1	Reserved [6:4]			IN_EN0	Reserved [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0

16.1.90 GPIO_SEC_INTR_CAUSE0

Description: Secure Interrupt port cause register 0

Address: 0x42817000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	PORT_INT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [23:22]		PORT_INT [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a combined interrupt line "gpio_interrupt". The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PRT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt. '0': Port has no pending interrupt '1': Port has pending interrupt Default Value: 0

16.1.91 GPIO_INTR_CAUSE0

Description: Interrupt port cause register 0

Address: 0x42818000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	PORT_INT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [23:22]		PORT_INT [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a combined interrupt line "gpio_interrupt". The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PRT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt. '0': Port has no pending interrupt '1': Port has pending interrupt Default Value: 0

16.1.92 GPIO_VDD_ACTIVE

Description: Extern power supply detection register

Address: 0x42818010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							VDDIO_ACTIVE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	Reserved					
HW Access	W	W	Reserved					
Name	VDDD_ACTIVE	VDDA_ACTIVE	Reserved [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	This bit indicates presence of the VDDD supply. This bit will always read-back 1. The VDDD supply has robust brown-out protection monitoring and it is not possible to read back this register without a valid supply. (This bit is used in certain test-modes to observe the brown-out detector status.) Default Value: 1
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
0	VDDIO_ACTIVE	Indicates presence or absence of VDDIO supplies (i.e. other than VDDD, VDDA) on the device (supplies are numbered 0..n-1). Note that VDDIO supplies have basic (crude) supply detectors only. If separate, robust, brown-out detection is desired on IO supplies, on-chip or off-chip analog resources need to provide it. For these bits to work reliable, the supply must be within valid spec range (per datasheet) or held at ground. Any in-between voltage has an undefined result. '0': Supply is not present '1': Supply is present When multiple VDDIO supplies are present, they will be assigned in alphanumeric ascending order to these bits during implementation. For example "vddusb, vddio_0, vddio_a, vbackup, vddio_r, vddio_1" are present then they will be assigned to these bits as below: 0: vbackup, 1: vddio_0, 2: vddio_1, 3: vddio_a, 4: vddio_r, 5: vddusb" Default Value: 0

16.1.93 GPIO_VDD_INTR

Description: Supply detection interrupt register

Address: 0x42818014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [7:1]							VDDIO_ACTIVE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	RW1C	Reserved					
HW Access	A	A	Reserved					
Name	VDDD_ACTIVE	VDDA_ACTIVE	Reserved [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	The VDDD supply is always present during operation so a supply transition can not occur. This bit will always read back '1'. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
0	VDDIO_ACTIVE	Supply state change detected. '0': No change to supply detected '1': Change to supply detected Default Value: 0

16.1.94 GPIO_VDD_INTR_MASK

Description: Supply detection interrupt mask register

Address: 0x42818018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							VDDIO_ACTIVE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved					
HW Access	R	R	Reserved					
Name	VDDD_ACTIVE	VDDA_ACTIVE	Reserved [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
0	VDDIO_ACTIVE	Masks supply interrupt on VDDIO. '0': VDDIO interrupt forwarding disabled '1': VDDIO interrupt forwarding enabled Default Value: 0

16.1.95 GPIO_VDD_INTR_MASKED

Description: Supply detection interrupt masked register

Address: 0x4281801C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							VDDIO_ACTIVE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	Reserved					
HW Access	W	W	Reserved					
Name	VDDD_ACTIVE	VDDA_ACTIVE	Reserved [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
0	VDDIO_ACTIVE	Supply transition detected AND masked '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.96 GPIO_VDD_INTR_SET

Description: Supply detection interrupt set register

Address: 0x42818020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							VDDIO_ACTIVE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW1S	Reserved					
HW Access	A	A	Reserved					
Name	VDDD_ACTIVE	VDDA_ACTIVE	Reserved [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
0	VDDIO_ACTIVE	Sets supply interrupt. '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16.1.97 GPIO_VDD_MODE_SEL

Description: Supply mode select for 3.3V domains

Address: 0x42818024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							MODE_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	MODE_SEL	Applicable if domain is 3.3V only, no impact to 1.8V domains This bit will be used to turn-off PGND bias circuit to save power. 1 - Corresponding 3.3V IO domain is in 3.3V mode 0 - Corresponding 3.3V IO domain is in 1.8V mode Default Value: 1

16.1.98 SMARTIO_PRT11_CTL

Description: Control register

Address: 0x42820B00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			CLOCK_SRC [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved					RW	RW
HW Access	R	Reserved					R	R
Name	ENABLED	Reserved [30:26]					PIPE-LINE_EN	HLD_OVR

Bits	Name	Description
31	ENABLED	Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated. If the IP is disabled: - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to "20"-"30" (clock is constant '0'), to ensure low power consumption. '1': Enabled. Once enabled, it takes 3 "clk_fabric" clock cycles till the fabric reset is de-activated and the fabric becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the fabric is fully functional. Default Value: 0
25	PIPELINE_EN	Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled. Default Value: 1

16.1.98 SMARTIO_PRT11_CTL (continued)

24	HLD_OVR	IO cell hold override functionality. In DeepSleep power mode, the HSIOM holds the IO cell output and output enable signals if Active functionality is connected to the IO pads. This is undesirable if the SMARTIO is supposed to deliver DeepSleep output functionality on these IO pads. This field is used to control the hold override functionality from the SMARTIO: '0': The HSIOM controls the IO cell hold override functionality ("hsiom_hld_ovr"). '1': The SMARTIO controls the IO cel hold override functionality: - In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM control is used. - In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the SMARTIO sets hold override to "pwr_hld_ovr_hib" to enable SMARTIO functionality in DeepSleep power mode (but disables it in Hibernate or Stop power mode). Default Value: Undefined
12 : 8	CLOCK_SRC	Clock ("clk_fabric") and reset ("rst_fabric_n") source selection: "0": io_data_in[0]/'1'. ... "7": io_data_in[7]/'1'. "8": chip_data[0]/'1'. ... "15": chip_data[7]/'1'. "16": clk_smartio/rst_sys_act_n. Used for both Active functionality synchronous logic on "clk_smartio". This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_smartio_pos_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "17": clk_smartio/rst_sys_dpslp_n. Used for both DeepSleep functionality synchronous logic on "clk_smartio" (note that "clk_smartio" is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_smartio_pos_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "18": Same as "17". Note that the M0S8 SMARTIO version used the Hibernate reset for this value, but the MXS40 SMARTIO version does not support Hibernate functionality. "19": clk_lf/rst_lf_dpslp_n (note that "clk_lf" is available in DeepSleep power mode). This selection is intended for synchronous operation on"clk_lf". Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to other "clk_lf" clocked elements. "20"-"30": Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption. "31": asynchronous mode/'1'. Select this when clockless operation is configured. NOTE: Two positive edges of the selected clock are required for the block to be enabled (to deactivate reset). In asynchronous (clockless) mode clk_sys is used to enable the block, but is not available for clocking. Default Value: 0x14
7 : 0	BYPASS	Bypass of the programmable IO, one bit for each IO pin: BYPASS[i] is for IO pin i. When ENABLED is '1', this field is used. When ENABLED is '0', this field is NOT used and SMARTIO fabric is always bypassed. '0': No bypass (programmable SMARTIO fabric is exposed). '1': Bypass (programmable SMARTIOIO fabric is hidden). Default Value: Undefined

16.1.99 SMARTIO_PRT11_SYNC_CTL

Description: Synchronization control register

Address: 0x42820B10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IO_SYNC_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHIP_SYNC_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	CHIP_SYNC_EN	Synchronization of the chip input signals to "clk_fabric", one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization. Default Value: Undefined
7 : 0	IO_SYNC_EN	Synchronization of the IO pin input signals to "clk_fabric", one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization. Default Value: Undefined

16.1.100 SMARTIO_PRT11_LUT_SEL0

Description: LUT component input selection

Address: 0x42820B20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

16.1.100 SMARTIO_PRT11_LUT_SEL0 (continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

16.1.101 SMARTIO_PRT11_LUT_CTL0

Description: LUT component control register

Address: 0x42820B40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined
7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

16.1.102 SMARTIO_PRT11_DU_SEL

Description: Data unit component input selection

Address: 0x42820BC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				DU_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				DU_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				DU_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW		Reserved		RW	
HW Access	Reserved		R		Reserved		R	
Name	Reserved [31:30]		DU_DATA1_SEL [29:28]		Reserved [27:26]		DU_DATA0_SEL [25:24]	

Bits	Name	Description
29 : 28	DU_DATA1_SEL	Data unit input data "data1_in" source selection. Encoding is the same as for DU_DATA0_SEL. Default Value: Undefined
25 : 24	DU_DATA0_SEL	Data unit input data "data0_in" source selection: "0": Constant "0". "1": chip_data[7:0]. "2": io_data_in[7:0]. "3": DATA.DATA MMIO register field. Default Value: Undefined
19 : 16	DU_TR2_SEL	Data unit input signal "tr2_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
11 : 8	DU_TR1_SEL	Data unit input signal "tr1_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
3 : 0	DU_TR0_SEL	Data unit input signal "tr0_in" source selection: "0": Constant '0'. "1": Constant '1'. "2": Data unit output. "10-3": LUT 7 - 0 outputs. Otherwise: Undefined. Default Value: Undefined

16.1.103 SMARTIO_PRT11_DU_CTL

Description: Data unit component control register

Address: 0x42820BC4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					DU_SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				DU_OPC [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11 : 8	DU_OPC	Data unit opcode specifies the data unit operation: "1": INCR "2": DECR "3": INCR_WRAP "4": DECR_WRAP "5": INCR_DECR "6": INCR_DECR_WRAP "7": ROR "8": SHR "9": AND_OR "10": SHR_MAJ3 "11": SHR_EQL. Otherwise: Undefined. Default Value: Undefined
2 : 0	DU_SIZE	Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. Default Value: Undefined

16.1.104 SMARTIO_PRT11_DATA

Description: Data register

Address: 0x42820BF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DATA	Data unit input data source. Default Value: Undefined

17 Timer, Counter, PWM (TCPWM) registers

This section discusses the TCPWM registers. It lists all the registers in mapping tables, in address order.

17.1 Register details

Register name	Address	Description
TCPWM0_GRP0_CNT0_CTRL	0x42860000	Counter control register
TCPWM0_GRP0_CNT0_STATUS	0x42860004	Counter status register
TCPWM0_GRP0_CNT0_COUNTER	0x42860008	Counter count register
TCPWM0_GRP0_CNT0_CC0	0x42860010	Counter compare/capture 0 register
TCPWM0_GRP0_CNT0_CC0_BUFF	0x42860014	Counter buffered compare/capture 0 register
TCPWM0_GRP0_CNT0_PERIOD	0x42860020	Counter period register
TCPWM0_GRP0_CNT0_PERIOD_BUFF	0x42860024	Counter buffered period register
TCPWM0_GRP0_CNT0_DT	0x42860030	Counter PWM dead time register
TCPWM0_GRP0_CNT0_TR_CMD	0x42860040	Counter trigger command register
TCPWM0_GRP0_CNT0_TR_IN_SEL0	0x42860044	Counter input trigger selection register 0
TCPWM0_GRP0_CNT0_TR_IN_SEL1	0x42860048	Counter input trigger selection register 1
TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL	0x4286004C	Counter input trigger edge selection register
TCPWM0_GRP0_CNT0_TR_PWM_CTRL	0x42860050	Counter trigger PWM control register
TCPWM0_GRP0_CNT0_TR_OUT_SEL	0x42860054	Counter output trigger selection register
TCPWM0_GRP0_CNT0_INTR	0x42860070	Interrupt request register
TCPWM0_GRP0_CNT0_INTR_SET	0x42860074	Interrupt set request register
TCPWM0_GRP0_CNT0_INTR_MASK	0x42860078	Interrupt mask register
TCPWM0_GRP0_CNT0_INTR_MASKED	0x4286007C	Interrupt masked request register
TCPWM0_GRP0_CNT1_CTRL	0x42860080	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT1_STATUS	0x42860084	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT1_COUNTER	0x42860088	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT1_CC0	0x42860090	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT1_CC0_BUFF	0x42860094	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT1_PERIOD	0x428600A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP0_CNT1_PERIOD_BUFF	0x428600A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT1_DT	0x428600B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_CMD	0x428600C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_SEL0	0x428600C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_SEL1	0x428600C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_EDGE_SEL	0x428600CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_PWM_CTRL	0x428600D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_OUT_SEL	0x428600D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR	0x428600F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_SET	0x428600F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_MASK	0x428600F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_MASKED	0x428600FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT2_CTRL	0x42860100	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT2_STATUS	0x42860104	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT2_COUNTER	0x42860108	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT2_CC0	0x42860110	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT2_CC0_BUFF	0x42860114	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_PERIOD	0x42860120	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT2_PERIOD_BUFF	0x42860124	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_DT	0x42860130	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_CMD	0x42860140	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_SEL0	0x42860144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_SEL1	0x42860148	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_EDGE_SEL	0x4286014C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_PWM_CTRL	0x42860150	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_OUT_SEL	0x42860154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR	0x42860170	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR_SET	0x42860174	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR_MASK	0x42860178	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR_MASKED	0x4286017C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP0_CNT3_CTRL	0x42860180	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT3_STATUS	0x42860184	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT3_COUNTER	0x42860188	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT3_CC0	0x42860190	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT3_CC0_BUFF	0x42860194	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_PERIOD	0x428601A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT3_PERIOD_BUFF	0x428601A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_DT	0x428601B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_CMD	0x428601C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_SEL0	0x428601C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_SEL1	0x428601C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_EDGE_SEL	0x428601CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_PWM_CTRL	0x428601D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_OUT_SEL	0x428601D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR	0x428601F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP0_CNT3_INTR_SET	0x428601F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_MASK	0x428601F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_MASKED	0x428601FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT4_CTRL	0x42860200	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT4_STATUS	0x42860204	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT4_COUNTER	0x42860208	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT4_CC0	0x42860210	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT4_CC0_BUFF	0x42860214	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT4_PERIOD	0x42860220	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT4_PERIOD_BUFF	0x42860224	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT4_DT	0x42860230	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT4_TR_CMD	0x42860240	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT4_TR_IN_SEL0	0x42860244	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT4_TR_IN_SEL1	0x42860248	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT4_TR_IN_EDGE_SEL	0x4286024C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP0_CNT4_TR_PWM_CTRL	0x42860250	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT4_TR_OUT_SEL	0x42860254	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT4_INTR	0x42860270	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT4_INTR_SET	0x42860274	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT4_INTR_MASK	0x42860278	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT4_INTR_MASKED	0x4286027C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT5_CTRL	0x42860280	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT5_STATUS	0x42860284	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT5_COUNTER	0x42860288	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT5_CC0	0x42860290	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT5_CC0_BUFF	0x42860294	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT5_PERIOD	0x428602A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT5_PERIOD_BUFF	0x428602A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT5_DT	0x428602B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_CMD	0x428602C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP0_CNT5_TR_IN_SEL0	0x428602C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_IN_SEL1	0x428602C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_IN_EDGE_SEL	0x428602CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_PWM_CTRL	0x428602D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_OUT_SEL	0x428602D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT5_INTR	0x428602F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT5_INTR_SET	0x428602F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT5_INTR_MASK	0x428602F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT5_INTR_MASKED	0x428602FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT6_CTRL	0x42860300	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT6_STATUS	0x42860304	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT6_COUNTER	0x42860308	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT6_CC0	0x42860310	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT6_CC0_BUFF	0x42860314	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT6_PERIOD	0x42860320	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT6_PERIOD_BUFF	0x42860324	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT6_DT	0x42860330	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_CMD	0x42860340	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_IN_SEL0	0x42860344	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_IN_SEL1	0x42860348	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_IN_EDGE_SEL	0x4286034C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_PWM_CTRL	0x42860350	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_OUT_SEL	0x42860354	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT6_INTR	0x42860370	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT6_INTR_SET	0x42860374	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT6_INTR_MASK	0x42860378	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT6_INTR_MASKED	0x4286037C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT7_CTRL	0x42860380	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT7_STATUS	0x42860384	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT7_COUNTER	0x42860388	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT7_CC0	0x42860390	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT7_CC0_BUFF	0x42860394	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT7_PERIOD	0x428603A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT7_PERIOD_BUFF	0x428603A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT7_DT	0x428603B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_CMD	0x428603C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_IN_SEL0	0x428603C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_IN_SEL1	0x428603C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_IN_EDGE_SEL	0x428603CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_PWM_CTRL	0x428603D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_OUT_SEL	0x428603D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT7_INTR	0x428603F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT7_INTR_SET	0x428603F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT7_INTR_MASK	0x428603F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT7_INTR_MASKED	0x428603FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT0_CTRL	0x42868000	Counter control register
TCPWM0_GRP1_CNT0_STATUS	0x42868004	Counter status register
TCPWM0_GRP1_CNT0_COUNTER	0x42868008	Counter count register
TCPWM0_GRP1_CNT0_CC0	0x42868010	Counter compare/capture 0 register
TCPWM0_GRP1_CNT0_CC0_BUFF	0x42868014	Counter buffered compare/capture 0 register
TCPWM0_GRP1_CNT0_CC1	0x42868018	Counter compare/capture 1 register
TCPWM0_GRP1_CNT0_CC1_BUFF	0x4286801C	Counter buffered compare/capture 1 register
TCPWM0_GRP1_CNT0_PERIOD	0x42868020	Counter period register
TCPWM0_GRP1_CNT0_PERIOD_BUFF	0x42868024	Counter buffered period register
TCPWM0_GRP1_CNT0_DT	0x42868030	Counter PWM dead time register
TCPWM0_GRP1_CNT0_TR_CMD	0x42868040	Counter trigger command register
TCPWM0_GRP1_CNT0_TR_IN_SEL0	0x42868044	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_IN_SEL1	0x42868048	Counter input trigger selection register 1
TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL	0x4286804C	Counter input trigger edge selection register
TCPWM0_GRP1_CNT0_TR_PWM_CTRL	0x42868050	Counter trigger PWM control register
TCPWM0_GRP1_CNT0_TR_OUT_SEL	0x42868054	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT0_INTR	0x42868070	Interrupt request register
TCPWM0_GRP1_CNT0_INTR_SET	0x42868074	Interrupt set request register
TCPWM0_GRP1_CNT0_INTR_MASK	0x42868078	Interrupt mask register
TCPWM0_GRP1_CNT0_INTR_MASKED	0x4286807C	Interrupt masked request register
TCPWM0_GRP1_CNT1_CTRL	0x42868080	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT1_STATUS	0x42868084	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT1_COUNTER	0x42868088	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT1_CC0	0x42868090	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT1_CC0_BUFF	0x42868094	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_CC1	0x42868098	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT1_CC1_BUFF	0x4286809C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_PERIOD	0x428680A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT1_PERIOD_BUFF	0x428680A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_DT	0x428680B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_CMD	0x428680C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_SEL0	0x428680C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_SEL1	0x428680C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_EDGE_SEL	0x428680CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_PWM_CTRL	0x428680D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_OUT_SEL	0x428680D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR	0x428680F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR_SET	0x428680F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR_MASK	0x428680F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR_MASKED	0x428680FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT2_CTRL	0x42868100	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT2_STATUS	0x42868104	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT2_COUNTER	0x42868108	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT2_CC0	0x42868110	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT2_CC0_BUFF	0x42868114	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_CC1	0x42868118	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT2_CC1_BUFF	0x4286811C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_PERIOD	0x42868120	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT2_PERIOD_BUFF	0x42868124	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_DT	0x42868130	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_CMD	0x42868140	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_SEL0	0x42868144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_SEL1	0x42868148	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_EDGE_SEL	0x4286814C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_PWM_CTRL	0x42868150	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_OUT_SEL	0x42868154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT2_INTR	0x42868170	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_SET	0x42868174	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_MASK	0x42868178	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_MASKED	0x4286817C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT3_CTRL	0x42868180	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT3_STATUS	0x42868184	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT3_COUNTER	0x42868188	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT3_CC0	0x42868190	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT3_CC0_BUFF	0x42868194	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_CC1	0x42868198	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT3_CC1_BUFF	0x4286819C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_PERIOD	0x428681A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT3_PERIOD_BUFF	0x428681A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_DT	0x428681B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_CMD	0x428681C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT3_TR_IN_SEL0	0x428681C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_IN_SEL1	0x428681C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_IN_EDGE_SEL	0x428681CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_PWM_CTRL	0x428681D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_OUT_SEL	0x428681D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR	0x428681F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_SET	0x428681F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_MASK	0x428681F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_MASKED	0x428681FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT4_CTRL	0x42868200	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT4_STATUS	0x42868204	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT4_COUNTER	0x42868208	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT4_CC0	0x42868210	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT4_CC0_BUFF	0x42868214	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_CC1	0x42868218	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT4_CC1_BUFF	0x4286821C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_PERIOD	0x42868220	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT4_PERIOD_BUFF	0x42868224	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_DT	0x42868230	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_CMD	0x42868240	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_SEL0	0x42868244	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_SEL1	0x42868248	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_EDGE_SEL	0x4286824C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_PWM_CTRL	0x42868250	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_OUT_SEL	0x42868254	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR	0x42868270	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_SET	0x42868274	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_MASK	0x42868278	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_MASKED	0x4286827C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT5_CTRL	0x42868280	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT5_STATUS	0x42868284	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT5_COUNTER	0x42868288	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT5_CC0	0x42868290	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT5_CC0_BUFF	0x42868294	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_CC1	0x42868298	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT5_CC1_BUFF	0x4286829C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_PERIOD	0x428682A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT5_PERIOD_BUFF	0x428682A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_DT	0x428682B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_CMD	0x428682C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_SEL0	0x428682C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_SEL1	0x428682C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_EDGE_SEL	0x428682CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_PWM_CTRL	0x428682D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_OUT_SEL	0x428682D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT5_INTR	0x428682F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_SET	0x428682F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_MASK	0x428682F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_MASKED	0x428682FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT6_CTRL	0x42868300	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT6_STATUS	0x42868304	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT6_COUNTER	0x42868308	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT6_CC0	0x42868310	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT6_CC0_BUFF	0x42868314	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_CC1	0x42868318	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT6_CC1_BUFF	0x4286831C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_PERIOD	0x42868320	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT6_PERIOD_BUFF	0x42868324	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_DT	0x42868330	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_CMD	0x42868340	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT6_TR_IN_SEL0	0x42868344	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_IN_SEL1	0x42868348	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_IN_EDGE_SEL	0x4286834C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_PWM_CTRL	0x42868350	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_OUT_SEL	0x42868354	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR	0x42868370	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_SET	0x42868374	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_MASK	0x42868378	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_MASKED	0x4286837C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT7_CTRL	0x42868380	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT7_STATUS	0x42868384	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT7_COUNTER	0x42868388	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT7_CC0	0x42868390	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT7_CC0_BUFF	0x42868394	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_CC1	0x42868398	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT7_CC1_BUFF	0x4286839C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_PERIOD	0x428683A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT7_PERIOD_BUFF	0x428683A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_DT	0x428683B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_CMD	0x428683C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_SEL0	0x428683C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_SEL1	0x428683C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_EDGE_SEL	0x428683CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_PWM_CTRL	0x428683D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_OUT_SEL	0x428683D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR	0x428683F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_SET	0x428683F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_MASK	0x428683F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_MASKED	0x428683FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT8_CTRL	0x42868400	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT8_STATUS	0x42868404	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT8_COUNTER	0x42868408	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT8_CC0	0x42868410	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT8_CC0_BUFF	0x42868414	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT8_CC1	0x42868418	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT8_CC1_BUFF	0x4286841C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT8_PERIOD	0x42868420	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT8_PERIOD_BUFF	0x42868424	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT8_DT	0x42868430	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_CMD	0x42868440	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_IN_SEL0	0x42868444	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_IN_SEL1	0x42868448	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_IN_EDGE_SEL	0x4286844C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_PWM_CTRL	0x42868450	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_OUT_SEL	0x42868454	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT8_INTR	0x42868470	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT8_INTR_SET	0x42868474	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT8_INTR_MASK	0x42868478	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT8_INTR_MASKED	0x4286847C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT9_CTRL	0x42868480	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT9_STATUS	0x42868484	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT9_COUNTER	0x42868488	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT9_CC0	0x42868490	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT9_CC0_BUFF	0x42868494	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT9_CC1	0x42868498	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT9_CC1_BUFF	0x4286849C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT9_PERIOD	0x428684A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT9_PERIOD_BUFF	0x428684A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT9_DT	0x428684B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT9_TR_CMD	0x428684C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT9_TR_IN_SEL0	0x428684C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT9_TR_IN_SEL1	0x428684C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT9_TR_IN_EDGE_SEL	0x428684CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT9_TR_PWM_CTRL	0x428684D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT9_TR_OUT_SEL	0x428684D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT9_INTR	0x428684F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT9_INTR_SET	0x428684F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT9_INTR_MASK	0x428684F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT9_INTR_MASKED	0x428684FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT10_CTRL	0x42868500	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT10_STATUS	0x42868504	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT10_COUNTER	0x42868508	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT10_CC0	0x42868510	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT10_CC0_BUFF	0x42868514	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT10_CC1	0x42868518	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT10_CC1_BUFF	0x4286851C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT10_PERIOD	0x42868520	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT10_PERIOD_BUFF	0x42868524	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT10_DT	0x42868530	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_CMD	0x42868540	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_IN_SEL0	0x42868544	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_IN_SEL1	0x42868548	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_IN_EDGE_SEL	0x4286854C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_PWM_CTRL	0x42868550	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_OUT_SEL	0x42868554	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT10_INTR	0x42868570	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT10_INTR_SET	0x42868574	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT10_INTR_MASK	0x42868578	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT10_INTR_MASKED	0x4286857C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT11_CTRL	0x42868580	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT11_STATUS	0x42868584	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT11_COUNTER	0x42868588	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT11_CC0	0x42868590	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT11_CC0_BUFF	0x42868594	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT11_CC1	0x42868598	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT11_CC1_BUFF	0x4286859C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT11_PERIOD	0x428685A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT11_PERIOD_BUFF	0x428685A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT11_DT	0x428685B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_CMD	0x428685C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_IN_SEL0	0x428685C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_IN_SEL1	0x428685C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_IN_EDGE_SEL	0x428685CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_PWM_CTRL	0x428685D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_OUT_SEL	0x428685D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT11_INTR	0x428685F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT11_INTR_SET	0x428685F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT11_INTR_MASK	0x428685F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT11_INTR_MASKED	0x428685FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT12_CTRL	0x42868600	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT12_STATUS	0x42868604	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT12_COUNTER	0x42868608	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT12_CC0	0x42868610	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT12_CC0_BUFF	0x42868614	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT12_CC1	0x42868618	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT12_CC1_BUFF	0x4286861C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT12_PERIOD	0x42868620	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT12_PERIOD_BUFF	0x42868624	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT12_DT	0x42868630	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT12_TR_CMD	0x42868640	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT12_TR_IN_SEL0	0x42868644	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT12_TR_IN_SEL1	0x42868648	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT12_TR_IN_EDGE_SEL	0x4286864C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT12_TR_PWM_CTRL	0x42868650	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT12_TR_OUT_SEL	0x42868654	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT12_INTR	0x42868670	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT12_INTR_SET	0x42868674	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT12_INTR_MASK	0x42868678	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT12_INTR_MASKED	0x4286867C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT13_CTRL	0x42868680	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT13_STATUS	0x42868684	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT13_COUNTER	0x42868688	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT13_CC0	0x42868690	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT13_CC0_BUFF	0x42868694	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT13_CC1	0x42868698	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT13_CC1_BUFF	0x4286869C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT13_PERIOD	0x428686A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT13_PERIOD_BUFF	0x428686A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT13_DT	0x428686B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT13_TR_CMD	0x428686C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT13_TR_IN_SEL0	0x428686C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT13_TR_IN_SEL1	0x428686C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT13_TR_IN_EDGE_SEL	0x428686CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT13_TR_PWM_CTRL	0x428686D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT13_TR_OUT_SEL	0x428686D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT13_INTR	0x428686F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT13_INTR_SET	0x428686F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT13_INTR_MASK	0x428686F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT13_INTR_MASKED	0x428686FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT14_CTRL	0x42868700	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT14_STATUS	0x42868704	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT14_COUNTER	0x42868708	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT14_CC0	0x42868710	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT14_CC0_BUFF	0x42868714	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT14_CC1	0x42868718	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT14_CC1_BUFF	0x4286871C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT14_PERIOD	0x42868720	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT14_PERIOD_BUFF	0x42868724	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT14_DT	0x42868730	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT14_TR_CMD	0x42868740	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT14_TR_IN_SEL0	0x42868744	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT14_TR_IN_SEL1	0x42868748	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT14_TR_IN_EDGE_SEL	0x4286874C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT14_TR_PWM_CTRL	0x42868750	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT14_TR_OUT_SEL	0x42868754	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT14_INTR	0x42868770	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT14_INTR_SET	0x42868774	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT14_INTR_MASK	0x42868778	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT14_INTR_MASKED	0x4286877C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT15_CTRL	0x42868780	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT15_STATUS	0x42868784	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT15_COUNTER	0x42868788	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT15_CC0	0x42868790	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT15_CC0_BUFF	0x42868794	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT15_CC1	0x42868798	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT15_CC1_BUFF	0x4286879C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT15_PERIOD	0x428687A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT15_PERIOD_BUFF	0x428687A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT15_DT	0x428687B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT15_TR_CMD	0x428687C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT15_TR_IN_SEL0	0x428687C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT15_TR_IN_SEL1	0x428687C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT15_TR_IN_EDGE_SEL	0x428687CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT15_TR_PWM_CTRL	0x428687D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT15_TR_OUT_SEL	0x428687D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT15_INTR	0x428687F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT15_INTR_SET	0x428687F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT15_INTR_MASK	0x428687F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT15_INTR_MASKED	0x428687FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT16_CTRL	0x42868800	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT16_STATUS	0x42868804	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT16_COUNTER	0x42868808	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT16_CC0	0x42868810	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT16_CC0_BUFF	0x42868814	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT16_CC1	0x42868818	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT16_CC1_BUFF	0x4286881C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT16_PERIOD	0x42868820	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT16_PERIOD_BUFF	0x42868824	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT16_DT	0x42868830	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT16_TR_CMD	0x42868840	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT16_TR_IN_SEL0	0x42868844	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT16_TR_IN_SEL1	0x42868848	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT16_TR_IN_EDGE_SEL	0x4286884C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT16_TR_PWM_CTRL	0x42868850	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT16_TR_OUT_SEL	0x42868854	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT16_INTR	0x42868870	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT16_INTR_SET	0x42868874	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT16_INTR_MASK	0x42868878	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT16_INTR_MASKED	0x4286887C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT17_CTRL	0x42868880	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT17_STATUS	0x42868884	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT17_COUNTER	0x42868888	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT17_CC0	0x42868890	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT17_CC0_BUFF	0x42868894	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT17_CC1	0x42868898	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT17_CC1_BUFF	0x4286889C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT17_PERIOD	0x428688A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT17_PERIOD_BUFF	0x428688A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT17_DT	0x428688B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT17_TR_CMD	0x428688C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT17_TR_IN_SEL0	0x428688C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT17_TR_IN_SEL1	0x428688C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT17_TR_IN_EDGE_SEL	0x428688CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT17_TR_PWM_CTRL	0x428688D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT17_TR_OUT_SEL	0x428688D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT17_INTR	0x428688F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT17_INTR_SET	0x428688F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT17_INTR_MASK	0x428688F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT17_INTR_MASKED	0x428688FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT18_CTRL	0x42868900	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT18_STATUS	0x42868904	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT18_COUNTER	0x42868908	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT18_CC0	0x42868910	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT18_CC0_BUFF	0x42868914	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT18_CC1	0x42868918	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT18_CC1_BUFF	0x4286891C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT18_PERIOD	0x42868920	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT18_PERIOD_BUFF	0x42868924	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT18_DT	0x42868930	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT18_TR_CMD	0x42868940	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT18_TR_IN_SEL0	0x42868944	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT18_TR_IN_SEL1	0x42868948	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT18_TR_IN_EDGE_SEL	0x4286894C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT18_TR_PWM_CTRL	0x42868950	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT18_TR_OUT_SEL	0x42868954	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT18_INTR	0x42868970	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT18_INTR_SET	0x42868974	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT18_INTR_MASK	0x42868978	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT18_INTR_MASKED	0x4286897C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT19_CTRL	0x42868980	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT19_STATUS	0x42868984	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT19_COUNTER	0x42868988	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT19_CC0	0x42868990	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT19_CC0_BUFF	0x42868994	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT19_CC1	0x42868998	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT19_CC1_BUFF	0x4286899C	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT19_PERIOD	0x428689A0	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT19_PERIOD_BUFF	0x428689A4	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT19_DT	0x428689B0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT19_TR_CMD	0x428689C0	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT19_TR_IN_SEL0	0x428689C4	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT19_TR_IN_SEL1	0x428689C8	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT19_TR_IN_EDGE_SEL	0x428689CC	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT19_TR_PWM_CTRL	0x428689D0	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT19_TR_OUT_SEL	0x428689D4	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT19_INTR	0x428689F0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT19_INTR_SET	0x428689F4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT19_INTR_MASK	0x428689F8	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT19_INTR_MASKED	0x428689FC	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT20_CTRL	0x42868A00	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT20_STATUS	0x42868A04	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT20_COUNTER	0x42868A08	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT20_CC0	0x42868A10	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT20_CC0_BUFF	0x42868A14	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT20_CC1	0x42868A18	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT20_CC1_BUFF	0x42868A1C	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT20_PERIOD	0x42868A20	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT20_PERIOD_BUFF	0x42868A24	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT20_DT	0x42868A30	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT20_TR_CMD	0x42868A40	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT20_TR_IN_SEL0	0x42868A44	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT20_TR_IN_SEL1	0x42868A48	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT20_TR_IN_EDGE_SEL	0x42868A4C	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT20_TR_PWM_CTRL	0x42868A50	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT20_TR_OUT_SEL	0x42868A54	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT20_INTR	0x42868A70	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT20_INTR_SET	0x42868A74	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT20_INTR_MASK	0x42868A78	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT20_INTR_MASKED	0x42868A7C	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT21_CTRL	0x42868A80	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT21_STATUS	0x42868A84	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT21_COUNTER	0x42868A88	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT21_CC0	0x42868A90	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT21_CC0_BUFF	0x42868A94	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT21_CC1	0x42868A98	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT21_CC1_BUFF	0x42868A9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT21_PERIOD	0x42868AA0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT21_PERIOD_BUFF	0x42868AA4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT21_DT	0x42868AB0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT21_TR_CMD	0x42868AC0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT21_TR_IN_SEL0	0x42868AC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT21_TR_IN_SEL1	0x42868AC8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT21_TR_IN_EDGE_SEL	0x42868ACC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT21_TR_PWM_CTRL	0x42868AD0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT21_TR_OUT_SEL	0x42868AD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT21_INTR	0x42868AF0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT21_INTR_SET	0x42868AF4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT21_INTR_MASK	0x42868AF8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT21_INTR_MASKED	0x42868AFC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT22_CTRL	0x42868B00	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT22_STATUS	0x42868B04	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT22_COUNTER	0x42868B08	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT22_CC0	0x42868B10	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT22_CC0_BUFF	0x42868B14	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT22_CC1	0x42868B18	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT22_CC1_BUFF	0x42868B1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT22_PERIOD	0x42868B20	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT22_PERIOD_BUFF	0x42868B24	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT22_DT	0x42868B30	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT22_TR_CMD	0x42868B40	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT22_TR_IN_SEL0	0x42868B44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT22_TR_IN_SEL1	0x42868B48	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT22_TR_IN_EDGE_SEL	0x42868B4C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT22_TR_PWM_CTRL	0x42868B50	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT22_TR_OUT_SEL	0x42868B54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT22_INTR	0x42868B70	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT22_INTR_SET	0x42868B74	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT22_INTR_MASK	0x42868B78	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT22_INTR_MASKED	0x42868B7C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT23_CTRL	0x42868B80	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT23_STATUS	0x42868B84	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT23_COUNTER	0x42868B88	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT23_CC0	0x42868B90	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT23_CC0_BUFF	0x42868B94	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT23_CC1	0x42868B98	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT23_CC1_BUFF	0x42868B9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT23_PERIOD	0x42868BA0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT23_PERIOD_BUFF	0x42868BA4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT23_DT	0x42868BB0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT23_TR_CMD	0x42868BC0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT23_TR_IN_SEL0	0x42868BC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT23_TR_IN_SEL1	0x42868BC8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT23_TR_IN_EDGE_SEL	0x42868BCC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT23_TR_PWM_CTRL	0x42868BD0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT23_TR_OUT_SEL	0x42868BD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.

Timer, Counter, PWM (TCPWM) registers

Register name	Address	Description
TCPWM0_GRP1_CNT23_INTR	0x42868BF0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT23_INTR_SET	0x42868BF4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT23_INTR_MASK	0x42868BF8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT23_INTR_MASKED	0x42868BFC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.

17.1.1 TCPWM0_GRP0_CNT0_CTRL

Description: Counter control register

Address: 0x42860000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	Reserved	RW
HW Access	Reserved					R	Reserved	R
Name	Reserved [7:3]					AUTO_RELOAD_PERIOD	Reserved	AUTO_RELOAD_CC0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW		Reserved	RW	RW	RW
HW Access	Reserved		R		Reserved	R	R	R
Name	Reserved [15:14]		PWM_DISABLE_MODE [13:12]		Reserved	PWM_SYNC_KILL	PWM_STOP_ON_KILL	PWM_IMM_KILL

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		Reserved	RW	RW	
HW Access	Reserved		R		Reserved	R	R	
Name	Reserved [23:22]		QUAD_ENCODING_MODE [21:20]		Reserved	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved			RW		
HW Access	R	R	Reserved			R		
Name	ENABLED	DBG_FREEZE_EN	Reserved [29:27]			MODE [26:24]		

Bits	Name	Description
31	ENABLED	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0
30	DBG_FREEZE_EN	Specifies the counter behavior in debug mode. '0': The counter operation continues in debug mode. '1': The counter operation freezes in debug mode. Default Value: 0
26 : 24	MODE	Counter mode. Default Value: 0

17.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

0x0: TIMER :

Timer mode

0x1: Reserved1 :

N/A

0x2: CAPTURE :

Capture mode

0x3: QUAD :

Quadrature mode
Different encoding modes can be selected by QUAD_ENCODING_MODE including up/down count functionality.
Different counter range, reload value and capture behavior can be selected by QUAD_RANGE_-MODE (overloaded field UP_DOWN_MODE).

0x4: PWM :

Pulse width modulation (PWM) mode

0x5: PWM_DT :

PWM with deadtime insertion mode

0x6: PWM_PR :

Pseudo random pulse width modulation

0x7: SR :

Shift register mode.

21 : 20	QUAD_ENCODING_-MODE	In QUAD mode this field selects the quadrature encoding mode (X1/X2/X4) or the Up / Down rotary counting mode. In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUAD_ENCODING_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUAD_ENCODING_MODE[1]. Default Value: 0

0x0: X1 :

X1 encoding (QUAD mode)
This encoding is identical with an up / down counting functionality of the following way: Rising edges of input phiA increment or decrement the counter depending on the state of input phiB (direction input).

0x1: X2 :

X2 encoding (QUAD mode)

0x2: X4 :

X4 encoding (QUAD mode)

17.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

		0x3: UP_DOWN : Up / Down rotary counting mode. Input phiA increments the counter, input phiB decrements the counter. The trigger edge detection settings apply. **0x1: INV_OUT :** When bit 0 is '1', QUADRATURE_ENCODING_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: INV_COMPL_OUT :** When bit 1 is '1', QUADRATURE_ENCODING_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. In QUAD mode this field acts as QUAD_RANGE_MODE field selecting between different counter range, reload value and compare / capture behavior. Default Value: 0 **0x0: COUNT_UP :** Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD. **0x1: COUNT_DOWN :** Count down (to "0"). An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0". **0x2: COUNT_UPDN1 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0". **0x3: COUNT_UPDN2 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0" AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).

17.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

0x0: QUAD_RANGE0 :

In QUAD mode this setting selects the QUAD_RANGE0 mode with the following behavior:
- COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32)
- on reload / index event:
 - CC0 is copied to CC0_BUFF
 - COUNTER is copied to CC0
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - tc and cc0_match events are generated
- when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF:
 - CC0 is copied to CC0_BUFF
 - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to CC0
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - cc0_match event is generated

0x1: QUAD_RANGE0_CMP :

In QUAD mode this setting selects the QUAD_RANGE0_CMP mode with the following behavior:
- COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32)
- the capture0 event acts as 2nd reload / index event
- on reload / index event:
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - when 'capture on index' is selected (AUTO_RELOAD_PERIOD=0):
 - tc event is generated
 - PERIOD is copied to PERIOD_BUFF
 - COUNTER is copied to PERIOD
- when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF:
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - when 'capture on wrap-around' is selected (AUTO_RELOAD_PERIOD=1):
 - tc event is generated
 - PERIOD is copied to PERIOD_BUFF
 - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to PERIOD
- 1 or 2 compare functions (depending on CC1_PRESENT) available

This mode is to a certain extend backward compatible with previous TCPWM quadrature behavior but allows a compare function during quadrature decoding using the CC0/CC_BUFF registers and the cc0_match event. Because of that the PERIOD/PERIOD_BUFF registers are used instead of CC0/CC_BUFF registers to capture COUNTER at reload / index event or wrap-around.

17.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

0x2: QUAD_RANGE1_CAPT :

In QUAD mode this setting selects the QUAD_RANGE1_CAPT mode with the following behavior:
- COUNTER range is between 0x0000 and PERIOD
- on reload / index event:
 - COUNTER is set to 0x0000
 - tc event is generated
- when COUNTER is 0x0000 and decrementing:
 - COUNTER is set to PERIOD
 - tc event is generated
- when COUNTER equals PERIOD and is incrementing:
 - COUNTER is set to 0x0000
 - tc event is generated
- 1 or 2 capture functions (depending on CC1_PRESENT) available
- on capture0 / capture1 event:
 - CC0 / CC1 is copied to CC0_BUFF / CC1_BUFF
 - COUNTER value is copied to CC0

It allows that the COUNTER register reflects the current angle position of the rotary encoder, i.e. no MOD or SUB calculations need to be done in SW on the COUNTER value to get the current angle position. This allows a DMA copy of the angle position from the COUNTER register. However, a disadvantage of this mode is that fast sequences of tc interrupts can occur (when encoder moves back and forth around start position). It is recommended to not use the tc interrupt in this mode.

0x3: QUAD_RANGE1_CMP :

In QUAD mode this setting selects the QUAD_RANGE1_CMP mode.
The behavior is the same as for QUAD_RANGE1_CAPT mode described above with the only difference that 1 or 2 compare functions (depending on CC1_PRESENT) are available instead of 1 or 2 capture functions.

13 : 12	PWM_DISABLE_MODE	Specifies the behavior of the PWM outputs "line_out" and "line_compl_out" while the TCPWM counter is disabled (CTL.ENABLED='0') or stopped. Note: The output signal of this selection can be further modified by the immediate kill logic and line_out polarity settings (CTRL.QUAD_ENCODING_MODE). Default Value: 0

0x0: Z :

When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are NOT driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance).
Note: This is realized by driving the TCPWM output "line_out_en" to 0.
When the counter is stopped upon a stop event the PWM outputs are deactivated (to the polarity defined by CTL.QUAD_ENCODING_MODE).

0x1: RETAIN :

When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM.
When the counter is disabled or stopped upon a stop event the PWM outputs are retained (keep their previous levels).
While the counter is disabled or stopped the PWM outputs can be changed via LINE_SEL (when parameter GRP_SMC_PRESENT = 1).

0x2: L :

When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM.
When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '0' and the PWM output "line_compl_out" is driven as a fixed '1'.

17.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

		0x3: H : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '1' and the PWM output "line_compl_out" is driven as a fixed '0'.
10	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
9	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
8	PWM_IMM_KILL	Specifies whether the kill event immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals or with the next module clock ("active count" pre-scaled "clk_counter"). '0': synchronous kill activation. Deactivates the "dt_line_out" and "dt_line_compl_out" signals with the next module clock ("active count" pre-scaled "clk_counter"). '1': immediate kill activation. Immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff. Default Value: 0
0	AUTO_RELOAD_CC0	Specifies switching of the CC0 and buffered CC0 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 0 event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

17.1.2 TCPWM0_GRP0_CNT0_STATUS

Description: Counter status register

Address: 0x42860004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	Reserved			R
HW Access	RW	RW	RW	RW	Reserved			RW
Name	TR_STOP	TR_RE-LOAD	TR_COUNT	TR_CAP-TURE0	Reserved [3:1]			DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R	Reserved			R	R	Reserved	R
HW Access	RW	Reserved			RW	RW	Reserved	RW
Name	RUNNING	Reserved [14:12]			LINE_COM-PL_OUT	LINE_OUT	Reserved	TR_START

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DT_CNT_L [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	DT_CNT_L	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion (8bit dead time counter or low byte of 16-bit dead time counter). In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
15	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. This field is used to indicate that the counter is running after a start/reload event and that the counter is stopped after a stop event. When a running counter operation is paused in debug state (see CTRL.DBG_PAUSE) then the RUNNING bit is still '1'. Default Value: 0
11	LINE_COMPL_OUT	Indicates the actual level of the complementary PWM line output signal. Default Value: 0
10	LINE_OUT	Indicates the actual level of the PWM line output signal. Default Value: 0
8	TR_START	Indicates the actual level of the selected start trigger. Default Value: 0
7	TR_STOP	Indicates the actual level of the selected stop trigger. Default Value: 0
6	TR_RELOAD	Indicates the actual level of the selected reload trigger. Default Value: 0

17.1.2 TCPWM0_GRP0_CNT0_STATUS (continued)

5	TR_COUNT	Indicates the actual level of the selected count trigger. Default Value: 1
4	TR_CAPTURE0	Indicates the actual level of the selected capture 0 trigger. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

17.1.3 TCPWM0_GRP0_CNT0_COUNTER

Description: Counter count register

Address: 0x42860008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	COUNTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	COUNTER [31:24]							

Bits	Name	Description
31 : 0	COUNTER	16-bit / 32-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

17.1.4 TCPWM0_GRP0_CNT0_CC0

Description: Counter compare/capture 0 register

Address: 0x42860010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 4294967295

17.1.5 TCPWM0_GRP0_CNT0_CC0_BUFF

Description: Counter buffered compare/capture 0 register

Address: 0x42860014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	Additional buffer for counter CC register. Default Value: 4294967295

17.1.6 TCPWM0_GRP0_CNT0_PERIOD

Description: Counter period register

Address: 0x42860020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 4294967295

17.1.7 TCPWM0_GRP0_CNT0_PERIOD_BUFF

Description: Counter buffered period register

Address: 0x42860024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 0	PERIOD	Additional buffer for counter PERIOD register. In PWM_PR mode PEROD_BUFF defines the LFSR polynomial. Each bit represents a tap of the shift register which can be feed back to the MSB via an XOR tree. Examples for GRP_CNT_WIDTH = 16: - Maximum length 16bit LFSR - polynomial x^16 + x^14 + x^13 + x^11 + 1 - taps 0,2,3,5 -> PERIOD = 0x002d - period is 2^16-1 = 65535 cycles - Maximum length 8bit LFSR: - polynomial x^8 + x^6 + x^5 + x^4 + 1 - taps 8,10,11,12 (realized in 8 MSBs of 16bit LFSR) - period is 2^8-1 = 255 cycles In SR mode PERIOD_BUFF defines which tap of the shift register generates the PWM output signals. For a delay of n cycles (from capture event to PWM output) the bit CNT_WIDTH-n should be set to '1'. For a shift register function only one tap should be use, i.e. a one-hot value must be written to PERIOD_BUFF. If multiple bits in PERIOD_BUFF are set then the taps are XOR combined. Default Value: 4294967295

17.1.8 TCPWM0_GRP0_CNT0_DT

Description: Counter PWM dead time register

Address: 0x42860030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DT_LINE_OUT_L	In PWM_DT mode, this field is used to determine the low byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Note: This field determines the low byte of the 16-bit dead time before activating "line_out" when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by this DT_LINE_OUT_L field is used before activating "line_out" and "line_compl_out". Default Value: 0 **0x0: DIVBY1 :** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2 :** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4 :** Divide by 4 (other-than-PWM_DT mode) **0x3: DIVBY8 :** Divide by 8 (other-than-PWM_DT mode)

17.1.8 TCPWM0_GRP0_CNT0_DT (continued)

0x4: DIVBY16 :

Divide by 16 (other-than-PWM_DT mode)

0x5: DIVBY32 :

Divide by 32 (other-than-PWM_DT mode)

0x6: DIVBY64 :

Divide by 64 (other-than-PWM_DT mode)

0x7: DIVBY128 :

Divide by 128 (other-than-PWM_DT mode)

17.1.9 TCPWM0_GRP0_CNT0_TR_CMD

Description: Counter trigger command register

Address: 0x42860040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1S	RW1S	RW1S	Reserved	RW1S
HW Access	Reserved			RW1C	RW1C	RW1C	Reserved	RW1C
Name	Reserved [7:5]			START	STOP	RELOAD	Reserved	CAPTURE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	START	SW start trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
3	STOP	SW stop trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
2	RELOAD	SW reload trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
0	CAPTURE0	SW capture 0 trigger. When written with '1', a capture 0 trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.ENABLED, the field is immediately set to '0'. Default Value: 0

17.1.10 TCPWM0_GRP0_CNT0_TR_IN_SEL0

Description: Counter input trigger selection register 0

Address: 0x42860044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			CAPTURE0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			COUNT_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [23:21]			RELOAD_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [31:29]			STOP_SEL [28:24]				

Bits	Name	Description
28 : 24	STOP_SEL	Selects one of the 256 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
20 : 16	RELOAD_SEL	Selects one of the 256 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In these modes, it will update the counter with 0x8000 (counter midpoint) or 0x0000 depending on the QUAD_RANGE_MODE. Default Value: 0
12 : 8	COUNT_SEL	Selects one of the 256 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Note: In the modes: TIMER, CAPTURE, PWM, PWM_DT, and SR, If the counter is externally triggered (COUNT_SEL > 1), an external trigger will be required for each TR_CMD to execute. For example, a write to TR_CMD.START will not start the counter until the trigger selected by COUNT_SEL asserts. The next trigger will increment the counter since the counter is now running. This goes for all TR_CMD fields. Default Value: 1

17.1.10 TCPWM0_GRP0_CNT0_TR_IN_SEL0 (continued)

4 : 0	CAPTURE0_SEL	Selects one of the up to 256 input triggers as a capture0 trigger. Input trigger 0 is always '0' and input trigger 1 is always '1'. If existing, the one-to-one trigger inputs "tr_one_cnt_in" (different to each counter) are selected by setting 2 and above. The settings above are used for the general purpose trigger inputs "tr_all_cnt_in" connected to all counters selected. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

17.1.11 TCPWM0_GRP0_CNT0_TR_IN_SEL1

Description: Counter input trigger selection register 1

Address: 0x42860048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			START_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	START_SEL	Selects one of the 256 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0

17.1.12 TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL

Description: Counter input trigger edge selection register

Address: 0x4286004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE0_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3

17.1.12 TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL (continued)

		0x0: RISING_EDGE : Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
1 : 0	CAPTURE0_EDGE	A capture 0 event will copy the counter value into the CC0 register. Default Value: 3

17.1.12 TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL (continued)

0x0: RISING_EDGE :

Rising edge. Any rising edge generates an event.

0x1: FALLING_EDGE :

Falling edge. Any falling edge generates an event.

0x2: ANY_EDGE :

Rising AND falling edge. Any odd amount of edges generates an event.

0x3: NO_EDGE_DET :

No edge detection, use trigger as is.

17.1.13 TCPWM0_GRP0_CNT0_TR_PWM_CTRL

Description: Counter trigger PWM control register

Address: 0x42860050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW		RW		RW	
HW Access	Reserved		R		R		R	
Name	Reserved [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC0_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3

17.1.13 TCPWM0_GRP0_CNT0_TR_PWM_CTRL (continued)

		0x0: SET : Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
1 : 0	CC0_MATCH_MODE	Determines the effect of a compare match 0 event (COUNTER equals CC0 register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC0 register should be set to "0". For a 100% duty cycle, the counter CC0 register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change

17.1.14 TCPWM0_GRP0_CNT0_TR_OUT_SEL

Description: Counter output trigger selection register

Address: 0x42860054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	R			Reserved	R		
Name	Reserved	OUT1 [6:4]			Reserved	OUT0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6 : 4	OUT1	Selects one of the internal events to generate the output trigger 1. Default setting selects the compare match 0 event. Default Value: 3 **0x0: OVERFLOW :** Overflow event **0x1: UNDERFLOW :** Underflow event **0x2: TC :** Terminal count event **0x3: CC0_MATCH :** Compare match 0 event (default selection) **0x4: CC1_MATCH :** Compare match 1 event

17.1.14 TCPWM0_GRP0_CNT0_TR_OUT_SEL (continued)

0x5: LINE_OUT :

PWM output signal "line_out"

0x6: Reserved6 :

This setting is reserved. Do not use.

0x7: Disabled :

Output trigger disabled.

2 : 0	OUT0	Selects one of the internal events to generate the output trigger 0. Default setting selects the terminal count event. Default Value: 2

0x0: OVERFLOW :

Overflow event

0x1: UNDERFLOW :

Underflow event

0x2: TC :

Terminal count event (default selection)

0x3: CC0_MATCH :

Compare match 0 event

0x4: CC1_MATCH :

Compare match 1 event

0x5: LINE_OUT :

PWM output signal "line_out"

0x6: Reserved6 :

This setting is reserved. Do not use.

0x7: Disabled :

Output trigger disabled.

17.1.15 TCPWM0_GRP0_CNT0_INTR

Description: Interrupt request register

Address: 0x42860070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1C	RW1C
HW Access	Reserved						RW1S	RW1S
Name	Reserved [7:2]						CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	CC0_MATCH	Counter matches CC0 register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

17.1.16 TCPWM0_GRP0_CNT0_INTR_SET

Description: Interrupt set request register

Address: 0x42860074

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1S	RW1S
HW Access	Reserved						A	A
Name	Reserved [7:2]						CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	CC0_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

17.1.17 TCPWM0_GRP0_CNT0_INTR_MASK

Description: Interrupt mask register

Address: 0x42860078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	CC0_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

17.1.18 TCPWM0_GRP0_CNT0_INTR_MASKED

Description: Interrupt masked request register

Address: 0x4286007C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	CC0_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

17.1.19 TCPWM0_GRP1_CNT0_CTRL

Description: Counter control register

Address: 0x42868000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	Reserved	RW	RW	RW
HW Access	R	R	R	R	Reserved	R	R	R
Name	CC1_-MATCH_DOWN_EN	CC1_-MATCH_UP_EN	CC0_-MATCH_DOWN_EN	CC0_-MATCH_UP_EN	Reserved	AUTO_RE-LOAD_PE-RIOD	AUTO_RE-LOAD_CC1	AUTO_RE-LOAD_CC0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW		Reserved	RW	RW	RW
HW Access	Reserved		R		Reserved	R	R	R
Name	Reserved [15:14]		PWM_DISABLE_MODE [13:12]		Reserved	PWM_SYN-C_KILL	PW-M_STOP_O N_KILL	PWM_IM-M_KILL

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		Reserved	RW	RW	
HW Access	Reserved		R		Reserved	R	R	
Name	Reserved [23:22]		QUAD_ENCODING_-MODE [21:20]		Reserved	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved			RW		
HW Access	R	R	Reserved			R		
Name	ENABLED	DBG_-FREEZE_EN	Reserved [29:27]			MODE [26:24]		

Bits	Name	Description
31	ENABLED	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_-SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0
30	DBG_FREEZE_EN	Specifies the counter behavior in debug mode. '0': The counter operation continues in debug mode. '1': The counter operation freezes in debug mode. Default Value: 0
26 : 24	MODE	Counter mode. Default Value: 0

17.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

0x0: TIMER :

Timer mode

0x1: Reserved1 :

N/A

0x2: CAPTURE :

Capture mode

0x3: QUAD :

Quadrature mode
Different encoding modes can be selected by QUAD_ENCODING_MODE including up/down count functionality.
Different counter range, reload value and capture behavior can be selected by QUAD_RANGE_-MODE (overloaded field UP_DOWN_MODE).

0x4: PWM :

Pulse width modulation (PWM) mode

0x5: PWM_DT :

PWM with deadtime insertion mode

0x6: PWM_PR :

Pseudo random pulse width modulation

0x7: SR :

Shift register mode.

21 : 20	QUAD_ENCODING_-MODE	In QUAD mode this field selects the quadrature encoding mode (X1/X2/X4) or the Up / Down rotary counting mode. In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUAD_ENCODING_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUAD_ENCODING_MODE[1]. Default Value: 0

0x0: X1 :

X1 encoding (QUAD mode)
This encoding is identical with an up / down counting functionality of the following way: Rising edges of input phiA increment or decrement the counter depending on the state of input phiB (direction input).

0x1: X2 :

X2 encoding (QUAD mode)

0x2: X4 :

X4 encoding (QUAD mode)

17.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

		0x3: UP_DOWN : Up / Down rotary counting mode. Input phiA increments the counter, input phiB decrements the counter. The trigger edge detection settings apply. **0x1: INV_OUT :** When bit 0 is '1', QUADRATURE_ENCODING_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: INV_COMPL_OUT :** When bit 1 is '1', QUADRATURE_ENCODING_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. In QUAD mode this field acts as QUAD_RANGE_MODE field selecting between different counter range, reload value and compare / capture behavior. Default Value: 0 **0x0: COUNT_UP :** Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD. **0x1: COUNT_DOWN :** Count down (to "0"). An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0". **0x2: COUNT_UPDN1 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0". **0x3: COUNT_UPDN2 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0" AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).

17.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

0x0: QUAD_RANGE0 :

In QUAD mode this setting selects the QUAD_RANGE0 mode with the following behavior:
- COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32)
- on reload / index event:
 - CC0 is copied to CC0_BUFF
 - COUNTER is copied to CC0
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - tc and cc0_match events are generated
- when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF:
 - CC0 is copied to CC0_BUFF
 - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to CC0
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - cc0_match event is generated

0x1: QUAD_RANGE0_CMP :

In QUAD mode this setting selects the QUAD_RANGE0_CMP mode with the following behavior:
- COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32)
- the capture0 event acts as 2nd reload / index event
- on reload / index event:
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - when 'capture on index' is selected (AUTO_RELOAD_PERIOD=0):
 - tc event is generated
 - PERIOD is copied to PERIOD_BUFF
 - COUNTER is copied to PERIOD
- when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF:
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - when 'capture on wrap-around' is selected (AUTO_RELOAD_PERIOD=1):
 - tc event is generated
 - PERIOD is copied to PERIOD_BUFF
 - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to PERIOD
- 1 or 2 compare functions (depending on CC1_PRESENT) available

This mode is to a certain extend backward compatible with previous TCPWM quadrature behavior but allows a compare function during quadrature decoding using the CC0/CC_BUFF registers and the cc0_match event. Because of that the PERIOD/PERIOD_BUFF registers are used instead of CC0/CC_BUFF registers to capture COUNTER at reload / index event or wrap-around.

17.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

0x2: QUAD_RANGE1_CAPT :

In QUAD mode this setting selects the QUAD_RANGE1_CAPT mode with the following behavior:
- COUNTER range is between 0x0000 and PERIOD
- on reload / index event:
 - COUNTER is set to 0x0000
 - tc event is generated
- when COUNTER is 0x0000 and decrementing:
 - COUNTER is set to PERIOD
 - tc event is generated
- when COUNTER equals PERIOD and is incrementing:
 - COUNTER is set to 0x0000
 - tc event is generated
- 1 or 2 capture functions (depending on CC1_PRESENT) available
- on capture0 / capture1 event:
 - CC0 / CC1 is copied to CC0_BUFF / CC1_BUFF
 - COUNTER value is copied to CC0

It allows that the COUNTER register reflects the current angle position of the rotary encoder, i.e. no MOD or SUB calculations need to be done in SW on the COUNTER value to get the current angle position. This allows a DMA copy of the angle position from the COUNTER register. However, a disadvantage of this mode is that fast sequences of tc interrupts can occur (when encoder moves back and forth around start position). It is recommended to not use the tc interrupt in this mode.

0x3: QUAD_RANGE1_CMP :

In QUAD mode this setting selects the QUAD_RANGE1_CMP mode.
The behavior is the same as for QUAD_RANGE1_CAPT mode described above with the only difference that 1 or 2 compare functions (depending on CC1_PRESENT) are available instead of 1 or 2 capture functions.

13 : 12 PWM_DISABLE_MODE

Specifies the behavior of the PWM outputs "line_out" and "line_compl_out" while the TCPWM counter is disabled (CTL.ENABLED='0') or stopped.
Note: The output signal of this selection can be further modified by the immediate kill logic and line_out polarity settings (CTRL.QUAD_ENCODING_MODE).
Default Value: 0

0x0: Z :

When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are NOT driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance).
Note: This is realized by driving the TCPWM output "line_out_en" to 0.
When the counter is stopped upon a stop event the PWM outputs are deactivated (to the polarity defined by CTL.QUAD_ENCODING_MODE).

0x1: RETAIN :

When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM.
When the counter is disabled or stopped upon a stop event the PWM outputs are retained (keep their previous levels).
While the counter is disabled or stopped the PWM outputs can be changed via LINE_SEL (when parameter GRP_SMC_PRESENT = 1).

0x2: L :

When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM.
When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '0' and the PWM output "line_compl_out" is driven as a fixed '1'.

17.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

		0x3: H : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '1' and the PWM output "line_compl_out" is driven as a fixed '0'.
10	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
9	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
8	PWM_IMM_KILL	Specifies whether the kill event immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals or with the next module clock ("active count" pre-scaled "clk_counter"). '0': synchronous kill activation. Deactivates the "dt_line_out" and "dt_line_compl_out" signals with the next module clock ("active count" pre-scaled "clk_counter"). '1': immediate kill activation. Immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
7	CC1_MATCH_DOWN_EN	Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 1 event generation disabled when counting down '1': compare match 1 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. Default Value: 1
6	CC1_MATCH_UP_EN	Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 1 event generation disabled when counting up '1': compare match 1 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. Default Value: 1
5	CC0_MATCH_DOWN_EN	Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting down '1': compare match 0 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. Default Value: 1
4	CC0_MATCH_UP_EN	Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting up '1': compare match 0 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. Default Value: 1

17.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

2	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff. Default Value: 0
1	AUTO_RELOAD_CC1	Specifies switching of the CC1 and buffered CC1 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 1 event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0
0	AUTO_RELOAD_CC0	Specifies switching of the CC0 and buffered CC0 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 0 event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

17.1.20 TCPWM0_GRP1_CNT0_STATUS

Description: Counter status register

Address: 0x42868004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	Reserved			R
HW Access	RW	RW	RW	RW	Reserved			RW
Name	TR_STOP	TR_RE-LOAD	TR_COUNT	TR_CAP-TURE0	Reserved [3:1]			DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R	Reserved			R	R	R	R
HW Access	RW	Reserved			RW	RW	RW	RW
Name	RUNNING	Reserved [14:12]			LINE_COM-PL_OUT	LINE_OUT	TR_CAP-TURE1	TR_START

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DT_CNT_L [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DT_CNT_H [31:24]							

Bits	Name	Description
31 : 24	DT_CNT_H	High byte of 16-bit dead time counter. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8bit wide and the only the field DT_CNT_L is used as dead time counter. Default Value: 0
23 : 16	DT_CNT_L	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion (8bit dead time counter or low byte of 16-bit dead time counter). In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
15	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. This field is used to indicate that the counter is running after a start/reload event and that the counter is stopped after a stop event. When a running counter operation is paused in debug state (see CTRL.DBG_PAUSE) then the RUNNING bit is still '1'. Default Value: 0
11	LINE_COMPL_OUT	Indicates the actual level of the complementary PWM line output signal. Default Value: 0
10	LINE_OUT	Indicates the actual level of the PWM line output signal. Default Value: 0

17.1.20 TCPWM0_GRP1_CNT0_STATUS (continued)

9	TR_CAPTURE1	Indicates the actual level of the selected capture 1 trigger. Default Value: 0
8	TR_START	Indicates the actual level of the selected start trigger. Default Value: 0
7	TR_STOP	Indicates the actual level of the selected stop trigger. Default Value: 0
6	TR_RELOAD	Indicates the actual level of the selected reload trigger. Default Value: 0
5	TR_COUNT	Indicates the actual level of the selected count trigger. Default Value: 1
4	TR_CAPTURE0	Indicates the actual level of the selected capture 0 trigger. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

17.1.21 TCPWM0_GRP1_CNT0_COUNTER

Description: Counter count register

Address: 0x42868008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit / 32-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

17.1.22 TCPWM0_GRP1_CNT0_CC0

Description: Counter compare/capture 0 register

Address: 0x42868010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

17.1.23 TCPWM0_GRP1_CNT0_CC0_BUFF

Description: Counter buffered compare/capture 0 register

Address: 0x42868014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

17.1.24 TCPWM0_GRP1_CNT0_CC1

Description: Counter compare/capture 1 register

Address: 0x42868018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

17.1.25 TCPWM0_GRP1_CNT0_CC1_BUFF

Description: Counter buffered compare/capture 1 register

Address: 0x4286801C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC1 register. Default Value: 65535

17.1.26 TCPWM0_GRP1_CNT0_PERIOD

Description: Counter period register

Address: 0x42868020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

17.1.27 TCPWM0_GRP1_CNT0_PERIOD_BUFF

Description: Counter buffered period register

Address: 0x42868024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. In PWM_PR mode PEROD_BUFF defines the LFSR polynomial. Each bit represents a tap of the shift register which can be feed back to the MSB via an XOR tree. Examples for GRP_CNT_WIDTH = 16: - Maximum length 16bit LFSR - polynomial x^16 + x^14 + x^13 + x^11 + 1 - taps 0,2,3,5 -> PERIOD = 0x002d - period is 2^16-1 = 65535 cycles - Maximum length 8bit LFSR: - polynomial x^8 + x^6 + x^5 + x^4 + 1 - taps 8,10,11,12 (realized in 8 MSBs of 16bit LFSR) - period is 2^8-1 = 255 cycles In SR mode PERIOD_BUFF defines which tap of the shift register generates the PWM output signals. For a delay of n cycles (from capture event to PWM output) the bit CNT_WIDTH-n should be set to '1'. For a shift register function only one tap should be use, i.e. a one-hot value must be written to PERIOD_BUFF. If multiple bits in PERIOD_BUFF are set then the taps are XOR combined. Default Value: 65535

17.1.28 TCPWM0_GRP1_CNT0_DT

Description: Counter PWM dead time register

Address: 0x42868030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DT_LINE_COMPL_OUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DT_LINE_COMPL_OUT [31:24]							

Bits	Name	Description
31 : 16	DT_LINE_COMPL_OUT	In PWM_DT mode, this field is used to determine the dead time before activating the complementary PWM line output signal "line_compl_out": amount of dead time cycles in the counter clock domain. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating "line_out" and "line_compl_out". Default Value: 0
15 : 8	DT_LINE_OUT_H	In PWM_DT mode, this field is used to determine the high byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating "line_out" and "line_compl_out". Default Value: 0
7 : 0	DT_LINE_OUT_L	In PWM_DT mode, this field is used to determine the low byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Note: This field determines the low byte of the 16-bit dead time before activating "line_out" when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by this DT_LINE_OUT_L field is used before activating "line_out" and "line_compl_out". Default Value: 0

17.1.28 TCPWM0_GRP1_CNT0_DT (continued)

0x0: DIVBY1 :

Divide by 1 (other-than-PWM_DT mode)

0x1: DIVBY2 :

Divide by 2 (other-than-PWM_DT mode)

0x2: DIVBY4 :

Divide by 4 (other-than-PWM_DT mode)

0x3: DIVBY8 :

Divide by 8 (other-than-PWM_DT mode)

0x4: DIVBY16 :

Divide by 16 (other-than-PWM_DT mode)

0x5: DIVBY32 :

Divide by 32 (other-than-PWM_DT mode)

0x6: DIVBY64 :

Divide by 64 (other-than-PWM_DT mode)

0x7: DIVBY128 :

Divide by 128 (other-than-PWM_DT mode)

17.1.29 TCPWM0_GRP1_CNT0_TR_CMD

Description: Counter trigger command register

Address: 0x42868040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW1S	RW1S	RW1S	RW1S	Reserved	RW1S
HW Access	Reserved		RW1C	RW1C	RW1C	RW1C	Reserved	RW1C
Name	Reserved [7:6]		CAPTURE1	START	STOP	RELOAD	Reserved	CAPTURE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	CAPTURE1	SW capture 1 trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
4	START	SW start trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
3	STOP	SW stop trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
2	RELOAD	SW reload trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
0	CAPTURE0	SW capture 0 trigger. When written with '1', a capture 0 trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.ENABLED, the field is immediately set to '0'. Default Value: 0

17.1.30 TCPWM0_GRP1_CNT0_TR_IN_SEL1

Description: Counter input trigger selection register 1

Address: 0x42868048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			START_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			CAPTURE1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12 : 8	CAPTURE1_SEL	Selects one of the 256 input triggers as a capture 1 trigger. Default Value: 0
4 : 0	START_SEL	Selects one of the 256 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0

17.1.31 TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL

Description: Counter input trigger edge selection register

Address: 0x4286804C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE0_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW		RW	
HW Access	Reserved				R		R	
Name	Reserved [15:12]				CAPTURE1_EDGE [11:10]		START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11 : 10	CAPTURE1_EDGE	A capture 1 event will copy the counter value into the CC1 register. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event.

17.1.31 TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL (continued)

		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event.

17.1.31 TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL (continued)

		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
1 : 0	CAPTURE0_EDGE	A capture 0 event will copy the counter value into the CC0 register. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.

17.1.32 TCPWM0_GRP1_CNT0_TR_PWM_CTRL

Description: Counter trigger PWM control register

Address: 0x42868050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CC1_MATCH_MODE [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC0_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 6	CC1_MATCH_MODE	Determines the effect of a compare match 1 event (COUNTER equals CC1 register) on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3

17.1.32 TCPWM0_GRP1_CNT0_TR_PWM_CTRL (continued)

		0x0: SET : Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
1 : 0	CC0_MATCH_MODE	Determines the effect of a compare match 0 event (COUNTER equals CC0 register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC0 register should be set to "0". For a 100% duty cycle, the counter CC0 register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change

17.1.33 TCPWM0_GRP1_CNT0_INTR

Description: Interrupt request register

Address: 0x42868070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1C	RW1C	RW1C
HW Access	Reserved					RW1S	RW1S	RW1S
Name	Reserved [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	CC1_MATCH	Counter matches CC1 register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
1	CC0_MATCH	Counter matches CC0 register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

17.1.34 TCPWM0_GRP1_CNT0_INTR_SET

Description: Interrupt set request register

Address: 0x42868074

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1S	RW1S	RW1S
HW Access	Reserved					A	A	A
Name	Reserved [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	CC1_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	CC0_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

17.1.35 TCPWM0_GRP1_CNT0_INTR_MASK

Description: Interrupt mask register

Address: 0x42868078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	CC1_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	CC0_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

17.1.36 TCPWM0_GRP1_CNT0_INTR_MASKED

Description: Interrupt masked request register

Address: 0x4286807C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R	R	R
HW Access	Reserved					W	W	W
Name	Reserved [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	CC1_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
1	CC0_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

18 Serial Communication Block (SCB) registers

This section discusses the SCB registers. It lists all the registers in mapping tables, in address order.

18.1 Register details

Register name	Address	Description
SCB0_CTRL	0x42990000	Generic control
SCB0_STATUS	0x42990004	Generic status
SCB0_CMD_RESP_CTRL	0x42990008	Command/response control
SCB0_CMD_RESP_STATUS	0x4299000C	Command/response status
SCB0_SPI_CTRL	0x42990020	SPI control
SCB0_SPI_STATUS	0x42990024	SPI status
SCB0_SPI_TX_CTRL	0x42990028	SPI transmitter control
SCB0_SPI_RX_CTRL	0x4299002C	SPI receiver control
SCB0_I2C_CTRL	0x42990060	I2C control
SCB0_I2C_STATUS	0x42990064	I2C status
SCB0_I2C_M_CMD	0x42990068	I2C master command
SCB0_I2C_S_CMD	0x4299006C	I2C slave command
SCB0_I2C_CFG	0x42990070	I2C configuration
SCB0_I2C_STRETCH_CTRL	0x42990074	I2C stretch control
SCB0_I2C_STRETCH_STATUS	0x42990078	I2C stretch status
SCB0_TX_CTRL	0x42990200	Transmitter control
SCB0_TX_FIFO_CTRL	0x42990204	Transmitter FIFO control
SCB0_TX_FIFO_STATUS	0x42990208	Transmitter FIFO status
SCB0_TX_FIFO_WR	0x42990240	Transmitter FIFO write
SCB0_RX_CTRL	0x42990300	Receiver control
SCB0_RX_FIFO_CTRL	0x42990304	Receiver FIFO control
SCB0_RX_FIFO_STATUS	0x42990308	Receiver FIFO status
SCB0_RX_MATCH	0x42990310	Slave address and mask
SCB0_RX_FIFO_RD	0x42990340	Receiver FIFO read
SCB0_RX_FIFO_RD_SILENT	0x42990344	Receiver FIFO read silent
SCB0_EZ_DATA0	0x42990400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB0_EZ_DATA0 to SCB0_EZ_DATA255).
SCB0_INTR_CAUSE	0x42990E00	Active clocked interrupt signal
SCB0_INTR_I2C_EC	0x42990E80	Externally clocked I2C interrupt request
SCB0_INTR_I2C_EC_MASK	0x42990E88	Externally clocked I2C interrupt mask
SCB0_INTR_I2C_EC_MASKED	0x42990E8C	Externally clocked I2C interrupt masked
SCB0_INTR_SPI_EC	0x42990EC0	Externally clocked SPI interrupt request
SCB0_INTR_SPI_EC_MASK	0x42990EC8	Externally clocked SPI interrupt mask

Register name	Address	Description
SCB0_INTR_I2C_EC_MASKED	0x42990ECC	Externally clocked SPI interrupt masked
SCB0_INTR_M	0x42990F00	Master interrupt request
SCB0_INTR_M_SET	0x42990F04	Master interrupt set request
SCB0_INTR_M_MASK	0x42990F08	Master interrupt mask
SCB0_INTR_M_MASKED	0x42990F0C	Master interrupt masked request
SCB0_INTR_S	0x42990F40	Slave interrupt request
SCB0_INTR_S_SET	0x42990F44	Slave interrupt set request
SCB0_INTR_S_MASK	0x42990F48	Slave interrupt mask
SCB0_INTR_S_MASKED	0x42990F4C	Slave interrupt masked request
SCB0_INTR_TX	0x42990F80	Transmitter interrupt request
SCB0_INTR_TX_SET	0x42990F84	Transmitter interrupt set request
SCB0_INTR_TX_MASK	0x42990F88	Transmitter interrupt mask
SCB0_INTR_TX_MASKED	0x42990F8C	Transmitter interrupt masked request
SCB0_INTR_RX	0x42990FC0	Receiver interrupt request
SCB0_INTR_RX_SET	0x42990FC4	Receiver interrupt set request
SCB0_INTR_RX_MASK	0x42990FC8	Receiver interrupt mask
SCB0_INTR_RX_MASKED	0x42990FCC	Receiver interrupt masked request
SCB2_CTRL	0x429A0000	Generic control
SCB2_SPI_CTRL	0x429A0020	SPI control
SCB2_SPI_STATUS	0x429A0024	SPI status
SCB2_SPI_TX_CTRL	0x429A0028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB2_SPI_RX_CTRL	0x429A002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB2_UART_CTRL	0x429A0040	UART control
SCB2_UART_TX_CTRL	0x429A0044	UART transmitter control
SCB2_UART_RX_CTRL	0x429A0048	UART receiver control
SCB2_UART_RX_STATUS	0x429A004C	UART receiver status
SCB2_UART_FLOW_CTRL	0x429A0050	UART flow control
SCB2_I2C_CTRL	0x429A0060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB2_I2C_STATUS	0x429A0064	I2C status
SCB2_I2C_M_CMD	0x429A0068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB2_I2C_S_CMD	0x429A006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB2_I2C_CFG	0x429A0070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB2_I2C_STRETCH_CTRL	0x429A0074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.

Serial Communication Block (SCB) registers

Register name	Address	Description
SCB2_I2C_STRETCH_STATUS	0x429A0078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB2_TX_CTRL	0x429A0200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB2_TX_FIFO_CTRL	0x429A0204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB2_TX_FIFO_STATUS	0x429A0208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB2_TX_FIFO_WR	0x429A0240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB2_RX_CTRL	0x429A0300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB2_RX_FIFO_CTRL	0x429A0304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB2_RX_FIFO_STATUS	0x429A0308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB2_RX_MATCH	0x429A0310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB2_RX_FIFO_RD	0x429A0340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB2_RX_FIFO_RD_SILENT	0x429A0344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB2_EZ_DATA0	0x429A0400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB2_EZ_DATA0 to SCB2_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_INTR_CAUSE	0x429A0E00	Active clocked interrupt signal
SCB2_INTR_M	0x429A0F00	Master interrupt request
SCB2_INTR_M_SET	0x429A0F04	Master interrupt set request
SCB2_INTR_M_MASK	0x429A0F08	Master interrupt mask
SCB2_INTR_M_MASKED	0x429A0F0C	Master interrupt masked request
SCB2_INTR_S	0x429A0F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB2_INTR_S_SET	0x429A0F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB2_INTR_S_MASK	0x429A0F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB2_INTR_S_MASKED	0x429A0F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB2_INTR_TX	0x429A0F80	Transmitter interrupt request
SCB2_INTR_TX_SET	0x429A0F84	Transmitter interrupt set request
SCB2_INTR_TX_MASK	0x429A0F88	Transmitter interrupt mask

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Register name	Address	Description
SCB2_INTR_TX_SET	0x429A0F8C	Transmitter interrupt masked request
SCB2_INTR_RX	0x429A0FC0	Receiver interrupt request
SCB2_INTR_RX_SET	0x429A0FC4	Receiver interrupt set request
SCB2_INTR_RX_MASK	0x429A0FC8	Receiver interrupt mask
SCB2_INTR_RX_MASKED	0x429A0FCC	Receiver interrupt masked request
SCB3_CTRL	0x429B0000	Generic control. See SCB2_CTRL for the details of bit fields.
SCB3_SPI_CTRL	0x429B0020	SPI control. See SCB2_SPI_CTRL for the details of bit fields.
SCB3_SPI_STATUS	0x429B0024	SPI status. See SCB2_SPI_STATUS for the details of bit fields.
SCB3_SPI_TX_CTRL	0x429B0028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB3_SPI_RX_CTRL	0x429B002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB3_UART_CTRL	0x429B0040	UART control. See SCB2_UART_CTRL for the details of bit fields.
SCB3_UART_TX_CTRL	0x429B0044	UART transmitter control. See SCB2_UART_TX_CTRL for the details of bit fields.
SCB3_UART_RX_CTRL	0x429B0048	UART receiver control. See SCB2_UART_RX_CTRL for the details of bit fields.
SCB3_UART_RX_STATUS	0x429B004C	UART receiver status. See SCB2_UART_RX_STATUS for the details of bit fields.
SCB3_UART_FLOW_CTRL	0x429B0050	UART flow control. See SCB2_UART_FLOW_CTRL for the details of bit fields.
SCB3_I2C_CTRL	0x429B0060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB3_I2C_STATUS	0x429B0064	I2C status. See SCB2_I2C_STATUS for the details of bit fields.
SCB3_I2C_M_CMD	0x429B0068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB3_I2C_S_CMD	0x429B006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB3_I2C_CFG	0x429B0070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB3_I2C_STRETCH_CTRL	0x429B0074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB3_I2C_STRETCH_STATUS	0x429B0078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB3_TX_CTRL	0x429B0200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB3_TX_FIFO_CTRL	0x429B0204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB3_TX_FIFO_STATUS	0x429B0208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.

Register name	Address	Description
SCB3_TX_FIFO_WR	0x429B0240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB3_RX_CTRL	0x429B0300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB3_RX_FIFO_CTRL	0x429B0304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB3_RX_FIFO_STATUS	0x429B0308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB3_RX_MATCH	0x429B0310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB3_RX_FIFO_RD	0x429B0340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB3_RX_FIFO_RD_SILENT	0x429B0344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB3_EZ_DATA0	0x429B0400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB3_EZ_DATA0 to SCB3_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_INTR_CAUSE	0x429B0E00	Active clocked interrupt signal. See SCB2_INTR_CAUSE for the details of bit fields.
SCB3_INTR_M	0x429B0F00	Master interrupt request. See SCB2_INTR_M for the details of bit fields.
SCB3_INTR_M_SET	0x429B0F04	Master interrupt set request. See SCB2_INTR_M_SET for the details of bit fields.
SCB3_INTR_M_MASK	0x429B0F08	Master interrupt mask. See SCB2_INTR_M_MASK for the details of bit fields.
SCB3_INTR_M_MASKED	0x429B0F0C	Master interrupt masked request. See SCB2_INTR_M_MASKED for the details of bit fields.
SCB3_INTR_S	0x429B0F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB3_INTR_S_SET	0x429B0F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB3_INTR_S_MASK	0x429B0F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB3_INTR_S_MASKED	0x429B0F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB3_INTR_TX	0x429B0F80	Transmitter interrupt request. See SCB2_INTR_TX for the details of bit fields.
SCB3_INTR_TX_SET	0x429B0F84	Transmitter interrupt set request. See SCB2_INTR_TX_SET for the details of bit fields.
SCB3_INTR_TX_MASK	0x429B0F88	Transmitter interrupt mask. See SCB2_INTR_TX_MASK for the details of bit fields.

Register name	Address	Description
SCB3_INTR_TX_MASKED	0x429B0F8C	Transmitter interrupt masked request. See SCB2_INTR_TX_MASKED for the details of bit fields.
SCB3_INTR_RX	0x429B0FC0	Receiver interrupt request. See SCB2_INTR_RX for the details of bit fields.
SCB3_INTR_RX_SET	0x429B0FC4	Receiver interrupt set request. See SCB2_INTR_RX_SET for the details of bit fields.
SCB3_INTR_RX_MASK	0x429B0FC8	Receiver interrupt mask. See SCB2_INTR_RX_MASK for the details of bit fields.
SCB3_INTR_RX_MASKED	0x429B0FCC	Receiver interrupt masked request. See SCB2_INTR_RX_MASKED for the details of bit fields.
SCB4_CTRL	0x429C0000	Generic control. See SCB2_CTRL for the details of bit fields.
SCB4_SPI_CTRL	0x429C0020	SPI control. See SCB2_SPI_CTRL for the details of bit fields.
SCB4_SPI_STATUS	0x429C0024	SPI status. See SCB2_SPI_STATUS for the details of bit fields.
SCB4_SPI_TX_CTRL	0x429C0028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB4_SPI_RX_CTRL	0x429C002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB4_UART_CTRL	0x429C0040	UART control. See SCB2_UART_CTRL for the details of bit fields.
SCB4_UART_TX_CTRL	0x429C0044	UART transmitter control. See SCB2_UART_TX_CTRL for the details of bit fields.
SCB4_UART_RX_CTRL	0x429C0048	UART receiver control. See SCB2_UART_RX_CTRL for the details of bit fields.
SCB4_UART_RX_STATUS	0x429C004C	UART receiver status. See SCB2_UART_RX_STATUS for the details of bit fields.
SCB4_UART_FLOW_CTRL	0x429C0050	UART flow control. See SCB2_UART_FLOW_CTRL for the details of bit fields.
SCB4_I2C_CTRL	0x429C0060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB4_I2C_STATUS	0x429C0064	I2C status. See SCB2_I2C_STATUS for the details of bit fields.
SCB4_I2C_M_CMD	0x429C0068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB4_I2C_S_CMD	0x429C006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB4_I2C_CFG	0x429C0070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB4_I2C_STRETCH_CTRL	0x429C0074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB4_I2C_STRETCH_STATUS	0x429C0078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB4_TX_CTRL	0x429C0200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.

Register name	Address	Description
SCB4_TX_FIFO_CTRL	0x429C0204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB4_TX_FIFO_STATUS	0x429C0208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB4_TX_FIFO_WR	0x429C0240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB4_RX_CTRL	0x429C0300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB4_RX_FIFO_CTRL	0x429C0304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB4_RX_FIFO_STATUS	0x429C0308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB4_RX_MATCH	0x429C0310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB4_RX_FIFO_RD	0x429C0340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB4_RX_FIFO_RD_SILENT	0x429C0344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB4_EZ_DATA0	0x429C0400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB4_EZ_DATA0 to SCB4_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_INTR_CAUSE	0x429C0E00	Active clocked interrupt signal. See SCB2_INTR_CAUSE for the details of bit fields.
SCB4_INTR_M	0x429C0F00	Master interrupt request. See SCB2_INTR_M for the details of bit fields.
SCB4_INTR_M_SET	0x429C0F04	Master interrupt set request. See SCB2_INTR_M_SET for the details of bit fields.
SCB4_INTR_M_MASK	0x429C0F08	Master interrupt mask. See SCB2_INTR_M_MASK for the details of bit fields.
SCB4_INTR_M_MASKED	0x429C0F0C	Master interrupt masked request. See SCB2_INTR_M_MASKED for the details of bit fields.
SCB4_INTR_S	0x429C0F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB4_INTR_S_SET	0x429C0F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB4_INTR_S_MASK	0x429C0F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB4_INTR_S_MASKED	0x429C0F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB4_INTR_TX	0x429C0F80	Transmitter interrupt request. See SCB2_INTR_TX for the details of bit fields.

Register name	Address	Description
SCB4_INTR_TX_SET	0x429C0F84	Transmitter interrupt set request. See SCB2_INTR_TX_SET for the details of bit fields.
SCB4_INTR_TX_MASK	0x429C0F88	Transmitter interrupt mask. See SCB2_INTR_TX_MASK for the details of bit fields.
SCB4_INTR_TX_MASKED	0x429C0F8C	Transmitter interrupt masked request. See SCB2_INTR_TX_MASKED for the details of bit fields.
SCB4_INTR_RX	0x429C0FC0	Receiver interrupt request. See SCB2_INTR_RX for the details of bit fields.
SCB4_INTR_RX_SET	0x429C0FC4	Receiver interrupt set request. See SCB2_INTR_RX_SET for the details of bit fields.
SCB4_INTR_RX_MASK	0x429C0FC8	Receiver interrupt mask. See SCB2_INTR_RX_MASK for the details of bit fields.
SCB4_INTR_RX_MASKED	0x429C0FCC	Receiver interrupt masked request. See SCB2_INTR_RX_MASKED for the details of bit fields.
SCB5_CTRL	0x429D0000	Generic control. See SCB2_CTRL for the details of bit fields.
SCB5_SPI_CTRL	0x429D0020	SPI control. See SCB2_SPI_CTRL for the details of bit fields.
SCB5_SPI_STATUS	0x429D0024	SPI status. See SCB2_SPI_STATUS for the details of bit fields.
SCB5_SPI_TX_CTRL	0x429D0028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB5_SPI_RX_CTRL	0x429D002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB5_UART_CTRL	0x429D0040	UART control. See SCB2_UART_CTRL for the details of bit fields.
SCB5_UART_TX_CTRL	0x429D0044	UART transmitter control. See SCB2_UART_TX_CTRL for the details of bit fields.
SCB5_UART_RX_CTRL	0x429D0048	UART receiver control. See SCB2_UART_RX_CTRL for the details of bit fields.
SCB5_UART_RX_STATUS	0x429D004C	UART receiver status. See SCB2_UART_RX_STATUS for the details of bit fields.
SCB5_UART_FLOW_CTRL	0x429D0050	UART flow control. See SCB2_UART_FLOW_CTRL for the details of bit fields.
SCB5_I2C_CTRL	0x429D0060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB5_I2C_STATUS	0x429D0064	I2C status. See SCB2_I2C_STATUS for the details of bit fields.
SCB5_I2C_M_CMD	0x429D0068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB5_I2C_S_CMD	0x429D006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB5_I2C_CFG	0x429D0070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB5_I2C_STRETCH_CTRL	0x429D0074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.

Register name	Address	Description
SCB5_I2C_STRETCH_STATUS	0x429D0078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB5_TX_CTRL	0x429D0200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB5_TX_FIFO_CTRL	0x429D0204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB5_TX_FIFO_STATUS	0x429D0208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB5_TX_FIFO_WR	0x429D0240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB5_RX_CTRL	0x429D0300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB5_RX_FIFO_CTRL	0x429D0304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB5_RX_FIFO_STATUS	0x429D0308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB5_RX_MATCH	0x429D0310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB5_RX_FIFO_RD	0x429D0340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB5_RX_FIFO_RD_SILENT	0x429D0344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB5_EZ_DATA0	0x429D0400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB5_EZ_DATA0 to SCB5_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB5_INTR_CAUSE	0x429D0E00	Active clocked interrupt signal. See SCB2_INTR_CAUSE for the details of bit fields.
SCB5_INTR_M	0x429D0F00	Master interrupt request. See SCB2_INTR_M for the details of bit fields.
SCB5_INTR_M_SET	0x429D0F04	Master interrupt set request. See SCB2_INTR_M_SET for the details of bit fields.
SCB5_INTR_M_MASK	0x429D0F08	Master interrupt mask. See SCB2_INTR_M_MASK for the details of bit fields.
SCB5_INTR_M_MASKED	0x429D0F0C	Master interrupt masked request. See SCB2_INTR_M_MASKED for the details of bit fields.
SCB5_INTR_S	0x429D0F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB5_INTR_S_SET	0x429D0F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB5_INTR_S_MASK	0x429D0F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.

Register name	Address	Description
SCB5_INTR_S_MASKED	0x429D0F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB5_INTR_TX	0x429D0F80	Transmitter interrupt request. See SCB2_INTR_TX for the details of bit fields.
SCB5_INTR_TX_SET	0x429D0F84	Transmitter interrupt set request. See SCB2_INTR_TX_SET for the details of bit fields.
SCB5_INTR_TX_MASK	0x429D0F88	Transmitter interrupt mask. See SCB2_INTR_TX_MASK for the details of bit fields.
SCB5_INTR_TX_MASKED	0x429D0F8C	Transmitter interrupt masked request. See SCB2_INTR_TX_MASKED for the details of bit fields.
SCB5_INTR_RX	0x429D0FC0	Receiver interrupt request. See SCB2_INTR_RX for the details of bit fields.
SCB5_INTR_RX_SET	0x429D0FC4	Receiver interrupt set request. See SCB2_INTR_RX_SET for the details of bit fields.
SCB5_INTR_RX_MASK	0x429D0FC8	Receiver interrupt mask. See SCB2_INTR_RX_MASK for the details of bit fields.
SCB5_INTR_RX_MASKED	0x429D0FCC	Receiver interrupt masked request. See SCB2_INTR_RX_MASKED for the details of bit fields.
SCB6_CTRL	0x429E0000	Generic control. See SCB2_CTRL for the details of bit fields.
SCB6_SPI_CTRL	0x429E0020	SPI control. See SCB2_SPI_CTRL for the details of bit fields.
SCB6_SPI_STATUS	0x429E0024	SPI status. See SCB2_SPI_STATUS for the details of bit fields.
SCB6_SPI_TX_CTRL	0x429E0028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB6_SPI_RX_CTRL	0x429E002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB6_UART_CTRL	0x429E0040	UART control. See SCB2_UART_CTRL for the details of bit fields.
SCB6_UART_TX_CTRL	0x429E0044	UART transmitter control. See SCB2_UART_TX_CTRL for the details of bit fields.
SCB6_UART_RX_CTRL	0x429E0048	UART receiver control. See SCB2_UART_RX_CTRL for the details of bit fields.
SCB6_UART_RX_STATUS	0x429E004C	UART receiver status. See SCB2_UART_RX_STATUS for the details of bit fields.
SCB6_UART_FLOW_CTRL	0x429E0050	UART flow control. See SCB2_UART_FLOW_CTRL for the details of bit fields.
SCB6_I2C_CTRL	0x429E0060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB6_I2C_STATUS	0x429E0064	I2C status. See SCB2_I2C_STATUS for the details of bit fields.
SCB6_I2C_M_CMD	0x429E0068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB6_I2C_S_CMD	0x429E006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.

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Register name	Address	Description
SCB6_I2C_CFG	0x429E0070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB6_I2C_STRETCH_CTRL	0x429E0074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB6_I2C_STRETCH_STATUS	0x429E0078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB6_TX_CTRL	0x429E0200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB6_TX_FIFO_CTRL	0x429E0204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB6_TX_FIFO_STATUS	0x429E0208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB6_TX_FIFO_WR	0x429E0240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB6_RX_CTRL	0x429E0300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB6_RX_FIFO_CTRL	0x429E0304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB6_RX_FIFO_STATUS	0x429E0308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB6_RX_MATCH	0x429E0310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB6_RX_FIFO_RD	0x429E0340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB6_RX_FIFO_RD_SILENT	0x429E0344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB6_EZ_DATA0	0x429E0400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB6_EZ_DATA0 to SCB6_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB6_INTR_CAUSE	0x429E0E00	Active clocked interrupt signal. See SCB2_INTR_CAUSE for the details of bit fields.
SCB6_INTR_M	0x429E0F00	Master interrupt request. See SCB2_INTR_M for the details of bit fields.
SCB6_INTR_M_SET	0x429E0F04	Master interrupt set request. See SCB2_INTR_M_SET for the details of bit fields.
SCB6_INTR_M_MASK	0x429E0F08	Master interrupt mask. See SCB2_INTR_M_MASK for the details of bit fields.
SCB6_INTR_M_MASKED	0x429E0F0C	Master interrupt masked request. See SCB2_INTR_M_MASKED for the details of bit fields.
SCB6_INTR_S	0x429E0F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.

Serial Communication Block (SCB) registers

Register name	Address	Description
SCB6_INTR_S_SET	0x429E0F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB6_INTR_S_MASK	0x429E0F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB6_INTR_S_MASKED	0x429E0F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB6_INTR_TX	0x429E0F80	Transmitter interrupt request. See SCB2_INTR_TX for the details of bit fields.
SCB6_INTR_TX_SET	0x429E0F84	Transmitter interrupt set request. See SCB2_INTR_TX_SET for the details of bit fields.
SCB6_INTR_TX_MASK	0x429E0F88	Transmitter interrupt mask. See SCB2_INTR_TX_MASK for the details of bit fields.
SCB6_INTR_TX_MASKED	0x429E0F8C	Transmitter interrupt masked request. See SCB2_INTR_TX_MASKED for the details of bit fields.
SCB6_INTR_RX	0x429E0FC0	Receiver interrupt request. See SCB2_INTR_RX for the details of bit fields.
SCB6_INTR_RX_SET	0x429E0FC4	Receiver interrupt set request. See SCB2_INTR_RX_SET for the details of bit fields.
SCB6_INTR_RX_MASK	0x429E0FC8	Receiver interrupt mask. See SCB2_INTR_RX_MASK for the details of bit fields.
SCB6_INTR_RX_MASKED	0x429E0FCC	Receiver interrupt masked request. See SCB2_INTR_RX_MASKED for the details of bit fields.
SCB7_CTRL	0x429F0000	Generic control. See SCB2_CTRL for the details of bit fields.
SCB7_SPI_CTRL	0x429F0020	SPI control. See SCB2_SPI_CTRL for the details of bit fields.
SCB7_SPI_STATUS	0x429F0024	SPI status. See SCB2_SPI_STATUS for the details of bit fields.
SCB7_SPI_TX_CTRL	0x429F0028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB7_SPI_RX_CTRL	0x429F002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB7_UART_CTRL	0x429F0040	UART control. See SCB2_UART_CTRL for the details of bit fields.
SCB7_UART_TX_CTRL	0x429F0044	UART transmitter control. See SCB2_UART_TX_CTRL for the details of bit fields.
SCB7_UART_RX_CTRL	0x429F0048	UART receiver control. See SCB2_UART_RX_CTRL for the details of bit fields.
SCB7_UART_RX_STATUS	0x429F004C	UART receiver status. See SCB2_UART_RX_STATUS for the details of bit fields.
SCB7_UART_FLOW_CTRL	0x429F0050	UART flow control. See SCB2_UART_FLOW_CTRL for the details of bit fields.
SCB7_I2C_CTRL	0x429F0060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB7_I2C_STATUS	0x429F0064	I2C status. See SCB2_I2C_STATUS for the details of bit fields.

Register name	Address	Description
SCB7_I2C_M_CMD	0x429F0068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB7_I2C_S_CMD	0x429F006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB7_I2C_CFG	0x429F0070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB7_I2C_STRETCH_CTRL	0x429F0074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB7_I2C_STRETCH_STATUS	0x429F0078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB7_TX_CTRL	0x429F0200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB7_TX_FIFO_CTRL	0x429F0204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB7_TX_FIFO_STATUS	0x429F0208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB7_TX_FIFO_WR	0x429F0240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB7_RX_CTRL	0x429F0300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB7_RX_FIFO_CTRL	0x429F0304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB7_RX_FIFO_STATUS	0x429F0308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB7_RX_MATCH	0x429F0310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB7_RX_FIFO_RD	0x429F0340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB7_RX_FIFO_RD_SILENT	0x429F0344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB7_EZ_DATA0	0x429F0400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB7_EZ_DATA0 to SCB7_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB7_INTR_CAUSE	0x429F0E00	Active clocked interrupt signal. See SCB2_INTR_CAUSE for the details of bit fields.
SCB7_INTR_M	0x429F0F00	Master interrupt request. See SCB2_INTR_M for the details of bit fields.
SCB7_INTR_M_SET	0x429F0F04	Master interrupt set request. See SCB2_INTR_M_SET for the details of bit fields.
SCB7_INTR_M_MASK	0x429F0F08	Master interrupt mask. See SCB2_INTR_M_MASK for the details of bit fields.

Register name	Address	Description
SCB7_INTR_M_MASKED	0x429F0F0C	Master interrupt masked request. See SCB2_INTR_M_MASKED for the details of bit fields.
SCB7_INTR_S	0x429F0F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB7_INTR_S_SET	0x429F0F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB7_INTR_S_MASK	0x429F0F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB7_INTR_S_MASKED	0x429F0F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB7_INTR_TX	0x429F0F80	Transmitter interrupt request. See SCB2_INTR_TX for the details of bit fields.
SCB7_INTR_TX_SET	0x429F0F84	Transmitter interrupt set request. See SCB2_INTR_TX_SET for the details of bit fields.
SCB7_INTR_TX_MASK	0x429F0F88	Transmitter interrupt mask. See SCB2_INTR_TX_MASK for the details of bit fields.
SCB7_INTR_TX_MASKED	0x429F0F8C	Transmitter interrupt masked request. See SCB2_INTR_TX_MASKED for the details of bit fields.
SCB7_INTR_RX	0x429F0FC0	Receiver interrupt request. See SCB2_INTR_RX for the details of bit fields.
SCB7_INTR_RX_SET	0x429F0FC4	Receiver interrupt set request. See SCB2_INTR_RX_SET for the details of bit fields.
SCB7_INTR_RX_MASK	0x429F0FC8	Receiver interrupt mask. See SCB2_INTR_RX_MASK for the details of bit fields.
SCB7_INTR_RX_MASKED	0x429F0FCC	Receiver interrupt masked request. See SCB2_INTR_RX_MASKED for the details of bit fields.
SCB8_CTRL	0x42A00000	Generic control. See SCB2_CTRL for the details of bit fields.
SCB8_SPI_CTRL	0x42A00020	SPI control. See SCB2_SPI_CTRL for the details of bit fields.
SCB8_SPI_STATUS	0x42A00024	SPI status. See SCB2_SPI_STATUS for the details of bit fields.
SCB8_SPI_TX_CTRL	0x42A00028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB8_SPI_RX_CTRL	0x42A0002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB8_UART_CTRL	0x42A00040	UART control. See SCB2_UART_CTRL for the details of bit fields.
SCB8_UART_TX_CTRL	0x42A00044	UART transmitter control. See SCB2_UART_TX_CTRL for the details of bit fields.
SCB8_UART_RX_CTRL	0x42A00048	UART receiver control. See SCB2_UART_RX_CTRL for the details of bit fields.
SCB8_UART_RX_STATUS	0x42A0004C	UART receiver status. See SCB2_UART_RX_STATUS for the details of bit fields.

Serial Communication Block (SCB) registers

Register name	Address	Description
SCB8_UART_FLOW_CTRL	0x42A00050	UART flow control. See SCB2_UART_FLOW_CTRL for the details of bit fields.
SCB8_I2C_CTRL	0x42A00060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB8_I2C_STATUS	0x42A00064	I2C status. See SCB2_I2C_STATUS for the details of bit fields.
SCB8_I2C_M_CMD	0x42A00068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB8_I2C_S_CMD	0x42A0006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB8_I2C_CFG	0x42A00070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB8_I2C_STRETCH_CTRL	0x42A00074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB8_I2C_STRETCH_STATUS	0x42A00078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB8_TX_CTRL	0x42A00200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB8_TX_FIFO_CTRL	0x42A00204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB8_TX_FIFO_STATUS	0x42A00208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB8_TX_FIFO_WR	0x42A00240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB8_RX_CTRL	0x42A00300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB8_RX_FIFO_CTRL	0x42A00304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB8_RX_FIFO_STATUS	0x42A00308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB8_RX_MATCH	0x42A00310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB8_RX_FIFO_RD	0x42A00340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB8_RX_FIFO_RD_SILENT	0x42A00344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB8_EZ_DATA0	0x42A00400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB8_EZ_DATA0 to SCB8_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB8_INTR_CAUSE	0x42A00E00	Active clocked interrupt signal. See SCB2_INTR_CAUSE for the details of bit fields.
SCB8_INTR_M	0x42A00F00	Master interrupt request. See SCB2_INTR_M for the details of bit fields.

Serial Communication Block (SCB) registers

Register name	Address	Description
SCB8_INTR_M_SET	0x42A00F04	Master interrupt set request. See SCB2_INTR_M_SET for the details of bit fields.
SCB8_INTR_M_MASK	0x42A00F08	Master interrupt mask. See SCB2_INTR_M_MASK for the details of bit fields.
SCB8_INTR_M_MASKED	0x42A00F0C	Master interrupt masked request. See SCB2_INTR_M_MASKED for the details of bit fields.
SCB8_INTR_S	0x42A00F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB8_INTR_S_SET	0x42A00F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB8_INTR_S_MASK	0x42A00F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB8_INTR_S_MASKED	0x42A00F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB8_INTR_TX	0x42A00F80	Transmitter interrupt request. See SCB2_INTR_TX for the details of bit fields.
SCB8_INTR_TX_SET	0x42A00F84	Transmitter interrupt set request. See SCB2_INTR_TX_SET for the details of bit fields.
SCB8_INTR_TX_MASK	0x42A00F88	Transmitter interrupt mask. See SCB2_INTR_TX_MASK for the details of bit fields.
SCB8_INTR_TX_MASKED	0x42A00F8C	Transmitter interrupt masked request. See SCB2_INTR_TX_MASKED for the details of bit fields.
SCB8_INTR_RX	0x42A00FC0	Receiver interrupt request. See SCB2_INTR_RX for the details of bit fields.
SCB8_INTR_RX_SET	0x42A00FC4	Receiver interrupt set request. See SCB2_INTR_RX_SET for the details of bit fields.
SCB8_INTR_RX_MASK	0x42A00FC8	Receiver interrupt mask. See SCB2_INTR_RX_MASK for the details of bit fields.
SCB8_INTR_RX_MASKED	0x42A00FCC	Receiver interrupt masked request. See SCB2_INTR_RX_MASKED for the details of bit fields.
SCB9_CTRL	0x42A10000	Generic control. See SCB2_CTRL for the details of bit fields.
SCB9_SPI_CTRL	0x42A10020	SPI control. See SCB2_SPI_CTRL for the details of bit fields.
SCB9_SPI_STATUS	0x42A10024	SPI status. See SCB2_SPI_STATUS for the details of bit fields.
SCB9_SPI_TX_CTRL	0x42A10028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB9_SPI_RX_CTRL	0x42A1002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB9_UART_CTRL	0x42A10040	UART control. See SCB2_UART_CTRL for the details of bit fields.
SCB9_UART_TX_CTRL	0x42A10044	UART transmitter control. See SCB2_UART_TX_CTRL for the details of bit fields.

Serial Communication Block (SCB) registers

Register name	Address	Description
SCB9_UART_RX_CTRL	0x42A10048	UART receiver control. See SCB2_UART_RX_CTRL for the details of bit fields.
SCB9_UART_RX_STATUS	0x42A1004C	UART receiver status. See SCB2_UART_RX_STATUS for the details of bit fields.
SCB9_UART_FLOW_CTRL	0x42A10050	UART flow control. See SCB2_UART_FLOW_CTRL for the details of bit fields.
SCB9_I2C_CTRL	0x42A10060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB9_I2C_STATUS	0x42A10064	I2C status. See SCB2_I2C_STATUS for the details of bit fields.
SCB9_I2C_M_CMD	0x42A10068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB9_I2C_S_CMD	0x42A1006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB9_I2C_CFG	0x42A10070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB9_I2C_STRETCH_CTRL	0x42A10074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB9_I2C_STRETCH_STATUS	0x42A10078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB9_TX_CTRL	0x42A10200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB9_TX_FIFO_CTRL	0x42A10204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB9_TX_FIFO_STATUS	0x42A10208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB9_TX_FIFO_WR	0x42A10240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB9_RX_CTRL	0x42A10300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB9_RX_FIFO_CTRL	0x42A10304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB9_RX_FIFO_STATUS	0x42A10308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB9_RX_MATCH	0x42A10310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB9_RX_FIFO_RD	0x42A10340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB9_RX_FIFO_RD_SILENT	0x42A10344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB9_EZ_DATA0	0x42A10400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB9_EZ_DATA0 to SCB9_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.

Register name	Address	Description
SCB9_INTR_CAUSE	0x42A10E00	Active clocked interrupt signal. See SCB2_INTR_CAUSE for the details of bit fields.
SCB9_INTR_M	0x42A10F00	Master interrupt request. See SCB2_INTR_M for the details of bit fields.
SCB9_INTR_M_SET	0x42A10F04	Master interrupt set request. See SCB2_INTR_M_SET for the details of bit fields.
SCB9_INTR_M_MASK	0x42A10F08	Master interrupt mask. See SCB2_INTR_M_MASK for the details of bit fields.
SCB9_INTR_M_MASKED	0x42A10F0C	Master interrupt masked request. See SCB2_INTR_M_MASKED for the details of bit fields.
SCB9_INTR_S	0x42A10F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB9_INTR_S_SET	0x42A10F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB9_INTR_S_MASK	0x42A10F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB9_INTR_S_MASKED	0x42A10F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB9_INTR_TX	0x42A10F80	Transmitter interrupt request. See SCB2_INTR_TX for the details of bit fields.
SCB9_INTR_TX_SET	0x42A10F84	Transmitter interrupt set request. See SCB2_INTR_TX_SET for the details of bit fields.
SCB9_INTR_TX_MASK	0x42A10F88	Transmitter interrupt mask. See SCB2_INTR_TX_MASK for the details of bit fields.
SCB9_INTR_TX_MASKED	0x42A10F8C	Transmitter interrupt masked request. See SCB2_INTR_TX_MASKED for the details of bit fields.
SCB9_INTR_RX	0x42A10FC0	Receiver interrupt request. See SCB2_INTR_RX for the details of bit fields.
SCB9_INTR_RX_SET	0x42A10FC4	Receiver interrupt set request. See SCB2_INTR_RX_SET for the details of bit fields.
SCB9_INTR_RX_MASK	0x42A10FC8	Receiver interrupt mask. See SCB2_INTR_RX_MASK for the details of bit fields.
SCB9_INTR_RX_MASKED	0x42A10FCC	Receiver interrupt masked request. See SCB2_INTR_RX_MASKED for the details of bit fields.
SCB10_CTRL	0x42A20000	Generic control. See SCB2_CTRL for the details of bit fields.
SCB10_SPI_CTRL	0x42A20020	SPI control. See SCB2_SPI_CTRL for the details of bit fields.
SCB10_SPI_STATUS	0x42A20024	SPI status. See SCB2_SPI_STATUS for the details of bit fields.
SCB10_SPI_TX_CTRL	0x42A20028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB10_SPI_RX_CTRL	0x42A2002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.

Serial Communication Block (SCB) registers

Register name	Address	Description
SCB10_UART_CTRL	0x42A20040	UART control. See SCB2_UART_CTRL for the details of bit fields.
SCB10_UART_TX_CTRL	0x42A20044	UART transmitter control. See SCB2_UART_TX_CTRL for the details of bit fields.
SCB10_UART_RX_CTRL	0x42A20048	UART receiver control. See SCB2_UART_RX_CTRL for the details of bit fields.
SCB10_UART_RX_STATUS	0x42A2004C	UART receiver status. See SCB2_UART_RX_STATUS for the details of bit fields.
SCB10_UART_FLOW_CTRL	0x42A20050	UART flow control. See SCB2_UART_FLOW_CTRL for the details of bit fields.
SCB10_I2C_CTRL	0x42A20060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB10_I2C_STATUS	0x42A20064	I2C status. See SCB2_I2C_STATUS for the details of bit fields.
SCB10_I2C_M_CMD	0x42A20068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB10_I2C_S_CMD	0x42A2006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB10_I2C_CFG	0x42A20070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB10_I2C_STRETCH_CTRL	0x42A20074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB10_I2C_STRETCH_STATUS	0x42A20078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB10_TX_CTRL	0x42A20200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB10_TX_FIFO_CTRL	0x42A20204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB10_TX_FIFO_STATUS	0x42A20208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB10_TX_FIFO_WR	0x42A20240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB10_RX_CTRL	0x42A20300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB10_RX_FIFO_CTRL	0x42A20304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB10_RX_FIFO_STATUS	0x42A20308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB10_RX_MATCH	0x42A20310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB10_RX_FIFO_RD	0x42A20340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB10_RX_FIFO_RD_SILENT	0x42A20344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.

Register name	Address	Description
SCB10_EZ_DATA0	0x42A20400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB10_EZ_DATA0 to SCB10_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB10_INTR_CAUSE	0x42A20E00	Active clocked interrupt signal. See SCB2_INTR_CAUSE for the details of bit fields.
SCB10_INTR_M	0x42A20F00	Master interrupt request. See SCB2_INTR_M for the details of bit fields.
SCB10_INTR_M_SET	0x42A20F04	Master interrupt set request. See SCB2_INTR_M_SET for the details of bit fields.
SCB10_INTR_M_MASK	0x42A20F08	Master interrupt mask. See SCB2_INTR_M_MASK for the details of bit fields.
SCB10_INTR_M_MASKED	0x42A20F0C	Master interrupt masked request. See SCB2_INTR_M_MASKED for the details of bit fields.
SCB10_INTR_S	0x42A20F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB10_INTR_S_SET	0x42A20F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB10_INTR_S_MASK	0x42A20F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB10_INTR_S_MASKED	0x42A20F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB10_INTR_TX	0x42A20F80	Transmitter interrupt request. See SCB2_INTR_TX for the details of bit fields.
SCB10_INTR_TX_SET	0x42A20F84	Transmitter interrupt set request. See SCB2_INTR_TX_SET for the details of bit fields.
SCB10_INTR_TX_MASK	0x42A20F88	Transmitter interrupt mask. See SCB2_INTR_TX_MASK for the details of bit fields.
SCB10_INTR_TX_MASKED	0x42A20F8C	Transmitter interrupt masked request. See SCB2_INTR_TX_MASKED for the details of bit fields.
SCB10_INTR_RX	0x42A20FC0	Receiver interrupt request. See SCB2_INTR_RX for the details of bit fields.
SCB10_INTR_RX_SET	0x42A20FC4	Receiver interrupt set request. See SCB2_INTR_RX_SET for the details of bit fields.
SCB10_INTR_RX_MASK	0x42A20FC8	Receiver interrupt mask. See SCB2_INTR_RX_MASK for the details of bit fields.
SCB10_INTR_RX_MASKED	0x42A20FCC	Receiver interrupt masked request. See SCB2_INTR_RX_MASKED for the details of bit fields.
SCB11_CTRL	0x42A30000	Generic control. See SCB2_CTRL for the details of bit fields.
SCB11_SPI_CTRL	0x42A30020	SPI control. See SCB2_SPI_CTRL for the details of bit fields.
SCB11_SPI_STATUS	0x42A30024	SPI status. See SCB2_SPI_STATUS for the details of bit fields.

Serial Communication Block (SCB) registers

Register name	Address	Description
SCB11_SPI_TX_CTRL	0x42A30028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB11_SPI_RX_CTRL	0x42A3002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB11_UART_CTRL	0x42A30040	UART control. See SCB2_UART_CTRL for the details of bit fields.
SCB11_UART_TX_CTRL	0x42A30044	UART transmitter control. See SCB2_UART_TX_CTRL for the details of bit fields.
SCB11_UART_RX_CTRL	0x42A30048	UART receiver control. See SCB2_UART_RX_CTRL for the details of bit fields.
SCB11_UART_RX_STATUS	0x42A3004C	UART receiver status. See SCB2_UART_RX_STATUS for the details of bit fields.
SCB11_UART_FLOW_CTRL	0x42A30050	UART flow control. See SCB2_UART_FLOW_CTRL for the details of bit fields.
SCB11_I2C_CTRL	0x42A30060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB11_I2C_STATUS	0x42A30064	I2C status. See SCB2_I2C_STATUS for the details of bit fields.
SCB11_I2C_M_CMD	0x42A30068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB11_I2C_S_CMD	0x42A3006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB11_I2C_CFG	0x42A30070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB11_I2C_STRETCH_CTRL	0x42A30074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB11_I2C_STRETCH_STATUS	0x42A30078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB11_TX_CTRL	0x42A30200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB11_TX_FIFO_CTRL	0x42A30204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB11_TX_FIFO_STATUS	0x42A30208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB11_TX_FIFO_WR	0x42A30240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB11_RX_CTRL	0x42A30300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB11_RX_FIFO_CTRL	0x42A30304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB11_RX_FIFO_STATUS	0x42A30308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB11_RX_MATCH	0x42A30310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.

Register name	Address	Description
SCB11_RX_FIFO_RD	0x42A30340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB11_RX_FIFO_RD_SILENT	0x42A30344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB11_EZ_DATA0	0x42A30400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB11_EZ_DATA0 to SCB11_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB11_INTR_CAUSE	0x42A30E00	Active clocked interrupt signal. See SCB2_INTR_CAUSE for the details of bit fields.
SCB11_INTR_M	0x42A30F00	Master interrupt request. See SCB2_INTR_M for the details of bit fields.
SCB11_INTR_M_SET	0x42A30F04	Master interrupt set request. See SCB2_INTR_M_SET for the details of bit fields.
SCB11_INTR_M_MASK	0x42A30F08	Master interrupt mask. See SCB2_INTR_M_MASK for the details of bit fields.
SCB11_INTR_M_MASKED	0x42A30F0C	Master interrupt masked request. See SCB2_INTR_M_MASKED for the details of bit fields.
SCB11_INTR_S	0x42A30F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB11_INTR_S_SET	0x42A30F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB11_INTR_S_MASK	0x42A30F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB11_INTR_S_MASKED	0x42A30F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB11_INTR_TX	0x42A30F80	Transmitter interrupt request. See SCB2_INTR_TX for the details of bit fields.
SCB11_INTR_TX_SET	0x42A30F84	Transmitter interrupt set request. See SCB2_INTR_TX_SET for the details of bit fields.
SCB11_INTR_TX_MASK	0x42A30F88	Transmitter interrupt mask. See SCB2_INTR_TX_MASK for the details of bit fields.
SCB11_INTR_TX_MASKED	0x42A30F8C	Transmitter interrupt masked request. See SCB2_INTR_TX_MASKED for the details of bit fields.
SCB11_INTR_RX	0x42A30FC0	Receiver interrupt request. See SCB2_INTR_RX for the details of bit fields.
SCB11_INTR_RX_SET	0x42A30FC4	Receiver interrupt set request. See SCB2_INTR_RX_SET for the details of bit fields.
SCB11_INTR_RX_MASK	0x42A30FC8	Receiver interrupt mask. See SCB2_INTR_RX_MASK for the details of bit fields.
SCB11_INTR_RX_MASKED	0x42A30FCC	Receiver interrupt masked request. See SCB2_INTR_RX_MASKED for the details of bit fields.
SCB1_CTRL	0x42D00000	Generic control. See SCB2_CTRL for the details of bit fields.

Register name	Address	Description
SCB1_SPI_CTRL	0x42D00020	SPI control. See SCB2_SPI_CTRL for the details of bit fields.
SCB1_SPI_STATUS	0x42D00024	SPI status. See SCB2_SPI_STATUS for the details of bit fields.
SCB1_SPI_TX_CTRL	0x42D00028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB1_SPI_RX_CTRL	0x42D0002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB1_UART_CTRL	0x42D00040	UART control. See SCB2_UART_CTRL for the details of bit fields.
SCB1_UART_TX_CTRL	0x42D00044	UART transmitter control. See SCB2_UART_TX_CTRL for the details of bit fields.
SCB1_UART_RX_CTRL	0x42D00048	UART receiver control. See SCB2_UART_RX_CTRL for the details of bit fields.
SCB1_UART_RX_STATUS	0x42D0004C	UART receiver status. See SCB2_UART_RX_STATUS for the details of bit fields.
SCB1_UART_FLOW_CTRL	0x42D00050	UART flow control. See SCB2_UART_FLOW_CTRL for the details of bit fields.
SCB1_I2C_CTRL	0x42D00060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB1_I2C_STATUS	0x42D00064	I2C status. See SCB2_I2C_STATUS for the details of bit fields.
SCB1_I2C_M_CMD	0x42D00068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB1_I2C_S_CMD	0x42D0006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB1_I2C_CFG	0x42D00070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB1_I2C_STRETCH_CTRL	0x42D00074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB1_I2C_STRETCH_STATUS	0x42D00078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB1_TX_CTRL	0x42D00200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB1_TX_FIFO_CTRL	0x42D00204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB1_TX_FIFO_STATUS	0x42D00208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB1_TX_FIFO_WR	0x42D00240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB1_RX_CTRL	0x42D00300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB1_RX_FIFO_CTRL	0x42D00304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.

Register name	Address	Description
SCB1_RX_FIFO_STATUS	0x42D00308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB1_RX_MATCH	0x42D00310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB1_RX_FIFO_RD	0x42D00340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB1_RX_FIFO_RD_SILENT	0x42D00344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB1_EZ_DATA0	0x42D00400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB1_EZ_DATA0 to SCB1_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_INTR_CAUSE	0x42D00E00	Active clocked interrupt signal. See SCB2_INTR_CAUSE for the details of bit fields.
SCB1_INTR_M	0x42D00F00	Master interrupt request. See SCB2_INTR_M for the details of bit fields.
SCB1_INTR_M_SET	0x42D00F04	Master interrupt set request. See SCB2_INTR_M_SET for the details of bit fields.
SCB1_INTR_M_MASK	0x42D00F08	Master interrupt mask. See SCB2_INTR_M_MASK for the details of bit fields.
SCB1_INTR_M_MASKED	0x42D00F0C	Master interrupt masked request. See SCB2_INTR_M_MASKED for the details of bit fields.
SCB1_INTR_S	0x42D00F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB1_INTR_S_SET	0x42D00F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB1_INTR_S_MASK	0x42D00F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB1_INTR_S_MASKED	0x42D00F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB1_INTR_TX	0x42D00F80	Transmitter interrupt request. See SCB2_INTR_TX for the details of bit fields.
SCB1_INTR_TX_SET	0x42D00F84	Transmitter interrupt set request. See SCB2_INTR_TX_SET for the details of bit fields.
SCB1_INTR_TX_MASK	0x42D00F88	Transmitter interrupt mask. See SCB2_INTR_TX_MASK for the details of bit fields.
SCB1_INTR_TX_MASKED	0x42D00F8C	Transmitter interrupt masked request. See SCB2_INTR_TX_MASKED for the details of bit fields.
SCB1_INTR_RX	0x42D00FC0	Receiver interrupt request. See SCB2_INTR_RX for the details of bit fields.
SCB1_INTR_RX_SET	0x42D00FC4	Receiver interrupt set request. See SCB2_INTR_RX_SET for the details of bit fields.

Serial Communication Block (SCB) registers

Register name	Address	Description
SCB1_INTR_RX_MASK	0x42D00FC8	Receiver interrupt mask. See SCB2_INTR_RX_MASK for the details of bit fields.
SCB1_INTR_RX_MASKED	0x42D00FCC	Receiver interrupt masked request. See SCB2_INTR_RX_MASKED for the details of bit fields.

18.1.1 SCB0_CTRL

Description: Generic control

Address: 0x42990000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		Reserved	RW	Reserved	RW	RW	RW
HW Access	R		Reserved	R	Reserved	R	R	R
Name	MEM_WIDTH [15:14]		Reserved	CMD_RESP_MODE	Reserved	EZ_MODE	EC_OP_MODE	EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [23:18]						BLOCK	ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved		RW	Reserved		RW	
HW Access	R	Reserved		R	Reserved		R	
Name	ENABLED	Reserved [30:29]		EC_ACCESS	Reserved [27:26]		MODE [25:24]	

Bits	Name	Description
31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. Generally when this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Specific to SPI master case, when SCB is idle, below registers can be changed without disabling SCB block, TX_CTRL TX_FIFO_CTRL RX_CTRL RX_FIFO_CTRL SPI_CTRL.SSEL, Default Value: 0

18.1.1 SCB0_CTRL (continued)

28	EC_ACCESS	EC_ACCESS is used to enable I2CS_EC or SPIS_EC access to internal EZ memory. 1: enable clk_scb 0: disable clk_scb Before going to deepsleep this field should be set to 1. when waking up from DeepSleep power mode, and PLL is locked (clk_scb is at expected frequency), this field should be set to 0. Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3 **0x0: I2C :** Inter-Integrated Circuits (I2C) mode. **0x1: SPI :** Serial Peripheral Interface (SPI) mode. **0x2: UART :** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is '0' and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
15 : 14	MEM_WIDTH	Determines the number of bits per FIFO data element, depending on physical SRAM cell data width. Default Value: 1 **0x0: BYTE :** 8-bit FIFO data elements. This mode provides the biggest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. **0x1: HALFWORD :** 16-bit FIFO data elements. TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 15]. **0x2: WORD :** 32-bit FIFO data elements. This mode provides the smallest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH can be in a range of [0, 31]. **0x3: Reserved :** This setting is reserved. Do not use.

18.1.1 SCB0_CTRL (continued)

12	CMD_RESP_MODE	Determines CMD_RESP mode of operation: '0': CMD_RESP mode disabled. '1': CMD_RESP mode enabled (also requires EC_AM_MODE and EC_OP_MODE to be set to '1'). Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0
8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

18.1.1 SCB0_CTRL (continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

18.1.2 SCB0_STATUS

Description: Generic status

Address: 0x42990004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

18.1.3 SCB0_CMD_RESP_CTRL

Description: Command/response control

Address: 0x42990008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BASE_RD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BASE_WR_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	BASE_WR_ADDR	I2C/SPI write base address for CMD_RESP mode. At the start of a write transfer this BASE_WR_ADDR is copied to CMD_RESP_STATUS.CURR_WR_ADDR. This field should not be modified during ongoing bus transfers. Default Value: 0
7 : 0	BASE_RD_ADDR	I2C/SPI read base address for CMD_RESP mode. At the start of a read transfer this BASE_RD_ADDR is copied to CMD_RESP_STATUS.CURR_RD_ADDR. This field should not be modified during ongoing bus transfers. Default Value: 0

18.1.4 SCB0_CMD_RESP_STATUS

Description: Command/response status

Address: 0x4299000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CURR_RD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	CURR_WR_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	Reserved					
HW Access	W	W	Reserved					
Name	CMD_RESP_EC_BUSY	CMD_RESP_EC_BUS_BUSY	Reserved [29:24]					

Bits	Name	Description
31	CMD_RESP_EC_BUSY	Indicates whether the CURR_RD_ADDR and CURR_WR_ADDR fields in this register are reliable (when CMD_RESP_EC_BUSY is '0') or not reliable (when CMD_RESP_EC_BUSY is '1'). Note: - When there is no ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable). - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable), when the CURR_RD_ADDR and CURR_WR_ADDR are not being updated by the HW. - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '1' (not reliable), when the CURR_RD_ADDR or CURR_WR_ADDR are being updated by the HW. Note that this update lasts one I2C clock cycle, or two SPI clock cycles. Default Value: Undefined
30	CMD_RESP_EC_BUS_BUSY	Indicates whether there is an ongoing bus transfer to the IP. '0': no ongoing bus transfer. '1': ongoing bus transfer. For SPI, the field is '1' when slave mode is selected. For I2C, the field is set to '1' at a I2C START/RESTART. In case of an address match, the field is set to '0' on a I2C STOP. In case of NO address match, the field is set to '0' after the failing address match. Default Value: Undefined

18.1.4 SCB0_CMD_RESP_STATUS (continued)

23 : 16	CURR_WR_ADDR	I2C/SPI write current address for CMD_RESP mode. HW increments the field after a write access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address). The field is used to determine how many bytes have been written (# bytes = CURR_WR_ADDR - CMD_RESP_CTRL.BASE_WR_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable. Default Value: Undefined
7 : 0	CURR_RD_ADDR	I2C/SPI read current address for CMD_RESP mode. HW increments the field after a read access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address). The field is used to determine how many bytes have been read (# bytes = CURR_RD_ADDR - CMD_RESP_CTRL.BASE_RD_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable. Default Value: Undefined

18.1.5 SCB0_SPI_CTRL

Description: SPI control

Address: 0x42990020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	RW	RW	Reserved
HW Access	Reserved			R	R	R	R	Reserved
Name	Reserved [7:5]			LATE_SAM-PLE	CPOL	CPHA	SE-LECT_PRE-CEDE	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved	R	R	R	R	R	R	R
Name	Reserved	SSEL_INTE R_-FRAME_DE L	SSEL_HOL D_DEL	SSEL_SET-UP_DEL	SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW		RW	
HW Access	Reserved				R		R	
Name	Reserved [31:28]				SSEL [27:26]		MODE [25:24]	

Bits	Name	Description
27 : 26	SSEL	Selects one of the four incoming/outgoing SPI slave select signals: - 0: Slave 0, SSEL[0]. - 1: Slave 1, SSEL[1]. - 2: Slave 2, SSEL[2]. - 3: Slave 3, SSEL[3]. SCB block should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3 **0x0: SPI_MOTOROLA :** SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.

18.1.5 SCB0_SPI_CTRL (continued)

		0x1: SPI_TI : SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS :** SPI National Semiconductors submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
14	SSEL_INTER_-FRAME_DEL	Indicates the SPI SELECT inter-dataframe delay (between SELECT deactivation and SELECT activation). '0': 1.5 SPI clock cycles '1': 2.5 SPI clock cycles Only applies in SPI MOTOROLA submode and when SPI_CTRL.SSEL_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
13	SSEL_HOLD_DEL	Indicates the SPI SELECT hold delay (between SPI clock edge to sample the last MOSI bit, and SELECT deactivation). '0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
12	SSEL_SETUP_DEL	Indicates the SPI SELECT setup delay (between SELECT activation and SCLK clock edge to sample the first MOSI bit). '0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0

18.1.5 SCB0_SPI_CTRL (continued)

4	LATE_SAMPLE	Changes the SCLK edge on which MISO is captured in master mode, or MOSI is captured in slave mode. When '0', the default applies, for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK(CPOL is '0' and CPHA is '1'), for National Semiconductors on the rising edge of SCLK(CPOL is '0' and CPHA is '0'). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). for master, applicable to all Motorola, TI and National Semiconductors flavors, and CPOL/CPHA timing mdoes. for slave, applicable to Motorola flavor only, and CPHA=0 timing modes only, and internally-clocked mode only. Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 1
3	CPOL	Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is '0': SCLK is '0' when not transmitting data. - CPOL is '1': SCLK is '1' when not transmitting data. Default Value: 0
2	CPHA	Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is '0', CPHA is '0': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is '0', CPHA is '1': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is '1', CPHA is '0': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is '1', CPHA is '1': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. In SPI Motorola submode, all four CPOL/CPHA modes are valid. in SPI NS submode, only CPOL=0 CPHA=0 mode is valid. in SPI TI submode, only CPOL=0 CPHA=1 mode is valid. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0

18.1.6 SCB0_SPI_STATUS

Description: SPI status

Address: 0x42990024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

18.1.7 SCB0_SPI_TX_CTRL

Description: SPI transmitter control

Address: 0x42990028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	Reserved			
HW Access	Reserved		R	R	Reserved			
Name	Reserved [7:6]		PARITY_ENABLED	PARITY	Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							MOSI_IDLE_HIGH

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	MOSI_IDLE_HIGH	SPI master MOSI output level when SELECT output inactive, 0: retain the level of last data bit 1: change to high, (MOSI level is high, before the first data bit time, and after data bit time, defined SSEL/SCLK driving edge with CPOL/CPHA) Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Default Value: 0

18.1.8 SCB0_SPI_RX_CTRL

Description: SPI receiver control

Address: 0x4299002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	Reserved			
HW Access	Reserved		R	R	Reserved			
Name	Reserved [7:6]		PARITY_ENABLED	PARITY	Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	DROP_ON_PARITY_ERROR	Behavior when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Default Value: 0

18.1.9 SCB0_I2C_CTRL

Description: I2C control

Address: 0x42990060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved	RW	RW
HW Access	R	R	R	R	R	Reserved	R	R
Name	S_NOT_READY_-DATA_NACK	S_NOT_READY_AD-DR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENER-AL_IGNORE	Reserved	M_NOT_READY_-DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved					
HW Access	R	R	Reserved					
Name	MASTER_-MODE	SLAVE_-MODE	Reserved [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0
15	S_NOT_READY_-DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

18.1.9 SCB0_I2C_CTRL (continued)

14	S_NOT_READY_ADDR_NACK	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles. in slave mode, this field is used to define number of clk_scb cycles for tSU-DAT timing (from ACK/NACK/data ready, to SCL rising edge (released from I2C slave clock stretching)) Default Value: 8
3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8

18.1.10 SCB0_I2C_STATUS

Description: I2C status

Address: 0x42990064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R	R	Reserved	R	R	R
HW Access	Reserved		W	W	Reserved	W	W	W
Name	Reserved [7:6]		M_READ	S_READ	Reserved	I2CS_IC_BUSY	I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
2	I2CS_IC_BUSY	Indicates whether the internally clocked slave logic is being accessed by external I2C master. --set at ADDR_MATCH --clear at START/RESET, STOP detection, or BUS_ERROR This bit can be used by SW to determine whether I2CS_IC is busy before entering DeepSleep. Default Value: 0
1	I2C_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_EZ_ADDR or CURR_EZ_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_EZ_ADDR and CURR_EZ_ADDR are reliable. Default Value: Undefined

18.1.10 SCB0_I2C_STATUS (continued)

0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

18.1.11 SCB0_I2C_M_CMD

Description: I2C master command

Address: 0x42990068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	RW	RW	RW
HW Access	Reserved			RW1C	RW1C	RW1C	RW1C	RW1C
Name	Reserved [7:5]			M_STOP	M_NACK	M_ACK	M_START_ ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	for I2C master, the NACKed byte should be properly received. it write the data byte, before ACK/ NACK decision. When '1', attempt to transmit a negative acknowledgement (NACK). if the reciever FIFO is full (the received data byte cannot be written), it stretch SCL(extend SCL low phase) until the receiver FIFO changes to not full, to write the last byte, then send out NACK. When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0

18.1.11 SCB0_I2C_M_CMD (continued)

0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

18.1.12 SCB0_I2C_S_CMD

Description: I2C slave command

Address: 0x4299006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	RW1C	RW1C
Name	Reserved [7:3]					S_TX-_ONES_ON_EMPTY	S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	S_TX_ONES_ON_EMP-TY	When '1', attempt to send ones when TX_FIFO is empty. Once hardware starts to send ones, it will continue send ones until NACK is received, regardless of TX_FIFO status (even if new data is written into TX_FIFO). This bit is used to avoid stretching SCL, which is not expected for some master devices. Default Value: 0
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is per-formed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_C-TRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

18.1.13 SCB0_I2C_CFG

Description: I2C configuration

Address: 0x42990070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved		RW	
HW Access	Reserved			R	Reserved		R	
Name	Reserved [7:5]			SDA_IN_-FILT_SEL	Reserved [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved		RW	
HW Access	Reserved			R	Reserved		R	
Name	Reserved [15:13]			SCL_IN_-FILT_SEL	Reserved [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		RW		RW	
HW Access	Reserved		R		R		R	
Name	Reserved [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW		Reserved			
HW Access	Reserved		R		Reserved			
Name	Reserved [31:30]		SDA_OUT_FILT_SEL [29:28]		Reserved [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative 'i2c_sda_out' filter delay on SDA output. "0": 0 ns. "1", "2" or "3": 50 ns (filter 0 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
12	SCL_IN_FILT_SEL	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch re-jections specs. Programmability available if required Default Value: 0

18.1.13 SCB0_I2C_CFG (continued)

4	SDA_IN_FILT_SEL	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 3

18.1.14 SCB0_I2C_STRETCH_CTRL

Description: I2C stretch control

Address: 0x42990074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				STRETCH_THRESHOLD [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	STRETCH_THRESHOLD	stretch threthold. Typically it is the SCL turaound delay (including IO cell delay, SCL rise time, analog filter delay), in number of clk_scb cycles. When STRETCH_COUNT is higher than this STRETCH_THRESHOLD, STRETCH_DETECTED will be set. STRETCH_DETECTED should be less than "HOVS-2", HOVS means I2C_CTRL.HIGH_PHASE_OVS, or I2C_CTRL_HS.HOVS_HS. Default Value: 0

18.1.15 SCB0_I2C_STRETCH_STATUS

Description: I2C stretch status

Address: 0x42990078

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R	R	R			
HW Access	Reserved		W	W	W			
Name	Reserved [7:6]		SYNC_DE-TECTED	STRETCH_ DETECTED	STRETCH_COUNT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							STRETCH-ING

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	STRETCHING	I2C SCL is stretched by this block. For I2C master, this can happen when TX FIFO is empty, or RX_FIFO is full, or ACK/NACK is not decided, or RESTART/STOP is not decided. For I2C slave, this can heppend, TX FIFO is empty, or RX_FIFO is full, or ACK/NACK is not decided. Default Value: 0
5	SYNC_DETECTED	Synchronization detected. Set when I2C falling edge comes in earlier than expected (suppressed by another I2C master during synchronization). Default Value: 0
4	STRETCH_DETECTED	Set when I2C rising edge comes later than expected (suppressed by another master or slave), and STRETCH_COUNT is higher than STRETCH_THRESHOLD. Default Value: 0
3 : 0	STRETCH_COUNT	Started when I2C device start to drive high phase on internal SCL output signal, stalled when it detected high level on SCL input signal. Default Value: 0

18.1.16 SCB0_TX_CTRL

Description: Transmitter control

Address: 0x42990200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			DATA_WIDTH [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [23:18]						OPEN_DRAIN_SCL	OPEN_DRAIN

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17	OPEN_DRAIN_SCL	Each IO cell "xxx" has two associated IP output signals "xxx_out_en" and "xxx_out". '0': Normal operation mode. Typically, this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by a single IO cell. In this operation mode, for an IO cell "xxx" that is used as an output, the "xxx_out_en" output enable signal is typically constant '1' the "xxx_out" output is the outputted value. In other words, in normal operation mode, the "xxx_out" output is used to control the IO cell output value: "xxx_out" is '0' to drive an IO cell output value of '0' and "xxx_out" is '1' to drive an IO cell output value of '1'. '1': Open drain operation mode. Typically this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by multiple IO cells (possibly on multiple chips). In this operation mode, for and IO cell "xxx" that is used as an output, the "xxx_out_en" output controls the outputted value. Typically, open drain operation mode drives low/'0' and the "xxx_out" output is constant '1'. In other words, in open drain operation mode, the "xxx_out_en" output is used to control the IO cell output value: in drive low/'0' mode: "xxx_out_en" is '1' (drive enabled) to drive an IO cell output value of '0' and "xxx_out_en" is '1' (drive disabled) to not drive an IO cell output value (another IO cell can drive the wire/line or a pull up results in a wire/line value '1'). this bit is applicable to I2C SCL only. I2C SDA always work in open-drain mode. this is not applicable to M0S8, which does not need special control in SCB for open-drain drive mode. Default Value: 1

18.1.16 SCB0_TX_CTRL (continued)

16	OPEN_DRAIN	Each IO cell "xxx" has two associated IP output signals "xxx_out_en" and "xxx_out". '0': Normal operation mode. Typically, this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by a single IO cell. In this operation mode, for an IO cell "xxx" that is used as an output, the "xxx_out_en" output enable signal is typically constant '1' the "xxx_out" output is the outputted value. In other words, in normal operation mode, the "xxx_out" output is used to control the IO cell output value: "xxx_out" is '0' to drive an IO cell output value of '0' and "xxx_out" is '1' to drive an IO cell output value of '1'. '1': Open drain operation mode. Typically this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by multiple IO cells (possibly on multiple chips). In this operation mode, for and IO cell "xxx" that is used as an output, the "xxx_out_en" output controls the outputted value. Typically, open drain operation mode drives low/'0' and the "xxx_out" output is constant '1'. In other words, in open drain operation mode, the "xxx_out_en" output is used to control the IO cell output value: in drive low/'0' mode: "xxx_out_en" is '1' (drive enabled) to drive an IO cell output value of '0' and "xxx_out_en" is '1' (drive disabled) to not drive an IO cell output value (another IO cell can drive the wire/line or a pull up results in a wire/line value '1'). The open drain mode is supported for: - UART mode, "uart_tx" IO cell. - SPI mode, "spi_miso" IO cell. this bit is not applicable to I2C mode, "i2c_scl" and "i2c_sda" IO cells. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
4 : 0	DATA_WIDTH	Dataframe width, depending on CTRL.MEM_WIDTH. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

18.1.17 SCB0_TX_FIFO_CTRL

Description: Transmitter FIFO control

Address: 0x42990204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event INTR_TX.TRIGGER is generated. Default Value: 0

18.1.18 SCB0_TX_FIFO_STATUS

Description: Transmitter FIFO status

Address: 0x42990208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	SR_VALID	Reserved [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	R						
HW Access	Reserved	W						
Name	Reserved	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R						
HW Access	Reserved	W						
Name	Reserved	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
22 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
7 : 0	USED	Amount of entries in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). Default Value: 0

18.1.19 SCB0_TX_FIFO_WR

Description: Transmitter FIFO write

Address: 0x42990240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

18.1.20 SCB0_RX_CTRL

Description: Receiver control

Address: 0x42990300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			DATA_WIDTH [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
4 : 0	DATA_WIDTH	Dataframe width, depending on CTRL.MEM_WIDTH. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

18.1.21 SCB0_RX_FIFO_CTRL

Description: Receiver FIFO control

Address: 0x42990304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event INTR_RX.TRIGGER is generated. Default Value: 0

18.1.22 SCB0_RX_FIFO_STATUS

Description: Receiver FIFO status

Address: 0x42990308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	SR_VALID	Reserved [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	R						
HW Access	Reserved	W						
Name	Reserved	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R						
HW Access	Reserved	W						
Name	Reserved	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
22 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
7 : 0	USED	Amount of entries in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). Default Value: 0

18.1.23 SCB0_RX_MATCH

Description: Slave address and mask

Address: 0x42990310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

18.1.24 SCB0_RX_FIFO_RD

Description: Receiver FIFO read

Address: 0x42990340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

18.1.25 SCB0_RX_FIFO_RD_SILENT

Description: Receiver FIFO read silent

Address: 0x42990344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

18.1.26 SCB0_EZ_DATA0

Description: Memory buffer

Address: 0x42990400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

18.1.27 SCB0_INTR_CAUSE

Description: Active clocked interrupt signal

Address: 0x42990E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		W	W	W	W	W	W
Name	Reserved [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

18.1.28 SCB0_INTR_I2C_EC

Description: Externally clocked I2C interrupt request

Address: 0x42990E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1C	RW1C	RW1C	RW1C
HW Access	Reserved				A	A	A	A
Name	Reserved [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

18.1.29 SCB0_INTR_I2C_EC_MASK

Description: Externally clocked I2C interrupt mask

Address: 0x42990E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.30 SCB0_INTR_I2C_EC_MASKED

Description: Externally clocked I2C interrupt masked

Address: 0x42990E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

18.1.31 SCB0_INTR_SPI_EC

Description: Externally clocked SPI interrupt request

Address: 0x42990EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1C	RW1C	RW1C	RW1C
HW Access	Reserved				A	A	A	A
Name	Reserved [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. Default Value: 0
0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

18.1.32 SCB0_INTR_SPI_EC_MASK

Description: Externally clocked SPI interrupt mask

Address: 0x42990EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.33 SCB0_INTR_SPI_EC_MASKED

Description: Externally clocked SPI interrupt masked

Address: 0x42990ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

18.1.34 SCB0_INTR_M

Description: Master interrupt request

Address: 0x42990F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	Reserved	RW1C	RW1C	RW1C
HW Access	Reserved			RW1S	Reserved	RW1S	RW1S	RW1S
Name	Reserved [7:5]			I2C_STOP	Reserved	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							RW1S
Name	Reserved [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. The Firmware should clear the TX FIFO, to re-do this transfer. Default Value: 0

18.1.35 SCB0_INTR_M_SET

Description: Master interrupt set request

Address: 0x42990F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1S	Reserved	RW1S	RW1S	RW1S
HW Access	Reserved			A	Reserved	A	A	A
Name	Reserved [7:5]			I2C_STOP	Reserved	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.36 SCB0_INTR_M_MASK

Description: Master interrupt mask

Address: 0x42990F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved	RW	RW	RW
HW Access	Reserved			R	Reserved	R	R	R
Name	Reserved [7:5]			I2C_STOP	Reserved	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.37 SCB0_INTR_M_MASKED

Description: Master interrupt masked request

Address: 0x42990F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R	Reserved	R	R	R
HW Access	Reserved			W	Reserved	W	W	W
Name	Reserved [7:5]			I2C_STOP	Reserved	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

18.1.38 SCB0_INTR_S

Description: Slave interrupt request

Address: 0x42990F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW1C	RW1C	RW1C	RW1C
HW Access	Reserved				RW1S	RW1S	RW1S	RW1S
Name	Reserved [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW1C
HW Access	Reserved							RW1S
Name	Reserved [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	I2C_RESTART	I2C slave RESTART received. Set to '1', when REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. Default Value: 0
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0

18.1.38 SCB0_INTR_S (continued)

6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

18.1.39 SCB0_INTR_S_SET

Description: Slave interrupt set request

Address: 0x42990F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW1S	RW1S	RW1S	RW1S
HW Access	Reserved				A	A	A	A
Name	Reserved [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	I2C_RESTART	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.39 SCB0_INTR_S_SET (continued)

2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.40 SCB0_INTR_S_MASK

Description: Slave interrupt mask

Address: 0x42990F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	I2C_RESTART	Mask bit for corresponding bit in interrupt request register. Default Value: 0
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.40 SCB0_INTR_S_MASK (continued)

2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.41 SCB0_INTR_S_MASKED

Description: Slave interrupt masked request

Address: 0x42990F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	I2C_RESTART	Logical and of corresponding request and mask bits. Default Value: 0
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0

18.1.41 SCB0_INTR_S_MASKED (continued)

2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

18.1.42 SCB0_INTR_TX

Description: Transmitter interrupt request

Address: 0x42990F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	Reserved		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	Reserved		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	Reserved [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	BLOCKED	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty) Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is "0": # entries != FF_DATA_NR. MEM_WIDTH is "1": # entries != FF_DATA_NR/2. MEM_WIDTH is "2": # entries != FF_DATA_NR/4. Only used in FIFO mode. Default Value: 0

18.1.42 SCB0_INTR_TX (continued)

0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

18.1.43 SCB0_INTR_TX_SET

Description: Transmitter interrupt set request

Address: 0x42990F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	Reserved		RW1S	RW1S
HW Access	A	A	A	A	Reserved		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	Reserved [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.44 SCB0_INTR_TX_MASK

Description: Transmitter interrupt mask

Address: 0x42990F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	Reserved		RW	RW
HW Access	R	R	R	R	Reserved		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	Reserved [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.45 SCB0_INTR_TX_MASKED

Description: Transmitter interrupt masked request

Address: 0x42990F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	Reserved		R	R
HW Access	W	W	W	W	Reserved		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	Reserved [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

18.1.46 SCB0_INTR_RX

Description: Receiver interrupt request

Address: 0x42990FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	Reserved	RW1C	RW1C	Reserved	RW1C
HW Access	RW1S	RW1S	RW1S	Reserved	RW1S	RW1S	Reserved	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	Reserved	FULL	NOT_EMP-TY	Reserved	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW1C	Reserved
HW Access	Reserved						RW1S	Reserved
Name	Reserved [15:10]						PARI-TY_ERROR	Reserved

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is "0": # entries == FF_DATA_NR. MEM_WIDTH is "1": # entries == FF_DATA_NR/2. MEM_WIDTH is "2": # entries == FF_DATA_NR/4. Only used in FIFO mode. Default Value: 0

18.1.46 SCB0_INTR_RX (continued)

2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by RX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

18.1.47 SCB0_INTR_RX_SET

Description: Receiver interrupt set request

Address: 0x42990FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	Reserved	RW1S	RW1S	Reserved	RW1S
HW Access	A	A	A	Reserved	A	A	Reserved	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	Reserved	FULL	NOT_EMP-TY	Reserved	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW1S	Reserved
HW Access	Reserved						A	Reserved
Name	Reserved [15:10]						PARI-TY_ERROR	Reserved

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.48 SCB0_INTR_RX_MASK

Description: Receiver interrupt mask

Address: 0x42990FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	Reserved	RW	RW	Reserved	RW
HW Access	R	R	R	Reserved	R	R	Reserved	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	Reserved	FULL	NOT_EMP-TY	Reserved	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	Reserved
HW Access	Reserved						R	Reserved
Name	Reserved [15:10]						PARI-TY_ERROR	Reserved

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.49 SCB0_INTR_RX_MASKED

Description: Receiver interrupt masked request

Address: 0x42990FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	Reserved	R	R	Reserved	R
HW Access	W	W	W	Reserved	W	W	Reserved	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	Reserved	FULL	NOT_EMP-TY	Reserved	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						R	Reserved
HW Access	Reserved						W	Reserved
Name	Reserved [15:10]						PARI-TY_ERROR	Reserved

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

18.1.50 SCB2_CTRL

Description: Generic control

Address: 0x429A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		Reserved			RW	Reserved	
HW Access	R		Reserved			R	Reserved	
Name	MEM_WIDTH [15:14]		Reserved [13:11]			EZ_MODE	Reserved [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved					RW	
HW Access	R	Reserved					R	
Name	ENABLED	Reserved [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. Generally when this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Specific to SPI master case, when SCB is idle, below registers can be changed without disabling SCB block, TX_CTRL TX_FIFO_CTRL RX_CTRL RX_FIFO_CTRL SPI_CTRL.SSEL, Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3

18.1.50 SCB2_CTRL (continued)

		0x0: I2C : Inter-Integrated Circuits (I2C) mode. **0x1: SPI :** Serial Peripheral Interface (SPI) mode. **0x2: UART :** Universal Asynchronous Receiver/Transmitter (UART) mode.
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
15 : 14	MEM_WIDTH	Determines the number of bits per FIFO data element, depending on physical SRAM cell data width. Default Value: 1 **0x0: BYTE :** 8-bit FIFO data elements. This mode provides the biggest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX-_CTRL.DATA_WIDTH are restricted to [0, 7]. **0x1: HALFWORD :** 16-bit FIFO data elements. TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 15]. **0x2: WORD :** 32-bit FIFO data elements. This mode provides the smallest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX-_CTRL.DATA_WIDTH can be in a range of [0, 31]. **0x3: Reserved :** This setting is reserved. Do not use.
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0

18.1.50 SCB2_CTRL (continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

18.1.51 SCB2_SPI_CTRL

Description: SPI control

Address: 0x429A0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		SCLK_-CONTINU-OUS	LATE_SAM-PLE	CPOL	CPHA	SE-LECT_PRE-CEDE	SSEL_-CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved	R	R	R	R	R	R	R
Name	Reserved	SSEL_INTE R_-FRAME_DE L	SSEL_HOL D_DEL	SSEL_SET-UP_DEL	SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved			RW		RW	
HW Access	R	Reserved			R		R	
Name	MASTER_-MODE	Reserved [30:28]			SSEL [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SSEL	Selects one of the four incoming/outgoing SPI slave select signals: - 0: Slave 0, SSEL[0]. - 1: Slave 1, SSEL[1]. - 2: Slave 2, SSEL[2]. - 3: Slave 3, SSEL[3]. SCB block should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

18.1.51 SCB2_SPI_CTRL (continued)

		0x0: SPI_MOTOROLA : SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive. **0x1: SPI_TI :** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS :** SPI National Semiconductors submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loop-back mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
14	SSEL_INTER_-FRAME_DEL	Indicates the SPI SELECT inter-dataframe delay (between SELECT deactivation and SELECT activation). '0': 1.5 SPI clock cycles '1': 2.5 SPI clock cycles Only applies in SPI MOTOROLA submode and when SPI_CTRL.SSEL_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
13	SSEL_HOLD_DEL	Indicates the SPI SELECT hold delay (between SPI clock edge to sample the last MOSI bit, and SELECT deactivation). '0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
12	SSEL_SETUP_DEL	Indicates the SPI SELECT setup delay (between SELECT activation and SCLK clock edge to sample the first MOSI bit). '0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. Default Value: 0

18.1.51 SCB2_SPI_CTRL (continued)

8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0
4	LATE_SAMPLE	Changes the SCLK edge on which MISO is captured in master mode, or MOSI is captured in slave mode. When '0', the default applies, for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK(CPOL is '0' and CPHA is '1'), for National Semiconductors on the rising edge of SCLK(CPOL is '0' and CPHA is '0'). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). for master, applicable to all Motorola, TI and National Semiconductors flavors, and CPOL/CPHA timing mdoes. for slave, applicable to Motorola flavor only, and CPHA=0 timing modes only, and internally-clocked mode only. Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 1
3	CPOL	Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is '0': SCLK is '0' when not transmitting data. - CPOL is '1': SCLK is '1' when not transmitting data. Default Value: 0
2	CPHA	Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is '0', CPHA is '0': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is '0', CPHA is '1': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is '1', CPHA is '0': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is '1', CPHA is '1': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. In SPI Motorola submode, all four CPOL/CPHA modes are valid. in SPI NS submode, only CPOL=0 CPHA=0 mode is valid. in SPI TI submode, only CPOL=0 CPHA=1 mode is valid. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0

18.1.51 SCB2_SPI_CTRL (continued)

0	SSEL_CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily separated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always separated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection. Default Value: 0

18.1.52 SCB2_SPI_STATUS

Description: SPI status

Address: 0x429A0024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

18.1.53 SCB2_UART_CTRL

Description: UART control

Address: 0x429A0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD :** Standard UART submode. **0x1: UART_SMARTCARD :** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA :** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

18.1.54 SCB2_UART_TX_CTRL

Description: UART transmitter control

Address: 0x429A0044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	Reserved	RW		
HW Access	Reserved		R	R	Reserved	R		
Name	Reserved [7:6]		PARITY_ENABLED	PARITY	Reserved	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

18.1.55 SCB2_UART_RX_CTRL

Description: UART receiver control

Address: 0x429A0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	Reserved	RW		
HW Access	Reserved	R	R	R	Reserved	R		
Name	Reserved	POLARITY	PARITY_ENABLED	PARITY	Reserved	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW	RW	Reserved	RW	RW	RW
HW Access	Reserved		R	R	Reserved	R	R	R
Name	Reserved [15:14]		SKIP_START	LIN_MODE	Reserved	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [31:25]							BREAK_LEVEL

Bits	Name	Description
24	BREAK_LEVEL	0: low level pulse detection, like Break field in LIN protocol 1: high level pulse detection, like IFS field in CXPI protocol, or idle line state in UART Default Value: 0
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

18.1.55 SCB2_UART_RX_CTRL (continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minimum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame separates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behavior when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behavior when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of half bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle time between data frames and the data frame value. Default Value: 2

18.1.56 SCB2_UART_RX_STATUS

Description: UART receiver status

Address: 0x429A004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of SCB clock periods that constitute the transmission of a 0x55 data frame (sent least significant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of SCB clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

18.1.57 SCB2_UART_FLOW_CTRL

Description: UART flow control

Address: 0x429A0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0
16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is effectively disabled (may be useful for debug purposes). Default Value: 0

18.1.58 SCB2_I2C_STATUS

Description: I2C status

Address: 0x429A0064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R	R	Reserved	R	Reserved	R
HW Access	Reserved		W	W	Reserved	W	Reserved	W
Name	Reserved [7:6]		M_READ	S_READ	Reserved	I2CS_IC_BUSY	Reserved	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
2	I2CS_IC_BUSY	Indicates whether the internally clocked slave logic is being accessed by external I2C master. --set at ADDR_MATCH --clear at START/RESET, STOP detection, or BUS_ERROR This bit can be used by SW to determine whether I2CS_IC is busy before entering DeepSleep. Default Value: 0

18.1.58 SCB2_I2C_STATUS (continued)

0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

18.1.59 SCB2_INTR_CAUSE

Description: Active clocked interrupt signal

Address: 0x429A0E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [7:4]				RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

18.1.60 SCB2_INTR_M

Description: Master interrupt request

Address: 0x429A0F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	Reserved	RW1C	RW1C	RW1C
HW Access	Reserved			RW1S	Reserved	RW1S	RW1S	RW1S
Name	Reserved [7:5]			I2C_STOP	Reserved	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW1C	RW1C
HW Access	Reserved						RW1S	RW1S
Name	Reserved [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent, the transmit FIFO is empty (both TX FIFO and transmit shifter register are empty), and SPI select output pin is de-selected. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. The Firmware should clear the TX FIFO, to re-do this transfer. Default Value: 0

18.1.61 SCB2_INTR_M_SET

Description: Master interrupt set request

Address: 0x429A0F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1S	Reserved	RW1S	RW1S	RW1S
HW Access	Reserved			A	Reserved	A	A	A
Name	Reserved [7:5]			I2C_STOP	Reserved	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW1S	RW1S
HW Access	Reserved						A	A
Name	Reserved [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.62 SCB2_INTR_M_MASK

Description: Master interrupt mask

Address: 0x429A0F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved	RW	RW	RW
HW Access	Reserved			R	Reserved	R	R	R
Name	Reserved [7:5]			I2C_STOP	Reserved	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.63 SCB2_INTR_M_MASKED

Description: Master interrupt masked request

Address: 0x429A0F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R	Reserved	R	R	R
HW Access	Reserved			W	Reserved	W	W	W
Name	Reserved [7:5]			I2C_STOP	Reserved	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

18.1.64 SCB2_INTR_TX

Description: Transmitter interrupt request

Address: 0x429A0F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW1C	RW1C	RW1C	Reserved		RW1C	RW1C
HW Access	Reserved	RW1S	RW1S	RW1S	Reserved		RW1S	RW1S
Name	Reserved	UNDER-FLOW	OVER-FLOW	EMPTY	Reserved [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW1C	RW1C	RW1C
HW Access	Reserved					RW1S	RW1S	RW1S
Name	Reserved [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NAC K

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is useful when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO, and the last stop field is transmitted (both TX FIFO and transmit shifter register are empty). Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty) Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0

18.1.64 SCB2_INTR_TX (continued)

4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is "0": # entries != FF_DATA_NR. MEM_WIDTH is "1": # entries != FF_DATA_NR/2. MEM_WIDTH is "2": # entries != FF_DATA_NR/4. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

18.1.65 SCB2_INTR_TX_SET

Description: Transmitter interrupt set request

Address: 0x429A0F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW1S	RW1S	RW1S	Reserved		RW1S	RW1S
HW Access	Reserved	A	A	A	Reserved		A	A
Name	Reserved	UNDER-FLOW	OVER-FLOW	EMPTY	Reserved [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW1S	RW1S	RW1S
HW Access	Reserved					A	A	A
Name	Reserved [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.66 SCB2_INTR_TX_MASK

Description: Transmitter interrupt mask

Address: 0x429A0F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	Reserved		RW	RW
HW Access	Reserved	R	R	R	Reserved		R	R
Name	Reserved	UNDER-FLOW	OVER-FLOW	EMPTY	Reserved [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.67 SCB2_INTR_TX_MASKED

Description: Transmitter interrupt masked request

Address: 0x429A0F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	Reserved		R	R
HW Access	Reserved	W	W	W	Reserved		W	W
Name	Reserved	UNDER-FLOW	OVER-FLOW	EMPTY	Reserved [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					R	R	R
HW Access	Reserved					W	W	W
Name	Reserved [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

18.1.68 SCB2_INTR_RX

Description: Receiver interrupt request

Address: 0x429A0FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW1C	RW1C	Reserved	RW1C	RW1C	Reserved	RW1C
HW Access	Reserved	RW1S	RW1S	Reserved	RW1S	RW1S	Reserved	RW1S
Name	Reserved	UNDER-FLOW	OVER-FLOW	Reserved	FULL	NOT_EMP-TY	Reserved	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW1C	RW1C	RW1C	RW1C
HW Access	Reserved				RW1S	RW1S	RW1S	RW1S
Name	Reserved [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STA-TUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guaran-tee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0

18.1.68 SCB2_INTR_RX (continued)

8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_-FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is "0": # entries == FF_DATA_NR. MEM_WIDTH is "1": # entries == FF_DATA_NR/2. MEM_WIDTH is "2": # entries == FF_DATA_NR/4. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by RX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

18.1.69 SCB2_INTR_RX_SET

Description: Receiver interrupt set request

Address: 0x429A0FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW1S	RW1S	Reserved	RW1S	RW1S	Reserved	RW1S
HW Access	Reserved	A	A	Reserved	A	A	Reserved	A
Name	Reserved	UNDER-FLOW	OVER-FLOW	Reserved	FULL	NOT_EMP-TY	Reserved	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW1S	RW1S	RW1S	RW1S
HW Access	Reserved				A	A	A	A
Name	Reserved [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.70 SCB2_INTR_RX_MASK

Description: Receiver interrupt mask

Address: 0x429A0FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	Reserved	RW	RW	Reserved	RW
HW Access	Reserved	R	R	Reserved	R	R	Reserved	R
Name	Reserved	UNDER-FLOW	OVER-FLOW	Reserved	FULL	NOT_EMP-TY	Reserved	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.71 SCB2_INTR_RX_MASKED

Description: Receiver interrupt masked request

Address: 0x429A0FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	Reserved	R	R	Reserved	R
HW Access	Reserved	W	W	Reserved	W	W	Reserved	W
Name	Reserved	UNDER-FLOW	OVER-FLOW	Reserved	FULL	NOT_EMP-TY	Reserved	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

19 Improved Inter-Integrated circuit (I3C) registers

This section discusses the I3C registers. It lists all the registers in mapping tables, in address order.

19.1 Register details

Register name	Address	Description
I3C_CORE_DEVICE_CTRL	0x42A50000	Device Control Register
I3C_CORE_DEVICE_ADDR	0x42A50004	Device Address Register
I3C_CORE_COMMAND_QUEUE_PORT	0x42A5000C	COMMAND_QUEUE_PORT
I3C_CORE_RESPONSE_QUEUE_PORT	0x42A50010	RESPONSE_QUEUE_PORT
I3C_CORE_TX_RX_DATA_PORT	0x42A50014	Transmit/Receive Data Port Register
I3C_CORE_IBI_QUEUE_DATA	0x42A50018	In-Band Interrupt Queue Data Register
I3C_CORE_QUEUE_THLD_CTRL	0x42A5001C	Queue Threshold Control Register
I3C_CORE_DATA_BUFFER_THLD_CTRL	0x42A50020	Data Buffer Threshold Control Register
I3C_CORE_IBI_QUEUE_CTRL	0x42A50024	IBI Queue Control Register
I3C_CORE_RESET_CTRL	0x42A50034	Reset Control Register
I3C_CORE_TGT_EVENT_STATUS	0x42A50038	Target Event Status Register
I3C_CORE_INTR_STATUS	0x42A5003C	Reset Control Register
I3C_CORE_INTR_STATUS_EN	0x42A50040	Interrupt Status Enable Register.
I3C_CORE_INTR_SIGNAL_EN	0x42A50044	Interrupt Signal Enable Register
I3C_CORE_INTR_FORCE	0x42A50048	Interrupt Force Enable Register
I3C_CORE_QUEUE_STATUS_LEVEL	0x42A5004C	Queue Status Level Register.
I3C_CORE_DATA_BUFFER_STATUS_LEVEL	0x42A50050	Data Buffer Status Level Register.
I3C_CORE_PRESENT_STATE	0x42A50054	Present State Register
I3C_CORE_CCC_DEVICE_STATUS	0x42A50058	Device Operating Status Register.
I3C_CORE_DEVICE_ADDR_TABLE_POINTER	0x42A5005C	Pointer for Device Address Table
I3C_CORE_DEV_CHAR_TABLE_POINTER	0x42A50060	Pointer for Device Characteristics Table
I3C_CORE_VENDOR_SPECIFIC_REG_POINTER	0x42A5006C	Pointer for Vendor Specific Registers.
I3C_CORE_TGT_MIPI_ID_VALUE	0x42A50070	I3C MIPI Manufacturer ID Register
I3C_CORE_TGT_PID_VALUE	0x42A50074	I3C Normal Provisional ID Register
I3C_CORE_TGT_CHAR_CTRL	0x42A50078	I3C Target Characteristic Register.
I3C_CORE_TGT_MAX_LEN	0x42A5007C	I3C Max Write/Read Length Register.
I3C_CORE_MAX_READ_TURNAROUND	0x42A50080	MXDS Maximum Read Turnaround Time.
I3C_CORE_MAX_DATA_SPEED	0x42A50084	Maximum Data Speed Register
I3C_CORE_TGT_INTR_REQ	0x42A5008C	Target Interrupt Request Register
I3C_CORE_TGT_TIR_DATA	0x42A50094	Target Interrupt Request Data Register
I3C_CORE_TGT_IBI_RESP	0x42A50098	Target IBI Response Register
I3C_CORE_DEVICE_CTRL_EXTENDED	0x42A500B0	Device Control Extended Register
I3C_CORE_SCL_I3C_OD_TIMING	0x42A500B4	SCL I3C Open Drain Timing Register

Improved Inter-Integrated circuit (I3C) registers

Register name	Address	Description
I3C_CORE_SCL_I3C_PP_TIMING	0x42A500B8	SCL I3C Push Pull Timing Register
I3C_CORE_SCL_I2C_FM_TIMING	0x42A500BC	SCL I2C Fast Mode Timing Register
I3C_CORE_SCL_I2C_FMP_TIMING	0x42A500C0	SCL I2C Fast Mode Plus Timing Register
I3C_CORE_SCL_EXT_LCNT_TIMING	0x42A500C8	SCL Extended Low Count Timing Register.
I3C_CORE_SCL_EXT_TERMN_LCNT_TIMING	0x42A500CC	SCL Termination Bit Low Count Timing Register
I3C_CORE_SDA_HOLD_SWITCH_DLY_TIMING	0x42A500D0	SDA Hold and Mode Switch Delay Timing Register
I3C_CORE_BUS_FREE_AVAIL_TIMING	0x42A500D4	Bus Free and Available Timing Register
I3C_CORE_BUS_IDLE_TIMING	0x42A500D8	Bus Idle Timing Register
I3C_CORE_SCL_LOW_CTR_EXT_TIMEOUT	0x42A500DC	SCL LOW Controller Timeout
I3C_CORE_RELEASE_SDA_TIMING	0x42A500EC	Release SDA count value.
I3C_CORE_EXT_TX_DATA_PORT_0	0x42A50130	DWC_mipi_i3c Directed read Vendor-specific CCC 0 TX Data Port Register
I3C_CORE_EXT_TX_DATA_PORT_1	0x42A50134	DWC_mipi_i3c Directed read Vendor-specific CCC 1 TX Data Port Register
I3C_CORE_EXT_TX_DATA_PORT_2	0x42A50138	DWC_mipi_i3c Directed read Vendor-specific CCC 2 TX Data Port Register
I3C_CORE_EXT_TX_DATA_PORT_3	0x42A5013C	DWC_mipi_i3c Directed read Vendor-specific CCC 3 TX Data Port Register
I3C_CORE_EXT_0_1_DATA_BUF_STS_LEVEL	0x42A50154	Vendor-specific CCC types 0 and 1 Data Buffer Status Level Register
I3C_CORE_EXT_2_3_DATA_BUF_STS_LEVEL	0x42A50158	Vendor-specific CCC types 2 and 3 Data Buffer Status Level Register
I3C_CORE_EXT_CMD_REG_0	0x42A50164	TID, CCC type value and Defining Byte of Vendor-specific CCC 0 Register
I3C_CORE_EXT_CMD_REG_1	0x42A50168	TID, CCC type value and Defining Byte of Vendor-specific CCC 1 Register
I3C_CORE_EXT_CMD_REG_2	0x42A5016C	TID, CCC type value and Defining Byte of Vendor-specific CCC 2 Register
I3C_CORE_EXT_CMD_REG_3	0x42A50170	TID, CCC type value and Defining Byte of Vendor-specific CCC 3 Register
I3C_CORE_EXT_TX_QUEUE_RESET_CTRL	0x42A50184	Individual Vendor CCC buffer reset.
I3C_CORE_DEV_CHAR_TABLE1_LOC1	0x42A50200	Device Characteristic Table Location-1 of Device1, MSB_PROVISIONAL_ID
I3C_CORE_DEV_CHAR_TABLE1_LOC2	0x42A50204	Device Characteristic Table Location-2 of Device1, LSB_PROVISIONAL_ID
I3C_CORE_DEV_CHAR_TABLE1_LOC3	0x42A50208	Device Characteristic Table Location-3 of Device1, BCR, DCR
I3C_CORE_DEV_CHAR_TABLE1_LOC4	0x42A5020C	Device Characteristic Table Location-4 of Device1, DEV_DYNAMIC_ADDR

Improved Inter-Integrated circuit (I3C) registers

Register name	Address	Description
I3C_CORE_DEV_CHAR_TABLE2_LOC1	0x42A50210	Device Characteristic Table Location-1 of Device2
I3C_CORE_DEV_CHAR_TABLE2_LOC2	0x42A50214	Device Characteristic Table Location-2 of Device2
I3C_CORE_DEV_CHAR_TABLE2_LOC3	0x42A50218	Device Characteristic Table Location-3 of Device2
I3C_CORE_DEV_CHAR_TABLE2_LOC4	0x42A5021C	Device Characteristic Table Location-4 of Device2
I3C_CORE_DEV_CHAR_TABLE3_LOC1	0x42A50220	Device Characteristic Table Location-1 of Device3
I3C_CORE_DEV_CHAR_TABLE3_LOC2	0x42A50224	Device Characteristic Table Location-2 of Device3
I3C_CORE_DEV_CHAR_TABLE3_LOC3	0x42A50228	Device Characteristic Table Location-3 of Device3
I3C_CORE_DEV_CHAR_TABLE3_LOC4	0x42A5022C	Device Characteristic Table Location-4 of Device3
I3C_CORE_DEV_CHAR_TABLE4_LOC1	0x42A50230	Device Characteristic Table Location-1 of Device4
I3C_CORE_DEV_CHAR_TABLE4_LOC2	0x42A50234	Device Characteristic Table Location-2 of Device4
I3C_CORE_DEV_CHAR_TABLE4_LOC3	0x42A50238	Device Characteristic Table Location-3 of Device4
I3C_CORE_DEV_CHAR_TABLE4_LOC4	0x42A5023C	Device Characteristic Table Location-4 of Device4
I3C_CORE_DEV_CHAR_TABLE5_LOC1	0x42A50240	Device Characteristic Table Location-1 of Device5
I3C_CORE_DEV_CHAR_TABLE5_LOC2	0x42A50244	Device Characteristic Table Location-4 of Device10
I3C_CORE_DEV_CHAR_TABLE5_LOC3	0x42A50248	Device Characteristic Table Location-3 of Device5
I3C_CORE_DEV_CHAR_TABLE5_LOC4	0x42A5024C	Device Characteristic Table Location-4 of Device5
I3C_CORE_DEV_CHAR_TABLE6_LOC1	0x42A50250	Device Characteristic Table Location-1 of Device6
I3C_CORE_DEV_CHAR_TABLE6_LOC2	0x42A50254	Device Characteristic Table Location-2 of Device6
I3C_CORE_DEV_CHAR_TABLE6_LOC3	0x42A50258	Device Characteristic Table Location-3 of Device6
I3C_CORE_DEV_CHAR_TABLE6_LOC4	0x42A5025C	Device Characteristic Table Location-4 of Device6
I3C_CORE_DEV_CHAR_TABLE7_LOC1	0x42A50260	Device Address Table of Device3
I3C_CORE_DEV_CHAR_TABLE7_LOC2	0x42A50264	Device Characteristic Table Location-2 of Device7

Improved Inter-Integrated circuit (I3C) registers

Register name	Address	Description
I3C_CORE_DEV_CHAR_TABLE7_LOC3	0x42A50268	Device Characteristic Table Location-3 of Device7
I3C_CORE_DEV_CHAR_TABLE7_LOC4	0x42A5026C	Device Characteristic Table Location-4 of Device7
I3C_CORE_DEV_CHAR_TABLE8_LOC1	0x42A50270	Device Characteristic Table Location-1 of Device8
I3C_CORE_DEV_CHAR_TABLE8_LOC2	0x42A50274	Device Characteristic Table Location-2 of Device8
I3C_CORE_DEV_CHAR_TABLE8_LOC3	0x42A50278	Device Characteristic Table Location-3 of Device8
I3C_CORE_DEV_CHAR_TABLE8_LOC4	0x42A5027C	Device Address Table of Device10
I3C_CORE_DEV_CHAR_TABLE9_LOC1	0x42A50280	Device Characteristic Table Location-1 of Device9
I3C_CORE_DEV_CHAR_TABLE9_LOC2	0x42A50284	Device Characteristic Table Location-2 of Device9
I3C_CORE_DEV_CHAR_TABLE9_LOC3	0x42A50288	Device Characteristic Table Location-3 of Device9
I3C_CORE_DEV_CHAR_TABLE9_LOC4	0x42A5028C	Device Characteristic Table Location-4 of Device9
I3C_CORE_DEV_CHAR_TABLE10_LOC1	0x42A50290	Device Characteristic Table Location-1 of Device10
I3C_CORE_DEV_CHAR_TABLE10_LOC2	0x42A50294	Device Characteristic Table Location-2 of Device10
I3C_CORE_DEV_CHAR_TABLE10_LOC3	0x42A50298	Device Characteristic Table Location-3 of Device10
I3C_CORE_DEV_CHAR_TABLE10_LOC4	0x42A5029C	Device Characteristic Table Location-4 of Device10
I3C_CORE_DEV_CHAR_TABLE11_LOC1	0x42A502A0	Device Characteristic Table Location-1 of Device11
I3C_CORE_DEV_CHAR_TABLE11_LOC2	0x42A502A4	0
I3C_CORE_DEV_CHAR_TABLE11_LOC3	0x42A502A8	Device Characteristic Table Location-3 of Device11
I3C_CORE_DEV_CHAR_TABLE11_LOC4	0x42A502AC	Device Characteristic Table Location-4 of Device11
I3C_CORE_DEV_ADDR_TABLE_LOC1	0x42A502C0	Device Address Table of Device1
I3C_CORE_DEV_ADDR_TABLE_LOC2	0x42A502C4	Device Address Table of Device2
I3C_CORE_DEV_ADDR_TABLE_LOC3	0x42A502C8	Device Address Table of Device3
I3C_CORE_DEV_ADDR_TABLE_LOC4	0x42A502CC	Device Address Table of Device4
I3C_CORE_DEV_ADDR_TABLE_LOC5	0x42A502D0	Device Address Table of Device5
I3C_CORE_DEV_ADDR_TABLE_LOC6	0x42A502D4	Device Address Table of Device6
I3C_CORE_DEV_ADDR_TABLE_LOC7	0x42A502D8	Device Address Table of Device7
I3C_CORE_DEV_ADDR_TABLE_LOC8	0x42A502DC	Device Address Table of Device8

Improved Inter-Integrated circuit (I3C) registers

Register name	Address	Description
I3C_CORE_DEV_ADDR_TABLE_LOC9	0x42A502E0	Device Address Table of Device9
I3C_CORE_DEV_ADDR_TABLE_LOC10	0x42A502E4	Device Address Table of Device10
I3C_CORE_DEV_ADDR_TABLE_LOC11	0x42A502E8	Device Address Table of Device11
I3C_CTRL	0x42A50400	I3C Block Control
I3C_TGT_STATUS	0x42A50418	This register provides additional status information when functioning as a Target.
I3C_CCC_GETSTATUS	0x42A50424	This register provides additional information on GETSTATUS CCCs received when functioning as a Target.
I3C_TIMING_CNT_CTRL	0x42A5042C	Controls the Counter used for timestamping I3C-relevant events, especially when communicating with Asynchronous Timing Control Mode 0 enabled.
I3C_TIMING_CNT0	0x42A50430	Most Significant Bits of the Counter
I3C_TIMING_CNT1	0x42A50434	Least Significant Bits of the Counter

19.1.1 I3C_CORE_DEVICE_CTRL

Description: Device Control Register

Address: 0x42A50000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved						RW
HW Access	R	Reserved						R
Name	I2C_TARGET_PRESENT	Reserved [6:1]						IBA_INCLUDE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							HOT_JOIN_CTRL

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	Reserved	RW	RW	RW	
HW Access	RW	R	R	Reserved	R	R	R	
Name	ENABLE	RESUME	ABORT	Reserved	ADAPTIVE_I2C_I3C	TARGET_PEC_EN	IDLE_CNT_MULTPLIER [25:24]	

Bits	Name	Description
31	ENABLE	I3C Enable Controls whether or not I3C functionality is enabled. When functioning as the Active Controller, software can write to this register to request to disable the I3C block. However, the block may not get disabled immediately and is 'Disabled' after commands in the Command queue (if any) are executed leading to a STOP condition on the bus and Controller FSM is in IDLE state (as indicated by PRESENT_STATE Register). When functioning as a Target, software can write to this register to request to disable the I3C block. However, the disable happens after the ongoing transfer is completed on the I3C bus. Software can read back 1'b0 from this field once disabling of I3C is completed. After power on reset, the software can enable I3C Secondary Controller or Target functionality by programming this bit to 1'b1. However the I3C bus interface of the block will respond to transfer on the bus, only after it observes Bus Available condition for BUS_AVAILABLE_TIME*IDLE_CNT_MULTPLIER counts of pclk period. The successful completion of Enable/Disable of the block depends on availability of SCL to the controller at the time of performing this operation, and hence may not happen instantly. Values: 0x0: Disables the I3C controller. 0x1: Enables the I3C controller. Default Value: 0x0

19.1.1 I3C_CORE_DEVICE_CTRL (continued)

30	RESUME	I3C Resume This bit is used to resume the I3C block after it goes to the Halt state. When functioning as the Active Controller, the block goes to the halt state (as indicated in PRESENT_STATE Register) due to any type of error in the transfer (the type of error is indicated by ERR_STATUS field in the RESPONSE_QUEUE_PORT register). After the block goes to the Halt state, the application has to write 1'b1 to this bit to resume. This bit is auto-cleared once the block resumes the transfers by initiating the next command. When functioning as a Target, the block goes to the halt state due to following conditions: 1 => Any type of error in the transfer (the type of error is indicated by ERR_STATUS field in the RESPONSE_QUEUE_PORT register) 2 => MRL Register updated by the Active Controller through SETMRL CCC. After the device has gone to halt state, the application has to take necessary action to handle the error condition and then write 1'b1 to this bit to resume the controller. This bit is auto-cleared once the controller is ready to accept new transfers. Default Value: 0x0
29	ABORT	I3C Abort. This bit is only valid when this I3C Device is functioning as the Active Controller. This bit allows this device to relinquish the I3C Bus before completing the issued transfer. In response to an ABORT request, the Controller issues the STOP condition after the complete data byte is transferred or received. This bit is auto-cleared once the transfer is aborted and the controller issues a 'Transfer Abort' interrupt. Default Value: 0x0
27	ADAPTIVE_I2C_I3C	Hot-Join Control for Adaptive I2C/I3C Mode This bit is only valid when this I3C Device is functioning as a Target. In Adaptive Mode, this bit is used to enable some features of this target device. This bit is cleared automatically if the controller determines the mode as I3C. Values: 0x0: The device initiates a Hot-Join without determining the bus mode and assuming itself to be on I3C bus. 0x1: The device initiates a Hot-Join request only after it has switched to I3C mode of operation. Default Value: 0x0
26	TARGET_PEC_EN	Target Parity Error Check (PEC) Enable This bit is only valid when this I3C Device is functioning as a Target. Values: 0x0: PEC is disabled 0x1: PEC is enabled Default Value: 0x0
25 : 24	IDLE_CNT_MULTPLIER	Idle count multiplier. This bit is only valid when this I3C Device is functioning as a Target. After power-on reset, this Target is enabled only after it sees both SDA and SCL lines idle for a specified time. This idle time is calculated by multipliying IDLE_CNT_MULTPLIER with BUS_AVAILABLE_TIME field in the BUS_FREE_AVAIL_TIMING register. Values: 0x00: BUS_AVAILABLE_TIME * 1 0x01: BUS_AVAILABLE_TIME * 2 0x10: BUS_AVAILABLE_TIME * 4 0x11: BUS_AVAILABLE_TIME * 8 Default Value: 0x0
8	HOT_JOIN_CTRL	Hot-Join ACK/NACK Control This bit is only valid when this I3C Device is functioning as the Active Controller. This bit acts as a global control to ACK/NACK the Hot-Join request from the devices. The Active Controller ACK/NACKs the Hot-Join request from other devices connected on the I3C Bus, based on programming of this bit. Values: 0x0: ACK the Hot-Join request. 0x1: NACK and send broadcast CCC(auto-disable) to disable Hot-join. Default Value: 0x0
7	I2C_TARGET_PRESENT	Default Value: 0x0

19.1.1 I3C_CORE_DEVICE_CTRL (continued)

0	IBA_INCLUDE	I3C Broadcast Address Include. This bit is only valid when this I3C Device is functioning as the Active Controller. This bit is used to include the I3C broadcast address (0x7E) in private transfers. Note: If the I3C broadcast address is not included in private transfers, In-band Interrupts (IBI) driven from Targets might not win address arbitration and IBIs will get delayed. Values: 0x0: I3C Broadcast Address is not included in Private Transfers 0x1: I3C Broadcast Address is included in Private Transfers Default Value: 0x0

19.1.2 I3C_CORE_DEVICE_ADDR

Description: Device Address Register

Address: 0x42A50004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	STAT-IC_AD-DR_VALID	Reserved [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DYNAMIC_ADDR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	DYNAM-IC_AD-DR_VALID	Reserved [30:24]						

Bits	Name	Description
31	DYNAMIC_ADDR_VALID	Dynamic Address Valid This bit is used to control whether the DYNAMIC_ADDR is valid or not. =>When functioning as the Primary Controller, the user/application must set this bit to 1 along with the DYNAMIC_ADDR. =>When functioning as a Target, the block sets this bit to 1 when the Active Controller assigns the Dynamic address during ENTDAA or SETDASA mechanism. + Values: 0x0: Dynamic Address is invalid 0x1: Dynamic Address is valid Default Value: 0x0
22 : 16	DYNAMIC_ADDR	Device Dynamic Address. This field is used to program the Device Dynamic Address. The block uses this address for I3C transfers. => When functioning as the Primary Controller, the user/application must program the Dynamic Address. => When functioning as a Target, the Active Controller assigns this address during ENTDAA or SETDASA procedures. Default Value: 0x0

19.1.2 I3C_CORE_DEVICE_ADDR (continued)

15	STATIC_ADDR_VALID	Static Address Valid. This field is only valid when this I3C Device is functioning as a Target. Values: 0x0: Static Address in STATIC_ADDR field is invalid 0x1: Static Address in STATIC_ADDR field is valid Default Value: 0x0
6 : 0	STATIC_ADDR	Device Static Address. This field is only valid when this I3C Device is functioning as a Target. The device uses this address to respond to SETDASA CCC Command to get the Dynamic Address if static address is valid (STATIC_ADDRESS_VALID must be set to 1). Default Value: 0x0

19.1.3 I3C_CORE_COMMAND_QUEUE_PORT

Description: COMMAND_QUEUE_PORT

Address: 0x42A5000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	RW							
Name	COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	RW							
Name	COMMAND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	RW							
Name	COMMAND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	RW							
Name	COMMAND [31:24]							

Bits	Name	Description
31 : 0	COMMAND	32-bit Command Default Value: Undefined

19.1.4 I3C_CORE_RESPONSE_QUEUE_PORT

Description: RESPONSE_QUEUE_PORT

Address: 0x42A50010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESPONSE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESPONSE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RESPONSE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	RESPONSE [31:24]							

Bits	Name	Description
31 : 0	RESPONSE	32-bit Response Default Value: 0x0

19.1.5 I3C_CORE_TX_RX_DATA_PORT

Description: Transmit/Receive Data Port Register

Address: 0x42A50014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_RX_DATA_PORT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TX_RX_DATA_PORT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	TX_RX_DATA_PORT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	TX_RX_DATA_PORT [31:24]							

Bits	Name	Description
31 : 0	TX_RX_DATA_PORT	Transmit Data Port for write access and Receive Data Port for read access. This field is mapped to the TX Data Buffer when writing and to the RX Data Buffer when reading. The data is always packed in 4-byte aligned data words. If the command length is not aligned to the 4-bytes, then the additional data bytes have to be ignored. Default Value: 0x0

19.1.6 I3C_CORE_IBI_QUEUE_DATA

Description: In-Band Interrupt Queue Data Register

Address: 0x42A50018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IBI_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	IBI_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	IBI_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	IBI_DATA [31:24]							

Bits	Name	Description
31 : 0	IBI_DATA	In-Band Interrupt Data This register is mapped to the IBI Queue. The IBI Data is always packed in 4-byte aligned and put to the IBI Queue. If the incoming data is not aligned to the 4-bytes, then there are unused bytes in the end location of the IBI transfer. Default Value: 0x0

19.1.7 I3C_CORE_QUEUE_THLD_CTRL

Description: Queue Threshold Control Register

Address: 0x42A5001C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMD_EMPTY_BUF_THLD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RESP_BUF_THLD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	IBI_DATA_THLD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	IBI_STATUS_THLD [31:24]							

Bits	Name	Description
31 : 24	IBI_STATUS_THLD	In-Band Interrupt Status Threshold Value. This field controls the number of IBI status entries (or greater) in the IBI queue that trigger the IBI_THLD_STAT interrupt. Every In Band Interrupt received (with or without Payload) by the block generates an IBI status. The application should program only valid values. NOTE: The valid value is only 0 if IBI with payload is selected in the configuration. Values: 0x0 <= N < 16: Interrupt will trigger when queue has N+1 valid entries. Default Value: 0x1
23 : 16	IBI_DATA_THLD	IBI Data Buffer Threshold Value This field represents the IBI data segment size in Dwords (4 bytes). The IBI_DATA_THLD field enables the slicing of the incoming IBI data and generate individual status and thereby promotes the cut-through operation in reading out the IBI data. Values: 0x1 <= N < IC_IBI_DATA_BUF_DEPTH Default Value: 0x1
15 : 8	RESP_BUF_THLD	Response Buffer Threshold Value. Controls the minimum number of valid entries in the Response Queue that trigger the RESP_READY_STAT_INTR interrupt. The application should programs only valid values. Values: 0x0 <= N < 8: Interrupt will trigger when queue has N+1 valid entries. Default Value: 0x1

19.1.7 I3C_CORE_QUEUE_THLD_CTRL (continued)

7 : 0	CMD_EMPTY_BUF_THLD	Command Buffer Empty Threshold Value Controls the minimum number of empty locations in the Command Queue that trigger the CMD_QUEUE_READY_STAT interrupt. The application should programs only valid values. Values: 0x0: Interrupt will trigger when the queue is completely empty 0x0 < N < 16: Interrupt will trigger when queue has N empty locations. Default Value: 0x1

19.1.8 I3C_CORE_DATA_BUFFER_THLD_CTRL

Description: Data Buffer Threshold Control Register

Address: 0x42A50020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					TX_EMPTY_BUF_THLD [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [15:11]					RX_BUF_THLD [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					TX_START_THLD [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					RX_START_THLD [26:24]		

Bits	Name	Description
26 : 24	RX_START_THLD	Receive Start Threshold Value. When functioning as the Active Controller, when the controller is set up to initiate a read transfer, it waits until either one of the conditions are met before it initiates the read transfer on the I3C Interface. => Data length (as specified in the command) number of locations are empty in the Receive FIFO. => Threshold number of locations (or more) are empty in the Receive FIFO. When functioning as a Target, the block ACKs a write request from the Active Controller only if threshold number of empty locations(or more) are available in its receive buffer. The supported values for RX_START_THLD are: 0x0: Threshold of at least 1 empty entry 0x1: Threshold of at least 4 empty entries 0x2: Threshold of at least 8 empty entries 0x3: Threshold of at least 16 empty entries 0x4: Threshold of at least 32 empty entries 0x5: Threshold of at least 64 empty entries Default Value: 0x1

19.1.8 I3C_CORE_DATA_BUFFER_THLD_CTRL (continued)

18 : 16	TX_START_THLD	Transfer Start Threshold Value. When functioning as the Active Controller, when the Controller is set up to initiate a write transfer, it waits until either one of the following conditions are met before it initiates the write transfer on the I3C Interface. => Data length (as specified in the command) number of locations are filled in the TX FIFO. => Threshold number of entries (or more) are available in the TX FIFO When functioning as a Target, the Target ACKs a read request from the Active Controller only if either one of the following conditions are met. => Data length (as specified in the command) number of locations are filled in the Transmit FIFO => Threshold number of entries (or more) are available in the Transmit FIFO Supported values: 0x0: Threshold of at least 1 valid entry 0x1: Threshold of at least 4 valid entries 0x2: Threshold of at least 8 valid entries 0x3: Threshold of at least 16 valid entries 0x4: Threshold of at least 32 valid entries 0x5: Threshold of at least 64 valid entries Default Value: 0x1
10 : 8	RX_BUF_THLD	Receive Buffer Threshold Value. This field controls the number of valid entries (or above) in the RX FIFO that trigger the RX_THLD_STAT interrupt. If the programmed value is greater than the buffer depth, then threshold is set to IC_RX_BUF_DEPTH. Supported values: 0x0: Interrupt triggers with at least 1 valid entry 0x1: Interrupt triggers with at least 4 valid entries 0x2: Interrupt triggers with at least 8 valid entries 0x3: Interrupt triggers with at least 16 valid entries 0x4: Interrupt triggers with at least 32 valid entries 0x5: Interrupt triggers with at least 64 valid entries Default Value: 0x1
2 : 0	TX_EMPTY_BUF_THLD	Transmit Buffer Empty Threshold Value This field controls the number of empty locations (or above) in the TX FIFO that trigger the TX_THLD_STAT interrupt. If the programmed value is greater than the buffer depth, then threshold is set to IC_TX_BUF_DEPTH. Supported values: 0x0: Interrupt triggers with at least 1 empty entry 0x1: Interrupt triggers with at least 4 empty entries 0x2: Interrupt triggers with at least 8 empty entries 0x3: Interrupt triggers with at least 16 empty entries 0x4: Interrupt triggers with at least 32 empty entries 0x5: Interrupt triggers with at least 64 empty entries Default Value: 0x1

19.1.9 I3C_CORE_IBI_QUEUE_CTRL

Description: IBI Queue Control Register

Address: 0x42A50024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	Reserved	RW	RW
HW Access	Reserved				R	Reserved	R	R
Name	Reserved [7:4]				NOTIFY_TIR_REJECTED	Reserved	NOTIFY_CR_REJECTED	NOTIFY_HJ_REJECTED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	NOTIFY_TIR_REJECTED	Notify Rejected Target Interrupt Request Control. This bit is only valid when this I3C Device is functioning the Active Controller, and is used to suppress reporting to the application about rejected Target Interrupt Request. Values: 0x0: Disables passing the IBI Status to the IBI FIFO (hence not notifying the application) when a Target Interrupt Request is NACKed and auto-disabled based on the IBI_TIR_REQ_REJECT Register. 0x1: Enables writing the IBI Status to the IBI FIFO (hence notifying the application) when a Target Interrupt Request is NACKed and auto-disabled based on the IBI_TIR_REQ_REJECT Register. Default Value: 0x0
1	NOTIFY_CR_REJECTED	Notify Rejected Controller Role Request (CR) Control. This bit is only valid when this I3C Device is functioning the Active Controller, and is used to suppress reporting to the application about Controller Role Request (CR) rejected. Values: 0x0: Disable passing the IBI Status to the IBI FIFO (hence not notifying the application) when a CR Request is NACKed and auto-disabled based on the IBI_CR_REQ_REJECT Register. 0x1: Enable writing the IBI Status to the IBI FIFO (hence notifying the application) when a CR Request is NACKed and auto-disabled based on the IBI_CR_REQ_REJECT Register. Default Value: 0x0

19.1.9 I3C_CORE_IBI_QUEUE_CTRL (continued)

0	NOTIFY_HJ_REJECTED	Notify Rejected Hot-Join Control. This bit is only valid when this I3C Device is functioning the Active Controller, and is used to suppress reporting to the application about Hot-Join request rejected (NACK and Auto Disable). Values: 0x0: Disable passing the IBI Status to the IBI FIFO (hence not notifying the application) when a HJ Request is NACKed and auto-disabled based on the DEVICE_CTRL.HOT_JOIN_CTRL. 0x1: Enable writing the IBI Status to the IBI FIFO (hence notifying the application) when a HJ Request is NACKed and auto-disabled based on the DEVICE_CTRL.HOT_JOIN_CTRL. Default Value: 0x0

19.1.10 I3C_CORE_RESET_CTRL

Description: Reset Control Register

Address: 0x42A50034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [7:6]		IBI_-QUEUE_RST	RX_FIFO_RST	TX_FIFO_RST	RESP_-QUEUE_RST	CMD_-QUEUE_RST	SOFT_RST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			Reserved			
HW Access	RW	RW			Reserved			
Name	BUS_RESET	BUS_RESET_TYPE [30:28]			Reserved [27:24]			

Bits	Name	Description
31	BUS_RESET	Write 1'b1 to this bit to exercise Bus Reset Reset Pattern Generation based on Bus Reset Type selection. This bit is cleared automatically once the Bus Reset Pattern Generation is completed. Default Value: 0x0
30 : 28	BUS_RESET_TYPE	Type of bus reset triggered by the BUS_RESET field. Values: 0x0: Exit Pattern 0x1: Target Reset Pattern 0x6: SCL Low Pattern Others: Reserved Default Value: 0x0
5	IBI_QUEUE_RST	IBI Queue Software Reset. This bit is only valid when functioning as the Active Controller. Write 0x1 to this bit to exercise IBI Queue reset. This bit is cleared automatically once the IBI Queue reset is completed. Before the reset is completed, write accesses and read accesses to the other registers will return a bus error. Default Value: 0x0

19.1.10 I3C_CORE_RESET_CTRL (continued)

4	RX_FIFO_RST	Receive Buffer Software Reset. Write 0x1 to this bit to exercise Receive Buffer reset This bit is cleared automatically once the Receive buffer reset is completed. Before the reset is completed, write accesses and read accesses to the other registers will return a bus error. Default Value: 0x0
3	TX_FIFO_RST	Transmit Buffer Software Reset. Write 0x1 to this bit to exercise Transmit Buffer reset. This bit is cleared automatically once the Transmit Buffer reset is completed. Before the reset is completed, write accesses and read accesses to the other registers will return a bus error. Default Value: 0x0
2	RESP_QUEUE_RST	Response Queue Software Reset. Write 1'b1 to this bit to exercise Response Queue reset. This bit is cleared automatically once the Response Queue reset is completed. Before the reset is completed, write accesses and read accesses to the other registers will return a bus error. Default Value: 0x0
1	CMD_QUEUE_RST	Command Queue Software Reset. Write 0x1 to this bit to exercise Command Queue reset. This bit is cleared automatically once the Command Queue reset is completed. Before the reset is completed, write accesses and read accesses to the other registers will return a bus error. Default Value: 0x0
0	SOFT_RST	Core Software Reset. Write 0x1 to this bit to exercise software reset. This will trigger an internal procedure that resets all Buffers - RX, TX, CMD, and Response. This bit is cleared automatically once the core reset is completed. Before the reset is completed, write accesses and read accesses to the other registers will return a bus error. Default Value: 0x0

19.1.11 I3C_CORE_TGT_EVENT_STATUS

Description: Target Event Status Register

Address: 0x42A50038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	R		RW	Reserved	R	R
HW Access	RW	RW	RW		R	Reserved	R	RW
Name	MWL_UP-DATED	MRL_UP-DATED	ACTIVITY_STATE [5:4]		HJ_EN	Reserved	CR_EN	TIR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	MWL_UPDATED	MWL Updated Status. This bit indicates a SETMWL CCC is received by the Target. The updated MWL value can be read from TGT_MAX_LEN register. This status can be cleared by writing 0x1 to this field after reading the updated MWL. Default Value: 0x0
6	MRL_UPDATED	MRL Updated Status. This bit indicates a SETMRL CCC is received by the Target. The updated MRL value can be read from TGT_MAX_LEN register. This status can be cleared by writing 0x1 to this field after reading the updated MRL. Default Value: 0x0
5 : 4	ACTIVITY_STATE	Activity State Status This bit reflects the Activity State of this Target set by the Active Controller. Values: 0x0: ENTAS0 0x1: ENTAS1 0x2: ENTAS2 0x3: ENTAS3 Default Value: 0x0

19.1.11 I3C_CORE_TGT_EVENT_STATUS (continued)

3	HJ_EN	Hot-Join Interrupt Enable. This bit is only valid when this I3C Device is functioning as a Target, and reflects whether the Hot-Join Request Interrupts are allowed on the I3C bus or not. The Target application can choose to Disable HJ Capability of the Target controller (if selected) by setting this field to 0 before 'Enabling' the block. When done so, the Target will not initiate Hot Join and will take part in Address Assignment without initiating Hot Join. If this field is NOT set to 0 by the Target application, it can be set or cleared by the I3C Controller via ENEC or DISEC CCCs. Once Disabled by software, CCCs do not have any effect on this field. Default Value: 0x1
1	CR_EN	Controller Role Request (CR) Enable. This bit is only valid when this I3C Device is functioning as a Target, and reflects whether the controller can initiate the Controller Role Request (CR) on the I3C bus or not. Usually, this bit is set or cleared by the Active Controller through ENEC or DISEC CCC. Default Value: 0x1
0	TIR_EN	Target Interrupt Request Enable. This bit is only valid when this I3C Device is functioning as a Target, and reflects whether the block can initiate the TIR on the I3C bus or not. Usually, this bit is set or cleared by the Active Controller through ENEC or DISEC CCC. Default Value: 0x1

19.1.12 I3C_CORE_INTR_STATUS

Description: Reset Control Register

Address: 0x42A5003C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW1C	RW1C	R	R	R	R	R
HW Access	Reserved	RW1S	RW1S	RW	RW	RW	RW	RW
Name	Reserved	CCC_UP-DAT-ED_STS	TRANS-FER_ABOR T_STS	RE-SP_READY _STS	CMD_-QUEUE_RE ADY_STS	IBI_TH-LD_STS	RX_TH-LD_STS	TX_TH-LD_STS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	Reserved	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	Reserved	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	BUS_RE-SET_-DONE_STS	Reserved	BUSOWN-ER_UP-DATED_ST S	IBI_UPDAT-ED_STS	READ_REQ _RECV_ST S	DEFT-GT_STS	TRANS-FER_ER-R_STS	DYN_AD-DR_ASS-GN_STS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW1C	RW1C	Reserved	RW1C	RW1C
HW Access	Reserved			RW1S	RW1S	Reserved	RW1S	RW1S
Name	Reserved [23:21]			EXT_CM-D_SENT_S TS	SDA_RE-LEASED_S TS	Reserved	TGT_RST_ PATTERN_-DET_STS	START_DE-T_STS

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20	EXT_CMD_SENT_STS	EXT_CMD_REG_x has finished Status. This field is used only in target mode of operation. This interrupt is generated if Read Transfer has finished in the EXT_CMD_REG_x registers. This interrupt is cleared automatically when register EXT_CMD_VLD_STAT is read Default Value: 0x0
19	SDA_RELEASED_STS	SDA Released from Stuck state Status. This field is used only in target mode of operation. This interrupt is generated if the SCL was not changed for the prescribed amount of time defined by RELEASE_SDA_TIMING register. This bit can be cleared by writing 1'b1 Default Value: 0x0
17	TGT_RST_PATTERN_-DET_STS	Target Reset Pattern Detection Interrupt This field is used only when functioning as a Target. This interrupt is generated when the Target Reset pattern is detected. Default Value: 0x0

19.1.12 I3C_CORE_INTR_STATUS (continued)

16	START_DET_STS	START Detection Interrupt. This field is used only when functioning as a Target and indicates that a START has been detected. This interrupt is provided for the user/application (in CCR mode) to decide whether the NCR has taken over the ownership after the bus handover was completed successfully to move to Target mode. And to reset the reset action configured by the RSTACT CCC. This bit can be cleared by writing 1'b1. Default Value: 0x0
15	BUS_RESET_DONE_STS	Bus Reset Pattern Generation Done Status This field is used only when functioning as a Controller. This interrupt is generated when the requested Bus Reset Pattern Generation is completed. This bit can be cleared by writing 1'b1. Default Value: 0x0
13	BUSOWNER_UPDATED_STS	This interrupt is set when the block changes from being the Active Controller to a Secondary Controller/Target or vice versa. This bit can be cleared by writing 0x1. Default Value: 0x0
12	IBI_UPDATED_STS	IBI status is updated. This field is used only when functioning as a Target. It indicates that the IBI request initiated through TIR request register is addressed and status is updated. Default Value: 0x0
11	READ_REQ_RECV_STS	Read Request Received. This field is used only when functioning as a Target. Read Request received from the Active Controller when CMDQ is empty. This bit can be cleared by writing 0x1. Default Value: 0x0
10	DEFTGT_STS	Define Target CCC Received Status. This interrupt is generated if DEFTGTS CCC is received. This bit can be cleared by writing 0x1. Default Value: 0x0
9	TRANSFER_ERR_STS	Transfer Error Status. This interrupt is generated if any error occurs during transfer. The error type is specified in the response packet associated with the command (in ERR_STATUS field of RESPONSE_QUEUE_PORT register). This bit can be cleared by writing 0x1. Default Value: 0x0
8	DYN_ADDR_ASSGN_STS	Dynamic Address Assigned Status This field is used only in Target mode of operation. This interrupt is generated when the device's Dynamic Address is assigned through SETDASA, SETAASA, SETNEWDA or ENTDAA CCC. This bit can be cleared by writing 0x1 Default Value: 0x0
6	CCC_UPDATED_STS	CCC Table Updated Status. This field is used only when functioning as a Target. This interrupt is generated if any of the CCC registers are updated by the I3C Controller through CCC commands. This interrupt can be cleared by writing 0x1. Default Value: 0x0
5	TRANSFER_ABORT_STS	Transfer Abort Status. This field is used only when functioning as the Active Controller,. This interrupt is generated if the transfer is aborted. This interrupt can be cleared by writing 0x1. Default Value: 0x0

19.1.12 I3C_CORE_INTR_STATUS (continued)

4	RESP_READY_STS	Response Queue Ready Status. This interrupt is generated when number of entries in the response queue is greater than or equal to the threshold value specified by the RESP_BUF_THLD field in the QUEUE_THLD_CTRL register. This interrupt is cleared automatically when the number of entries in the response buffer is less than the threshold value specified. Default Value: 0x0
3	CMD_- QUEUE_READY_STS	Command Queue Ready. This interrupt is generated when number of empty locations in the command queue is greater than or equal to the threshold value specified by the CMD_EMPTY_BUF_THLD field in the QUEUE_THLD_CTRL register. This interrupt is cleared automatically when the number of empty locations in the command buffer is less than the threshold value specified. Default Value: 0x0
2	IBI_THLD_STS	IBI Buffer Threshold Status. This field is only used when the block is functioning as the Active Controller. This interrupt is generated when the number of entries in the IBI buffer is greater than or equal to the threshold value specified by the IBI_BUF_THLD field in the QUEUE_THLD_CTRL register. This interrupt is cleared automatically when the number of entries in IBI buffer is less than the threshold value specified. Default Value: 0x0
1	RX_THLD_STS	Receive Buffer Threshold Status. This interrupt is generated when number of entries in the receive buffer is greater than or equal to threshold value specified by the RX_BUF_THLD field in the DATA_BUFFER_THLD_CTRL register. This interrupt is cleared automatically when the number of entries in receive buffer is less than the threshold value specified. Default Value: 0x0
0	TX_THLD_STS	Transmit Buffer Threshold Status. This interrupt is generated when the number of empty locations in the transmit buffer is greater than or equal to the threshold value specified by the TX_EMPTY_BUF_THLD field in the DATA_BUFFER_THLD_CTRL register. This interrupt is cleared automatically when the number of empty locations in transmit buffer is less than threshold value specified. Default Value: 0x0

19.1.13 I3C_CORE_INTR_STATUS_EN

Description: Interrupt Status Enable Register.

Address: 0x42A50040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved	R	R	R	R	R	R	R
Name	Reserved	CCC_UP-DAT-ED_STS_EN	TRANS-FER_ABOR T_STS_EN	RE-SP_READY _STS_EN	CMD_-QUEUE_RE ADY_STS_ EN	IBI_TH-LD_STS_E N	RX_TH-LD_STS_E N	TX_TH-LD_STS_E N

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved	RW	RW	RW	RW	RW	RW
HW Access	R	Reserved	R	R	R	R	R	R
Name	BUS_RE-SET_-DONE_STS _EN	Reserved	BUSOWN-ER_UP-DATED_ST S_EN	IBI_UPDAT-ED_STS_E N	READ_REQ _RECV_ST S_EN	DEFT-GT_STS_E N	TRANS-FER_ER-R_STS_EN	DYN_AD-DR_ASS-GN_STS_E N

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW	RW	Reserved	RW	RW
HW Access	Reserved			R	R	Reserved	R	R
Name	Reserved [23:21]			EXT_CM-D_SENT_S TS_EN	SDA_RE-LEASED_S TS_EN	Reserved	TGT_RST_ PATTERN_-DE-T_STS_EN	START_DE-T_STS_EN

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20	EXT_CM-D_SENT_STS_EN	EXT_CMD_REG_x has finished Signal Enable. This field is used when operating as a Target. Default Value: 0x0
19	SDA_RE-LEASED_STS_EN	SDA Released from Stuck state Status Enable. This field is used in target mode of operation Default Value: 0x0
17	TGT_RST_PATTERN_-DET_STS_EN	Target Reset Pattern Detection Interrupt Status Enable Default Value: 0x0
16	START_DET_STS_EN	START Detection Interrupt Status Enable Default Value: 0x0
15	BUS_RESET_-DONE_STS_EN	Bus Reset Pattern Generation Done Status Enable Default Value: 0x0
13	BUSOWNER_UPDAT-ED_STS_EN	Bus owner Updated Status Enable Default Value: 0x0

19.1.13 I3C_CORE_INTR_STATUS_EN (continued)

12	IBI_UPDATED_STS_EN	IBI Updated Status Enable This field is only valid when functioning as a Target. Default Value: 0x0
11	READ_REQ_RECV_STS_EN	Read Request Received Status Enable This field is only valid when functioning as a Target. Default Value: 0x0
10	DEFTGT_STS_EN	Define Target CCC Received Status Enable Default Value: 0x0
9	TRANSFER_ERR_STS_EN	Transfer Error Status Enable Default Value: 0x0
8	DYN_ADDR_ASSGN_STS_EN	Dynamic Address Assigned Status Enable This field is only valid when functioning as a Target. Default Value: 0x0
6	CCC_UPDATED_STS_EN	CCC Table Updated Status Enable. This field is only valid when functioning as a Target. Default Value: 0x0
5	TRANSFER_ABORT_STS_EN	Transfer Abort Status Enable. This field is only valid when functioning as the Active Controller. Default Value: 0x0
4	RESP_READY_STS_EN	Response Queue Ready Status Enable Default Value: 0x0
3	CMD_QUEUE_READY_STS_EN	Command Queue Ready Status Enable Default Value: 0x0
2	IBI_THLD_STS_EN	IBI Buffer Threshold Status Enable This field is only valid when functioning aa the Active Controller. Default Value: 0x0
1	RX_THLD_STS_EN	Receive Buffer Threshold Status Enable Default Value: 0x0
0	TX_THLD_STS_EN	Transmit Buffer Threshold Status Enable Default Value: 0x0

19.1.14 I3C_CORE_INTR_SIGNAL_EN

Description: Interrupt Signal Enable Register

Address: 0x42A50044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved	R	R	R	R	R	R	R
Name	Reserved	CCC_UP-DAT-ED_SIGNA L_EN	TRANS-FER_ABOR T_SIG-NAL_EN	RE-SP_READY _SIG-NAL_EN	CMD_-QUEUE_RE ADY_SIG-NAL_EN	IBI_TH-LD_SIG-NAL_EN	RX_TH-LD_SIG-NAL_EN	TX_TH-LD_SIG-NAL_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved	RW	RW	RW	RW	RW	RW
HW Access	R	Reserved	R	R	R	R	R	R
Name	BUS_RE-SET_-DONE_SIG NAL_EN	Reserved	BUSOWN-ER_UP-DATED_SI GNAL_EN	IBI_UPDAT-ED_SIG-NAL_EN	READ_REQ _RECV_SI GNAL_EN	DEFT-GT_SIG-NAL_EN	TRANS-FER_ER-R_SIGNAL_ EN	DYN_AD-DR_ASS-GN_SIGNA L_EN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW	RW	Reserved	RW	RW
HW Access	Reserved			R	R	Reserved	R	R
Name	Reserved [23:21]			EXT_CM-D_SENT_SI GNAL_EN	SDA_RE-LEASED_SI GNAL_EN	Reserved	TGT_RST_ PATTERN_-DET_SIG-NAL_EN	START_DE-T_SIG-NAL_EN

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20	EXT_CMD_SENT_SIG-NAL_EN	EXT_CMD_REG_x has finished Signal Enable. This field is used when operating as a Target. Default Value: 0x0
19	SDA_RELEASED_SIG-NAL_EN	SDA Released from Stuck state Signal Enable. This field is used in target mode of operation Default Value: 0x0
17	TGT_RST_PATTERN_-DET_SIGNAL_EN	Target Reset Pattern Detection Interrupt Signal Enable Default Value: 0x0
16	START_DET_SIG-NAL_EN	START Detection Interrupt Signal Enable Default Value: 0x0
15	BUS_RESET_-DONE_SIGNAL_EN	Bus Reset Pattern Generation Done Signal Enable Default Value: 0x0
13	BUSOWNER_UPDAT-ED_SIGNAL_EN	Bus owner Updated Signal Enable Default Value: 0x0

19.1.14 I3C_CORE_INTR_SIGNAL_EN (continued)

12	IBI_UPDATED_SIGNAL_EN	IBI Updated Signal Enable This field is only valid when functioning as a Target. Default Value: 0x0
11	READ_REQ_RECV_SIGNAL_EN	Read Request Received Signal Enable This field is only valid when functioning as a Target. Default Value: 0x0
10	DEFTGT_SIGNAL_EN	Define Target CCC Received Signal Enable Default Value: 0x0
9	TRANSFER_ERR_SIGNAL_EN	Transfer Error Signal Enable Default Value: 0x0
8	DYN_ADDR_ASSGN_SIGNAL_EN	Dynamic Address Assigned Signal Enable This field is only valid when functioning as a Target. Default Value: 0x0
6	CCC_UPDATED_SIGNAL_EN	CCC Table Updated Signal Enable. This field is only valid when functioning as a Target. Default Value: 0x0
5	TRANSFER_ABORT_SIGNAL_EN	Transfer Abort Signal Enable. This field is only valid when functioning as the Active Controller. Default Value: 0x0
4	RESP_READY_SIGNAL_EN	Response Queue Ready Signal Enable Default Value: 0x0
3	CMD_QUEUE_READY_SIGNAL_EN	Command Queue Ready Signal Enable Default Value: 0x0
2	IBI_THLD_SIGNAL_EN	IBI Buffer Threshold Signal Enable This field is only valid when functioning aa the Active Controller. Default Value: 0x0
1	RX_THLD_SIGNAL_EN	Receive Buffer Threshold Signal Enable Default Value: 0x0
0	TX_THLD_SIGNAL_EN	Transmit Buffer Threshold Signal Enable Default Value: 0x0

19.1.15 I3C_CORE_INTR_FORCE

Description: Interrupt Force Enable Register

Address: 0x42A50048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	W	W	W	W	W	W	W
HW Access	Reserved	R	R	R	R	R	R	R
Name	Reserved	CCC_UP-DATED_-FORCE_EN	TRANS-FER_ABOR T_-FORCE_EN	RE-SP_READY _FORCE_E N	CMD_-QUEUE_RE ADY_-FORCE_EN	IBI_THLD_-FORCE_EN	RX_THLD_-FORCE_EN	TX_THLD_-FORCE_EN

Bits	15	14	13	12	11	10	9	8
SW Access	W	Reserved	W	W	W	W	W	W
HW Access	R	Reserved	R	R	R	R	R	R
Name	BUS_RE-SET_-DONE_FO RCE_EN	Reserved	BUSOWN-ER_UP-DATED_FO RCE_EN	IBI_UPDAT-ED_-FORCE_EN	READ_REQ _FORCE_E N	DEFTGT_-FORCE_EN	TRANS-FER_ER-R_FORCE_ EN	DYN_AD-DR_ASS-GN_FORC E_EN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			W	W	Reserved	W	W
HW Access	Reserved			R	R	Reserved	R	R
Name	Reserved [23:21]			EXT_CM-D_SENT_-FORCE_EN	SDA_RE-LEASED_-FORCE_EN	Reserved	TGT_RST_ PATTERN_-DET_-FORCE_EN	START_DE-T_-FORCE_EN

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20	EXT_CMD_SENT_-FORCE_EN	EXT_CMD_REG_x has finished Force Enable. This field is used when operating as a Target. Default Value: 0x0
19	SDA_RELEASED_-FORCE_EN	SDA Released from Stuck state Force Enable. This field is used in target mode of operation Default Value: 0x0
17	TGT_RST_PATTERN_-DET_FORCE_EN	Target Reset Pattern Detection Interrupt force Enable Default Value: 0x0
16	START_DET_FORCE_EN	START Detection Interrupt force Enable Default Value: 0x0
15	BUS_RESET_DONE_-FORCE_EN	Bus Reset Pattern Generation Done force Enable Default Value: 0x0
13	BUSOWNER_UPDAT-ED_FORCE_EN	Bus owner Updated Force Enable Default Value: 0x0

19.1.15 I3C_CORE_INTR_FORCE (continued)

12	IBI_UPDATED_-FORCE_EN	IBI Updated Force Enable This field is only valid when functioning as a Target. Default Value: 0x0
11	READ_REQ_FORCE_EN	Read Request Received Force Enable This field is only valid when functioning as a Target. Default Value: 0x0
10	DEFTGT_FORCE_EN	Define Target CCC Received Force Enable Default Value: 0x0
9	TRANSFER_ERR_-FORCE_EN	Transfer Error Force Enable Default Value: 0x0
8	DYN_ADDR_ASSGN_-FORCE_EN	Dynamic Address Assigned Force Enable This field is only valid when functioning as a Target. Default Value: 0x0
6	CCC_UPDATED_-FORCE_EN	CCC Table Updated Force Enable. This field is only valid when functioning as a Target. Default Value: 0x0
5	TRANSFER_ABORT_-FORCE_EN	Transfer Abort Force Enable. This field is only valid when functioning as the Active Controller. Default Value: 0x0
4	RESP_READY_-FORCE_EN	Response Queue Ready Force Enable Default Value: 0x0
3	CMD_QUEUE_READY_-FORCE_EN	Command Queue Ready Force Enable Default Value: 0x0
2	IBI_THLD_FORCE_EN	IBI Buffer Threshold Force Enable This field is only valid when functioning aa the Active Controller. Default Value: 0x0
1	RX_THLD_FORCE_EN	Receive Buffer Threshold Force Enable Default Value: 0x0
0	TX_THLD_FORCE_EN	Transmit Buffer Threshold Force Enable Default Value: 0x0

19.1.16 I3C_CORE_QUEUE_STATUS_LEVEL

Description: Queue Status Level Register.

Address: 0x42A5004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CMD_QUEUE_EMPTY_LOC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESP_BUF_BLR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	IBI_BUF_BLR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			RW				
Name	Reserved [31:29]			IBI_STS_CNT [28:24]				

Bits	Name	Description
28 : 24	IBI_STS_CNT	Default Value: 0x0
23 : 16	IBI_BUF_BLR	IBI Buffer Level Value. This field is used when functioning as the Active Controller. Contains the number of Valid IBI Status entries in the IBI Buffer. Default Value: 0x0
15 : 8	RESP_BUF_BLR	Response Buffer Level Value. Contains the number of valid data entries in the response Buffer. Default Value: 0x0
7 : 0	CMD_QUEUE_EMPTY-_LOC	Command Queue Empty Locations. Contains the number of empty locations in the command Buffer. Default Value: 0x10

19.1.17 I3C_CORE_DATA_BUFFER_STATUS_LEVEL

Description: Data Buffer Status Level Register.

Address: 0x42A50050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TX_BUF_EMPTY_LOC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RX_BUF_BLR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	RX_BUF_BLR	Receive Buffer Level Value. Contains the number of valid data entries in the receive Buffer. Default Value: 0x0
7 : 0	TX_BUF_EMPTY_LOC	Transmit Buffer Empty Level Value. Contains the number of empty locations in the transmit Buffer. Default Value: 0x40

19.1.18 I3C_CORE_PRESENT_STATE

Description: Present State Register

Address: 0x42A50054

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R	R	R
HW Access	Reserved					RW	RW	RW
Name	Reserved [7:3]					ACTIVE_-CONTROL-LER	SDA_LINE_SIG-NAL_LEV-EL	SCL_LINE_SIG-NAL_LEV-EL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [15:14]		CM_TFR_STS [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [23:22]		CM_TFR_ST_STS [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R	R			
HW Access	Reserved			RW	RW			
Name	Reserved [31:29]			CONTROL-LER_IDLE	CMD_TID [27:24]			

Bits	Name	Description
28	CONTROLLER_IDLE	This bit is only valid when this I3C Device is functioning the Active Controller, and reflects whether the block is in the Idle state or not. This bit is set when all the Queues (Command , Response, IBI) and Buffers (Transmit and Receive) are empty and the Controller State machine is in Idle state. Values: 0x0 Controller is not in IDLE State 0x1 Controller is in IDLE State. Default Value: 0x1
27 : 24	CMD_TID	This field reflects the Transaction-ID of the current executing command. Default Value: 0x0

19.1.18 I3C_CORE_PRESENT_STATE (continued)

21 : 16	CM_TFR_ST_STS	Active Controller Transfer State Status. This bit is only valid when this I3C Device is functioning the Active Controller, and indicates the state of current transfer currently executing by the I3C block. Values: 0x0: IDLE (Controller is Idle state, waiting for commands from application or Target initated In-band Interrupt) 0x1: START Generation State. 0x2: RESTART Generation State. 0x3: STOP Generation State. 0x4: START Hold Generation for the Target Initiated START State. 0x5: Broadcast Write Address Header(7'h7E,W) Generation State. 0x6: Broadcast Read Address Header(7'h7E,R) Generation State. 0x7: Dynamic Address Assignment State. 0x8: Target Address Generation State. 0xB: CCC Byte Generation State. 0xC: HDR Command Generation State. 0xD: Write Data Transfer State. 0xE: Read Data Transfer State. 0xF: In-Band Interrupt (TIR) Read Data State. 0x10: In-Band Interrupt Auto-Disable State 0x11: HDR-DDR CRC Data Generation/Receive State. 0x12: Clock Extension State. 0x13: Halt State. Default Value: 0x0
13 : 8	CM_TFR_STS	Transfer Type Status. Indicates the type of transfer currently executing by the I3C block. When functioning as the Active Controller, possible values are: 0x0: IDLE (Block is in Idle state, waiting for commands from application or Target initated In-band Interrupt) 0x1: Broadcast CCC Write Transfer. 0x2: Directed CCC Write Transfer. 0x3: Directed CCC Read Transfer. 0x4: ENTDAA Address Assignment Transfer. 0x5: SETDASA Address Assignment Transfer. 0x6: Private I3C SDR Write Transfer. 0x7: Private I3C SDR Read Transfer. 0x8: Private I2C SDR Write Transfer. 0x9: Private I2C SDR Read Transfer. 0xA: Private HDR Ternary Symbol (TS) Write Transfer. 0xB: Private HDR Ternary Symbol (TS) Read Transfer. 0xC: Private HDR Double-Data Rate (DDR) Write Transfer. 0xD: Private HDR Double-Data Rate (DDR) Read Transfer. 0xE: Servicing In-Band Interrupt Transfer. 0xF: Halt state (Block is in Halt State, waiting for the application to resume through DEVICE_CTRL Register) When functioning as a Target, possible values are: 0x0: IDLE (Block is in Idle state) 0x1: Hot-Join transfer state 0x2: IBI transfer state 0x3: Controller write transfer ongoing 0x4: Read data prefetch state 0x5: Controller read transfer ongoing 0x6: Bock is controller in Halt State waiting for resume from application Default Value: 0x0
2	ACTIVE_CONTROLLER	This Bit is used to check whether the block is currently the Active Controller or not. The Active Controller is the Controller that owns the SCL line. Values: 0x0: Secondary Controller is not the Active Controller and needs to request to be the Active Controller before initiating any transfer on the line. 0x1: Secondary Controller is the Active Controller and can initiate transfers on the line. Default Value: 0x0

19.1.18 I3C_CORE_PRESENT_STATE (continued)

1	SDA_LINE_SIGNAL_LEVEL	This bit is only valid when this I3C Device is functioning the Active Controller, and is used for debug and error recovery. This bit reflects the value of the SDA line as observed inside the block (after input synchronization). Default Value: 0x1
0	SCL_LINE_SIGNAL_LEVEL	This bit is only valid when this I3C Device is functioning the Active Controller, and is used for debug and error recovery. This bit reflects the value of the SCL line as observed inside the block (after input synchronization). Default Value: 0x1

19.1.19 I3C_CORE_CCC_DEVICE_STATUS

Description: Device Operating Status Register.

Address: 0x42A50058

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R	Reserved	R			
HW Access	RW		RW	Reserved	RW			
Name	ACTIVITY_MODE [7:6]		PROTO-COL_ERR	Reserved	PENDING_INTR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [15:14]		FRAME_ER ROR	BUFFER_N OT_AVAIL	DATA_NOT _READY	OVER-FLOW_ER R	TAR-GET_BUSY	UNDER-FLOW_ER R

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
13	FRAME_ERROR	Frame Error This bit is only valid when this I3C Device is functioning as a Target, and is set when a private write request initiated by the Active Controller has a frame error in HDR-DDR/HDR-TSP/TSL mode. This is cleared only after the Active Controller reads the device status through GETSTATUS_C-CC. Default Value: 0x0
12	BUFFER_NOT_AVAIL	Buffer not available This bit is only valid when this I3C Device is functioning as a Target, and is set when a private write request initiated by the Active Controller is NACKED because of RX buffer not having RX-_BUF_THLD number of empty locations or Response buffer being full. In SDR mode of operation this is cleared when the Active Controller issues GETSTATUS CCC or upon space becoming available in the buffer and the successful completion of the next write transfer. In HDR mode of operation it is cleared only when the Active Controller issues GETSTATUS CCC. Default Value: 0x0

19.1.19 I3C_CORE_CCC_DEVICE_STATUS (continued)

11	DATA_NOT_READY	Data not ready This bit is only valid when this I3C Device is functioning as a Target, and is set when private a private read request initiated by the Active Controller is NACKED because of any of the following conditions Command FIFO Empty. Transmit FIFO threshold is not met. Response FIFO Full. This bit is cleared when the Active Controller issues GETSTATUS CCC or upon successful completion of the subsequent read transfer. Default Value: 0x0
10	OVERFLOW_ERR	Overflow Error This bit is only valid when this I3C Device is functioning as a Target, and is set when an overflow error condition is detected during a private write transfer initiated by the Active Controller. This is cleared only after the Active Controller reads the Device Status through GETSTATUS CCC. Default Value: 0x0
9	TARGET_BUSY	Target Busy This bit is set if any change is made by the Active Controller to the MRL register or occurance of any error. It is cleared after Target application resumes the block operation by writing to the RESUME bit of the DEVICE_CONTROL register. Default Value: 0x0
8	UNDERFLOW_ERR	Underflow error This bit is only valid when this I3C Device is functioning as a Target, and is set when terminates a private read transfer initiated by the Active Controller is terminated by the device because of unavailability of data in the transmit buffer. This bit is cleared only after the Active Controller reads the Device Status through a GETSTATUS CCC. Default Value: 0x0
7 : 6	ACTIVITY_MODE	Pending Interrupt This field reflects the value from I3C.CCC_GETSTATUS.ACT_MODE. Default Value: 0x0
5	PROTOCOL_ERR	Protocol Error This bit is only valid when this I3C Device is functioning as a Target, and is set when a Parity/CRC error is encountered during a private write transfer initiated by the Active Controller. Default Value: 0x0
3 : 0	PENDING_INTR	Pending Interrupt This field reflects the value from I3C.CCC_GETSTATUS.PENDING_INT. Default Value: 0x0

19.1.20 I3C_CORE_DEVICE_ADDR_TABLE_POINTER

Description: Pointer for Device Address Table

Address: 0x42A5005C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	P_DEV_ADDR_TABLE_START_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	P_DEV_ADDR_TABLE_START_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	DEV_ADDR_TABLE_DEPTH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DEV_ADDR_TABLE_DEPTH [31:24]							

Bits	Name	Description
31 : 16	DEV_ADDR_TABLE_DEPTH	Depth of the Device Address Table in the internal memory. Default Value: 0xB
15 : 0	P_DEV_ADDR_TABLE_START_ADDR	Start Address of the Device Address Table in the internal memory. Default Value: 0x2C0

19.1.21 I3C_CORE_DEV_CHAR_TABLE_POINTER

Description: Pointer for Device Characteristics Table

Address: 0x42A50060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	P_DEV_CHAR_TABLE_START_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	R				R			
Name	DEV_CHAR_TABLE_DEPTH [15:12]				P_DEV_CHAR_TABLE_START_ADDR [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW				R		
HW Access	Reserved	RW				R		
Name	Reserved	PRESENT_DEV_CHAR_TABLE_INDX [22:19]				DEV_CHAR_TABLE_DEPTH [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
22 : 19	PRESENT_DEV_CHAR_TABLE_INDX	Current index of the Device Characteristics Table. This field returns the current location of Device Characteristics Table index. Initially, this index points to 0. Once the complete characteristics information of a Target device is written into Device Characteristics Table during ENTDAA, this index increments by 1. The first winning device information is stored in Device Characteristics Table index 0, the second winning device information in index 1, and so on. If required, this index can be used to override the location, where characteristic information of Target devices on the I3C bus are written during ENTDAA. Hence, this field is useful only when the device is functioning as the Active Controller. During DEFTGTS CCC, the index always starts from 0. When the device is functioning as a Target, this field is read-only. Default Value: 0x0
18 : 12	DEV_CHAR_TABLE_DEPTH	Depth of Device Characteristics Table in the internal memory. Default Value: 0x2C
11 : 0	P_DEV_CHAR_TABLE_START_ADDR	Start Address of the Device Characteristics Table in the internal memory. Default Value: 0x200

19.1.22 I3C_CORE_VENDOR_SPECIFIC_REG_POINTER

Description: Pointer for Vendor Specific Registers.

Address: 0x42A5006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	P_VENDOR_REG_START_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	P_VENDOR_REG_START_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	P_VENDOR_REG_START_ADDR	Start Address of Vendor specific registers. Default Value: 0xB0

19.1.23 I3C_CORE_TGT_MIPI_ID_VALUE

Description: I3C MIPI Manufacturer ID Register

Address: 0x42A50070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							RW
HW Access	R							R
Name	TGT_MIPI_MFG_ID [7:1]							TGT_PROV_ID_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TGT_MIPI_MFG_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 1	TGT_MIPI_MFG_ID	Specifies the MIPI Manufacturer ID (Provisioned ID [47:33]). Default Value: 0x0
0	TGT_PROV_ID_SEL	Specifies the Provisioned ID Type Selector (Provisioned ID [32]). Values: 0x0: Vendor Fixed Value 0x1: Random Value Default Value: 0x0

19.1.24 I3C_CORE_TGT_PID_VALUE

Description: I3C Normal Provisional ID Register

Address: 0x42A50074

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TGT_PID_DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	TGT_INST_ID [15:12]				TGT_PID_DCR [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TGT_PART_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TGT_PART_ID [31:24]							

Bits	Name	Description
31 : 16	TGT_PART_ID	Specifies the Part ID of this I3C block (PID[31:16]). Default Value: 0x0
15 : 12	TGT_INST_ID	Specifies the MIPI Instance ID of this I3C block (Provisioned ID [15:12]). Default Value: 0x0
11 : 0	TGT_PID_DCR	Specifies the last 12 bit of the MIPI Provisioned ID of this I3C block (Provisioned ID [11:0]). Default Value: 0x0

19.1.25 I3C_CORE_TGT_CHAR_CTRL

Description: I3C Target Characteristic Register.

Address: 0x42A50078

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	R	R	R	R	RW
HW Access	R		R	R	R	R	R	R
Name	DEVICE_ROLE [7:6]		HDR_CA-PABLE	BRIDGE_ID ENTIFIER	OFFLINE_-CAPABLE	IBI_PAY-LOAD	IBI_RE-QUEST_-CAPABLE	MAX_-DATA_-SPEED_LI MIT

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	HDR_CAP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	HDR_CAP	Default Value: 0x1
15 : 8	DCR	I3C Device Characteristic Regster (DCR) Value Default Value: 0x0
7 : 6	DEVICE_ROLE	Device Role field in Bus Characteristic Register (BCR[7:6]). This bit is set by default as 0x1 (device has Controller capabilities) and the application is not expected to change it. However, if the application chooses to operate the device as a Target-only device (no controlelr capability), then the Device Role can be overwritten as Target-only. Values: 0x0: I3C Target 0x1: I3C Controller capable The field is Reset to its default value upon HW/SW Reset. SW must program the values again after issuing reset. Default Value: 0x1
5	HDR_CAPABLE	SDR Only or SDR and HDR Capable field in Bus Characteristic Register (BCR[5]). This bit can be modified by the application if it does not want to advertize the Target's HDR capability to the Active Controller. The field is Reset to its default value upon HW/SW Reset. SW must program the values again after issuing reset. Default Value: 0x1
4	BRIDGE_IDENTIFIER	Default Value: 0x0
3	OFFLINE_CAPABLE	Default Value: 0x0

19.1.25 I3C_CORE_TGT_CHAR_CTRL (continued)

2	IBI_PAYLOAD	Default Value: 0x1
1	IBI_REQUEST_CAPABLE	Default Value: 0x1
0	MAX_DATA_SPEED_LIMIT	Max Data Speed Limitation field in Bus Characteristic Register (BCR[0]). Specifies whether or not this I3C device has a maximum data speed limitation. If this bit is set to 0, controller NACK's the GETMXDS CCC sent by the Active Controller. If this bit is set to 1, controller returns the data in MAX_DATA_SPEED and MAX_READ_TURNAROUND register in response the GETMXDS CCC sent by the Active Controller. The field is reset to its default value upon HW/SW Reset. SW must program the values again after issuing reset. Default Value: 0x1

19.1.26 I3C_CORE_TGT_MAX_LEN

Description: I3C Max Write/Read Length Register.

Address: 0x42A5007C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MWL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MWL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MRL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MRL [31:24]							

Bits	Name	Description
31 : 16	MRL	I3C Device Max Read Length Default Value: 0xFF
15 : 0	MWL	I3C Device Max Write Length Default Value: 0xFF

19.1.27 I3C_CORE_MAX_READ_TURNAROUND

Description: MXDS Maximum Read Turnaround Time.

Address: 0x42A50080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	MXDS_MAX_RD_TURN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MXDS_MAX_RD_TURN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	MXDS_MAX_RD_TURN [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 0	MXDS_MAX_RD_TURN	Specifies the maximum read turnaround time (in microseconds (us)) of this I3C device. Default Value: 0x0

19.1.28 I3C_CORE_MAX_DATA_SPEED

Description: Maximum Data Speed Register

Address: 0x42A50084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW		
HW Access	Reserved				R	R		
Name	Reserved [7:4]				MXDS_DEF_BYTE_-SUPPORT	MXDS_MAX_WR_SPEED [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [15:11]					MXDS_MAX_RD_SPEED [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW	RW		
HW Access	Reserved				R	R		
Name	Reserved [23:20]				MXDS_STO P_PERMIT	MXDS_CLK_DATA_TURN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [31:27]					MXDS_SET_ACTIVI-TY_STATE	MXDS_ACTIVITY_STATE [25:24]	

Bits	Name	Description
26	MXDS_SET_ACTIVI-TY_STATE	This bit indicates whether the Active Controller should set the Bus to the Activity State indicated in bits 25:24 before handing the Controller Role off to this I3C Device as part of the normal flow. Values: - 0x0 (SET_ACIVITY_STATE_0): The controller will not set the Bus to any Activity state. - 0x1 (SET_ACIVITY_STATE_1): The controller will set the Bus to any Activity state based on the value in 25:24 field of register Default Value: 0x0
25 : 24	MXDS_ACTIVITY_STATE	This 2-bit integer indicates whether this I3C Device initially acts with a given Activity State, after becoming Active Controller on the Bus according to the Controller handoff flow Values: - 0x0 (ACIVITY_STATE_0): Acts as Activity state 0. - 0x1 (ACIVITY_STATE_1): Acts as Activity state 1. - 0x2 (ACIVITY_STATE_2): Acts as Activity state 2. - 0x3 (ACIVITY_STATE_3): Acts as Activity state 3 Default Value: 0x0
19	MXDS_STOP_PERMIT	Specifies the stop support between write and read Values: - 0x0 (STOP_PERMIT_0): Stop after write will cancel the read. - 0x1 (STOP_PERMIT_1): Target permits the write and read to be seperated by a STOP Default Value: 0x0

19.1.28 I3C_CORE_MAX_DATA_SPEED (continued)

18 : 16	MXDS_CLK_-DATA_TURN	Specifies the clock to data turnaround time (Tsco parameter) of this I3C Target device. Values: 0x0 : 8ns 0x1 : 9ns 0x2 : 10ns 0x3 : 11ns 0x4 : 12ns > 0x4: Reserved/user Defined Default Value: 0x0
10 : 8	MXDS_MAX_RD_SPEED	Specifies the Maximum Sustained Data Rate for non-CCC messages sent by this I3C Target device to the Active Controller. Values: 0x0 : 12.5MHz 0x1 : 8MHZ 0x2 : 6MHz 0x3 : 4MHz 0x4 : 2MHz > 0x4: Reserved/User Defined Default Value: 0x0
3	MXDS_DEF_BYTE_SUP-PORT	Specifies the defining byte support of GETMXDS CCC Values: - 0x0 (DEF_BYTE_0): Defining byte is not supported for GETMXDS CCC. - 0x1 (DEF_BYTE_1): Defining byte is supported for GETMXDS CCC Default Value: 0x0
2 : 0	MXDS_MAX_WR_SPEED	Specifies the Maximum Sustained Data Rate for non-CCC messages sent by the Active Controller to this I3C Target device. Values: 0x0 : 12.5MHz 0x1 : 8MHZ 0x2 : 6MHz 0x3 : 4MHz 0x4 : 2MHz > 0x4: Reserved for future use by MIPI Alliance Default Value: 0x0

19.1.29 I3C_CORE_TGT_INTR_REQ

Description: Target Interrupt Request Register

Address: 0x42A5008C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved		RW	RW	RW		RW
HW Access	R	Reserved		R	RW	RW		RW
Name	CE3_RECOVERY	Reserved [6:5]		TS	CR	TIR_CTRL [2:1]		TIR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MDB [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIR_DATA_LENGTH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	TIR_DATA_LENGTH	TIR Data Length This field should be programmed by the Target application to give the data length for the payload data other than the MDB byte. This field is only applicable when BCR[2] is set indicating that TIR supports payload data. Only a maximum of 4 bytes of TIR payload is supported. Default Value: 0x0
15 : 8	MDB	Mandatory Data Byte This field gives the mandatory data byte which is required to be transmitted after the Active Controller ACKs the Target address during TIR transfer. This field is only applicable when BCR[2] is set indicating that TIR supports payload data. Default Value: 0x0
7	CE3_RECOVERY	Recovery from CE3 error. When the conditions for entering CE3 error are met (expiry of application running timer and TGT_INTR_REQ[TIR] is not set to '0'), the user will program this bit for recovering from CE3 error. Upon receiving this bit, the Target will move to Controller Mode (update PRESENT_STATE.ACTIVE_CONTROLLER bit to 1) and generate a START (also clear the TGT_INTR_REQ[TIR]) and continue in generating 0x7E followed by STOP. This bit is auto cleared by the Controller after the completion of recovery and moved to Active Controller mode. Default Value: 0x0

19.1.29 I3C_CORE_TGT_INTR_REQ (continued)

4	TS	Support for Asynchronous Time Stamp (Mode-0). Enabling this bit will allow the Target to capture the Time_x0002_Stamp from external input signal 'async0_ts_cntr' during T_C1 and T_C2 markers and append it along with the Payload data. NOTE: This bit is valid only if TGT_INTR_REQ[MDB] and TGT_INTR_REQ[TIR] bits are set to '1'. Default Value: 0x0
3	CR	Controller Role Request When set, the block attempts to issue the request to become the Active Controller on the I3C bus. Once that is issued and the Active Controller accepts (ACK), or if the block is unable to issue the request, then the block clears this bit automatically and updates the IBI_STS field. If NACK response is received for the request, the block reattempts the CR upon detecting the next START condition from the Active Controller or after the Bus Available time. Once set, the application cannot clear this bit. Default Value: 0x0
2 : 1	TIR_CTRL	Target Interrupt Request Control Values: 0x0: Indicates source of TIR data to be from the registers. 0x1: Pull SDA line low and release SDA after sampling SCL low (pulled by controller). Used for CE3 recovery during Controller Handover procedure. Default Value: 0x0
0	TIR	Target Interrupt Request When set, the Target Controller attempts to issue the TIR on the I3C bus. Once issued and when the Active Controller accepts (ACK), or if the block is unable to issue the TIR, then the block clears this bit automatically and updates the IBI_STS field. If the NACK response is received for the TIR, the block reattempts the TIR upon detecting the next START condition from the Active Controller or after the Bus Available Time. Once set, the application cannot clear this bit. Default Value: 0x0

19.1.30 I3C_CORE_TGT_TIR_DATA

Description: Target Interrupt Request Data Register

Address: 0x42A50094

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIR_DATA_BYTE0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIR_DATA_BYTE1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIR_DATA_BYTE2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TIR_DATA_BYTE3 [31:24]							

Bits	Name	Description
31 : 24	TIR_DATA_BYTE3	Target Interrupt Request Data Byte0 This register TGT_TIR_DATA containing four bytes of TIR Data will be in effect only when TIR_CTRL field in TGT_INTR_REQ is programmed to 00 00 provided the data length is up to 4. This field holds the first byte of TIR DATA that will be passed after the MDB when TIR is initiated by the application on writing into TIR bit in TGT_INTR_REQ Register. Default Value: 0x0
23 : 16	TIR_DATA_BYTE2	Target Interrupt Request Data Byte0 This register TGT_TIR_DATA containing four bytes of TIR Data will be in effect only when TIR_CTRL field in TGT_INTR_REQ is programmed to 00 00 provided the data length is up to 3. This field holds the first byte of TIR DATA that will be passed after the MDB when TIR is initiated by the application on writing into TIR bit in TGT_INTR_REQ Register. Default Value: 0x0
15 : 8	TIR_DATA_BYTE1	Target Interrupt Request Data Byte0 This register TGT_TIR_DATA containing four bytes of TIR Data will be in effect only when TIR_CTRL field in TGT_INTR_REQ is programmed to 00 00 provided the data length is up to 2. This field holds the first byte of TIR DATA that will be passed after the MDB when TIR is initiated by the application on writing into TIR bit in TGT_INTR_REQ Register. Default Value: 0x0

19.1.30 I3C_CORE_TGT_TIR_DATA (continued)

7 : 0	TIR_DATA_BYTE0	Target Interrupt Request Data Byte0 This register TGT_TIR_DATA containing four bytes of TIR Data will be in effect only when TIR_CTRL field in TGT_INTR_REQ is programmed to 00 00 provided the data length is up to 1. This field holds the first byte of TIR DATA that will be passed after the MDB when TIR is initiated by the application on writing into TIR bit in TGT_INTR_REQ Register. Default Value: 0x0

19.1.31 I3C_CORE_TGT_IBI_RESP

Description: Target IBI Response Register

Address: 0x42A50098

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	
HW Access	Reserved						RW	
Name	Reserved [7:2]						IBI_STS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TIR_RESP_DATA_LENGTH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TIR_RESP_DATA_LENGTH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 8	TIR_RESP_- DATA_LENGTH	Data Length for TIR Response The value in this filed will indicate the number of bytes remaining that was not transmitted because of the Active Controller early terminating the TIR transfer Default Value: 0x0
1 : 0	IBI_STS	IBI Completion Status This field is common for TIR and CR IBIs. Values: 0x00: Reserved 0x01: IBI accepted by the Active Controller (ACK response received) 0x10: Controller Early Terminate (only for TIR with Data). 0x11: IBI Not Attempted Default Value: 0x0

19.1.32 I3C_CORE_DEVICE_CTRL_EXTENDED

Description: Device Control Extended Register

Address: 0x42A500B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	Reserved	RW	
HW Access	Reserved			R	R	Reserved	RW	
Name	Reserved [7:5]			DEEP-_SLEEP_-CAP	GETAC-CCR_ACK_CTRL	Reserved	DEV_OPERATION_-MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	DEEP_SLEEP_CAP	This bit indicates the Deep Sleep capability of the Secondary Controller Device. Values: 0x0: This Device shall remain active and continue to monitor the I3C Bus to listen for these Broadcast CCCs, and shall not enter a deep sleep state from which it must be re-synchronized by the Active Controller before it can accept the Controller Role. 0x1: This Device may enter a deep sleep state during which it may miss some Broadcast DEFTGTS and DEFGRPA CCCs sent by the Active Controller. It will require re-synchronization upon re-entering a normal operating state,before it can accept the Controller Role with the GETACCCR CCC. Default Value: 0x0
3	GETACCCR_ACK_CTRL	In Target mode of operation, this bit serves as a control to ACK/NACK the GETACCCR CCC from the Active Controller. Values: 0x0: ACK GETACCCR CCC 0x1: NACK GETACCCR CCC Default Value: 0x0
1 : 0	DEV_OPERATION_-MODE	This bit is used to select the initial device role before the block is enabled. This field should only be written before the I3C block is enabled This field is automatically updated by the block once the a role change takes place. Values: 0x0: Primary Controller (starts as the Active Controller and initializes/configures the I3C bus) 0x1: Secondary Controller (starts as a Target, but can become the Active Controller) Default Value: 0x1

19.1.33 I3C_CORE_SCL_I3C_OD_TIMING

Description: SCL I3C Open Drain Timing Register

Address: 0x42A500B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	I3C_OD_LCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	I3C_OD_HCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	I3C_OD_HCNT	I3C Open Drain High Count. SCL open-drain High count (I3C) for I3C transfers targeted to I3C devices. Default Value: 0xA
7 : 0	I3C_OD_LCNT	I3C Open Drain Low Count. SCL Open-drain low count for I3C transfers targeted to I3C devices. Default Value: 0x10

19.1.34 I3C_CORE_SCL_I3C_PP_TIMING

Description: SCL I3C Push Pull Timing Register

Address: 0x42A500B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	I3C_PP_LCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	I3C_PP_HCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	I3C_PP_HCNT	I3C Push Pull High Count. SCL push-pull High count for I3C transfers targeted to I3C devices. Default Value: 0xA
7 : 0	I3C_PP_LCNT	I3C Push Pull Low Count. SCL Push-pull low count for I3C transfers targeted to I3C devices. Default Value: 0xA

19.1.35 I3C_CORE_SCL_I2C_FM_TIMING

Description: SCL I2C Fast Mode Timing Register

Address: 0x42A500BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	I2C_FM_LCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	I2C_FM_LCNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	I2C_FM_HCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	I2C_FM_HCNT [31:24]							

Bits	Name	Description
31 : 16	I2C_FM_HCNT	I2C Fast Mode High Count The SCL open-drain high count timing for I2C fast mode transfers. Default Value: 0x10
15 : 0	I2C_FM_LCNT	I2C Fast Mode Low Count The SCL open-drain low count timing for I2C fast mode transfers. Default Value: 0x10

19.1.36 I3C_CORE_SCL_I2C_FMP_TIMING

Description: SCL I2C Fast Mode Plus Timing Register

Address: 0x42A500C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	I2C_FMP_LCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	I2C_FMP_LCNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	I2C_FMP_HCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	I2C_FMP_HCNT	I2C Fast Mode Plus High Count The SCL open-drain high count timing for I2C fast mode plus transfers. Default Value: 0x10
15 : 0	I2C_FMP_LCNT	I2C Fast Mode Plus Low Count The SCL open-drain low count timing for I2C fast mode plus transfers. Default Value: 0x10

19.1.37 I3C_CORE_SCL_EXT_LCNT_TIMING

Description: SCL Extended Low Count Timing Register.

Address: 0x42A500C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	I3C_EXT_LCNT_1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	I3C_EXT_LCNT_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	I3C_EXT_LCNT_3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	I3C_EXT_LCNT_4 [31:24]							

Bits	Name	Description
31 : 24	I3C_EXT_LCNT_4	I3C Extended Low Count Register 4 SDR4 uses this register field for determining the extended SCL low phase. Default Value: 0x20
23 : 16	I3C_EXT_LCNT_3	I3C Extended Low Count Register 3 SDR3 uses this register field for determining the extended SCL low phase. Default Value: 0x20
15 : 8	I3C_EXT_LCNT_2	I3C Extended Low Count Register 2 SDR2 uses this register field for determining the extended SCL low phase. Default Value: 0x20
7 : 0	I3C_EXT_LCNT_1	I3C Extended Low Count Register 1 SDR1 uses this register field for determining the extended SCL low phase. Default Value: 0x20

19.1.38 I3C_CORE_SCL_EXT_TERMN_LCNT_TIMING

Description: SCL Termination Bit Low Count Timing Register

Address: 0x42A500CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				I3C_EXT_TERMN_LCNT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	STOP_HLD_CNT [31:28]				Reserved [27:24]			

Bits	Name	Description
31 : 28	STOP_HLD_CNT	STOP HOLD Count. Stop Hold Count in terms of core_clks which is used for generation of Stop Hold generation in Controller Mode. Default Value: 0x1
3 : 0	I3C_EXT_TERMN_LCNT	I3C Read Termination Bit Low count. Extended I3C Read Termination Bit low count for I3C Read transfers. Effective Termination-Bit Low Period is derived based on the SDR speed as shown below. SDR0 speed: I3C_PP_LCNT + I3C_EXT_TERMN_LCNT SDR1 speed: I3C_EXT_LCNT_1 + I3C_EXT_TERMN_LCNT SDR2 speed: I3C_EXT_LCNT_2 + I3C_EXT_TERMN_LCNT SDR3 speed: I3C_EXT_LCNT_3 + I3C_EXT_TERMN_LCNT SDR4 speed: I3C_EXT_LCNT_4 + I3C_EXT_TERMN_LCNT Default Value: 0x0

19.1.39 I3C_CORE_SDA_HOLD_SWITCH_DLY_TIMING

Description: SDA Hold and Mode Switch Delay Timing Register

Address: 0x42A500D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					SDA_OD_PP_SWITCH_DLY [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [15:11]					SDA_PP_OD_SWITCH_DLY [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					SDA_TX_HOLD [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18 : 16	SDA_TX_HOLD	This field controls the hold time (in terms of the CORE_CLK cycles) of the transmit data (SDA) with respect to the SCL edge in FM, FM+, SDR and DDR speed mode of operations. The valid values are 0x1 to 0x7. Others are Reserved. Default Value: 0x1
10 : 8	SDA_P-P_OD_SWITCH_DLY	This field is used to delay the sda_oe with respect to sda_out (in terms of the core clock period) while switching the transfer from PP1 (Push-Pull Mode SDA=1) to OD1 (Open- Drain SDA=1). The valid value can range from 0 to 4. Others are Reserved. Default Value: 0x0
2 : 0	SDA_OD_P-P_SWITCH_DLY	This field is used to delay the sda_oe with respect to sda_out while switching the transfer from OD1 (Open-Drain Mode SDA=1) to PP1 (Push-Pull Mode SDA=1). The valid value can range from 0 to 4. Others are reserved. Default Value: 0x0

19.1.40 I3C_CORE_BUS_FREE_AVAIL_TIMING

Description: Bus Free and Available Timing Register

Address: 0x42A500D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BUS_FREE_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	BUS_FREE_TIME [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BUS_AVAILABLE_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	BUS_AVAILABLE_TIME [31:24]							

Bits	Name	Description
31 : 16	BUS_AVAILABLE_TIME	Bus Available Count Value This register field is used only When functioning as a Target. This field is used by the block to initiate an IBI after the STOP condition. Default Value: 0x20
15 : 0	BUS_FREE_TIME	I3C Bus Free Count Value This register field is used only when functioning as the Active Controller. In a Pure Bus System, this field represents the tCAS parameter. In a Mixed Bus system, this field is expected to be programmed to tLOW of I2C Timing. Default Value: 0x20

19.1.41 I3C_CORE_BUS_IDLE_TIMING

Description: Bus Idle Timing Register

Address: 0x42A500D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BUS_IDLE_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	BUS_IDLE_TIME [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				BUS_IDLE_TIME [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 0	BUS_IDLE_TIME	Bus Idle Count Value This field is used by the block to initiate a Hot-Join request if the dynamic address is not valid. Default Value: 0x20

19.1.42 I3C_CORE_SCL_LOW_CTR_EXT_TIMEOUT

Description: SCL LOW Controller Timeout

Address: 0x42A500DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCL_LOW_CTR_TIMEOUT_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SCL_LOW_CTR_TIMEOUT_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SCL_LOW_CTR_TIMEOUT_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [31:26]						SCL_LOW_CTR_TIME-OUT_COUNT [25:24]	

Bits	Name	Description
25 : 0	SCL_LOW_CTR_TIME-OUT_COUNT	This count defines the number of core clock periods to count for generation of the SCL Low Bus Reset Pattern. Default Value: 0x3567E0

19.1.43 I3C_CORE_RELEASE_SDA_TIMING

Description: Release SDA count value.

Address: 0x42A500EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELEASE_SDA_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELEASE_SDA_TIME [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				RELEASE_SDA_TIME [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 0	RELEASE_SDA_TIME	Release SDA count value This field is used in the target mode of operation to release the SDA line if SCL is not changing for a prescribed amount of time programmed in this register (RELEASE_SDA_TIME * (in terms of the core clock/pclk period). Default Value: 0x4E20

19.1.44 I3C_CORE_EXT_TX_DATA_PORT_0

Description: DWC_mipi_i3c Directed read Vendor-specific CCC 0 TX Data Port Register

Address: 0x42A50130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_0 [31:24]							

Bits	Name	Description
31 : 0	EXT_TX_DATA_PORT_0	Transmit Data Port for Directed Read Vendor CCC 0. This port is mapped to the Directed Read Vendor CCC 0 Tx_x0002_Data Buffer. The transmit data should always be packed as 4-byte aligned data words and written to the Transmit Data Port register. If the Command length is not aligned to 4-bytes, then the additional bytes are ignored. Default Value: 0x0

19.1.45 I3C_CORE_EXT_TX_DATA_PORT_1

Description: DWC_mipi_i3c Directed read Vendor-specific CCC 1 TX Data Port Register

Address: 0x42A50134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_1 [31:24]							

Bits	Name	Description
31 : 0	EXT_TX_DATA_PORT_1	Transmit Data Port for Directed Read Vendor CCC 1. This port is mapped to the Directed Read Vendor CCC 1 Tx_x0002_Data Buffer. The transmit data should always be packed as 4-byte aligned data words and written to the Transmit Data Port register. If the Command length is not aligned to 4-bytes, then the additional bytes are ignored. Default Value: 0x0

19.1.46 I3C_CORE_EXT_TX_DATA_PORT_2

Description: DWC_mipi_i3c Directed read Vendor-specific CCC 2 TX Data Port Register

Address: 0x42A50138

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_2 [31:24]							

Bits	Name	Description
31 : 0	EXT_TX_DATA_PORT_2	Transmit Data Port for Directed Read Vendor CCC 2. This port is mapped to the Directed Read Vendor CCC 2 Tx_x0002_Data Buffer. The transmit data should always be packed as 4-byte aligned data words and written to the Transmit Data Port register. If the Command length is not aligned to 4-bytes, then the additional bytes are ignored. Default Value: 0x0

19.1.47 I3C_CORE_EXT_TX_DATA_PORT_3

Description: DWC_mipi_i3c Directed read Vendor-specific CCC 3 TX Data Port Register

Address: 0x42A5013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_3 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	EXT_TX_DATA_PORT_3 [31:24]							

Bits	Name	Description
31 : 0	EXT_TX_DATA_PORT_3	Transmit Data Port for Directed Read Vendor CCC 3. This port is mapped to the Directed Read Vendor CCC 3 Tx_x0002_Data Buffer. The transmit data should always be packed as 4-byte aligned data words and written to the Transmit Data Port register. If the Command length is not aligned to 4-bytes, then the additional bytes are ignored. Default Value: 0x0

19.1.48 I3C_CORE_EXT_0_1_DATA_BUF_STS_LEVEL

Description: Vendor-specific CCC types 0 and 1 Data Buffer Status Level Register

Address: 0x42A50154

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	EXT_0_TX_BUF_EMPTY_LOC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	EXT_1_TX_BUF_EMPTY_LOC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	EXT_1_TX_BUF_EMPTY-_LOC	Directed Read Vendor CCC 1 Transmit Buffer Empty Level Value. Contains the number of empty locations in the Directed Read Vendor CCC 1 transmit Buffer Default Value: 0x2
7 : 0	EXT_0_TX_BUF_EMPTY-_LOC	Directed Read Vendor CCC 0 Transmit Buffer Empty Level Value. Contains the number of empty locations in the Directed Read Vendor CCC 0 transmit Buffer Default Value: 0x2

19.1.49 I3C_CORE_EXT_2_3_DATA_BUF_STS_LEVEL

Description: Vendor-specific CCC types 2 and 3 Data Buffer Status Level Register

Address: 0x42A50158

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	EXT_2_TX_BUF_EMPTY_LOC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	EXT_3_TX_BUF_EMPTY_LOC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	EXT_3_TX_BUF_EMPTY-_LOC	Directed Read Vendor CCC 3 Transmit Buffer Empty Level Value. Contains the number of empty locations in the Directed Read Vendor CCC 3 transmit Buffer Default Value: 0x2
7 : 0	EXT_2_TX_BUF_EMPTY-_LOC	Directed Read Vendor CCC 2 Transmit Buffer Empty Level Value. Contains the number of empty locations in the Directed Read Vendor CCC 2 transmit Buffer Default Value: 0x2

19.1.50 I3C_CORE_EXT_CMD_REG_0

Description: TID, CCC type value and Defining Byte of Vendor-specific CCC 0 Register

Address: 0x42A50164

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			Reserved		
HW Access	R		R			Reserved		
Name	DL_LSB [7:6]		TID [5:3]			Reserved [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEFINING_BYTE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CCC_TYPE [31:24]							

Bits	Name	Description
31 : 24	CCC_TYPE	Directed Read Vendor-specific CCC 0 Type. Contains the CCC type 0. Data corresponds to this CCC type is mapped to EXT_TX_DATA_PORT_0. Default Value: 0x0
23 : 16	DEFINING_BYTE	Directed Read Vendor CCC 0 Defining Byte. Contains the Defining byte of CCC type 0. Data corresponds to this Defining byte with CCC type 0 is mapped to EXT_TX_DATA_PORT_0. Default Value: 0x0
7 : 6	DL_LSB	LSB 2bits of Data Length. Contains the Last two bits of data length. This 2bits will act as a byte enable for last Data DWORD of CCC type 0 Default Value: 0x0
5 : 3	TID	Transaction ID. For a Vendor Specific CCC TID should be always 3'b111 Data corresponds to this CCC type is mapped to EXT_TX_DATA_PORT_0. Default Value: 0x7

19.1.51 I3C_CORE_EXT_CMD_REG_1

Description: TID, CCC type value and Defining Byte of Vendor-specific CCC 1 Register

Address: 0x42A50168

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			Reserved		
HW Access	R		R			Reserved		
Name	DL_LSB [7:6]		TID [5:3]			Reserved [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEFINING_BYTE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CCC_TYPE [31:24]							

Bits	Name	Description
31 : 24	CCC_TYPE	Directed Read Vendor-specific CCC 1 Type. Contains the CCC type 1. Data corresponds to this CCC type is mapped to EXT_TX_DATA_PORT_1. Default Value: 0x0
23 : 16	DEFINING_BYTE	Directed Read Vendor CCC 1 Defining Byte. Contains the Defining byte of CCC type 1. Data corresponds to this Defining byte with CCC type 0 is mapped to EXT_TX_DATA_PORT_1. Default Value: 0x0
7 : 6	DL_LSB	LSB 2bits of Data Length. Contains the Last two bits of data length. This 2bits will act as a byte enable for last Data DWORD of CCC type 1 Default Value: 0x0
5 : 3	TID	Transaction ID. For a Vendor Specific CCC TID should be always 3'b111 Data corresponds to this CCC type is mapped to EXT_TX_DATA_PORT_1. Default Value: 0x7

19.1.52 I3C_CORE_EXT_CMD_REG_2

Description: TID, CCC type value and Defining Byte of Vendor-specific CCC 2 Register

Address: 0x42A5016C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			Reserved		
HW Access	R		R			Reserved		
Name	DL_LSB [7:6]		TID [5:3]			Reserved [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEFINING_BYTE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CCC_TYPE [31:24]							

Bits	Name	Description
31 : 24	CCC_TYPE	Directed Read Vendor-specific CCC 2 Type. Contains the CCC type 2. Data corresponds to this CCC type is mapped to EXT_TX_DATA_PORT_2. Default Value: 0x0
23 : 16	DEFINING_BYTE	Directed Read Vendor CCC 2 Defining Byte. Contains the Defining byte of CCC type 2. Data corresponds to this Defining byte with CCC type 0 is mapped to EXT_TX_DATA_PORT_2. Default Value: 0x0
7 : 6	DL_LSB	LSB 2bits of Data Length. Contains the Last two bits of data length. This 2bits will act as a byte enable for last Data DWORD of CCC type 2 Default Value: 0x0
5 : 3	TID	Transaction ID. For a Vendor Specific CCC TID should be always 3'b111 Data corresponds to this CCC type is mapped to EXT_TX_DATA_PORT_2. Default Value: 0x7

19.1.53 I3C_CORE_EXT_CMD_REG_3

Description: TID, CCC type value and Defining Byte of Vendor-specific CCC 3 Register

Address: 0x42A50170

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			Reserved		
HW Access	R		R			Reserved		
Name	DL_LSB [7:6]		TID [5:3]			Reserved [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEFINING_BYTE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CCC_TYPE [31:24]							

Bits	Name	Description
31 : 24	CCC_TYPE	Directed Read Vendor-specific CCC 3 Type. Contains the CCC type 3. Data corresponds to this CCC type is mapped to EXT_TX_DATA_PORT_3. Default Value: 0x0
23 : 16	DEFINING_BYTE	Directed Read Vendor CCC 3 Defining Byte. Contains the Defining byte of CCC type 3. Data corresponds to this Defining byte with CCC type 3 is mapped to EXT_TX_DATA_PORT_3. Default Value: 0x0
7 : 6	DL_LSB	LSB 2bits of Data Length. Contains the Last two bits of data length. This 2bits will act as a byte enable for last Data DWORD of CCC type 3 Default Value: 0x0
5 : 3	TID	Transaction ID. For a Vendor Specific CCC TID should be always 3'b111 Data corresponds to this CCC type is mapped to EXT_TX_DATA_PORT_3. Default Value: 0x7

19.1.54 I3C_CORE_EXT_TX_QUEUE_RESET_CTRL

Description: Individual Vendor CCC buffer reset.

Address: 0x42A50184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				RW	RW	RW	RW
Name	Reserved [7:4]				EXT_TX-_FI-FO_RST_3	EXT_TX-_FI-FO_RST_2	EXT_TX-_FI-FO_RST_1	EXT_TX-_FI-FO_RST_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	EXT_TX_FIFO_RST_3	Vendor-specific Directed Read CCC 3 Transmit Buffer Software Reset. Write '1' to this bit to exercise Vendor CCC type 3 Transmit Buffer reset. This bit is cleared automatically once the Vendor CCC type 3 Transmit Buffer reset is completed Default Value: 0x0
2	EXT_TX_FIFO_RST_2	Vendor-specific Directed Read CCC 2 Transmit Buffer Software Reset. Write '1' to this bit to exercise Vendor CCC type 2 Transmit Buffer reset. This bit is cleared automatically once the Vendor CCC type 2 Transmit Buffer reset is completed Default Value: 0x0
1	EXT_TX_FIFO_RST_1	Vendor-specific Directed Read CCC 1 Transmit Buffer Software Reset. Write '1' to this bit to exercise Vendor CCC type 1 Transmit Buffer reset. This bit is cleared automatically once the Vendor CCC type 1 Transmit Buffer reset is completed Default Value: 0x0

19.1.54 I3C_CORE_EXT_TX_QUEUE_RESET_CTRL (continued)

0	EXT_TX_FIFO_RST_0	Vendor-specific Directed Read CCC 0 Transmit Buffer Software Reset. Write '1' to this bit to exercise Vendor CCC type 0 Transmit Buffer reset. This bit is cleared automatically once the Vendor CCC type 0 Transmit Buffer reset is completed Default Value: 0x0

19.1.55 I3C_CORE_DEV_CHAR_TABLE1_LOC1

Description: Device Characteristic Table Location-1 of Device1, MSB_PROVISIONAL_ID

Address: 0x42A50200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.56 I3C_CORE_DEV_CHAR_TABLE1_LOC2

Description: Device Characteristic Table Location-2 of Device1, LSB_PROVISIONAL_ID

Address: 0x42A50204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.57 I3C_CORE_DEV_CHAR_TABLE1_LOC3

Description: Device Characteristic Table Location-3 of Device1, BCR, DCR

Address: 0x42A50208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.58 I3C_CORE_DEV_CHAR_TABLE1_LOC4

Description: Device Characteristic Table Location-4 of Device1, DEV_DYNAMIC_ADDR

Address: 0x42A5020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.59 I3C_CORE_DEV_CHAR_TABLE2_LOC1

Description: Device Characteristic Table Location-1 of Device2

Address: 0x42A50210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.60 I3C_CORE_DEV_CHAR_TABLE2_LOC2

Description: Device Characteristic Table Location-2 of Device2

Address: 0x42A50214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.61 I3C_CORE_DEV_CHAR_TABLE2_LOC3

Description: Device Characteristic Table Location-3 of Device2

Address: 0x42A50218

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.62 I3C_CORE_DEV_CHAR_TABLE2_LOC4

Description: Device Characteristic Table Location-4 of Device2

Address: 0x42A5021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.63 I3C_CORE_DEV_CHAR_TABLE3_LOC1

Description: Device Characteristic Table Location-1 of Device3

Address: 0x42A50220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.64 I3C_CORE_DEV_CHAR_TABLE3_LOC2

Description: Device Characteristic Table Location-2 of Device3

Address: 0x42A50224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.65 I3C_CORE_DEV_CHAR_TABLE3_LOC3

Description: Device Characteristic Table Location-3 of Device3

Address: 0x42A50228

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.66 I3C_CORE_DEV_CHAR_TABLE3_LOC4

Description: Device Characteristic Table Location-4 of Device3

Address: 0x42A5022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.67 I3C_CORE_DEV_CHAR_TABLE4_LOC1

Description: Device Characteristic Table Location-1 of Device4

Address: 0x42A50230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.68 I3C_CORE_DEV_CHAR_TABLE4_LOC2

Description: Device Characteristic Table Location-2 of Device4

Address: 0x42A50234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.69 I3C_CORE_DEV_CHAR_TABLE4_LOC3

Description: Device Characteristic Table Location-3 of Device4

Address: 0x42A50238

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.70 I3C_CORE_DEV_CHAR_TABLE4_LOC4

Description: Device Characteristic Table Location-4 of Device4

Address: 0x42A5023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.71 I3C_CORE_DEV_CHAR_TABLE5_LOC1

Description: Device Characteristic Table Location-1 of Device5

Address: 0x42A50240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.72 I3C_CORE_DEV_CHAR_TABLE5_LOC2

Description: Device Characteristic Table Location-4 of Device10

Address: 0x42A50244

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.73 I3C_CORE_DEV_CHAR_TABLE5_LOC3

Description: Device Characteristic Table Location-3 of Device5

Address: 0x42A50248

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.74 I3C_CORE_DEV_CHAR_TABLE5_LOC4

Description: Device Characteristic Table Location-4 of Device5

Address: 0x42A5024C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.75 I3C_CORE_DEV_CHAR_TABLE6_LOC1

Description: Device Characteristic Table Location-1 of Device6

Address: 0x42A50250

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.76 I3C_CORE_DEV_CHAR_TABLE6_LOC2

Description: Device Characteristic Table Location-2 of Device6

Address: 0x42A50254

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.77 I3C_CORE_DEV_CHAR_TABLE6_LOC3

Description: Device Characteristic Table Location-3 of Device6

Address: 0x42A50258

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.78 I3C_CORE_DEV_CHAR_TABLE6_LOC4

Description: Device Characteristic Table Location-4 of Device6

Address: 0x42A5025C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.79 I3C_CORE_DEV_CHAR_TABLE7_LOC1

Description: Device Address Table of Device3

Address: 0x42A50260

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.80 I3C_CORE_DEV_CHAR_TABLE7_LOC2

Description: Device Characteristic Table Location-2 of Device7

Address: 0x42A50264

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.81 I3C_CORE_DEV_CHAR_TABLE7_LOC3

Description: Device Characteristic Table Location-3 of Device7

Address: 0x42A50268

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.82 I3C_CORE_DEV_CHAR_TABLE7_LOC4

Description: Device Characteristic Table Location-4 of Device7

Address: 0x42A5026C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.83 I3C_CORE_DEV_CHAR_TABLE8_LOC1

Description: Device Characteristic Table Location-1 of Device8

Address: 0x42A50270

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.84 I3C_CORE_DEV_CHAR_TABLE8_LOC2

Description: Device Characteristic Table Location-2 of Device8

Address: 0x42A50274

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.85 I3C_CORE_DEV_CHAR_TABLE8_LOC3

Description: Device Characteristic Table Location-3 of Device8

Address: 0x42A50278

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.86 I3C_CORE_DEV_CHAR_TABLE8_LOC4

Description: Device Address Table of Device10

Address: 0x42A5027C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.87 I3C_CORE_DEV_CHAR_TABLE9_LOC1

Description: Device Characteristic Table Location-1 of Device9

Address: 0x42A50280

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.88 I3C_CORE_DEV_CHAR_TABLE9_LOC2

Description: Device Characteristic Table Location-2 of Device9

Address: 0x42A50284

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.89 I3C_CORE_DEV_CHAR_TABLE9_LOC3

Description: Device Characteristic Table Location-3 of Device9

Address: 0x42A50288

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.90 I3C_CORE_DEV_CHAR_TABLE9_LOC4

Description: Device Characteristic Table Location-4 of Device9

Address: 0x42A5028C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.91 I3C_CORE_DEV_CHAR_TABLE10_LOC1

Description: Device Characteristic Table Location-1 of Device10

Address: 0x42A50290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.92 I3C_CORE_DEV_CHAR_TABLE10_LOC2

Description: Device Characteristic Table Location-2 of Device10

Address: 0x42A50294

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.93 I3C_CORE_DEV_CHAR_TABLE10_LOC3

Description: Device Characteristic Table Location-3 of Device10

Address: 0x42A50298

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.94 I3C_CORE_DEV_CHAR_TABLE10_LOC4

Description: Device Characteristic Table Location-4 of Device10

Address: 0x42A5029C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.95 I3C_CORE_DEV_CHAR_TABLE11_LOC1

Description: Device Characteristic Table Location-1 of Device11

Address: 0x42A502A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MSB_PROVISIONAL_ID [31:24]							

Bits	Name	Description
31 : 0	MSB_PROVISIONAL_ID	The 32 Most Significant Bits (MSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.96 I3C_CORE_DEV_CHAR_TABLE11_LOC2

Description: 0

Address: 0x42A502A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LSB_PROVISIONAL_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	LSB_PROVISIONAL_ID	The 16 Least Significant Bits (LSBs) from the 48-bit MIPI Provisioned ID Default Value: Undefined

19.1.97 I3C_CORE_DEV_CHAR_TABLE11_LOC3

Description: Device Characteristic Table Location-3 of Device11

Address: 0x42A502A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	BCR	Bus Characteristic Register (BCR) Default Value: Undefined
7 : 0	DCR	Device Characteristic Register (DCR) Default Value: Undefined

19.1.98 I3C_CORE_DEV_CHAR_TABLE11_LOC4

Description: Device Characteristic Table Location-4 of Device11

Address: 0x42A502AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DEV_DYNAMIC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEV_DYNAMIC_ADDR	Dynamic Address assigned to the device. Default Value: Undefined

19.1.99 I3C_CORE_DEV_ADDR_TABLE_LOC1

Description: Device Address Table of Device1

Address: 0x42A502C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is an I3C Device 0x1: Device is a Legacy I2C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.99 I3C_CORE_DEV_ADDR_TABLE_LOC1 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.100 I3C_CORE_DEV_ADDR_TABLE_LOC2

Description: Device Address Table of Device2

Address: 0x42A502C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is a Legacy I2C Device 0x1: Device is an I3C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.100 I3C_CORE_DEV_ADDR_TABLE_LOC2 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.101 I3C_CORE_DEV_ADDR_TABLE_LOC3

Description: Device Address Table of Device3

Address: 0x42A502C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is a Legacy I2C Device 0x1: Device is an I3C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.101 I3C_CORE_DEV_ADDR_TABLE_LOC3 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.102 I3C_CORE_DEV_ADDR_TABLE_LOC4

Description: Device Address Table of Device4

Address: 0x42A502CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is a Legacy I2C Device 0x1: Device is an I3C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.102 I3C_CORE_DEV_ADDR_TABLE_LOC4 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.103 I3C_CORE_DEV_ADDR_TABLE_LOC5

Description: Device Address Table of Device5

Address: 0x42A502D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is a Legacy I2C Device 0x1: Device is an I3C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.103 I3C_CORE_DEV_ADDR_TABLE_LOC5 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.104 I3C_CORE_DEV_ADDR_TABLE_LOC6

Description: Device Address Table of Device6

Address: 0x42A502D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is a Legacy I2C Device 0x1: Device is an I3C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.104 I3C_CORE_DEV_ADDR_TABLE_LOC6 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.105 I3C_CORE_DEV_ADDR_TABLE_LOC7

Description: Device Address Table of Device7

Address: 0x42A502D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is a Legacy I2C Device 0x1: Device is an I3C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.105 I3C_CORE_DEV_ADDR_TABLE_LOC7 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.106 I3C_CORE_DEV_ADDR_TABLE_LOC8

Description: Device Address Table of Device8

Address: 0x42A502DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is a Legacy I2C Device 0x1: Device is an I3C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.106 I3C_CORE_DEV_ADDR_TABLE_LOC8 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.107 I3C_CORE_DEV_ADDR_TABLE_LOC9

Description: Device Address Table of Device9

Address: 0x42A502E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is a Legacy I2C Device 0x1: Device is an I3C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.107 I3C_CORE_DEV_ADDR_TABLE_LOC9 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.108 I3C_CORE_DEV_ADDR_TABLE_LOC10

Description: Device Address Table of Device10

Address: 0x42A502E4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is a Legacy I2C Device 0x1: Device is an I3C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.108 I3C_CORE_DEV_ADDR_TABLE_LOC10 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.109 I3C_CORE_DEV_ADDR_TABLE_LOC11

Description: Device Address Table of Device11

Address: 0x42A502E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	DEV_STATIC_ADDR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved		
HW Access	R	R	R	R	R	Reserved		
Name	TS	CR_RE-JECT	TIR_RE-JECT	IBI_WITH_-DATA	IBI_PEC_EN	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEV_DYNAMIC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		Reserved				
HW Access	R	R		Reserved				
Name	LEGA-CY_I2C_DE VICE	DEV_NACK_RE-TRY_CNT [30:29]		Reserved [28:24]				

Bits	Name	Description
31	LEGACY_I2C_DEVICE	Legacy I2C Device Values: 0x0: Device is a Legacy I2C Device 0x1: Device is an I3C Device Default Value: Undefined
30 : 29	DEV_NACK_RE-TRY_CNT	This field is used to set the Device NACK Retry count for the particular device. If the Device NACKs for the device address, the block automatically retries the transfer until this count expires. If the Target NACKs for the mentioned number of retries, then the block generates an error response and moves to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: => Retry Model for Direct GET CCC Commands => The incoming TIR-IBI matches with the Target address initated by the Active Controller Default Value: Undefined
23 : 16	DEV_DYNAMIC_ADDR	Device Dynamic Address with parity. This field consists of a Dynamic Address and a Parity Bit. The LSBs [22:16] consist of the Dynamic Address to be assigned for the winning I3C device when using ENTDAA command. The MSB [23] is the odd parity of the 7-bit Dynamic Address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16]) Default Value: Undefined

19.1.109 I3C_CORE_DEV_ADDR_TABLE_LOC11 (continued)

15	TS	Marker for Timestamping IBI for specific device. Whether IBI was timestamped or not is provided in IBI Status Descriptor. Default Value: Undefined
14	CR_REJECT	In-Band Controller Request Reject field is used to control, per device, whether to accept Controller Request from Devices. Values: 0x0: Accept: ACK the Controller Request 0x1: Reject: NACK the Controller Request and send auto disable CCC. Default Value: Undefined
13	TIR_REJECT	In-Band Target Interrupt Request Reject This field is used when operating as the Active Controller to control, per device, whether to accept Target Interrupt request from this device. Values: 0x0: Accept: ACK the TIR 0x1: Reject: NACK the TIR and send auto disable CCC. Default Value: Undefined
12	IBI_WITH_DATA	Mandatory one or more data bytes follow the accepted IBI from the device. Data byte continuation is indicated by T-Bit. Values: 0x0: IBI Without Mandatory Byte 0x1: IBI with one or more Mandatory Bytes. Default Value: Undefined
11	IBI_PEC_EN	Packet Error Check enabled for accepted IBI from the device. PEC byte is appended at the end of IBI data from the device. This bit controls whether PEC check should be performed for IBI data from device. This bit also controls whether PEC byte has to be send for auto disable CCC when the block NACKs the IBI. Values: 0x0: Packet Error Check disabled for IBI 0x1: Packet Error Check enabled for IBI Default Value: Undefined
6 : 0	DEV_STATIC_ADDR	Device Static Address. Default Value: Undefined

19.1.110 I3C_CTRL

Description: I3C Block Control

Address: 0x42A50400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	I3C Block Pre-Enable When disabled, all write accesses to the I3C configuration registeres are ignored. Enable this preior to starting the configuration of the I3C block. Values: 0x0: Disable the I3C block 0x1: Pre-Enable the I3C block Default Value: 0

19.1.111 I3C_TGT_STATUS

Description: This register provides additional status information when functioning as a Target.

Address: 0x42A50418

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							WAKEUP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [15:9]							I2C_GLITCH_FIL-TER_EN

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	IBI_PAYLOAD_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	IBI_PAYLOAD_SIZE	IBI Payload Size This field provides the application with the expected IBI Payload Size as configured by in the I3C bus by the Active Controller via the SETMRL CCC. Default Value: 1
8	I2C_GLITCH_FILTER_EN	Default Value: 1
0	WAKEUP	Target wakeup signal This field is only valid when functioning as a Target. Default Value: 0

19.1.112 I3C_CCC_GETSTATUS

Description: This register provides additional information on GETSTATUS CCCs received when functioning as a Target.

Address: 0x42A50424

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				PENDING_INT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [31:26]						ACT_MODE [25:24]	

Bits	Name	Description
25 : 24	ACT_MODE	Target activity mode for GETSTATUS CCC. This bit is only valid when functioning as a Target. The value is propagated to the I3C Target and providing in response to an incoming GETSTATUS CCC with Format 1 (LSB bits 7:6). Default Value: 0
19 : 16	PENDING_INT	Pending interrupt info for GETSTATUS CCC. This bit is only valid when functioning as a Target. The value is propagated to the I3C Target and providing in response to an incoming GETSTATUS CCC with Format 1 (LSB bits 3:0). Default Value: 0

19.1.113 I3C_TIMING_CNT_CTRL

Description: Controls the Counter used for timestamping I3C-relevant events, especially when communicating with Asynchronous Timing Control Mode 0 enabled.

Address: 0x42A5042C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW1C	Reserved					
HW Access	R	RW	Reserved					
Name	CNT_EN-ABLE	CNT_RE-SET	Reserved [29:24]					

Bits	Name	Description
31	CNT_ENABLE	Enable the counter Default Value: 0
30	CNT_RESET	Resets the counter. This bit is automatically set to 0 after the reset is applied. Default Value: 0

19.1.114 I3C_TIMING_CNT0

Description: Most Significant Bits of the Counter

Address: 0x42A50430

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TIMING_COUNTER_MSB [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TIMING_COUNTER_MSB [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TIMING_COUNTER_MSB [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TIMING_COUNTER_MSB [31:24]							

Bits	Name	Description
31 : 0	TIMING_COUNTER_MSB	Most-Significant Bits of the timing counter used for I3C timing control. In Target mode, these bits shall be ignored because the counter is only 16 bit. Default Value: 0

19.1.115 I3C_TIMING_CNT1

Description: Least Significant Bits of the Counter

Address: 0x42A50434

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TIMING_COUNTER_LSB [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TIMING_COUNTER_LSB [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TIMING_COUNTER_LSB [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TIMING_COUNTER_LSB [31:24]							

Bits	Name	Description
31 : 0	TIMING_COUNTER_LSB	Least-Significant Bits of the timing counter used for I3C timing control In Target mode, bits 31:16 shall be ignored because the counter is only 16 bit. Default Value: 0

20 Pulse Density Modulation- Pulse Code Modulation (PDM-PCM) Converter registers

This section discusses the PDM- PCM converter registers. It lists all the registers in mapping tables, in address order.

20.1 Register details

Register name	Address	Description
PDM0_CTL	0x44400000	Control
PDM0_CTL_CLR	0x44400004	Control clear
PDM0_CTL_SET	0x44400008	Control set
PDM0_CLOCK_CTL	0x44400010	Clock control
PDM0_ROUTE_CTL	0x44400020	Route control
PDM0_TEST_CTL	0x44400030	Test control
PDM0_FIR0_COEFF0	0x44400100	FIR 0 coefficients 0
PDM0_FIR0_COEFF1	0x44400104	FIR 0 coefficients 1
PDM0_FIR0_COEFF2	0x44400108	FIR 0 coefficients 2
PDM0_FIR0_COEFF3	0x4440010C	FIR 0 coefficients 3
PDM0_FIR0_COEFF4	0x44400110	FIR 0 coefficients 4
PDM0_FIR0_COEFF5	0x44400114	FIR 0 coefficients 5
PDM0_FIR0_COEFF6	0x44400118	FIR 0 coefficients 6
PDM0_FIR0_COEFF7	0x4440011C	FIR 0 coefficients 7
PDM0_FIR1_COEFF0	0x44400140	FIR 1 coefficients 0
PDM0_FIR1_COEFF1	0x44400144	FIR 1 coefficients 1
PDM0_FIR1_COEFF2	0x44400148	FIR 1 coefficients 2
PDM0_FIR1_COEFF3	0x4440014C	FIR 1 coefficients 3
PDM0_FIR1_COEFF4	0x44400150	FIR 1 coefficients 4
PDM0_FIR1_COEFF5	0x44400154	FIR 1 coefficients 5
PDM0_FIR1_COEFF6	0x44400158	FIR 1 coefficients 6
PDM0_FIR1_COEFF7	0x4440015C	FIR 1 coefficients 7
PDM0_FIR1_COEFF8	0x44400160	FIR 1 coefficients 8
PDM0_FIR1_COEFF9	0x44400164	FIR 1 coefficients 9
PDM0_FIR1_COEFF10	0x44400168	FIR 1 coefficients 10
PDM0_FIR1_COEFF11	0x4440016C	FIR 1 coefficients 11
PDM0_FIR1_COEFF12	0x44400170	FIR 1 coefficients 12
PDM0_FIR1_COEFF13	0x44400174	FIR 1 coefficients 13
PDM0_CH0_CTL	0x44408000	Control
PDM0_CH0_IF_CTL	0x44408010	Interface control
PDM0_CH0_CIC_CTL	0x44408014	CIC control

Pulse Density Modulation- Pulse Code Modulation (PDM-PCM) Converter registers

Register name	Address	Description
PDM0_CH0_FIR0_CTL	0x44408018	FIR 0 control
PDM0_CH0_FIR1_CTL	0x4440801C	FIR 1 control
PDM0_CH0_DC_BLOCK_CTL	0x44408020	DC block control
PDM0_CH0_RX_FIFO_CTL	0x44408080	RX FIFO control
PDM0_CH0_RX_FIFO_STATUS	0x44408084	RX FIFO status
PDM0_CH0_RX_FIFO_RD	0x44408088	RX FIFO read
PDM0_CH0_RX_FIFO_RD_SILENT	0x4440808C	RX FIFO silent read
PDM0_CH0_INTR_RX	0x444080C0	Interrupt
PDM0_CH0_INTR_RX_SET	0x444080C4	Interrupt set
PDM0_CH0_INTR_RX_MASK	0x444080C8	Interrupt mask
PDM0_CH0_INTR_RX_MASKED	0x444080CC	Interrupt masked
PDM0_CH1_CTL	0x44408100	Control. See PDM0_CH0_CTL for the details of bit fields.
PDM0_CH1_IF_CTL	0x44408110	Interface control. See PDM0_CH0_IF_CTL for the details of bit fields.
PDM0_CH1_CIC_CTL	0x44408114	CIC control. See PDM0_CH0_CIC_CTL for the details of bit fields.
PDM0_CH1_FIR0_CTL	0x44408118	FIR 0 control. See PDM0_CH0_FIR0_CTL for the details of bit fields.
PDM0_CH1_FIR1_CTL	0x4440811C	FIR 1 control. See PDM0_CH0_FIR1_CTL for the details of bit fields.
PDM0_CH1_DC_BLOCK_CTL	0x44408120	DC block control. See PDM0_CH0_DC_BLOCK_CTL for the details of bit fields.
PDM0_CH1_RX_FIFO_CTL	0x44408180	RX FIFO control. See PDM0_CH0_RX_FIFO_CTL for the details of bit fields.
PDM0_CH1_RX_FIFO_STATUS	0x44408184	RX FIFO status. See PDM0_CH0_RX_FIFO_STATUS for the details of bit fields.
PDM0_CH1_RX_FIFO_RD	0x44408188	RX FIFO read. See PDM0_CH0_RX_FIFO_RD for the details of bit fields.
PDM0_CH1_RX_FIFO_RD_SILENT	0x4440818C	RX FIFO silent read. See PDM0_CH0_RX_FIFO_RD_SILENT for the details of bit fields.
PDM0_CH1_INTR_RX	0x444081C0	Interrupt. See PDM0_CH0_INTR_RX for the details of bit fields.
PDM0_CH1_INTR_RX_SET	0x444081C4	Interrupt set. See PDM0_CH0_INTR_RX_SET for the details of bit fields.
PDM0_CH1_INTR_RX_MASK	0x444081C8	Interrupt mask. See PDM0_CH0_INTR_RX_MASK for the details of bit fields.
PDM0_CH1_INTR_RX_MASKED	0x444081CC	Interrupt masked. See PDM0_CH0_INTR_RX_MASKED for the details of bit fields.
PDM0_CH2_CTL	0x44408200	Control. See PDM0_CH0_CTL for the details of bit fields.
PDM0_CH2_IF_CTL	0x44408210	Interface control. See PDM0_CH0_IF_CTL for the details of bit fields.

Pulse Density Modulation- Pulse Code Modulation (PDM-PCM) Converter registers

Register name	Address	Description
PDM0_CH2_CIC_CTL	0x44408214	CIC control. See PDM0_CH0_CIC_CTL for the details of bit fields.
PDM0_CH2_FIR0_CTL	0x44408218	FIR 0 control. See PDM0_CH0_FIR0_CTL for the details of bit fields.
PDM0_CH2_FIR1_CTL	0x4440821C	FIR 1 control. See PDM0_CH0_FIR1_CTL for the details of bit fields.
PDM0_CH2_DC_BLOCK_CTL	0x44408220	DC block control. See PDM0_CH0_DC_BLOCK_CTL for the details of bit fields.
PDM0_CH2_RX_FIFO_CTL	0x44408280	RX FIFO control. See PDM0_CH0_RX_FIFO_CTL for the details of bit fields.
PDM0_CH2_RX_FIFO_STATUS	0x44408284	RX FIFO status. See PDM0_CH0_RX_FIFO_STATUS for the details of bit fields.
PDM0_CH2_RX_FIFO_RD	0x44408288	RX FIFO read. See PDM0_CH0_RX_FIFO_RD for the details of bit fields.
PDM0_CH2_RX_FIFO_RD_SILENT	0x4440828C	RX FIFO silent read. See PDM0_CH0_RX_FIFO_RD_SILENT for the details of bit fields.
PDM0_CH2_INTR_RX	0x444082C0	Interrupt. See PDM0_CH0_INTR_RX for the details of bit fields.
PDM0_CH2_INTR_RX_SET	0x444082C4	Interrupt set. See PDM0_CH0_INTR_RX_SET for the details of bit fields.
PDM0_CH2_INTR_RX_MASK	0x444082C8	Interrupt mask. See PDM0_CH0_INTR_RX_MASK for the details of bit fields.
PDM0_CH2_INTR_RX_MASKED	0x444082CC	Interrupt masked. See PDM0_CH0_INTR_RX_MASKED for the details of bit fields.
PDM0_CH3_CTL	0x44408300	Control. See PDM0_CH0_CTL for the details of bit fields.
PDM0_CH3_IF_CTL	0x44408310	Interface control. See PDM0_CH0_IF_CTL for the details of bit fields.
PDM0_CH3_CIC_CTL	0x44408314	CIC control. See PDM0_CH0_CIC_CTL for the details of bit fields.
PDM0_CH3_FIR0_CTL	0x44408318	FIR 0 control. See PDM0_CH0_FIR0_CTL for the details of bit fields.
PDM0_CH3_FIR1_CTL	0x4440831C	FIR 1 control. See PDM0_CH0_FIR1_CTL for the details of bit fields.
PDM0_CH3_DC_BLOCK_CTL	0x44408320	DC block control. See PDM0_CH0_DC_BLOCK_CTL for the details of bit fields.
PDM0_CH3_RX_FIFO_CTL	0x44408380	RX FIFO control. See PDM0_CH0_RX_FIFO_CTL for the details of bit fields.
PDM0_CH3_RX_FIFO_STATUS	0x44408384	RX FIFO status. See PDM0_CH0_RX_FIFO_STATUS for the details of bit fields.
PDM0_CH3_RX_FIFO_RD	0x44408388	RX FIFO read. See PDM0_CH0_RX_FIFO_RD for the details of bit fields.
PDM0_CH3_RX_FIFO_RD_SILENT	0x4440838C	RX FIFO silent read. See PDM0_CH0_RX_FIFO_RD_SILENT for the details of bit fields.

Pulse Density Modulation- Pulse Code Modulation (PDM-PCM) Converter registers

Register name	Address	Description
PDM0_CH3_INTR_RX	0x444083C0	Interrupt. See PDM0_CH0_INTR_RX for the details of bit fields.
PDM0_CH3_INTR_RX_SET	0x444083C4	Interrupt set. See PDM0_CH0_INTR_RX_SET for the details of bit fields.
PDM0_CH3_INTR_RX_MASK	0x444083C8	Interrupt mask. See PDM0_CH0_INTR_RX_MASK for the details of bit fields.
PDM0_CH3_INTR_RX_MASKED	0x444083CC	Interrupt masked. See PDM0_CH0_INTR_RX_MASKED for the details of bit fields.
PDM0_CH4_CTL	0x44408400	Control. See PDM0_CH0_CTL for the details of bit fields.
PDM0_CH4_IF_CTL	0x44408410	Interface control. See PDM0_CH0_IF_CTL for the details of bit fields.
PDM0_CH4_CIC_CTL	0x44408414	CIC control. See PDM0_CH0_CIC_CTL for the details of bit fields.
PDM0_CH4_FIR0_CTL	0x44408418	FIR 0 control. See PDM0_CH0_FIR0_CTL for the details of bit fields.
PDM0_CH4_FIR1_CTL	0x4440841C	FIR 1 control. See PDM0_CH0_FIR1_CTL for the details of bit fields.
PDM0_CH4_DC_BLOCK_CTL	0x44408420	DC block control. See PDM0_CH0_DC_BLOCK_CTL for the details of bit fields.
PDM0_CH4_RX_FIFO_CTL	0x44408480	RX FIFO control. See PDM0_CH0_RX_FIFO_CTL for the details of bit fields.
PDM0_CH4_RX_FIFO_STATUS	0x44408484	RX FIFO status. See PDM0_CH0_RX_FIFO_STATUS for the details of bit fields.
PDM0_CH4_RX_FIFO_RD	0x44408488	RX FIFO read. See PDM0_CH0_RX_FIFO_RD for the details of bit fields.
PDM0_CH4_RX_FIFO_RD_SILENT	0x4440848C	RX FIFO silent read. See PDM0_CH0_RX_FIFO_RD_SILENT for the details of bit fields.
PDM0_CH4_INTR_RX	0x444084C0	Interrupt. See PDM0_CH0_INTR_RX for the details of bit fields.
PDM0_CH4_INTR_RX_SET	0x444084C4	Interrupt set. See PDM0_CH0_INTR_RX_SET for the details of bit fields.
PDM0_CH4_INTR_RX_MASK	0x444084C8	Interrupt mask. See PDM0_CH0_INTR_RX_MASK for the details of bit fields.
PDM0_CH4_INTR_RX_MASKED	0x444084CC	Interrupt masked. See PDM0_CH0_INTR_RX_MASKED for the details of bit fields.
PDM0_CH5_CTL	0x44408500	Control. See PDM0_CH0_CTL for the details of bit fields.
PDM0_CH5_IF_CTL	0x44408510	Interface control. See PDM0_CH0_IF_CTL for the details of bit fields.
PDM0_CH5_CIC_CTL	0x44408514	CIC control. See PDM0_CH0_CIC_CTL for the details of bit fields.
PDM0_CH5_FIR0_CTL	0x44408518	FIR 0 control. See PDM0_CH0_FIR0_CTL for the details of bit fields.

Pulse Density Modulation- Pulse Code Modulation (PDM-PCM) Converter registers

Register name	Address	Description
PDM0_CH5_FIR1_CTL	0x4440851C	FIR 1 control. See PDM0_CH0_FIR1_CTL for the details of bit fields.
PDM0_CH5_DC_BLOCK_CTL	0x44408520	DC block control. See PDM0_CH0_DC_BLOCK_CTL for the details of bit fields.
PDM0_CH5_RX_FIFO_CTL	0x44408580	RX FIFO control. See PDM0_CH0_RX_FIFO_CTL for the details of bit fields.
PDM0_CH5_RX_FIFO_STATUS	0x44408584	RX FIFO status. See PDM0_CH0_RX_FIFO_STATUS for the details of bit fields.
PDM0_CH5_RX_FIFO_RD	0x44408588	RX FIFO read. See PDM0_CH0_RX_FIFO_RD for the details of bit fields.
PDM0_CH5_RX_FIFO_RD_SILENT	0x4440858C	RX FIFO silent read. See PDM0_CH0_RX_FIFO_RD_SILENT for the details of bit fields.
PDM0_CH5_INTR_RX	0x444085C0	Interrupt. See PDM0_CH0_INTR_RX for the details of bit fields.
PDM0_CH5_INTR_RX_SET	0x444085C4	Interrupt set. See PDM0_CH0_INTR_RX_SET for the details of bit fields.
PDM0_CH5_INTR_RX_MASK	0x444085C8	Interrupt mask. See PDM0_CH0_INTR_RX_MASK for the details of bit fields.
PDM0_CH5_INTR_RX_MASKED	0x444085CC	Interrupt masked. See PDM0_CH0_INTR_RX_MASKED for the details of bit fields.

20.1.1 PDM0_CTL

Description: Control

Address: 0x44400000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		RW					
Name	Reserved [7:6]		ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	ACTIVE	Activate functionality (1 bit for each channel): '0': Reception disabled. The FIFO_OVERFLOW interrupt cause will not be activated. '1': Reception enabled. The FIFO_OVERFLOW interrupt may be activated (when an overflow event occurs). Note: This functionality is intended for startup purposes. Typically, the startup sequence is as follows: - global registers CLOCK_CTL, ROUTE_CTL, TEST_CTL, FIR*_COEFF* are initialized - One or more structures are enabled (structure specific CTL.ENABLED register field is set to '1'). - The structures are initialized (structure specific MMIO registers are written). - The structures are activated. This last step is performed by writing the CTL or CTL_SET MMIO registers, or on a rising edge ('0' to '1' transition) of a receiver's "tr_activate" input trigger. Note: on a rising edge ('0' to '1' transition) of a receiver's "tr_activate" input trigger, its associated CTL.ACTIVE field is set to '1'. This allows HW based synchronization of PDM receiver activation based on system triggers. Implementation note: the trigger is synchronized on the receiver clock with the receiver reset (this requires the receiver to be enabled; i.e. CTL.ENABLED is '1'). Note: if CTL_CLR.ACTIVE[i] is written to '1' at the same time a rising edge of "tr_activate[i]" occurs, CTL.ACTIVE[i] is set to '1' (i.e. trigger takes precedence). Default Value: 0

20.1.2 PDM0_CTL_CLR

Description: Control clear

Address: 0x44400004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW1C					
HW Access	Reserved		A					
Name	Reserved [7:6]		ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	ACTIVE	Activate functionality: '0': No effect. '1': Bit is set to '0'. Default Value: 0

20.1.3 PDM0_CTL_SET

Description: Control set

Address: 0x44400008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW1S					
HW Access	Reserved		A					
Name	Reserved [7:6]		ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	ACTIVE	Activate functionality: '0': No effect. '1': Bit is set to '1'. Default Value: 0

20.1.4 PDM0_CLOCK_CTL

Description: Clock control

Address: 0x44400010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLOCK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						CLOCK_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							HALVE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	HALVE	Halve rate sampling: '0': Full rate sampling. The PDM interface clock pdm_clk is as specified by CLOCK_DIV[]. Each captured PDM value is provided once to the CIC filter. '1': Halve rate sampling. The PDM interface clock clk_pdm is as specified by CLOCK_DIV[] divided by two (halve the frequency). Each PDM value is captured twice and provided twice to the CIC filter; i.e. the PDM value is repeated. Note: this field is provided to dynamically change the digital microphone's clock (pdm_clk) without affecting the PDM sample frequency towards the CIC filter. Halving the microphone clock results in lower system power consumption, but does lower audio quality. Default Value: 0 **0x0: FULL :** **0x1: HALVE :**
9 : 8	CLOCK_SEL	Interface clock clk_if selection: "0": SRSS clock clk_if_srss. "1": IOSS data input signal "pdm_data[0]". "2": IOSS data input signal "pdm_data[1]". "3": undefined. Note: when a data input signal is used as a clock source, it cannot be used as a data line. Note: the application is always required to program this field to a value different from the default. Default Value: 3 **0x0: SEL_SRSS_CLOCK :**

20.1.4 PDM0_CLOCK_CTL (continued)

		0x1: SEL_PDM_DATA0 :
		0x2: SEL_PDM_DATA1 :
		0x3: SEL_OR :
7 : 0	CLOCK_DIV	PDM interface clock divider (legal range [3, 255]). The PDM interface clock clk_pdm ("pdm_clk[]" output signals) is defined as pdm_clk = clk_if / (CLOCK_DIV + 1); i.e. each PDM interface clock cycle equals CLOCK_DIV + 1 clk_if clock cycles. CLOCK_DIV should be set to an odd value ([3, 5, ..., 255]), to ensure a 50/50% duty cycle PDM interface clock pdm_clk. "0-2": Illegal value. "3": pdm_clk frequency is 1/4 clk_if frequency (1 pdm_clk cycle consists of 4 clk_if cycles). "4": pdm_clk frequency is 1/5 clk_if frequency. Note: results in a non 50/50% duty cycle pdm_-clk). ... "255": pdm_clk frequency is 1/256 clk_if frequency. Default Value: 7
		0x3: DIV_BY_4 :
		0x4: DIV_BY_5 :
		0xff: DIV_BY_256 :

20.1.5 PDM0_ROUTE_CTL

Description: Route control

Address: 0x44400020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		DATA_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	DATA_SEL	Specifies which IOSS data input signal "pdm_data[]" is routed to a specific PDM receiver. Each PDM receiver j has a dedicated 1-bit control field: PDM receiver j uses DATA_SEL[j]. The 1-bit field DATA_SEL[j] specification is as follows: '0': PDM receiver j uses data input signal "pdm_data[j]". '1': PDM receiver j uses data input signal "pdm_data[j ^ 1]" (the lower bit of the index is inverted). Routing the same data input signal to two PDM receivers allows for: - A single stereo digital microphone. - Two (mono) digital microphones that share a data line. E.g., if DATA_SEL is 0b00000010, PDM receivers 0 and 1 BOTH use "pdm_data[0]". Default Value: 0

20.1.6 PDM0_TEST_CTL

Description: Test control

Address: 0x44400030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DRIVE_DELAY_HI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DRIVE_DELAY_LO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW		RW	
HW Access	R				R		R	
Name	AUDIO_FREQ_DIV [23:20]				MODE_LO [19:18]		MODE_HI [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CH_ENABLED [31:24]							

Bits	Name	Description
31 : 24	CH_ENABLED	Pattern generator enable (1 bit for each channel): '0' : disabled, the channel input is taken as normal from external pin pdm_data_in '1' : enabled, the channel input is taken from the pattern generator Note: the pattern generator output is routed to pdm_data_out for testing purposes Note: when all channels are disabled the pattern generator is switched off Default Value: 0
23 : 20	AUDIO_FREQ_DIV	Frequency division factor (legal range [3, 13]) to obtain audio frequency from the PDM clock frequency. This field determines the frequency of the sine wave generated by the pattern generator when MODE=3. The formula is below: Sine wave Frequency = PDM clock frequency / 2p*2^(AUDIO_FREQ_DIV) Example: when PDM clock frequency = 3.072 MHz the audio frequencies obtained for the various values of AUDIO_FREQ_DIV are shown below: "3" : 61.115 kHz "4" : 30.558 kHz "5" : 15.279 kHz "6" : 7.639 kHz "7" : 3.820 kHz "8" : 1.910 kHz "9" : 955 Hz "10" : 477 Hz "11" : 239 Hz "12" : 119 Hz "13" : 60 Hz Default Value: 7

20.1.6 PDM0_TEST_CTL (continued)

		0x3: DIV_PDM_FREQ_BY_2PI_x_8 : Example: 3.072 MHz/(2p*8) = 61.115 kHz **0x4: DIV_PDM_FREQ_BY_2PI_x_16 :** Example: 3.072 MHz/(2p*16) = 30.558 kHz **0xd: DIV_PDM_FREQ_BY_2PI_x_8192 :** Example: 3.072 MHz/(2p*8192) = 60 Hz
19 : 18	MODE_LO	Pattern generator mode on the low phase of the PDM interface clock. This field specifies the type of pattern driven by the generator: "0": constant 0's "1": constant 1's "2": alternating 0's and 1's (clock pattern) "3": sine wave Default Value: 3 **0x0: CONSTANT_0 :** **0x1: CONSTANT_1 :** **0x2: ALTERNATING :** **0x3: SINUSOID :**
17 : 16	MODE_HI	Pattern generator mode on the high phase of the PDM interface clock. This field specifies the type of PDM pattern driven by the generator: "0": constant 0's "1": constant 1's "2": alternating 0's and 1's (clock pattern) "3": sinusoid Default Value: 3 **0x0: CONSTANT_0 :** **0x1: CONSTANT_1 :** **0x2: ALTERNATING :** **0x3: SINUSOID :**
15 : 8	DRIVE_DELAY_LO	Interface drive delay on the low phase of the PDM interface clock. This field specifies when a PDM value is driven expressed in clk_if clock cycles. DRIVE_DELAY should be set in the range [0, IF_CTL.CLOCK_DIV]: "0": Drive PDM value 1 clk_if cycle after the rising edge of clk_pdm. "1": Drive PDM value 2 clk_if cycles after the rising edge of clk_pdm. ... "255": Drive PDM value 256 clk_if cycles after the rising edge of clk_pdm. Note: To drive on the falling edge of the PDM interface clock clk_pdm, DRIVE_DELAY should be set to IF_CTL.CLOCK_DIV/2. To drive on the rising edge of clk_pdm, DRIVE_DELAY should be set to IF_CTL.CLOCK_DIV. Default Value: 4 **0x0: DELAY_1 :** **0x1: DELAY_2 :**

20.1.6 PDM0_TEST_CTL (continued)

		0xff: DELAY_256 :
7 : 0	DRIVE_DELAY_HI	Interface drive delay on the high phase of the PDM interface clock. This field specifies when a PDM value is driven expressed in clk_if clock cycles. DRIVE_DELAY should be set in the range [0, IF_CTL.CLOCK_DIV]: "0": Drive PDM value 1 clk_if cycle after the rising edge of clk_pdm. "1": Drive PDM value 2 clk_if cycles after the rising edge of clk_pdm. ... "255": Drive PDM value 256 clk_if cycles after the rising edge of clk_pdm. Note: To drive on the falling edge of the PDM interface clock clk_pdm, DRIVE_DELAY should be set to IF_CTL.CLOCK_DIV/2. To drive on the rising edge of clk_pdm, DRIVE_DELAY should be set to IF_CTL.CLOCK_DIV. Default Value: 0 **0x0: DELAY_1 :** **0x1: DELAY_2 :** **0xff: DELAY_256 :**

20.1.7 PDM0_FIR0_COEFF0

Description: FIR 0 coefficients 0

Address: 0x44400100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 1 and 28 coefficient. Default Value: Undefined
13 : 0	DATA0	Filter taps 0 and 29 coefficient. Default Value: Undefined

20.1.8 PDM0_FIR0_COEFF1

Description: FIR 0 coefficients 1

Address: 0x44400104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 3 and 26 coefficient. Default Value: Undefined
13 : 0	DATA0	Filter taps 2 and 27 coefficient. Default Value: Undefined

20.1.9 PDM0_FIR0_COEFF2

Description: FIR 0 coefficients 2

Address: 0x44400108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 5 and 24 coefficient. Default Value: Undefined
13 : 0	DATA0	Filter taps 4 and 25 coefficient. Default Value: Undefined

20.1.10 PDM0_FIR0_COEFF3

Description: FIR 0 coefficients 3

Address: 0x4440010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 7 and 22 coefficient. Default Value: Undefined
13 : 0	DATA0	Filter taps 6 and 23 coefficient. Default Value: Undefined

20.1.11 PDM0_FIR0_COEFF4

Description: FIR 0 coefficients 4

Address: 0x44400110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 9 and 20 coefficient. Default Value: Undefined
13 : 0	DATA0	Filter taps 8 and 21 coefficient. Default Value: Undefined

20.1.12 PDM0_FIR0_COEFF5

Description: FIR 0 coefficients 5

Address: 0x44400114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 11 and 18 coefficient. Default Value: Undefined
13 : 0	DATA0	Filter taps 10 and 19 coefficient. Default Value: Undefined

20.1.13 PDM0_FIR0_COEFF6

Description: FIR 0 coefficients 6

Address: 0x44400118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 13 and 16 coefficient. Default Value: Undefined
13 : 0	DATA0	Filter taps 12 and 17 coefficient. Default Value: Undefined

20.1.14 PDM0_FIR0_COEFF7

Description: FIR 0 coefficients 7

Address: 0x4440011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter tap 15 coefficient. Default Value: Undefined
13 : 0	DATA0	Filter tap 14 coefficient. Default Value: Undefined

20.1.15 PDM0_FIR1_COEFF0

Description: FIR 1 coefficients 0

Address: 0x44400140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 1 and 53 coefficient (default value 21). Default Value: 0x0015
13 : 0	DATA0	Filter taps 0 and 54 coefficient (default value -2). Default Value: 0x3FFE

20.1.16 PDM0_FIR1_COEFF1

Description: FIR 1 coefficients 1

Address: 0x44400144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 3 and 51 coefficient (default value -17). Default Value: 0x3FEF
13 : 0	DATA0	Filter taps 2 and 52 coefficient (default value 26). Default Value: 0x001A

20.1.17 PDM0_FIR1_COEFF2

Description: FIR 1 coefficients 2

Address: 0x44400148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 5 and 49 coefficient (default value 25). Default Value: 0x0019
13 : 0	DATA0	Filter taps 4 and 50 coefficient (default value -41). Default Value: 0x3FD7

20.1.18 PDM0_FIR1_COEFF3

Description: FIR 1 coefficients 3

Address: 0x4440014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 7 and 47 coefficient (default value -33). Default Value: 0x3FDF
13 : 0	DATA0	Filter taps 6 and 48 coefficient (default value 68). Default Value: 0x0044

20.1.19 PDM0_FIR1_COEFF4

Description: FIR 1 coefficients 4

Address: 0x44400150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 9 and 45 coefficient (default value 41). Default Value: 0x0029
13 : 0	DATA0	Filter taps 8 and 46 coefficient (default value -107). Default Value: 0x3F95

20.1.20 PDM0_FIR1_COEFF5

Description: FIR 1 coefficients 5

Address: 0x44400154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 11 and 43 coefficient (default value -48). Default Value: 0x3FD0
13 : 0	DATA0	Filter taps 10 and 44 coefficient (default value 160). Default Value: 0x00A0

20.1.21 PDM0_FIR1_COEFF6

Description: FIR 1 coefficients 6

Address: 0x44400158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 13 and 41 coefficient (default value 54). Default Value: 0x0036
13 : 0	DATA0	Filter taps 12 and 42 coefficient (default value -230). Default Value: 0x3F1A

20.1.22 PDM0_FIR1_COEFF7

Description: FIR 1 coefficients 7

Address: 0x4440015C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 15 and 39 coefficient (default value -56). Default Value: 0x3FC8
13 : 0	DATA0	Filter taps 14 and 40 coefficient (default value 325). Default Value: 0x0145

20.1.23 PDM0_FIR1_COEFF8

Description: FIR 1 coefficients 8

Address: 0x44400160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 17 and 37 coefficient (default value 51). Default Value: 0x0033
13 : 0	DATA0	Filter taps 16 and 38 coefficient (default value -453). Default Value: 0x3E3B

20.1.24 PDM0_FIR1_COEFF9

Description: FIR 1 coefficients 9

Address: 0x44400164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 19 and 35 coefficient (default value -31). Default Value: 0x3FE1
13 : 0	DATA0	Filter taps 18 and 36 coefficient (default value 631). Default Value: 0x0277

20.1.25 PDM0_FIR1_COEFF10

Description: FIR 1 coefficients 10

Address: 0x44400168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 21 and 33 coefficient (default value -21). Default Value: 0x3FEB
13 : 0	DATA0	Filter taps 20 and 34 coefficient (default value -894). Default Value: 0x3C82

20.1.26 PDM0_FIR1_COEFF11

Description: FIR 1 coefficients 11

Address: 0x4440016C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 23 and 31 coefficient (default value 172). Default Value: 0x00AC
13 : 0	DATA0	Filter taps 22 and 32 coefficient (default value 1326). Default Value: 0x052E

20.1.27 PDM0_FIR1_COEFF12

Description: FIR 1 coefficients 12

Address: 0x44400170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 25 and 29 coefficient (default value -770). Default Value: 0x3CFE
13 : 0	DATA0	Filter taps 24 and 30 coefficient (default value -2191). Default Value: 0x3771

20.1.28 PDM0_FIR1_COEFF13

Description: FIR 1 coefficients 13

Address: 0x44400174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		DATA0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		DATA1 [29:24]					

Bits	Name	Description
29 : 16	DATA1	Filter taps 27 (center tap) coefficient (default value 8191). Default Value: 0x1FFF
13 : 0	DATA0	Filter taps 26 and 28 coefficient (default value 4859). Default Value: 0x12FB

20.1.29 PDM0_CH0_CTL

Description: Control

Address: 0x44408000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				WORD_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							WORD_SIGN_EXTEND

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	Receiver enable: '0': Disabled. If a receiver is disabled, all non-retained MMIO registers (e.g. the RX_FIFO_STATUS and INTR_RX registers) have their fields reset to their default value. '1': Enabled. Note: when all receivers are disabled, the SRAMs are driven into low power mode, if supported by the SRAM. When exiting such low power mode software needs to allow for a certain power up time before SRAM can be used, i.e. before ACTIVE can be asserted. The power up time is equivalent to the system SRAM power up time specified in the CPUSS.RAM_PWR_DELAY_CTL register. Default Value: 0
8	WORD_SIGN_EXTEND	Word extension: '0': zero extension. '1': sign extension. Default Value: 1 **0x0: ZERO_EXTEND :** **0x1: SIGN_EXTEND :**

20.1.29 PDM0_CH0_CTL (continued)

3 : 0	WORD_SIZE	PCM word size: "0": 8 bit. "1": 10 bit. "2": 12 bit. "3": 14 bit. "4": 16 bit. "5": 18 bit. "6": 20 bit. "7": 24 bit. "8": 32 bit. "9"-"15": Undefined. Default Value: 0 **0x0: SIZE_8 :** **0x1: SIZE_10 :** **0x2: SIZE_12 :** **0x3: SIZE_14 :** **0x4: SIZE_16 :** **0x5: SIZE_18 :** **0x6: SIZE_20 :** **0x7: SIZE_24 :** **0x8: SIZE_32 :**

20.1.30 PDM0_CH0_IF_CTL

Description: Interface control

Address: 0x44408010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	SAMPLE_DELAY	Interface sample delay. This field specifies when a PDM value is captured, expressed in clk_if clock cycles. When CLOCK_CTL.HALVE=0: "0": Capture PDM value 1 clk_if cycle after the rising edge of clk_pdm. "1": Capture PDM value 2 clk_if cycles after the rising edge of clk_pdm. ... "255": Capture PDM value 256 clk_if cycles after the rising edge of clk_pdm. When CLOCK_CTL.HALVE=1: "0": Capture PDM value 1 and 2 clk_if cycles after the rising edge of clk_pdm. "1": Capture PDM value 3 and 4 clk_if cycles after the rising edge of clk_pdm. ... "255": Capture PDM value 511 and 512 clk_if cycles after the rising edge of clk_pdm. SAMPLE_DELAY should be set such that the clk_if capture edge is at the middle point between pdm_clk_out edges. Under ideal conditions the middle point is 1/4 of the PDM interface period for the first/even/left channel, and 3/4 of the PDM interface period for the second/odd/right channel, which corresponds to the following programmings: SAMPLE_DELAY(left)=((CLOCK_DIV+1)/4) - 1 SAMPLE_DELAY(right)=(3*(CLOCK_DIV+1)/4) - 1 In practice, due to the roundtrip delay, SAMPLE_DELAY may be set to a later point with respect to the ideal middle point. Note: in all cases a SAMPLE_DELAY value that brings the capture edge close to the pdm_clk_out edges should be avoided. Default Value: 3 **0x0: DELAY_1 :** **0x1: DELAY_2 :**

20.1.30 PDM0_CH0_IF_CTL (continued)

0xff: DELAY_256 :

20.1.31 PDM0_CH0_CIC_CTL

Description: CIC control

Address: 0x44408014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					DECIM_CODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	DECIM_CODE	CIC filter decimation. The CIC filter PCM frequency is a fraction of the PDM frequency: "0": CIC filter PCM frequency is 1/2 * PDM frequency. CIC PCM values are in the range [-0x10, 0x10]. "1": CIC filter PCM frequency is 1/4 * PDM frequency. CIC PCM values are in the range [-0x200, 0x200]. "2": CIC filter PCM frequency is 1/8 * PDM frequency. CIC PCM values are in the range [-0x4000, 0x4000]. "3": CIC filter PCM frequency is 1/16 * PDM frequency. CIC PCM values are in the range [-0x8:0000, 0x8:0000]. "4": CIC filter PCM frequency is 1/32 * PDM frequency. CIC PCM values are in the range [-0x100:0000, 0x100:0000]. "5"-"7": Illegal values. Note: The CIC filter functionality includes offsetting logic to ensure that "digital silence" on the PDM interface (an alternating pattern of '0', '1', '0', '1' ... PDM values) results in CIC filter PCM values of "0". Similarly, a pattern of '0', '0', '0', ... PDM values results in minimum CIC PCM value (-0x100:0000 when DECIMATION is "4") and a pattern of '1', '1', '1', ... PDM values results in maximum CIC PCM value (0x100:0000 when DECIMATION is "4"). Note: The IP's desired "clk_sys" frequency is a function of the PDM interface clock, the CIC filter decimation (CIC_CTL.DECIM_CODE[]) and the FIR filter decimation (FIR_CTL.DEC-IM_CODE[]). Default Value: 4 **0x0: DECIM_2 :** **0x1: DECIM_4 :**

20.1.31 PDM0_CH0_CIC_CTL (continued)

0x2: DECIM_8 :

0x3: DECIM_16 :

0x4: DECIM_32 :

This is the default value and the most realistic value (together with the value "3"). Typically, an overall decimation (or oversample rate (OSR)) of 64 is used, and this is achieved with the default CIC and FIR decimation values.

20.1.32 PDM0_CH0_FIR0_CTL

Description: FIR 0 control

Address: 0x44408018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					DECIM3 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			SCALE [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	FIR 0 filter coefficient enable (does NOT effect FIR filter scaling and FIR filter decimation): '0': Disabled. The middle FIR filter coefficient (16th coefficient, or tap 15 in [0:29] range) is "1" and all other FIR filter coefficients are "0"; i.e. the FIR filter is a pass through filter and the filter gain is "1". fir0_pcm[44:0] = cic_pcm[25:0] (with sign extension) '1': Enabled. Note: This filter is disabled by default, and typically only used for sample frequencies (Fs) of 8 and 16 kHz. Default Value: 0

12 : 8	SCALE	FIR 0 filter PCM scaling. FIR 0 filter PCM values (fir0_pcm[44:0]) are scaled (right shifted, rounded and clipped) to 26-bit signed PCM values (fir0_scaled_pcm[25:0]). These 26-bit PCM values are input to the FIR 1 filter. SCALE specifies the right shift amount (and performs a rounding):
		"0": fir0_scaled_pcm = CLIP26 (fir0_pcm[44:0]).
		"1": fir0_scaled_pcm = CLIP26 (fir0_pcm[44:1] + fir0_pcm[0]).
		...
		"31": fir0_scaled_pcm = CLIP26 (fir0_pcm[44:31] + fir0_pcm[30]).
		With CLIP26(a) defined as:
		if (a >= 0x1ff:ffff) result = 0x1ff:ffff;
		else if (a < -0x200:0000) result = -0x200:0000;
		else result = a;
		Note: Clipping is not necessary for larger SCALE values, as the scaled value is guarneteed to be within the 26-bit signed integer range.
		Default Value: 0
		
		0x0: SCALE_0 :

20.1.32 PDM0_CH0_FIR0_CTL (continued)

		0x1: SCALE_1 :
		0x1f: SCALE_31 :
2 : 0	DECIM3	FIR filter decimation. The FIR filter PCM frequency is a fraction of the CIC filter PCM frequency: "0": FIR 0 filter PCM frequency is 1 * CIC filter PCM frequency. The FIR 0 filter is performed for every CIC filter PCM sample. "1": FIR 0 filter PCM frequency is 1/2 * CIC filter PCM frequency. The FIR 0 filter is performed for every second CIC filter PCM sample. "2": FIR 0 filter PCM frequency is 1/3 * CIC filter PCM frequency. The FIR 0 filter is performed for every third CIC filter PCM sample. "3": FIR 0 filter PCM frequency is 1/4 * CIC filter PCM frequency. The FIR 0 filter is performed for every fourth CIC filter PCM sample. "4": FIR 0 filter PCM frequency is 1/5 * CIC filter PCM frequency. The FIR 0 filter is performed for every fifth CIC filter PCM sample. Default Value: 0
		0x0: DECIM_1 :
		0x1: DECIM_2 :
		0x2: DECIM_3 :
		0x3: DECIM_4 :
		0x4: DECIM_5 :

20.1.33 PDM0_CH0_FIR1_CTL

Description: FIR 1 control

Address: 0x4440801C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						DECIM2 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			SCALE [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	FIR 1 filter coefficient enable (does NOT effect FIR filter scaling and FIR filter decimation): '0': Disabled. The middle FIR filter coefficient (28th coefficient, or tap 27 in [0:54] range) is "1" and all other FIR filter coefficients are "0"; i.e. the FIR filter is a pass through filter and the filter gain is "1". fir1_pcm[43:0] = fir0_scaled_pcm[25:0] (with sign extension) '1': Enabled. Note: Disabling of the filter functionality is provided for debug purposes. Default Value: 1

12 : 8	SCALE	FIR 1 filter PCM scaling. FIR filter PCM values (fir1_pcm[43:0]) are scaled (right shifted, rounded and clipped) to 24-bit signed PCM values (fir1_scaled_pcm[23:0]). These 24-bit PCM values are input to the DC blocker. SCALE specifies the right shift amount (and performs a rounding):
		"0": fir1_scaled_pcm = CLIP24 (fir1_pcm[43:0]).
		"1": fir1_scaled_pcm = CLIP24 (fir1_pcm[43:1] + fir1_pcm[0]).
		...
		"31": fir1_scaled_pcm = CLIP24 (fir1_pcm[43:31] + fir1_pcm[30]).
		With CLIP24(a) defined as:
		if (a >= 0x7f:ffff) result = 0x7f:ffff;
		else if (a < -0x80:0000) result = -0x80:0000;
		else result = a;
		Note: Clipping is not necessary for larger SCALE values, as the scaled value is guarneteed to be within the 24-bit signed integer range.
		Default Value: 15
		0x0: SCALE_0 :
		0x1: SCALE_1 :

20.1.33 PDM0_CH0_FIR1_CTL (continued)

		0x1f: SCALE_31 :
1 : 0	DECIM2	FIR 1 filter decimation. The FIR filter PCM frequency is a fraction of the FIR0 filter PCM frequency: "0": FIR 1 filter PCM frequency is 1 * FIR 0 filter PCM frequency. The FIR filter is performed for every FIR 0 filter PCM sample. "1": FIR 1 filter PCM frequency is 1/2 * FIR 0 filter PCM frequency. The FIR filter is performed for every second FIR 0 filter PCM sample. "2": FIR 1 filter PCM frequency is 1/3 * FIR 0 filter PCM frequency. The FIR filter is performed for every third FIR 0 filter PCM sample. "3": FIR 1 filter PCM frequency is 1/4 * FIR 0 filter PCM frequency. The FIR filter is performed for every fourth FIR 0 filter PCM sample. Default Value: 1 **0x0: DECIM_1 :** **0x1: DECIM_2 :** **0x2: DECIM_3 :** **0x3: DECIM_4 :**

20.1.34 PDM0_CH0_DC_BLOCK_CTL

Description: DC block control

Address: 0x44408020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					CODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	DC blocker enable: '0': Disabled. The functionality is defined as: dc_block_pcm(n) = fir1_scaled_pcm(n) '1': Enabled. The functionality is as specified by the CODE field. Note: disabling of the DC blocker filter functionality is provided for debug purposes. Default Value: 1
2 : 0	CODE	DC blocker coefficient. The DC blocker is defined as: dc_block_state_scaled(n-1) = dc_block_state(n-1) - (dc_block_state(n-1) >> (12-CODE)) dc_block_state(n) = CLIP37 (2^13 * (fir1_scaled_pcm(n) - fir1_scaled_pcm(n-1)) + dc_block_state_scaled(n-1)) dc_block_pcm(n) = dc_block_state(n) >> 13 This first step is a scaling step of the DC block state. It effectively multiplies the DC block state with a variable "alpha" that is close to "1": "0": alpha = 1 - (1/2^(12-0)) = 0.999755859. "1": alpha = 1 - (1/2^(12-1)) = 0.999511719. "2": alpha = 1 - (1/2^(12-2)) = 0.999023438. "3": alpha = 1 - (1/2^(12-3)) = 0.998046875. "4": alpha = 1 - (1/2^(12-4)) = 0.99609375. "5": alpha = 1 - (1/2^(12-5)) = 0.9921875. "6": alpha = 1 - (1/2^(12-6)) = 0.984375. "7": alpha = 1 - (1/2^(12-7)) = 0.96875. Default Value: 1 **0x0: CODE_1 :**

20.1.34 PDM0_CH0_DC_BLOCK_CTL (continued)

0x1: CODE_2 :

0x2: CODE_4 :

0x3: CODE_8 :

0x4: CODE_16 :

0x5: CODE_32 :

0x6: CODE_64 :

0x7: CODE_128 :

20.1.35 PDM0_CH0_RX_FIFO_CTL

Description: RX FIFO control

Address: 0x44408080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		TRIGGER_LEVEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	Reserved
HW Access	Reserved						R	Reserved
Name	Reserved [23:18]						FREEZE	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17	FREEZE	Freeze functionality: '0': HW writes to the RX FIFO and advances the FIFO write pointer. '1': HW writes from the RX FIFO have no effect: freeze will not advance the FIFO write pointer. Note: This functionality is intended for debugging purposes. Default Value: 0
5 : 0	TRIGGER_LEVEL	Trigger level. When the RX FIFO has more entries than the number of this field, a receiver trigger event is generated: - INTR_RX.FIFO_TRIGGER = (# FIFO entries > TRIGGER_LEVEL) Default Value: 0 **0x0: EMPTY :** **0x0: USED_0 :** **0x1: USED_1 :** **0x3f: USED_63 :**

20.1.36 PDM0_CH0_RX_FIFO_STATUS

Description: RX FIFO status

Address: 0x44408084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R						
HW Access	Reserved	W						
Name	Reserved	USED [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [23:22]		RD_PTR [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [31:30]		WR_PTR [29:24]					

Bits	Name	Description
29 : 24	WR_PTR	RX FIFO write pointer: FIFO location at which a new data is written by the hardware. Note: This functionality is intended for debugging purposes. Default Value: 0
21 : 16	RD_PTR	RX FIFO read pointer: FIFO location from which a data is read. Note: This functionality is intended for debugging purposes. Default Value: 0
6 : 0	USED	Number of used/occupied entries in the RX FIFO. The field value is in the range [0, 64]. When "0", the FIFO is empty. When "64", the FIFO is full. Default Value: 0 **0x0: EMPTY :** **0x0: USED_0 :** **0x1: USED_1 :** **0x40: FULL :** **0x40: USED_64 :**

20.1.37 PDM0_CH0_RX_FIFO_RD

Description: RX FIFO read

Address: 0x44408088

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data (PCM sample) read from the RX FIFO. Reading removes the data from the RX FIFO; i.e. behavior is similar to that of a POP operation (RX_FIFO_STATUS.RD_PTR is incremented and RX_FIFO_STATUS.USED is decremented). The read data (DATA) is right aligned (unused bit positions follow the specified sign extension per CTL.WORD_SIGN_EXTEND) when it is read from the FIFO entry (data[23:0]): - 8 bit, DATA[7:0] = data[23:16]. - 10 bit, DATA[9:0] = data[23:14]. - 12 bit, DATA[11:0] = data[23:12]. - 14 bit, DATA[13:0] = data[23:10]. - 16 bit, DATA[15:0] = data[23:8]. - 18 bit, DATA[17:0] = data[23:6]. - 20 bit, DATA[19:0] = data[23:4]. - 24 bit, DATA[23:0] = data[23:0]. - 32 bit, DATA[31:0] = data[23:0] << 8. Note: Reading from an empty RX FIFO activates INTR_RX.FIFO_UNDERFLOW. Default Value: 0

20.1.38 PDM0_CH0_RX_FIFO_RD_SILENT

Description: RX FIFO silent read

Address: 0x4440808C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data (PCM sample) read from the RX FIFO. Reading will NOT remove the data from the RX FIFO; i.e. behavior is similar to that of a PEEK operation. See RX_FIFO_RD for data alignment. Note: Reading from an empty RX FIFO activates INTR.RX_FIFO_UNDERFLOW (the read returns 0xffff:ffff). Note: This functionality is intended for debugging purposes. Default Value: 0

20.1.39 PDM0_CH0_INTR_RX

Description: Interrupt

Address: 0x444080C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1C	Reserved	RW1C	RW1C	RW1C
HW Access	Reserved			RW1S	Reserved	RW1S	RW1S	RW1S
Name	Reserved [7:5]			FIR_OVER-FLOW	Reserved	FIFO_UN-DERFLOW	FI-FO_OVER-FLOW	FI-FO_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							RW1S
Name	Reserved [15:9]							IF_OVER-FLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_OVERFLOW	HW sets this field to '1', when PDM samples are generated too fast by the interface logic (interface overflow). This may be an indication that the IP system frequency is too low wrt. the interface frequency (a SW configuration error). The interface overflow is a non-recoverable error and requires SW disabling (CTL.ENABLED) of the receiver clearing INTR_RX.IF_OVERFLOW to '0' does not resolve the interface underflow). Note: This functionality is intended for debug purposes. Default Value: 0
4	FIR_OVERFLOW	HW sets this field to '1', when CIC filter PCM samples are produced at a faster rate than the FIR filter can process them. This is an indication that the IP system frequency is too low. Note: This functionality is intended for debugging purposes. Default Value: 0
2	FIFO_UNDERFLOW	HW sets this field to '1', when reading from an empty RX FIFO (RX_FIFO_STATUS.USED is "0"). Default Value: 0
1	FIFO_OVERFLOW	HW sets this field to '1', when writing to a full RX FIFO (RX_FIFO_STATUS.USED is "64"). Default Value: 0
0	FIFO_TRIGGER	HW sets this field to '1', when a RX trigger is generated. Default Value: 0

20.1.40 PDM0_CH0_INTR_RX_SET

Description: Interrupt set

Address: 0x444080C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW1S	Reserved	RW1S	RW1S	RW1S
HW Access	Reserved			A	Reserved	A	A	A
Name	Reserved [7:5]			FIR_OVER-FLOW	Reserved	FIFO_UN-DERFLOW	FI-FO_OVER-FLOW	FI-FO_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							IF_OVER-FLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_OVERFLOW	Write this field with '1' to set corresponding INTR_RX field (a write of '0' has no effect). Default Value: 0
4	FIR_OVERFLOW	Write this field with '1' to set corresponding INTR_RX field (a write of '0' has no effect). Default Value: 0
2	FIFO_UNDERFLOW	Write this field with '1' to set corresponding INTR_RX field (a write of '0' has no effect). Default Value: 0
1	FIFO_OVERFLOW	Write this field with '1' to set corresponding INTR_RX field (a write of '0' has no effect). Default Value: 0
0	FIFO_TRIGGER	Write this field with '1' to set corresponding INTR_RX field (a write of '0' has no effect). Default Value: 0

20.1.41 PDM0_CH0_INTR_RX_MASK

Description: Interrupt mask

Address: 0x444080C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved	RW	RW	RW
HW Access	Reserved			R	Reserved	R	R	R
Name	Reserved [7:5]			FIR_OVER-FLOW	Reserved	FIFO_UN-DERFLOW	FI-FO_OVER-FLOW	FI-FO_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							IF_OVER-FLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_OVERFLOW	Mask for corresponding field in INTR_RX register. Default Value: 0
4	FIR_OVERFLOW	Mask for corresponding field in INTR_RX register. Default Value: 0
2	FIFO_UNDERFLOW	Mask for corresponding field in INTR_RX register. Default Value: 0
1	FIFO_OVERFLOW	Mask for corresponding field in INTR_RX register. Default Value: 0
0	FIFO_TRIGGER	Mask for corresponding field in INTR_RX register. Default Value: 0

20.1.42 PDM0_CH0_INTR_RX_MASKED

Description: Interrupt masked

Address: 0x444080CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R	Reserved	R	R	R
HW Access	Reserved			W	Reserved	W	W	W
Name	Reserved [7:5]			FIR_OVER-FLOW	Reserved	FIFO_UN-DERFLOW	FI-FO_OVER-FLOW	FI-FO_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							IF_OVER-FLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_OVERFLOW	Logical AND of corresponding INTR_RX and INTR_RX_MASK fields. Default Value: 0
4	FIR_OVERFLOW	Logical AND of corresponding INTR_RX and INTR_RX_MASK fields. Default Value: 0
2	FIFO_UNDERFLOW	Logical AND of corresponding INTR_RX and INTR_RX_MASK fields. Default Value: 0
1	FIFO_OVERFLOW	Logical AND of corresponding INTR_RX and INTR_RX_MASK fields. Default Value: 0
0	FIFO_TRIGGER	Logical AND of corresponding INTR_RX and INTR_RX_MASK fields. Default Value: 0

21 Inter- IC Sound Bus (I2S) registers

This section discusses the I2S registers. It lists all the registers in mapping tables, in address order.

21.1 Register details

Register name	Address	Description
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_CTL	0x44418000	TX control
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_IF_CTL	0x44418010	TX interface control
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_CH_CTL	0x44418014	TX channel control
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_TEST_CTL	0x44418020	TX test control
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_ROUTE_CTL	0x44418024	TX route control
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_FIFO_CTL	0x44418080	TX FIFO control
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_FIFO_STATUS	0x44418084	TX FIFO status
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_FIFO_WR	0x44418088	TX FIFO write
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX	0x444180C0	Interrupt
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_SET	0x444180C4	Interrupt set
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_MASK	0x444180C8	Interrupt mask
TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_MASKED	0x444180CC	Interrupt masked
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_CTL	0x44418100	RX control
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_IF_CTL	0x44418110	RX interface control
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_CH_CTL	0x44418114	RX channel control
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_TEST_CTL	0x44418120	RX test control
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_ROUTE_CTL	0x44418124	RX route control
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_CTL	0x44418180	RX FIFO control
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_STATUS	0x44418184	RX FIFO status
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_RD	0x44418188	RX FIFO read

Inter- IC Sound Bus (I2S) registers

Register name	Address	Description
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_RD_SILENT	0x4441818C	RX FIFO silent read
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_INTR_RX	0x444181C0	Interrupt
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_INTR_RX_SET	0x444181C4	Interrupt set
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_INTR_RX_MASK	0x444181C8	Interrupt mask
TDM0_TDM_STRUCT0_TDM_RX_STRUCT_INTR_RX_MASKED	0x444181CC	Interrupt masked
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX_CTL	0x44418200	TX control. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX_IF_CTL	0x44418210	TX interface control. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_IF_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX_CH_CTL	0x44418214	TX channel control. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_CH_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX_TEST_CTL	0x44418220	TX test control. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_TEST_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX_ROUTE_CTL	0x44418224	TX route control. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_ROUTE_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX_FIFO_CTL	0x44418280	TX FIFO control. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_FIFO_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX_FIFO_STATUS	0x44418284	TX FIFO status. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_FIFO_STATUS for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX_FIFO_WR	0x44418288	TX FIFO write. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_FIFO_WR for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_INTR_TX	0x444182C0	Interrupt. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_INTR_TX_SET	0x444182C4	Interrupt set. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_SET for the details of bit fields.

Inter- IC Sound Bus (I2S) registers

Register name	Address	Description
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_INTR_TX_MASK	0x444182C8	Interrupt mask. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_MASK for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_TX_STRUCT_INTR_TX_MASKED	0x444182CC	Interrupt masked. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_MASKED for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX_CTL	0x44418300	RX control. See TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX_IF_CTL	0x44418310	RX interface control. See TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_IF_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX_CH_CTL	0x44418314	RX channel control. See TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_CH_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX_TEST_CTL	0x44418320	RX test control. See TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_TEST_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX_ROUTE_CTL	0x44418324	RX route control. See TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_ROUTE_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX_FIFO_CTL	0x44418380	RX FIFO control. See TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_CTL for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX_FIFO_STATUS	0x44418384	RX FIFO status. See TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_STATUS for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX_FIFO_RD	0x44418388	RX FIFO read. See TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_RD for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX_FIFO_RD_SILENT	0x4441838C	RX FIFO silent read. See TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_RD_SILENT for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_INTR_RX	0x444183C0	Interrupt. See TDM0_TDM_STRUCT0_TDM_RX_STRUCT_INTR_RX for the details of bit fields.

Inter- IC Sound Bus (I2S) registers

Register name	Address	Description
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_INTR_RX_SET	0x444183C4	Interrupt set. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_SET for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_INTR_RX_MASK	0x444183C8	Interrupt mask. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_MASK for the details of bit fields.
TDM0_TDM_STRUCT1_TDM_RX_STRUCT_INTR_RX_MASKED	0x444183CC	Interrupt masked. See TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_MASKED for the details of bit fields.

21.1.1 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_CTL

Description: TX control

Address: 0x44418000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				WORD_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW		Reserved			
HW Access	Reserved		R		Reserved			
Name	Reserved [15:14]		FORMAT [13:12]		Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							MS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	Transmitter (TX) enable: '0': Disabled. All non-retained MMIO registers (e.g. the TX_FIFO_STATUS and INTR_TX registers) have their fields reset to their default value. '1': Enabled. Note: when all transmitters and receivers are disabled, the SRAMs are driven into low power mode, if supported by the SRAM. When exiting such low power mode software needs to allow for a certain power up time before SRAM can be used, i.e. before ACTIVE can be asserted. Default Value: 0
16	MS	Master/slave setting: '0': Slave. - Externally driven signals: "tdm_tx_sck_in" and frame sync "tdm_tx_fsync_in" '1': Master. - Interface clock "clk_if" is used to generate transmitter "tdm_tx_sck_out" and transmitter "tdm_tx_fsync_out". Default Value: 1 **0x0: SLAVE :** **0x1: MASTER :**
13 : 12	FORMAT	Format: "0": Left-aligned delayed. "1": Left-aligned. "2": Right-aligned delayed. "3": Right-aligned. Default Value: 0

21.1.1 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_CTL (continued)

		0x0: LEFT_DELAYED :
		0x1: LEFT :
		0x2: RIGHT_DELAYED :
		0x3: RIGHT :
3 : 0	WORD_SIZE	PCM word size: "0": 8 bit. "1": 10 bit. "2": 12 bit. "3": 14 bit. "4": 16 bit. "5": 18 bit. "6": 20 bit. "7": 24 bit. "8": 32 bit. "9"-"15": Undefined. Default Value: 0
		0x0: SIZE_8 :
		0x1: SIZE_10 :
		0x2: SIZE_12 :
		0x3: SIZE_14 :
		0x4: SIZE_16 :
		0x5: SIZE_18 :
		0x6: SIZE_20 :
		0x7: SIZE_24 :
		0x8: SIZE_32 :

21.1.2 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_IF_CTL

Description: TX interface control

Address: 0x44418010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLOCK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved	RW	RW	Reserved	RW		
HW Access	R	Reserved	R	R	Reserved	R		
Name	FSYNC_-FORMAT	Reserved	FSYN-C_POLARI-TY	SCK_PO-LARITY	Reserved	CLOCK_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [23:21]			CH_NR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved		RW				
HW Access	R	Reserved		R				
Name	I2S_MODE	Reserved [30:29]		CH_SIZE [28:24]				

Bits	Name	Description
31	I2S_MODE	I2S mode setting: '0': TDM mode. '1': I2S mode. Default Value: 0 **0x0: TDM :** **0x1: I2S :**
28 : 24	CH_SIZE	Channel size: "0"-"2": Undefined/illegal. "3": 4 bits. ... "31": 32 bits. Note: if TX_CTL.WORD_SIZE is greater than CH_SIZE, the more significant bits of the word are transmitted and the lesser significant bits of the word are dropped. Default Value: 31 **0x0: SIZE_1 :** **0x1: SIZE_2 :** **0x1f: SIZE_32 :**

21.1.2 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_IF_CTL (continued)

20 : 16	CH_NR	Number of channels in the frame: "0": Undefined/illegal. "1": 2 channels. "2": 3 channels. ... "31": 32 channels. Note: the field value should be less than CH_NR (the number of support channels). Note: the TX_CH_CTL.CH_EN fields can be used to enable/disable indvidual channels. Default Value: 1
15	FSYNC_FORMAT	Channel synchronization pulse format: '0': Duration of a single bit period. '1': Duration of the first channel. Default Value: 1 **0x0: BIT_PERIOD :** **0x1: CH_PERIOD :**
13	FSYNC_POLARITY	Channel synchronization polarity: '0': Channel synchronization signal is used "as is". '1': Channel synchronization signal is inverted. Note: Used in BOTH master and slave configurations. Default Value: 0
12	SCK_POLARITY	Clock polarity: '0': Clock signal is used "as is". '1': Clock signal is inverted. Note: Used in BOTH master and slave configurations. Default Value: 0
10 : 8	CLOCK_SEL	Interface clock "clk_if" selection: "0": SRSS clock clk_if_srss[0]. "1": SRSS clock clk_if_srss[1]. "2": SRSS clock clk_if_srss[2]. "3": SRSS clock clk_if_srss[3]. "4": Master interface clock "tdm_tx_mck_in". "5"-"7": undefined. Note: the application is always required to program this field to a value different from the default. Default Value: 7 **0x0: SEL_SRSS_CLOCK0 :** **0x1: SEL_SRSS_CLOCK1 :** **0x2: SEL_SRSS_CLOCK2 :** **0x3: SEL_SRSS_CLOCK3 :** **0x4: SEL_TDM_TX_MCK_IN :**
7 : 0	CLOCK_DIV	Interface clock divider (legal range [1, 255]). The TDM interface "tdm_tx_sck_out" output signal is defined as clk_if / (CLOCK_DIV + 1). CLOCK_DIV should be set to an odd value ({1, 3, 5, ..., 255}), to ensure a 50/50% duty cycle clock. Note: Used in master configuration only. Default Value: 7 **0x0: DIV_BY_1 :** illegal **0x1: DIV_BY_2 :**

21.1.2 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_IF_CTL (continued)

0xff: DIV_BY_256 :

21.1.3 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_CH_CTL

Description: TX channel control

Address: 0x44418014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CH_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	CH_EN	Channel enables: channel i is controlled by CH_EN[i]. '0': Disabled. The TX FIFO does not produce channel i words and the transmitted channel i words on the interface are not driven (the output enable of the "tdm_tx_sd_out" output signal is not driven). '1': Enabled. Note: Only bit 0 through TX_IF_CTL.CH_NR may be set to '1'; i.e. only channels that are present in the frame can be enabled. Default Value: 0

21.1.4 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_TEST_CTL

Description: TX test control

Address: 0x44418020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	Test mode enable. '0': Disabled. Functional mode. - Transmitter tx_sck_in = IOSS tdm_tx_sck_in. - Transmitter tx_fsync_in = IOSS tdm_tx_fsync_in. - Receiver rx_sd_in = IOSS tdm_rx_sd_in. '1': Enabled. Test mode (intended to be used with (slave transmitter, master receiver) configuration). - Transmitter tx_sck_in = Receiver tdm_rx_sck_out. - Transmitter tx_fsync_in = Receiver tdm_rx_fsync_out. - Receiver rx_sd_in = Transmitter tdm_tx_sd_out. Note: TX_TEST_CTL.ENABLED and RX_TEST_CTL.ENABLED should not be set to '1' simultaneously. Default Value: 0 **0x0: FUNCTIONAL :** **0x1: TEST :**

21.1.5 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_ROUTE_CTL

Description: TX route control

Address: 0x44418024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	MODE	Controls routing to the TX slave signalling inputs (FSYNC/SCK): '0': TX slave signaling indipendent from RX signaling: - Transmitter tx_sck_in = IOSS tdm_tx_sck_in - Transmitter tx_fsync_in = IOSS tdm_tx_fsync_in '1': TX slave signalling inputs driven by RX Slave: - Transmitter tx_sck_in = IOSS tdm_rx_sck_in - Transmitter tx_fsync_in = IOSS tdm_rx_fsync_in '2': TX slave signalling inputs driven by RX Master: - Transmitter tx_sck_in = receiver tdm_rx_sck_out - Transmitter tx_fsync_in = receiver tdm_rx_fsync_out Note: MODE=0 is the default behaviour. MODE=1 or 2 is intended to allow the TX slave to share the same signaling used by the RX. This feature can be used to reduce the number of IO pins necessary to connect to an external codec supporting common TX/RX signaling. Note: when MODE=1 or 2, TX_TEST_CTL.ENABLED and RX_TEST_CTL.ENABLED should not be set to '1'. Default Value: 0 **0x0: TX_IN_DRIVEN_BY_IOSS_TX_IN :** **0x1: TX_IN_DRIVEN_BY_IOSS_RX_IN :** **0x2: TX_IN_DRIVEN_BY_RX_OUT :**

21.1.6 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_FIFO_CTL

Description: TX FIFO control

Address: 0x44418080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [23:19]					ACTIVE	FREEZE	MUTE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	ACTIVE	Activate functionality: '0': Transmitter off. The FIFO_UNDERFLOW interrupt cause will not be activated. '1': Transmitter on. The FIFO_UNDERFLOW interrupt may be activated (when an underflow event occurs). Note: This functionality is intended for startup purposes. Default Value: 0
17	FREEZE	Freeze functionality: '0': HW uses TX FIFO data and advances the FIFO read pointer. '1': HW uses a constant PCM data value of "0" or the previous channel PCM data is replayed. Freeze does not advance the FIFO read pointer (the FIFO data is not used). Note: HW ensures that freeze functionality synchronizes on the first channel of a frame to ensure that PCM data of one channel is not misassigned to another channel. As a result, the freeze functionality can be activated at any time. Note: This functionality is intended for debugging purposes. Default Value: 0
16	MUTE	Mute functionality: '0': HW uses TX FIFO data. '1': HW uses a constant PCM data value of "0". Mute does advance the FIFO read pointer. Note: HW ensures that mute functionality synchronizes on the first channel of a frame to ensure that either all or none of the frame's channels are muted. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the TX FIFO has less entries than the number of this field, a transmitter trigger event is generated: - INTR_TX.FIFO_TRIGGER = (# FIFO entries < TRIGGER_LEVEL) Default Value: 0

21.1.6 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_FIFO_CTL (continued)

0x0: EMPTY :

0x0: USED_0 :

0x1: USED_1 :

0x7f: USED_127 :

21.1.7 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_FIFO_STATUS

Description: TX FIFO status

Address: 0x44418084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	R						
HW Access	Reserved	W						
Name	Reserved	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R						
HW Access	Reserved	W						
Name	Reserved	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	TX FIFO write pointer: FIFO location at which a new data is written by the hardware. Note: This functionality is intended for debugging purposes. Default Value: 0
22 : 16	RD_PTR	TX FIFO read pointer: FIFO location from which a data is read. Note: This functionality is intended for debugging purposes. Default Value: 0
7 : 0	USED	Number of used/occupied entries in the TX FIFO. The field value is in the range [0, 128]. When "0", the FIFO is empty. When "128", the FIFO is full. Default Value: 0 **0x0: EMPTY :** **0x0: USED_0 :** **0x1: USED_1 :** **0x80: FULL :** **0x80: USED_128 :**

21.1.8 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX_FIFO_WR

Description: TX FIFO write

Address: 0x44418088

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data (PCM sample) written to the TX FIFO. Writing adds the data to the TX FIFO; i.e. behavior is similar to that of a PUSH operation (TX_FIFO_STATUS.WR_PTR is incremented and TX_FIFO_STATUS.USED is incremented). The write data (DATA) should be right aligned when it is written to the FIFO entry (data[31:0]): - 8 bit, data[31:0] = DATA[7:0] << 24. - 10 bit, data[31:0] = DATA[9:0] << 22. - 12 bit, data[31:0] = DATA[11:0] << 20. - 14 bit, data[31:0] = DATA[13:0] << 18. - 16 bit, data[31:0] = DATA[15:0] << 16. - 18 bit, data[31:0] = DATA[17:0] << 14. - 20 bit, data[31:0] = DATA[19:0] << 12. - 24 bit, data[31:0] = DATA[23:0] << 8. - 32 bit, data[31:0] = DATA[31:0]. Note: Writing to a full TX FIFO activates INTR.TX_FIFO_OVERFLOW. Default Value: 0

21.1.9 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX

Description: Interrupt

Address: 0x444180C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1C	RW1C	RW1C
HW Access	Reserved					RW1S	RW1S	RW1S
Name	Reserved [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							RW1S
Name	Reserved [15:9]							IF_UNDERFLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_UNDERFLOW	HW sets this field to '1', when PCM samples are not generated in time for the interface logic (interface underflow). This may be an indication that the IP system frequency is too low wrt. the interface frequency (a SW configuration error). The interface underflow is a non-recoverable error and requires SW disabling of the channel (a SW write to INTR_TX.IF_UNDERFLOW does not resolve the interface underflow). Note: This functionality is intended for debug purposes. Default Value: 0
2	FIFO_UNDERFLOW	HW sets this field to '1', when reading from an (almost) empty TX FIFO (TX_FIFO_STATUS.USED < "number of enabled channels per frame"). This is referred to as an underflow event. Note: HW ensures that either all or none of the frame's channels are transmitted. In a TX FIFO underflow situation, HW replays previous PCM data or uses a constant PCM data value of "0". Default Value: 0
1	FIFO_OVERFLOW	HW sets this field to '1', when writing to a full TX FIFO (TX_FIFO_STATUS.USED is "128"). Default Value: 0
0	FIFO_TRIGGER	HW sets this field to '1', when a TX trigger is generated. Default Value: 0

21.1.10 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_SET

Description: Interrupt set

Address: 0x444180C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1S	RW1S	RW1S
HW Access	Reserved					A	A	A
Name	Reserved [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							IF_UNDERFLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_UNDERFLOW	Write this field with '1' to set corresponding INTR_TX field (a write of '0' has no effect). Default Value: 0
2	FIFO_UNDERFLOW	Write this field with '1' to set corresponding INTR_TX field (a write of '0' has no effect). Default Value: 0
1	FIFO_OVERFLOW	Write this field with '1' to set corresponding INTR_TX field (a write of '0' has no effect). Default Value: 0
0	FIFO_TRIGGER	Write this field with '1' to set corresponding INTR_TX field (a write of '0' has no effect). Default Value: 0

21.1.11 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_MASK

Description: Interrupt mask

Address: 0x444180C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							IF_UNDERFLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_UNDERFLOW	Mask for corresponding field in INTR_TX register. Default Value: 0
2	FIFO_UNDERFLOW	Mask for corresponding field in INTR_TX register. Default Value: 0
1	FIFO_OVERFLOW	Mask for corresponding field in INTR_TX register. Default Value: 0
0	FIFO_TRIGGER	Mask for corresponding field in INTR_TX register. Default Value: 0

21.1.12 TDM0_TDM_STRUCT0_TDM_TX_STRUCT_INTR_TX_MASKED

Description: Interrupt masked

Address: 0x444180CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R	R	R
HW Access	Reserved					W	W	W
Name	Reserved [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							IF_UNDERFLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_UNDERFLOW	Logical AND of corresponding INTR_TX and INTR_TX_MASK fields. Default Value: 0
2	FIFO_UNDERFLOW	Logical AND of corresponding INTR_TX and INTR_TX_MASK fields. Default Value: 0
1	FIFO_OVERFLOW	Logical AND of corresponding INTR_TX and INTR_TX_MASK fields. Default Value: 0
0	FIFO_TRIGGER	Logical AND of corresponding INTR_TX and INTR_TX_MASK fields. Default Value: 0

21.1.13 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_CTL

Description: RX control

Address: 0x44418100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				WORD_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW		Reserved			RW
HW Access	Reserved		R		Reserved			R
Name	Reserved [15:14]		FORMAT [13:12]		Reserved [11:9]			WORD_SIGN_EXTEND

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							MS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	Receiver (RX) enable: '0': Disabled. All non-retained MMIO registers (e.g. the RX_FIFO_STATUS and INTR_RX registers) have their fields reset to their default value. '1': Enabled. Note: when all transmitters and receivers are disabled, the SRAMs are driven into low power mode, if supported by the SRAM. When exiting such low power mode software needs to allow for a certain power up time before SRAM can be used, i.e. before ACTIVE can be asserted. Default Value: 0
16	MS	Master/slave setting: '0': Slave. - Externally driven signas: clock "tdm_rx_sck_in" and frame sync "tdm_rx_fsync_in". '1': Master. - Interface clock "clk_if" is used to generate receiver "tdm_rx_sck_out" and receiver "tdm_rx_fsync_out". Default Value: 0 **0x0: SLAVE :** **0x1: MASTER :**
13 : 12	FORMAT	Format: "0": Left-aligned delayed. "1": Left-aligned. "2": Right-aligned delayed. "3": Right-aligned. Default Value: 0

21.1.13 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_CTL (continued)

		0x0: LEFT_DELAYED :
		0x1: LEFT :
		0x2: RIGHT_DELAYED :
		0x3: RIGHT :
8	WORD_SIGN_EXTEND	Word extension: '0': zero extension. '1': sign extension. Default Value: 1
		0x0: ZERO_EXTEND :
		0x1: SIGN_EXTEND :
3 : 0	WORD_SIZE	PCM word size: "0": 8 bit. "1": 10 bit. "2": 12 bit. "3": 14 bit. "4": 16 bit. "5": 18 bit. "6": 20 bit. "7": 24 bit. "8": 32 bit. "9"-"15": Undefined. Default Value: 0
		0x0: SIZE_8 :
		0x1: SIZE_10 :
		0x2: SIZE_12 :
		0x3: SIZE_14 :
		0x4: SIZE_16 :
		0x5: SIZE_18 :
		0x6: SIZE_20 :
		0x7: SIZE_24 :
		0x8: SIZE_32 :

21.1.14 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_IF_CTL

Description: RX interface control

Address: 0x44418110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLOCK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	Reserved	RW		
HW Access	R	R	R	R	Reserved	R		
Name	FSYNC_-FORMAT	LATE_SAM-PLE	FSYN-C_POLARI-TY	SCK_PO-LARITY	Reserved	CLOCK_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [23:21]			CH_NR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		RW				
HW Access	R	R		R				
Name	I2S_MODE	LATE_CAPTURE [30:29]		CH_SIZE [28:24]				

Bits	Name	Description
31	I2S_MODE	I2S mode setting: '0': TDM mode. '1': I2S mode. Default Value: 0 **0x0: TDM :** **0x1: I2S :**
30 : 29	LATE_CAPTURE	Extra delay (in "rx_sck_out" cycles) for capturing "tdm_rx_sd_in": "0": no extra delay "1": 1 cycle extra delay "2": 2 cycles extra delay "3": 3 cycles extra delay Note: the value of this field pushes further out the capturing edges used by the receiver to sample "tdm_rx_sd_in". This function is intended to support very large round-trip delays in a master receiver configuration, where the delay at the receiver between "tdm_rx_fsync_out" and the arrival of the first bit on "tdm_rx_sd_in" is multiple clock cycles. Default Value: 0 **0x0: EXTRA_DELAY_0 :** **0x1: EXTRA_DELAY_1 :**

21.1.14 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_IF_CTL (continued)

		0x2: EXTRA_DELAY_2 :
		0x3: EXTRA_DELAY_3 :
28 : 24	CH_SIZE	Channel size: "0"-"2": Undefined/illegal. "3": 4 bits. ... "31": 32 bits. Note: if RX_CTL.WORD_SIZE is greater than CH_SIZE, the lesser significant bits of the word are filled with '0's. Default Value: 31 **0x0: SIZE_1 :** **0x1: SIZE_2 :** **0x1f: SIZE_32 :**
20 : 16	CH_NR	Number of channels in the frame: "0": Undefined/illegal. "1": 2 channels. "2": 3 channels. ... "31": 32 channels. Note: the field value chould be less than CH_NR (the number of support channels). Note: the RX_CH_CTL.CH_EN fields can be used to enable/disable indvidual channels. Default Value: 1
15	FSYNC_FORMAT	Channel synchronization pulse format: '0': Duration of a single bit period. '1': Duration of the first channel. Default Value: 1 **0x0: BIT_PERIOD :** **0x1: CH_PERIOD :**
14	LATE_SAMPLE	Interface late sample sample delay: Slave configuration (RX_CTL.MS is '0'). '0': Sample PCM bit value on rising edge (SCK_POLARITY is '0') or falling edge (SCK_POLARITY is '1') of receiver "rx_sck_in". '1': Sample PCM bit value on falling edge (SCK_POLARITY is '0') or rising edge (SCK_POLARITY is '1') of receiver "rx_sck_in" (half a cycle delay). Master configuration (RX_CTL.MS is '1'). '0': Sample PCM bit value on rising edge (SCK_POLARITY is '0') or falling edge (SCK_POLARITY is '1') of receiver "rx_sck_out". '1': Sample PCM bit value on falling edge (SCK_POLARITY is '0') or rising edge (SCK_POLARITY is '1') of receiver "rx_sck_out" (half a cycle delay). Note: This field can be set to '1' when the roundtrip delay is large (typically) in a master receiver configuration. Default Value: 0 **0x0: RISING :** **0x1: FALLING :**
13	FSYNC_POLARITY	Channel synchronization polarity: '0': Channel synchronization signal is used "as is". '1': Channel synchronization signal is inverted. Note: Used in BOTH master and slave configurations. Default Value: 0

21.1.14 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_IF_CTL (continued)

12	SCK_POLARITY	Clock polarity: '0': Clock signal is used "as is". '1': Clock signal is inverted. Note: Used in BOTH master and slave configurations. Default Value: 0
10 : 8	CLOCK_SEL	Interface clock "clk_if" selection: "0": SRSS clock clk_if_srss[0]. "1": SRSS clock clk_if_srss[1]. "2": SRSS clock clk_if_srss[2]. "3": SRSS clock clk_if_srss[3]. "4": Master interface clock "tdm_rx_mck_in". "5"-"7": undefined. Note: the application is always required to program this field to a value different from the default. Default Value: 7 **0x0: SEL_SRSS_CLOCK0 :** **0x1: SEL_SRSS_CLOCK1 :** **0x2: SEL_SRSS_CLOCK2 :** **0x3: SEL_SRSS_CLOCK3 :** **0x4: SEL_TDM_RX_MCK_IN :**
7 : 0	CLOCK_DIV	Interface clock divider (legal range [1, 255]). The TDM interface "tdm_rx_sck_out" output signals is defined as clk_if / (CLOCK_DIV + 1). CLOCK_DIV should be set to an odd value ({1, 3, 5, ..., 255}), to ensure a 50/50% duty cycle clock. Note: Used in master configuration only. Note: Due to delays in the IO SubSystem (specifically the IO cells), the maximum TDM interface clock "tdm_rx_sck_out" may be restricted. As a result, the maximum bitrate is less than the theoretical maximum (32 channels, 32 bits per channel and a high Fs of e.g. 48 kHz). This restriction is most applicable to the master, receiver configuration. Default Value: 7 **0x0: DIV_BY_1 :** illegal **0x1: DIV_BY_2 :** **0xff: DIV_BY_256 :**

21.1.15 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_CH_CTL

Description: RX channel control

Address: 0x44418114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CH_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	CH_EN	Channel enables: channel i is controlled by CH_EN[i]. '0': Disabled. The RX FIFO does not consume channel i words and the received channel i words on the interface are discarded. '1': Enabled.. Note: Only bit 0 through RX_IF_CTL.CH_NR may be set to '1'; i.e. only channels that are present in the frame can be enabled. Default Value: 0

21.1.16 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_TEST_CTL

Description: RX test control

Address: 0x44418120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	Test mode enable. '0': Disabled. Functional mode. - Receiver rx_sck_in = IOSS tdm_rx_sck_in. - Receiver rx_fsync_in = IOSS tdm_rx_fsync_in. - Receiver rx_sd_in = IOSS tdm_rx_sd_in. '1': Enabled. Test mode (intended to be used with (master transmitter, slave receiver) configuration). - Receiver rx_sck_in = Transmitter tdm_tx_sck_out. - Receiver rx_fsync_in = Transmitter tdm_tx_fsync_out. - Receiver rx_sd_in = Transmitter tdm_tx_sd_out. Note: TX_TEST_CTL.ENABLED and RX_TEST_CTL.ENABLED should not be set to '1' simultaneously. Default Value: 0 **0x0: FUNCTIONAL :** **0x1: TEST :**

21.1.17 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_ROUTE_CTL

Description: RX route control

Address: 0x44418124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	MODE	Controls routing to the RX slave signalling inputs (FSYNC/SCK): '0': RX slave signaling indipendent from TX signaling: - Receiver rx_sck_in = IOSS tdm_rx_sck_in - Receiver rx_fsync_in = IOSS tdm_rx_fsync_in '1': RX slave signalling inputs driven by TX Slave: - Receiver rx_sck_in = IOSS tdm_tx_sck_in - Receiver rx_fsync_in = IOSS tdm_tx_fsync_in '2': RX slave signalling inputs driven by TX Master: - Receiver rx_sck_in = transmitter tdm_tx_sck_out - Receiver rx_fsync_in = transmitter tdm_tx_fsync_out Note: MODE=0 is the default behaviour. MODE=1 or 2 is intended to allow the RX slave to share the same signaling used by the TX. This feature can be used to reduce the number of IO pins necessary to connect to an external codec supporting common TX/RX signaling. Note: when MODE=1 or 2, TX_TEST_CTL.ENABLED and RX_TEST_CTL.ENABLED should not be set to '1'. Default Value: 0 **0x0: RX_IN_DRIVEN_BY_IOSS_RX_IN :** **0x1: RX_IN_DRIVEN_BY_IOSS_TX_IN :** **0x2: RX_IN_DRIVEN_BY_TX_OUT :**

21.1.18 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_CTL

Description: RX FIFO control

Address: 0x44418180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	Reserved
HW Access	Reserved					R	R	Reserved
Name	Reserved [23:19]					ACTIVE	FREEZE	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	ACTIVE	Activate functionality: '0': Receiver off. The FIFO_OVERFLOW interrupt cause will not be activated. '1': Receiver on. The FIFO_OVERFLOW interrupt may be activated (when an overflow event occurs). Note: This functionality is intended for stopping purposes. Default Value: 0
17	FREEZE	Freeze functionality: '0': HW writes to the RX FIFO and advances the FIFO write pointer. '1': HW writes from the RX FIFO have no effect: freeze will not advance the FIFO write pointer. Note: HW ensures that freeze functionality synchronizes on the first channel of a frame to ensure that PCM data of one channel is not misassigned to another channel. As a result, the freeze functionality can be activated at any time. Note: This functionality is intended for debugging purposes. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the RX FIFO has more entries than the number of this field, a receiver trigger event is generated: - INTR_RX.FIFO_TRIGGER = (# FIFO entries > TRIGGER_LEVEL) Default Value: 0 **0x0: EMPTY :** **0x0: USED_0 :** **0x1: USED_1 :**

21.1.18 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_CTL (continued)

0x7f: USED_127 :

21.1.19 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_STATUS

Description: RX FIFO status

Address: 0x44418184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	R						
HW Access	Reserved	W						
Name	Reserved	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R						
HW Access	Reserved	W						
Name	Reserved	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	RX FIFO write pointer: FIFO location at which a new data is written by the hardware. Note: This functionality is intended for debugging purposes. Default Value: 0
22 : 16	RD_PTR	RX FIFO read pointer: FIFO location from which a data is read. Note: This functionality is intended for debugging purposes. Default Value: 0
7 : 0	USED	Number of used/occupied entries in the RX FIFO. The field value is in the range [0, 128]. When "0", the FIFO is empty. When "128", the FIFO is full. Default Value: 0 **0x0: EMPTY :** **0x0: USED_0 :** **0x1: USED_1 :** **0x80: FULL :** **0x80: USED_128 :**

21.1.20 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_RD

Description: RX FIFO read

Address: 0x44418188

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data (PCM sample) read from the RX FIFO. Reading removes the data from the RX FIFO; i.e. behavior is similar to that of a POP operation (RX_FIFO_STATUS.RD_PTR is incremented and RX_FIFO_STATUS.USED is decremented). The read data (DATA) is right aligned (unused bit positions follow the specified sign extension per RX_CTL.WORD_SIGN_EXTEND) when it is read from the FIFO entry (data[31:0]): - 8 bit, DATA[7:0] = data[31:24]. - 10 bit, DATA[9:0] = data[31:22]. - 12 bit, DATA[11:0] = data[31:20]. - 14 bit, DATA[13:0] = data[31:18]. - 16 bit, DATA[15:0] = data[31:16]. - 18 bit, DATA[17:0] = data[31:14]. - 20 bit, DATA[19:0] = data[31:12]. - 24 bit, DATA[23:0] = data[31:8]. - 32 bit, DATA[31:0] = data[31:0]. Note: Reading from an empty RX FIFO activates INTR_RX.FIFO_UNDERFLOW. Default Value: 0

21.1.21 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX_FIFO_RD_SILENT

Description: RX FIFO silent read

Address: 0x4441818C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Default Value: 0

21.1.22 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_INTR_RX

Description: Interrupt

Address: 0x444181C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1C	RW1C	RW1C
HW Access	Reserved					RW1S	RW1S	RW1S
Name	Reserved [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							RW1S
Name	Reserved [15:9]							IF_OVERFLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_OVERFLOW	HW sets this field to '1', when PCM samples are generated too fast by the interface logic (interface overflow). This may be an indication that the IP system frequency is too low wrt. the interface frequency (a SW configuration error). The interface overflow is a non-recoverable error and requires SW disabling of the channel (a SW write to INTR_RX.IF_OVERFLOW does not resolve the interface underflow). Note: This functionality is intended for debug purposes. Default Value: 0
2	FIFO_UNDERFLOW	HW sets this field to '1', when reading from an empty RX FIFO (RX_FIFO_STATUS.USED is "0"). Default Value: 0
1	FIFO_OVERFLOW	HW sets this field to '1', when writing to a (almost) full RX FIFO (128 -RX_FIFO_STATUS.USED < "number of enabled channels per frame"). This is referred to as an overflow event. Note: HW ensures that either all or none of the frame's channels are received. In a RX FIFO overflow situation, HW discards received PCM data values. Default Value: 0
0	FIFO_TRIGGER	HW sets this field to '1', when a RX trigger is generated. Default Value: 0

21.1.23 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_INTR_RX_SET

Description: Interrupt set

Address: 0x444181C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW1S	RW1S	RW1S
HW Access	Reserved					A	A	A
Name	Reserved [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							IF_OVERFLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_OVERFLOW	Write this field with '1' to set corresponding INTR_RX field (a write of '0' has no effect). Default Value: 0
2	FIFO_UNDERFLOW	Write this field with '1' to set corresponding INTR_RX field (a write of '0' has no effect). Default Value: 0
1	FIFO_OVERFLOW	Write this field with '1' to set corresponding INTR_RX field (a write of '0' has no effect). Default Value: 0
0	FIFO_TRIGGER	Write this field with '1' to set corresponding INTR_RX field (a write of '0' has no effect). Default Value: 0

21.1.24 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_INTR_RX_MASK

Description: Interrupt mask

Address: 0x444181C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							IF_OVERFLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_OVERFLOW	Mask for corresponding field in INTR_RX register. Default Value: 0
2	FIFO_UNDERFLOW	Mask for corresponding field in INTR_RX register. Default Value: 0
1	FIFO_OVERFLOW	Mask for corresponding field in INTR_RX register. Default Value: 0
0	FIFO_TRIGGER	Mask for corresponding field in INTR_RX register. Default Value: 0

21.1.25 TDM0_TDM_STRUCT0_TDM_RX_STRUCT_INTR_RX_MASKED

Description: Interrupt masked

Address: 0x444181CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R	R	R
HW Access	Reserved					W	W	W
Name	Reserved [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							IF_OVERFLOW

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	IF_OVERFLOW	Logical AND of corresponding INTR_RX and INTR_RX_MASK fields. Default Value: 0
2	FIFO_UNDERFLOW	Logical AND of corresponding INTR_RX and INTR_RX_MASK fields. Default Value: 0
1	FIFO_OVERFLOW	Logical AND of corresponding INTR_RX and INTR_RX_MASK fields. Default Value: 0
0	FIFO_TRIGGER	Logical AND of corresponding INTR_RX and INTR_RX_MASK fields. Default Value: 0

22 Serial Memory Interface (SMIF) registers

This section discusses the SMIF registers. It lists all the registers in mapping tables, in address order.

22.1 Register details

Register name	Address	Description
SMIF0_CACHE_BLOCK_HWPARAMS	0x44450000	Hardware Parameter register
SMIF0_CACHE_BLOCK_CTRL	0x44450010	Control Register
SMIF0_CACHE_BLOCK_NSEC_ACCESS	0x44450014	Non-secure access information
SMIF0_CACHE_BLOCK_MAINT_CTRL_ALL	0x44450020	Maintenance control for the entire cache
SMIF0_CACHE_BLOCK_MAINT_CTRL_LINES	0x44450024	Maintenance control for individual lines
SMIF0_CACHE_BLOCK_MAINT_STATUS	0x44450028	Maintenance status for the cache
SMIF0_CACHE_BLOCK_SECIRQSTAT	0x44450100	Secure Interrupt Request Status register
SMIF0_CACHE_BLOCK_SECIRQSCLR	0x44450104	Secure Interrupt Status Clear register
SMIF0_CACHE_BLOCK_SECIRQEN	0x44450108	Secure Interrupt Enable register
SMIF0_CACHE_BLOCK_SECIRQINFO1	0x4445010C	Secure transfer error information 1
SMIF0_CACHE_BLOCK_SECIRQINFO2	0x44450110	Secure transfer error information 2
SMIF0_CACHE_BLOCK_NSECIRQSTAT	0x44450140	Non-secure Interrupt Request Status register
SMIF0_CACHE_BLOCK_NSECIRQSCLR	0x44450144	Non-secure Interrupt Status Clear register
SMIF0_CACHE_BLOCK_NSECIRQEN	0x44450148	Non-secure Interrupt Enable register
SMIF0_CACHE_BLOCK_NSECIRQINFO1	0x4445014C	Non-secure transfer error information 1
SMIF0_CACHE_BLOCK_NSECIRQINFO2	0x44450150	Non-secure transfer error information 2
SMIF0_CACHE_BLOCK_SECHIT	0x44450300	Secure transfers Hit register
SMIF0_CACHE_BLOCK_SECMISS	0x44450304	Secure transfers Miss register
SMIF0_CACHE_BLOCK_SECSTATCTRL	0x44450308	Secure transfers statistic counters control
SMIF0_CACHE_BLOCK_NSECHIT	0x44450310	Non-secure transfers Hit register
SMIF0_CACHE_BLOCK_NSECMISS	0x44450314	Non-secure transfers Miss register
SMIF0_CACHE_BLOCK_NSECSTATCTRL	0x44450318	Non-secure transfers statistic counters control
SMIF0_CACHE_BLOCK_PMSVR0	0x44450600	Saved Value Register 0 - Secure Hit
SMIF0_CACHE_BLOCK_PMSVR1	0x44450604	Saved Value Register 1 - Secure Miss
SMIF0_CACHE_BLOCK_PMSVR2	0x44450608	Saved Value Register 2 - Non-secure Hit
SMIF0_CACHE_BLOCK_PMSVR3	0x4445060C	Saved Value Register 3 - Non-secure Miss
SMIF0_CACHE_BLOCK_PMSSSR	0x44450680	PMU Snapshot Status Register
SMIF0_CACHE_BLOCK_PMSSCR	0x444506F0	PMU Snapshot Capture Register
SMIF0_CACHE_BLOCK_PMSSRR	0x444506F4	PMU Snapshot Reset Register
SMIF0_CACHE_BLOCK_PIDR4	0x44450FD0	Peripheral ID 4
SMIF0_CACHE_BLOCK_PIDR5	0x44450FD4	Peripheral ID 5
SMIF0_CACHE_BLOCK_PIDR6	0x44450FD8	Peripheral ID 6
SMIF0_CACHE_BLOCK_PIDR7	0x44450FDC	Peripheral ID 7
SMIF0_CACHE_BLOCK_PIDR0	0x44450FE0	Peripheral ID 0

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF0_CACHE_BLOCK_PIDR1	0x44450FE4	Peripheral ID 1
SMIF0_CACHE_BLOCK_PIDR2	0x44450FE8	Peripheral ID 2
SMIF0_CACHE_BLOCK_PIDR3	0x44450FEC	Peripheral ID 3
SMIF0_CACHE_BLOCK_CIDR0	0x44450FF0	Component ID 0
SMIF0_CACHE_BLOCK_CIDR1	0x44450FF4	Component ID 1
SMIF0_CACHE_BLOCK_CIDR2	0x44450FF8	Component ID 2
SMIF0_CACHE_BLOCK_CIDR3	0x44450FFC	Component ID 3
SMIF0_CACHE_BLOCK_MMIO_BYPASS_WI	0x44452000	Bypass wrap to increment conversion logic
SMIF0_CACHE_BLOCK_MMIO_MASTER_ID	0x44452004	The cache generates transactions (linefill and eviction Write-Back) that are marked with the value specified by MASTER_ID on hmaster_m.
SMIF0_CACHE_BLOCK_MMIO_DIS_CACHE_EN_MAINT	0x44452008	This signal turns on/off cache enable maintenance.
SMIF0_CACHE_BLOCK_MMIO_DIS_CACHE_DIS_MAINT	0x4445200C	This signal turns on/off cache disable maintenance.
SMIF0_CACHE_BLOCK_MMIO_APB_VIOLATION_RESP	0x44452010	This signal controls if the APB interface of cache responds with an error to illegal operations on the APB interface. Illegal operations on the APB interface include Writing with no full write strobe, Accessing non-word aligned addresses, Instruction accesses, Non-privileged accesses 1 - The Cache responds with an APB error. Read data is masked with zeros and write data is ignored. 0 - The Cache sends an OK response. Read data is masked with zeros and write data is ignored.
SMIF0_CACHE_BLOCK_MMIO_MMIO_ACTIVE_EN	0x44452014	SW control to put SMIF.6 in active or clock gated mode
SMIF0_CACHE_BLOCK_MMIO_POWER_ON_ENABLE	0x44452018	This signal configures the cache to enable the cache automatically after powerup.
SMIF0_CACHE_BLOCK_MMIO_MMIO_CACHE_RET_EN	0x4445201C	Controls if cache SRAMs are retained during DPSLP
SMIF0_CACHE_BLOCK_MMIO_DIS_PWR_DOWN_MAINT	0x44452020	This signal turns on/off powerdown maintenance.
SMIF0_CACHE_BLOCK_MMIO_REGION0_BASE	0x44452024	Region 0 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle
SMIF0_CACHE_BLOCK_MMIO_REGION0_LIMIT	0x44452028	Region 0 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF0_CACHE_BLOCK_MMIO_REGION1_BASE	0x4445202C	Region 1 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle
SMIF0_CACHE_BLOCK_MMIO_REGION1_LIMIT	0x44452030	Region 1 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle
SMIF0_CACHE_BLOCK_MMIO_REGION2_BASE	0x44452034	Region 2 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle
SMIF0_CACHE_BLOCK_MMIO_REGION2_LIMIT	0x44452038	Region 2 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle
SMIF0_CACHE_BLOCK_MMIO_REGION3_BASE	0x4445203C	Region 3 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle
SMIF0_CACHE_BLOCK_MMIO_REGION3_LIMIT	0x44452040	Region 3 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CFG	0x44454000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CTRL	0x44454100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_MAX	0x44454104	Max value of block-based index register
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_CFG	0x44454108	Block size & initialization in progress
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_IDX	0x4445410C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_LUT	0x44454110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_CTRL	0x44454200	Control register with lock bit and auto-increment only

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_MAX	0x44454208	Max value of block-based index register for ROT
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_CFG	0x4445420C	Same as BLK_CFG
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_IDX	0x44454210	Index of 8-block group accessed through ROT_BLK_LUT_*
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_PC	0x44454214	Protection context of 8-block group accesses through ROT_BLK_LUT
SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_CFG	0x44454218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC
SMIF0_CORE_CTL	0x44460000	Control
SMIF0_CORE_STATUS	0x44460004	Status
SMIF0_CORE_CTL2	0x44460008	Control 2
SMIF0_CORE_DLP_DELAY_TAP_SEL0	0x44460010	DLP Delay Tap Select Register 0
SMIF0_CORE_DLP_DELAY_TAP_SEL1	0x44460014	DLP Delay Tap Select Register 1
SMIF0_CORE_DLP_CTL	0x44460018	DLP Control Register
SMIF0_CORE_DLP_STATUS0	0x44460020	DLP Status Register 0
SMIF0_CORE_DLP_STATUS1	0x44460024	DLP Status Register 1
SMIF0_CORE_TX_CMD_FIFO_STATUS	0x44460044	Transmitter command FIFO status
SMIF0_CORE_TX_CMD_MMIO_FIFO_STATUS	0x44460048	Transmitter command MMIO FIFO status
SMIF0_CORE_TX_CMD_MMIO_FIFO_WR	0x44460050	Transmitter command MMIO FIFO write
SMIF0_CORE_TX_DATA_MMIO_FIFO_CTL	0x44460080	Transmitter data MMIO FIFO control
SMIF0_CORE_TX_DATA_FIFO_STATUS	0x44460084	Transmitter data FIFO status
SMIF0_CORE_TX_DATA_MMIO_FIFO_STATUS	0x44460088	Transmitter data MMIO FIFO status
SMIF0_CORE_TX_DATA_MMIO_FIFO_WR1	0x44460090	Transmitter data MMIO FIFO write
SMIF0_CORE_TX_DATA_MMIO_FIFO_WR2	0x44460094	Transmitter data MMIO FIFO write
SMIF0_CORE_TX_DATA_MMIO_FIFO_WR4	0x44460098	Transmitter data MMIO FIFO write
SMIF0_CORE_TX_DATA_MMIO_FIFO_WR1ODD	0x4446009C	Transmitter data MMIO FIFO write
SMIF0_CORE_RX_DATA_MMIO_FIFO_CTL	0x444600C0	Receiver data MMIO FIFO control
SMIF0_CORE_RX_DATA_MMIO_FIFO_STATUS	0x444600C4	Receiver data MMIO FIFO status
SMIF0_CORE_RX_DATA_FIFO_STATUS	0x444600C8	Receiver data FIFO status
SMIF0_CORE_RX_DATA_MMIO_FIFO_RD1	0x444600D0	Receiver data MMIO FIFO read
SMIF0_CORE_RX_DATA_MMIO_FIFO_RD2	0x444600D4	Receiver data MMIO FIFO read
SMIF0_CORE_RX_DATA_MMIO_FIFO_RD4	0x444600D8	Receiver data MMIO FIFO read
SMIF0_CORE_RX_DATA_MMIO_FIFO_RD1_SILENT	0x444600E0	Receiver data MMIO FIFO silent read
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_CMD	0x44460200	Cryptography command
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_ADDR	0x44460204	Cryptography base address
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_MASK	0x44460208	Cryptography mask

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_SUBREGION	0x4446020C	Cryptography subregion disable
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT0	0x44460220	Cryptography input 0
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT1	0x44460224	Cryptography input 1
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT2	0x44460228	Cryptography input 2
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT3	0x4446022C	Cryptography input 3
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY0	0x44460240	Cryptography key 0
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY1	0x44460244	Cryptography key 1
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY2	0x44460248	Cryptography key 2
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY3	0x4446024C	Cryptography key 3
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT0	0x44460260	Cryptography output 0
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT1	0x44460264	Cryptography output 1
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT2	0x44460268	Cryptography output 2
SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT3	0x4446026C	Cryptography output 3
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_CMD	0x44460280	Cryptography command. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_CMD for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_ADDR	0x44460284	Cryptography base address. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_ADDR for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_MASK	0x44460288	Cryptography mask. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_MASK for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_SUBREGION	0x4446028C	Cryptography subregion disable. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_SUBREGION for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_INPUT0	0x444602A0	Cryptography input 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT0 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_INPUT1	0x444602A4	Cryptography input 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT1 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_INPUT2	0x444602A8	Cryptography input 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT2 for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_INPUT3	0x444602AC	Cryptography input 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT3 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_KEY0	0x444602C0	Cryptography key 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY0 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_KEY1	0x444602C4	Cryptography key 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY1 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_KEY2	0x444602C8	Cryptography key 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY2 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_KEY3	0x444602CC	Cryptography key 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY3 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_OUTPUT0	0x444602E0	Cryptography output 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT0 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_OUTPUT1	0x444602E4	Cryptography output 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT1 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_OUTPUT2	0x444602E8	Cryptography output 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT2 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO1_CRYPTO_OUTPUT3	0x444602EC	Cryptography output 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT3 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_CMD	0x44460300	Cryptography command. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_CMD for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_ADDR	0x44460304	Cryptography base address. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_ADDR for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_MASK	0x44460308	Cryptography mask. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_MASK for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_SUBREGION	0x4446030C	Cryptography subregion disable. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_SUBREGION for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_INPUT0	0x44460320	Cryptography input 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT0 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_INPUT1	0x44460324	Cryptography input 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT1 for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_INPUT2	0x44460328	Cryptography input 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT2 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_INPUT3	0x4446032C	Cryptography input 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT3 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_KEY0	0x44460340	Cryptography key 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY0 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_KEY1	0x44460344	Cryptography key 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY1 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_KEY2	0x44460348	Cryptography key 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY2 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_KEY3	0x4446034C	Cryptography key 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY3 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_OUTPUT0	0x44460360	Cryptography output 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT0 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_OUTPUT1	0x44460364	Cryptography output 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT1 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_OUTPUT2	0x44460368	Cryptography output 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT2 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO2_CRYPTO_OUTPUT3	0x4446036C	Cryptography output 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT3 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_CMD	0x44460380	Cryptography command. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_CMD for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_ADDR	0x44460384	Cryptography base address. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_ADDR for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_MASK	0x44460388	Cryptography mask. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_MASK for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_SUBREGION	0x4446038C	Cryptography subregion disable. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_SUBREGION for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_INPUT0	0x444603A0	Cryptography input 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT0 for the details of bit fields.

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Register name	Address	Description
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_INPUT1	0x444603A4	Cryptography input 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT1 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_INPUT2	0x444603A8	Cryptography input 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT2 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_INPUT3	0x444603AC	Cryptography input 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT3 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_KEY0	0x444603C0	Cryptography key 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY0 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_KEY1	0x444603C4	Cryptography key 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY1 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_KEY2	0x444603C8	Cryptography key 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY2 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_KEY3	0x444603CC	Cryptography key 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY3 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_OUTPUT0	0x444603E0	Cryptography output 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT0 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_OUTPUT1	0x444603E4	Cryptography output 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT1 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_OUTPUT2	0x444603E8	Cryptography output 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT2 for the details of bit fields.
SMIF0_CORE_SMIF_CRYPTO3_CRYPTO_OUTPUT3	0x444603EC	Cryptography output 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT3 for the details of bit fields.
SMIF0_CORE_INTR	0x444607C0	Interrupt register
SMIF0_CORE_INTR_SET	0x444607C4	Interrupt set register
SMIF0_CORE_INTR_MASK	0x444607C8	Interrupt mask register
SMIF0_CORE_INTR_MASKED	0x444607CC	Interrupt masked register
SMIF0_CORE_DLL_IDAC	0x444607D8	DLL IDAC (when DLL runs in open loop, selects the delay of the delay line)
SMIF0_CORE_DLL_IVR	0x444607DC	DLL IVR (Contol Output Voltage of internal Voltage Regulator)
SMIF0_CORE_DEVICE0_CTL	0x44460800	Control
SMIF0_CORE_DEVICE0_ADDR	0x44460808	Device region base address

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Register name	Address	Description
SMIF0_CORE_DEVICE0_MASK	0x4446080C	Device region mask
SMIF0_CORE_DEVICE0_ADDR_CTL	0x44460820	Address control
SMIF0_CORE_DEVICE0_RX_CAPTURE_CONFIG	0x44460828	RX capture configuration
SMIF0_CORE_DEVICE0_RD_CMD_CTL	0x44460840	Read command control
SMIF0_CORE_DEVICE0_RD_ADDR_CTL	0x44460844	Read address control
SMIF0_CORE_DEVICE0_RD_MODE_CTL	0x44460848	Read mode control
SMIF0_CORE_DEVICE0_RD_DUMMY_CTL	0x4446084C	Read dummy control
SMIF0_CORE_DEVICE0_RD_DATA_CTL	0x44460850	Read data control
SMIF0_CORE_DEVICE0_RD_BOUND_CTL	0x44460858	Read boundary control
SMIF0_CORE_DEVICE0_WR_CMD_CTL	0x44460860	Write command control
SMIF0_CORE_DEVICE0_WR_ADDR_CTL	0x44460864	Write address control
SMIF0_CORE_DEVICE0_WR_MODE_CTL	0x44460868	Write mode control
SMIF0_CORE_DEVICE0_WR_DUMMY_CTL	0x4446086C	Write dummy control
SMIF0_CORE_DEVICE0_WR_DATA_CTL	0x44460870	Write data control
SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0	0x44460878	HB FW Calibration Delay Tap Select 0
SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1	0x4446087C	HB FW Calibration Delay Tap Select 1
SMIF0_CORE_DEVICE1_CTL	0x44460880	Control. See SMIF0_CORE_DEVICE0_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_ADDR	0x44460888	Device region base address. See SMIF0_CORE_DEVICE0_ADDR for the details of bit fields.
SMIF0_CORE_DEVICE1_MASK	0x4446088C	Device region mask. See SMIF0_CORE_DEVICE0_MASK for the details of bit fields.
SMIF0_CORE_DEVICE1_ADDR_CTL	0x444608A0	Address control. See SMIF0_CORE_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_RX_CAPTURE_CONFIG	0x444608A8	RX capture configuration. See SMIF0_CORE_DEVICE0_RX_CAPTURE_CONFIG for the details of bit fields.
SMIF0_CORE_DEVICE1_RD_CMD_CTL	0x444608C0	Read command control. See SMIF0_CORE_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_RD_ADDR_CTL	0x444608C4	Read address control. See SMIF0_CORE_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_RD_MODE_CTL	0x444608C8	Read mode control. See SMIF0_CORE_DEVICE0_RD_MODE_CTL for the details of bit fields.

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Register name	Address	Description
SMIF0_CORE_DEVICE1_RD_DUMMY_CTL	0x444608CC	Read dummy control. See SMIF0_CORE_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_RD_DATA_CTL	0x444608D0	Read data control. See SMIF0_CORE_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_RD_BOUND_CTL	0x444608D8	Read boundary control. See SMIF0_CORE_DEVICE0_RD_BOUND_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_WR_CMD_CTL	0x444608E0	Write command control. See SMIF0_CORE_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_WR_ADDR_CTL	0x444608E4	Write address control. See SMIF0_CORE_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_WR_MODE_CTL	0x444608E8	Write mode control. See SMIF0_CORE_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_WR_DUMMY_CTL	0x444608EC	Write dummy control. See SMIF0_CORE_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_WR_DATA_CTL	0x444608F0	Write data control. See SMIF0_CORE_DEVICE0_WR_DATA_CTL for the details of bit fields.
SMIF0_CORE_DEVICE1_HB_FW_DEL_TAP_SEL_0	0x444608F8	HB FW Calibration Delay Tap Select 0. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0 for the details of bit fields.
SMIF0_CORE_DEVICE1_HB_FW_DEL_TAP_SEL_1	0x444608FC	HB FW Calibration Delay Tap Select 1. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1 for the details of bit fields.
SMIF0_CORE_DEVICE2_CTL	0x44460900	Control. See SMIF0_CORE_DEVICE0_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_ADDR	0x44460908	Device region base address. See SMIF0_CORE_DEVICE0_ADDR for the details of bit fields.
SMIF0_CORE_DEVICE2_MASK	0x4446090C	Device region mask. See SMIF0_CORE_DEVICE0_MASK for the details of bit fields.
SMIF0_CORE_DEVICE2_ADDR_CTL	0x44460920	Address control. See SMIF0_CORE_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_RX_CAPTURE_CONFIG	0x44460928	RX capture configuration. See SMIF0_CORE_DEVICE0_RX_CAPTURE_CONFIG for the details of bit fields.

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Register name	Address	Description
SMIF0_CORE_DEVICE2_RD_CMD_CTL	0x44460940	Read command control. See SMIF0_CORE_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_RD_ADDR_CTL	0x44460944	Read address control. See SMIF0_CORE_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_RD_MODE_CTL	0x44460948	Read mode control. See SMIF0_CORE_DEVICE0_RD_MODE_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_RD_DUMMY_CTL	0x4446094C	Read dummy control. See SMIF0_CORE_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_RD_DATA_CTL	0x44460950	Read data control. See SMIF0_CORE_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_RD_BOUND_CTL	0x44460958	Read boundary control. See SMIF0_CORE_DEVICE0_RD_BOUND_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_WR_CMD_CTL	0x44460960	Write command control. See SMIF0_CORE_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_WR_ADDR_CTL	0x44460964	Write address control. See SMIF0_CORE_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_WR_MODE_CTL	0x44460968	Write mode control. See SMIF0_CORE_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_WR_DUMMY_CTL	0x4446096C	Write dummy control. See SMIF0_CORE_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_WR_DATA_CTL	0x44460970	Write data control. See SMIF0_CORE_DEVICE0_WR_DATA_CTL for the details of bit fields.
SMIF0_CORE_DEVICE2_HB_FW_DEL_TAP_SEL_0	0x44460978	HB FW Calibration Delay Tap Select 0. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0 for the details of bit fields.
SMIF0_CORE_DEVICE2_HB_FW_DEL_TAP_SEL_1	0x4446097C	HB FW Calibration Delay Tap Select 1. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1 for the details of bit fields.
SMIF0_CORE_DEVICE3_CTL	0x44460980	Control. See SMIF0_CORE_DEVICE0_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_ADDR	0x44460988	Device region base address. See SMIF0_CORE_DEVICE0_ADDR for the details of bit fields.

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Register name	Address	Description
SMIF0_CORE_DEVICE3_MASK	0x4446098C	Device region mask. See SMIF0_CORE_DEVICE0_MASK for the details of bit fields.
SMIF0_CORE_DEVICE3_ADDR_CTL	0x444609A0	Address control. See SMIF0_CORE_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_RX_CAPTURE_CONFIG	0x444609A8	RX capture configuration. See SMIF0_CORE_DEVICE0_RX_CAPTURE_CONFIG for the details of bit fields.
SMIF0_CORE_DEVICE3_RD_CMD_CTL	0x444609C0	Read command control. See SMIF0_CORE_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_RD_ADDR_CTL	0x444609C4	Read address control. See SMIF0_CORE_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_RD_MODE_CTL	0x444609C8	Read mode control. See SMIF0_CORE_DEVICE0_RD_MODE_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_RD_DUMMY_CTL	0x444609CC	Read dummy control. See SMIF0_CORE_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_RD_DATA_CTL	0x444609D0	Read data control. See SMIF0_CORE_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_RD_BOUND_CTL	0x444609D8	Read boundary control. See SMIF0_CORE_DEVICE0_RD_BOUND_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_WR_CMD_CTL	0x444609E0	Write command control. See SMIF0_CORE_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_WR_ADDR_CTL	0x444609E4	Write address control. See SMIF0_CORE_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_WR_MODE_CTL	0x444609E8	Write mode control. See SMIF0_CORE_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_WR_DUMMY_CTL	0x444609EC	Write dummy control. See SMIF0_CORE_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_WR_DATA_CTL	0x444609F0	Write data control. See SMIF0_CORE_DEVICE0_WR_DATA_CTL for the details of bit fields.
SMIF0_CORE_DEVICE3_HB_FW_DEL_TAP_SEL_0	0x444609F8	HB FW Calibration Delay Tap Select 0. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0 for the details of bit fields.

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Register name	Address	Description
SMIF0_CORE_DEVICE3_HB_FW_DEL_TAP_SEL_1	0x444609FC	HB FW Calibration Delay Tap Select 1. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1 for the details of bit fields.
SMIF0_CORE_AXI_MPC0_CFG	0x44463000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CFG for the details of bit fields.
SMIF0_CORE_AXI_MPC0_CTRL	0x44463100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc). See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CTRL for the details of bit fields.
SMIF0_CORE_AXI_MPC0_BLK_MAX	0x44463104	Max value of block-based index register. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_MAX for the details of bit fields.
SMIF0_CORE_AXI_MPC0_BLK_CFG	0x44463108	Block size & initialization in progress. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_CFG for the details of bit fields.
SMIF0_CORE_AXI_MPC0_BLK_IDX	0x4446310C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc). See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_IDX for the details of bit fields.
SMIF0_CORE_AXI_MPC0_BLK_LUT	0x44463110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_LUT for the details of bit fields.
SMIF0_CORE_AXI_MPC0_ROT_CTRL	0x44463200	Control register with lock bit and auto-increment only. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_CTRL for the details of bit fields.
SMIF0_CORE_AXI_MPC0_ROT_BLK_MAX	0x44463208	Max value of block-based index register for ROT. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_MAX for the details of bit fields.
SMIF0_CORE_AXI_MPC0_ROT_BLK_CFG	0x4446320C	Same as BLK_CFG. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_CFG for the details of bit fields.
SMIF0_CORE_AXI_MPC0_ROT_BLK_IDX	0x44463210	Index of 8-block group accessed through ROT_BLK_LUT_*. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_IDX for the details of bit fields.

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Register name	Address	Description
SMIF0_CORE_AXI_MPC0_ROT_BLK_PC	0x44463214	Protection context of 8-block group accesses through ROT_BLK_LUT. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_PC for the details of bit fields.
SMIF0_CORE_AXI_MPC0_ROT_BLK_LUT	0x44463218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_CFG for the details of bit fields.
SMIF0_CORE_SMIF_HSIOM_SMIF_PRT0_PORT_SEL0	0x44464000	Port selection 0
SMIF0_CORE_SMIF_HSIOM_SMIF_PRT0_PORT_SEL1	0x44464004	Port selection 1
SMIF0_CORE_SMIF_HSIOM_SMIF_PRT1_PORT_SEL0	0x44464010	Port selection 0
SMIF0_CORE_SMIF_HSIOM_SMIF_PRT2_PORT_SEL0	0x44464020	Port selection 0
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT	0x44470000	Port output data register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_CLR	0x44470004	Port output data clear register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_SET	0x44470008	Port output data set register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_INV	0x4447000C	Port output data invert register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_IN	0x44470010	Port input state register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR	0x44470014	Port interrupt status register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_MASK	0x44470018	Port interrupt mask register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_MASKED	0x4447001C	Port interrupt masked status register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_SET	0x44470020	Port interrupt set register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_CFG	0x44470040	Port interrupt configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG	0x44470044	Port configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_IN	0x44470048	Port input buffer configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_OUT	0x4447004C	Port output buffer configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_SLEW_EXT	0x44470064	Port output buffer slew extension configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT0	0x44470068	Port output buffer drive sel extension configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT1	0x4447006C	Port output buffer drive sel extension configuration register

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_OUT	0x44470080	Port output data register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_OUT_CLR	0x44470084	Port output data clear register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_CLR for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_OUT_SET	0x44470088	Port output data set register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_SET for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_OUT_INV	0x4447008C	Port output data invert register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_INV for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_IN	0x44470090	Port input state register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR	0x44470094	Port interrupt status register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_MASK	0x44470098	Port interrupt mask register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_MASKED	0x4447009C	Port interrupt masked status register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_SET	0x444700A0	Port interrupt set register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_CFG	0x444700C0	Port interrupt configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG	0x444700C4	Port configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG_IN	0x444700C8	Port input buffer configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG_OUT	0x444700CC	Port output buffer configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG_SLEW_EXT	0x444700E4	Port output buffer slew extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_SLEW_EXT for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG_DRIVE_EXT0	0x444700E8	Port output buffer drive sel extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG_DRIVE_EXT1	0x444700EC	Port output buffer drive sel extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_OUT	0x44470100	Port output data register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_OUT_CLR	0x44470104	Port output data clear register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_CLR for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_OUT_SET	0x44470108	Port output data set register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_SET for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_OUT_INV	0x4447010C	Port output data invert register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_INV for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_IN	0x44470110	Port input state register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR	0x44470114	Port interrupt status register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR_MASK	0x44470118	Port interrupt mask register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR_MASKED	0x4447011C	Port interrupt masked status register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR_SET	0x44470120	Port interrupt set register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR_CFG	0x44470140	Port interrupt configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG	0x44470144	Port configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG_IN	0x44470148	Port input buffer configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG_OUT	0x4447014C	Port output buffer configuration register
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG_SLEW_EXT	0x44470164	Port output buffer slew extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_SLEW_EXT for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG_DRIVE_EXT0	0x44470168	Port output buffer drive sel extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG_DRIVE_EXT1	0x4447016C	Port output buffer drive sel extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_INTR_CAUSE00	0x44478000	Interrupt port cause register 0
SMIF0_CORE_SMIF_GPIO_INTR_CAUSE01	0x44478004	Interrupt port cause register 0. See SMIF0_CORE_SMIF_GPIO_INTR_CAUSE00 for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_INTR_CAUSE02	0x44478008	Interrupt port cause register 0. See SMIF0_CORE_SMIF_GPIO_INTR_CAUSE00 for the details of bit fields.
SMIF0_CORE_SMIF_GPIO_VDD_ACTIVE	0x44478010	Extern power supply detection register
SMIF0_CORE_SMIF_GPIO_VDD_INTR	0x44478014	Supply detection interrupt register
SMIF0_CORE_SMIF_GPIO_VDD_INTR_MASK	0x44478018	Supply detection interrupt mask register
SMIF0_CORE_SMIF_GPIO_VDD_INTR_MASKED	0x4447801C	Supply detection interrupt masked register
SMIF0_CORE_SMIF_GPIO_VDD_INTR_SET	0x44478020	Supply detection interrupt set register

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CACHE_BLOCK_HWPARAMS	0x44490000	Hardware Parameter register. See SMIF0_CACHE_BLOCK_HWPARAMS for the details of bit fields.
SMIF1_CACHE_BLOCK_CTRL	0x44490010	Control Register. See SMIF0_CACHE_BLOCK_CTRL for the details of bit fields.
SMIF1_CACHE_BLOCK_NSEC_ACCESS	0x44490014	Non-secure access information. See SMIF0_CACHE_BLOCK_NSEC_ACCESS for the details of bit fields.
SMIF1_CACHE_BLOCK_MAINT_CTRL_ALL	0x44490020	Maintenance control for the entire cache. See SMIF0_CACHE_BLOCK_MAINT_CTRL_ALL for the details of bit fields.
SMIF1_CACHE_BLOCK_MAINT_CTRL_LINES	0x44490024	Maintenance control for individual lines. See SMIF0_CACHE_BLOCK_MAINT_CTRL_LINES for the details of bit fields.
SMIF1_CACHE_BLOCK_MAINT_STATUS	0x44490028	Maintenance status for the cache. See SMIF0_CACHE_BLOCK_MAINT_STATUS for the details of bit fields.
SMIF1_CACHE_BLOCK_SECIRQSTAT	0x44490100	Secure Interrupt Request Status register. See SMIF0_CACHE_BLOCK_SECIRQSTAT for the details of bit fields.
SMIF1_CACHE_BLOCK_SECIRQSCLR	0x44490104	Secure Interrupt Status Clear register. See SMIF0_CACHE_BLOCK_SECIRQSCLR for the details of bit fields.
SMIF1_CACHE_BLOCK_SECIRQEN	0x44490108	Secure Interrupt Enable register. See SMIF0_CACHE_BLOCK_SECIRQEN for the details of bit fields.
SMIF1_CACHE_BLOCK_SECIRQINFO1	0x4449010C	Secure transfer error information 1. See SMIF0_CACHE_BLOCK_SECIRQINFO1 for the details of bit fields.
SMIF1_CACHE_BLOCK_SECIRQINFO2	0x44490110	Secure transfer error information 2. See SMIF0_CACHE_BLOCK_SECIRQINFO2 for the details of bit fields.
SMIF1_CACHE_BLOCK_NSECIRQSTAT	0x44490140	Non-secure Interrupt Request Status register. See SMIF0_CACHE_BLOCK_NSECIRQSTAT for the details of bit fields.
SMIF1_CACHE_BLOCK_NSECIRQSCLR	0x44490144	Non-secure Interrupt Status Clear register. See SMIF0_CACHE_BLOCK_NSECIRQSCLR for the details of bit fields.
SMIF1_CACHE_BLOCK_NSECIRQEN	0x44490148	Non-secure Interrupt Enable register. See SMIF0_CACHE_BLOCK_NSECIRQEN for the details of bit fields.
SMIF1_CACHE_BLOCK_NSECIRQINFO1	0x4449014C	Non-secure transfer error information 1. See SMIF0_CACHE_BLOCK_NSECIRQINFO1 for the details of bit fields.

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Register name	Address	Description
SMIF1_CACHE_BLOCK_NSECIRQINFO2	0x44490150	Non-secure transfer error information 2. See SMIF0_CACHE_BLOCK_NSECIRQINFO2 for the details of bit fields.
SMIF1_CACHE_BLOCK_SECHIT	0x44490300	Secure transfers Hit register. See SMIF0_CACHE_BLOCK_SECHIT for the details of bit fields.
SMIF1_CACHE_BLOCK_SECMISS	0x44490304	Secure transfers Miss register. See SMIF0_CACHE_BLOCK_SECMISS for the details of bit fields.
SMIF1_CACHE_BLOCK_SECSTATCTRL	0x44490308	Secure transfers statistic counters control. See SMIF0_CACHE_BLOCK_SECSTATCTRL for the details of bit fields.
SMIF1_CACHE_BLOCK_NSECHIT	0x44490310	Non-secure transfers Hit register. See SMIF0_CACHE_BLOCK_NSECHIT for the details of bit fields.
SMIF1_CACHE_BLOCK_NSECMISS	0x44490314	Non-secure transfers Miss register. See SMIF0_CACHE_BLOCK_NSECMISS for the details of bit fields.
SMIF1_CACHE_BLOCK_NSECSTATCTRL	0x44490318	Non-secure transfers statistic counters control. See SMIF0_CACHE_BLOCK_NSECSTATCTRL for the details of bit fields.
SMIF1_CACHE_BLOCK_PMSVR0	0x44490600	Saved Value Register 0 - Secure Hit. See SMIF0_CACHE_BLOCK_PMSVR0 for the details of bit fields.
SMIF1_CACHE_BLOCK_PMSVR1	0x44490604	Saved Value Register 1 - Secure Miss. See SMIF0_CACHE_BLOCK_PMSVR1 for the details of bit fields.
SMIF1_CACHE_BLOCK_PMSVR2	0x44490608	Saved Value Register 2 - Non-secure Hit. See SMIF0_CACHE_BLOCK_PMSVR2 for the details of bit fields.
SMIF1_CACHE_BLOCK_PMSVR3	0x4449060C	Saved Value Register 3 - Non-secure Miss. See SMIF0_CACHE_BLOCK_PMSVR3 for the details of bit fields.
SMIF1_CACHE_BLOCK_PMSSSR	0x44490680	PMU Snapshot Status Register. See SMIF0_CACHE_BLOCK_PMSSSR for the details of bit fields.
SMIF1_CACHE_BLOCK_PMSSCR	0x444906F0	PMU Snapshot Capture Register. See SMIF0_CACHE_BLOCK_PMSSCR for the details of bit fields.
SMIF1_CACHE_BLOCK_PMSSRR	0x444906F4	PMU Snapshot Reset Register. See SMIF0_CACHE_BLOCK_PMSSRR for the details of bit fields.
SMIF1_CACHE_BLOCK_PIDR4	0x44490FD0	Peripheral ID 4. See SMIF0_CACHE_BLOCK_PIDR4 for the details of bit fields.

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Register name	Address	Description
SMIF1_CACHE_BLOCK_PIDR5	0x44490FD4	Peripheral ID 5. See SMIF0_CACHE_BLOCK_PIDR5 for the details of bit fields.
SMIF1_CACHE_BLOCK_PIDR6	0x44490FD8	Peripheral ID 6. See SMIF0_CACHE_BLOCK_PIDR6 for the details of bit fields.
SMIF1_CACHE_BLOCK_PIDR7	0x44490FDC	Peripheral ID 7. See SMIF0_CACHE_BLOCK_PIDR7 for the details of bit fields.
SMIF1_CACHE_BLOCK_PIDR0	0x44490FE0	Peripheral ID 0. See SMIF0_CACHE_BLOCK_PIDR0 for the details of bit fields.
SMIF1_CACHE_BLOCK_PIDR1	0x44490FE4	Peripheral ID 1. See SMIF0_CACHE_BLOCK_PIDR1 for the details of bit fields.
SMIF1_CACHE_BLOCK_PIDR2	0x44490FE8	Peripheral ID 2. See SMIF0_CACHE_BLOCK_PIDR2 for the details of bit fields.
SMIF1_CACHE_BLOCK_PIDR3	0x44490FEC	Peripheral ID 3. See SMIF0_CACHE_BLOCK_PIDR3 for the details of bit fields.
SMIF1_CACHE_BLOCK_CIDR0	0x44490FF0	Component ID 0. See SMIF0_CACHE_BLOCK_CIDR0 for the details of bit fields.
SMIF1_CACHE_BLOCK_CIDR1	0x44490FF4	Component ID 1. See SMIF0_CACHE_BLOCK_CIDR1 for the details of bit fields.
SMIF1_CACHE_BLOCK_CIDR2	0x44490FF8	Component ID 2. See SMIF0_CACHE_BLOCK_CIDR2 for the details of bit fields.
SMIF1_CACHE_BLOCK_CIDR3	0x44490FFC	Component ID 3. See SMIF0_CACHE_BLOCK_CIDR3 for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_BYPASS_WI	0x44492000	Bypass wrap to increment conversion logic. See SMIF0_CACHE_BLOCK_MMIO_BYPASS_WI for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_MASTER_ID	0x44492004	The cache generates transactions (linefill and eviction Write-Back) that are marked with the value specified by MASTER_ID on hmaster_m. See SMIF0_CACHE_BLOCK_MMIO_MASTER_ID for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_DIS_CACHE_EN_MAINT	0x44492008	This signal turns on/off cache enable maintenance. See SMIF0_CACHE_BLOCK_MMIO_DIS_CACHE_EN_MAINT for the details of bit fields.

Register name	Address	Description
SMIF1_CACHE_BLOCK_MMIO_DIS_CACHE_DIS_MAINT	0x4449200C	This signal turns on/off cache disable maintenance. See SMIF0_CACHE_BLOCK_MMIO_DIS_CACHE_DIS_MAINT for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_APB_VIOLATION_RESP	0x44492010	This signal controls if the APB interface of cache responds with an error to illegal operations on the APB interface. Illegal operations on the APB interface include Writing with no full write strobe, Accessing non-word aligned addresses, Instruction accesses, Non-privileged accesses 1 - The Cache responds with an APB error. Read data is masked with zeros and write data is ignored. 0 - The Cache sends an OK response. Read data is masked with zeros and write data is ignored. See SMIF0_CACHE_BLOCK_MMIO_APB_VIOLATION_RESP for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_MMIO_ACTIVE_EN	0x44492014	SW control to put SMIF.6 in active or clock gated mode. See SMIF0_CACHE_BLOCK_MMIO_MMIO_ACTIVE_EN for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_POWER_ON_ENABLE	0x44492018	This signal configures the cache to enable the cache automatically after powerup. See SMIF0_CACHE_BLOCK_MMIO_POWER_ON_ENABLE for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_MMIO_CACHE_RET_EN	0x4449201C	Controls if cache SRAMs are retained during DPSLP. See SMIF0_CACHE_BLOCK_MMIO_MMIO_CACHE_RET_EN for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_DIS_PWR_DOWN_MAINT	0x44492020	This signal turns on/off powerdown maintenance. See SMIF0_CACHE_BLOCK_MMIO_DIS_PWR_DOWN_MAINT for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_REGION0_BASE	0x44492024	Region 0 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle. See SMIF0_CACHE_BLOCK_MMIO_REGION0_BASE for the details of bit fields.

Register name	Address	Description
SMIF1_CACHE_BLOCK_MMIO_REGION0_LIMIT	0x44492028	Region 0 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle. See SMIF0_CACHE_BLOCK_MMIO_REGION0_LIMIT for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_REGION1_BASE	0x4449202C	Region 1 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle. See SMIF0_CACHE_BLOCK_MMIO_REGION1_BASE for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_REGION1_LIMIT	0x44492030	Region 1 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle. See SMIF0_CACHE_BLOCK_MMIO_REGION1_LIMIT for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_REGION2_BASE	0x44492034	Region 2 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle. See SMIF0_CACHE_BLOCK_MMIO_REGION2_BASE for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_REGION2_LIMIT	0x44492038	Region 2 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle. See SMIF0_CACHE_BLOCK_MMIO_REGION2_LIMIT for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_REGION3_BASE	0x4449203C	Region 3 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle. See SMIF0_CACHE_BLOCK_MMIO_REGION3_BASE for the details of bit fields.
SMIF1_CACHE_BLOCK_MMIO_REGION3_LIMIT	0x44492040	Region 3 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle. See SMIF0_CACHE_BLOCK_MMIO_REGION3_LIMIT for the details of bit fields.

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Register name	Address	Description
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CFG	0x44494000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CFG for the details of bit fields.
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CTRL	0x44494100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc). See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CTRL for the details of bit fields.
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_MAX	0x44494104	Max value of block-based index register. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_MAX for the details of bit fields.
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_CFG	0x44494108	Block size & initialization in progress. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_CFG for the details of bit fields.
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_IDX	0x4449410C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc). See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_IDX for the details of bit fields.
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_LUT	0x44494110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_LUT for the details of bit fields.
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_CTRL	0x44494200	Control register with lock bit and auto-increment only. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_CTRL for the details of bit fields.
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_MAX	0x44494208	Max value of block-based index register for ROT. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_MAX for the details of bit fields.
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_CFG	0x4449420C	Same as BLK_CFG. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_CFG for the details of bit fields.
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_IDX	0x44494210	Index of 8-block group accessed through ROT_BLK_LUT_*. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_IDX for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_PC	0x44494214	Protection context of 8-block group accesses through ROT_BLK_LUT. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_PC for the details of bit fields.
SMIF1_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_LUT	0x44494218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_CFG for the details of bit fields.
SMIF1_CORE_CTL	0x444A0000	Control. See SMIF0_CORE_CTL for the details of bit fields.
SMIF1_CORE_STATUS	0x444A0004	Status. See SMIF0_CORE_STATUS for the details of bit fields.
SMIF1_CORE_CTL2	0x444A0008	Control 2. See SMIF0_CORE_CTL2 for the details of bit fields.
SMIF1_CORE_DLP_DELAY_TAP_SEL0	0x444A0010	DLP Delay Tap Select Register 0. See SMIF0_CORE_DLP_DELAY_TAP_SEL0 for the details of bit fields.
SMIF1_CORE_DLP_DELAY_TAP_SEL1	0x444A0014	DLP Delay Tap Select Register 1. See SMIF0_CORE_DLP_DELAY_TAP_SEL1 for the details of bit fields.
SMIF1_CORE_DLP_CTL	0x444A0018	DLP Control Register. See SMIF0_CORE_DLP_CTL for the details of bit fields.
SMIF1_CORE_DLP_STATUS0	0x444A0020	DLP Status Register 0. See SMIF0_CORE_DLP_STATUS0 for the details of bit fields.
SMIF1_CORE_DLP_STATUS1	0x444A0024	DLP Status Register 1. See SMIF0_CORE_DLP_STATUS1 for the details of bit fields.
SMIF1_CORE_TX_CMD_FIFO_STATUS	0x444A0044	Transmitter command FIFO status. See SMIF0_CORE_TX_CMD_FIFO_STATUS for the details of bit fields.
SMIF1_CORE_TX_CMD_MMIO_FIFO_STATUS	0x444A0048	Transmitter command MMIO FIFO status. See SMIF0_CORE_TX_CMD_MMIO_FIFO_STATUS for the details of bit fields.
SMIF1_CORE_TX_CMD_MMIO_FIFO_WR	0x444A0050	Transmitter command MMIO FIFO write. See SMIF0_CORE_TX_CMD_MMIO_FIFO_WR for the details of bit fields.
SMIF1_CORE_TX_DATA_MMIO_FIFO_CTL	0x444A0080	Transmitter data MMIO FIFO control. See SMIF0_CORE_TX_DATA_MMIO_FIFO_CTL for the details of bit fields.
SMIF1_CORE_TX_DATA_FIFO_STATUS	0x444A0084	Transmitter data FIFO status. See SMIF0_CORE_TX_DATA_FIFO_STATUS for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_TX_DATA_MMIO_FIFO_STATUS	0x444A0088	Transmitter data MMIO FIFO status. See SMIF0_CORE_TX_DATA_MMIO_FIFO_STATUS for the details of bit fields.
SMIF1_CORE_TX_DATA_MMIO_FIFO_WR1	0x444A0090	Transmitter data MMIO FIFO write. See SMIF0_CORE_TX_DATA_MMIO_FIFO_WR1 for the details of bit fields.
SMIF1_CORE_TX_DATA_MMIO_FIFO_WR2	0x444A0094	Transmitter data MMIO FIFO write. See SMIF0_CORE_TX_DATA_MMIO_FIFO_WR2 for the details of bit fields.
SMIF1_CORE_TX_DATA_MMIO_FIFO_WR4	0x444A0098	Transmitter data MMIO FIFO write. See SMIF0_CORE_TX_DATA_MMIO_FIFO_WR4 for the details of bit fields.
SMIF1_CORE_TX_DATA_MMIO_FIFO_WR1ODD	0x444A009C	Transmitter data MMIO FIFO write. See SMIF0_CORE_TX_DATA_MMIO_FIFO_WR1ODD for the details of bit fields.
SMIF1_CORE_RX_DATA_MMIO_FIFO_CTL	0x444A00C0	Receiver data MMIO FIFO control. See SMIF0_CORE_RX_DATA_MMIO_FIFO_CTL for the details of bit fields.
SMIF1_CORE_RX_DATA_MMIO_FIFO_STATUS	0x444A00C4	Receiver data MMIO FIFO status. See SMIF0_CORE_RX_DATA_MMIO_FIFO_STATUS for the details of bit fields.
SMIF1_CORE_RX_DATA_FIFO_STATUS	0x444A00C8	Receiver data FIFO status. See SMIF0_CORE_RX_DATA_FIFO_STATUS for the details of bit fields.
SMIF1_CORE_RX_DATA_MMIO_FIFO_RD1	0x444A00D0	Receiver data MMIO FIFO read. See SMIF0_CORE_RX_DATA_MMIO_FIFO_RD1 for the details of bit fields.
SMIF1_CORE_RX_DATA_MMIO_FIFO_RD2	0x444A00D4	Receiver data MMIO FIFO read. See SMIF0_CORE_RX_DATA_MMIO_FIFO_RD2 for the details of bit fields.
SMIF1_CORE_RX_DATA_MMIO_FIFO_RD4	0x444A00D8	Receiver data MMIO FIFO read. See SMIF0_CORE_RX_DATA_MMIO_FIFO_RD4 for the details of bit fields.
SMIF1_CORE_RX_DATA_MMIO_FIFO_RD1_SILENT	0x444A00E0	Receiver data MMIO FIFO silent read. See SMIF0_CORE_RX_DATA_MMIO_FIFO_RD1_SILENT for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_CMD	0x444A0200	Cryptography command. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_CMD for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_ADDR	0x444A0204	Cryptography base address. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_ADDR for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_MASK	0x444A0208	Cryptography mask. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_MASK for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_SUBREGION	0x444A020C	Cryptography subregion disable. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_SUBREGION for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_INPUT0	0x444A0220	Cryptography input 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_INPUT1	0x444A0224	Cryptography input 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_INPUT2	0x444A0228	Cryptography input 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_INPUT3	0x444A022C	Cryptography input 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT3 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_KEY0	0x444A0240	Cryptography key 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_KEY1	0x444A0244	Cryptography key 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_KEY2	0x444A0248	Cryptography key 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_KEY3	0x444A024C	Cryptography key 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY3 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT0	0x444A0260	Cryptography output 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT1	0x444A0264	Cryptography output 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT2	0x444A0268	Cryptography output 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT3	0x444A026C	Cryptography output 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT3 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_CMD	0x444A0280	Cryptography command. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_CMD for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_ADDR	0x444A0284	Cryptography base address. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_ADDR for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_MASK	0x444A0288	Cryptography mask. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_MASK for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_SUBREGION	0x444A028C	Cryptography subregion disable. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_SUBREGION for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_INPUT0	0x444A02A0	Cryptography input 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_INPUT1	0x444A02A4	Cryptography input 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_INPUT2	0x444A02A8	Cryptography input 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_INPUT3	0x444A02AC	Cryptography input 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT3 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_KEY0	0x444A02C0	Cryptography key 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_KEY1	0x444A02C4	Cryptography key 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_KEY2	0x444A02C8	Cryptography key 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_KEY3	0x444A02CC	Cryptography key 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY3 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_OUTPUT0	0x444A02E0	Cryptography output 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_OUTPUT1	0x444A02E4	Cryptography output 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_OUTPUT2	0x444A02E8	Cryptography output 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO1_CRYPTO_OUTPUT3	0x444A02EC	Cryptography output 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT3 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_CMD	0x444A0300	Cryptography command. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_CMD for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_ADDR	0x444A0304	Cryptography base address. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_ADDR for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_MASK	0x444A0308	Cryptography mask. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_MASK for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_SUBREGION	0x444A030C	Cryptography subregion disable. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_SUBREGION for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_INPUT0	0x444A0320	Cryptography input 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_INPUT1	0x444A0324	Cryptography input 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_INPUT2	0x444A0328	Cryptography input 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_INPUT3	0x444A032C	Cryptography input 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT3 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_KEY0	0x444A0340	Cryptography key 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_KEY1	0x444A0344	Cryptography key 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_KEY2	0x444A0348	Cryptography key 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_KEY3	0x444A034C	Cryptography key 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY3 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_OUTPUT0	0x444A0360	Cryptography output 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_OUTPUT1	0x444A0364	Cryptography output 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_OUTPUT2	0x444A0368	Cryptography output 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO2_CRYPTO_OUTPUT3	0x444A036C	Cryptography output 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT3 for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_CMD	0x444A0380	Cryptography command. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_CMD for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_ADDR	0x444A0384	Cryptography base address. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_ADDR for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_MASK	0x444A0388	Cryptography mask. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_MASK for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_SUBREGION	0x444A038C	Cryptography subregion disable. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_SUBREGION for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_INPUT0	0x444A03A0	Cryptography input 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_INPUT1	0x444A03A4	Cryptography input 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_INPUT2	0x444A03A8	Cryptography input 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_INPUT3	0x444A03AC	Cryptography input 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT3 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_KEY0	0x444A03C0	Cryptography key 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_KEY1	0x444A03C4	Cryptography key 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_KEY2	0x444A03C8	Cryptography key 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY2 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_KEY3	0x444A03CC	Cryptography key 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY3 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_OUTPUT0	0x444A03E0	Cryptography output 0. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT0 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_OUTPUT1	0x444A03E4	Cryptography output 1. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT1 for the details of bit fields.
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_OUTPUT2	0x444A03E8	Cryptography output 2. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT2 for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_SMIF_CRYPTO3_CRYPTO_OUTPUT3	0x444A03EC	Cryptography output 3. See SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT3 for the details of bit fields.
SMIF1_CORE_INTR	0x444A07C0	Interrupt register. See SMIF0_CORE_INTR for the details of bit fields.
SMIF1_CORE_INTR_SET	0x444A07C4	Interrupt set register. See SMIF0_CORE_INTR_SET for the details of bit fields.
SMIF1_CORE_INTR_MASK	0x444A07C8	Interrupt mask register. See SMIF0_CORE_INTR_MASK for the details of bit fields.
SMIF1_CORE_INTR_MASKED	0x444A07CC	Interrupt masked register. See SMIF0_CORE_INTR_MASKED for the details of bit fields.
SMIF1_CORE_DLL_IDAC	0x444A07D8	DLL IDAC (when DLL runs in open loop, selects the delay of the delay line). See SMIF0_CORE_DLL_IDAC for the details of bit fields.
SMIF1_CORE_DLL_IVR	0x444A07DC	DLL IVR (Contol Output Voltage of internal Voltage Regulator). See SMIF0_CORE_DLL_IVR for the details of bit fields.
SMIF1_CORE_DEVICE0_CTL	0x444A0800	Control. See SMIF0_CORE_DEVICE0_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_ADDR	0x444A0808	Device region base address. See SMIF0_CORE_DEVICE0_ADDR for the details of bit fields.
SMIF1_CORE_DEVICE0_MASK	0x444A080C	Device region mask. See SMIF0_CORE_DEVICE0_MASK for the details of bit fields.
SMIF1_CORE_DEVICE0_ADDR_CTL	0x444A0820	Address control. See SMIF0_CORE_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_RX_CAPTURE_CONFIG	0x444A0828	RX capture configuration. See SMIF0_CORE_DEVICE0_RX_CAPTURE_CONFIG for the details of bit fields.
SMIF1_CORE_DEVICE0_RD_CMD_CTL	0x444A0840	Read command control. See SMIF0_CORE_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_RD_ADDR_CTL	0x444A0844	Read address control. See SMIF0_CORE_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_RD_MODE_CTL	0x444A0848	Read mode control. See SMIF0_CORE_DEVICE0_RD_MODE_CTL for the details of bit fields.

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Register name	Address	Description
SMIF1_CORE_DEVICE0_RD_DUMMY_CTL	0x444A084C	Read dummy control. See SMIF0_CORE_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_RD_DATA_CTL	0x444A0850	Read data control. See SMIF0_CORE_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_RD_BOUND_CTL	0x444A0858	Read boundary control. See SMIF0_CORE_DEVICE0_RD_BOUND_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_WR_CMD_CTL	0x444A0860	Write command control. See SMIF0_CORE_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_WR_ADDR_CTL	0x444A0864	Write address control. See SMIF0_CORE_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_WR_MODE_CTL	0x444A0868	Write mode control. See SMIF0_CORE_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_WR_DUMMY_CTL	0x444A086C	Write dummy control. See SMIF0_CORE_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_WR_DATA_CTL	0x444A0870	Write data control. See SMIF0_CORE_DEVICE0_WR_DATA_CTL for the details of bit fields.
SMIF1_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0	0x444A0878	HB FW Calibration Delay Tap Select 0. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0 for the details of bit fields.
SMIF1_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1	0x444A087C	HB FW Calibration Delay Tap Select 1. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1 for the details of bit fields.
SMIF1_CORE_DEVICE1_CTL	0x444A0880	Control. See SMIF0_CORE_DEVICE0_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_ADDR	0x444A0888	Device region base address. See SMIF0_CORE_DEVICE0_ADDR for the details of bit fields.
SMIF1_CORE_DEVICE1_MASK	0x444A088C	Device region mask. See SMIF0_CORE_DEVICE0_MASK for the details of bit fields.
SMIF1_CORE_DEVICE1_ADDR_CTL	0x444A08A0	Address control. See SMIF0_CORE_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_RX_CAPTURE_CONFIG	0x444A08A8	RX capture configuration. See SMIF0_CORE_DEVICE0_RX_CAPTURE_CONFIG for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_DEVICE1_RD_CMD_CTL	0x444A08C0	Read command control. See SMIF0_CORE_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_RD_ADDR_CTL	0x444A08C4	Read address control. See SMIF0_CORE_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_RD_MODE_CTL	0x444A08C8	Read mode control. See SMIF0_CORE_DEVICE0_RD_MODE_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_RD_DUMMY_CTL	0x444A08CC	Read dummy control. See SMIF0_CORE_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_RD_DATA_CTL	0x444A08D0	Read data control. See SMIF0_CORE_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_RD_BOUND_CTL	0x444A08D8	Read boundary control. See SMIF0_CORE_DEVICE0_RD_BOUND_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_WR_CMD_CTL	0x444A08E0	Write command control. See SMIF0_CORE_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_WR_ADDR_CTL	0x444A08E4	Write address control. See SMIF0_CORE_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_WR_MODE_CTL	0x444A08E8	Write mode control. See SMIF0_CORE_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_WR_DUMMY_CTL	0x444A08EC	Write dummy control. See SMIF0_CORE_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_WR_DATA_CTL	0x444A08F0	Write data control. See SMIF0_CORE_DEVICE0_WR_DATA_CTL for the details of bit fields.
SMIF1_CORE_DEVICE1_HB_FW_DEL_TAP_SEL_0	0x444A08F8	HB FW Calibration Delay Tap Select 0. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0 for the details of bit fields.
SMIF1_CORE_DEVICE1_HB_FW_DEL_TAP_SEL_1	0x444A08FC	HB FW Calibration Delay Tap Select 1. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1 for the details of bit fields.
SMIF1_CORE_DEVICE2_CTL	0x444A0900	Control. See SMIF0_CORE_DEVICE0_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_ADDR	0x444A0908	Device region base address. See SMIF0_CORE_DEVICE0_ADDR for the details of bit fields.

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Register name	Address	Description
SMIF1_CORE_DEVICE2_MASK	0x444A090C	Device region mask. See SMIF0_CORE_DEVICE0_MASK for the details of bit fields.
SMIF1_CORE_DEVICE2_ADDR_CTL	0x444A0920	Address control. See SMIF0_CORE_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_RX_CAPTURE_CONFIG	0x444A0928	RX capture configuration. See SMIF0_CORE_DEVICE0_RX_CAPTURE_CONFIG for the details of bit fields.
SMIF1_CORE_DEVICE2_RD_CMD_CTL	0x444A0940	Read command control. See SMIF0_CORE_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_RD_ADDR_CTL	0x444A0944	Read address control. See SMIF0_CORE_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_RD_MODE_CTL	0x444A0948	Read mode control. See SMIF0_CORE_DEVICE0_RD_MODE_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_RD_DUMMY_CTL	0x444A094C	Read dummy control. See SMIF0_CORE_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_RD_DATA_CTL	0x444A0950	Read data control. See SMIF0_CORE_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_RD_BOUND_CTL	0x444A0958	Read boundary control. See SMIF0_CORE_DEVICE0_RD_BOUND_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_WR_CMD_CTL	0x444A0960	Write command control. See SMIF0_CORE_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_WR_ADDR_CTL	0x444A0964	Write address control. See SMIF0_CORE_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_WR_MODE_CTL	0x444A0968	Write mode control. See SMIF0_CORE_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_WR_DUMMY_CTL	0x444A096C	Write dummy control. See SMIF0_CORE_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_WR_DATA_CTL	0x444A0970	Write data control. See SMIF0_CORE_DEVICE0_WR_DATA_CTL for the details of bit fields.
SMIF1_CORE_DEVICE2_HB_FW_DEL_TAP_SEL_0	0x444A0978	HB FW Calibration Delay Tap Select 0. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0 for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_DEVICE2_HB_FW_DEL_TAP_SEL_1	0x444A097C	HB FW Calibration Delay Tap Select 1. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1 for the details of bit fields.
SMIF1_CORE_DEVICE3_CTL	0x444A0980	Control. See SMIF0_CORE_DEVICE0_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_ADDR	0x444A0988	Device region base address. See SMIF0_CORE_DEVICE0_ADDR for the details of bit fields.
SMIF1_CORE_DEVICE3_MASK	0x444A098C	Device region mask. See SMIF0_CORE_DEVICE0_MASK for the details of bit fields.
SMIF1_CORE_DEVICE3_ADDR_CTL	0x444A09A0	Address control. See SMIF0_CORE_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_RX_CAPTURE_CONFIG	0x444A09A8	RX capture configuration. See SMIF0_CORE_DEVICE0_RX_CAPTURE_CONFIG for the details of bit fields.
SMIF1_CORE_DEVICE3_RD_CMD_CTL	0x444A09C0	Read command control. See SMIF0_CORE_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_RD_ADDR_CTL	0x444A09C4	Read address control. See SMIF0_CORE_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_RD_MODE_CTL	0x444A09C8	Read mode control. See SMIF0_CORE_DEVICE0_RD_MODE_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_RD_DUMMY_CTL	0x444A09CC	Read dummy control. See SMIF0_CORE_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_RD_DATA_CTL	0x444A09D0	Read data control. See SMIF0_CORE_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_RD_BOUND_CTL	0x444A09D8	Read boundary control. See SMIF0_CORE_DEVICE0_RD_BOUND_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_WR_CMD_CTL	0x444A09E0	Write command control. See SMIF0_CORE_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_WR_ADDR_CTL	0x444A09E4	Write address control. See SMIF0_CORE_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_WR_MODE_CTL	0x444A09E8	Write mode control. See SMIF0_CORE_DEVICE0_WR_MODE_CTL for the details of bit fields.

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Register name	Address	Description
SMIF1_CORE_DEVICE3_WR_DUMMY_CTL	0x444A09EC	Write dummy control. See SMIF0_CORE_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_WR_DATA_CTL	0x444A09F0	Write data control. See SMIF0_CORE_DEVICE0_WR_DATA_CTL for the details of bit fields.
SMIF1_CORE_DEVICE3_HB_FW_DEL_TAP_SEL_0	0x444A09F8	HB FW Calibration Delay Tap Select 0. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0 for the details of bit fields.
SMIF1_CORE_DEVICE3_HB_FW_DEL_TAP_SEL_1	0x444A09FC	HB FW Calibration Delay Tap Select 1. See SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1 for the details of bit fields.
SMIF1_CORE_AXI_MPC0_CFG	0x444A3000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CFG for the details of bit fields.
SMIF1_CORE_AXI_MPC0_CTRL	0x444A3100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc). See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CTRL for the details of bit fields.
SMIF1_CORE_AXI_MPC0_BLK_MAX	0x444A3104	Max value of block-based index register. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_MAX for the details of bit fields.
SMIF1_CORE_AXI_MPC0_BLK_CFG	0x444A3108	Block size & initialization in progress. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_CFG for the details of bit fields.
SMIF1_CORE_AXI_MPC0_BLK_IDX	0x444A310C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc). See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_IDX for the details of bit fields.
SMIF1_CORE_AXI_MPC0_BLK_LUT	0x444A3110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_LUT for the details of bit fields.
SMIF1_CORE_AXI_MPC0_ROT_CTRL	0x444A3200	Control register with lock bit and auto-increment only. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_CTRL for the details of bit fields.

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Register name	Address	Description
SMIF1_CORE_AXI_MPC0_ROT_BLK_MAX	0x444A3208	Max value of block-based index register for ROT. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_MAX for the details of bit fields.
SMIF1_CORE_AXI_MPC0_ROT_BLK_CFG	0x444A320C	Same as BLK_CFG. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_CFG for the details of bit fields.
SMIF1_CORE_AXI_MPC0_ROT_BLK_IDX	0x444A3210	Index of 8-block group accessed through ROT_BLK_LUT_*. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_IDX for the details of bit fields.
SMIF1_CORE_AXI_MPC0_ROT_BLK_PC	0x444A3214	Protection context of 8-block group accesses through ROT_BLK_LUT. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_PC for the details of bit fields.
SMIF1_CORE_AXI_MPC0_ROT_BLK_LUT	0x444A3218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC. See SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_CFG for the details of bit fields.
SMIF1_CORE_SMIF_HSIOM_SMIF_PRT0_PORT_SEL0	0x444A4000	Port selection 0. See SMIF0_CORE_SMIF_HSIOM_SMIF_PRT0_PORT_SEL0 for the details of bit fields.
SMIF1_CORE_SMIF_HSIOM_SMIF_PRT0_PORT_SEL1	0x444A4004	Port selection 1. See SMIF0_CORE_SMIF_HSIOM_SMIF_PRT0_PORT_SEL1 for the details of bit fields.
SMIF1_CORE_SMIF_HSIOM_SMIF_PRT1_PORT_SEL0	0x444A4010	Port selection 0. See SMIF0_CORE_SMIF_HSIOM_SMIF_PRT1_PORT_SEL0 for the details of bit fields.
SMIF1_CORE_SMIF_HSIOM_SMIF_PRT2_PORT_SEL0	0x444A4020	Port selection 0. See SMIF0_CORE_SMIF_HSIOM_SMIF_PRT2_PORT_SEL0 for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_OUT	0x444B0000	Port output data register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_OUT_CLR	0x444B0004	Port output data clear register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_CLR for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_OUT_SET	0x444B0008	Port output data set register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_SET for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_OUT_INV	0x444B000C	Port output data invert register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_INV for the details of bit fields.

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Register name	Address	Description
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_IN	0x444B0010	Port input state register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_IN for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_INTR	0x444B0014	Port interrupt status register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_INTR_MASK	0x444B0018	Port interrupt mask register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_MASK for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_INTR_MASKED	0x444B001C	Port interrupt masked status register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_MASKED for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_INTR_SET	0x444B0020	Port interrupt set register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_SET for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_INTR_CFG	0x444B0040	Port interrupt configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_CFG for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_CFG	0x444B0044	Port configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_CFG_IN	0x444B0048	Port input buffer configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_IN for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_CFG_OUT	0x444B004C	Port output buffer configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_OUT for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_CFG_SLEW_EXT	0x444B0064	Port output buffer slew extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_SLEW_EXT for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT0	0x444B0068	Port output buffer drive sel extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT1	0x444B006C	Port output buffer drive sel extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_OUT	0x444B0080	Port output data register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_OUT for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_OUT_CLR	0x444B0084	Port output data clear register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_CLR for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_OUT_SET	0x444B0088	Port output data set register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_SET for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_OUT_INV	0x444B008C	Port output data invert register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_INV for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_IN	0x444B0090	Port input state register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_IN for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_INTR	0x444B0094	Port interrupt status register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_INTR_MASK	0x444B0098	Port interrupt mask register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_MASK for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_INTR_MASKED	0x444B009C	Port interrupt masked status register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_MASKED for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_INTR_SET	0x444B00A0	Port interrupt set register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_SET for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_INTR_CFG	0x444B00C0	Port interrupt configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_CFG for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_CFG	0x444B00C4	Port configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_CFG_IN	0x444B00C8	Port input buffer configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG_IN for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_CFG_OUT	0x444B00CC	Port output buffer configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG_OUT for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_CFG_SLEW_EXT	0x444B00E4	Port output buffer slew extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_SLEW_EXT for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_CFG_DRIVE_EXT0	0x444B00E8	Port output buffer drive sel extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT1_CFG_DRIVE_EXT1	0x444B00EC	Port output buffer drive sel extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_OUT	0x444B0100	Port output data register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_OUT for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_OUT_CLR	0x444B0104	Port output data clear register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_CLR for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_OUT_SET	0x444B0108	Port output data set register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_SET for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_OUT_INV	0x444B010C	Port output data invert register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_INV for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_IN	0x444B0110	Port input state register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_IN for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_INTR	0x444B0114	Port interrupt status register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_INTR_MASK	0x444B0118	Port interrupt mask register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_MASK for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_INTR_MASKED	0x444B011C	Port interrupt masked status register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_MASKED for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_INTR_SET	0x444B0120	Port interrupt set register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_SET for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_INTR_CFG	0x444B0140	Port interrupt configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_CFG for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_CFG	0x444B0144	Port configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_CFG_IN	0x444B0148	Port input buffer configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG_IN for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_CFG_OUT	0x444B014C	Port output buffer configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG_OUT for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_CFG_SLEW_EXT	0x444B0164	Port output buffer slew extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_SLEW_EXT for the details of bit fields.

Serial Memory Interface (SMIF) registers

Register name	Address	Description
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_CFG_DRIVE_EXT0	0x444B0168	Port output buffer drive sel extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_SMIF_PRT2_CFG_DRIVE_EXT1	0x444B016C	Port output buffer drive sel extension configuration register. See SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_INTR_CAUSE00	0x444B8000	Interrupt port cause register 0. See SMIF0_CORE_SMIF_GPIO_INTR_CAUSE00 for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_INTR_CAUSE01	0x444B8004	Interrupt port cause register 0. See SMIF0_CORE_SMIF_GPIO_INTR_CAUSE00 for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_INTR_CAUSE02	0x444B8008	Interrupt port cause register 0. See SMIF0_CORE_SMIF_GPIO_INTR_CAUSE00 for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_VDD_ACTIVE	0x444B8010	Extern power supply detection register. See SMIF0_CORE_SMIF_GPIO_VDD_ACTIVE for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_VDD_INTR	0x444B8014	Supply detection interrupt register. See SMIF0_CORE_SMIF_GPIO_VDD_INTR for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_VDD_INTR_MASK	0x444B8018	Supply detection interrupt mask register. See SMIF0_CORE_SMIF_GPIO_VDD_INTR_MASK for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_VDD_INTR_MASKED	0x444B801C	Supply detection interrupt masked register. See SMIF0_CORE_SMIF_GPIO_VDD_INTR_MASKED for the details of bit fields.
SMIF1_CORE_SMIF_GPIO_VDD_INTR_SET	0x444B8020	Supply detection interrupt set register. See SMIF0_CORE_SMIF_GPIO_VDD_INTR_SET for the details of bit fields.

22.1.1 SMIF0_CACHE_BLOCK_HWPARAMS

Description: Hardware Parameter register

Address: 0x44450000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	
HW Access	Reserved				R	R	R	
Name	Reserved [7:4]				SNAP-SHOTTING	XOM	ENDIANNESS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	CACHE_MEM_SIZE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	MASTER_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	Reserved		R	R	R	R
HW Access	R	R	Reserved		R	R	R	R
Name	AHB_VIO-LA-TION_RES P	APB_VIO-LA-TION_RES P	Reserved [29:28]		POW-ER_ON_EN ABLE	DIS_P-WR_DOWN _MAINT	DIS_-CACHE_DI S_MAINT	DIS_-CACHE_EN _MAINT

Bits	Name	Description
31	AHB_VIOLATION_RESP	Respond with error (1) or RAZ/WI (0) for illegal AHB operations (eg. XOM). Fixed to 0 if XOM render parameter is OFF Default Value: 0
30	APB_VIOLATION_RESP	Respond with error (1) or RAZ/WI (0) for illegal APB operations. These are transfers that are any of: non-privileged, instruction, unaligned or incomplete write strobes Default Value: 1
27	POWER_ON_ENABLE	Value of the input configuration port that controls whether the cache should be enabled automatically after power up Default Value: 0
26	DIS_PWR_DOWN_-MAINT	Value of the input configuration port that controls the function to disable automatic clean at power down Default Value: 0
25	DIS_CACHE_DIS_MAINT	Value of the input configuration port that controls the function to disable automatic maintenance at disabling the cache Default Value: 0
24	DIS_CACHE_EN_MAINT	Value of the input configuration port that controls the function to disable automatic maintenance at enabling the cache Default Value: 1
23 : 16	MASTER_ID	The cache generates transactions with this ID Default Value: 30

22.1.1 SMIF0_CACHE_BLOCK_HWPARAMS (continued)

15 : 8	CACHE_MEM_SIZE	Cache memory size in address bits. The actual size is this value to the power of 2 (11->2KB,..,16->64KB) Default Value: 15
3	SNAPSHOTTING	SNAPSHOTTING supported 1-ON, 0-OFF Default Value: 1
2	XOM	XOM supported 1-ON, 0-OFF Default Value: 0
1 : 0	ENDIANNESS	The endianness of the module 0 - LE, 1 - BE8, 2 - BE32 Default Value: 0

22.1.2 SMIF0_CACHE_BLOCK_CTRL

Description: Control Register

Address: 0x44450010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved							
Name	Reserved [7:2]						FORCE_WT	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							
Name	Reserved [15:9]							DENY_POWERDOWN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	RW
HW Access	Reserved							
Name	Reserved [23:19]					ALLOW_NSEC_NSECSTAT	ALLOW_NSEC_MAINT_LINES	ALLOW_NSEC_ENABLE_READ

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	ALLOW_NSEC_NSECSTAT	Allow non-secure to read and control non-secure statistics counter registers and receive saturation interrupt Default Value: 0
17	ALLOW_NSEC_MAINT_LINES	Allow non-secure to trigger maintenance (only for lines and only non-secure views of cache lines) Default Value: 0
16	ALLOW_NSEC_ENABLE_READ	Allow non-secure to see if the cache is enabled Default Value: 0
8	DENY_POWERDOWN	When set, power-down LPI requests are denied. Does not affect clock LPI requests. Default Value: 0
1	FORCE_WT	Force Write-Through policy Default Value: 0
0	ENABLE	Enable cache (1-enabled, 0-disabled) Default Value: 0

22.1.3 SMIF0_CACHE_BLOCK_NSEC_ACCESS

Description: Non-secure access information

Address: 0x44450014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							
Name	Reserved [7:1]							CACHE_ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					R	R	R
HW Access	Reserved							
Name	Reserved [23:19]					NSEC_NSECSTAT_ALLOWED	NSEC_MAINT_LINES_ALLOWED	NSEC_ENABLE_READ_ALLOWED

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	NSEC_NSECSTAT_ALLOWED	Non-secure is allowed to read and control non-secure statistics counters and receives saturation interrupt Default Value: 0
17	NSEC_MAINT_LINES_ALLOWED	Non-secure is allowed to trigger maintenance (only for lines) Default Value: 0
16	NSEC_ENABLE_READ_ALLOWED	Non-secure is allowed to see the cache enabled state Default Value: 0
0	CACHE_ENABLED	Enable cache (1-enabled, 0-disabled). Only valid if bit NSEC_ENABLE_READ_ALLOWED is set Default Value: 0

22.1.4 SMIF0_CACHE_BLOCK_MAINT_CTRL_ALL

Description: Maintenance control for the entire cache

Address: 0x44450020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						W	W
HW Access	Reserved							
Name	Reserved [7:2]						TRIG_IN-VALI-DATE_ALL	TRIG_-CLEAN_ALL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	TRIG_INVALIDATE_ALL	Trigger Invalidate on all cache (can be used together with cleaning) Default Value: 0
0	TRIG_CLEAN_ALL	Trigger Cleaning on all cache (can be used together with invalidate) Default Value: 0

22.1.5 SMIF0_CACHE_BLOCK_MAINT_CTRL_LINES

Description: Maintenance control for individual lines

Address: 0x44450024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W			Reserved		W	W	W
HW Access				Reserved				
Name	ADDR [7:5]			Reserved [4:3]		SECURITY	TRIG_IN-VALIDATE	TRIG_-CLEAN

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access								
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access								
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access								
Name	ADDR [31:24]							

Bits	Name	Description
31 : 5	ADDR	Address to look up in the cache and perform invalidate or cleaning on matching cache line. Use bits [31:5] of the address. Default Value: 0
2	SECURITY	Cache maintenance is performed on the secure or non-secure view of the address. (It is possible to have both the secure and non-secure views of the same address allocated in the cache.) 0 - Secure, 1 - Non-secure; For non-secure accesses, this is ignored, and the non-secure is selected always Default Value: 0
1	TRIG_INVALIDATE	Trigger Invalidate on addressed cache line Default Value: 0
0	TRIG_CLEAN	Trigger Cleaning on addressed cache line Default Value: 0

22.1.6 SMIF0_CACHE_BLOCK_MAINT_STATUS

Description: Maintenance status for the cache

Address: 0x44450028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	R
HW Access	Reserved							
Name	Reserved [7:4]				ONGO-ING_P-WR_MAINT	ONGO-ING_MAINT	ONGO-IN-G_EN_DIS	CACHE_EN ABLED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							
Name	Reserved [15:9]							CACHE_IS _CLEAN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	CACHE_IS_CLEAN	Reading 1 means the cache doesnt have dirty data. Default Value: 0
3	ONGOING_PWR_MAINT	Reading 1 means a full cache cleaning operation is in progress triggered by a power down request. Default Value: 0
2	ONGOING_MAINT	Reading 1 means a cache maintenance operation is in progress (clean and/or invalidate or enable/disable). Default Value: 0
1	ONGOING_EN_DIS	Ongoing Enable or Disable. Reading 1 means the cache is in progress of being disabled or enabled and the CACHE_ENABLED bit will change when done. Default Value: 0
0	CACHE_ENABLED	Cache enable status. Reading 1 means the cache is enabled, 0 the cache is disabled Default Value: 0

22.1.7 SMIF0_CACHE_BLOCK_SECIRQSTAT

Description: Secure Interrupt Request Status register

Address: 0x44450100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	R	R	R	R
HW Access	Reserved							
Name	Reserved	NSE-CURE_CNT_SAT	SE-CURE_CNT_SAT	TR_ERR	MAINT_IGNORED	MAINT_-DONE	DISABLE_-DONE	ENABLE_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6	NSECURE_CNT_SAT	Non-secure statistics counters saturated and stopped (when ALLOW_NSEC_NSECSTAT is not set) Default Value: 0
5	SECURE_CNT_SAT	Secure statistics counters saturated and stopped Default Value: 0
4	TR_ERR	Secure transaction error on master side (any bus error, data type access to XOM) Default Value: 0
3	MAINT_IGNORED	Secure software attempted maintenance or enable/disable of cache while such an operation was already in progress and the new request was ignored. Default Value: 0
2	MAINT_DONE	Manual maintenance operation (clean and/or invalidate) started by secure software finished Default Value: 0
1	DISABLE_DONE	Disable operation completed, cache is bypassed Default Value: 0
0	ENABLE_DONE	Enable operation completed, cache is operational Default Value: 0

22.1.8 SMIF0_CACHE_BLOCK_SECIRQSCLR

Description: Secure Interrupt Status Clear register

Address: 0x44450104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	W	W	W	W	W	W	W
HW Access	Reserved							
Name	Reserved	NSE-CURE_CNT_SAT	SE-CURE_CNT_SAT	TR_ERR	MAINT_IGNORED	MAINT_-DONE	DISABLE_-DONE	ENABLE_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6	NSECURE_CNT_SAT	Clear NSECURE_CNT_SAT interrupt Default Value: 0
5	SECURE_CNT_SAT	Clear SECURE_CNT_SAT interrupt Default Value: 0
4	TR_ERR	Clear secure TR_ERR Interrupt Default Value: 0
3	MAINT_IGNORED	Clear secure MAINT_IGNORED interrupt Default Value: 0
2	MAINT_DONE	Clear secure MAINT_DONE interrupt Default Value: 0
1	DISABLE_DONE	Clear secure DISABLE_DONE interrupt Default Value: 0
0	ENABLE_DONE	Clear ENABLE_DONE interrupt Default Value: 0

22.1.9 SMIF0_CACHE_BLOCK_SECIRQEN

Description: Secure Interrupt Enable register

Address: 0x44450108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	NSE-CURE_CNT_SAT	SE-CURE_CNT_SAT	TR_ERR	MAINT_IGNORED	MAINT_-DONE	DISABLE_-DONE	ENABLE_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6	NSECURE_CNT_SAT	Enable NSECURE_CNT_SAT interrupt Default Value: 0
5	SECURE_CNT_SAT	Enable SECURE_CNT_SAT interrupt Default Value: 0
4	TR_ERR	Enable secure TR_ERR Interrupt Default Value: 0
3	MAINT_IGNORED	Enable secure MAINT_IGNORED interrupt Default Value: 0
2	MAINT_DONE	Enable secure MAINT_DONE interrupt Default Value: 0
1	DISABLE_DONE	Enable secure DISABLE_DONE interrupt Default Value: 0
0	ENABLE_DONE	Enable ENABLE_DONE interrupt Default Value: 0

22.1.10 SMIF0_CACHE_BLOCK_SECIRQINFO1

Description: Secure transfer error information 1

Address: 0x4445010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address used by the secure transfer that caused the SECURE_TR_ERR Default Value: 0

22.1.11 SMIF0_CACHE_BLOCK_SECIRQINFO2

Description: Secure transfer error information 2

Address: 0x44450110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	MASTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						R	
HW Access	Reserved							
Name	Reserved [15:10]						ERROR_SRC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 8	ERROR_SRC	Origin of the secure transfer that received the bus error Default Value: 0
7 : 0	MASTER	HMASTER ID of the secure transfer that caused the error Default Value: 0

22.1.12 SMIF0_CACHE_BLOCK_NSECIRQSTAT

Description: Non-secure Interrupt Request Status register

Address: 0x44450140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	Reserved	R	R	R	Reserved	
HW Access	Reserved		Reserved				Reserved	
Name	Reserved	NSE-CURE_CNT_SAT	Reserved	TR_ERR	MAINT_IGNORED	MAINT_-DONE	Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6	NSECURE_CNT_SAT	Non-secure statistics counters saturated and stopped (when ALLOW_NSEC_NSECSTAT is not set) Default Value: 0
4	TR_ERR	Non-secure transaction error on master side.The details of the transaction are saved in the NSE-CIRQINFOx registers. Default Value: 0
3	MAINT_IGNORED	Non-secure software attempted maintenance or enable/disable of cache while such an operation was already in progress and the new request was ignored. Default Value: 0
2	MAINT_DONE	Manual maintenance operation (clean and/or invalidate) started by non-secure software finished Default Value: 0

22.1.13 SMIF0_CACHE_BLOCK_NSECIRQSCLR

Description: Non-secure Interrupt Status Clear register

Address: 0x44450144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	W	Reserved	W	W	W	Reserved	
HW Access	Reserved		Reserved				Reserved	
Name	Reserved	NSE-CURE_CNT_SAT	Reserved	TR_ERR	MAINT_IGNORED	MAINT_-DONE	Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6	NSECURE_CNT_SAT	Clear NSECURE_CNT_SAT interrupt Default Value: 0
4	TR_ERR	Clear non-secure TR_ERR Interrupt Default Value: 0
3	MAINT_IGNORED	Clear non-secure MAINT_IGNORED interrupt Default Value: 0
2	MAINT_DONE	Clear non-secure MAINT_DONE interrupt Default Value: 0

22.1.14 SMIF0_CACHE_BLOCK_NSECIRQEN

Description: Non-secure Interrupt Enable register

Address: 0x44450148

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	Reserved	RW	RW	RW	Reserved	
HW Access	Reserved		Reserved				Reserved	
Name	Reserved	NSE-CURE_CNT_SAT	Reserved	TR_ERR	MAINT_IGNORED	MAINT_-DONE	Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
6	NSECURE_CNT_SAT	Enable NSECURE_CNT_SAT interrupt Default Value: 0
4	TR_ERR	Enable non-secure TR_ERR Interrupt Default Value: 0
3	MAINT_IGNORED	Enable non-secure MAINT_IGNORED interrupt Default Value: 0
2	MAINT_DONE	Enable non-secure MAINT_DONE interrupt Default Value: 0

22.1.15 SMIF0_CACHE_BLOCK_NSECIRQINFO1

Description: Non-secure transfer error information 1

Address: 0x4445014C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address used by the non-secure transfer that caused NSECURE_TR_ERR Default Value: 0

22.1.16 SMIF0_CACHE_BLOCK_NSECIRQINFO2

Description: Non-secure transfer error information 2

Address: 0x44450150

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	MASTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						R	
HW Access	Reserved							
Name	Reserved [15:10]						ERROR_SRC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 8	ERROR_SRC	Origin of the non-secure transfer that received the bus error Default Value: 0
7 : 0	MASTER	HMASTER ID of the non-secure transfer that caused the error Default Value: 0

22.1.17 SMIF0_CACHE_BLOCK_SECHIT

Description: Secure transfers Hit register

Address: 0x44450300

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	SECHITCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	SECHITCNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	SECHITCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	SECHITCNT [31:24]							

Bits	Name	Description
31 : 0	SECHITCNT	Number of secure transfers that hit the cache Default Value: 0

22.1.18 SMIF0_CACHE_BLOCK_SECMISS

Description: Secure transfers Miss register

Address: 0x44450304

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	SECMISSCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	SECMISSCNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	SECMISSCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	SECMISSCNT [31:24]							

Bits	Name	Description
31 : 0	SECMISSCNT	Number of secure transfers that missed the cache Default Value: 0

22.1.19 SMIF0_CACHE_BLOCK_SECSTATCTRL

Description: Secure transfers statistic counters control

Address: 0x44450308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved							
Name	Reserved [7:2]						RESET	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	RESET	Reset statistics counters for secure transactions Default Value: 0
0	ENABLE	Enable statistics counters for secure transactions Default Value: 0

22.1.20 SMIF0_CACHE_BLOCK_NSECHIT

Description: Non-secure transfers Hit register

Address: 0x44450310

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	NSECHITCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	NSECHITCNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	NSECHITCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	NSECHITCNT [31:24]							

Bits	Name	Description
31 : 0	NSECHITCNT	Number of non-secure transfers that hit the cache Default Value: 0

22.1.21 SMIF0_CACHE_BLOCK_NSECMISS

Description: Non-secure transfers Miss register

Address: 0x44450314

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	NSECMISSCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	NSECMISSCNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	NSECMISSCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	NSECMISSCNT [31:24]							

Bits	Name	Description
31 : 0	NSECMISSCNT	Number of non-secure transfers that missed the cache Default Value: 0

22.1.22 SMIF0_CACHE_BLOCK_NSECSTATCTRL

Description: Non-secure transfers statistic counters control

Address: 0x44450318

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved							
Name	Reserved [7:2]						RESET	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	RESET	Reset statistics counters for non-secure transactions Default Value: 0
0	ENABLE	Enable statistics counters for non-secure transactions Default Value: 0

22.1.23 SMIF0_CACHE_BLOCK_PMSVR0

Description: Saved Value Register 0 - Secure Hit

Address: 0x44450600

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	SHCS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	SHCS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	SHCS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	SHCS [31:24]							

Bits	Name	Description
31 : 0	SHCS	Secure hit counter snapshot Default Value: 0

22.1.24 SMIF0_CACHE_BLOCK_PMSVR1

Description: Saved Value Register 1 - Secure Miss

Address: 0x44450604

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	SMCS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	SMCS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	SMCS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	SMCS [31:24]							

Bits	Name	Description
31 : 0	SMCS	Secure miss counter snapshot Default Value: 0

22.1.25 SMIF0_CACHE_BLOCK_PMSVR2

Description: Saved Value Register 2 - Non-secure Hit

Address: 0x44450608

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	NSHCS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	NSHCS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	NSHCS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	NSHCS [31:24]							

Bits	Name	Description
31 : 0	NSHCS	Non-secure hit counter snapshot Default Value: 0

22.1.26 SMIF0_CACHE_BLOCK_PMSVR3

Description: Saved Value Register 3 - Non-secure Miss

Address: 0x4445060C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	NSMCS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	NSMCS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	NSMCS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	NSMCS [31:24]							

Bits	Name	Description
31 : 0	NSMCS	Non-secure miss counter snapshot Default Value: 0

22.1.27 SMIF0_CACHE_BLOCK_PMSSSR

Description: PMU Snapshot Status Register

Address: 0x44450680

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							
Name	Reserved [7:1]							NC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	NC	No capture. Indicates whether the PMU counters have been captured Default Value: 1

22.1.28 SMIF0_CACHE_BLOCK_PMSSCR

Description: PMU Snapshot Capture Register

Address: 0x444506F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							W
HW Access	Reserved							
Name	Reserved [7:1]							SS

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	SS	Provides a mechanism for software to initiate a sample. Writing 1 initiates a capture immediately. Writing 0 is ignored. Default Value: 0

22.1.29 SMIF0_CACHE_BLOCK_PMSSRR

Description: PMU Snapshot Reset Register

Address: 0x444506F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved [7:4]				RP_NSMC	RP_NSHC	RP_SMC	RP_SHC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	RP_NSMC	Reset non-secure miss counter when making snapshot. Mirrors RP_NSHC as the 2 counters are grouped and should not be reset separately Default Value: 0
2	RP_NSHC	Reset non-secure hit counter when making snapshot. Miss counter copies this value Default Value: 0
1	RP_SMC	Reset secure miss counter when making snapshot. Mirrors RP_SHC as the 2 counters are grouped and should not be reset separately Default Value: 0
0	RP_SHC	Reset secure hit counter when making snapshot. Miss counter copies this value Default Value: 0

22.1.30 SMIF0_CACHE_BLOCK_PIDR4

Description: Peripheral ID 4

Address: 0x44450FD0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access								
Name	SIZE [7:4]				DES_2 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	SIZE	4KB Count. Default Value: 0
3 : 0	DES_2	JEP106 Continuation Code. Default Value: 4

22.1.31 SMIF0_CACHE_BLOCK_PIDR5

Description: Peripheral ID 5

Address: 0x44450FD4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	RSVD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	RSVD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	RSVD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	RSVD [31:24]							

Bits	Name	Description
31 : 0	RSVD	Reserved Default Value: 0

22.1.32 SMIF0_CACHE_BLOCK_PIDR6

Description: Peripheral ID 6

Address: 0x44450FD8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	RSVD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	RSVD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	RSVD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	RSVD [31:24]							

Bits	Name	Description
31 : 0	RSVD	Reserved Default Value: 0

22.1.33 SMIF0_CACHE_BLOCK_PIDR7

Description: Peripheral ID 7

Address: 0x44450FDC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	RSVD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	RSVD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	RSVD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	RSVD [31:24]							

Bits	Name	Description
31 : 0	RSVD	Reserved Default Value: 0

22.1.34 SMIF0_CACHE_BLOCK_PIDR0

Description: Peripheral ID 0

Address: 0x44450FE0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	PART_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	RES0_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	RES0_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	RES0_0 [31:24]							

Bits	Name	Description
31 : 8	RES0_0	Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior. Default Value: 0
7 : 0	PART_0	Part Number [7:0]. Default Value: 0x31

22.1.35 SMIF0_CACHE_BLOCK_PIDR1

Description: Peripheral ID 1

Address: 0x44450FE4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access								
Name	DES_0 [7:4]				PART_1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	DES_0	JEP106 Identity Code [3:0]. Default Value: 0xB
3 : 0	PART_1	Part Number [11:8]. Default Value: 0x8

22.1.36 SMIF0_CACHE_BLOCK_PIDR2

Description: Peripheral ID 2

Address: 0x44450FE8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R	R		
HW Access								
Name	REVISION [7:4]				JEDEC	DES_1 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	RES0_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	RES0_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	RES0_0 [31:24]							

Bits	Name	Description
31 : 8	RES0_0	Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior. Default Value: 0
7 : 4	REVISION	Revision Code. Default Value: 0
3	JEDEC	JEDEC. Default Value: 1
2 : 0	DES_1	JEP106 Identity Code [6:4]. Default Value: 3

22.1.37 SMIF0_CACHE_BLOCK_PIDR3

Description: Peripheral ID 3

Address: 0x44450FEC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access								
Name	REVAND [7:4]				CMOD [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	REVAND	Manufacturer revision number. Default Value: 0
3 : 0	CMOD	Customer Modified. Default Value: 0

22.1.38 SMIF0_CACHE_BLOCK_CIDR0

Description: Component ID 0

Address: 0x44450FF0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	PRMBL_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PRMBL_0	Preamble. Default Value: 0xD

22.1.39 SMIF0_CACHE_BLOCK_CIDR1

Description: Component ID 1

Address: 0x44450FF4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access								
Name	CLASS [7:4]				PRMBL_1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	CLASS	Component class. Default Value: 0xF
3 : 0	PRMBL_1	Preamble. Default Value: 0

22.1.40 SMIF0_CACHE_BLOCK_CIDR2

Description: Component ID 2

Address: 0x44450FF8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	PRMBL_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	RES0_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	RES0_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	RES0_0 [31:24]							

Bits	Name	Description
31 : 8	RES0_0	Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior. Default Value: 0
7 : 0	PRMBL_2	Preamble. Default Value: 5

22.1.41 SMIF0_CACHE_BLOCK_CIDR3

Description: Component ID 3

Address: 0x44450FFC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	PRMBL_3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	PRMBL_3	Preamble. Default Value: 0xB1

22.1.42 SMIF0_CACHE_BLOCK_MMIO_BYPASS_WI

Description: Bypass wrap to increment conversion logic

Address: 0x44452000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							BYPASS_-WI

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	BYPASS_WI	0 = Do Not Bypass wrap to increment conversion logic 1 = Bypass wrap to increment conversion logic Default Value: 0

22.1.43 SMIF0_CACHE_BLOCK_MMIO_MASTER_ID

Description: The cache generates transactions (linefill and eviction Write-Back) that are marked with the value specified by MASTER_ID on hmaster_m.

Address: 0x44452004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MASTER_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	MASTER_ID	The cache generates transactions (linefill and eviction Write-Back) that are marked with the given value on hmaster_m. Default Value: 30

22.1.44 SMIF0_CACHE_BLOCK_MMIO_DIS_CACHE_EN_MAINT

Description: This signal turns on/off cache enable maintenance.

Address: 0x44452008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							DIS_-CACHE_EN_MAINT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	DIS_CACHE_EN_MAINT	The dis_cache_en_maint port determines if the AHB Cache starts the predefined cache maintenance before the cache enable command would take effect. dis_cache_en_maint = 1 The AHB Cache does not start any maintenance before applying the cache enable command. Caution If cache enable maintenance is disabled, the software must manage the AHB Cache. It must invalidate the content before cache enable if: - The cache RAMs have not been invalidated after the last power cycle. - The content is not valid anymore. Otherwise the data in the cacheable regions is corrupted. dis_cache_en_maint = 0, The AHB Cache starts invalidate all maintenance before it applies the cache enable command that it has received on the APB interface. While the cache enable maintenance is running, the AHB Cache works as if it were disabled. The traffic is not affected. When the invalidation is completed, the next NSEQ transaction on the AHB slave interface is looked up in the cache according to its transaction attributes. The status of ongoing enable or disable related maintenance can be read at MAINT_STATUS.ONGOING_EN_DIS status register bit. The effective enabled or disabled status can be read at MAINT_STATUS.CACHE_ENABLED status register bit. Default Value: 1

22.1.45 SMIF0_CACHE_BLOCK_MMIO_DIS_CACHE_DIS_MAINT

Description: This signal turns on/off cache disable maintenance.

Address: 0x4445200C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							DIS_-CACHE_DIS_MAINT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	DIS_CACHE_DIS_MAINT	The dis_cache_dis_maint determines if the AHB Cache starts the predefined cache maintenance before the cache disable command would take effect. dis_cache_dis_maint = 1 The AHB Cache drains the internal buffers but does not complete any other maintenance before applying the cache disable command. It only waits for any ongoing Burst on the AHB slave interface to finish. Caution If cache disable maintenance is disabled, the software must manage the AHB Cache. If there is any dirty data in the cache RAMs, the software must clean the cache before disable. Otherwise, the main memory is not updated. dis_cache_dis_maint = 0, The AHB Cache starts clean all maintenance before it applies the cache disable command that it has received on the APB interface. While this maintenance is running, the AHB Cache stalls the AHB slave interface. After accepting the disable command, the AHB Cache stalls the AHB traffic at the next NSEQ transaction on the AHB slave interface. Then it runs a clean all maintenance process and when it is completed the disable becomes effective and the AHB slave interface is released. The status of ongoing disable related maintenance can be read at MAINT_STATUS.ONGOING_EN_DIS status register bit. The effective enabled or disabled status can be read at MAINT_STATUS.CACHE_ENABLED status register bit. Default Value: 0

22.1.46 SMIF0_CACHE_BLOCK_MMIO_APB_VIOLATION_RESP

Description: This signal controls if the APB interface of cache responds with an error to illegal operations on the APB interface. Illegal operations on the APB interface include Writing with no full write strobe, Accessing non-word aligned addresses, Instruction accesses, Non-privileged accesses 1 - The Cache responds with an APB error. Read data is masked with zeros and write data is ignored. 0 - The Cache sends an OK response. Read data is masked with zeros and write data is ignored.

Address: 0x44452010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							APB_VIOLATION_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	APB_VIOLATION_RESP	This bit controls if the APB interface of cache responds with an error to illegal operations on the APB interface. Illegal operations on the APB interface include Writing with no full write strobe, Accessing non-word aligned addresses, Instruction accesses, Non-privileged accesses 1 - The AHB Cache responds with an APB error. Read data is masked with zeros and write data is ignored. 0 - The AHB Cache sends an OK response. Read data is masked with zeros and write data is ignored. Default Value: 1

22.1.47 SMIF0_CACHE_BLOCK_MMIO_MMIO_ACTIVE_EN

Description: SW control to put SMIF.6 in active or clock gated mode

Address: 0x44452014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							MMIO_ACTIVE_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	MMIO_ACTIVE_EN	SW control to put SMIF.6 in active or clock gated mode 0 - Software writes this value to put SMIF.6 in clock gated mode w/ clocks gated 1 - Software writes this value to put SMIF.6 in active mode w/ clocks from MXSPERI restored Default Value: 1

22.1.48 SMIF0_CACHE_BLOCK_MMIO_POWER_ON_ENABLE

Description: This signal configures the cache to enable the cache automatically after powerup.

Address: 0x44452018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							POWER_ON_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	POWER_ON_ENABLE	The power_on_enable port can be set so that the AHB Cache is enabled when the LPI interfaces first reach QRUN state after reset. The cache enable bit is combinatorially driven from this bit. With a default of 0, cache comes up disabled upon cold start. Before enabling the cache, the SW should set this bit to 1 (if it intends to have the cache come-up enabled after power-down/power-up sequence). The expected behaviour here is that this bit is retained during cache power down and when cache is subsequently powered down and back up, this bit would drive the cache enable bit to 1, thereby automatically enabling the cache. If the SW wants to use the cache contents upon return from deep sleep, it should make sure to have set dis_cache_en_maint set to 1 prior to going into deep sleep. Setting dis_cache_en_maint to 1 has an effect of preventing a cache from doing a force invalidate of cache lines prior to enable. power_on_enable = 1 The cache is enabled automatically after powerup. This signal is affected by the dis_cache_en_maint. power_on_enable = 0 The cache waits for software to enable the cache through the APB programming interface. Default Value: 0

22.1.49 SMIF0_CACHE_BLOCK_MMIO_MMIO_CACHE_RET_EN

Description: Controls if cache SRAMs are retained during DPSLP

Address: 0x4445201C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							MMIO_-CACHE_RET_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	MMIO_CACHE_RET_EN	mmio_cache_ret_en = 1 The cache SRAM array retains contents even when cache controller is powered down. mmio_cache_ret_en = 0 The cache SRAM array does not retain its contents even when cache controller is powered down. NOTE This bit controls the retention only in DPSLP mode. In DPSLP_RAM and DPSLP_OFF modes cache is never retained regarless of the setting of this bit. Default Value: 1

22.1.50 SMIF0_CACHE_BLOCK_MMIO_DIS_PWR_DOWN_MAINT

Description: This signal turns on/off powerdown maintenance.

Address: 0x44452020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							DIS_PWR_DOWN_MAINT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	DIS_PWR_DOWN_MAINT	The dis_pwr_down_maint port determines if the AHB Cache starts the predefined cache maintenance process before accepting a powerdown request. dis_pwr_down_maint = 1 If there is no deny condition, the AHB Cache merges any data from its internal buffers into the cache RAMs and accepts the power quiescence request immediately. dis_pwr_down_maint = 0 The AHB Cache checks the cache clean status whenever a power quiescence request is received through the power Q-Channel interface. If the cache status is clean and otherwise idle, then it accepts the quiescence request. If the cache status is dirty but otherwise idle, it starts a clean all maintenance process. The AHB Cache delays the response and only denies the request if a dirty line is actually found in the cache memory during the maintenance operation. During powerdown maintenance, any AHB activity that would cause a power quiescence request to be denied (except for the maintenance driven activity) results in the maintenance being aborted. Any subsequent quiescence request is denied while the maintenance is in progress. The status of the powerdown maintenance can be monitored - On the pwr_maintenance output port. This port is driven high only while this process is running. - By reading the MAINT_STATUS.ONGOING_PWR_MAINT status register bit. Default Value: 0

22.1.51 SMIF0_CACHE_BLOCK_MMIO_REGION0_BASE

Description: Region 0 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle

Address: 0x44452024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	ADDR [15:12]				Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					ADDR [26:24]		

Bits	Name	Description
26 : 12	ADDR	Determines the base address of a region 0 within a SMIF external memory address space The region 0 is hit when REGION0_LIMIT.ENABLE bit is set to 1 and transfer address is inside the range defined by REGION0_BASE.ADDR and REGION0_LIMIT.ADDR: REGION0_BASE.ADDR <= address[26:12] <= REGION0_LIMIT.ADDR Regions are not allowed to overlap; it is SW responsibility to set BASE and LIMIT address values for enabled regions in a way that there is no overlap. HW is not having any protection and will not generate any notification/interrupt in case of wrong configuration. Default Value: 0

22.1.52 SMIF0_CACHE_BLOCK_MMIO_REGION0_LIMIT

Description: Region 0 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle

Address: 0x44452028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					RW
HW Access	Reserved		R					R
Name	Reserved [7:6]		ATTR [5:1]					ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	ADDR [15:12]				Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					ADDR [26:24]		

Bits	Name	Description
26 : 12	ADDR	Determines the end address of a region 0 within a SMIF external memory address space Regions are not allowed to overlap; it is SW responsibility to set BASE and LIMIT address values for enabled regions in a way that there is no overlap. HW is not having any protection and will not generate any notification/interrupt in case of wrong configuration Default Value: 0
5 : 1	ATTR	This field defines transaction attributes for the region 0 and indicates how the transaction should be handled within a Cache Block: [5] R: Read Allocate [4] W: Write Allocate [3] L: Lookup [2] M: Modifiable [1] B: Bufferable The following ATTR values are supported: 5'b00000 - Non-Cacheable, Non-Bufferable (reset value) - nCnB 5'b00001 - Non-Cacheable, Bufferable - nCB 5'b01110 - Cacheable, Write Through, Write Allocate - WTWA 5'b10110 - Cacheable, Write Through, Read Allocate - WTRA 5'b11110 - Cacheable, Write Through, Read & Write Allocate - WTRWA 5'b01111 - Cacheable, Write Back , Write Allocate - WBWA 5'b10111 - Cacheable, Write Back , Read Allocate - WBRA 5'b11111 - Cacheable, Write Back , Read & Write Allocate - WBRWA If region is enabled and transaction address is hitting the predefined region address range, corresponding ATTR field is used to overwrite transaction HPROT bits Default Value: 0

22.1.52 SMIF0_CACHE_BLOCK_MMIO_REGION0_LIMIT (continued)

0	ENABLE	Region 0 Enable By default, all regions are disabled (all transfers are interpreted as non-cacheable) Default Value: 0

22.1.53 SMIF0_CACHE_BLOCK_MMIO_REGION1_BASE

Description: Region 1 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle

Address: 0x4445202C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	ADDR [15:12]				Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					ADDR [26:24]		

Bits	Name	Description
26 : 12	ADDR	Determines the base address of a region 1 within a SMIF external memory address space The region 1 is hit when REGION1_LIMIT.ENABLE bit is set to 1 and transfer address is inside the range defined by REGION1_BASE.ADDR and REGION1_LIMIT.ADDR: REGION1_BASE.ADDR <= address[26:12] <= REGION1_LIMIT.ADDR Regions are not allowed to overlap; it is SW responsibility to set BASE and LIMIT address values for enabled regions in a way that there is no overlap. HW is not having any protection and will not generate any notification/interrupt in case of wrong configuration Default Value: 0

22.1.54 SMIF0_CACHE_BLOCK_MMIO_REGION1_LIMIT

Description: Region 1 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle

Address: 0x44452030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					RW
HW Access	Reserved		R					R
Name	Reserved [7:6]		ATTR [5:1]					ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	ADDR [15:12]				Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					ADDR [26:24]		

Bits	Name	Description
26 : 12	ADDR	Determines the end address of a region 1 within a SMIF external memory address space Regions are not allowed to overlap; it is SW responsibility to set BASE and LIMIT address values for enabled regions in a way that there is no overlap. HW is not having any protection and will not generate any notification/interrupt in case of wrong configuration Default Value: 0
5 : 1	ATTR	This field defines transaction attributes for the region 1 and indicates how the transaction should be handled within a Cache Block: [5] R: Read Allocate [4] W: Write Allocate [3] L: Lookup [2] M: Modifiable [1] B: Bufferable The following ATTR values are supported: 5'b00000 - Non-Cacheable, Non-Bufferable (reset value) - nCnB 5'b00001 - Non-Cacheable, Bufferable - nCB 5'b01110 - Cacheable, Write Through, Write Allocate - WTWA 5'b10110 - Cacheable, Write Through, Read Allocate - WTRA 5'b11110 - Cacheable, Write Through, Read & Write Allocate - WTRWA 5'b01111 - Cacheable, Write Back , Write Allocate - WBWA 5'b10111 - Cacheable, Write Back , Read Allocate - WBRA 5'b11111 - Cacheable, Write Back , Read & Write Allocate - WBRWA If region is enabled and transaction address is hitting the predefined region address range, corresponding ATTR field is used to overwrite transaction HPROT bits Default Value: 0

22.1.54 SMIF0_CACHE_BLOCK_MMIO_REGION1_LIMIT (continued)

0	ENABLE	Region 1 Enable By default, all regions are disabled (all transfers are interpreted as non-cacheable) Default Value: 0

22.1.55 SMIF0_CACHE_BLOCK_MMIO_REGION2_BASE

Description: Region 2 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle

Address: 0x44452034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	ADDR [15:12]				Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					ADDR [26:24]		

Bits	Name	Description
26 : 12	ADDR	Determines the base address of a region 2 within a SMIF external memory address space The region 2 is hit when REGION2_LIMIT.ENABLE bit is set to 1 and transfer address is inside the range defined by REGION2_BASE.ADDR and REGION2_LIMIT.ADDR: REGION2_BASE.ADDR <= address[26:12] <= REGION2_LIMIT.ADDR Regions are not allowed to overlap; it is SW responsibility to set BASE and LIMIT address values for enabled regions in a way that there is no overlap. HW is not having any protection and will not generate any notification/interrupt in case of wrong configuration Default Value: 0

22.1.56 SMIF0_CACHE_BLOCK_MMIO_REGION2_LIMIT

Description: Region 2 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle

Address: 0x44452038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					RW
HW Access	Reserved		R					R
Name	Reserved [7:6]		ATTR [5:1]					ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	ADDR [15:12]				Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					ADDR [26:24]		

Bits	Name	Description
26 : 12	ADDR	Determines the end address of a region 2 within a SMIF external memory address space Regions are not allowed to overlap; it is SW responsibility to set BASE and LIMIT address values for enabled regions in a way that there is no overlap. HW is not having any protection and will not generate any notification/interrupt in case of wrong configuration Default Value: 0
5 : 1	ATTR	This field defines transaction attributes for the region 2 and indicates how the transaction should be handled within a Cache Block: [5] R: Read Allocate [4] W: Write Allocate [3] L: Lookup [2] M: Modifiable [1] B: Bufferable The following ATTR values are supported: 5'b00000 - Non-Cacheable, Non-Bufferable (reset value) - nCnB 5'b00001 - Non-Cacheable, Bufferable - nCB 5'b01110 - Cacheable, Write Through, Write Allocate - WTWA 5'b10110 - Cacheable, Write Through, Read Allocate - WTRA 5'b11110 - Cacheable, Write Through, Read & Write Allocate - WTRWA 5'b01111 - Cacheable, Write Back , Write Allocate - WBWA 5'b10111 - Cacheable, Write Back , Read Allocate - WBRA 5'b11111 - Cacheable, Write Back , Read & Write Allocate - WBRWA If region is enabled and transaction address is hitting the predefined region address range, corresponding ATTR field is used to overwrite transaction HPROT bits Default Value: 0

22.1.56 SMIF0_CACHE_BLOCK_MMIO_REGION2_LIMIT (continued)

0	ENABLE	Region 2 Enable By default, all regions are disabled (all transfers are interpreted as non-cacheable) Default Value: 0

22.1.57 SMIF0_CACHE_BLOCK_MMIO_REGION3_BASE

Description: Region 3 Attributes - register 0; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle

Address: 0x4445203C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	ADDR [15:12]				Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					ADDR [26:24]		

Bits	Name	Description
26 : 12	ADDR	Determines the base address of a region 3 within a SMIF external memory address space The region 3 is hit when REGION3_LIMIT.ENABLE bit is set to 1 and transfer address is inside the range defined by REGION3_BASE.ADDR and REGION3_LIMIT.ADDR: REGION3_BASE.ADDR <= address[26:12] <= REGION3_LIMIT.ADDR Regions are not allowed to overlap; it is SW responsibility to set BASE and LIMIT address values for enabled regions in a way that there is no overlap. HW is not having any protection and will not generate any notification/interrupt in case of wrong configuration Default Value: 0

22.1.58 SMIF0_CACHE_BLOCK_MMIO_REGION3_LIMIT

Description: Region 3 Attributes - register 1; Region attributes shall be changed exclusively while the SMIF is disabled, and the XIP interfaces are idle

Address: 0x44452040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					RW
HW Access	Reserved		R					R
Name	Reserved [7:6]		ATTR [5:1]					ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	ADDR [15:12]				Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					ADDR [26:24]		

Bits	Name	Description
26 : 12	ADDR	Determines the end address of a region 3 within a SMIF external memory address space Regions are not allowed to overlap; it is SW responsibility to set BASE and LIMIT address values for enabled regions in a way that there is no overlap. HW is not having any protection and will not generate any notification/interrupt in case of wrong configuration Default Value: 0
5 : 1	ATTR	This field defines transaction attributes for the region 3 and indicates how the transaction should be handled within a Cache Block: [5] R: Read Allocate [4] W: Write Allocate [3] L: Lookup [2] M: Modifiable [1] B: Bufferable The following ATTR values are supported: 5'b00000 - Non-Cacheable, Non-Bufferable (reset value) - nCnB 5'b00001 - Non-Cacheable, Bufferable - nCB 5'b01110 - Cacheable, Write Through, Write Allocate - WTWA 5'b10110 - Cacheable, Write Through, Read Allocate - WTRA 5'b11110 - Cacheable, Write Through, Read & Write Allocate - WTRWA 5'b01111 - Cacheable, Write Back , Write Allocate - WBWA 5'b10111 - Cacheable, Write Back , Read Allocate - WBRA 5'b11111 - Cacheable, Write Back , Read & Write Allocate - WBRWA If region is enabled and transaction address is hitting the predefined region address range, corresponding ATTR field is used to overwrite transaction HPROT bits Default Value: 0

22.1.58 SMIF0_CACHE_BLOCK_MMIO_REGION3_LIMIT (continued)

0	ENABLE	Region 3 Enable By default, all regions are disabled (all transfers are interpreted as non-cacheable) Default Value: 0

22.1.59 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CFG

Description: Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.

Address: 0x44454000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			
HW Access	Reserved			R	Reserved			
Name	Reserved [7:5]			RE-SPONSE	Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	RESPONSE	Response Configuration for Security and PC violations 0: Read-Zero Write Ignore (RAZ/WI) 1: Bus Error Default Value: 0

22.1.60 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_CTRL

Description: Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)

Address: 0x44454100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	Reserved						
HW Access	R	Reserved						
Name	LOCK	Reserved [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for this protection context. Software can set this bit but not clear it once set. When set, write operations to BLK_LUT are not possible from this protection context. Setting LOCK also blocks writes to CTRL itself (for that PC copy). All writes are ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for this protection context as a side effect of each read/write access to BLK_LUT Default Value: 1

22.1.61 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_MAX

Description: Max value of block-based index register

Address: 0x44454104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				VALUE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; See product datasheet for details on protection of external memories. Default Value: 15

22.1.62 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_CFG

Description: Block size & initialization in progress

Address: 0x44454108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	INIT_IN_PROGRESS	Reserved [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to BLK_LUT is blocked (BLK_IDX increment is also ignored). The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ... up to 15: 1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 12

22.1.63 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_IDX

Description: Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)

Address: 0x4445410C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				RW			
Name	Reserved [7:4]				VALUE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	VALUE	Index value for accessing block-based lookup table using BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

22.1.64 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_LUT

Description: NS status for 32 blocks at BLK_IDX with PC=_pc>

Address: 0x44454110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS7	ATTR_NS6	ATTR_NS5	ATTR_NS4	ATTR_NS3	ATTR_NS2	ATTR_NS1	ATTR_NS0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	AT-TR_NS15	AT-TR_NS14	AT-TR_NS13	AT-TR_NS12	ATTR_NS11	AT-TR_NS10	ATTR_NS9	ATTR_NS8

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	AT-TR_NS23	AT-TR_NS22	AT-TR_NS21	AT-TR_NS20	AT-TR_NS19	AT-TR_NS18	AT-TR_NS17	AT-TR_NS16

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	AT-TR_NS31	AT-TR_NS30	AT-TR_NS29	AT-TR_NS28	AT-TR_NS27	AT-TR_NS26	AT-TR_NS25	AT-TR_NS24

Bits	Name	Description
31	ATTR_NS31	NS bit for block 31 based on BLK_IDX Default Value: 0
30	ATTR_NS30	NS bit for block 30 based on BLK_IDX Default Value: 0
29	ATTR_NS29	NS bit for block 29 based on BLK_IDX Default Value: 0
28	ATTR_NS28	NS bit for block 28 based on BLK_IDX Default Value: 0
27	ATTR_NS27	NS bit for block 27 based on BLK_IDX Default Value: 0
26	ATTR_NS26	NS bit for block 26 based on BLK_IDX Default Value: 0
25	ATTR_NS25	NS bit for block 25 based on BLK_IDX Default Value: 0
24	ATTR_NS24	NS bit for block 24 based on BLK_IDX Default Value: 0
23	ATTR_NS23	NS bit for block 23 based on BLK_IDX Default Value: 0
22	ATTR_NS22	NS bit for block 22 based on BLK_IDX Default Value: 0

22.1.64 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_BLK_LUT (continued)

21	ATTR_NS21	NS bit for block 21 based on BLK_IDX Default Value: 0
20	ATTR_NS20	NS bit for block 20 based on BLK_IDX Default Value: 0
19	ATTR_NS19	NS bit for block 19 based on BLK_IDX Default Value: 0
18	ATTR_NS18	NS bit for block 18 based on BLK_IDX Default Value: 0
17	ATTR_NS17	NS bit for block 17 based on BLK_IDX Default Value: 0
16	ATTR_NS16	NS bit for block 16 based on BLK_IDX Default Value: 0
15	ATTR_NS15	NS bit for block 15 based on BLK_IDX Default Value: 0
14	ATTR_NS14	NS bit for block 14 based on BLK_IDX Default Value: 0
13	ATTR_NS13	NS bit for block 13 based on BLK_IDX Default Value: 0
12	ATTR_NS12	NS bit for block 12 based on BLK_IDX Default Value: 0
11	ATTR_NS11	NS bit for block 11 based on BLK_IDX Default Value: 0
10	ATTR_NS10	NS bit for block 10 based on BLK_IDX Default Value: 0
9	ATTR_NS9	NS bit for block 9 based on BLK_IDX Default Value: 0
8	ATTR_NS8	NS bit for block 8 based on BLK_IDX Default Value: 0
7	ATTR_NS7	NS bit for block 7 based on BLK_IDX Default Value: 0
6	ATTR_NS6	NS bit for block 6 based on BLK_IDX Default Value: 0
5	ATTR_NS5	NS bit for block 5 based on BLK_IDX Default Value: 0
4	ATTR_NS4	NS bit for block 4 based on BLK_IDX Default Value: 0
3	ATTR_NS3	NS bit for block 3 based on BLK_IDX Default Value: 0
2	ATTR_NS2	NS bit for block 2 based on BLK_IDX Default Value: 0
1	ATTR_NS1	NS bit for block 1 based on BLK_IDX Default Value: 0
0	ATTR_NS0	NS bit for block 0 based on BLK_IDX Default Value: 0

22.1.65 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_CTRL

Description: Control register with lock bit and auto-increment only

Address: 0x44454200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	Reserved						
HW Access	R	Reserved						
Name	LOCK	Reserved [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for the root-of-trust configuration registers. Software can set this bit but not clear it once set. When set, write operations to ROT_BLK_LUT are not possible. Write is ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for each read/write of ROT_BLK_LUT Default Value: 1

22.1.66 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_-MAX

Description: Max value of block-based index register for ROT

Address: 0x44454208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R					
HW Access	Reserved		R					
Name	Reserved [7:6]		VALUE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 63

22.1.67 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_CFG

Description: Same as BLK_CFG

Address: 0x4445420C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	INIT_IN_PROGRESS	Reserved [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to ROT_BLK_LUT is RAZWI. The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ...up to 15:1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 12

22.1.68 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_IDX

Description: Index of 8-block group accessed through ROT_BLK_LUT_*

Address: 0x44454210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		RW					
Name	Reserved [7:6]		VALUE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	VALUE	Index value for accessing block-based lookup table using ROT_BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

22.1.69 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_PC

Description: Protection context of 8-block group accesses through ROT_BLK_LUT

Address: 0x44454214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	PC	Specify PC values for ROT_BLK_IDX and ROT_BLK_LUT Default Value: 0

22.1.70 SMIF0_CACHE_BLOCK_CACHEBLK_AHB_MPC0_ROT_BLK_LUT

Description: (R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC

Address: 0x44454218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR1 [6:4]			Reserved	ATTR0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR3 [14:12]			Reserved	ATTR2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR5 [22:20]			Reserved	ATTR4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	RW			Reserved	RW		
Name	Reserved	ATTR7 [30:28]			Reserved	ATTR6 [26:24]		

Bits	Name	Description
30 : 28	ATTR7	W/R/NS bits for block 7 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
26 : 24	ATTR6	W/R/NS bits for block 6 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
22 : 20	ATTR5	W/R/NS bits for block 5 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
18 : 16	ATTR4	W/R/NS bits for block 4 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
14 : 12	ATTR3	W/R/NS bits for block 3 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
10 : 8	ATTR2	W/R/NS bits for block 2 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
6 : 4	ATTR1	W/R/NS bits for block 1 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
2 : 0	ATTR0	W/R/NS bits for block 0 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0

22.1.71 SMIF0_CORE_CTL

Description: Control

Address: 0x44460000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							XIP_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		Reserved	RW		
HW Access	R		R		Reserved	R		
Name	SELECT_HOLD_DELAY [23:22]		SELECT_SETUP_DELAY [21:20]		Reserved	DESELECT_DELAY [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved					RW	RW
HW Access	R	Reserved					R	R
Name	ENABLED	Reserved [30:26]					CLOCK_IF_SEL	BLOCK

Bits	Name	Description
31	ENABLED	SMIF core enable: '0': Disabled. All non-retention registers are reset to their default value when this SMIF core is disabled. When this SMIF core is disabled, the XIP accesses produce AHB-Lite bus errors and AXI error responses. '1': Enabled. Notes: - Before disabling or resetting this SMIF core, SW should ensure that this SMIF core is NOT busy (STATUS.BUSY is '0'), otherwise illegal interface transfers may occur. - After CTL.ENABLED is set to 1 it takes up to 20 clk_if cycles until the memory interface registers are realeased from reset. - The DLL is powered up when CTL.ENABLED is set to 1 (if CTL2.BYPASS_MODE is 0). In closed loop mode, it takes maximum 8us for the DLL to stabilize and lock to the freerunning PLL clock at which point STATUS.DLL_LOCKED and INTR.DLL_LOCK will be set. In open loop mode, the lock signal is asserted 261 clk_pll cycles after the DLL is enabled. Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**
25	CLOCK_IF_SEL	Specifies the clock source for "clk_if". Must be 0 (clk_pll_normal) before entering DeepSleep; can be returned to 1 (clk_pll_direct) afterwards. '0': clk_pll_normal is used to create clk_if '1': clk_pll_direct is used to create clk_if Default Value: 0

22.1.71 SMIF0_CORE_CTL (continued)

24	BLOCK	Specifies what happens for MMIO interface read accesses to an empty RX data FIFO or to a full TX format/data FIFO. This field is not used for test controller accesses. Default Value: 0 **0x0: BUS_ERROR :** 0': Generate an AHB-Lite bus error. This option is useful when SW decides to use polling on STATUS.TR_BUSY to determine if a interface transfer is no longer busy (transfer is completed). This option adds SW complexity, but limits the number of AHB-Lite wait states (and limits ISR latency). **0x1: WAIT_STATES :** 1': Introduce wait states. This setting potentially locks up the AHB-Lite infrastructure and may increase the CPU interrupt latency.This option is useful when SW performs TX/RX data FIFO accesses immediately after a command is setup using the TX format FIFO. This option has low SW complexity, but may result in a significant number of AHB-Lite wait states (and may increase ISR latency). This can be particularly true if ARB_MODE=1 and an MMIO access must wait a potentially long time behind a XIP access.
23 : 22	SELECT_HOLD_DELAY	Specifies the duration between the last "spi_clk_out" falling edge and "spi_select_out[]" deactivating (going high) before considering any MDL delay due to CTL2.MDL_TAP_SEL. Add that delay to the below values, plus allow some margin for combinatorial variances between spi_select_out[] and spi_clk_out. i.e., if after adding the MDL delay the timing would barely meet the memory datasheet requirement then it is recommended to go to the next higher setting. These values apply for DDR mode, or SDR mode with CTL2.TX_SDR_EXTRA_SETUP=0. For SDR mode with CTL2.TX_SDR_EXTRA_SETUP=1 subtract 1 PLL clock cycle from these values. DDR or SDR mode is determined by the mode of the last phase of the transaction. "0": 1 memory interface clock cycle + CTL2.CLKOUT_DIV adjustment "1": 2 memory interface clock cycles + CTL2.CLKOUT_DIV adjustment "2": 3 memory interface clock cycles + CTL2.CLKOUT_DIV adjustment "3": 4 memory interface clock cycles + CTL2.CLKOUT_DIV adjustment For the following settings of CTL2.CLKOUT_DIV apply these adjustments to the above: 0 (DIV2): subtract 1 PLL clock cycle 1 (DIV4): no adjustment needed 2 (DIV8): add 2 PLL clock cycles 3 (DIV16): add 6 PLL clock cycles Default Value: 1
21 : 20	SELECT_SETUP_DELAY	Specifies the duration between "spi_select_out[]" activating (going low) to the first "spi_clk_out" rising edge before considering any MDL delay due to CTL2.MDL_TAP_SEL. Subtract that delay from the below values, plus allow some margin for combinatorial variances between spi_select_out[] and spi_clk_out. i.e., if after subtracting the MDL delay the timing would barely meet the memory datasheet requirement then it is recommended to go to the next higher setting. These values apply for DDR mode, or SDR mode with CTL2.TX_SDR_EXTRA_SETUP=0. For SDR mode with CTL2.TX_SDR_EXTRA_SETUP=1 add 1 PLL clock cycle to these values. DDR or SDR mode is determined by the mode of the first phase of the transaction. "0": 2 PLL clock cycles "1": 2 PLL clock cycles + 1 memory interface clock cycles "2": 2 PLL clock cycles + 2 memory interface clock cycles "3": 2 PLL clock cycles + 3 memory interface clock cycles Default Value: 1

22.1.71 SMIF0_CORE_CTL (continued)

18 : 16	DESELECT_DELAY	Specifies the minimum duration of SPI deselection ("spi_select_out[]" is high/'1') in between SPI transfers: "0": 1 memory interface clock cycle. "1": 2 memory interface clock cycles. "2": 3 memory interface clock cycles. "3": 4 memory interface clock cycles. "4": 5 memory interface clock cycles. "5": 6 memory interface clock cycles. "6": 7 memory interface clock cycles. "7": 8 memory interface clock cycles. During SPI deselection, "spi_select_out[]" are '1'/inactive, "spi_data_out[]" are '1' and "spi_-clk_out" is '0'/inactive. Default Value: 0
0	XIP_MODE	Mode of operation. Note: this field should only be changed when the IP is disabled or when STATUS.BUSY is '0' and SW should not be executing from the XIP interface or MMIO interface. Default Value: 0 **0x0: MMIO_MODE :** '0': MMIO mode. Individual MMIO accesses to TX and RX FIFOs are used to generate a sequence of SPI transfers. This mode of operation allows for large flexibility in terms of the SPI transfers that can be generated. **0x1: ARB_MODE :** "1': Arbitration mode. Arbitrates XIP vs. MMIO SPI/xSPI accesses such that any ongoing, pending, or "merged" transactions on XIP always take priority over any MMIO accesses to the device. However, if an MMIO access is in process it cannot be interrupted until it completes (as defined by sending the "last command" via TX_CMD_MMIO_FIFO_WR). If MMIO accesses are not happening at all, though, then the XIP accesses endure no extra arbitration latency.

22.1.72 SMIF0_CORE_STATUS

Description: Status

Address: 0x44460004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							DLL_LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	BUSY	Reserved [30:24]						

Bits	Name	Description
31	BUSY	AHB Cache, AXI interface, cryptography, XIP, device interface, MPC (if present) initialization, or any other key logic busy in the IP: '0': not busy '1': busy When BUSY is '0', the IP can be safely disabled without: - the potential loss of transient write data. - the potential risk of aborting an inflight SPI device interface transfer. - disrupting MPC (if present) initialization When BUSY is '0', the mode of operation (ARB_MODE or MMIO_MODE) can be safely changed. Default Value: Undefined
0	DLL_LOCKED	DLL lock status signal 0: DLL not locked 1b: DLL locked (also set to 1b after entering open-loop mode) Once the reference clock to the DLL is stable and the DLL is powered (CTL.ENABLED=1), the DLL should lock within 8us. The lock time will also be incurred when transitioning from DeepSleep to Active. Wait another 4us beyond the lock indication before executing any transactions on the memory interface; the MDL and SDLs require that extra time after the lock indication to reach their final stable delay values. If the DLL suddenly becomes unlocked then the TX interface will be held in reset to prevent any further transactions to the memory. The block should be disabled (CTL.ENABLED=0) to reset all other non-retention registers. Any data in the internal FIFOs will be lost. The DLL suddenly unlocking is considered an unusual event that would only occur if the reference clock to the DLL had a sudden change in frequency, which should only happen at the direction of SW. When transitioning to DeepSleep the DLL will naturally unlock. However, upon returning to Active all non-retention registers are reset and thus disabling the block to enact that reset is not necessary. Default Value: Undefined

22.1.73 SMIF0_CORE_CTL2

Description: Control 2

Address: 0x44460008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	DLL_IGNORE_LOCK	DLL_MDL_BYPASS_MODE	CLKOUT_DIV [5:4]		DLL_BYPASS_MODE	DLL_OPEN LOOP_ENABLE	DLL_SPEED_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	DLL_UNLOCK_VALUE	DLL_GATING_PERIOD [14:12]			MDL_TAP_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	RX_CHASE_MARGIN [23:22]		RX_CAPTURE_MODE [21:20]		DLL_SKIP_LSB [19:18]		DLL_UNLOCK_VALUE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	TX_SDR_EXTRA_SETUP	Reserved [30:24]						

Bits	Name	Description
31	TX_SDR_EXTRA_SETUP	This field is only applicable in SDR transmit mode. 0: transmit data is launched nominally 1 PLL clock period ahead of the rising edge of the clock out to the memory 1: transmit data is launched nominally 2 PLL clock periods ahead of the rising edge of the clock out to the memory Default Value: 0
23 : 22	RX_CHASE_MARGIN	Determines how long the design should wait after sending the last clock out to the memory interface before "chase" clocks should be created internally to push remainder data in the interface pipeline into the RX FIFO. Lesser numbers allow for shorter deselect cycles between packets, but if the time is too short then the chase clocks will interfere with the normal capture clock from the last clock cycle from the memory interface (whether it is feedback or RWDS). So a proper balance must be struck. The default value is expected to work for all situations. Other values are there as a backup plan in case something more aggressive can be achieved or whether something even more conservative should be used. Default Value: 2

22.1.73 SMIF0_CORE_CTL2 (continued)

21 : 20	RX_CAPTURE_MODE	Determines the receive capture mode: 0: Normal SPI without DLP 1: Normal SPI with DLP 2: Hyperbus / xSPI / Octal SPI w/DQS When using RX_CAPTURE_MODE=2: 1) DEVICE.RX_CAPTURE_CONFIG.DDR_PIPELINE_POS_DAT must be set to 1 2) DEVICE.RX_CAPTURE_CONFIG.DDR_SWAP_BYTES MMIO programming is ignored, bytes are always swapped as if set to 1. Default Value: 0
19 : 18	DLL_SKIP_LSB	number of LSBs which are skipped for loop regulation 00b: 0 (default) 01b: 1 10b: 2 11b: 3 Default Value: 0
17 : 15	DLL_UNLOCK_VALUE	value for the unlock counter 000b: 8 001b: 16 (default) 010b: 24 011b: 32 100b: 64 101b: 128 110b: 256 111b: 1023 Default Value: 1
14 : 12	DLL_GATING_PERIOD	Gating period of the digital logic 000b: 2 clock cycles -- use only in burn-in 001b: 4 clock cycles -- don't use 010b: 8 clock cycles -- don't use 011b: 16 clock cycles 100b: 24 clock cycles 101b: 32 clock cycles (default) 110b: 40 clock cycles 111b: 48 clock cycles Default Value: 5
11 : 8	MDL_TAP_SEL	Determines the relative amount of delay through the MDL for the reference clock in terms of the number of tap delays. There are 16 MDL taps that evenly divide the reference clock period into 16 delay steps. Setting 0 constitutes 1 tap delay, setting 1 constitutes 2 tap delays, etc., setting 15 constitutes 16 tap delays (which is effectively a full MDL reference clock period). Tap delay 15 is only verified in openloop mode as it can't send data reliably in functional simulations. Default Value: 0
7	DLL_IGNORE_LOCK	When set to 1, is used to block the TX logic reset that is generated when the DLL unlocks. 0b: Reset the TX logic when DLL unlocks 1b: Ignore the DLL unlock, do not reset the TX logic Default Value: 0
6	DLL_MDL_BYPASS_-MODE	Bypass MDL only. Transmit clock is generated from clk_pll and transmit data is clocked with inverted clk_pll. DLL is enabled because SDL phases are needed for receive data. 0b: MDL is not bypassed 1b: MDL is bypassed Default Value: 0
5 : 4	CLKOUT_DIV	The clock out to the memory is a divided version of the MDL clock out: 0: divide by 2 1: divide by 4 2: divide by 8 3: divide by 16 Default Value: 0
3	DLL_BYPASS_MODE	Bypass DLL in lower frequencies 0b: DLL is enabled if CTL.EN = 1 and not bypassed 1b: DLL is disabled independent of CTL.EN and bypassed Default Value: 0

22.1.73 SMIF0_CORE_CTL2 (continued)

2	DLL_OPENLOOP_ENABLE	operate the DLL in open loop mode (frequency < 150MHz) 0b: DLL tries to lock (150MHz - 400MHz) (default) 1b: DLL runs in open loop. DLL does not try to lock when open loop mode is selected independent of the frequency of the input clock. Default Value: 0
1 : 0	DLL_SPEED_MODE	Set according to the PLL clock frequency that feeds the DLL: speed mode control speed mode control 00b: 150-192MHz (default) 01b: 193-245MHz 10b: 246-313MHz 11b: 314 - 400MHz Default Value: 0

22.1.74 SMIF0_CORE_DLP_DELAY_TAP_SEL0

Description: DLP Delay Tap Select Register 0

Address: 0x44460010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA_BIT0_TAP_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA_BIT1_TAP_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA_BIT2_TAP_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA_BIT3_TAP_SEL [31:24]							

Bits	Name	Description
31 : 24	DATA_BIT3_TAP_SEL	Delay line tap selection for the IP's spi_data[3] (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: Undefined
23 : 16	DATA_BIT2_TAP_SEL	Delay line tap selection for the IP's spi_data[2] (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: Undefined
15 : 8	DATA_BIT1_TAP_SEL	Delay line tap selection for the IP's spi_data[1] (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: Undefined
7 : 0	DATA_BIT0_TAP_SEL	DLP tap selection for the IP's spi_data[0] (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). In SDR mode: The upper 4 bits of this field are zero, while the lower 4 bits represent the winning tap selection for all received bits on this data line. In DDR mode: The upper 4 bits of this field represent the winning tap selection for the bits received in the MSB data of the DDR pair, while the lower 4 bits represent the winning tap selection for the bits received in the LSB data of the DDR pair on this data line. A "winning tap selection" in either case is mapped as {tap15 of neg SDL, tap13 of neg SDL,..., tap1 of neg SDL, tap15 of pos SDL, tap13 of pos SDL,..., tap1 of pos SDL} for values 15 to 0, respectively. Default Value: Undefined

22.1.75 SMIF0_CORE_DLP_DELAY_TAP_SEL1

Description: DLP Delay Tap Select Register 1

Address: 0x44460014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA_BIT4_TAP_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA_BIT5_TAP_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA_BIT6_TAP_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA_BIT7_TAP_SEL [31:24]							

Bits	Name	Description
31 : 24	DATA_BIT7_TAP_SEL	Delay line tap selection for the IP's spi_data[7] (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: Undefined
23 : 16	DATA_BIT6_TAP_SEL	Delay line tap selection for the IP's spi_data[6] (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: Undefined
15 : 8	DATA_BIT5_TAP_SEL	Delay line tap selection for the IP's spi_data[5] (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: Undefined
7 : 0	DATA_BIT4_TAP_SEL	Delay line tap selection for the IP's spi_data[4] (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: Undefined

22.1.76 SMIF0_CORE_DLP_CTL

Description: DLP Control Register

Address: 0x44460018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DLP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DLP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				DLP_SIZE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				DLP_WARNING_LEVEL [27:24]			

Bits	Name	Description
27 : 24	DLP_WARNING_LEVEL	Determines when the DLP_WARNING interrupt cause field is set: - DLP_WARNING is set when the number of delay line taps resulting to a correctly captured DLP is less than DLP_WARNING_LEVEL for at least one input data line Note: To provide a margin in both directions relatively to the selected middle tap at least 3 delay line taps have to result into a correctly captured DLP, i.e. the DLP_WARNING_LEVEL has to be set to greater or equal 3. Default Value: 0x3
19 : 16	DLP_SIZE	Size of data learning pattern as such: "0": 1 bit ... "15": 16 bit. If CTL2.RX_CAPTURE_MODE=1 then the DLP_SIZE+1 LSBs of the expected data learning pattern (DLP[DLP_SIZE:0]) are compared with the data learning pattern generated by the memory device and captured during the last latency / dummy cycles of a memory read transfer. Note: For DDR read data transfers the size of the DLP must be an even number, i.e. DLP_SIZE must be an odd number. Default Value: 0x7
15 : 0	DLP	Data Learning Pattern Default Value: 0x0000

22.1.77 SMIF0_CORE_DLP_STATUS0

Description: DLP Status Register 0

Address: 0x44460020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [7:5]			DATA_BIT0 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [15:13]			DATA_BIT1 [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [23:21]			DATA_BIT2 [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			DATA_BIT3 [28:24]				

Bits	Name	Description
28 : 24	DATA_BIT3	Same as the DATA_BIT0 description except for spi_data[3] Default Value: Undefined
20 : 16	DATA_BIT2	Same as the DATA_BIT0 description except for spi_data[2] Default Value: Undefined
12 : 8	DATA_BIT1	Same as the DATA_BIT0 description except for spi_data[1] Default Value: Undefined
4 : 0	DATA_BIT0	In SDR mode: Number of delay line taps for the IP's spi_data[0] (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL) with correctly captured DLP in last read transaction. Legal values: 0 to 16. In DDR mode: Similar to SDR except the MSB and LSB data of the DDR pair are evaluated separately and this field reflects the least number of successful taps between those two evaluations. Default Value: Undefined

22.1.78 SMIF0_CORE_DLP_STATUS1

Description: DLP Status Register 1

Address: 0x44460024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [7:5]			DATA_BIT4 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [15:13]			DATA_BIT5 [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [23:21]			DATA_BIT6 [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R				
HW Access	Reserved			W				
Name	Reserved [31:29]			DATA_BIT7 [28:24]				

Bits	Name	Description
28 : 24	DATA_BIT7	Same as the DATA_BIT0 description except for spi_data[7] Default Value: Undefined
20 : 16	DATA_BIT6	Same as the DATA_BIT0 description except for spi_data[6] Default Value: Undefined
12 : 8	DATA_BIT5	Same as the DATA_BIT0 description except for spi_data[5] Default Value: Undefined
4 : 0	DATA_BIT4	Same as the DATA_BIT0 description except for spi_data[4] Default Value: Undefined

22.1.79 SMIF0_CORE_TX_CMD_FIFO_STATUS

Description: Transmitter command FIFO status

Address: 0x44460044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				USED4 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	USED4	Number of entries that are used in the TX command FIFO. Legal range: [0, 8]. Default Value: 0

22.1.80 SMIF0_CORE_TX_CMD_MMIO_FIFO_STATUS

Description: Transmitter command MMIO FIFO status

Address: 0x44460048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				USED4 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	USED4	Number of entries that are used in the TX command MMIO FIFO. Legal range: [0, 8]. Default Value: 0

22.1.81 SMIF0_CORE_TX_CMD_MMIO_FIFO_WR

Description: Transmitter command MMIO FIFO write

Address: 0x44460050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA27 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA27 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA27 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					W		
HW Access	Reserved					R		
Name	Reserved [31:27]					DATA27 [26:24]		

Bits	Name	Description

22.1.81 SMIF0_CORE_TX_CMD_MMIO_FIFO_WR (continued)

26 : 0	DATA27	Command data. The higher two bits DATA[26:24] specify the specific command "0"/TX: A SPI transfer always start with a TX command FIFO entry of the "TX" format. - DATA[23:20] specifies which of the four devices are selected. DATA[23:20] are directly mapped to "spi_select_out[3:0]". Two devices can be selected at the same time in dual-quad mode. - '0': device deselected - '1': device selected - DATA[19] specifies whether this is the last TX Byte; i.e. whether the "spi_select_out[3:0]" IO output signals are de-activated after the transfer. - "0": not the last TX byte - "1": the last TX byte - DATA[18] specifies the mode of transfer rate: - "0": SDR mode - "1": DDR mode - DATA[17:16] specifies the width of the data transfer: - "0": 1 bit/cycle (single data transfer). - "1": 2 bits/cycle (dual data transfer). - "2": 4 bits/cycle (quad data transfer). - "3": 8 bits/cycle (octal data transfer). - DATA[15:8] specifies the second transmitted Byte. This is only used (and must be specified) for octal data transfer with DDR mode, i.e. when DATA[17:16]="3" and DATA[18]="1". - DATA[7:0] specifies the transmitted Byte. "1"/TX_COUNT: The "TX_COUNT" command relies on the TX data FIFO to provide the transmitted bytes. - DATA[19] specifies whether this is the last command of a data transfer; i.e. whether the "spi_select_out[3:0]" IO output signals are de-activated after the transfer. - DATA[18] specifies the mode of transfer rate. - DATA[17:16] specifies the width of the transfer. - DATA[15:0] specifies the number of to be transmitted memory data units (minus 1). "0": 1 unit, "1": 2 units. For SPI (except octal SPI with DDR) one memory data unit is a byte, for octal SPI with DDR and Hyperbus one memory data unit is a 2-byte word. The number of used TX data FIFO entries (in TX_DATA_MMIO_FIFO_STATUS) = number of memory data units to be transmitted. "2"/RX_COUNT: The "RX_COUNT" command relies on the RX data FIFO to accept the received bytes. - DATA[19] specifies whether this is the last command of a data transfer; i.e. whether the "spi_select_out[3:0]" IO output signals are de-activated after the transfer. - DATA[18] specifies the mode of transfer rate. - DATA[17:16] specifies the width of the transfer. - DATA[15:0] specifies the number of to be received memory data units (minus 1). "0": 1 unit, "1": 2 units. For SPI (except octal SPI with DDR) one memory data unit is a byte, for octal SPI with DDR and Hyperbus one memory data unit is a 2-byte word. The number of used RX data FIFO entries (in RX_DATA_FIFO_STATUS) = number of memory data units to be received * 8 / data width (1, 2, 4, 8). The number of used RX data MMIO FIFO entries (in RX_DATA_MMIO_FIFO_STATUS) = number of bytes. "3"/DUMMY_COUNT: The "DUMMY_COUNT" command conveys dummy cycles. Dummy cycles are used to implement a Turn-Around time in which the SPI master changes from a transmitter driving the data lines to a receiver receiving on the same data lines. The "DUMMY_COUNT" command is ALWAYS considered to be NOT the last command of a SPI data transfer; i.e. it needs to be followed by another command. - DATA[23] specifies whether RWDS / DQS based capturing is enabled in the last dummy cycle, i.e. this needs to be set to '1' for read transactions to memory device using RWDS / DQS capturing scheme. - DATA[21] specifies whether the RWDS output signal should be driven starting in the last dummy cycle until DESELECT. This is needed for write transactions with RWDS (e.g. Hyperbus) before a TX_COUNT command. - DATA[20] specifies whether an active RWDS refresh indicator (captured with the previous rising memory clock output) causes to double the number of dummy cycles. This is used for the variable latency in HyperRAM. - DATA[18] specifies the mode of transfer rate. This is used for data learning and RWDS / DQS capturing. For XIP accesses this field is taken from DEVICE.RD_DATA_CTL.DDR_MODE. - DATA[17:16] specifies the width of the transfer. This is used for data learning and RWDS / DQS capturing. For XIP accesses this field is taken from DEVICE.RD_DATA_CTL.WIDTH. - DATA[15:0] specifies the number of dummy cycles (minus 1). In dummy cycles, the data lines are not driven. Notes: - If transmitting command, address and mode fields in SDR mode (driving data between falling edges of spihb_clk_out) and the memory is driving read data in DDR mode (based on memory type and transmitted command), then there must be at least 1 latency / dummy cycle specified (DUMMY_COUNT command must be present) to prevent controller and memory driving data signals at the same time. The same is true for the theoretical (practically irrelevant case) of transmitting at least one of the command, address and mode fields in DDR mode but receiving data from the memory in SDR mode. - When using the RWDS / DQS based capturing scheme (CTL2.RX_CAPTURE_MODE]), then there is a minimum number of latency / dummy cycles required (DUMMY_COUNT command must be present). For the Hyperbus protocol (DDR_CTL.SIZE3=7) at least 1 latency / dummy cycle has to be specified, for SPI with DQS capturing at least 2 latency / dummy cycles need to be selected (RD_DUMMY_CTL.SIZE5 > 0, exception see following note). - In case of falling edge RWDS / DQS capturing (CTL.CLOCK_IF_RX_SEL = "6") and SDR mode, SW should reduce the number of dummy cycles by 1 compared to the latency cycles required by the memory device. "4"/DESELECT: The "DESELECT" command de-activates the "spi"select_out[3:0] IO output signals. The "DESELECT" command is ALWAYS considered to be the last command of an SPI data transfer. It is used to finish the last transfer of merged continuous transfers. Default Value: 0

22.1.82 SMIF0_CORE_TX_DATA_MMIO_FIFO_CTL

Description: Transmitter data MMIO FIFO control

Address: 0x44460080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					TX_TRIGGER_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	TX_TRIGGER_LEVEL	Determines when the TX data MMIO FIFO "tr_tx_req" trigger is activated: - Trigger is active when TX_DATA_MMIO FIFO_STATUS.USED < TRIGGER_LEVEL. Default Value: 0

22.1.83 SMIF0_CORE_TX_DATA_FIFO_STATUS

Description: Transmitter data FIFO status

Address: 0x44460084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				USED4 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	USED4	Number of entries that are used in the TX data FIFO. Legal range: [0, 8]. Default Value: 0

22.1.84 SMIF0_CORE_TX_DATA_MMIO_FIFO_STATUS

Description: Transmitter data MMIO FIFO status

Address: 0x44460088

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				USED4 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	USED4	Number of entries that are used in the TX data MMIO FIFO. Legal range: [0, 8]. Default Value: 0

22.1.85 SMIF0_CORE_TX_DATA_MMIO_FIFO_WR1

Description: Transmitter data MMIO FIFO write

Address: 0x44460090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DATA0	TX data (written to TX data MMIO FIFO). Default Value: 0

22.1.86 SMIF0_CORE_TX_DATA_MMIO_FIFO_WR2

Description: Transmitter data MMIO FIFO write

Address: 0x44460094

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	DATA1	TX data (written to TX data MMIO FIFO, second byte). Default Value: 0
7 : 0	DATA0	TX data (written to TX data MMIO FIFO, first byte). Default Value: 0

22.1.87 SMIF0_CORE_TX_DATA_MMIO_FIFO_WR4

Description: Transmitter data MMIO FIFO write

Address: 0x44460098

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA3 [31:24]							

Bits	Name	Description
31 : 24	DATA3	TX data (written to TX data MMIO FIFO, fourth byte). Default Value: 0
23 : 16	DATA2	TX data (written to TX data MMIO FIFO, third byte). Default Value: 0
15 : 8	DATA1	TX data (written to TX data MMIO FIFO, second byte). Default Value: 0
7 : 0	DATA0	TX data (written to TX data MMIO FIFO, first byte). Default Value: 0

22.1.88 SMIF0_CORE_TX_DATA_MMIO_FIFO_WR1ODD

Description: Transmitter data MMIO FIFO write

Address: 0x4446009C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DATA0	TX data (written to TX data MMIO FIFO). Default Value: 0

22.1.89 SMIF0_CORE_RX_DATA_MMIO_FIFO_CTL

Description: Receiver data MMIO FIFO control

Address: 0x444600C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					RX_TRIGGER_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	RX_TRIGGER_LEVEL	Determines when RX data FIFO "tr_rx_req" trigger is activated: - Trigger is active when RX_DATA_MMIO_FIFO_STATUS.USED > TRIGGER_LEVEL. Default Value: 0

22.1.90 SMIF0_CORE_RX_DATA_MMIO_FIFO_STATUS

Description: Receiver data MMIO FIFO status

Address: 0x444600C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				USED4 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	USED4	Number of entries that are used in the RX data MMIO FIFO. Legal range: [0, 8]. Default Value: 0

22.1.91 SMIF0_CORE_RX_DATA_FIFO_STATUS

Description: Receiver data FIFO status

Address: 0x444600C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [7:4]				USED4 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							RX_S-R_USED

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	RX_SR_USED	Data available in RX Shift Register, i.e. completely read from RX data FIFO. Default Value: 0
3 : 0	USED4	Number of entries that are used in the RX data FIFO. Legal range: [0, 8]. Default Value: 0

22.1.92 SMIF0_CORE_RX_DATA_MMIO_FIFO_RD1

Description: Receiver data MMIO FIFO read

Address: 0x444600D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DATA0	RX data (read from RX data FIFO). Default Value: 0

22.1.93 SMIF0_CORE_RX_DATA_MMIO_FIFO_RD2

Description: Receiver data MMIO FIFO read

Address: 0x444600D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	DATA1	RX data (read from RX data FIFO, second byte). Default Value: 0
7 : 0	DATA0	RX data (read from RX data FIFO, first byte). Default Value: 0

22.1.94 SMIF0_CORE_RX_DATA_MMIO_FIFO_RD4

Description: Receiver data MMIO FIFO read

Address: 0x444600D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA3 [31:24]							

Bits	Name	Description
31 : 24	DATA3	RX data (read from RX data FIFO, fourth byte). Default Value: 0
23 : 16	DATA2	RX data (read from RX data FIFO, third byte). Default Value: 0
15 : 8	DATA1	RX data (read from RX data FIFO, second byte). Default Value: 0
7 : 0	DATA0	RX data (read from RX data FIFO, first byte). Default Value: 0

22.1.95 SMIF0_CORE_RX_DATA_MMIO_FIFO_RD1_SILENT

Description: Receiver data MMIO FIFO silent read

Address: 0x444600E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DATA0	RX data (read from RX data FIFO). Default Value: 0

22.1.96 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_CMD

Description: Cryptography command

Address: 0x44460200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							RW1C
Name	Reserved [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	START	SW sets this field to '1' to start an AES-128 forward block cipher operation (on CRYPTO_INPUT0-3). HW sets this field to '0' to indicate that the operation has completed. Once completed, the result of the operation can be read from CRYPTO_OUTPUT0, ..., CRYPTO_OUTPUT3. The operation takes roughly 13 clk_mem clock cycles. This register is only applicable for MMIO accesses and only in MMIO_MODE. XIP accesses are encrypted on-the-fly in ARB_MODE and thus do not use this register. Because XIP has exclusive access to the crypto engine in ARB_MODE, MMIO encryption is not available in that mode. As such if encryption is needed for MMIO accesses in ARB_MODE that encryption must be done by other means (i.e., chip level crypto). Default Value: 0

22.1.97 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_ADDR

Description: Cryptography base address

Address: 0x44460204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 8	ADDR	Only applies to XIP accesses. Specifies the base address of the memory region that will have cryptography applied on XIP accesses with a unique key. If this region overlaps with another key's region, the lower numbered key is used (i.e., crypto key 0 has the highest priority). If the region is 2^m Bytes, ADDR MUST be a multiple of 2^m. The most significant bit fields are constants and set based on the SMIF_XIP_ADDR parameter. The most significant bits are identified on the SMIF_XIP_MASK parameter. E.g., if SMIF_XIP_MASK is 0xff00:0000 (16 MB XIP memory region), ADDR[31:24] = SMIF_XIP_ADDR[31:24]. Note that in order for cryptogrpahy to be applied the DEVICE.CTL.CRYPTO_EN must be set to 1 as well for any devices that share this region. Default Value: 0

22.1.98 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_MASK

Description: Cryptography mask

Address: 0x44460208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	MASK [31:24]							

Bits	Name	Description
31 : 8	MASK	Only applies to XIP accesses. Specifies the size of the memory region whose base address is determined by CRYPTO_ADDR. All '1' bits are used to compare the incoming transfer request address A[31:0] with the address as specified in CRYPTO_ADDR.ADDR: Address A is in the cryptography region when (A[31:8] & MASK[31:8]) == CRYPTO_ADDR.ADDR[31:8]. The most significant bit fields are constants and set to'1'. The most significant bits are identified on the SMIF_XIP_MASK parameter. E.g., if SMIF_XIP_MASK is 0xff00:0000 (16 MB XIP memory region), MASK[31:24] = 0xff. Default Value: 0

22.1.99 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_SUBREGION

Description: Cryptography subregion disable

Address: 0x4446020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	SUBREGION_DISABLE	Only applies to XIP accesses. The cryptography region for this key as determined by CRYPTO_ADDR and CRYPTO_MASK is further divided into 8 equal subregions. e.g., if a 1 MB region is specified then the 8 subregions will be 128 KB. If SUBREGION_DISABLE=0 then cryptography will be performed on that subregion (assuming any associated DEVICE.CTL.CRYPTO_EN=1). Otherwise if SUBREGION_DISABLE=1 then cryptography is not applied. Note that setting all SUBREGION_DISABLE bits to 1 will effectively disable this key. The encryption decision and the associated key are locked in at the beginning of a memory access and will apply until the end of such atomic accesses. Therefore, it is the user's responsibility to ensure memory accesses do not span across (sub)regions that have different keys and/or crypto enabled/disabled differently across such (sub)regions. Default Value: 0

22.1.100 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT0

Description: Cryptography input 0

Address: 0x44460220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INPUT_MSB [7:4]				INPUT_LSB [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT_MSB [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT_MSB [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT_MSB [31:24]							

Bits	Name	Description
31 : 4	INPUT_MSB	Plaintext PT[31:4] = CRYPTO_INPUT0.INPUT_MSB. Default Value: Undefined
3 : 0	INPUT_LSB	Plaintext PT[3:0] = CRYPTO_INPUT0.INPUT_LSB. Default Value: Undefined

22.1.101 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT1

Description: Cryptography input 1

Address: 0x44460224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Plaintext PT[63:32] = CRYPTO_INPUT1.INPUT[31:0]. Default Value: Undefined

22.1.102 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT2

Description: Cryptography input 2

Address: 0x44460228

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Plaintext PT[95:64] = CRYPTO_INPUT2.INPUT[31:0]. Default Value: Undefined

22.1.103 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_INPUT3

Description: Cryptography input 3

Address: 0x4446022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Plaintext PT[127:96] = CRYPTO_INPUT3.INPUT[31:0]. Default Value: Undefined

22.1.104 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY0

Description: Cryptography key 0

Address: 0x44460240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[31:0] = CRYPTO_KEY0.KEY[31:0]. Default Value: Undefined

22.1.105 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY1

Description: Cryptography key 1

Address: 0x44460244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[63:32] = CRYPTO_KEY1.KEY[31:0]. Default Value: Undefined

22.1.106 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY2

Description: Cryptography key 2

Address: 0x44460248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[95:64] = CRYPTO_KEY2.KEY[31:0]. Default Value: Undefined

22.1.107 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_KEY3

Description: Cryptography key 3

Address: 0x4446024C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[127:96] = CRYPTO_KEY3.KEY[31:0]. Default Value: Undefined

22.1.108 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT0

Description: Cryptography output 0

Address: 0x44460260

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[31:0] = CRYPTO_OUTPUT0.OUTPUT[31:0]. Default Value: Undefined

22.1.109 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT1

Description: Cryptography output 1

Address: 0x44460264

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[63:32] = CRYPTO_OUTPUT1.OUTPUT[31:0]. Default Value: Undefined

22.1.110 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT2

Description: Cryptography output 2

Address: 0x44460268

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[95:64] = CRYPTO_OUTPUT2.OUTPUT[31:0]. Default Value: Undefined

22.1.111 SMIF0_CORE_SMIF_CRYPTO0_CRYPTO_OUTPUT3

Description: Cryptography output 3

Address: 0x4446026C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[127:96] = CRYPTO_OUTPUT3.OUTPUT[31:0]. Default Value: Undefined

22.1.112 SMIF0_CORE_INTR

Description: Interrupt register

Address: 0x444607C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	Reserved [7:6]		RX_-DATA_M-MIO_FIFO_UNDER-FLOW	TX_-DATA_FI-FO_OVERFLOW	TX_CM-D_FI-FO_OVERFLOW	XIP_ALIGN-MENT_ER-ROR	TR_RX-_REQ	TR_TX-_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW1C	RW1C	RW1C	Reserved			RW1C
HW Access	Reserved	RW1S	RW1S	RW1S	Reserved			RW1S
Name	Reserved	DLL_UN-LOCK	DLL_LOCK	DLP_WARN ING	Reserved [11:9]			DLP_FAIL

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	DLL_UNLOCK	DLL unlock (edge detected) Default Value: 0
13	DLL_LOCK	DLL lock (edge detected) Default Value: 0
12	DLP_WARNING	Data Learning Warning (for at least one input data line less then DLP.DLP_WARNING_LEVEL delay line taps resulted in a correct DLP capturing when CTL2.RX_CAPTURE_MODE=1). This interrupt will be suppressed, though, if DLP_FAIL also occurs during the same DLP evaluation cycle. Default Value: 0
8	DLP_FAIL	Data Learning Failed (no DLP match found on at least one of the input data lines when CTL2.RX-_CAPTURE_MODE=1). Default Value: 0
5	RX_DATA_MMIO_FI-FO_UNDERFLOW	Activated on an AHB-Lite read transfer from the RX data MMIO FIFO (RX_DATA_MMIO_FI-FO_RD1, RX_DATA_MMIO_FIFO_RD2, RX_DATA_MMIO_FIFO_RD4) with not enough entries available. Only activated for NON test bus controller transfers. Default Value: 0
4	TX_DATA_FIFO_OVER-FLOW	Activated on an AHB-Lite write transfer to the TX data MMIO FIFO (TX_DATA_MMIO_FI-FO_WR1, TX_DATA_MMIO_FIFO_WR2, TX_DATA_MMIO_FIFO_WR4, TX_DATA_MMIO_FI-FO_WR1ODD) with not enough free entries available. Default Value: 0

22.1.112 SMIF0_CORE_INTR (continued)

3	TX_CMD_FIFO_OVERFLOW	Activated on an AHB-Lite write transfer to the TX command MMIO FIFO (TX_CMD_MMIO_FIFO_WR) with not enough free entries available. Default Value: 0
2	XIP_ALIGNMENT_ERROR	Activated on a XIP access, when: - a write transfer is requested and - Dual-Quad SPI mode (selected device's ADDR_CTL.DIV2 is '1') is selected or - Octal SPI DDR mode (selected device's DATA_CTL.DDR_MODE = '1' and DATA_CTL.WIDTH = "3") or Hyperbus mode (selected device's ADDR_CTL.SIZE3 = "7") is selected without memory write byte masking (selected device's WR_DUMMY_CTL.RWDS_EN = '0') and - the AHB-Lite / AXI bus transfer address is not a multiple of "2" or - the requested AHB-Lite / AXI bus transfer size is NOT a multiple of "2". Additionally, it is activated on a XIP access when the selected memory device does not support write byte masking (WR_DUMMY_CTL.RWDS_EN=0) and an AXI transfer occurs with not all of the AXI write strobes ("wstrb") enabled according to the transfer size ("assize"). Note: In dual-quad SPI mode (ADDR_CTL.DIV is '1'), each memory device contributes a 4-bit nibble for read data or write data. Write accesses are only possible if the request address is a multiple of 2 and the number of requested Bytes is a multiple of 2. Octal SPI DDR mode or Hyperbus mode are 16-bit word based protocols, writing single bytes is only possible when write byte masking is supported (via RWDS). Read accesses are always possible by extending the transfer size and / or aligning the address as needed and discarding the non-relevant byte(s). Default Value: 0
1	TR_RX_REQ	Activated when a RX data MMIO FIFO trigger "tr_rx_req" is activated. Default Value: 0
0	TR_TX_REQ	Activated when a TX data MMIO FIFO trigger "tr_tx_req" is activated. Default Value: 0

22.1.113 SMIF0_CORE_INTR_SET

Description: Interrupt set register

Address: 0x444607C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	Reserved		A	A	A	A	A	A
Name	Reserved [7:6]		RX_-DATA_M-MIO_FIFO_UNDER-FLOW	TX_-DATA_FI-FO_OVERFLOW	TX_CM-D_FI-FO_OVERFLOW	XIP_ALIGN-MENT_ER-ROR	TR_RX-_REQ	TR_TX-_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW1S	RW1S	RW1S	Reserved			RW1S
HW Access	Reserved	A	A	A	Reserved			A
Name	Reserved	DLL_UN-LOCK	DLL_LOCK	DLP_WARNING	Reserved [11:9]			DLP_FAIL

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	DLL_UNLOCK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
13	DLL_LOCK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
12	DLP_WARNING	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	DLP_FAIL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	RX_DATA_MMIO_FI-FO_UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	TX_DATA_FIFO_OVER-FLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	TX_CMD_FIFO_OVER-FLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	XIP_ALIGNMENT_ER-ROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	TR_RX_REQ	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

22.1.113 SMIF0_CORE_INTR_SET (continued)

0	TR_TX_REQ	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

22.1.114 SMIF0_CORE_INTR_MASK

Description: Interrupt mask register

Address: 0x444607C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		RX_-DATA_M-MIO_FIFO_UNDER-FLOW	TX_-DATA_FI-FO_OVERFLOW	TX_CM-D_FI-FO_OVERFLOW	XIP_ALIGN-MENT_ER-ROR	TR_RX-_REQ	TR_TX-_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	Reserved			RW
HW Access	Reserved	R	R	R	Reserved			R
Name	Reserved	DLL_UN-LOCK	DLL_LOCK	DLP_WARNING	Reserved [11:9]			DLP_FAIL

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	DLL_UNLOCK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
13	DLL_LOCK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
12	DLP_WARNING	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	DLP_FAIL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	RX_DATA_MMIO_FI-FO_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	TX_DATA_FIFO_OVER-FLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	TX_CMD_FIFO_OVER-FLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	XIP_ALIGNMENT_ER-ROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	TR_RX_REQ	Mask bit for corresponding bit in interrupt request register. Default Value: 0

22.1.114 SMIF0_CORE_INTR_MASK (continued)

0	TR_TX_REQ	Mask bit for corresponding bit in interrupt request register. Default Value: 0

22.1.115 SMIF0_CORE_INTR_MASKED

Description: Interrupt masked register

Address: 0x444607CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		W	W	W	W	W	W
Name	Reserved [7:6]		RX_-DATA_M-MIO_FIFO_UNDER-FLOW	TX_-DATA_FI-FO_OVERFLOW	TX_CM-D_FI-FO_OVERFLOW	XIP_ALIGN-MENT_ER-ROR	TR_RX-_REQ	TR_TX-_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	R	R	R	Reserved			R
HW Access	Reserved	W	W	W	Reserved			W
Name	Reserved	DLL_UN-LOCK	DLL_LOCK	DLP_WARNING	Reserved [11:9]			DLP_FAIL

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	DLL_UNLOCK	Logical and of corresponding request and mask bits. Default Value: 0
13	DLL_LOCK	Logical and of corresponding request and mask bits. Default Value: 0
12	DLP_WARNING	Logical and of corresponding request and mask bits. Default Value: 0
8	DLP_FAIL	Logical and of corresponding request and mask bits. Default Value: 0
5	RX_DATA_MMIO_FI-FO_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	TX_DATA_FIFO_OVER-FLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	TX_CMD_FIFO_OVER-FLOW	Logical and of corresponding request and mask bits. Default Value: 0
2	XIP_ALIGNMENT_ER-ROR	Logical and of corresponding request and mask bits. Default Value: 0
1	TR_RX_REQ	Logical and of corresponding request and mask bits. Default Value: 0

22.1.115 SMIF0_CORE_INTR_MASKED (continued)

0	TR_TX_REQ	Logical and of corresponding request and mask bits. Default Value: 0

22.1.116 SMIF0_CORE_DLL_IDAC

Description: DLL IDAC (when DLL runs in open loop, selects the delay of the delay line)

Address: 0x444607D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11 : 0	SEL	IDAC binary control (effective only if dll_openloop_en_i=1) 000h: max delay ... A7Fh: min delay Default Value: 0xA7F

22.1.117 SMIF0_CORE_DLL_IVR

Description: DLL IVR (Contol Output Voltage of internal Voltage Regulator)

Address: 0x444607DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					SELECT [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	SELECT	IVR output voltage selection 000b: 0.767V 001b: 0.795V 010b: 0.825V 011b: 0.857V (default) 100b: 0.892V 101b: 0.929V 110b: 0.971V (burn-in) 111b: 1.216V (don't use) Default Value: 0x3

22.1.118 SMIF0_CORE_DEVICE0_CTL

Description: Control

Address: 0x44460800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [7:5]			CRYP-TO_EN	Reserved [3:1]			WR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			Reserved		RW	
HW Access	R	R			Reserved		R	
Name	MERGE_EN	MERGE_TIMEOUT [14:12]			Reserved [11:10]		DATA_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TOTAL_TIMEOUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	ENABLED	TOTAL_-TIME-OUT_EN	TOTAL_TIMEOUT [29:24]					

Bits	Name	Description
31	ENABLED	Device enable: '0': Disabled. '1': Enabled. Default Value: 0
30	TOTAL_TIMEOUT_EN	Total transfer timeout enable. '0': Disabled. There is no limit for the total transfer time. The continuous transfer merge timeout for limiting the idle time of the memory interface still applies. '1': Enabled. The maximum total transfer time is limited by field TOTAL_TIMEOUT. Default Value: 0

22.1.118 SMIF0_CORE_DEVICE0_CTL (continued)

29 : 16	TOTAL_TIMEOUT	Total transfer timeout in clk_mem cycles. The counting of the total timout period is done in the XIP block using clk_mem cycles. It starts when the first command of a new (not merged) transaction is transferred to the TX command FIFO causing the interface logic to select the memory. After this period the memory device is deselected. This feature is needed for RAM devices requiring refresh cycles. The value needs to be derived from the RAMs maximum transaction length time (tCMS) minus the time of transferring 2x16byte data block (data granularity of the XIP ports is 16byte, 1 16byte block transfer outstanding, another available for merging). If the result in negative, MERGE_EN must be set to "0". Example: RAM device tCMS = 4us, interface clock frequency = 100MHz: total transfer timeout is 4us - 2x16x10ns = 3680ns. With clk_mem frequency of 200MHz the TOTAL_TIMEOUT value is 3680/5 = 736. Note: In the unlikely case that the total transfer timeout is used (usually for RAM devices) while the page boundary crossing latency generation is enabled via RD_BOUND_CTL.PRESENT (usually for FLASH devices) the additional time needs to taken into account. Default Value: 0
15	MERGE_EN	Continous transfer merge enable: '0': Disabled. No merging of transfers is done. Longest possible memory transfer is 16 Byte. '1': Enabled. Merging of continous transfers is done. This skips the overhead (command, address, mode, dummy cycles) for a continuous (linear sequential) transfer. Default Value: 0
14 : 12	MERGE_TIMEOUT	Continuous transfer merge timeout in clk_mem cycles. This limits the standby time of the memory interface, i.e. the time the memory device is selected but no data is transferred. The counting of the merge timeout period is done in the XIP block using clk_mem cycles. It starts when the last TX or RX byte is transferred to or from the data FIFOs. After this period the memory device is deselected. A later transfer, even from a continuous address, starts with the overhead phases (command, address, mode, dummy cycles). Default Value: 0 **0x0: _1_cycle :** Timeout after 1 clk_mem cycle. That means transfers will only be merged if the continuous transfer request is already available when the previous transfer is finished. **0x1: _16_cycles :** Timeout after 2^4 = 16 clk_mem cycles. At a clk_mem frequency of 200MHz this means 80ns. **0x2: _256_cycles :** Timeout after 2^8 = 256 clk_mem cycles. At a clk_mem frequency of 200MHz this means ~1.3us. **0x3: _4096_cycles :** Timeout after 2^12 = 4096 clk_mem cycles. At a clk_mem frequency of 200MHz this means ~20us. **0x4: _65536_cycles :** Timeout after 2^16 = 65536 clk_mem cycles. At a clk_mem frequency of 200MHz this means ~330us. **0x5: Reserved5 :** This setting is reserved. Do not use.

22.1.118 SMIF0_CORE_DEVICE0_CTL (continued)

		0x6: Reserved6 : This setting is reserved. Do not use. **0x7: Reserved7 :** This setting is reserved. Do not use.
9 : 8	DATA_SEL	Specifies the connection of the IP's data lines (spi_data[0], ..., spi_data[7]) to the device's data lines (SI/IO0, SO/IO1, IO2, IO3, IO4, IO5, IO6, IO7): "0": spi_data[0] = IO0, spi_data[1] = IO1, ..., spi_data[7] = IO7. This value is allowed for single, dual, quad, dual quad and octal SPI modes. This value must be used for the first device in dual quad SPI mode. This value must be used for octal SPI mode. "1": spi_data[2] = IO0, spi_data[3] = IO1. This value is only allowed for single and dual SPI modes. "2": spi_data[4] = IO0, spi_data[5] = IO1, ..., spi_data[7] = IO3. This value is only allowed for single, dual, quad and dual quad SPI modes. In dual quad SPI mode, this value must be used for the second device. "3": spi_data[6] = IO0, spi_data[7] = IO1. This value is only allowed for single and dual SPI modes. Default Value: 0
4	CRYPTO_EN	Cryptography on read/write accesses: '0': disabled. '1': enabled. This register should not be changed dynamically. Conditions 1. The same CRYPTO_EN setting should be used when a memory is read back after a write. 2. CRYPTO_EN should not be changed while IP is busy. Default Value: 0
0	WR_EN	Write enable: '0': write transfers are not allowed to this device. An attempt to write to this device results in an AHB-Lite bus error. '1': write transfers are allowed to this device. Default Value: 0

22.1.119 SMIF0_CORE_DEVICE0_ADDR

Description: Device region base address

Address: 0x44460808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 8	ADDR	Specifies the base address of the device region. If the device region is 2^m Bytes, ADDR MUST be a multiple of 2^m. In dual quad SPI data transfer, the two devices should have the same ADDR and MASK register settings. The device control information (ADDR_CTL, RD_CMD_CTL, etc.) are provided by the MMIO control registers of the device with the lowest index. The most significant bit fields are constants and set based on the SMIF_XIP_ADDR parameter. The most significant bits are identified on the SMIF_XIP_MASK parameter. E.g., if SMIF_X-IP_MASK is 0xff00:0000 (16 MB XIP memory region), ADDR[31:24] = SMIF_XIP_ADDR[31:24]. Default Value: Undefined

22.1.120 SMIF0_CORE_DEVICE0_MASK

Description: Device region mask

Address: 0x4446080C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	MASK [31:24]							

Bits	Name	Description
31 : 8	MASK	Specifies the size of the device region. All '1' bits are used to compare the incoming transfer request address A[31:0] with the address as specified in ADDR.ADDR: Address A is in the device when (A[31:8] & MASK[31:8]) == ADDR.ADDR[31:8]. The most significant bit fields are constants and set to'1'. The most significant bits are identified on the SMIF_XIP_MASK parameter. E.g., if SMIF_XIP_MASK is 0xff00:0000 (16 MB XIP memory region), MASK[31:24] = 0xff. Note: a transfer request that is not in any device region results in an AHB-Lite bus error. Default Value: Undefined

22.1.121 SMIF0_CORE_DEVICE0_ADDR_CTL

Description: Address control

Address: 0x44460820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					SIZE3 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							DIV2

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	DIV2	Specifies if the AHB-Lite bus transfer address is divided by 2 or not: '0': No divide by 2. '1': Divide by 2. This functionality is used for read and write operation in XIP, dual quad SPI mode; i.e. this DIV2 must be set to '1' in dual quad SPI mode. If DIV2 is set to '1', the memory does not support write masking (WR_DUMMY_CTL.RWDS_EN = '0'), and in this configuration a write transfer is requested and the write transfer request address is NOT a multiple of 2 or the requested number of Bytes to be written is not a multiple of 2, the XIP_ALIGNMENT_ERROR interrupt cause is activated. Default Value: 0
2 : 0	SIZE3	Specifies the size of the XIP device address in Bytes: "0": 1 Byte address. "1": 2 Byte address. "2": 3 Byte address. "3": 4 Byte address. "4"-"6": These settings are reserved. Do not use. "7": 4 Byte address (spread over 5 bytes) according to Hyperbus protocol. The lower significant address Bytes of the transfer request are used as XIP address to the external device. Note that for dual quad SPI data transfer, the XIP transfer request address is divided by 2. Therefore, the XIP transfer request address needs to be a multiple of 2. If the address is NOT a multiple of 2, the XIP_ALIGNMENT_ERROR interrupt cause is activated. Note: If Hyperbus protocol is selected (SIZE3="7") then the WIDTH field must be set to "3" (octal data transfer) and the DDR_MODE field must be set to "1" (DDR mode) in the read/write command and address control registers, and the PRESENT field in read/write command control registers need be set to "1" (1 command byte). Default Value: 0

22.1.122 SMIF0_CORE_DEVICE0_RX_CAPTURE_CONFIG

Description: RX capture configuration

Address: 0x44460828

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	POS_SDL_TAP_SEL [7:4]				NEG_SDL_TAP_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							FW_CALI-BRATION_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [23:18]						SDR_SWAP_BYTES	SDR_PIPE-LINE_NEG_DAT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [31:26]						DDR_SWAP_BYTES	DDR_PIPE-LINE_POS_DAT

Bits	Name	Description
25	DDR_SWAP_BYTES	0: Does not swap DDR receive data captured relative to the negedge of the receive clock with the data captured relative to the posedge of the receive clock 1: Does swap The setting DDR_SWAP_BYTES is ignored and operates as if set to 1 (even if set to 0) when CORE.CTL2.RX_CAPTURE_MODE=2 Default Value: 0
24	DDR_PIPELINE_POS_-DAT	0: Does not pipeline DDR receive data captured relative to the posedge of the receive clock 1: Does pipeline DDR_PIPELINE_POS_DAT must be set to "1" if CORE.CTL2.RX_CAPTURE_MODE=2 Default Value: 0
17	SDR_SWAP_BYTES	0: Does not swap SDR receive data captured relative to the negedge of the receive clock with the data captured relative to the posedge of the receive clock 1: Does swap Default Value: 0
16	SDR_PIPELINE_NEG_-DAT	0: Does not pipeline SDR receive data captured relative to the negedge of the receive clock 1: Does pipeline Default Value: 0

22.1.122 SMIF0_CORE_DEVICE0_RX_CAPTURE_CONFIG (continued)

8	FW_CALIBRATION_-MODE	0: Disabled 1: Enabled Hyperbus / xSPI / Octal SPI w/DQS and Software De-skewing Mode based on register HB FW Calibration tap sel0/1 Default Value: 0
7 : 4	POS_SDL_TAP_SEL	Same as NEG_SDL_TAP_SEL except for the "pos" SDL. Default Value: 0
3 : 0	NEG_SDL_TAP_SEL	Determines the amount of delay through the "neg" SDL for the receive clock coming from the pins in terms of the number of tap delays. There are 16 SDL taps and the delay resolution of each tap is controlled by and thus closely mimics the delay resolution of the MDL. i.e., each tap has a resolution roughly equal to 1/16th of the DLL reference clock period. Setting 0 constitutes 1 tap delay, setting 1 constitutes 2 tap delays, etc., setting 15 constitutes 16 tap delays (effectively a full DLL reference clock period). Default Value: 0

22.1.123 SMIF0_CORE_DEVICE0_RD_CMD_CTL

Description: Read command control

Address: 0x44460840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CODEH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [23:19]					DDR_-MODE	WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		Reserved					
HW Access	R		Reserved					
Name	PRESENT2 [31:30]		Reserved [29:24]					

Bits	Name	Description
31 : 30	PRESENT2	Presence of command field: '0': not present '1': present (1 Byte) '2': present (2 Byte for OPI) Note: For octal data transfer with DDR mode (WIDTH="3" and DDR_MODE="1") either the HB protocol needs to be selected (by ADDR_CTL.SIZE3="7") or this field needs to be set to PRESENT2="2". Default Value: 0
18	DDR_MODE	Mode of transfer rate: "0": SDR mode "1": DDR mode Default Value: 0
17 : 16	WIDTH	Width of data transfer: "0": 1 bit/cycle (single data transfer). "1": 2 bits/cycle (dual data transfer). "2": 4 bits/cycle (quad data transfer). "3": 8 bits/cycle (octal data transfer). Default Value: 0
15 : 8	CODEH	Command high byte code. This field specifies the most significant command byte, sent before the least significant command byte (CODE). It is only used when PRESENT2 = "2". Default Value: 0
7 : 0	CODE	Command byte code. Default Value: 0

22.1.124 SMIF0_CORE_DEVICE0_RD_ADDR_CTL

Description: Read address control

Address: 0x44460844

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [23:19]					DDR_-MODE	WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	DDR_MODE	Mode of transfer rate. Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0

22.1.125 SMIF0_CORE_DEVICE0_RD_MODE_CTL

Description: Read mode control

Address: 0x44460848

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CODEH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [23:19]					DDR_-MODE	WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		Reserved					
HW Access	R		Reserved					
Name	PRESENT2 [31:30]		Reserved [29:24]					

Bits	Name	Description
31 : 30	PRESENT2	Presence of mode field: '0': not present '1': present (1 Byte) '2': present (2 Byte for OPI) Note: For octal data transfer with DDR mode (WIDTH="3" and DDR_MODE="1") this field needs to be set to PRESENT2="2" to generate a mode field (or to PRESENT2="0"). Default Value: 0
18	DDR_MODE	Mode of transfer rate. Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0
15 : 8	CODEH	Mode high byte code. This field specifies the most significant mode byte, sent before the least significant mode byte (CODE). It is only used when PRESENT2 = "2". Default Value: 0
7 : 0	CODE	Mode byte code. Note: If a mode field is present (PRESENT='1') for octal data transfer with DDR mode (WIDTH="3" and DDR_MODE="1") the CODE is sent twice. Default Value: 0

22.1.126 SMIF0_CORE_DEVICE0_RD_DUMMY_CTL

Description: Read dummy control

Address: 0x4446084C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			SIZE5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		Reserved					
HW Access	R		Reserved					
Name	PRESENT2 [31:30]		Reserved [29:24]					

Bits	Name	Description
31 : 30	PRESENT2	Presence of dummy cycles: '0': not present '1': present '2': present - Dummy cycles are doubled when RWDS refresh indicator is high during CA cycle. (HyperRAM variable latency mode) Notes: - If transmitting command, address and mode fields in SDR mode (driving data between falling edges of spihb_clk_out) and the memory is driving read data in DDR mode (based on memory type and transmitted command), then there must be at least 1 latency / dummy cycle specified (RD_DUMMY_CTL.PRESENT2 > 0') to prevent controller and memory driving data signals at the same time. The same is true for the theoretical (practically irrelevant case) of transmitting at least one of the command, address and mode fields in DDR mode but receiving data from the memory in SDR mode. - When using the RWDS / DQS based capturing scheme (CTL2.RX_CAPTURE_MODE), then there is a minimum number of latency / dummy cycles required (RD_DUMMY_CTL.PRESENT2 > 0). For the Hyperbus protocol (DDR_CTL.SIZE3=7) at least 1 latency / dummy cycle has to be specified, for SPI with DQS capturing at least 2 latency / dummy cycles need to be selected (RD_DUMMY_CTL.SIZE5 > 0, exception see following note). - In case of falling edge RWDS / DQS capturing (CTL2.RX_CAPTURE_MODE) and SDR mode, SW should reduce the number of dummy cycles by 1 compared to the latency cycles required by the memory device. -DDR read commands need at least one dummy cycle -For Hyperbus, set RD DUMMY_CTL.SIZE5=initial latency cycles-2 Default Value: 0

22.1.126 SMIF0_CORE_DEVICE0_RD_DUMMY_CTL (continued)

4 : 0	SIZE5	Number of dummy cycles (minus 1): "0": 1 cycles ... "31": 32 cycles. Note: this field specifies dummy cycles, not dummy Bytes! Default Value: 0

22.1.127 SMIF0_CORE_DEVICE0_RD_DATA_CTL

Description: Read data control

Address: 0x44460850

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [23:19]					DDR_-MODE	WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	DDR_MODE	Mode of transfer rate. Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0

22.1.128 SMIF0_CORE_DEVICE0_RD_BOUND_CTL

Description: Read boundary control

Address: 0x44460858

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			SIZE5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW		Reserved		RW	
HW Access	Reserved		R		Reserved		R	
Name	Reserved [23:22]		SUB_PAGE_NR [21:20]		Reserved [19:18]		SUB_PAGE_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved		RW	Reserved			
HW Access	R	Reserved		R	Reserved			
Name	PRESENT	Reserved [30:29]		SUBSE-Q_BOUND_EN	Reserved [27:24]			

Bits	Name	Description
31	PRESENT	Presence of first page boundary latency cycles: '0': not present '1': present Default Value: 0
28	SUBSEQ_BOUND_EN	Enable subsequent page boundary latency cycles. '0': Disabled. The page crossing latency cycles are only generated when crossing the first page boundary (i.e. the first time when the SUB_PAGE_NRth sub page boundary is crossed, e.g. with 2 sub pages per page when the 2nd sub page boundary is crossed). '1': Enabled. The page crossing latency cycles are generated when crossing the first and subsequent page boundaries (i.e. every time when a SUB_PAGE_NRth sub page boundary is crossed, e.g. with 2 sub pages per page when the 2nd, 4th, 6th, ... sub page boundary is crossed). Note: This only applies when the number of base latency cycles (SIZE5+1) is greater than the size of a page (base_latency > page_size). Must be set to 0 otherwise. Default Value: 0
21 : 20	SUB_PAGE_NR	Specifies the number of sub pages per page. "0": 1 sub pages per page, i.e. page_size = sub_page_size "1": 2 sub pages per page, i.e. page_size = 2 x sub_page_size "2": 4 sub pages per page, i.e. page_size = 4 x sub_page_size "3": 8 sub pages per page, i.e. page_size = 8 x sub_page_size Default Value: 1

22.1.128 SMIF0_CORE_DEVICE0_RD_BOUND_CTL (continued)

17 : 16	SUB_PAGE_SIZE	Specifies the size of a memory sub page "sub_page_size". "0": sub_page_size = 8 words = 16 bytes (default). "1": sub_page_size = 16 words = 32 bytes. "2": sub_page_size = 32 words = 64 bytes. "3": sub_page_size = 64 words = 128 bytes. Default Value: 0

4 : 0	SIZE5	Number of base latency cycles (minus 1) used for calculating the number of fist page boundary crossing latency cycles:
		"0": base_latency = 1 cycles
		...
		"31": base_latency = 32 cycles.
		The actual latency cycles when crossing the first page boundary depend on the start address of the transaction and is calculated as follows:
		if ((page_size - base_latency) < Start_Addr & (sub_page_size - 1))
		{ ((Start_Addr & (sub_page_size - 1)) - page_size + base_latency) }
		else
		{ 0 }
		Default Value: 0

22.1.129 SMIF0_CORE_DEVICE0_WR_CMD_CTL

Description: Write command control

Address: 0x44460860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CODEH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [23:19]					DDR_-MODE	WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		Reserved					
HW Access	R		Reserved					
Name	PRESENT2 [31:30]		Reserved [29:24]					

Bits	Name	Description
31 : 30	PRESENT2	Presence of command field: '0': not present '1': present (1 Byte) '2': present (2 Byte for OPI) Note: For octal data transfer with DDR mode (WIDTH="3" and DDR_MODE="1") either the HB protocol needs to be selected (by ADDR_CTL.SIZE3="7") or this field needs to be set to PRESENT2="2". Default Value: 0
18	DDR_MODE	Mode of transfer rate. Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0
15 : 8	CODEH	Command high byte code. This field specifies the most significant command byte, sent before the least significant command byte (CODE). It is only used when PRESENT2 = "2". Default Value: 0
7 : 0	CODE	Command byte code. Default Value: 0

22.1.130 SMIF0_CORE_DEVICE0_WR_ADDR_CTL

Description: Write address control

Address: 0x44460864

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [23:19]					DDR_-MODE	WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	DDR_MODE	Mode of transfer rate. Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0

22.1.131 SMIF0_CORE_DEVICE0_WR_MODE_CTL

Description: Write mode control

Address: 0x44460868

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CODEH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [23:19]					DDR_-MODE	WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		Reserved					
HW Access	R		Reserved					
Name	PRESENT2 [31:30]		Reserved [29:24]					

Bits	Name	Description
31 : 30	PRESENT2	Presence of mode field: '0': not present '1': present (1 Byte) '2': present (2 Byte for OPI) Note: For octal data transfer with DDR mode (WIDTH="3" and DDR_MODE="1") this field needs to be set to PRESENT2="2" to generate a mode field (or to PRESENT2="0"). Default Value: 0
18	DDR_MODE	Mode of transfer rate. Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0
15 : 8	CODEH	Mode high byte code. This field specifies the most significant mode byte, sent before the least significant mode byte (CODE). It is only used when PRESENT2 = "2". Default Value: 0
7 : 0	CODE	Mode byte code. Default Value: 0

22.1.132 SMIF0_CORE_DEVICE0_WR_DUMMY_CTL

Description: Write dummy control

Address: 0x4446086C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			SIZE5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	Reserved
HW Access	Reserved						R	Reserved
Name	Reserved [23:18]						RWDS_EN	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	RW		Reserved					
HW Access	R		Reserved					
Name	PRESENT2 [31:30]		Reserved [29:24]					

Bits	Name	Description
31 : 30	PRESENT2	Presence of dummy cycles: '0': not present '1': present '2': present - Dummy cycles are doubled when RWDS refresh indicator is high during CA cycle. (HyperRAM variable latency mode) Default Value: 0
17	RWDS_EN	Read-Write-Data-Strobe Enable. Specifies whether the RWDS output signal should be driven starting in the last dummy cycle until DESELECT. This is needed for write transactions with byte masking via RWDS (e.g. Hyperbus). '0': do not drive RWDS output '1': drive RWDS output starting in last dummy cycle until DESELECT Note: this field is located in the WR_DUMMY_CTL register (and not in the WR_DATA_CTL register) since the RWDS signal needs to be driven already in the last dummy cycle. Default Value: 0
4 : 0	SIZE5	Number of dummy cycles (minus 1): "0": 1 cycles ... "31": 32 cycles. Default Value: 0

22.1.133 SMIF0_CORE_DEVICE0_WR_DATA_CTL

Description: Write data control

Address: 0x44460870

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [23:19]					DDR_-MODE	WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	DDR_MODE	Mode of transfer rate. Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0

22.1.134 SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0

Description: HB FW Calibration Delay Tap Select 0

Address: 0x44460878

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DATA_BIT0_TAP_SEL_NEG [7:4]				DATA_BIT0_TAP_SEL_POS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	DATA_BIT1_TAP_SEL_NEG [15:12]				DATA_BIT1_TAP_SEL_POS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	DATA_BIT2_TAP_SEL_NEG [23:20]				DATA_BIT2_TAP_SEL_POS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	DATA_BIT3_TAP_SEL_NEG [31:28]				DATA_BIT3_TAP_SEL_POS [27:24]			

Bits	Name	Description
31 : 28	DATA_BIT3_TAP_SEL_NEG	HB FW Calibration: Delay line tap select for spi_data[3], NEG Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
27 : 24	DATA_BIT3_TAP_SEL_POS	HB FW Calibration: Delay line tap select for spi_data[3], POS Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
23 : 20	DATA_BIT2_TAP_SEL_NEG	HB FW Calibration: Delay line tap select for spi_data[2], NEG Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
19 : 16	DATA_BIT2_TAP_SEL_POS	HB FW Calibration: Delay line tap select for spi_data[2], POS Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
15 : 12	DATA_BIT1_TAP_SEL_NEG	HBs FW Calibration: Delay line tap select for spi_data[1], NEG Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
11 : 8	DATA_BIT1_TAP_SEL_POS	HB FW Calibration: Delay line tap select for spi_data[1], POS Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0

22.1.134 SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_0 (continued)

7 : 4	DATA_BIT0_TAP_SEL_NEG	HB FW Calibration: Delay line tap select for spi_data[0], NEG Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
3 : 0	DATA_BIT0_TAP_SEL_-POS	HB FW Calibration tap select for spi_data[0], POS clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). Default Value: 0

22.1.135 SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1

Description: HB FW Calibration Delay Tap Select 1

Address: 0x4446087C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DATA_BIT4_TAP_SEL_NEG [7:4]				DATA_BIT4_TAP_SEL_POS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	DATA_BIT5_TAP_SEL_NEG [15:12]				DATA_BIT5_TAP_SEL_POS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	DATA_BIT6_TAP_SEL_NEG [23:20]				DATA_BIT6_TAP_SEL_POS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	DATA_BIT7_TAP_SEL_NEG [31:28]				DATA_BIT7_TAP_SEL_POS [27:24]			

Bits	Name	Description
31 : 28	DATA_BIT7_TAP_SEL_NEG	HB FW Calibration: Delay line tap select for spi_data[7], NEG Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
27 : 24	DATA_BIT7_TAP_SEL_POS	HB FW Calibration: Delay line tap select for spi_data[7], POS Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
23 : 20	DATA_BIT6_TAP_SEL_NEG	HB FW Calibration: Delay line tap select for spi_data[6], NEG Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
19 : 16	DATA_BIT6_TAP_SEL_POS	HB FW Calibration: Delay line tap select for spi_data[6], POS Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
15 : 12	DATA_BIT5_TAP_SEL_NEG	HBs FW Calibration: Delay line tap select for spi_data[5], NEG Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
11 : 8	DATA_BIT5_TAP_SEL_POS	HB FW Calibration: Delay line tap select for spi_data[5], POS Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0

22.1.135 SMIF0_CORE_DEVICE0_HB_FW_DEL_TAP_SEL_1 (continued)

7 : 4	DATA_BIT4_TAP_SEL_NEG	HB FW Calibration: Delay line tap select for spi_data[4], NEG Clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). See DATA_BIT0_TAP_SEL. Default Value: 0
3 : 0	DATA_BIT4_TAP_SEL_-POS	HB FW Calibration tap select for spi_data[4], POS clock Phase (note the mapping of spi_data to IO in DEVICE.CTL.DATA_SEL). Default Value: 0

22.1.136 SMIF0_CORE_SMIF_HSIOM_SMIF_PRT0_PORT_SEL0

Description: Port selection 0

Address: 0x44464000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [23:21]			IO2_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [31:29]			IO3_SEL [28:24]				

Bits	Name	Description
28 : 24	IO3_SEL	Selects connection for IO pin 3 route. Default Value: 0
20 : 16	IO2_SEL	Selects connection for IO pin 2 route. Default Value: 0
12 : 8	IO1_SEL	Selects connection for IO pin 1 route. Default Value: 0
4 : 0	IO0_SEL	Selects connection for IO pin 0 route. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable" **0x3: DSI_GPIO :** DSI controls "out", GPIO controls "output enable"

22.1.136 SMIF0_CORE_SMIF_HSIOM_SMIF_PRT0_PORT_SEL0 (continued)

0x4: AMUXA :

Analog mux bus A

0x5: AMUXB :

Analog mux bus B

0x6: AMUXA_DSI :

Analog mux bus A, DSI control

0x7: AMUXB_DSI :

Analog mux bus B, DSI control

0x8: ACT_0 :

Active functionality 0

0x9: ACT_1 :

Active functionality 1

0xa: ACT_2 :

Active functionality 2

0xb: ACT_3 :

Active functionality 3

0xc: DS_0 :

DeepSleep functionality 0

0xd: DS_1 :

DeepSleep functionality 1

0xe: DS_2 :

DeepSleep functionality 2

0xf: DS_3 :

DeepSleep functionality 3

0x10: ACT_4 :

Active functionality 4

0x11: ACT_5 :

Active functionality 5

22.1.136 SMIF0_CORE_SMIF_HSIOM_SMIF_PRT0_PORT_SEL0 (continued)

0x12: ACT_6 :

Active functionality 6

0x13: ACT_7 :

Active functionality 7

0x14: ACT_8 :

Active functionality 8

0x15: ACT_9 :

Active functionality 9

0x16: ACT_10 :

Active functionality 10

0x17: ACT_11 :

Active functionality 11

0x18: ACT_12 :

Active functionality 12

0x19: ACT_13 :

Active functionality 13

0x1a: ACT_14 :

Active functionality 14. Use this setting for AUX functionality (PRT0_PORT_SEL0 for DATA LSBs).

0x1b: ACT_15 :

Active functionality 15. Use this setting for SMIF functionality (PRT0_PORT_SEL0 for DATA LSBs, PRT1_PORT_SEL0 for CLK, PRT2_PORT_SEL0 for RWDS).

0x1c: DS_4 :

DeepSleep functionality 4

0x1d: DS_5 :

DeepSleep functionality 5

0x1e: DS_6 :

DeepSleep functionality 6

0x1f: DS_7 :

DeepSleep functionality 7

22.1.137 SMIF0_CORE_SMIF_HSIOM_SMIF_PRT0_PORT_SEL1

Description: Port selection 1

Address: 0x44464004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [23:21]			IO6_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [31:29]			IO7_SEL [28:24]				

Bits	Name	Description
28 : 24	IO7_SEL	Selects connection for IO pin 7 route. Default Value: 0
20 : 16	IO6_SEL	Selects connection for IO pin 6 route. Default Value: 0
12 : 8	IO5_SEL	Selects connection for IO pin 5 route. Default Value: 0
4 : 0	IO4_SEL	Selects connection for IO pin 4 route. See PORT_SEL0 for connection details. PRT0_PORT_SEL1 is used for DATA MSBs. Default Value: 0

22.1.138 SMIF0_CORE_SMIF_HSIOM_SMIF_PRT1_PORT_SEL0

Description: Port selection 0

Address: 0x44464010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12 : 8	IO1_SEL	Selects connection for IO pin 1 route. Default Value: 0
4 : 0	IO0_SEL	Selects connection for IO pin 0 route. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable" **0x3: DSI_GPIO :** DSI controls "out", GPIO controls "output enable" **0x4: AMUXA :** Analog mux bus A

22.1.138 SMIF0_CORE_SMIF_HSIOM_SMIF_PRT1_PORT_SEL0 (continued)

0x5: AMUXB :

Analog mux bus B

0x6: AMUXA_DSI :

Analog mux bus A, DSI control

0x7: AMUXB_DSI :

Analog mux bus B, DSI control

0x8: ACT_0 :

Active functionality 0

0x9: ACT_1 :

Active functionality 1

0xa: ACT_2 :

Active functionality 2

0xb: ACT_3 :

Active functionality 3

0xc: DS_0 :

DeepSleep functionality 0

0xd: DS_1 :

DeepSleep functionality 1

0xe: DS_2 :

DeepSleep functionality 2

0xf: DS_3 :

DeepSleep functionality 3

0x10: ACT_4 :

Active functionality 4

0x11: ACT_5 :

Active functionality 5

0x12: ACT_6 :

Active functionality 6

22.1.138 SMIF0_CORE_SMIF_HSIOM_SMIF_PRT1_PORT_SEL0 (continued)

0x13: ACT_7 :

Active functionality 7

0x14: ACT_8 :

Active functionality 8

0x15: ACT_9 :

Active functionality 9

0x16: ACT_10 :

Active functionality 10

0x17: ACT_11 :

Active functionality 11

0x18: ACT_12 :

Active functionality 12

0x19: ACT_13 :

Active functionality 13

0x1a: ACT_14 :

Active functionality 14. Use this setting for AUX functionality (PRT0_PORT_SEL0 for DATA LSBs).

0x1b: ACT_15 :

Active functionality 15. Use this setting for SMIF functionality (PRT0_PORT_SEL0 for DATA LSBs, PRT1_PORT_SEL0 for CLK, PRT2_PORT_SEL0 for RWDS).

0x1c: DS_4 :

DeepSleep functionality 4

0x1d: DS_5 :

DeepSleep functionality 5

0x1e: DS_6 :

DeepSleep functionality 6

0x1f: DS_7 :

DeepSleep functionality 7

22.1.139 SMIF0_CORE_SMIF_HSIOM_SMIF_PRT2_PORT_SEL0

Description: Port selection 0

Address: 0x44464020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			RW				
Name	Reserved [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	IO0_SEL	Selects connection for IO pin 0 route. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable" **0x3: DSI_GPIO :** DSI controls "out", GPIO controls "output enable" **0x4: AMUXA :** Analog mux bus A

22.1.139 SMIF0_CORE_SMIF_HSIOM_SMIF_PRT2_PORT_SEL0 (continued)

0x5: AMUXB :

Analog mux bus B

0x6: AMUXA_DSI :

Analog mux bus A, DSI control

0x7: AMUXB_DSI :

Analog mux bus B, DSI control

0x8: ACT_0 :

Active functionality 0

0x9: ACT_1 :

Active functionality 1

0xa: ACT_2 :

Active functionality 2

0xb: ACT_3 :

Active functionality 3

0xc: DS_0 :

DeepSleep functionality 0

0xd: DS_1 :

DeepSleep functionality 1

0xe: DS_2 :

DeepSleep functionality 2

0xf: DS_3 :

DeepSleep functionality 3

0x10: ACT_4 :

Active functionality 4

0x11: ACT_5 :

Active functionality 5

0x12: ACT_6 :

Active functionality 6

22.1.139 SMIF0_CORE_SMIF_HSIOM_SMIF_PRT2_PORT_SEL0 (continued)

0x13: ACT_7 :

Active functionality 7

0x14: ACT_8 :

Active functionality 8

0x15: ACT_9 :

Active functionality 9

0x16: ACT_10 :

Active functionality 10

0x17: ACT_11 :

Active functionality 11

0x18: ACT_12 :

Active functionality 12

0x19: ACT_13 :

Active functionality 13

0x1a: ACT_14 :

Active functionality 14. Use this setting for AUX functionality (PRT0_PORT_SEL0 for DATA LSBs).

0x1b: ACT_15 :

Active functionality 15. Use this setting for SMIF functionality (PRT0_PORT_SEL0 for DATA LSBs, PRT1_PORT_SEL0 for CLK, PRT2_PORT_SEL0 for RWDS).

0x1c: DS_4 :

DeepSleep functionality 4

0x1d: DS_5 :

DeepSleep functionality 5

0x1e: DS_6 :

DeepSleep functionality 6

0x1f: DS_7 :

DeepSleep functionality 7

22.1.140 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT

Description: Port output data register

Address: 0x44470000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

22.1.141 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_CLR

Description: Port output data clear register

Address: 0x44470004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO clear output for pin 7 Default Value: 0
6	OUT6	IO clear output for pin 6 Default Value: 0
5	OUT5	IO clear output for pin 5 Default Value: 0
4	OUT4	IO clear output for pin 4 Default Value: 0
3	OUT3	IO clear output for pin 3 Default Value: 0
2	OUT2	IO clear output for pin 2 Default Value: 0
1	OUT1	IO clear output for pin 1 Default Value: 0
0	OUT0	IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. Default Value: 0

22.1.142 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_SET

Description: Port output data set register

Address: 0x44470008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO set output for pin 7 Default Value: 0
6	OUT6	IO set output for pin 6 Default Value: 0
5	OUT5	IO set output for pin 5 Default Value: 0
4	OUT4	IO set output for pin 4 Default Value: 0
3	OUT3	IO set output for pin 3 Default Value: 0
2	OUT2	IO set output for pin 2 Default Value: 0
1	OUT1	IO set output for pin 1 Default Value: 0
0	OUT0	IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. Default Value: 0

22.1.143 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_OUT_INV

Description: Port output data invert register

Address: 0x4447000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	OUT7	IO invert output for pin 7 Default Value: 0
6	OUT6	IO invert output for pin 6 Default Value: 0
5	OUT5	IO invert output for pin 5 Default Value: 0
4	OUT4	IO invert output for pin 4 Default Value: 0
3	OUT3	IO invert output for pin 3 Default Value: 0
2	OUT2	IO invert output for pin 2 Default Value: 0
1	OUT1	IO invert output for pin 1 Default Value: 0
0	OUT0	IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). Default Value: 0

22.1.144 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_IN

Description: Port input state register

Address: 0x44470010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
6	IN6	IO pin state for pin 6 Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

22.1.145 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR

Description: Port interrupt status register

Address: 0x44470014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN_IN7	IN_IN6	IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
22	IN_IN6	IO pin state for pin 6 Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detect for IO pin 7 Default Value: 0

22.1.145 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR (continued)

6	EDGE6	Edge detect for IO pin 6 Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

22.1.146 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_MASK

Description: Port interrupt mask register

Address: 0x44470018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
6	EDGE6	Masks edge interrupt on IO pin 6 Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

22.1.147 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_MASKED

Description: Port interrupt masked status register

Address: 0x4447001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
6	EDGE6	Edge detected and masked on IO pin 6 Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

22.1.148 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_SET

Description: Port interrupt set register

Address: 0x44470020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
6	EDGE6	Sets edge detect interrupt for IO pin 6 Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

22.1.149 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_CFG

Description: Port interrupt configuration register

Address: 0x44470040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW			RW	
HW Access	Reserved			R			R	
Name	Reserved [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pin 6 Default Value: 0

22.1.149 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_INTR_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

22.1.150 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG

Description: Port configuration register

Address: 0x44470044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6 Default Value: 0
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0

22.1.150 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG (continued)

10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: CFG3_EN :** Enables CFG3.Bit 0 to control Port Pin 0. **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

22.1.150 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG (continued)

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up
Use this setting in PRT0_CFG for DATA. for SMIF functionality

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down
Use this setting in PRT2_CFG for RWDS for SMIF functionality.

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

22.1.150 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG (continued)

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance
Use this setting in PRT1_CFG for CLK for SMIF functionality.

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

22.1.151 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_IN

Description: Port input buffer configuration register

Address: 0x44470048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VTRIP_-SEL7_0	VTRIP_-SEL6_0	VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
6	VTRIP_SEL6_0	Configures the pin 6 input buffer mode (trip points and hysteresis) Default Value: 0
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** Input buffer compatible with CMOS and I2C interfaces

22.1.151 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_IN (continued)

0x1: TTL :

Input buffer compatible with TTL and MediaLB interfaces

22.1.152 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_OUT

Description: Port output buffer configuration register

Address: 0x4447004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 Default Value: 0
		0x0: DRIVE_SEL_ZERO :
		0x1: DRIVE_SEL_ONE :
		0x2: DRIVE_SEL_TWO :

22.1.152 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_OUT (continued)

0x3: DRIVE_SEL_THREE :

22.1.153 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_SLEW_EXT

Description: Port output buffer slew extension configuration register

Address: 0x44470064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [7:5]			SLEW1	Reserved [3:1]			SLEW0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			SLEW3	Reserved [11:9]			SLEW2

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [23:21]			SLEW5	Reserved [19:17]			SLEW4

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [31:29]			SLEW7	Reserved [27:25]			SLEW6

Bits	Name	Description
28	SLEW7	Slew rate for IO pin 7 Default Value: 0
24	SLEW6	Slew rate for IO pin 6 Default Value: 0
20	SLEW5	Slew rate for IO pin 5 Default Value: 0
16	SLEW4	Slew rate for IO pin 4 Default Value: 0
12	SLEW3	Slew rate for IO pin 3 Default Value: 0
8	SLEW2	Slew rate for IO pin 2 Default Value: 0
4	SLEW1	Slew rate for IO pin 1 Default Value: 0
0	SLEW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

22.1.154 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT0

Description: Port output buffer drive sel extension configuration register

Address: 0x44470068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					DRIVE_SEL_EXT0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [15:11]					DRIVE_SEL_EXT1 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					DRIVE_SEL_EXT2 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					DRIVE_SEL_EXT3 [26:24]		

Bits	Name	Description
26 : 24	DRIVE_SEL_EXT3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
18 : 16	DRIVE_SEL_EXT2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
10 : 8	DRIVE_SEL_EXT1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
2 : 0	DRIVE_SEL_EXT0	Sets the GPIO drive strength for IO pin 0 Default Value: 0

22.1.155 SMIF0_CORE_SMIF_GPIO_SMIF_PRT0_CFG_DRIVE_EXT1

Description: Port output buffer drive sel extension configuration register

Address: 0x4447006C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					DRIVE_SEL_EXT4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [15:11]					DRIVE_SEL_EXT5 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [23:19]					DRIVE_SEL_EXT6 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					DRIVE_SEL_EXT7 [26:24]		

Bits	Name	Description
26 : 24	DRIVE_SEL_EXT7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
18 : 16	DRIVE_SEL_EXT6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
10 : 8	DRIVE_SEL_EXT5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
2 : 0	DRIVE_SEL_EXT4	Sets the GPIO drive strength for IO pin 4 Default Value: 0

22.1.156 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_OUT

Description: Port output data register

Address: 0x44470080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						RW	RW
Name	Reserved [7:2]						OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

22.1.157 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_IN

Description: Port input state register

Address: 0x44470090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

22.1.158 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR

Description: Port interrupt status register

Address: 0x44470094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1C	RW1C
HW Access	Reserved						A	A
Name	Reserved [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [23:18]						IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

22.1.159 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_MASK

Description: Port interrupt mask register

Address: 0x44470098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

22.1.160 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_MASKED

Description: Port interrupt masked status register

Address: 0x4447009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

22.1.161 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_SET

Description: Port interrupt set register

Address: 0x444700A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1S	RW1S
HW Access	Reserved						A	A
Name	Reserved [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

22.1.162 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_CFG

Description: Port interrupt configuration register

Address: 0x444700C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW		RW	
HW Access	Reserved				R		R	
Name	Reserved [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW			RW	
HW Access	Reserved			R			R	
Name	Reserved [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0

22.1.162 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_INTR_CFG (continued)

0x0: DISABLE :

Disabled

0x1: RISING :

Rising edge

0x2: FALLING :

Falling edge

0x3: BOTH :

Both rising and falling edges

22.1.163 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG

Description: Port configuration register

Address: 0x444700C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: CFG3_EN :** Enables CFG3.Bit 0 to control Port Pin 0.

22.1.163 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG (continued)

0x1: RESERVED :

This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases.
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up
Use this setting in PRT0_CFG for DATA. for SMIF functionality

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down
Use this setting in PRT2_CFG for RWDS for SMIF functionality.

22.1.163 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG (continued)

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance
Use this setting in PRT1_CFG for CLK for SMIF functionality.

22.1.163 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG (continued)

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

22.1.164 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG_IN

Description: Port input buffer configuration register

Address: 0x444700C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** Input buffer compatible with CMOS and I2C interfaces **0x1: TTL :** Input buffer compatible with TTL and MediaLB interfaces

22.1.165 SMIF0_CORE_SMIF_GPIO_SMIF_PRT1_CFG_OUT

Description: Port output buffer configuration register

Address: 0x444700CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW		RW	
HW Access	Reserved				R		R	
Name	Reserved [23:20]				DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 Default Value: 0
		0x0: DRIVE_SEL_ZERO :
		0x1: DRIVE_SEL_ONE :
		0x2: DRIVE_SEL_TWO :
		0x3: DRIVE_SEL_THREE :

22.1.166 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_OUT

Description: Port output data register

Address: 0x44470100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							RW
Name	Reserved [7:1]							OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

22.1.167 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_IN

Description: Port input state register

Address: 0x44470110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							IN0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

22.1.168 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR

Description: Port interrupt status register

Address: 0x44470114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [7:1]							EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [23:17]							IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

22.1.169 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR_MASK

Description: Port interrupt mask register

Address: 0x44470118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

22.1.170 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR_MASKED

Description: Port interrupt masked status register

Address: 0x4447011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

22.1.171 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR_SET

Description: Port interrupt set register

Address: 0x44470120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

22.1.172 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR_CFG

Description: Port interrupt configuration register

Address: 0x44470140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW			RW	
HW Access	Reserved			R			R	
Name	Reserved [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0

22.1.172 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_INTR_CFG (continued)

0x0: DISABLE :

Disabled

0x1: RISING :

Rising edge

0x2: FALLING :

Falling edge

0x3: BOTH :

Both rising and falling edges

22.1.173 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG

Description: Port configuration register

Address: 0x44470144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW		
HW Access	Reserved				R	R		
Name	Reserved [7:4]				IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: CFG3_EN :** Enables CFG3.Bit 0 to control Port Pin 0.

22.1.173 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG (continued)

0x1: RESERVED :

This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases.
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up
Use this setting in PRT0_CFG for DATA. for SMIF functionality

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down
Use this setting in PRT2_CFG for RWDS for SMIF functionality.

22.1.173 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG (continued)

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance
Use this setting in PRT1_CFG for CLK for SMIF functionality.

22.1.173 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG (continued)

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

22.1.174 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG_IN

Description: Port input buffer configuration register

Address: 0x44470148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** Input buffer compatible with CMOS and I2C interfaces **0x1: TTL :** Input buffer compatible with TTL and MediaLB interfaces

22.1.175 SMIF0_CORE_SMIF_GPIO_SMIF_PRT2_CFG_OUT

Description: Port output buffer configuration register

Address: 0x4447014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [23:18]						DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 Default Value: 0 **0x0: DRIVE_SEL_ZERO :** **0x1: DRIVE_SEL_ONE :** **0x2: DRIVE_SEL_TWO :** **0x3: DRIVE_SEL_THREE :**

22.1.176 SMIF0_CORE_SMIF_GPIO_INTR_CAUSE00

Description: Interrupt port cause register 0

Address: 0x44478000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	
HW Access	Reserved						W	
Name	Reserved [7:3]						PORT_INT [2:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a combined interrupt line "gpio_interrupt". The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PRT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt. '0': Port has no pending interrupt '1': Port has pending interrupt Default Value: 0

22.1.177 SMIF0_CORE_SMIF_GPIO_VDD_ACTIVE

Description: Extern power supply detection register

Address: 0x44478010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	Reserved					
HW Access	W	W	Reserved					
Name	VDDD_ACTIVE	VDDA_ACTIVE	Reserved [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	This bit indicates presence of the VDDD supply. This bit will always read-back 1. The VDDD supply has robust brown-out protection monitoring and it is not possible to read back this register without a valid supply. (This bit is used in certain test-modes to observe the brown-out detector status.) Default Value: 1
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0

22.1.178 SMIF0_CORE_SMIF_GPIO_VDD_INTR

Description: Supply detection interrupt register

Address: 0x44478014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	RW1C	Reserved					
HW Access	A	A	Reserved					
Name	VDDD_ACTIVE	VDDA_ACTIVE	Reserved [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	The VDDD supply is always present during operation so a supply transition can not occur. This bit will always read back '1'. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0

22.1.179 SMIF0_CORE_SMIF_GPIO_VDD_INTR_MASK

Description: Supply detection interrupt mask register

Address: 0x44478018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved					
HW Access	R	R	Reserved					
Name	VDDD_ACTIVE	VDDA_ACTIVE	Reserved [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0

22.1.180 SMIF0_CORE_SMIF_GPIO_VDD_INTR_MASKED

Description: Supply detection interrupt masked register

Address: 0x4447801C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	Reserved					
HW Access	W	W	Reserved					
Name	VDDD_ACTIVE	VDDA_ACTIVE	Reserved [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0

22.1.181 SMIF0_CORE_SMIF_GPIO_VDD_INTR_SET

Description: Supply detection interrupt set register

Address: 0x44478020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW1S	Reserved					
HW Access	A	A	Reserved					
Name	VDDD_ACTIVE	VDDA_ACTIVE	Reserved [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0

23 Secure Digital Host Controller (SDHC) registers

This section discusses the SDHC registers. It lists all the registers in mapping tables, in address order.

23.1 Register details

Register name	Address	Description
SDHC0_WRAP_CTL	0x44810000	Top level wrapper control
SDHC0_CORE_SDMASA_R	0x44811000	SDMA System Address register
SDHC0_CORE_BLOCKSIZE_R	0x44811004	Block Size register
SDHC0_CORE_BLOCKCOUNT_R	0x44811006	16-bit Block Count register
SDHC0_CORE_ARGUMENT_R	0x44811008	Argument register
SDHC0_CORE_XFER_MODE_R	0x4481100C	Transfer Mode register
SDHC0_CORE_CMD_R	0x4481100E	Command register
SDHC0_CORE_RESP01_R	0x44811010	Response Register 0/1
SDHC0_CORE_RESP23_R	0x44811014	Response Register 2/3
SDHC0_CORE_RESP45_R	0x44811018	Response Register 4/5
SDHC0_CORE_RESP67_R	0x4481101C	Response Register 6/7
SDHC0_CORE_BUF_DATA_R	0x44811020	Buffer Data Port Register
SDHC0_CORE_PSTATE_REG	0x44811024	Present State Register
SDHC0_CORE_HOST_CTRL1_R	0x44811028	Host Control 1 Register
SDHC0_CORE_PWR_CTRL_R	0x44811029	Power Control Register
SDHC0_CORE_BGAP_CTRL_R	0x4481102A	Block Gap Control Register
SDHC0_CORE_WUP_CTRL_R	0x4481102B	Wakeup Control Register
SDHC0_CORE_CLK_CTRL_R	0x4481102C	Clock Control Register
SDHC0_CORE_TOUT_CTRL_R	0x4481102E	Timeout Control Register
SDHC0_CORE_SW_RST_R	0x4481102F	Software Reset Register
SDHC0_CORE_NORMAL_INT_STAT_R	0x44811030	Normal Interrupt Status Register
SDHC0_CORE_ERROR_INT_STAT_R	0x44811032	Error Interrupt Status Register
SDHC0_CORE_NORMAL_INT_STAT_EN_R	0x44811034	Normal Interrupt Status Enable Register
SDHC0_CORE_ERROR_INT_STAT_EN_R	0x44811036	Error Interrupt Status Enable Register
SDHC0_CORE_NORMAL_INT_SIGNAL_EN_R	0x44811038	Normal Interrupt Signal Enable Register
SDHC0_CORE_ERROR_INT_SIGNAL_EN_R	0x4481103A	Error Interrupt Signal Enable Register
SDHC0_CORE_AUTO_CMD_STAT_R	0x4481103C	Auto CMD Status Register
SDHC0_CORE_HOST_CTRL2_R	0x4481103E	Host Control 2 Register
SDHC0_CORE_CAPABILITIES1_R	0x44811040	Capabilities 1 Register - 0 to 31

Secure Digital Host Controller (SDHC) registers

Register name	Address	Description
SDHC0_CORE_CAPABILITIES2_R	0x44811044	Capabilities Register - 32 to 63
SDHC0_CORE_CURR_CAPABILITIES1_R	0x44811048	Current Capabilities Register - 0 to 31
SDHC0_CORE_CURR_CAPABILITIES2_R	0x4481104C	Maximum Current Capabilities Register - 32 to 63
SDHC0_CORE_FORCE_AUTO_CMD_STAT_R	0x44811050	Force Event Register for Auto CMD Error Status register
SDHC0_CORE_FORCE_ERROR_INT_STAT_R	0x44811052	Force Event Register for Error Interrupt Status
SDHC0_CORE_ADMA_ERR_STAT_R	0x44811054	ADMA Error Status Register
SDHC0_CORE_ADMA_SA_LOW_R	0x44811058	ADMA System Address Register - Low
SDHC0_CORE_ADMA_ID_LOW_R	0x44811078	ADMA3 Integrated Descriptor Address Register - Low
SDHC0_CORE_HOST_CNTRL_VERS_R	0x448110FE	Host Controller Version
SDHC0_CORE_CQVER	0x44811180	Command Queuing Version register
SDHC0_CORE_CQCAP	0x44811184	Command Queuing Capabilities register
SDHC0_CORE_CQCFG	0x44811188	Command Queuing Configuration register
SDHC0_CORE_CQCTL	0x4481118C	Command Queuing Control register
SDHC0_CORE_CQIS	0x44811190	Command Queuing Interrupt Status register
SDHC0_CORE_CQISE	0x44811194	Command Queuing Interrupt Status Enable register
SDHC0_CORE_CQISGE	0x44811198	Command Queuing Interrupt signal enable register
SDHC0_CORE_CQIC	0x4481119C	Command Queuing Interrupt Coalescing register
SDHC0_CORE_CQTDLBA	0x448111A0	Command Queuing Task Descriptor List Base Address register
SDHC0_CORE_CQTDBR	0x448111A8	Command Queuing DoorBell register
SDHC0_CORE_CQTCN	0x448111AC	Command Queuing TaskClear Notification register
SDHC0_CORE_CQDQS	0x448111B0	Device queue status register
SDHC0_CORE_CQDPT	0x448111B4	Device pending tasks register
SDHC0_CORE_CQTCLR	0x448111B8	Command Queuing DoorBell register
SDHC0_CORE_CQSSC1	0x448111C0	CQ Send Status Configuration 1 register
SDHC0_CORE_CQSSC2	0x448111C4	CQ Send Status Configuration 2 register
SDHC0_CORE_CQCRDCT	0x448111C8	Command response for direct command register
SDHC0_CORE_CQRMEM	0x448111D0	Command response mode error mask register
SDHC0_CORE_CQTERRI	0x448111D4	CQ Task Error Information register
SDHC0_CORE_CQCRI	0x448111D8	CQ Command response index
SDHC0_CORE_CQCRA	0x448111DC	CQ Command response argument register
SDHC0_CORE_MSHC_VER_ID_R	0x44811500	MSHC version
SDHC0_CORE_MSHC_VER_TYPE_R	0x44811504	MSHC version type
SDHC0_CORE_MSHC_CTRL_R	0x44811508	MSHC Control register
SDHC0_CORE_MBIU_CTRL_R	0x44811510	MBIU Control register

Secure Digital Host Controller (SDHC) registers

Register name	Address	Description
SDHC0_CORE_EMMC_CTRL_R	0x4481152C	eMMC Control register
SDHC0_CORE_BOOT_CTRL_R	0x4481152E	eMMC Boot Control register
SDHC0_CORE_GP_IN_R	0x44811530	General Purpose Input register
SDHC0_CORE_GP_OUT_R	0x44811534	General Purpose Output register
SDHC1_WRAP_CTL	0x44820000	Top level wrapper control. See SDHC0_WRAP_CTL for the details of bit fields.
SDHC1_CORE_SDMASA_R	0x44821000	SDMA System Address register. See SDHC0_CORE_SDMASA_R for the details of bit fields.
SDHC1_CORE_BLOCKSIZE_R	0x44821004	Block Size register. See SDHC0_CORE_BLOCKSIZE_R for the details of bit fields.
SDHC1_CORE_BLOCKCOUNT_R	0x44821006	16-bit Block Count register. See SDHC0_CORE_BLOCKCOUNT_R for the details of bit fields.
SDHC1_CORE_ARGUMENT_R	0x44821008	Argument register. See SDHC0_CORE_ARGUMENT_R for the details of bit fields.
SDHC1_CORE_XFER_MODE_R	0x4482100C	Transfer Mode register. See SDHC0_CORE_XFER_MODE_R for the details of bit fields.
SDHC1_CORE_CMD_R	0x4482100E	Command register. See SDHC0_CORE_CMD_R for the details of bit fields.
SDHC1_CORE_RESP01_R	0x44821010	Response Register 0/1. See SDHC0_CORE_RESP01_R for the details of bit fields.
SDHC1_CORE_RESP23_R	0x44821014	Response Register 2/3. See SDHC0_CORE_RESP23_R for the details of bit fields.
SDHC1_CORE_RESP45_R	0x44821018	Response Register 4/5. See SDHC0_CORE_RESP45_R for the details of bit fields.
SDHC1_CORE_RESP67_R	0x4482101C	Response Register 6/7. See SDHC0_CORE_RESP67_R for the details of bit fields.
SDHC1_CORE_BUF_DATA_R	0x44821020	Buffer Data Port Register. See SDHC0_CORE_BUF_DATA_R for the details of bit fields.
SDHC1_CORE_PSTATE_REG	0x44821024	Present State Register. See SDHC0_CORE_PSTATE_REG for the details of bit fields.
SDHC1_CORE_HOST_CTRL1_R	0x44821028	Host Control 1 Register. See SDHC0_CORE_HOST_CTRL1_R for the details of bit fields.
SDHC1_CORE_PWR_CTRL_R	0x44821029	Power Control Register. See SDHC0_CORE_PWR_CTRL_R for the details of bit fields.
SDHC1_CORE_BGAP_CTRL_R	0x4482102A	Block Gap Control Register. See SDHC0_CORE_BGAP_CTRL_R for the details of bit fields.
SDHC1_CORE_WUP_CTRL_R	0x4482102B	Wakeup Control Register. See SDHC0_CORE_WUP_CTRL_R for the details of bit fields.
SDHC1_CORE_CLK_CTRL_R	0x4482102C	Clock Control Register. See SDHC0_CORE_CLK_CTRL_R for the details of bit fields.

Secure Digital Host Controller (SDHC) registers

Register name	Address	Description
SDHC1_CORE_TOUT_CTRL_R	0x4482102E	Timeout Control Register. See SDHC0_CORE_TOUT_CTRL_R for the details of bit fields.
SDHC1_CORE_SW_RST_R	0x4482102F	Software Reset Register. See SDHC0_CORE_SW_RST_R for the details of bit fields.
SDHC1_CORE_NORMAL_INT_STAT_R	0x44821030	Normal Interrupt Status Register. See SDHC0_CORE_NORMAL_INT_STAT_R for the details of bit fields.
SDHC1_CORE_ERROR_INT_STAT_R	0x44821032	Error Interrupt Status Register. See SDHC0_CORE_ERROR_INT_STAT_R for the details of bit fields.
SDHC1_CORE_NORMAL_INT_STAT_EN_R	0x44821034	Normal Interrupt Status Enable Register. See SDHC0_CORE_NORMAL_INT_STAT_EN_R for the details of bit fields.
SDHC1_CORE_ERROR_INT_STAT_EN_R	0x44821036	Error Interrupt Status Enable Register. See SDHC0_CORE_ERROR_INT_STAT_EN_R for the details of bit fields.
SDHC1_CORE_NORMAL_INT_SIGNAL_EN_R	0x44821038	Normal Interrupt Signal Enable Register. See SDHC0_CORE_NORMAL_INT_SIGNAL_EN_R for the details of bit fields.
SDHC1_CORE_ERROR_INT_SIGNAL_EN_R	0x4482103A	Error Interrupt Signal Enable Register. See SDHC0_CORE_ERROR_INT_SIGNAL_EN_R for the details of bit fields.
SDHC1_CORE_AUTO_CMD_STAT_R	0x4482103C	Auto CMD Status Register. See SDHC0_CORE_AUTO_CMD_STAT_R for the details of bit fields.
SDHC1_CORE_HOST_CTRL2_R	0x4482103E	Host Control 2 Register. See SDHC0_CORE_HOST_CTRL2_R for the details of bit fields.
SDHC1_CORE_CAPABILITIES1_R	0x44821040	Capabilities 1 Register - 0 to 31. See SDHC0_CORE_CAPABILITIES1_R for the details of bit fields.
SDHC1_CORE_CAPABILITIES2_R	0x44821044	Capabilities Register - 32 to 63. See SDHC0_CORE_CAPABILITIES2_R for the details of bit fields.
SDHC1_CORE_CURR_CAPABILITIES1_R	0x44821048	Current Capabilities Register - 0 to 31. See SDHC0_CORE_CURR_CAPABILITIES1_R for the details of bit fields.
SDHC1_CORE_CURR_CAPABILITIES2_R	0x4482104C	Maximum Current Capabilities Register - 32 to 63. See SDHC0_CORE_CURR_CAPABILITIES2_R for the details of bit fields.
SDHC1_CORE_FORCE_AUTO_CMD_STAT_R	0x44821050	Force Event Register for Auto CMD Error Status register. See SDHC0_CORE_FORCE_AUTO_CMD_STAT_R for the details of bit fields.

Secure Digital Host Controller (SDHC) registers

Register name	Address	Description
SDHC1_CORE_FORCE_ERROR_INT_STAT_R	0x44821052	Force Event Register for Error Interrupt Status. See SDHC0_CORE_FORCE_ERROR_INT_STAT_R for the details of bit fields.
SDHC1_CORE_ADMA_ERR_STAT_R	0x44821054	ADMA Error Status Register. See SDHC0_CORE_ADMA_ERR_STAT_R for the details of bit fields.
SDHC1_CORE_ADMA_SA_LOW_R	0x44821058	ADMA System Address Register - Low. See SDHC0_CORE_ADMA_SA_LOW_R for the details of bit fields.
SDHC1_CORE_ADMA_ID_LOW_R	0x44821078	ADMA3 Integrated Descriptor Address Register - Low. See SDHC0_CORE_ADMA_ID_LOW_R for the details of bit fields.
SDHC1_CORE_HOST_CNTRL_VERS_R	0x448210FE	Host Controller Version. See SDHC0_CORE_HOST_CNTRL_VERS_R for the details of bit fields.
SDHC1_CORE_CQVER	0x44821180	Command Queuing Version register. See SDHC0_CORE_CQVER for the details of bit fields.
SDHC1_CORE_CQCAP	0x44821184	Command Queuing Capabilities register. See SDHC0_CORE_CQCAP for the details of bit fields.
SDHC1_CORE_CQCFG	0x44821188	Command Queuing Configuration register. See SDHC0_CORE_CQCFG for the details of bit fields.
SDHC1_CORE_CQCTL	0x4482118C	Command Queuing Control register. See SDHC0_CORE_CQCTL for the details of bit fields.
SDHC1_CORE_CQIS	0x44821190	Command Queuing Interrupt Status register. See SDHC0_CORE_CQIS for the details of bit fields.
SDHC1_CORE_CQISE	0x44821194	Command Queuing Interrupt Status Enable register. See SDHC0_CORE_CQISE for the details of bit fields.
SDHC1_CORE_CQISGE	0x44821198	Command Queuing Interrupt signal enable register. See SDHC0_CORE_CQISGE for the details of bit fields.
SDHC1_CORE_CQIC	0x4482119C	Command Queuing Interrupt Coalescing register. See SDHC0_CORE_CQIC for the details of bit fields.
SDHC1_CORE_CQTDLBA	0x448211A0	Command Queuing Task Descriptor List Base Address register. See SDHC0_CORE_CQTDLBA for the details of bit fields.
SDHC1_CORE_CQTDBR	0x448211A8	Command Queuing DoorBell register. See SDHC0_CORE_CQTDBR for the details of bit fields.
SDHC1_CORE_CQTCN	0x448211AC	Command Queuing TaskClear Notification register. See SDHC0_CORE_CQTCN for the details of bit fields.
SDHC1_CORE_CQDQS	0x448211B0	Device queue status register. See SDHC0_CORE_CQDQS for the details of bit fields.
SDHC1_CORE_CQDPT	0x448211B4	Device pending tasks register. See SDHC0_CORE_CQDPT for the details of bit fields.
SDHC1_CORE_CQTCLR	0x448211B8	Command Queuing DoorBell register. See SDHC0_CORE_CQTCLR for the details of bit fields.

Secure Digital Host Controller (SDHC) registers

Register name	Address	Description
SDHC1_CORE_CQSSC1	0x448211C0	CQ Send Status Configuration 1 register. See SDHC0_CORE_CQSSC1 for the details of bit fields.
SDHC1_CORE_CQSSC2	0x448211C4	CQ Send Status Configuration 2 register. See SDHC0_CORE_CQSSC2 for the details of bit fields.
SDHC1_CORE_CQCRDCT	0x448211C8	Command response for direct command register. See SDHC0_CORE_CQCRDCT for the details of bit fields.
SDHC1_CORE_CQRMEM	0x448211D0	Command response mode error mask register. See SDHC0_CORE_CQRMEM for the details of bit fields.
SDHC1_CORE_CQTERRI	0x448211D4	CQ Task Error Information register. See SDHC0_CORE_CQTERRI for the details of bit fields.
SDHC1_CORE_CQCRI	0x448211D8	CQ Command response index. See SDHC0_CORE_CQCRI for the details of bit fields.
SDHC1_CORE_CQCRA	0x448211DC	CQ Command response argument register. See SDHC0_CORE_CQCRA for the details of bit fields.
SDHC1_CORE_MSHC_VER_ID_R	0x44821500	MSHC version. See SDHC0_CORE_MSHC_VER_ID_R for the details of bit fields.
SDHC1_CORE_MSHC_VER_TYPE_R	0x44821504	MSHC version type. See SDHC0_CORE_MSHC_VER_TYPE_R for the details of bit fields.
SDHC1_CORE_MSHC_CTRL_R	0x44821508	MSHC Control register. See SDHC0_CORE_MSHC_CTRL_R for the details of bit fields.
SDHC1_CORE_MBIU_CTRL_R	0x44821510	MBIU Control register. See SDHC0_CORE_MBIU_CTRL_R for the details of bit fields.
SDHC1_CORE_EMMC_CTRL_R	0x4482152C	eMMC Control register. See SDHC0_CORE_EMMC_CTRL_R for the details of bit fields.
SDHC1_CORE_BOOT_CTRL_R	0x4482152E	eMMC Boot Control register. See SDHC0_CORE_BOOT_CTRL_R for the details of bit fields.
SDHC1_CORE_GP_IN_R	0x44821530	General Purpose Input register. See SDHC0_CORE_GP_IN_R for the details of bit fields.
SDHC1_CORE_GP_OUT_R	0x44821534	General Purpose Output register. See SDHC0_CORE_GP_OUT_R for the details of bit fields.

23.1.1 SDHC0_WRAP_CTL

Description: Top level wrapper control

Address: 0x44810000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLE	Reserved [30:24]						

Bits	Name	Description
31	ENABLE	IP Enable: 0: IP disabled, RAM in DeepSleep, SDHC_CORE regs are inaccessible (any attempts to access will result in AHB Error responses), IP is NOT held in reset but the clocks are gated 1: IP enabled, normal operation Default Value: 0

23.1.2 SDHC0_CORE_SDMASA_R

Description: SDMA System Address register

Address: 0x44811000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BLOCKCNT_SDMASA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	BLOCKCNT_SDMASA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	BLOCKCNT_SDMASA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	BLOCKCNT_SDMASA [31:24]							

Bits	Name	Description

23.1.2 SDHC0_CORE_SDMASA_R (continued)

31 : 0	BLOCKCNT_SDMASA	32-bit Block Count (SDMA System Address) - SDMA System Address (Host Version 4 Enable = 0): This register contains the system memory address for an SDMA transfer in the 32-bit addressing mode. When the Host Controller stops an SDMA transfer, this register points to the system address of the next contiguous data position. It can be accessed only if no transaction is executing. Reading this register during data transfers may return an invalid value. - 32-bit Block Count (Host Version 4 Enable = 1): From the Host Controller Version 4.10 specification, this register is redefined as 32-bit Block Count. The Host Controller decrements the block count of this register for every block transfer and the data transfer stops when the count reaches zero. This register must be accessed when no transaction is executing. Reading this register during data transfers may return invalid value. Following are the values for BLOCKCNT_SDMASA: - 0xFFFF_FFFF - 4G - 1 Block - ..... - 0x0000_0002 - 2 Blocks - 0x0000_0001 - 1 Block - 0x0000_0000 - Stop Count Note: - When Host Version 4 Enable = 0, SDMA uses this register as system address and hence Auto CMD23 cannot be used with SDMA since this register is assigned for Auto CMD23 as 32-bit Block Count register. -When Host Version 4 Enable = 1, SDMA uses ADMA system address register and this register is reassigned to 32-bit Block Count. This register must be programmed with a non-zero value for data transfer if the 32-bit Block count register is used instead of the 16-bit Block count register. SDMA may use Auto CMD23 if 32-bit Block Count register is used. Default Value: 0

23.1.3 SDHC0_CORE_BLOCKSIZE_R

Description: Block Size register

Address: 0x44811004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	XFER_BLOCK_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW			RW			
HW Access	Reserved	R			R			
Name	Reserved	SDMA_BUF_BDARY [14:12]			XFER_BLOCK_SIZE [11:8]			

Bits	Name	Description
14 : 12	SDMA_BUF_BDARY	SDMA Buffer Boundary These bits specify the size of contiguous buffer in system memory. The SDMA transfer waits at every boundary specified by these fields and the Host Controller generates the DMA interrupt to request the Host Driver to update the SDMA System Address register. Values: - 0x0 (BYTES_4K): 4K bytes SDMA Buffer Boundary - 0x1 (BYTES_8K): 8K bytes SDMA Buffer Boundary - 0x2 (BYTES_16K): 16K bytes SDMA Buffer Boundary - 0x3 (BYTES_32K): 32K bytes SDMA Buffer Boundary - 0x4 (BYTES_64K): 64K bytes SDMA Buffer Boundary - 0x5 (BYTES_128K): 128K bytes SDMA Buffer Boundary - 0x6 (BYTES_256K): 256K bytes SDMA Buffer Boundary - 0x7 (BYTES_512K): 512K bytes SDMA Buffer Boundary Default Value: 0
11 : 0	XFER_BLOCK_SIZE	Transfer Block Size These bits specify the block size of data transfers. In case of memory, it is set to 512 bytes. It can be accessed only if no transaction is executing. Read operations during transfers may return an invalid value, and write operations are ignored. Following are the values for XFER_BLOCK_SIZE: - 0x1: 1 byte - 0x2: 2 bytes - 0x3: 3 bytes - ..... - 0x1FF: 511 byte - 0x200: 512 bytes - ..... - 0x800: 2048 bytes Note: This register must be programmed with a non-zero value for data transfer. Default Value: 0

23.1.4 SDHC0_CORE_BLOCKCOUNT_R

Description: 16-bit Block Count register

Address: 0x44811006

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BLOCK_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	BLOCK_CNT [15:8]							

Bits	Name	Description
15 : 0	BLOCK_CNT	16-bit Block Count - If the Host Version 4 Enable bit is set 0 or the 16-bit Block Count register is set to non-zero, the 16-bit Block Count register is selected. - If the Host Version 4 Enable bit is set 1 and the 16-bit Block Count register is set to zero, the 32-bit Block Count register is selected. Following are the values for BLOCK_CNT: - 0x0: Stop Count - 0x1: 1 Block - 0x2: 2 Blocks - ... - ... - 0xFFFF: 65535 Blocks Note: For Host Version 4 Enable = 0, this register must be set to 0000h before programming the 32-bit block count register when Auto CMD23 is enabled for non-DMA and ADMA modes. Default Value: 0

23.1.5 SDHC0_CORE_ARGUMENT_R

Description: Argument register

Address: 0x44811008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ARGUMENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ARGUMENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ARGUMENT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ARGUMENT [31:24]							

Bits	Name	Description
31 : 0	ARGUMENT	Command Argument These bits specify the SD/eMMC command argument that is specified in bits 39-8 of the Command format. Default Value: 0

23.1.6 SDHC0_CORE_XFER_MODE_R

Description: Transfer Mode register

Address: 0x4481100C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	RW
HW Access	R	R	R	R	R		R	R
Name	RESP_ER-R_CH-K_ENABLE	RESP_-TYPE	MUL-TI_BLK_-SEL	DATA_X-FER_DIR	AUTO_CMD_ENABLE [3:2]		BLOCK_CO UNT_EN-ABLE	DMA_EN-ABLE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							RE-SP_INT_-DISABLE

Bits	Name	Description
8	RESP_INT_DISABLE	Response Interrupt Disable The Host Controller supports response check function to avoid overhead of response error check by the Host driver. Response types of only R1 and R5 can be checked by the Controller. If Host Driver checks the response error, set this bit to 0 and wait for Command Complete Interrupt and then check the response register. If the Host Controller checks the response error, set this bit to 1 and set the Response Error Check Enable bit to 1. The Command Complete Interrupt is disabled by this bit regardless of the Command Complete Signal Enable. Values: - 0x0 (ENABLED): Response Interrupt is enabled - 0x1 (DISABLED): Response Interrupt is disabled Default Value: 0
7	RESP_ERR_CHK_EN-ABLE	Response Error Check Enable The Host Controller supports response check function to avoid overhead of response error check by Host driver. Response types of only R1 and R5 can be checked by the Controller. If the Host Controller checks the response error, set this bit to 1 and set Response Interrupt Disable to 1. If an error is detected, the Response Error interrupt is generated in the Error Interrupt Status register. Note: - Response error check must not be enabled for any response type other than R1 and R5. Values: - 0x0 (DISABLED): Response Error Check is disabled - 0x1 (ENABLED): Response Error Check is enabled Default Value: 0

23.1.6 SDHC0_CORE_XFER_MODE_R (continued)

6	RESP_TYPE	Response Type R1/R5 This bit selects either R1 or R5 as a response type when the Response Error Check is selected. Error statuses checked in R1: - OUT_OF_RANGE - ADDRESS_ERROR - BLOCK_LEN_ERROR - WP_VIOLATION - CARD_IS_LOCKED - COM_CRC_ERROR - CARD_ECC_FAILED - CC_ERROR - ERROR Response Flags checked in R5: - COM_CRC_ERROR - ERROR - FUNCTION_NUMBER - OUT_OF_RANGE Values: - 0x0 (RESP_R1): R1 (Memory) - 0x1 (RESP_R5): R5 (SDIO) Default Value: 0
5	MULTI_BLK_SEL	Multi/Single Block Select This bit is set when issuing multiple-block transfer commands using the DAT line. If this bit is set to 0, it is not necessary to set the Block Count register. Default Value: 0
4	DATA_XFER_DIR	Data Transfer Direction Select This bit defines the direction of DAT line data transfers. This bit is set to 1 by the Host Driver to transfer data from the SD/eMMC card to the Host Controller and it is set to 0 for all other commands. Values: - 0x1 (READ): Read (Card to Host) - 0x0 (WRITE): Write (Host to Card) Default Value: 0
3 : 2	AUTO_CMD_ENABLE	Auto Command Enable This field determines use of Auto Command functions. Note: In SDIO, this field must be set as 00b (Auto Command Disabled). Values: - 0x0 (AUTO_CMD_DISABLED): Auto Command Disabled - 0x1 (AUTO_CMD12_ENABLED): Auto CMD12 Enable - 0x2 (AUTO_CMD23_ENABLED): Auto CMD23 Enable - 0x3 (AUTO_CMD_AUTO_SEL): Auto CMD Auto Select Default Value: 0
1	BLOCK_COUNT_ENABLE	Block Count Enable This bit is used to enable the Block Count register, which is relevant for multiple block transfers. If this bit is set to 0, the Block Count register is disabled, which is useful in executing an infinite transfer. The Host Driver must set this bit to 0 when ADMA is used. When 16-bit Block Count register is used, the Host Driver can set this bit to 0 in ADMA2 mode to enable larger data transfer than the maximum of 65535 block counts supported by the 16-bit Block Count register. Default Value: 0

23.1.6 SDHC0_CORE_XFER_MODE_R (continued)

0	DMA_ENABLE	DMA Enable This bit enables the DMA functionality. If this bit is set to 1, a DMA operation begins when the Host Driver writes to the Command register. You can select one of the DMA modes by using DMA Select in the Host Control 1 register. Values: - 0x1 (ENABLED): DMA Data transfer - 0x0 (DISABLED): No data transfer or Non-DMA data transfer Default Value: 0

23.1.7 SDHC0_CORE_CMD_R

Description: Command register

Address: 0x4481100E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	R		R	R	R	R	R	
Name	CMD_TYPE [7:6]		DATA_PRE-SENT_SEL	CMD_IDX-_CHK_EN-ABLE	CM-D_CRC_CH K_ENABLE	SUB_CM-D_FLAG	RESP_TYPE_SELECT [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		CMD_INDEX [13:8]					

Bits	Name	Description
13 : 8	CMD_INDEX	Command Index These bits are set to the command number that is specified in bits 45-40 of the Command Format. Default Value: 0
7 : 6	CMD_TYPE	Command Type These bits indicate the command type. Note: While issuing Abort CMD using CMD12/CMD52 or reset CMD using CMD0/CMD52, CMD_TYPE field shall be set to 0x3. Values: - 0x3 (ABORT_CMD): Abort - 0x2 (RESUME_CMD): Resume - 0x1 (SUSPEND_CMD): Suspend - 0x0 (NORMAL_CMD): Normal Default Value: 0
5	DATA_PRESENT_SEL	Data Present Select This bit is set to 1 to indicate that data is present and that the data is transferred using the DAT line. This bit is set to 0 in the following instances: - Command using the CMD line - Command with no data transfer but using busy signal on the DAT[0] line - Resume Command Values: - 0x0 (NO_DATA): No Data Present - 0x1 (DATA): Data Present Default Value: 0

23.1.7 SDHC0_CORE_CMD_R (continued)

4	CMD_IDX_CHK_ENABLE	Command Index Check Enable This bit enables the Host Controller to check the index field in the response to verify if it has the same value as the command index. If the value is not the same, it is reported as a Command Index error. Note: - Index Check enable must be set to 0 for the command with no response, R2 response, R3 response and R4 response. Values: - 0x0 (DISABLED): Disable - 0x1 (ENABLED): Enable Default Value: 0
3	CMD_CRC_CHK_ENABLE	Command CRC Check Enable This bit enables the Host Controller to check the CRC field in the response. If an error is detected, it is reported as a Command CRC error. Note: - CRC Check enable must be set to 0 for the command with no response, R3 response, and R4 response. Values: - 0x0 (DISABLED): Disable - 0x1 (ENABLED): Enable Default Value: 0
2	SUB_CMD_FLAG	Sub Command Flag This bit distinguishes between a main command and a sub command. Values: - 0x0 (MAIN): Main Command - 0x1 (SUB): Sub Command Default Value: 0
1 : 0	RESP_TYPE_SELECT	Response Type Select This bit indicates the type of response expected from the card. Values: - 0x0 (NO_RESP): No Response - 0x1 (RESP_LEN_136): Response Length 136 - 0x2 (RESP_LEN_48): Response Length 48 - 0x3 (RESP_LEN_48B): Response Length 48; Check Busy after response Default Value: 0

23.1.8 SDHC0_CORE_RESP01_R

Description: Response Register 0/1

Address: 0x44811010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESP01 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESP01 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RESP01 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	RESP01 [31:24]							

Bits	Name	Description
31 : 0	RESP01	Command Response These bits reflect 39-8 bits of SD/eMMC Response Field. Note: For Auto CMD, the 32-bit response (bits 39-8 of the Response Field) is updated in the RESP67_R register. Default Value: 0

23.1.9 SDHC0_CORE_RESP23_R

Description: Response Register 2/3

Address: 0x44811014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESP23 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESP23 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RESP23 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	RESP23 [31:24]							

Bits	Name	Description
31 : 0	RESP23	Command Response These bits reflect 71-40 bits of the SD/eMMC Response Default Value: 0

23.1.10 SDHC0_CORE_RESP45_R

Description: Response Register 4/5

Address: 0x44811018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESP45 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESP45 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RESP45 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	RESP45 [31:24]							

Bits	Name	Description
31 : 0	RESP45	Command Response These bits reflect 103-72 bits of the Response Field. Default Value: 0

23.1.11 SDHC0_CORE_RESP67_R

Description: Response Register 6/7

Address: 0x4481101C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESP67 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESP67 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RESP67 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	RESP67 [31:24]							

Bits	Name	Description
31 : 0	RESP67	Command Response These bits reflect bits 135-104 of SD/EMMC Response Field. Note: For Auto CMD, this register also reflects the 32-bit response (bits 39-8 of the Response Field). Default Value: 0

23.1.12 SDHC0_CORE_BUF_DATA_R

Description: Buffer Data Port Register

Address: 0x44811020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BUF_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	BUF_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	BUF_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	BUF_DATA [31:24]							

Bits	Name	Description
31 : 0	BUF_DATA	Buffer Data These bits enable access to the Host Controller packet buffer. Default Value: 0

23.1.13 SDHC0_CORE_PSTATE_REG

Description: Present State Register

Address: 0x44811024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				Reserved	R	R	R
HW Access	RW				Reserved	RW	RW	RW
Name	DAT_7_4 [7:4]				Reserved	DAT_LINE_ACTIVE	CMD_IN-HIBIT_DAT	CMD_IN-HIBIT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R	R	R	R
HW Access	Reserved				RW	RW	RW	RW
Name	Reserved [15:12]				BUF_RD_ENABLE	BUF_WR_ENABLE	RD_X-FER_AC-TIVE	WR_X-FER_AC-TIVE

Bits	23	22	21	20	19	18	17	16
SW Access	R				R	R	R	R
HW Access	RW				RW	RW	RW	RW
Name	DAT_3_0 [23:20]				WR_PRO-TECT_SW_LVL	CARD_DE-TECT_PIN_LEVEL	CARD_STABLE	CARD_IN-SERTED

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R	R	Reserved	R	R
HW Access	Reserved			RW	RW	Reserved	RW	RW
Name	Reserved [31:29]			SUB_CM-D_STAT	CMD_IS-SU_ERR	Reserved	HOST_REG_VOL	CM-D_LINE_LVL

Bits	Name	Description
28	SUB_CMD_STAT	Sub Command Status This bit is used to distinguish between a main command and a sub command status. Values: - 0x0 (FALSE): Main Command Status - 0x1 (TRUE): Sub Command Status Default Value: 0
27	CMD_ISSU_ERR	Command Not Issued by Error This bit is set if a command cannot be issued after setting the command register due to an error except the Auto CMD12 error. Values: - 0x0 (FALSE): No error for issuing a command - 0x1 (TRUE): Command cannot be issued Default Value: 0

23.1.13 SDHC0_CORE_PSTATE_REG (continued)

25	HOST_REG_VOL	Host Regulator Voltage Stable This bit is used to check whether the host regulator voltage is stable for switching the voltage of UHS-I mode. This bit reflects the synchronized value of the host_reg_vol_stable signal. Values: - 0x0 (FALSE): Host Regulator Voltage is not stable - 0x1 (TRUE): Host Regulator Voltage is stable Default Value: 0
24	CMD_LINE_LVL	Command-Line Signal Level This bit is used to check the CMD line level to recover from errors and for debugging. These bits reflect the value of the sd_cmd_in signal. Default Value: 0
23 : 20	DAT_3_0	DAT[3:0] Line Signal Level This bit is used to check the DAT line level to recover from errors and for debugging. These bits reflect the value of the sd_dat_in (lower nibble) signal. Default Value: 0
19	WR_PROTECT_SW_LVL	Write Protect Switch Pin Level This bit is supported only for memory and combo cards. This bit reflects the synchronized value of the card_write_prot signal. Values: - 0x0 (FALSE): Write protected - 0x1 (TRUE): Write enabled Default Value: 0
18	CARD_DE-TECT_PIN_LEVEL	Card Detect Pin Level This bit reflects the inverse synchronized value of the card_detect_n signal. Values: - 0x0 (FALSE): No card present - 0x1 (TRUE): Card Present Default Value: 0
17	CARD_STABLE	Card Stable This bit indicates the stability of the Card Detect Pin Level. A card is not detected if this bit is set to 1 and the value of the CARD_INSERTED bit is 0. Values: - 0x0 (FALSE): Reset or Debouncing - 0x1 (TRUE): No Card or Inserted Default Value: 0
16	CARD_INSERTED	Card Inserted This bit indicates whether a card has been inserted. The Host Controller debounces this signal so that Host Driver need not wait for it to stabilize. Values: - 0x0 (FALSE): Reset, Debouncing, or No card - 0x1 (TRUE): Card Inserted Default Value: 0
11	BUF_RD_ENABLE	Buffer Read Enable This bit is used for non-DMA transfers. This bit is set if valid data exists in the Host buffer. Values: - 0x0 (DISABLED): Read disable - 0x1 (ENABLED): Read enable Default Value: 0

23.1.13 SDHC0_CORE_PSTATE_REG (continued)

10	BUF_WR_ENABLE	Buffer Write Enable This bit is used for non-DMA transfers. This bit is set if space is available for writing data. Values: - 0x0 (DISABLED): Write disable - 0x1 (ENABLED): Write enable Default Value: 0
9	RD_XFER_ACTIVE	Read Transfer Active This bit indicates whether a read transfer is active for SD/eMMC mode. Values: - 0x0 (INACTIVE): No valid data - 0x1 (ACTIVE): Transferring data Default Value: 0
8	WR_XFER_ACTIVE	Write Transfer Active This status indicates whether a write transfer is active for SD/eMMC mode. Values: - 0x0 (INACTIVE): No valid data - 0x1 (ACTIVE): Transferring data Default Value: 0
7 : 4	DAT_7_4	DAT[7:4] Line Signal Level This bit is used to check the DAT line level to recover from errors and for debugging. These bits reflect the value of the sd_dat_in (upper nibble) signal. Default Value: 0
2	DAT_LINE_ACTIVE	DAT Line Active (SD/eMMC Mode only) This bit indicates whether one of the DAT lines on the SD/eMMC bus is in use. In the case of read transactions, this bit indicates whether a read transfer is executing on the SD/eMMC bus. In the case of write transactions, this bit indicates whether a write transfer is executing on the SD/eMMC bus. For a command with busy, this status indicates whether the command executing busy is executing on an SD or eMMC bus. Values: - 0x0 (INACTIVE): DAT Line Inactive - 0x1 (ACTIVE): DAT Line Active Default Value: 0
1	CMD_INHIBIT_DAT	Command Inhibit (DAT) This bit is applicable for SD/eMMC mode and is generated if either DAT line active or Read transfer active is set to 1. If this bit is set to 0, it indicates that the Host Controller can issue subsequent SD/eMMC commands. Values: - 0x0 (READY): Can issue command which used DAT line - 0x1 (NOT_READY): Cannot issue command which used DAT line Default Value: 0

23.1.13 SDHC0_CORE_PSTATE_REG (continued)

0	CMD_INHIBIT	Command Inhibit (CMD) This bit indicates the following : - SD/eMMC mode: If this bit is set to 0, it indicates that the CMD line is not in use and the Host controller can issue an SD/eMMC command using the CMD line. This bit is set when the command register is written. This bit is cleared when the command response is received. This bit is not cleared by the response of auto CMD12/23 but cleared by the response of read/write command. Values: - 0x0 (READY): Host Controller is ready to issue a command - 0x1 (NOT_READY): Host Controller is not ready to issue a command Default Value: 0

23.1.14 SDHC0_CORE_HOST_CTRL1_R

Description: Host Control 1 Register

Address: 0x44811028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW		RW	RW	RW
HW Access	R	R	R	R		R	R	R
Name	CARD_DE-TECT_SIG_SEL	CARD_DE-TECT_TEST_LVL	EXT_-DAT_XFER	DMA_SEL [4:3]		HIGH_-SPEED_EN	DAT_X-FER_WIDTH	LED_CTRL

Bits	Name	Description
7	CARD_DETECT_SIG_-SEL	Card Detect Signal Selection This bit selects a source for card detection. When the source for the card detection is switched, the interrupt must be disabled during the switching period. Values: - 0x1 (CARD_DT_TEST_LEVEL): Card Detect Test Level is selected (for test purpose) - 0x0 (card_detect_n): card_detect_n signal is selected (for normal use) Default Value: 0
6	CARD_DE-TECT_TEST_LVL	Card Detect Test Level This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates whether a card inserted or not. Values: - 0x1 (CARD_INSERTED): Card Inserted - 0x0 (No_CARD): No Card Default Value: 0
5	EXT_DAT_XFER	Extended Data Transfer Width This bit controls 8-bit bus width mode of embedded device. Values: - 0x1 (EIGHT_BIT): 8-bit Bus Width - 0x0 (DEFAULT): Bus Width is selected by the Data Transfer Width Default Value: 0
4 : 3	DMA_SEL	DMA Select This field is used to select the DMA type. When Host Version 4 Enable is 1 in Host Control 2 register: - 0x0 - SDMA is selected - 0x1 - Reserved - 0x2 - ADMA2 is selected - 0x3 - ADMA2 or ADMA3 is selected When Host Version 4 Enable is 0 in Host Control 2 register: - 0x0 - SDMA is selected - 0x1 - Reserved - 0x2 - 32-bit Address ADMA2 is selected - 0x3 - Reserved Values: - 0x0 (SDMA): SDMA is selected - 0x1 (RSVD_BIT): Reserved - 0x2 (ADMA2): ADMA2 is selected - 0x3 (ADMA2_3): ADMA2 or ADMA3 is selected Default Value: 0

23.1.14 SDHC0_CORE_HOST_CTRL1_R (continued)

2	HIGH_SPEED_EN	High Speed Enable (SD/eMMC Mode only) Before setting this bit, the Host Driver checks the High Speed Support in the Capabilities register. Note: SDHC always outputs the sd_cmd_out and sd_dat_out lines at the rising edge of card clock irrespective of this bit. Values: - 0x1 (HIGH_SPEED): High Speed mode - 0x0 (NORMAL_SPEED): Normal Speed mode Default Value: 0
1	DAT_XFER_WIDTH	Data Transfer Width For SD/eMMC mode,this bit selects the data transfer width of the Host Controller. The Host Driver sets it to match the data width of the SD/eMMC card. Values: - 0x1 (FOUR_BIT): 4-bit mode - 0x0 (ONE_BIT): 1-bit mode Default Value: 0
0	LED_CTRL	LED Control This bit is used to caution the user not to remove the card while the SD card is being accessed. The value is reflected on the led_ctrl ouput. Values: - 0x0 (OFF): LED off - 0x1 (ON): LED on Default Value: 0

23.1.15 SDHC0_CORE_PWR_CTRL_R

Description: Power Control Register

Address: 0x44811029

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			RW
HW Access	Reserved				R			R
Name	Reserved [7:4]				SD_BUS_VOL_VDD1 [3:1]			SD_BUS_PWR_VDD1

Bits	Name	Description
3 : 1	SD_BUS_VOL_VDD1	These bits are NON-operational (they can be written and read but they have no effect). In a generic HCI host these would select the card supply voltage. But, for the applications targeted for this block it is assumed that the card supply voltage is always fixed at the board level. If for some reason there is a variable power supply then that can be managed through normal GPIO programming separately. Default Value: 0
0	SD_BUS_PWR_VDD1	SD Bus Power for VDD1 This bit enables VDD1 power of the card. This setting is available on the card_if_pwr_en output so that it can be used to control the VDD1 power supply of the card. Before setting this bit, the SD Host Driver sets the SD Bus Voltage Select bit. If the Host Controller detects a No Card state, this bit is cleared. In SD mode, if this bit is cleared, the Host Controller stops the SD Clock by clearing the SD_CLK_IN bit in the CLK_CTRL_R register. Values: - 0x0 (OFF): Power off - 0x1 (ON): Power on Default Value: 0

23.1.16 SDHC0_CORE_BGAP_CTRL_R

Description: Block Gap Control Register

Address: 0x4481102A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	RW	R
Name	Reserved [7:4]				INT_AT_B-GAP	RD_WAIT_CTRL	CONTIN-UE_REQ	STOP_B-G_REQ

Bits	Name	Description
3	INT_AT_BGAP	Interrupt At Block Gap This bit is valid only in the 4-bit mode of an SDIO card and is used to select a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Values: - 0x0 (DISABLE): Disabled - 0x1 (ENABLE): Enabled Default Value: 0
2	RD_WAIT_CTRL	Reserved: set to 0 Default Value: 0
1	CONTINUE_REQ	Continue Request This bit is used to restart the transaction, which was stopped using the Stop At Block Gap Request. The Host Controller automatically clears this bit when the transaction restarts. If stop at block gap request is set to 1, any write to this bit is ignored. Values: - 0x0 (NO_AFFECT): No Affect - 0x1 (RESTART): Restart Default Value: 0
0	STOP_BG_REQ	Stop At Block Gap Request This bit is used to stop executing read and write transactions at the next block gap for non-DMA, SDMA, and ADMA transfers. Values: - 0x0 (XFER): Transfer - 0x1 (STOP): Stop Default Value: 0

23.1.17 SDHC0_CORE_WUP_CTRL_R

Description: Wakeup Control Register

Address: 0x4481102B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [7:3]					WUP_-CARD_RE-MOVAL	WUP_-CARD_INS ERT	WUP_-CARD_INT

Bits	Name	Description
2	WUP_CARD_REMOVAL	Wakeup Event Enable on SD Card Removal This bit enables wakeup event through Card Removal assertion in the Normal Interrupt Status register. For the SDIO card, Wake Up Support (FN_WUS) in the Card Information Structure (CIS) register does not affect this bit. Values: - 0x0 (DISABLED): Disable - 0x1 (ENABLED): Enable Default Value: 0
1	WUP_CARD_INSERT	Wakeup Event Enable on SD Card Insertion This bit enables wakeup event through Card Insertion assertion in the Normal Interrupt Status register. FN_WUS (Wake Up Support) in CIS does not affect this bit. Values: - 0x0 (DISABLED): Disable - 0x1 (ENABLED): Enable Default Value: 0
0	WUP_CARD_INT	Wakeup Event Enable on SDIO Card Interrupt (through DAT[1]). This bit enables wakeup event through an SDIO Card Interrupt assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. Values: - 0x0 (DISABLED): Disable - 0x1 (ENABLED): Enable Default Value: 0

23.1.18 SDHC0_CORE_CLK_CTRL_R

Description: Clock Control Register

Address: 0x4481102C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	Reserved	RW	RW	R	RW
HW Access	RW		RW	Reserved	R	R	RW	R
Name	UPPER_FREQ_SEL [7:6]		CLK_-GEN_SE-LECT	Reserved	PLL_EN-ABLE	SD_-CLK_EN	INTER-NAL_-CLK_STAB LE	INTER-NAL_-CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	FREQ_SEL [15:8]							

Bits	Name	Description
15 : 8	FREQ_SEL	SDCLK Frequency Select These bits are used to select the frequency of the SDCLK signal. 10-bit Divided Clock Mode: - 0x3FF - 1/2046 Divided clock - ..... - N - 1/2N Divided Clock - ..... - 0x002 - 1/4 Divided Clock - 0x001 - 1/2 Divided Clock - 0x000 - Base clock (10MHz - 255 MHz) Default Value: 0
7 : 6	UPPER_FREQ_SEL	These bits specify the upper 2 bits of 10-bit SDCLK Frequency Select control. Default Value: 0
5	CLK_GEN_SELECT	Clock Generator Select This bit is used to select the clock generator mode in SDCLK Frequency Select. Values: - 0x0 (FALSE): Divided Clock Mode - 0x1 (TRUE): Programmable Clock Mode Default Value: 0
3	PLL_ENABLE	PLL Enable This bit is used to activate the PLL (applicable when Host Version 4 Enable = 1). Values: - 0x0 (FALSE): PLL is in low power mode - 0x1 (TRUE): PLL is enabled Default Value: 0
2	SD_CLK_EN	SD/eMMC Clock Enable This bit stops the clk_card output when set to 0. The SDCLK Frequency Select bit can be changed when this bit is set to 0. Values: - 0x0 (FALSE): Disable providing clk_card - 0x1 (TRUE): Enable providing clk_card Default Value: 0

23.1.18 SDHC0_CORE_CLK_CTRL_R (continued)

1	INTERNAL_CLK_STABLE	Internal Clock Stable This bit enables the Host Driver to check the clock stability twice after the Internal Clock Enable bit is set and after the PLL Enable bit is set. This bit reflects the synchronized value of the Internal Clock Stable signal after the Internal Clock Enable bit is set to 1 and also reflects the synchronized value of the Card Clock Stable signal after the PLL Enable bit is set to 1. Values: - 0x0 (FALSE): Not Ready - 0x1 (TRUE): Ready Default Value: 0
0	INTERNAL_CLK_EN	Internal Clock Enable This bit is set to 0 when the Host Driver is not using the Host Controller or the Host Controller awaits a wakeup interrupt. The Host Controller must stop its internal clock to enter a very low power state. Certain registers are not accessible when this bit is off. So, to be safe turn it on for any register access. Values: - 0x0 (FALSE): Stop - 0x1 (TRUE): Oscillate Default Value: 0

23.1.19 SDHC0_CORE_TOUT_CTRL_R

Description: Timeout Control Register

Address: 0x4481102E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				TOUT_CNT [3:0]			

Bits	Name	Description
3 : 0	TOUT_CNT	Data Timeout Counter Value. This value determines the interval by which DAT line timeouts are detected. The Timeout clock frequency is generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register). The values for these bits are: - 0xF - Reserved - 0xE - TMCLK x 2^27 - ..... - 0x1 - TMCLK x 2^14 - 0x0 - TMCLK x 2^13 Note: During a boot operating in an eMMC mode, an application must configure the boot data timeout value (approximately 1 sec) in this bit. Default Value: 0

23.1.20 SDHC0_CORE_SW_RST_R

Description: Software Reset Register

Address: 0x4481102F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					RW	RW	RW
Name	Reserved [7:3]					SW_RST_-DAT	SW_RST_CMD	SW_RST_ALL

Bits	Name	Description
2	SW_RST_DAT	Software Reset For DAT line This bit is used in SD/eMMC mode and it resets only a part of the data circuit and the DMA circuit is also reset. The following registers and bits are cleared by this bit: - Buffer Data Port register - Buffer is cleared and initialized. - Present state register - Buffer Read Enable - Buffer Write Enable - Read Transfer Active - Write Transfer Active - DAT Line Active - Command Inhibit (DAT) - Block Gap Control register - Continue Request - Stop At Block Gap Request - Normal Interrupt status register - Buffer Read Ready - Buffer Write Ready - DMA Interrupt - Block Gap Event - Transfer Complete Values: - 0x0 (FALSE): Work - 0x1 (TRUE): Reset Default Value: 0
1	SW_RST_CMD	Software Reset For CMD line This bit resets only a part of the command circuit to be able to issue a command. This reset is effective only for a command issuing circuit (including response error statuses related to Command Inhibit (CMD) control) and does not affect the data transfer circuit. Host Controller can continue data transfer even after this reset is executed while handling subcommand-response errors. The following registers and bits are cleared by this bit: - Present State register - Command Inhibit (CMD) bit - Normal Interrupt Status register - Command Complete bit - Error Interrupt Status - Response error statuses related to Command Inhibit (CMD) bit Values: - 0x0 (FALSE): Work - 0x1 (TRUE): Reset Default Value: 0

23.1.20 SDHC0_CORE_SW_RST_R (continued)

0	SW_RST_ALL	Software Reset For All This reset affects the entire Host Controller except for the card detection circuit. During its initialization, the Host Driver sets this bit to 1 to reset the Host Controller. All registers are reset except the capabilities register. If this bit is set to 1, the Host Driver must issue reset command and reinitialize the card. Values: - 0x0 (FALSE): Work - 0x1 (TRUE): Reset Default Value: 0

23.1.21 SDHC0_CORE_NORMAL_INT_STAT_R

Description: Normal Interrupt Status Register

Address: 0x44811030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	CARD_RE-MOVAL	CARD_IN-SERTION	BUF_RD_R EADY	BUF_WR_R EADY	DMA_IN-TERRUPT	BGAP_EVE NT	XFER_-COMPLETE	CMD_COM-PLETE

Bits	15	14	13	12	11	10	9	8
SW Access	R	RW1C	R	Reserved				R
HW Access	RW	RW	RW	Reserved				RW
Name	ERR_IN-TERRUPT	CQE_EVEN T	FX_EVENT	Reserved [12:9]				CARD_IN-TERRUPT

Bits	Name	Description
15	ERR_INTERRUPT	Error Interrupt If any of the bits in the Error Interrupt Status register are set, then this bit is set. Values: - 0x0 (FALSE): No Error - 0x1 (TRUE): Error Default Value: 0
14	CQE_EVENT	Command Queuing Event This status is set if Command Queuing/Crypto related event has occurred in eMMC/SD mode. Read CQHCI's CQIS/CRNQIS register for more details. In UHS-II Mode, this bit is irrelevant. Values: - 0x0 (FALSE): No Event - 0x1 (TRUE): Command Queuing Event is detected Default Value: 0
13	FX_EVENT	FX Event This status is set when R[14] of response register is set to 1 and Response Type R1/R5 is set to 0 in Transfer Mode register. This interrupt is used with response check function. Values: - 0x0 (FALSE): No Event - 0x1 (TRUE): FX Event is detected Default Value: 0
8	CARD_INTERRUPT	Card Interrupt This bit reflects the synchronized value of: - DAT[1] Interrupt Input for SD Mode Values: - 0x0 (FALSE): No Card Interrupt - 0x1 (TRUE): Generate Card Interrupt Default Value: 0
7	CARD_REMOVAL	Card Removal This bit is set if the Card Inserted in the Present State register changes from 1 to 0. Values: - 0x0 (FALSE): Card state stable or Debouncing - 0x1 (TRUE): Card Removed Default Value: 0

23.1.21 SDHC0_CORE_NORMAL_INT_STAT_R (continued)

6	CARD_INSERTION	Card Insertion This bit is set if the Card Inserted in the Present State register changes from 0 to 1. Values: - 0x0 (FALSE): Card state stable or Debouncing - 0x1 (TRUE): Card Inserted Default Value: 0
5	BUF_RD_READY	Buffer Read Ready This bit is set if the Buffer Read Enable changes from 0 to 1. Values: - 0x0 (FALSE): Not ready to read buffer - 0x1 (TRUE): Ready to read buffer Default Value: 0
4	BUF_WR_READY	Buffer Write Ready This bit is set if the Buffer Write Enable changes from 0 to 1. Values: - 0x0 (FALSE): Not ready to write buffer - 0x1 (TRUE): Ready to write buffer Default Value: 0
3	DMA_INTERRUPT	DMA Interrupt This bit is set if the Host Controller detects the SDMA Buffer Boundary during transfer. In case of ADMA, by setting the Int field in the descriptor table, the Host controller generates this interrupt. This interrupt is not generated after a Transfer Complete. Values: - 0x0 (FALSE): No DMA Interrupt - 0x1 (TRUE): DMA Interrupt is generated Default Value: 0
2	BGAP_EVENT	Block Gap Event This bit is set when both read/write transaction is stopped at block gap due to a Stop at Block Gap Request. Values: - 0x0 (FALSE): No Block Gap Event - 0x1 (TRUE): Transaction stopped at block gap Default Value: 0
1	XFER_COMPLETE	Transfer Complete This bit is set when a read/write transfer and a command with status busy is completed. Values: - 0x0 (FALSE): Not complete - 0x1 (TRUE): Command execution is completed Default Value: 0
0	CMD_COMPLETE	Command Complete In an SD/eMMC Mode, this bit is set when the end bit of a response except for Auto CMD12 and Auto CMD23. This interrupt is not generated when the Response Interrupt Disable in Transfer Mode Register is set to 1. Values: - 0x0 (FALSE): No command complete - 0x1 (TRUE): Command Complete Default Value: 0

23.1.22 SDHC0_CORE_ERROR_INT_STAT_R

Description: Error Interrupt Status Register

Address: 0x44811032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	CUR_LMT_ERR	DATA_END_BIT_ERR	DATA_CRC_ERR	DATA_TOUT_ERR	CMD_IDX-_ERR	CM-D_END_BIT_ERR	CM-D_CRC_ERR	CM-D_TOUT_ERR

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved			RW	RW	RW	RW	RW
Name	Reserved [15:13]			BOOT_ACK_ERR	RESP_ERR	TUN-ING_ERR	AD-MA_ERR	AUTO_CM-D_ERR

Bits	Name	Description
12	BOOT_ACK_ERR	Boot Acknowledgement Error This bit is set when there is a timeout for boot acknowledgement or when detecting boot ack status having a value other than 010. This is applicable only when boot acknowledgement is expected in eMMC mode. In SD mode, this bit is irrelevant. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Error Default Value: 0
11	RESP_ERR	Response Error Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1.This is applicable in SD/eMMC mode. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Error Default Value: 0
10	TUNING_ERR	Reserved Default Value: 0

23.1.22 SDHC0_CORE_ERROR_INT_STAT_R (continued)

9	ADMA_ERR	ADMA Error This bit is set when the Host Controller detects error during ADMA-based data transfer. The error could be due to following reasons: - Error response received from System bus (Master I/F) - ADMA3,ADMA2 Descriptors invalid - CQE Task or Transfer descriptors invalid When the error occurs, the state of the ADMA is saved in the ADMA Error Status register. In eMMC CQE mode: The Host Controller generates this Interrupt when it detects an invalid descriptor data (Valid=0) at the ST_FDS state. ADMA Error State in the ADMA Error Status indicates that an error has occurred in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Error Default Value: 0
8	AUTO_CMD_ERR	Auto CMD Error This error status is used by Auto CMD12 and Auto CMD23 in SD/eMMC mode. This bit is set when detecting that any of the bits D00 to D05 in Auto CMD Error Status register has changed from 0 to 1. D07 is effective in case of Auto CMD12. Auto CMD Error Status register is valid while this bit is set to 1 and may be cleared by clearing of this bit. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Error Default Value: 0
7	CUR_LMT_ERR	Current Limit Error By setting the SD Bus Power bit in the Power Control register, the Host Controller is requested to supply power for the SD Bus. If the Host Controller supports the Current Limit function, it can be protected from an illegal card by stopping power supply to the card in which case this bit indicates a failure status. A reading of 1 for this bit means that the Host Controller is not supplying power to the SD card due to some failure. A reading of 0 for this bit means that the Host Controller is supplying power and no error has occurred. The Host Controller may require some sampling time to detect the current limit. DWC_mshc Host Controller does not support this function, this bit is always set to 0. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Power Fail Default Value: 0
6	DATA_END_BIT_ERR	Data End Bit Error This error occurs in SD/eMMC mode either when detecting 0 at the end bit position of read data that uses the DAT line or at the end bit position of the CRC status. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Error Default Value: 0

23.1.22 SDHC0_CORE_ERROR_INT_STAT_R (continued)

5	DATA_CRC_ERR	Data CRC Error This error occurs in SD/eMMC mode when detecting CRC error when transferring read data which uses the DAT line, when detecting the Write CRC status having a value of other than 010 or when write CRC status timeout. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Error Default Value: 0
4	DATA_TOUT_ERR	Data Timeout Error This bit is set in SD/eMMC mode when detecting one of the following timeout conditions: - Busy timeout for R1b, R5b type - Busy timeout after Write CRC status - Write CRC Status timeout - Read Data timeout Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Time out Default Value: 0
3	CMD_IDX_ERR	Command Index Error This bit is set if a Command Index error occurs in the command respons in SD/eMMC mode. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Error Default Value: 0
2	CMD_END_BIT_ERR	Command End Bit Error This bit is set when detecting that the end bit of a command response is 0 in SD/eMMC mode. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): End Bit error generated Default Value: 0
1	CMD_CRC_ERR	Command CRC Error Command CRC Error is generated in SD/eMMC mode for following two cases. - If a response is returned and the Command Timeout Error is set to 0 (indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. - The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller aborts the command (stop driving CMD line) and set this bit to 1. The Command Timeout Error is also set to 1 to distinguish a CMD line conflict. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): CRC error generated Default Value: 0
0	CMD_TOUT_ERR	Command Timeout Error In SD/eMMC Mode,this bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict, along with Command CRC Error bit, this bit is set to 1, without waiting for 64 SD/eMMC card clock cycles. Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Time out Default Value: 0

23.1.23 SDHC0_CORE_NORMAL_INT_STAT_EN_R

Description: Normal Interrupt Status Enable Register

Address: 0x44811034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CARD_REMOVAL_STAT_EN	CARD_INSERTION_STAT_EN	BUF_RD_READY_STAT_EN	BUF_WR_READY_STAT_EN	DMA_INTERRUPT_STAT_EN	BGAP_EVENT_STAT_EN	XFER_COMPLETE_STAT_EN	CMD_COMPLETE_STAT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved	R	R	R	R	R	R	R
Name	Reserved	CQE_EVENT_STAT_EN	FX_EVENT_STAT_EN	RE_TUNE_EVENT_STAT_EN	INT_C_STAT_EN	INT_B_STAT_EN	INT_A_STAT_EN	CARD_INTERRUPT_STAT_EN

Bits	Name	Description
14	CQE_EVENT_STAT_EN	CQE Event Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
13	FX_EVENT_STAT_EN	FX Event Status Enable This bit is added from Version 4.10. Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
12	RE_TUNE_EVENT_STAT_EN	Reserved: set to 0 Default Value: 0
11	INT_C_STAT_EN	Reserved: set to 0 Default Value: 0
10	INT_B_STAT_EN	Reserved: set to 0 Default Value: 0
9	INT_A_STAT_EN	Reserved: set to 0 Default Value: 0
8	CARD_INTERRUPT_STAT_EN	Card Interrupt Status Enable If this bit is set to 0, the Host Controller clears the interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The Host Driver may clear the Card Interrupt Status Enable before servicing the Card Interrupt and may set this bit again after all interrupt requests from the card are cleared to prevent inadvertent interrupts. Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0

23.1.23 SDHC0_CORE_NORMAL_INT_STAT_EN_R (continued)

7	CARD_REMOV-AL_STAT_EN	Card Removal Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
6	CARD_INSER-TION_STAT_EN	Card Insertion Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
5	BUF_RD_READY_STAT_EN	Buffer Read Ready Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
4	BUF_WR_READY_STAT_EN	Buffer Write Ready Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
3	DMA_INTER-RUPT_STAT_EN	DMA Interrupt Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
2	BGAP_EVENT_STAT_EN	Block Gap Event Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
1	XFER_COM-PLETE_STAT_EN	Transfer Complete Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
0	CMD_COM-PLETE_STAT_EN	Command Complete Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0

23.1.24 SDHC0_CORE_ERROR_INT_STAT_EN_R

Description: Error Interrupt Status Enable Register

Address: 0x44811036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CUR_LMT_ER-R_STAT_EN	DATA_END_BIT_ER-R_STAT_EN	DATA_CRC_ER-R_STAT_EN	DATA_TOUT_ER-R_STAT_EN	CMD_IDX-_ER-R_STAT_EN	CM-D_END_BIT_ER-R_STAT_EN	CM-D_CRC_ER R_STAT_EN	CM-D_TOUT_E RR_STAT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VEN-DOR_ER-R_STAT_EN3	VEN-DOR_ER-R_STAT_EN2	VEN-DOR_ER-R_STAT_EN1	BOOT_ACK_ER-R_STAT_EN	RESP_ER-R_STAT_EN	TUN-ING_ER-R_STAT_EN	ADMA_ER-R_STAT_EN	AUTO_CM-D_ER-R_STAT_EN

Bits	Name	Description
15	VENDOR_ER-R_STAT_EN3	Reserved: set to 0 Default Value: 0
14	VENDOR_ER-R_STAT_EN2	Reserved: set to 0 Default Value: 0
13	VENDOR_ER-R_STAT_EN1	Reserved: set to 0 Default Value: 0
12	BOOT_ACK_ER-R_STAT_EN	Boot Acknowledgment Error (eMMC Mode only) Setting this bit to 1 enables setting of Boot Acknowledgment Error in Error Interrupt Status register (ERROR_INT_STAT_R). Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
11	RESP_ERR_STAT_EN	Response Error Status Enable (SD Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
10	TUNING_ERR_STAT_EN	Tuning Error Status Enable (UHS-I Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
9	ADMA_ERR_STAT_EN	ADMA Error Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0

23.1.24 SDHC0_CORE_ERROR_INT_STAT_EN_R (continued)

8	AUTO_CMD_ER-R_STAT_EN	Auto CMD Error Status Enable (SD/eMMC Mode only). Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
7	CUR_LMT_ER-R_STAT_EN	Current Limit Error Status Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
6	DATA_END_BIT_ER-R_STAT_EN	Data End Bit Error Status Enable (SD/eMMC Mode only). Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
5	DATA_CRC_ER-R_STAT_EN	Data CRC Error Status Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
4	DATA_TOUT_ER-R_STAT_EN	Data Timeout Error Status Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
3	CMD_IDX_ER-R_STAT_EN	Command Index Error Status Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
2	CMD_END_BIT_ER-R_STAT_EN	Command End Bit Error Status Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
1	CMD_CRC_ER-R_STAT_EN	ommand CRC Error Status Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
0	CMD_TOUT_ER-R_STAT_EN	Command Timeout Error Status Enable (SD/eMMC Mode only). Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0

23.1.25 SDHC0_CORE_NORMAL_INT_SIGNAL_EN_R

Description: Normal Interrupt Signal Enable Register

Address: 0x44811038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CARD_REMOVAL_SIGNAL_EN	CARD_INSERTION_SIGNAL_EN	BUF_RD_READY_SIGNAL_EN	BUF_WR_READY_SIGNAL_EN	DMA_INTERRUPT_SIGNAL_EN	BGAP_EVENT_SIGNAL_EN	XFER_COMPLETE_SIGNAL_EN	CMD_COMPLETE_SIGNAL_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved	R	R	R	R	R	R	R
Name	Reserved	CQE_EVENT_SIGNAL_EN	FX_EVENT_SIGNAL_EN	RE_TUNE_EVENT_SIGNAL_EN	INT_C_SIGNAL_EN	INT_B_SIGNAL_EN	INT_A_SIGNAL_EN	CARD_INTERRUPT_SIGNAL_EN

Bits	Name	Description
14	CQE_EVENT_SIGNAL_EN	Command Queuing Engine Event Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
13	FX_EVENT_SIGNAL_EN	FX Event Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
12	RE_TUNE_EVENT_SIGNAL_EN	Reserved: set to 0 Default Value: 0
11	INT_C_SIGNAL_EN	Reserved: set to 0 Default Value: 0
10	INT_B_SIGNAL_EN	Reserved: set to 0 Default Value: 0
9	INT_A_SIGNAL_EN	Reserved: set to 0 Default Value: 0
8	CARD_INTERRUPT_SIGNAL_EN	Card Interrupt Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
7	CARD_REMOVAL_SIGNAL_EN	Card Removal Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0

23.1.25 SDHC0_CORE_NORMAL_INT_SIGNAL_EN_R (continued)

6	CARD_INSERTION_SIGNAL_EN	Card Insertion Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
5	BUF_RD_READY_SIGNAL_EN	Buffer Read Ready Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
4	BUF_WR_READY_SIGNAL_EN	Buffer Write Ready Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
3	DMA_INTERRUPT_SIGNAL_EN	DMA Interrupt Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
2	BGAP_EVENT_SIGNAL_EN	Block Gap Event Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
1	XFER_COMPLETE_SIGNAL_EN	Transfer Complete Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
0	CMD_COMPLETE_SIGNAL_EN	Command Complete Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0

23.1.26 SDHC0_CORE_ERROR_INT_SIGNAL_EN_R

Description: Error Interrupt Signal Enable Register

Address: 0x4481103A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CUR_LMT_ERR_SIGNAL_EN	DATA_END_BIT_ERR_SIGNAL_EN	DATA_CRC_ERR_SIGNAL_EN	DATA_TOUT_ERR_SIGNAL_EN	CMD_IDX_ERR_SIGNAL_EN	CMD_END_BIT_ERR_SIGNAL_EN	CMD_CRC_ERR_SIGNAL_EN	CMD_TOUT_ERR_SIGNAL_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VENDOR_ERR_SIGNAL_EN3	VENDOR_ERR_SIGNAL_EN2	VENDOR_ERR_SIGNAL_EN1	BOOT_ACK_ERR_SIGNAL_EN	RESP_ERR_SIGNAL_EN	TUNING_ERR_SIGNAL_EN	ADMA_ERR_SIGNAL_EN	AUTO_CMD_ERR_SIGNAL_EN

Bits	Name	Description
15	VENDOR_ERR_SIGNAL_EN3	Reserved: set to 0 Default Value: 0
14	VENDOR_ERR_SIGNAL_EN2	Reserved: set to 0 Default Value: 0
13	VENDOR_ERR_SIGNAL_EN1	Reserved: set to 0 Default Value: 0
12	BOOT_ACK_ERR_SIGNAL_EN	Boot Acknowledgment Error (eMMC Mode only). Setting this bit to 1 enables generating interrupt signal when Boot Acknowledgement Error in Error Interrupt Status register is set. Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
11	RESP_ERR_SIGNAL_EN	Response Error Signal Enable (SD Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
10	TUNING_ERR_SIGNAL_EN	Reserved: set to 0 Default Value: 0
9	ADMA_ERR_SIGNAL_EN	ADMA Error Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
8	AUTO_CMD_ERR_SIGNAL_EN	Auto CMD Error Signal Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0

23.1.26 SDHC0_CORE_ERROR_INT_SIGNAL_EN_R (continued)

7	CUR_LMT_ERR_SIGNAL_EN	Current Limit Error Signal Enable Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
6	DATA_END_BIT_ERR_SIGNAL_EN	Data End Bit Error Signal Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
5	DATA_CRC_ERR_SIGNAL_EN	Data CRC Error Signal Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
4	DATA_TOUT_ERR_SIGNAL_EN	Data Timeout Error Signal Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
3	CMD_IDX_ERR_SIGNAL_EN	Command Index Error Signal Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): No error - 0x1 (TRUE): Error Default Value: 0
2	CMD_END_BIT_ERR_SIGNAL_EN	Command End Bit Error Signal Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
1	CMD_CRC_ERR_SIGNAL_EN	Command CRC Error Signal Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0
0	CMD_TOUT_ERR_SIGNAL_EN	Command Timeout Error Signal Enable (SD/eMMC Mode only) Values: - 0x0 (FALSE): Masked - 0x1 (TRUE): Enabled Default Value: 0

23.1.27 SDHC0_CORE_AUTO_CMD_STAT_R

Description: Auto CMD Status Register

Address: 0x4481103C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	Reserved	R	R	R	R	R	R
HW Access	RW	Reserved	RW	RW	RW	RW	RW	RW
Name	CMD_NOT_ISSUED_AUTO_CMD12	Reserved	AUTO_CMD_RESP_ERR	AUTO_CMD_IDX_ERR	AUTO_CMD_EBIT_ERR	AUTO_CMD_CRC_ERR	AUTO_CMD_TOUT_ERR	AUTO_CMD12_NOT_EXEC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	Name	Description
7	CMD_NOT_ISSUED_AUTO_CMD12	Command Not Issued By Auto CMD12 Error If this bit is set to 1, CMD_wo_DAT is not executed due to an Auto CMD12 Error (D04-D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: - 0x1 (TRUE): Not Issued - 0x0 (FALSE): No Error Default Value: 0
5	AUTO_CMD_RESP_ERR	Auto CMD Response Error This bit is set when Response Error Check Enable in the Transfer Mode register is set to 1 and an error is detected in R1 response of either Auto CMD12 or CMD13. This status is ignored if any bit between D00 to D04 is set to 1. Values: - 0x1 (TRUE): Error - 0x0 (FALSE): No Error Default Value: 0
4	AUTO_CMD_IDX_ERR	Auto CMD Index Error This bit is set if the command index error occurs in response to a command. Values: - 0x1 (TRUE): Error - 0x0 (FALSE): No Error Default Value: 0
3	AUTO_CMD_EBIT_ERR	Auto CMD End Bit Error This bit is set when detecting that the end bit of command response is 0. Values: - 0x1 (TRUE): End Bit Error Generated - 0x0 (FALSE): No Error Default Value: 0

23.1.27 SDHC0_CORE_AUTO_CMD_STAT_R (continued)

2	AUTO_CMD_CRC_ERR	Auto CMD CRC Error This bit is set when detecting a CRC error in the command response. Values: - 0x1 (TRUE): CRC Error Generated - 0x0 (FALSE): No Error Default Value: 0
1	AUTO_CMD_TOUT_ERR	Auto CMD Timeout Error This bit is set if no response is returned with 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, error status bits (D04-D01) are meaningless. Values: - 0x1 (TRUE): Time out - 0x0 (FALSE): No Error Default Value: 0
0	AUTO_CMD12_NOT_EXEC	Auto CMD12 Not Executed If multiple memory block data transfer is not started due to a command error, this bit is not set because it is not necessary to issue an Auto CMD12. Setting this bit to 1 means that the Host Controller cannot issue Auto CMD12 to stop multiple memory block data transfer, due to some error. If this bit is set to 1, error status bits (D04-D01) is meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: - 0x1 (TRUE): Not Executed - 0x0 (FALSE): Executed Default Value: 0

23.1.28 SDHC0_CORE_HOST_CTRL2_R

Description: Host Control 2 Register

Address: 0x4481103E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW		
HW Access	RW	RW	RW		RW	R		
Name	SAMPLE_CLK_SEL	EXEC_TUNING	DRV_STRENGTH_SEL [5:4]		SIGNALING_EN	UHS_MODE_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	Reserved	RW
HW Access	R	R	R	R	R	R	Reserved	R
Name	PRESET_VAL_ENABLE	ASYNC_INT_ENABLE	ADDRESSING	HOST_VER4_ENABLE	CMD23_ENABLE	ADMA2_LEN_MODE	Reserved	UHS2_IF_ENABLE

Bits	Name	Description
15	PRESET_VAL_ENABLE	Reserved: set to 0 Default Value: 0
14	ASYNC_INT_ENABLE	Asynchronous Interrupt Enable This bit can be set if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Values: - 0x0 (FALSE): Disabled - 0x1 (TRUE): Enabled Default Value: 0
13	ADDRESSING	Reserved: set to 0 Default Value: 0
12	HOST_VER4_ENABLE	Host Version 4 Enable This bit selects either Version 3.00 compatible mode or Version 4 mode. Functions of following fields are modified for Host Version 4 mode: - SDMA Address: SDMA uses ADMA System Address (05Fh-058h) instead of SDMA System Address register (003h-000h) - ADMA2/ADMA3 selection: ADMA3 is selected by DMA select in Host Control 1 register - 32-bit Block Count: SDMA System Address register (003h-000h) is modified to 32-bit Block Count register Note: It is recommended not to program ADMA3 Integrated Descriptor Address registers and Command Queuing registers (if applicable) while operating in Host version less than 4 mode (Host Version 4 Enable = 0). Values: - 0x0 (FALSE): Version 3.00 compatible mode - 0x1 (TRUE): Version 4 mode Default Value: 0

23.1.28 SDHC0_CORE_HOST_CTRL2_R (continued)

11	CMD23_ENABLE	CMD23 Enable If the card supports CMD23, this bit is set to 1. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 data transfer. Values: - 0x0 (FALSE): Auto CMD23 is disabled - 0x1 (TRUE): Auto CMD23 is enabled Default Value: 0
10	ADMA2_LEN_MODE	ADMA2 Length Mode This bit selects ADMA2 Length mode to be either 16-bit or 26-bit. Values: - 0x0 (FALSE): 16-bit Data Length Mode - 0x1 (TRUE): 26-bit Data Length Mode Default Value: 0
8	UHS2_IF_ENABLE	Reserved: set to 0 Default Value: 0
7	SAMPLE_CLK_SEL	Reserved: set to 0 Default Value: 0
6	EXEC_TUNING	Reserved: set to 0 Default Value: 0
5 : 4	DRV_STRENGTH_SEL	Driver Strength Select These bits are used to select the Host Controller output driver in 1.8V signaling UHS-I/eMMC speed modes. The value is reflected on the io_drive_strength[1:0] output. - 0x0 (TYPEB): Driver TYPEB is selected - 0x1 (TYPEA): Driver TYPEA is selected - 0x2 (TYPEC): Driver TYPEC is selected - 0x3 (TYPED): Driver TYPED is selected Default Value: 0
3	SIGNALING_EN	1.8V Signaling Enable This bit controls voltage regulator for I/O cell in SD UHS-I mode. Setting this bit from 0 to 1 starts changing the signal voltage from 3.3V to 1.8V. Host Controller clears this bit if switching to 1.8V signaling fails per protocol. The value is reflected on the io_volt_sel output which can then be used to change an external regulator to supply 1.8V instead of 3.3V on the VDDIO pin associated with the CLK/CMD/DAT signals. Note: This bit must be set for all UHS-I speed modes (SDR12/SDR25/SDR50/DDR50). Values: - 0x0 (V_3_3): 3.3V Signalling - 0x1 (V_1_8): 1.8V Signalling Default Value: 0

23.1.28 SDHC0_CORE_HOST_CTRL2_R (continued)

2 : 0	UHS_MODE_SEL	UHS Mode/eMMC Speed Mode Select These bits are used to select UHS mode in the SD mode of operation. In eMMC mode, these bits are used to select eMMC Speed mode. UHS-I Mode: - 0x0: SDR12 - 0x1: SDR25 - 0x2: SDR50 - 0x3: Reserved - 0x4: DDR50 - 0x5: Reserved - 0x6: Reserved - 0x7: Reserved eMMC Speed Mode (eMMC mode only): - 0x0: Legacy - 0x1: High Speed SDR - 0x2: Reserved - 0x3: Reserved - 0x4: High Speed DDR - 0x5: Reserved - 0x6: Reserved - 0x7: Reserved Default Value: 0

23.1.29 SDHC0_CORE_CAPABILITIES1_R

Description: Capabilities 1 Register - 0 to 31

Address: 0x44811040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	Reserved	R					
HW Access	R	Reserved	R					
Name	TOUT_-CLK_UNIT	Reserved	TOUT_CLK_FREQ [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	BASE_CLK_FREQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	Reserved	R	R	R	
HW Access	R	R	R	Reserved	R	R	R	
Name	SUS_RES_SUPPORT	SDMA_-SUPPORT	HIGH_-SPEED_-SUPPORT	Reserved	ADMA2_-SUPPORT	EMBED-DED_8_BIT	MAX_BLK_LEN [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R		R	R	R	R	R	R
HW Access	R		R	R	R	R	R	R
Name	SLOT_TYPE_R [31:30]		ASYN-C_INT_-SUPPORT	SYS_AD-DR_64_V3	SYS_AD-DR_64_V4	VOLT_18	VOLT_30	VOLT_33

Bits	Name	Description
31 : 30	SLOT_TYPE_R	Slot Type These bits indicate usage of a slot by a specific Host System. Values: - 0x0 (REMOVABLE_SLOT): Removable Card Slot - 0x1 (EMBEDDED_SLOT): Embedded Slot for one Device - 0x2 (SHARED_SLOT): Shared Bus Slot (SD mode) - 0x3 (UHS2_EMBEDDED_SLOT): UHS-II Multiple Embedded Devices Default Value: 0
29	ASYNC_INT_SUPPORT	Asynchronous Interrupt Support (SD Mode only) Values: - 0x0 (FALSE): Asynchronous Interrupt Not Supported - 0x1 (TRUE): Asynchronous Interrupt Supported Default Value: 1

23.1.29 SDHC0_CORE_CAPABILITIES1_R (continued)

28	SYS_ADDR_64_V3	64-bit System Address Support for V3 This bit sets the Host controller to support 64-bit System Addressing of V3 mode. SDMA cannot be used in 64-bit Addressing in Version 3 Mode. If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor can be enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 0) and DMA select (DMA_SEL = 11b). Values: - 0x0 (FALSE): 64-bit System Address for V3 is Not Supported - 0x1 (TRUE): 64-bit System Address for V3 is Supported Default Value: 0
27	SYS_ADDR_64_V4	64-bit System Address Support for V4 This bit sets the Host Controller to support 64-bit System Addressing of V4 mode. When this bit is set to 1, full or part of 64-bit address must be used to decode the Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller registers is effective regardless of setting to 64-bit Addressing in Host Control 2. If this bit is set to 1, 64-bit DMA Addressing for version 4 is enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 1) and by setting 64-bit Addressing (ADDRESSING =1) in the Host Control 2 register. SDMA can be used and ADMA2 uses 128-bit Descriptor. Values: - 0x0 (FALSE): 64-bit System Address for V4 is Not Supported - 0x1 (TRUE): 64-bit System Address for V4 is Supported Default Value: 0
26	VOLT_18	Voltage Support 1.8V Values: - 0x0 (FALSE): 1.8V Not Supported - 0x1 (TRUE): 1.8V Supported Default Value: 1
25	VOLT_30	Voltage Support 3.0V Values: - 0x0 (FALSE): 3.0V Not Supported - 0x1 (TRUE): 3.0V Supported Default Value: 1
24	VOLT_33	Voltage Support 3.3V Values: - 0x0 (FALSE): 3.3V Not Supported - 0x1 (TRUE): 3.3V Supported Default Value: 1
23	SUS_RES_SUPPORT	Suspense/Resume Support This bit indicates whether the Host Controller supports Suspend/Resume functionality. If this bit is 0, the Host Driver does not issue either Suspend or Resume commands because the Suspend and Resume mechanism is not supported. Values: - 0x0 (FALSE): Not Supported - 0x1 (TRUE): Supported Default Value: 0

23.1.29 SDHC0_CORE_CAPABILITIES1_R (continued)

22	SDMA_SUPPORT	SDMA Support This bit indicates whether the Host Controller is capable of using SDMA to transfer data between the system memory and the Host Controller directly. Values: - 0x0 (FALSE): SDMA not Supported - 0x1 (TRUE): SDMA Supported Default Value: 1
21	HIGH_SPEED_SUPPORT	High Speed Support This bit indicates whether the Host Controller and the Host System supports High Speed mode and they can supply the SD Clock frequency from 25 MHz to 50 MHz. Values: - 0x0 (FALSE): High Speed not Supported - 0x1 (TRUE): High Speed Supported Default Value: 1
19	ADMA2_SUPPORT	ADMA2 Support This bit indicates whether the Host Controller is capable of using ADMA2. Values: - 0x0 (FALSE): ADMA2 not Supported - 0x1 (TRUE): ADMA2 Supported Default Value: 1
18	EMBEDDED_8_BIT	8-bit Support for Embedded Device This bit indicates whether the Host Controller is capable of using an 8-bit bus width mode. This bit is not effective when the Slot Type is set to 10b. Values: - 0x0 (FALSE): 8-bit Bus Width not Supported - 0x1 (TRUE): 8-bit Bus Width Supported Default Value: 1
17 : 16	MAX_BLK_LEN	Maximum Block Length This bit indicates the maximum block size that the Host driver can read and write to the buffer in the Host Controller. The buffer transfers this block size without wait cycles. The transfer block length is always 512 bytes for the SD Memory irrespective of this bit. Value is fixed to (including the default value): 0x0: when MAX_BLK_SIZE=0 indicating 512 Bytes 0x1: when MAX_BLK_SIZE=1 indicating 1024 Bytes 0x2: Reserved 0x3: Reserved Default Value: 1

23.1.29 SDHC0_CORE_CAPABILITIES1_R (continued)

15 : 8	BASE_CLK_FREQ	Base Clock Frequency for SD clock These bits indicate the base (maximum) clock frequency for the SD Clock. The definition of these bits depend on the Host Controller Version. - 6-Bit Base Clock Frequency: This mode is supported by the Host Controller version 1.00 and 2.00. The upper 2 bits are not effective and are always 0. The unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz. - 0x00 - Get information through another method - 0x01 - 1 MHz - 0x02 - 2 MHz - ..... - 0x3F - 63 MHz - 0x40-0xFF - Not Supported - 8-Bit Base Clock Frequency: This mode is supported by the Host Controller version 3.00. The unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz. - 0x00 - Get information through another method - 0x01 - 1 MHz - 0x02 - 2 MHz - ..... - 0xFF - 255 MHz If the frequency is 16.5 MHz, the larger value is set to 0001001b (17 MHz) because the Host Driver uses this value to calculate the clock divider value and it does not exceed the upper limit of the SD Clock frequency. If these bits are all 0, the Host system has to get information using a different method. Default Value: 0x64
7	TOUT_CLK_UNIT	Timeout Clock Unit This bit shows the unit of base clock frequency used to detect Data TImeout Error. Values: - 0x0 (KHZ): KHz - 0x1 (MHZ): MHz Default Value: 1
5 : 0	TOUT_CLK_FREQ	Timeout Clock Frequency This bit shows the base clock frequency used to detect Data Timeout Error. The Timeout Clock unit defines the unit of timeout clock frequency. It can be KHz or MHz. - 0x00 - Get information through another method - 0x01 - 1KHz / 1MHz - 0x02 - 2KHz / 2MHz - 0x03 - 3KHz / 3MHz - ..... - 0x3F - 63KHz / 63MHz Default Value: 1

23.1.30 SDHC0_CORE_CAPABILITIES2_R

Description: Capabilities Register - 32 to 63

Address: 0x44811044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	R	R	R	R
HW Access	Reserved	R	R	R	R	R	R	R
Name	Reserved	DRV_-TYPED	DRV_-TYPEC	DRV_-TYPEA	UHS2_-SUPPORT	DDR50_-SUPPORT	SDR104_-SUPPORT	SDR50_-SUPPORT

Bits	15	14	13	12	11	10	9	8
SW Access	R		R	Reserved	R			
HW Access	R		R	Reserved	R			
Name	RE_TUNING_MODES [15:14]		USE_TUN-ING_S-DR50	Reserved	RETUNE_CNT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	CLK_MUL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R	R	Reserved		
HW Access	Reserved			R	R	Reserved		
Name	Reserved [31:29]			VDD2_18V_SUPPORT	ADMA3_-SUPPORT	Reserved [26:24]		

Bits	Name	Description
28	VDD2_18V_SUPPORT	1.8V VDD2 Support This bit indicates support of VDD2 for the Host System. Values: - 0x0 (FALSE): 1.8V VDD2 is not Supported - 0x1 (TRUE): 1.8V VDD2 is Supported Default Value: 0
27	ADMA3_SUPPORT	ADMA3 Support This bit indicates whether the Host Controller is capable of using ADMA3. Values: - 0x0 (FALSE): ADMA3 not Supported - 0x1 (TRUE): ADMA3 Supported Default Value: 1
23 : 16	CLK_MUL	Clock Multiplier These bits indicate the clock multiplier of the programmable clock generator. Setting these bits to 0 means that the Host Controller does not support a programmable clock generator. - 0x0: Clock Multiplier is not Supported - 0x1: Clock Multiplier M = 2 - 0x2: Clock Multiplier M = 3 - ..... - 0xFF: Clock Multiplier M = 256 Default Value: 0

23.1.30 SDHC0_CORE_CAPABILITIES2_R (continued)

15 : 14	RE_TUNING_MODES	Re-Tuning Modes (UHS-I only) These bits select the re-tuning method and limit the maximum data length. Values: - 0x0 (MODE1): Timer - 0x1 (MODE2): Timer and Re-Tuning Request (Not supported) - 0x2 (MODE3): Auto Re-Tuning (for transfer) - 0x3 (RSVD_MODE): Reserved Default Value: 0
13	USE_TUNING_SDR50	Use Tuning for SDR50 (UHS-I only) Values: - 0x0 (ZERO): SDR50 does not require tuning - 0x1 (ONE): SDR50 requires tuning Default Value: 0
11 : 8	RETUNE_CNT	Timer Count for Re-Tuning (UHS-I only) - 0x0: Re-Tuning Timer disabled - 0x1: 1 seconds - 0x2: 2 seconds - 0x3: 4 seconds - ..... - 0xB: 1024 seconds - 0xC: Reserved - 0xD: Reserved - 0xE: Reserved - 0xF: Get information from other source Default Value: 0
6	DRV_TYPED	Driver Type D Support (UHS-I only) This bit indicates support of Driver Type D for 1.8 Signaling. Values: - 0x0 (FALSE): Driver Type D is not supported - 0x1 (TRUE): Driver Type D is supported Default Value: 1
5	DRV_TYPEC	Driver Type C Support (UHS-I only) This bit indicates support of Driver Type C for 1.8 Signaling. Values: - 0x0 (FALSE): Driver Type C is not supported - 0x1 (TRUE): Driver Type C is supported Default Value: 1
4	DRV_TYPEA	Driver Type A Support (UHS-I only) This bit indicates support of Driver Type A for 1.8 Signaling. Values: - 0x0 (FALSE): Driver Type A is not supported - 0x1 (TRUE): Driver Type A is supported Default Value: 1
3	UHS2_SUPPORT	UHS-II Support (UHS-II only) This bit indicates whether Host Controller supports UHS-II. Values: - 0x0 (FALSE): UHS-II is not supported - 0x1 (TRUE): UHS-II is supported Default Value: 0
2	DDR50_SUPPORT	DDR50 Support (UHS-I only) Values: - 0x0 (FALSE): DDR50 is not supported - 0x1 (TRUE): DDR50 is supported Default Value: 1

23.1.30 SDHC0_CORE_CAPABILITIES2_R (continued)

1	SDR104_SUPPORT	SDR104 Support (UHS-I only) This bit mentions that SDR104 requires tuning. Values: - 0x0 (FALSE): SDR104 is not supported - 0x1 (TRUE): SDR104 is supported (NOT ACTUALLY SUPPORTED) Default Value: 1
0	SDR50_SUPPORT	SDR50 Support (UHS-I only) Thsi bit indicates that SDR50 is supported. The bit 13 (USE_TUNING_SDR50) indicates whether SDR50 requires tuning or not. Values: - 0x0 (FALSE): SDR50 is not supported - 0x1 (TRUE): SDR50 is supported Default Value: 1

23.1.31 SDHC0_CORE_CURR_CAPABILITIES1_R

Description: Current Capabilities Register - 0 to 31

Address: 0x44811048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	MAX_CUR_33V [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MAX_CUR_30V [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	MAX_CUR_18V [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	MAX_CUR_18V	Maximum Current for 1.8V This bit specifies the Maximum Current for 1.8V VDD1 power supply for the card. - 0: Get information through another method - 1: 4mA - 2: 8mA - 3: 13mA - ..... - 255: 1020mA Default Value: 0
15 : 8	MAX_CUR_30V	Maximum Current for 3.0V This bit specifies the Maximum Current for 3.0V VDD1 power supply for the card. - 0: Get information through another method - 1: 4mA - 2: 8mA - 3: 13mA - ..... - 255: 1020mA Default Value: 0

23.1.31 SDHC0_CORE_CURR_CAPABILITIES1_R (continued)

7 : 0	MAX_CUR_33V	Maximum Current for 3.3V This bit specifies the Maximum Current for 3.3V VDD1 power supply for the card. - 0: Get information through another method - 1: 4mA - 2: 8mA - 3: 13mA - ..... - 255: 1020mA Default Value: 0

23.1.32 SDHC0_CORE_CURR_CAPABILITIES2_R

Description: Maximum Current Capabilities Register - 32 to 63

Address: 0x4481104C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	MAX_CUR_VDD2_18V [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	MAX_CUR_VDD2_18V	Maximum Current for 1.8V VDD2 This bit specifies the Maximum Current for 1.8V VDD2 power supply for the UHS-II card. - 0: Get information through another method - 1: 4mA - 2: 8mA - 3: 13mA - ..... - 255: 1020mA Default Value: 0

23.1.33 SDHC0_CORE_FORCE_AUTO_CMD_STAT_R

Description: Force Event Register for Auto CMD Error Status register

Address: 0x44811050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	Reserved	W	W	W	W	W	W
HW Access	R	Reserved	R	R	R	R	R	R
Name	FORCE_CMD_NOT_ISSUED_AUTO_CMD12	Reserved	FORCE_AUTO_CMD_RESP_ERR	FORCE_AUTO_CMD_IDX_ERR	FORCE_AUTO_CMD_EBIT_ERR	FORCE_AUTO_CMD_CRC_ERR	FORCE_AUTO_CMD_TOUT_ERR	FORCE_AUTO_CMD12_NOT_EXEC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	Name	Description
7	FORCE_CMD_NOT_ISSUED_AUTO_CMD12	Force Event for Command Not Issued By Auto CMD12 Error Values: - 0x1 (TRUE): Command Not Issued By Auto CMD12 Error Status is set - 0x0 (FALSE): Not Affected Default Value: 0
5	FORCE_AUTO_CMD_RESP_ERR	Force Event for Auto CMD Response Error Values: - 0x1 (TRUE): Auto CMD Response Error Status is set - 0x0 (FALSE): Not Affected Default Value: 0
4	FORCE_AUTO_CMD_IDX_ERR	Force Event for Auto CMD Index Error Values: - 0x1 (TRUE): Auto CMD Index Error Status is set - 0x0 (FALSE): Not Affected Default Value: 0
3	FORCE_AUTO_CMD_EBIT_ERR	Force Event for Auto CMD End Bit Error Values: - 0x1 (TRUE): Auto CMD End Bit Error Status is set - 0x0 (FALSE): Not Affected Default Value: 0
2	FORCE_AUTO_CMD_CRC_ERR	Force Event for Auto CMD CRC Error Values: - 0x1 (TRUE): Auto CMD CRC Error Status is set - 0x0 (FALSE): Not Affected Default Value: 0
1	FORCE_AUTO_CMD_TOUT_ERR	Force Event for Auto CMD Timeout Error Values: - 0x1 (TRUE): Auto CMD Timeout Error Status is set - 0x0 (FALSE): Not Affected Default Value: 0
0	FORCE_AUTO_CMD12_NOT_EXEC	Force Event for Auto CMD12 Not Executed Values: - 0x1 (TRUE): Auto CMD12 Not Executed Status is set - 0x0 (FALSE): Not Affected Default Value: 0

23.1.34 SDHC0_CORE_FORCE_ERROR_INT_STAT_R

Description: Force Event Register for Error Interrupt Status

Address: 0x44811052

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	FORCE_CUR_LMT_ERR	FORCE_-DATA_END_BIT_ERR	FORCE_-DATA_CRC_ERR	FORCE_-DATA_TOUT_ERR	FORCE_C-MD_IDX-_ERR	FORCE_C-MD_END_BIT_ERR	FORCE_C-MD_CRC_ERR	FORCE_C-MD_TOUT_ERR

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	FORCE_VENDOR_ERR3	FORCE_VENDOR_ERR2	FORCE_VENDOR_ERR1	FORCE_-BOOT_ACK_ERR	FORCE_RESP_ERR	FORCE_TUNING_ERR	FORCE_ADMA_ERR	FORCE_AUTO_CM-D_ERR

Bits	Name	Description
15	FORCE_VENDOR_ERR3	This bit (FORCE_VENDOR_ERR3) of the FORCE_ERROR_INT_STAT_R register is reserved. It always returns 0. Default Value: 0
14	FORCE_VENDOR_ERR2	This bit (FORCE_VENDOR_ERR2) of the FORCE_ERROR_INT_STAT_R register is reserved. It always returns 0. Default Value: 0
13	FORCE_VENDOR_ERR1	This bit (FORCE_VENDOR_ERR1) of the FORCE_ERROR_INT_STAT_R register is reserved. It always returns 0. Default Value: 0
12	FORCE_-BOOT_ACK_ERR	Force Event for Boot Ack error Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Boot ack Error Status is set Default Value: 0
11	FORCE_RESP_ERR	Force Event for Response Error (SD Mode only) Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Response Error Status is set Default Value: 0
10	FORCE_TUNING_ERR	Force Event for Tuning Error (UHS-I Mode only) Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Tuning Error Status is set Default Value: 0
9	FORCE_ADMA_ERR	Force Event for ADMA Error Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): ADMA Error Status is set Default Value: 0

23.1.34 SDHC0_CORE_FORCE_ERROR_INT_STAT_R (continued)

8	FORCE_AUTO_CMD_ERR	Force Event for Auto CMD Error (SD/eMMC Mode only) Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Auto CMD Error Status is set Default Value: 0
7	FORCE_CUR_LMT_ERR	Force Event for Current Limit Error Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Current Limit Error Status is set Default Value: 0
6	FORCE_DATA_END_BIT_ERR	Force Event for Data End Bit Error (SD/eMMC Mode only) Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Data End Bit Error Status is set Default Value: 0
5	FORCE_DATA_CRC_ERR	Force Event for Data CRC Error (SD/eMMC Mode only) Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Data CRC Error Status is set Default Value: 0
4	FORCE_DATA_TOUT_ERR	Force Event for Data Timeout Error (SD/eMMC Mode only) Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Data Timeout Error Status is set Default Value: 0
3	FORCE_CMD_IDX_ERR	Force Event for Command Index Error (SD/eMMC Mode only) Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Command Index Error Status is set Default Value: 0
2	FORCE_CMD_END_BIT_ERR	Force Event for Command End Bit Error (SD/eMMC Mode only) Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Command End Bit Error Status is set Default Value: 0
1	FORCE_CMD_CRC_ERR	Force Event for Command CRC Error (SD/eMMC Mode only) Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Command CRC Error Status is set Default Value: 0
0	FORCE_CMD_TOUT_ERR	Force Event for Command Timeout Error (SD/eMMC Mode only) Values: - 0x0 (FALSE): Not Affected - 0x1 (TRUE): Command Timeout Error Status is set Default Value: 0

23.1.35 SDHC0_CORE_ADMA_ERR_STAT_R

Description: ADMA Error Status Register

Address: 0x44811054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R	R	
HW Access	Reserved					RW	RW	
Name	Reserved [7:3]					ADMA_LEN_ERR	ADMA_ERR_STATES [1:0]	

Bits	Name	Description
2	ADMA_LEN_ERR	ADMA Length Mismatch Error States This error occurs in the following instances: - While the Block Count Enable is being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length - When the total data length cannot be divided by the block length Values: - 0x0 (NO_ERR): No Error - 0x1 (ERROR): Error Default Value: 0
1 : 0	ADMA_ERR_STATES	ADMA Error States These bits indicate the state of ADMA when an error occurs during ADMA data transfer. Values: - 0x0 (ST_STOP): Stop DMA - SYS_ADR register points to a location next to the error descriptor - 0x1 (ST_FDS): Fetch Descriptor - SYS_ADR register points to the error descriptor - 0x2 (UNUSED): Never set this state - 0x3 (ST_TFR): Transfer Data - SYS_ADR register points to a location next to the error descriptor Default Value: 0

23.1.36 SDHC0_CORE_ADMA_SA_LOW_R

Description: ADMA System Address Register - Low

Address: 0x44811058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADMA_SA_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADMA_SA_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADMA_SA_LOW [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADMA_SA_LOW [31:24]							

Bits	Name	Description
31 : 0	ADMA_SA_LOW	ADMA System Address These bits indicate the lower 32 bits of the ADMA system address. - SDMA: If Host Version 4 Enable is set to 1, this register stores the system address of the data location - ADMA2: This register stores the byte address of the executing command of the descriptor table - ADMA3: This register is set by ADMA3. ADMA2 increments the address of this register that points to the next line, every time a Descriptor line is fetched. Default Value: 0

23.1.37 SDHC0_CORE_ADMA_ID_LOW_R

Description: ADMA3 Integrated Descriptor Address Register - Low

Address: 0x44811078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADMA_ID_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADMA_ID_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADMA_ID_LOW [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADMA_ID_LOW [31:24]							

Bits	Name	Description
31 : 0	ADMA_ID_LOW	ADMA Integrated Descriptor Address These bits indicate the lower 32-bit of the ADMA Integrated Descriptor address. The start address of Integrated Descriptor is set to these register bits. The ADMA3 fetches one Descriptor Address and increments these bits to indicate the next Descriptor address. Default Value: 0

23.1.38 SDHC0_CORE_HOST_CNTRL_VERS_R

Description: Host Controller Version

Address: 0x448110FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SPEC_VERSION_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VENDOR_VERSION_NUM [15:8]							

Bits	Name	Description
15 : 8	VENDOR_VERSION_-NUM	Vendor Version Number This field is reserved for the vendor version number. Host Driver must not use this status. Default Value: 0
7 : 0	SPEC_VERSION_NUM	Specification Version Number These bits indicate the Host controller specification version. The upper and lower 4-bits indicate the version. Values 0x06-0xFF are reserved. Values: - 0x0 (VER_1_00): SD Host Controller Specification Version 1.00 - 0x1 (VER_2_00): SD Host Controller Specification Version 2.00 - 0x2 (VER_3_00): SD Host Controller Specification Version 3.00 - 0x3 (VER_4_00): SD Host Controller Specification Version 4.00 - 0x4 (VER_4_10): SD Host Controller Specification Version 4.10 - 0x5 (VER_4_20): SD Host Controller Specification Version 4.20 Default Value: 5

23.1.39 SDHC0_CORE_CQVER

Description: Command Queuing Version register

Address: 0x44811180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	EMMC_VER_MINOR [7:4]				EMMC_VER_SUFFIX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R			
HW Access	Reserved				R			
Name	Reserved [15:12]				EMMC_VER_MAJOR [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11 : 8	EMMC_VER_MAJOR	This bit indicates the eMMC major version (1st digit left of decimal point) in BCD format. Default Value: 5
7 : 4	EMMC_VER_MINOR	This bit indicates the eMMC minor version (1st digit right of decimal point) in BCD format. Default Value: 1
3 : 0	EMMC_VER_SUFFIX	This bit indicates the eMMC version suffix (2nd digit right of decimal point) in BCD format. Default Value: 0

23.1.40 SDHC0_CORE_CQCAP

Description: Command Queuing Capabilities register

Address: 0x44811184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	ITCFVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				Reserved		R	
HW Access	R				Reserved		R	
Name	ITCFMUL [15:12]				Reserved [11:10]		ITCFVAL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R	Reserved			
HW Access	Reserved			R	Reserved			
Name	Reserved [31:29]			CRYPTO_-SUPPORT	Reserved [27:24]			

Bits	Name	Description
28	CRYPTO_SUPPORT	Crypto Support This bit indicates whether the Host Controller supports cryptographic operations. Values: - 0x0 (FALSE): Crypto not Supported - 0x1 (TRUE): Crypto Supported Default Value: 0
15 : 12	ITCFMUL	Internal Timer Clock Frequency Multiplier (ITCFMUL) This field indicates the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. See ITCFVAL definition for details. Values 0x5 to 0xF are reserved. Values: - 0x0 (CLK_1KHz): 1KHz clock - 0x1 (CLK_10KHz): 10KHz clock - 0x2 (CLK_100KHz): 100KHz clock - 0x3 (CLK_1MHz): 1MHz clock - 0x4 (CLK_10MHz): 10MHz clock Value After Reset: DWC_MSHC_CQE_TIMER_CLK_FMUL for DWC_MSHC cfg11 the value is constant = 0x1 Default Value: 1
9 : 0	ITCFVAL	Internal Timer Clock Frequency Value (ITCFVAL) This field scales the frequency of the timer clock provided by ITCFMUL. The Final clock frequency of actual timer clock is calculated as ITCFVAL* ITCFMUL. Default Value: 0xC8

23.1.41 SDHC0_CORE_CQCFG

Description: Command Queuing Configuration register

Address: 0x44811188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						CR_GEN-ERAL_EN	CQ_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [15:13]			DCMD_EN	Reserved [11:9]			TASK_-DESC_-SIZE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12	DCMD_EN	This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a data transfer descriptor or a direct-command descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Values: - 0x1 (SLOT31_DCMD_ENABLE): Task descriptor in slot #31 is a DCMD Task Descriptor - 0x0 (SLOT31_DCMD_DISABLE): Task descriptor in slot #31 is a data Transfer Task Descriptor Default Value: 0
8	TASK_DESC_SIZE	Bit Value Description This bit indicates the size of task descriptor used in host memory. This bit can only be configured when Command Queuing Enable bit is 0 (command queuing is disabled). Values: - 0x1 (TASK_DESC_128b): Task descriptor size is 128 bits - 0x0 (TASK_DESC_64b): Task descriptor size is 64 bits Default Value: 0

23.1.41 SDHC0_CORE_CQCFG (continued)

1	CR_GENERAL_EN	Crypto General Enable Enable/Disable bit for Crypto Engine. If cryptographic operations are not supported, this status bit is reserved. Values: - 0x1 (ENABLE): Enable cryptographic operations for transactions where TD.CE=1 or CRNQP.CE=1 - 0x0 (DISABLE): Disable cryptographic operations for all transactions Bit only available if DWC_MSHC_CRYPTO_SUPPORT = 1 Default Value: 0
0	CQ_EN	Enable command queuing engine (CQE). When CQE is disable, the software controls the eMMC bus using the registers between the addresses 0x000 to 0x1FF. Before the software writes to this bit, the software verifies that the eMMC host controller is in idle state and there are no ongoing commands or data transfers. When software wants to exit command queuing mode, it clears all previous tasks (if any) before setting this bit to 0. Values: - 0x1 (CQE_ENABLE): Enable command queuing - 0x0 (CQE_DISABLE): Disable command queuing Default Value: 0

23.1.42 SDHC0_CORE_CQCTL

Description: Command Queuing Control register

Address: 0x4481118C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							RW
Name	Reserved [7:1]							HALT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							RW
Name	Reserved [15:9]							CL-R_ALL_TASKS

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	CLR_ALL_TASKS	Clear all tasks This bit can only be written when the controller is halted. This bit does not clear tasks in the device. The software has to use the CMDQ_TASK_MGMT command to clear device's queue. Values: - 0x1 (CLEAR_ALL_TASKS): Clears all the tasks in the controller - 0x0 (NO_EFFECT): Programming 0 has no effect Default Value: 0
0	HALT	Halt request and resume Values: - 0x1 (HALT_CQE): Software writes 1 to this bit when it wants to acquire software control over the eMMC bus and to disable CQE from issuing command on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT). When the software writes 1, CQE completes the ongoing task (if any in progress). After the task is completed and the CQE is in idle state, CQE does not issue new commands and indicates to the software by setting this bit to 1. The software can poll on this bit until it is set to 1 and only then send commands on the eMMC bus. - 0x0 (RESUME_CQE): Software writes 0 to this bit to exit from the halt state and resume CQE activity. Default Value: 0

23.1.43 SDHC0_CORE_CQIS

Description: Command Queuing Interrupt Status register

Address: 0x44811190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [7:6]		ICCE	GCE	TCL	RED	TCC	HAC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	ICCE	Invalid Crypto Configuration Error If cryptographic operations is supported by host controller (CQCAP.CS=1) and (CQCFG.GCE=1); and encryption/decryption is enabled (TD.CE=1), this status bit is asserted (if CQISE.ICCE_STE=1) if either of the below conditions are met. - CRYPTOCFG disabled (CRYPTOCFG_i_16[TD.CCI].CFGE_i=0) OR nonexistent (TD.CCI>=CRCAP.CFGC) - Capability index in Configuration (CRYPTOCFG_i_16[TD.CCI].CAPIDX_i) is greater than maximum number of capabilities supported (CAPIDX_i > CRCAP.CC) - Data unit size in Configuration (CRYPTOCFG_i_16[TD.CCI].DUSIZE_i) is not supported by selected capability (CRYPTOCAP_x[CAPIDX_i].SDUSB) If cryptographic operations are not supported, this status bit is reserved. Values: - 0x1 (SET): ICCE interrupt is set - 0x0 (UNSET): ICCE interrupt is not set Bit only available if DWC_MSHC_CRYPTO_SUPPORT = 1 Default Value: 0

23.1.43 SDHC0_CORE_CQIS (continued)

4	GCE	General Crypto Error If cryptographic operations is supported by host controller (CQCAP.CS=1) and (CQCFG.GCE=1); and encryption/decryption is enabled (TD.CE=1), this status bit is asserted (if CQISE.GCE_STE=1) when the crypto hardware encounters any of the following error in the processing of a transaction. - Block size is not multiple of 16 bytes - Total transfer length (Block size * Block count) is not an integral multiple of DUSize - Device data block transfer starting address is not aligned to DUSize - CQE task descriptor data transfer length is not multiple of 16 bytes If cryptographic operations are not supported, this status bit is reserved. Values: - 0x1 (SET): GCE interrupt is set - 0x0 (UNSET): GCE interrupt is not set Bit only available if DWC_MSHC_CRYPTO_SUPPORT = 1 Default Value: 0
3	TCL	Task cleared interrupt This status bit is asserted (if CQISE.TCL_STE=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (by writing CQTCLR) or clearing of all tasks (by writing CQCTL). A value of 1 clears this status bit. Values: - 0x1 (SET): TCL Interrupt is set - 0x0 (NOTSET): TCL Interrupt is not set Default Value: 0
2	RED	Response error detected interrupt This status bit is asserted (if CQISE.RED_STE=1) when a response is received with an error bit set in the device status field. Configure the CQRMEM register to identify device status bit fields that may trigger an interrupt and that are masked. A value of 1 clears this status bit. Values: - 0x1 (SET): RED Interrupt is set - 0x0 (NOTSET): RED Interrupt is not set Default Value: 0
1	TCC	Task complete interrupt This status bit is asserted (if CQISE.TCC_STE=1) when at least one of the following conditions are met: - A task is completed and the INT bit is set in its Task Descriptor - Interrupt caused by Interrupt Coalescing logic due to timeout - Interrupt Coalescing logic reached the configured threshold A value of 1 clears this status bit Values: - 0x1 (SET): TCC Interrupt is set - 0x0 (NOTSET): TCC Interrupt is not set Default Value: 0

23.1.43 SDHC0_CORE_CQIS (continued)

0	HAC	Halt complete interrupt This status bit is asserted (only if CQISE.HAC_STE=1) when halt bit in the CQCTL register transitions from 0 to 1 indicating that the host controller has completed its current ongoing task and has entered halt state. A value of 1 clears this status bit. Values: - 0x1 (SET): HAC Interrupt is set - 0x0 (NOTSET): HAC Interrupt is not set Default Value: 0

23.1.44 SDHC0_CORE_CQISE

Description: Command Queuing Interrupt Status Enable register

Address: 0x44811194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		ICCE_STE	GCE_STE	TCL_STE	RED_STE	TCC_STE	HAC_STE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	ICCE_STE	Invalid Crypto Configuration Error interrupt status enable Values: - 0x1 (INT_STS_ENABLE): CQIS.ICCE is set when its interrupt condition is active - 0x0 (INT_STS_DISABLE): CQIS.ICCE is disabled Bit only available if DWC_MSHC_CRYPTO_SUPPORT = 1 Default Value: 0
4	GCE_STE	General Crypto Error interrupt status enable Values: - 0x1 (INT_STS_ENABLE): CQIS.GCE is set when its interrupt condition is active - 0x0 (INT_STS_DISABLE): CQIS.GCE is disabled Bit only available if DWC_MSHC_CRYPTO_SUPPORT = 1 Default Value: 0
3	TCL_STE	Task cleared interrupt status enable Values: - 0x1 (INT_STS_ENABLE): CQIS.TCL is set when its interrupt condition is active - 0x0 (INT_STS_DISABLE): CQIS.TCL is disabled Default Value: 0
2	RED_STE	Response error detected interrupt status enable Values: - 0x1 (INT_STS_ENABLE): CQIS.RED is set when its interrupt condition is active - 0x0 (INT_STS_DISABLE): CQIS.RED is disabled Default Value: 0

23.1.44 SDHC0_CORE_CQISE (continued)

1	TCC_STE	Task complete interrupt status enable Values: - 0x1 (INT_STS_ENABLE): CQIS.TCC is set when its interrupt condition is active - 0x0 (INT_STS_DISABLE): CQIS.TCC is disabled Default Value: 0
0	HAC_STE	Halt complete interrupt status enable Values: - 0x1 (INT_STS_ENABLE): CQIS.HAC is set when its interrupt condition is active - 0x0 (INT_STS_DISABLE): CQIS.HAC is disabled Default Value: 0

23.1.45 SDHC0_CORE_CQISGE

Description: Command Queuing Interrupt signal enable register

Address: 0x44811198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [7:6]		ICCE_SGE	GCE_SGE	TCL_SGE	RED_SGE	TCC_SGE	HAC_SGE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	ICCE_SGE	Invalid Crypto Configuration Error interrupt signal enable Values: - 0x1 (INT_SIG_ENABLE): CQIS.ICCE interrupt signal generation is active - 0x0 (INT_SIG_DISABLE): CQIS.ICCE interrupt signal generation is disabled Bit only available if DWC_MSHC_CRYPTO_SUPPORT = 1 Default Value: 0
4	GCE_SGE	General Crypto Error interrupt signal enable Values: - 0x1 (INT_SIG_ENABLE): CQIS.GCE interrupt signal generation is active - 0x0 (INT_SIG_DISABLE): CQIS.GCE interrupt signal generation is disabled Bit only available if DWC_MSHC_CRYPTO_SUPPORT = 1 Default Value: 0
3	TCL_SGE	Task cleared interrupt signal enable Values: - 0x1 (INT_SIG_ENABLE): CQIS.TCL interrupt signal generation is active - 0x0 (INT_SIG_DISABLE): CQIS.TCL interrupt signal generation is disabled Default Value: 0

23.1.45 SDHC0_CORE_CQISGE (continued)

2	RED_SGE	Response error detected interrupt signal enable Values: - 0x1 (INT_SIG_ENABLE): CQIS.RED interrupt signal generation is active - 0x0 (INT_SIG_DISABLE): CQIS.RED interrupt signal generation is disabled Default Value: 0
1	TCC_SGE	Task complete interrupt signal enable Values: - 0x1 (INT_SIG_ENABLE): CQIS.TCC interrupt signal generation is active - 0x0 (INT_SIG_DISABLE): CQIS.TCC interrupt signal generation is disabled Default Value: 0
0	HAC_SGE	Halt complete interrupt signal enable Values: - 0x1 (INT_SIG_ENABLE): CQIS.HAC interrupt signal generation is active - 0x0 (INT_SIG_DISABLE): CQIS.HAC interrupt signal generation is disabled Default Value: 0

23.1.46 SDHC0_CORE_CQIC

Description: Command Queuing Interrupt Coalescing register

Address: 0x4481119C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	RW						
HW Access	R	R						
Name	TOUT_VAL_WEN	TOUT_VAL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	W	Reserved		W				
HW Access	R	Reserved		R				
Name	INTC_TH_WEN	Reserved [14:13]		INTC_TH [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			R	Reserved			W
HW Access	Reserved			R	Reserved			R
Name	Reserved [23:21]			INTC_STAT	Reserved [19:17]			INTC_RST

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	INTC_EN	Reserved [30:24]						

Bits	Name	Description
31	INTC_EN	Interrupt Coalescing Enable Bit Values: - 0x1 (ENABLE_INT_COALESCING): Interrupt coalescing mechanism is active. Interrupts are counted and timed, and coalesced interrupts are generated - 0x0 (DISABLE_INT_COALESCING): Interrupt coalescing mechanism is disabled (Default). Default Value: 0
20	INTC_STAT	Interrupt Coalescing Status Bit This bit indicates to the software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (that is, this is set if and only if INTC counter > 0). Values: - 0x1 (INTC_ATLEAST1_COMP): At least one INT0 task completion has been counted (INTC counter > 0) - 0x0 (INTC_NO_TASK_COMP): INT0 Task completions have not occurred since last counter reset (INTC counter == 0) Default Value: 0

23.1.46 SDHC0_CORE_CQIC (continued)

16	INTC_RST	Counter and Timer Reset When host driver writes 1, the interrupt coalescing timer and counter are reset. Values: - 0x1 (ASSERT_INTC_RESET): Interrupt coalescing timer and counter are reset - 0x0 (NO_EFFECT): No Effect Default Value: 0
15	INTC_TH_WEN	Interrupt Coalescing Counter Threshold Write Enable When software writes 1 to this bit, the value INTC_TH is updated with the contents written on the same cycle. Values: - 0x1 (WEN_SET): Sets INTC_TH_WEN - 0x0 (WEN_CLR): Clears INTC_TH_WEN Default Value: 0
12 : 8	INTC_TH	Interrupt Coalescing Counter Threshold filed Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor), which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in INTC_TH, and generates interrupt. - 0x0: Interrupt coalescing feature disabled - 0x1: Interrupt coalescing interrupt generated after 1 task when INT=0 completes - 0x2: Interrupt coalescing interrupt generated after 2 tasks when INT=0 completes - ..... - 0x1f: Interrupt coalescing interrupt generated after 31 tasks when INT=0 completes To write to this field, the INTC_TH_WEN bit must be set during the same write operation. Default Value: 0
7	TOUT_VAL_WEN	When software writes 1 to this bit, the value TOUT_VAL is updated with the contents written on the same cycle. Values: - 0x1 (WEN_SET): Sets TOUT_VAL_WEN - 0x0 (WEN_CLR): clears TOUT_VAL_WEN Default Value: 0
6 : 0	TOUT_VAL	Interrupt Coalescing Timeout Value Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when the first data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field, it generates an interrupt and stops. The timer's unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. - 0x0: Timer is disabled. Timeout-based interrupt is not generated - 0x1: Timeout on 01x1024 cycles of timer clock frequency - 0x2: Timeout on 02x1024 cycles of timer clock frequency - ..... - 0x7f: Timeout on 127x1024 cycles of timer clock frequency In order to write to this field, the TOUT_VAL_WEN bit must be set at the same write operation. Default Value: 0

23.1.47 SDHC0_CORE_CQTDLBA

Description: Command Queuing Task Descriptor List Base Address register

Address: 0x448111A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TDLBA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TDLBA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	TDLBA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	TDLBA [31:24]							

Bits	Name	Description
31 : 0	TDLBA	This register stores the LSB bits (31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by the host driver. This address is set on 1 KB boundary. The lower 10 bits of this register are set to 0 by the software and are ignored by CQE. Default Value: 0

23.1.48 SDHC0_CORE_CQTDBR

Description: Command Queuing DoorBell register

Address: 0x448111A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DBR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DBR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DBR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DBR [31:24]							

Bits	Name	Description
31 : 0	DBR	The software configures TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. Writing 0 by the software does not have any impact on the hardware, and does not change the value of the register bit. CQE always processes tasks according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: - A task execution is completed (with success or error). - The task is cleared using CQTCLR register. - All tasks are cleared using CQCTL register. - CQE is disabled using CQCFG register. Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission, CQE processes the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution is based on said processing order. Default Value: 0

23.1.49 SDHC0_CORE_CQTCN

Description: Command Queuing TaskClear Notification register

Address: 0x448111AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	TCN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	TCN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	TCN [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	TCN [31:24]							

Bits	Name	Description
31 : 0	TCN	Task Completion Notification Each of the 32 bits are bit mapped to the 32 tasks. - Bit-N(1): Task-N has completed execution (with success or errors) - Bit-N(0): Task-N has not completed, could be pending or not submitted. On task completion, software may read this register to know tasks that have completed. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits. Default Value: 0

23.1.50 SDHC0_CORE_CQDQS

Description: Device queue status register

Address: 0x448111B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DQS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DQS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DQS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DQS [31:24]							

Bits	Name	Description
31 : 0	DQS	Device Queue Status Each of the 32 bits are bit mapped to the 32 tasks. - Bit-N(1): Device has marked task N as ready for execution - Bit-N(0): Task-N is not ready for execution. This task could be pending in device or not submitted. Host controller updates this register with response of the Device Queue Status command. Default Value: 0

23.1.51 SDHC0_CORE_CQDPT

Description: Device pending tasks register

Address: 0x448111B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DPT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DPT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DPT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DPT [31:24]							

Bits	Name	Description
31 : 0	DPT	Device-Pending Tasks Each of the 32 bits are bit mapped to the 32 tasks. - Bit-N(1): Task-N has been successfully queued into the device and is awaiting execution - Bit-N(0): Task-N is not yet queued. Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task has not been executed. The controller sets this bit after receiving a successful response for CMD45. CQE clears this bit after the task has completed execution. Software reads this register in the task-discard procedure to determine if the task is queued in the device. Default Value: 0

23.1.52 SDHC0_CORE_CQTCLR

Description: Command Queuing DoorBell register

Address: 0x448111B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TCLR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TCLR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	TCLR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	TCLR [31:24]							

Bits	Name	Description
31 : 0	TCLR	Writing 1 to bit n of this register orders CQE to clear a task that the software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCFG register Halt bit. When software writes 1 to a bit in this register, CQE updates the value to 1, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDBR once the clear operation is complete. Software must poll on the CQTCLR until it is cleared to verify that a clear operation was done. Default Value: 0

23.1.53 SDHC0_CORE_CQSSC1

Description: CQ Send Status Configuration 1 register

Address: 0x448111C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SQSCMD_IDLE_TMR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SQSCMD_IDLE_TMR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				SQSCMD_BLK_CNT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 16	SQSCMD_BLK_CNT	This field indicates when SQS CMD is sent while data transfer is in progress. A value of 'n' indicates that CQE sends status command on the CMD line, during the transfer of data block BLOCK_CNTn, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. - 0x0: SEND_QUEUE_STATUS (CMD13) command is not sent during the transaction. Instead, it is sent only when the data lines are idle. - 0x1: SEND_QUEUE_STATUS command is to be sent during the last block of the transaction. - 0x2: SEND_QUEUE_STATUS command when last 2 blocks are pending. - 0x3: SEND_QUEUE_STATUS command when last 3 blocks are pending. - ..... - 0xf: SEND_QUEUE_STATUS command when last 15 blocks are pending. Should be programmed only when CQCFG.CQ_EN is '0' Default Value: 0x1

23.1.53 SDHC0_CORE_CQSSC1 (continued)

15 : 0	SQSCMD_IDLE_TMR	This field configures the polling period to be used when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicates that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0001h (1 clock period) and the maximum value is FFFFh (65535 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 1000h, the calculated polling period is 4096*52.08 ns= 213.33 ns. Should be programmed only when CQCFG.CQ_EN is '0'. Default Value: 0x1000

23.1.54 SDHC0_CORE_CQSSC2

Description: CQ Send Status Configuration 2 register

Address: 0x448111C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SQSCMD_RCA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SQSCMD_RCA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	SQSCMD_RCA	This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE copies this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS (CMD13) command. Default Value: 0

23.1.55 SDHC0_CORE_CQCRDCT

Description: Command response for direct command register

Address: 0x448111C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DCMD_RESP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DCMD_RESP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DCMD_RESP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DCMD_RESP [31:24]							

Bits	Name	Description
31 : 0	DCMD_RESP	This register contains the response of the command generated by the last direct command (DCMD) task that was sent. Contents of this register are valid only after bit 31 of CQTDBR register is cleared by the controller. Default Value: 0

23.1.56 SDHC0_CORE_CQRMEM

Description: Command response mode error mask register

Address: 0x448111D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RESP_ERR_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RESP_ERR_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RESP_ERR_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RESP_ERR_MASK [31:24]							

Bits	Name	Description
31 : 0	RESP_ERR_MASK	The bits of this field are bit mapped to the device response. This bit is used as an interrupt mask on the device status filed that is received in R1/R1b responses. - 1: When a R1/R1b response is received, with a bit i in the device status set, a RED interrupt is generated. - 0: When a R1/R1b response is received, bit i in the device status is ignored. The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status. Note: Responses to CMD13 (SQS) encode the QSR so that they are ignored by this logic. Default Value: 0xFDF9A080

23.1.57 SDHC0_CORE_CQTERRI

Description: CQ Task Error Information register

Address: 0x448111D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [7:6]		RESP_ERR_CMD_INDX [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R	Reserved		R				
HW Access	RW	Reserved		RW				
Name	RESP_ER-R_-FIELDS_VALID	Reserved [14:13]		RESP_ERR_TASKID [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [23:22]		TRANS_ERR_CMD_INDX [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved		R				
HW Access	RW	Reserved		RW				
Name	TRANS_ERR_-FIELDS_VALID	Reserved [30:29]		TRANS_ERR_TASKID [28:24]				

Bits	Name	Description
31	TRANS_ERR_-FIELDS_VALID	This bit is updated when an error is detected while a data transfer transaction was in progress. Values: - 0x1 (SET): data transfer related error detected. Check contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX fields - 0x0 (NOT_SET): Ignore contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX Default Value: 0
28 : 24	TRANS_ERR_TASKID	This field captures the ID of the task that was executed and whose data transfer has errors. Default Value: 0
21 : 16	TRANS_ERR_CMD_INDX	This field captures the index of the command that was executed and whose data transfer has errors. Default Value: 0

23.1.57 SDHC0_CORE_CQTERRI (continued)

15	RESP_ERR_-FIELDS_VALID	This bit is updated when an error is detected while a command transaction was in progress. Values: - 0x1 (SET): Response-related error is detected. Check contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX fields - 0x0 (NOT_SET): Ignore contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX Default Value: 0
12 : 8	RESP_ERR_TASKID	This field captures the ID of the task which was executed on the command line when the error occurred. Default Value: 0
5 : 0	RESP_ERR_CMD_INDX	This field captures the index of the command that was executed on the command line when the error occurred. Default Value: 0

23.1.58 SDHC0_CORE_CQCRI

Description: CQ Command response index

Address: 0x448111D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [7:6]		CMD_RESP_INDX [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	CMD_RESP_INDX	Last Command Response index This field stores the index of the last received command response. Controller updates the value every time a command response is received. Default Value: 0

23.1.59 SDHC0_CORE_CQCRA

Description: CQ Command response argument register

Address: 0x448111DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CMD_RESP_ARG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CMD_RESP_ARG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CMD_RESP_ARG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	CMD_RESP_ARG [31:24]							

Bits	Name	Description
31 : 0	CMD_RESP_ARG	Last Command Response argument This field stores the argument of the last received command response. Controller updates the value every time a command response is received. Default Value: 0

23.1.60 SDHC0_CORE_MSHC_VER_ID_R

Description: MSHC version

Address: 0x44811500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	MSHC_VER_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MSHC_VER_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	MSHC_VER_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	MSHC_VER_ID [31:24]							

Bits	Name	Description
31 : 0	MSHC_VER_ID	Current release number This field indicates the Synopsys DesignWare Cores DWC_mshc/DWC_mshc_lite current release number that is read by an application. For example, release number "1.60a" is represented in ASCII as 0x313630. Lower 8 bits read from this register can be ignored by the application. An application reading this register in conjunction with the MSHC_VER_TYPE_R register, gathers details of the current release. Default Value: 0x3137302A

23.1.61 SDHC0_CORE_MSHC_VER_TYPE_R

Description: MSHC version type

Address: 0x44811504

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	MSHC_VER_TYPE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MSHC_VER_TYPE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	MSHC_VER_TYPE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	MSHC_VER_TYPE [31:24]							

Bits	Name	Description
31 : 0	MSHC_VER_TYPE	Current release type This field indicates the Synopsys DesignWare Cores DWC_mshc/DWC_mshc_lite current release type that is read by an application. For example, release type is "ga" is represented in ASCII as 0x6761. Lower 16 bits read from this register can be ignored by the application. An application reading this register in conjunction with the MSHC_VER_ID_R register, gathers details of the current release. Default Value: 0x67612A2A

23.1.62 SDHC0_CORE_MSHC_CTRL_R

Description: MSHC Control register

Address: 0x44811508

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	Reserved			RW
HW Access	Reserved			R	Reserved			R
Name	Reserved [7:5]			SW_CG_DIS	Reserved [3:1]			CMD_CONFLICT_CHECK

Bits	Name	Description
4	SW_CG_DIS	Internal clock gating disable control This bit must be used to disable IP's internal clock gating when required. when disabled clocks are not gated. Clocks to the core (except hclk) must be stopped when programming this bit. Values: - 0x0 (ENABLE): Internal clock gates are active and clock gating is controlled internally - 0x1 (DISABLE): Internal clock gating is disabled, clocks are not gated internally Default Value: 0
0	CMD_CONFLICT_CHECK	Command conflict check This bit enables command conflict check. Note: DWC_mshc controller monitors the CMD line whenever a command is issued and checks whether the value driven on sd_cmd_out matches the value on sd_cmd_in at next subsequent edge of cclk_tx to determine command conflict error. This bit is cleared only if the feed back delay (including IO Pad delay) is more than (t_card_clk_period - t_setup), where t_setup is the setup time of a flop in DWC_mshc. The I/O pad delay is consistent across CMD and DATA lines, and it is within the value: (2*t_card_clk_period - t_setup) Values: - 0x0 (DISABLE_CMD_CONFLICT_CHK): Disable command conflict check - 0x1 (CMD_CONFLICT_CHK_LAT1): Check for command conflict after 1 card clock cycle Default Value: 1

23.1.63 SDHC0_CORE_MBIU_CTRL_R

Description: MBIU Control register

Address: 0x44811510

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				BURST_IN-CR16_EN	BURST_IN-CR8_EN	BURST_IN-CR4_EN	UNDE-FL_IN-CR_EN

Bits	Name	Description
3	BURST_INCR16_EN	INCR16 Burst Controls generation of INCR16 transfers on Master interface. Values: - 0x0 (FALSE): AHB INCR16 burst type is not generated on Master I/F - 0x1 (TRUE): AHB INCR16 burst type can be generated on Master I/F Default Value: 0
2	BURST_INCR8_EN	INCR8 Burst Controls generation of INCR8 transfers on Master interface. Values: - 0x0 (FALSE): AHB INCR8 burst type is not generated on Master I/F - 0x1 (TRUE): AHB INCR8 burst type can be generated on Master I/F Default Value: 0
1	BURST_INCR4_EN	INCR4 Burst Controls generation of INCR4 transfers on Master interface. Values: - 0x0 (FALSE): AHB INCR4 burst type is not generated on Master I/F - 0x1 (TRUE): AHB INCR4 burst type can be generated on Master I/F Default Value: 0
0	UNDEFL_INCR_EN	Undefined INCR Burst Controls generation of undefined length INCR transfer on Master interface. Values: - 0x0 (FALSE): Undefined INCR type burst is the least preferred burst on AHB Master I/F - 0x1 (TRUE): Undefined INCR type burst is the most preferred burst on AHB Master I/F Default Value: 1

23.1.64 SDHC0_CORE_EMMC_CTRL_R

Description: eMMC Control register

Address: 0x4481152C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [7:4]				EMMC_RST_N_OE	EMMC_RST_N	DISABLE_DATA_CRC_CHK	CARD_IS_EMMC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW	RW	Reserved
HW Access	Reserved					R	R	Reserved
Name	Reserved [15:11]					CQE_PREFETCH_DISABLE	CQE_ALGO_SEL	Reserved

Bits	Name	Description
10	CQE_PREFETCH_DISABLE	Enable or Disable CQE's PREFETCH feature This field allows Software to disable CQE's data prefetch feature when set to 1. Values: - 0x0 (PREFETCH_ENABLE): CQE can Prefetch data for sucessive WRITE transfers and pipeline sucessive READ transfers - 0x1 (PREFETCH_DISABLE): Prefetch for WRITE and Pipeline for READ are disabled Default Value: 0
9	CQE_ALGO_SEL	Scheduler algorithm selected for execution This bit selects the Algorithm used for selecting one of the many ready tasks for execution. Values: - 0x0 (PRI_REORDER_PLUS_FCFS): Priority based reordering with FCFS to resolve equal priority tasks - 0x1 (FCFS_ONLY): First come First serve, in the order of DBR rings Default Value: 0
3	EMMC_RST_N_OE	Output Enable (OE) control for EMMC Device Reset signal (card_emmc_reset_n). Values: - 0x1 (ENABLE): OE for card_emmc_reset_n is 1 - 0x0 (DISABLE): OE for card_emmc_reset_n is 0 Default Value: 1
2	EMMC_RST_N	EMMC Device Reset signal control. This register field controls the card_emmc_reset_n output of SDHC Values: - 0x1 (RST_DEASSERT): Reset to eMMC device is deasserted - 0x0 (RST_ASSERT): Reset to eMMC device asserted (active low) Default Value: 1

23.1.64 SDHC0_CORE_EMMC_CTRL_R (continued)

1	DISABLE_- DATA_CRC_CHK	Disable Data CRC Check This bit controls masking of CRC16 error for Card Write in eMMC mode. This is useful in bus testing (CMD19) for an eMMC device. In bus testing, an eMMC card does not send CRC status for a block, which may generate CRC error. This CRC error can be masked using this bit during bus testing. Values: - 0x1 (DISABLE): DATA CRC check is disabled - 0x0 (ENABLE): DATA CRC check is enabled Default Value: 0
0	CARD_IS_EMMC	eMMC Card present This bit indicates the type of card connected. An application program this bit based on the card connected to SDHC. Values: - 0x1 (EMMC_CARD): Card connected to SDHC is an eMMC card - 0x0 (NON_EMMC_CARD): Card connected to SDHC is a non-eMMC card Default Value: 0

23.1.65 SDHC0_CORE_BOOT_CTRL_R

Description: eMMC Boot Control register

Address: 0x4481152E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	Reserved						RW
HW Access	R	Reserved						R
Name	VALI-DATE_-BOOT	Reserved [6:1]						MAN_-BOOT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW				Reserved			RW
HW Access	R				Reserved			R
Name	BOOT_TOUT_CNT [15:12]				Reserved [11:9]			BOOT_ACK_ENABLE

Bits	Name	Description
15 : 12	BOOT_TOUT_CNT	Boot Ack Timeout Counter Value. This value determines the interval by which boot ack timeout (50 ms) is detected when boot ack is expected during boot operation. - 0xF - Reserved - 0xE - TMCLK x 2^27 - .. - ..... - 0x1 - TMCLK x 2^14 - 0x0 - TMCLK x 2^13 Default Value: 0
8	BOOT_ACK_ENABLE	Boot Acknowledge Enable When this bit set, SDHC checks for boot acknowledge start pattern of 0-1-0 during boot operation. This bit is applicable for both mandatory and alternate boot mode. Values: - 0x1 (TRUE): Boot Ack enable - 0x0 (FALSE): Boot Ack disable Default Value: 0
7	VALIDATE_BOOT	Validate Mandatory Boot Enable bit This bit is used to validate the MAN_BOOT_EN bit. Values: - 0x1 (TRUE): Validate Mandatory boot enable bit - 0x0 (FALSE): Ignore Mandatory boot Enable bit Default Value: 0
0	MAN_BOOT_EN	Mandatory Boot Enable This bit is used to initiate the mandatory boot operation. The application sets this bit along with VALIDATE_BOOT bit. Writing 0 is ignored. The SDHC clears this bit after the boot transfer is completed or terminated. Values: - 0x1 (MAN_BOOT_EN): Mandatory boot enable - 0x0 (MAN_BOOT_DIS): Mandatory boot disable Default Value: 0

23.1.66 SDHC0_CORE_GP_IN_R

Description: General Purpose Input register

Address: 0x44811530

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							GP_IN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	GP_IN	It reflects the value of gp_in ports. NOT USED - ALWAYS READS 0 Default Value: 0

23.1.67 SDHC0_CORE_GP_OUT_R

Description: General Purpose Output register

Address: 0x44811534

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW	RW	RW	RW
HW Access	R		R	R	R	R	R	R
Name	CARD_CLOCK_OUT_D-LY [7:6]		IO_-VOLT_SEL_OE	CARD_IF_PWR_EN_OE	CARD_-CLOCK_OE	LED_C-TRL_OE	CARD_-MECH_WRITE_PROT_EN	CARD_DE-TECT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						CARD_CLOCK_IN_DLY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 8	CARD_CLOCK_IN_DLY	Delay CARD_CLOCK input internally to optimally sample CMD/DAT; set according to interface mode: 00: SD Default Speed, SD SDR12, eMMC Legacy 01: SD SDR25, SD SDR50 10: SD High Speed, eMMC High Speed SDR 11: SD DDR50, eMMC DDR Default Value: 0
7 : 6	CARD_CLOCK_OUT_D-LY	Delay CARD_CLOCK output relative to CMD/DAT to meet output setup/hold times; set according to interface mode: 00: SD Default Speed, SD High Speed, SD SDR12, eMMC Legacy 01: SD SDR25, SD SDR50, eMMC High Speed SDR 10: RESERVED 11: SD DDR50, eMMC DDR Default Value: 0
5	IO_VOLT_SEL_OE	Active high output enable for the IO voltage selection signal (io_volt_sel) controlled through HOST_CTRL_2.SIGNALING_EN: 0: disable OE to the io_volt_sel output 1: enable OE to the io_volt_sel output Default Value: 0

23.1.67 SDHC0_CORE_GP_OUT_R (continued)

4	CARD_IF_PWR_EN_OE	Active high output enable for the card interface power enable output (card_if_pwr_en) controlled through PWR_CTRL_R.SD_BUS_PWR_VDD1: 0: disable OE to the card_if_pwr_en output 1: enable OE to the card_if_pwr_en output Default Value: 0
3	CARD_CLOCK_OE	Active high output enable for the card clock output (clk_card) which is gated by CLK_CTRL_R.SD_CLK_EN: 0: disable OE to the clk_card output 1: enable OE to the clk_card output Default Value: 0
2	LED_CTRL_OE	Active high output enable for the LED output signal (led_ctrl) controlled through HOST_CTRL1_R.LED_CTRL: 0: disable OE associated with the led_ctrl output 1: enable OE associated with the led_ctrl output Default Value: 0
1	CARD_MECH_WRITE_PROT_EN	card_mech_write_prot, despite its name, is an active low signal (per the SD Host Controller Standard spec it is officially called SDWP#). Consider that in the following: 0: Force card_mech_write_prot input to 0 internally; this forces write protection to be active 1: Allow card_mech_write_prot to work normally per the device's pin state Default Value: 0
0	CARD_DETECT_EN	0: Force card_detect_n input to 0 1: Normal card_detect_n operation allowing card detection from a device pin Default Value: 0

24 Universal Serial Bus High-Speed registers

This section discusses the USBHS registers. It lists all the registers in mapping tables, in address order.

24.1 Register details

Register name	Address	Description
USBHS_DWC_otg_intreg_GOTGCTL	0x44900000	The OTG Control and Status register controls the behavior and reflects the status of the OTG function of the controller.
USBHS_DWC_otg_intreg_GOTGINT	0x44900004	The application reads this register whenever there is an OTG interrupt and clears the bits in this register to clear the OTG interrupt.
USBHS_DWC_otg_intreg_GAHBCFG	0x44900008	This register can be used to configure the core after power-on or a change in mode. This register mainly contains AHB system-related configuration parameters. Do not change this register after the initial programming. The application must program this register before starting any transactions on either the AHB or the USB.
USBHS_DWC_otg_intreg_GUSBCFG	0x4490000C	This register can be used to configure the core after power-on or when changing to Host mode or Device mode. It contains USB and USB-PHY related configuration parameters. The application must program this register before starting any transactions on either the AHB or the USB. If you are using the HSIC interface, HSIC PHY must be in reset while programming this register. Do not make changes to this register after the initial programming.
USBHS_DWC_otg_intreg_GRSTCTL	0x44900010	The application uses this register to reset various hardware features inside the controller.

Register name	Address	Description
USBHS_DWC_otg_intreg_GINTSTS	0x44900014	This register interrupts the application for system-level events in the current mode (Device mode or Host mode). Some of the bits in this register are valid only in Host mode, while others are valid in Device mode only. This register also indicates the current mode. To clear the interrupt status bits of type R_SS_WC, the application must write 1'b1 to the bit. The FIFO status interrupts are read only; once software reads from or writes to the FIFO while servicing these interrupts, FIFO interrupt conditions are cleared automatically. The application must clear the GINTSTS register at initialization before unmasking the interrupt bit to avoid any interrupts generated prior to initialization. Note: Read the reset value of GINTSTS.CurMod only after the following conditions: - If IDDIG_FILTER is disabled, read only after PHY clock is stable. - If IDDIG_FILTER is enabled, read only after the filter timer expires.
USBHS_DWC_otg_intreg_GINTMSK	0x44900018	This register works with the Interrupt Register (GINTSTS) to interrupt the application. When an interrupt bit is masked, the interrupt associated with that bit is not generated. However, the GINTSTS register bit corresponding to that interrupt is still set. Note: The fields of this register change depending on host or device mode.
USBHS_DWC_otg_intreg_GRXSTSR	0x4490001C	A read to the Receive Status Debug Read register returns the contents of the top of the Receive FIFO. The receive status contents must be interpreted differently in Host and Device modes. The core ignores the receive status read when the receive FIFO is empty and returns a value of 32'h0000_0000. Note: - Use of these fields vary based on whether the core is functioning as a host or a device. - Do not read this register's reset value before configuring the core because the read value is 'X' in the simulation.

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Register name	Address	Description
USBHS_DWC_otg_intreg_GRXSTSP	0x44900020	A read to the Receive Status Read and Pop register returns the contents of the top of the Receive FIFO and additionally pops the top data entry out of the RxFIFO. The receive status contents must be interpreted differently in Host and Device modes. The core ignores the receive status pop/read when the receive FIFO is empty and returns a value of 32'h0000_0000. The application must only pop the Receive Status FIFO when the Receive FIFO Non-Empty bit of the Core Interrupt register (GINTSTS.RxFLvl) is asserted. Note: - Use of these fields vary based on whether the core is functioning as a host or a device. - Do not read this register's reset value before configuring the core because the read value is 'X' in the simulation.
USBHS_DWC_otg_intreg_GRXFSIZ	0x44900024	The application can program the RAM size that must be allocated to the RxFIFO.
USBHS_DWC_otg_intreg_GNPTXFSIZ	0x44900028	The application can program the RAM size and the memory start address for the Non-periodic TxFIFO Note: The fields of this register change depending on host or device mode.
USBHS_DWC_otg_intreg_GNPTXSTS	0x4490002C	In Device mode, this register is valid only in Shared FIFO operation. This read-only register contains the free space information for the Non-periodic TxFIFO and the Non-periodic Transmit Request Queue.
USBHS_DWC_otg_intreg_GGPIO	0x44900038	The application can use this register for general purpose input/output ports or for debugging.
USBHS_DWC_otg_intreg_GUID	0x4490003C	This is a read/write register containing the User ID. It is implemented only if Remove Optional Features? was deselected during coreConsultant configuration (parameter OTG_RM_OPT_FEATURES = 0). The power-on value for this register is specified as the Power-on Value of User ID Register User Identification Register during coreConsultant configuration (parameter OTG_USERID). This register can be used in the following ways: - To store the version or revision of your system - To store hardware configurations that are outside the DWC_otg core - As a scratch register
USBHS_DWC_otg_intreg_GSNPSID	0x44900040	This read-only register contains the release number of the core being used.

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Register name	Address	Description
USBHS_DWC_otg_intreg_GHWCFG1	0x44900044	This register contains the logical endpoint direction(s) selected using coreConsultant.
USBHS_DWC_otg_intreg_GHWCFG2	0x44900048	This register contains configuration options selected using coreConsultant.
USBHS_DWC_otg_intreg_GHWCFG3	0x4490004C	This register contains configuration options selected using coreConsultant.
USBHS_DWC_otg_intreg_GHWCFG4	0x44900050	This register contains configuration options selected using coreConsultant. Note: Bit [31] is available only when Scatter/Gather DMA mode is enabled. When Scatter/Gather DMA mode is disabled, this field is reserved.
USBHS_DWC_otg_intreg_GLPMCFG	0x44900054	Register to control the LPM functionality of the controller.
USBHS_DWC_otg_intreg_GDFIFOCFG	0x4490005C	Register to configure the DFIFOs for the controller.
USBHS_DWC_otg_intreg_GINTMSK2	0x44900068	This register works with the Interrupt Register (GINTSTS2) to interrupt the application. When an interrupt bit is masked, the interrupt associated with that bit is not generated. However, the GINTSTS2 register bit corresponding to that interrupt is still set. Note: The fields of this register change depending on host or device mode.
USBHS_DWC_otg_intreg_GINTSTS2	0x4490006C	This register interrupts the application for system-level events in the current mode (Device mode or Host mode). Some of the bits in this register are valid only in Host mode, while others are valid in Device mode only. This register also indicates the current mode. To clear the interrupt status bits of type R_SS_WC, the application must write 1'b1 to the bit. The application must clear the GINTSTS2 register at initialization before unmasking the interrupt bit to avoid any interrupts generated prior to initialization.
USBHS_DWC_otg_intreg_HPTXFSIZ	0x44900100	This register holds the size and the memory start address of the Periodic TxFIFO. Note: Read the reset value of this register only after the following conditions: - If IDDIG_FILTER is disabled, read only after PHY clock is stable. - If IDDIG_FILTER is enabled, read only after the filter timer expires.

Register name	Address	Description
USBHS_DWC_otg_intreg_DIEPTXF1	0x44900104	This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.
USBHS_DWC_otg_intreg_DIEPTXF2	0x44900108	This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.
USBHS_DWC_otg_intreg_DIEPTXF3	0x4490010C	This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.
USBHS_DWC_otg_intreg_DIEPTXF4	0x44900110	This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.
USBHS_DWC_otg_intreg_DIEPTXF5	0x44900114	This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.

Register name	Address	Description
USBHS_DWC_otg_intreg_DIEPTXF6	0x44900118	This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.
USBHS_DWC_otg_intreg_DIEPTXF7	0x4490011C	This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.
USBHS_DWC_otg_intreg_DIEPTXF8	0x44900120	This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.
USBHS_DWC_otg_intreg_HCFG	0x44900400	This register is used to configure the controller in Host mode.
USBHS_DWC_otg_intreg_HFIR	0x44900404	This register is used to control the interval between two consecutive SOFs.
USBHS_DWC_otg_intreg_HFNUM	0x44900408	This register indicates the current frame number. It also indicates the time remaining (in terms of the number of PHY clocks) in the current (micro)frame. Note: Read the reset value of this register only after the following conditions: - If IDDIG_FILTER is disabled, read only when the PHY clock is stable. - If IDDIG_FILTER is enabled, read only after the filter timer expires.
USBHS_DWC_otg_intreg_HPTXSTS	0x44900410	This register contains information about the Periodic Transmit Queue in the Host controller.

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Register name	Address	Description
USBHS_DWC_otg_intreg_HAINT	0x44900414	When a significant event occurs on a channel, the Host All Channels Interrupt register interrupts the application using the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt). This is shown in the "Interrupt Hierarchy" figure in the databook. There is one interrupt bit per channel, up to a maximum of 16 bits. Bits in this register are set and cleared when the application sets and clears bits in the corresponding Host Channel-n Interrupt register.
USBHS_DWC_otg_intreg_HAINTMSK	0x44900418	The Host All Channel Interrupt Mask register works with the Host All Channel Interrupt register to interrupt the application when an event occurs on a channel. There is one interrupt mask bit per channel, up to a maximum of 16 bits.
USBHS_DWC_otg_intreg_HFLBAddr	0x4490041C	This register is present only in case of Scatter/Gather DMA. It is implemented as flops. This register holds the starting address of the Frame list information.
USBHS_DWC_otg_intreg_HPRT	0x44900440	This register is available only in Host mode. Currently, the OTG Host supports only one port. A single register holds USB port-related information such as USB reset, enable, suspend, resume, connect status, and test mode for each port. It is shown in the "Interrupt Hierarchy" figure in the databook. The R_SS_WC bits in this register can trigger an interrupt to the application through the Host Port Interrupt bit of the Core Interrupt register (GINTSTS.PrtInt). On a Port Interrupt, the application must read this register and clear the bit that caused the interrupt. For the R_SS_WC bits, the application must write a 1 to the bit to clear the interrupt.
USBHS_DWC_otg_intreg_HCCHAR0	0x44900500	This register contains the characteristics of the Host Channel.
USBHS_DWC_otg_intreg_HCSPLT0	0x44900504	This register contains the Split characteristics of the Host Channel.
USBHS_DWC_otg_intreg_HCINT0	0x44900508	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers.

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Register name	Address	Description
USBHS_DWC_otg_intreg_HCINTMSK0	0x4490050C	This register reflects the mask for each channel status described in the previous section.
USBHS_DWC_otg_intreg_HCTSIZ0	0x44900510	This register reflects the transfer size for the Host Channel.
USBHS_DWC_otg_intreg_HCDMA0	0x44900514	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned.
USBHS_DWC_otg_intreg_HCDMAB0	0x4490051C	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address.
USBHS_DWC_otg_intreg_HCCHAR1	0x44900520	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT1	0x44900524	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINT1	0x44900528	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK1	0x4490052C	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ1	0x44900530	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA1	0x44900534	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCDMAB1	0x4490053C	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR2	0x44900540	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT2	0x44900544	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINT2	0x44900548	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK2	0x4490054C	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ2	0x44900550	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA2	0x44900554	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB2	0x4490055C	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCCHAR3	0x44900560	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT3	0x44900564	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINT3	0x44900568	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK3	0x4490056C	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ3	0x44900570	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA3	0x44900574	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB3	0x4490057C	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR4	0x44900580	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT4	0x44900584	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT4	0x44900588	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK4	0x4490058C	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ4	0x44900590	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA4	0x44900594	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB4	0x4490059C	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR5	0x449005A0	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT5	0x449005A4	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT5	0x449005A8	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK5	0x449005AC	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ5	0x449005B0	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA5	0x449005B4	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB5	0x449005BC	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR6	0x449005C0	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT6	0x449005C4	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT6	0x449005C8	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK6	0x449005CC	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ6	0x449005D0	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA6	0x449005D4	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB6	0x449005DC	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR7	0x449005E0	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT7	0x449005E4	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT7	0x449005E8	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK7	0x449005EC	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ7	0x449005F0	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA7	0x449005F4	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB7	0x449005FC	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR8	0x44900600	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT8	0x44900604	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT8	0x44900608	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK8	0x4490060C	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ8	0x44900610	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA8	0x44900614	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB8	0x4490061C	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR9	0x44900620	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT9	0x44900624	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT9	0x44900628	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK9	0x4490062C	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ9	0x44900630	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA9	0x44900634	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB9	0x4490063C	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR10	0x44900640	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT10	0x44900644	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT10	0x44900648	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK10	0x4490064C	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ10	0x44900650	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA10	0x44900654	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB10	0x4490065C	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR11	0x44900660	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT11	0x44900664	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT11	0x44900668	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK11	0x4490066C	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ11	0x44900670	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA11	0x44900674	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB11	0x4490067C	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR12	0x44900680	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT12	0x44900684	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

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Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT12	0x44900688	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK12	0x4490068C	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ12	0x44900690	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA12	0x44900694	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB12	0x4490069C	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR13	0x449006A0	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT13	0x449006A4	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT13	0x449006A8	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK13	0x449006AC	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ13	0x449006B0	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA13	0x449006B4	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB13	0x449006BC	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR14	0x449006C0	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT14	0x449006C4	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT14	0x449006C8	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK14	0x449006CC	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ14	0x449006D0	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA14	0x449006D4	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB14	0x449006DC	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCCHAR15	0x449006E0	This register contains the characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCCHAR0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCSPLT15	0x449006E4	This register contains the Split characteristics of the Host Channel. See USBHS_DWC_otg_intreg_HCSPLT0 for the details of bit fields.

Register name	Address	Description
USBHS_DWC_otg_intreg_HCINT15	0x449006E8	This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers. See USBHS_DWC_otg_intreg_HCINT0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCINTMSK15	0x449006EC	This register reflects the mask for each channel status described in the previous section. See USBHS_DWC_otg_intreg_HCINTMSK0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCTSIZ15	0x449006F0	This register reflects the transfer size for the Host Channel. See USBHS_DWC_otg_intreg_HCTSIZ0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMA15	0x449006F4	This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned. See USBHS_DWC_otg_intreg_HCDMA0 for the details of bit fields.
USBHS_DWC_otg_intreg_HCDMAB15	0x449006FC	This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address. See USBHS_DWC_otg_intreg_HCDMAB0 for the details of bit fields.
USBHS_DWC_otg_intreg_DCFG	0x44900800	This register configures the core in Device mode after power-on or after certain control commands or enumeration. Do not make changes to this register after initial programming.
USBHS_DWC_otg_intreg_DCTL	0x44900804	This register is used to control the characteristics of the Device controller.
USBHS_DWC_otg_intreg_DSTS	0x44900808	This register indicates the status of the core with respect to USB-related events. It must be read on interrupts from Device All Interrupts (DAINT) register.

Register name	Address	Description
USBHS_DWC_otg_intreg_DIEPMSK	0x44900810	This register works with each of the Device IN Endpoint Interrupt (DIEPINTn) registers for all endpoints to generate an interrupt per IN endpoint. The IN endpoint interrupt for a specific status in the DIEPINTn register can be masked by writing to the corresponding bit in this register. Status bits are masked by default.
USBHS_DWC_otg_intreg_DOEPMSK	0x44900814	This register works with each of the Device OUT Endpoint Interrupt (DOEPINTn) registers for all endpoints to generate an interrupt per OUT endpoint. The OUT endpoint interrupt for a specific status in the DOEPINTn register can be masked by writing into the corresponding bit in this register. Status bits are masked by default.
USBHS_DWC_otg_intreg_DAINT	0x44900818	When a significant event occurs on an endpoint, a Device All Endpoints Interrupt register interrupts the application using the Device OUT Endpoints Interrupt bit or Device IN Endpoints Interrupt bit of the Core Interrupt register (GINTSTS.OEPInt or GINTSTS.IEPInt, respectively). This is shown in Figure 5-2. There is one interrupt bit per endpoint, up to a maximum of 16 bits for OUT endpoints and 16 bits for IN endpoints. For a bidirectional endpoint, the corresponding IN and OUT interrupt bits are used. Bits in this register are set and cleared when the application sets and clears bits in the corresponding Device Endpoint-n Interrupt register (DIEPINTn/DOEPINTn).
USBHS_DWC_otg_intreg_DAINTMSK	0x4490081C	The Device Endpoint Interrupt Mask register works with the Device Endpoint Interrupt register to interrupt the application when an event occurs on a device endpoint. However, the Device All Endpoints Interrupt (DAINT) register bit corresponding to that interrupt is still set.
USBHS_DWC_otg_intreg_DVBUSDIS	0x44900828	This register specifies the VBUS discharge time after VBUS pulsing during SRP.
USBHS_DWC_otg_intreg_DVBUSPULSE	0x4490082C	This register contains the VBUS pulsing time during SRP.
USBHS_DWC_otg_intreg_DTHRCTL	0x44900830	This register contains the Receive and Transmit Threshold characteristics of the Device controller.
USBHS_DWC_otg_intreg_DIEPEMPMSK	0x44900834	This register is valid only in Dedicated FIFO operation (OTG_EN_DED_TX_FIFO = 1). This register is used to control the IN endpoint FIFO empty interrupt generation (DIEPINTn.TxfEmp).

Register name	Address	Description
USBHS_DWC_otg_intreg_DIEPCTL0	0x44900900	This register is used to control the characteristics of the IN Endpoint 0 of the Device controller.
USBHS_DWC_otg_intreg_DIEPINT0	0x44900908	This register indicates the status of an endpoint with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the OUT Endpoints Interrupt bit or IN Endpoints Interrupt bit of the Core Interrupt register (GINTSTS.OEPInt or GINTSTS.IEPInt, respectively) is set. Before the application can read this register, it must first read the Device All Endpoints Interrupt (DAINT) register to get the exact endpoint number for the Device Endpoint-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the DAINT and GINTSTS registers
USBHS_DWC_otg_intreg_DIEPTSIZ0	0x44900910	The application must modify this register before enabling endpoint 0. Once endpoint 0 is enabled using Endpoint Enable bit of the Device Control Endpoint 0 Control registers (DIEPCTL0.EPEna/DOEPCTL0.EPEna), the core modifies this register. The application can only read this register once the core has cleared the Endpoint Enable bit. Nonzero endpoints use the registers for endpoints 115. When Scatter/Gather DMA mode is enabled, this register must not be programmed by the application. If the application reads this register when Scatter/Gather DMA mode is enabled, the core returns all zeros.
USBHS_DWC_otg_intreg_DIEPDMA0	0x44900914	This register contains the DMA Address for the IN Endpoint 0 of the Device controller.
USBHS_DWC_otg_intreg_DTXFSTS0	0x44900918	This register contains information about the IN Endpoint Transmit FIFO of the Device controller.
USBHS_DWC_otg_intreg_DIEPDMAB0	0x4490091C	This register contains the DMA Buffer Address for the IN Endpoint 0 of the Device controller.
USBHS_DWC_otg_intreg_DIEPCTL1	0x44900920	This register is used to control the characteristics of Endpoint 1. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPINT1	0x44900928	This register contains the interrupts for the IN Endpoint 1 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

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Register name	Address	Description
USBHS_DWC_otg_intreg_DIEPTSIZ1	0x44900930	This register reflects the Transfer Size of the IN Endpoint 1 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMA1	0x44900934	This register contains the DMA Address for the IN Endpoint 1 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DTXFSTS1	0x44900938	This register reflects the status of the IN Endpoint Transmit FIFO Status Register 1 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMAB1	0x4490093C	This register contains the DMA Buffer Address of the IN Endpoint 1 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPCTL2	0x44900940	This register is used to control the characteristics of Endpoint 2. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPINT2	0x44900948	This register contains the interrupts for the IN Endpoint 2 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPTSIZ2	0x44900950	This register reflects the Transfer Size of the IN Endpoint 2 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMA2	0x44900954	This register contains the DMA Address for the IN Endpoint 2 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DTXFSTS2	0x44900958	This register reflects the status of the IN Endpoint Transmit FIFO Status Register 2 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMAB2	0x4490095C	This register contains the DMA Buffer Address of the IN Endpoint 2 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPCTL3	0x44900960	This register is used to control the characteristics of Endpoint 3. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Register name	Address	Description
USBHS_DWC_otg_intreg_DIEPINT3	0x44900968	This register contains the interrupts for the IN Endpoint 3 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPTSIZ3	0x44900970	This register reflects the Transfer Size of the IN Endpoint 3 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMA3	0x44900974	This register contains the DMA Address for the IN Endpoint 3 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DTXFSTS3	0x44900978	This register reflects the status of the IN Endpoint Transmit FIFO Status Register 3 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMAB3	0x4490097C	This register contains the DMA Buffer Address of the IN Endpoint 3 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPCTL4	0x44900980	This register is used to control the characteristics of Endpoint 4. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPINT4	0x44900988	This register contains the interrupts for the IN Endpoint 4 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPTSIZ4	0x44900990	This register reflects the Transfer Size of the IN Endpoint 4 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMA4	0x44900994	This register contains the DMA Address for the IN Endpoint 4 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DTXFSTS4	0x44900998	This register reflects the status of the IN Endpoint Transmit FIFO Status Register 4 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Register name	Address	Description
USBHS_DWC_otg_intreg_DIEPDMAB4	0x4490099C	This register contains the DMA Buffer Address of the IN Endpoint 4 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPCTL5	0x449009A0	This register is used to control the characteristics of Endpoint 5. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPINT5	0x449009A8	This register contains the interrupts for the IN Endpoint 5 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPTSIZ5	0x449009B0	This register reflects the Transfer Size of the IN Endpoint 5 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMA5	0x449009B4	This register contains the DMA Address for the IN Endpoint 5 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DTXFSTS5	0x449009B8	This register reflects the status of the IN Endpoint Transmit FIFO Status Register 5 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMAB5	0x449009BC	This register contains the DMA Buffer Address of the IN Endpoint 5 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPCTL6	0x449009C0	This register is used to control the characteristics of Endpoint 6. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPINT6	0x449009C8	This register contains the interrupts for the IN Endpoint 6 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPTSIZ6	0x449009D0	This register reflects the Transfer Size of the IN Endpoint 6 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Register name	Address	Description
USBHS_DWC_otg_intreg_DIEPDMA6	0x449009D4	This register contains the DMA Address for the IN Endpoint 6 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DTXFSTS6	0x449009D8	This register reflects the status of the IN Endpoint Transmit FIFO Status Register 6 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMAB6	0x449009DC	This register contains the DMA Buffer Address of the IN Endpoint 6 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPCTL7	0x449009E0	This register is used to control the characteristics of Endpoint 7. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPINT7	0x449009E8	This register contains the interrupts for the IN Endpoint 7 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPTSIZ7	0x449009F0	This register reflects the Transfer Size of the IN Endpoint 7 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMA7	0x449009F4	This register contains the DMA Address for the IN Endpoint 7 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DTXFSTS7	0x449009F8	This register reflects the status of the IN Endpoint Transmit FIFO Status Register 7 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMAB7	0x449009FC	This register contains the DMA Buffer Address of the IN Endpoint 7 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPCTL8	0x44900A00	This register is used to control the characteristics of Endpoint 8. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPINT8	0x44900A08	This register contains the interrupts for the IN Endpoint 8 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

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Register name	Address	Description
USBHS_DWC_otg_intreg_DIEPTSIZ8	0x44900A10	This register reflects the Transfer Size of the IN Endpoint 8 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMA8	0x44900A14	This register contains the DMA Address for the IN Endpoint 8 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DTXFSTS8	0x44900A18	This register reflects the status of the IN Endpoint Transmit FIFO Status Register 8 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DIEPDMAB8	0x44900A1C	This register contains the DMA Buffer Address of the IN Endpoint 8 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.
USBHS_DWC_otg_intreg_DOEPCTL0	0x44900B00	This register is used to control the characteristics of the OUT Endpoint 0 of the Device controller.
USBHS_DWC_otg_intreg_DOEPINT0	0x44900B08	This register contains the interrupts for the OUT Endpoint 0 of the Device controller.
USBHS_DWC_otg_intreg_DOEPTSIZ0	0x44900B10	This register contains the Transfer Size for the OUT Endpoint 0 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMA0	0x44900B14	This register contains the DMA Address for the OUT Endpoint 0 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMAB0	0x44900B1C	This register contains the DMA Buffer Address for the OUT Endpoint 0 of the Device controller.
USBHS_DWC_otg_intreg_DOEPCTL1	0x44900B20	This register is used to control the characteristics of OUT Endpoint 1 of the Device controller.
USBHS_DWC_otg_intreg_DOEPINT1	0x44900B28	This register contains the interrupts for the OUT Endpoint 1 of the Device controller.
USBHS_DWC_otg_intreg_DOEPTSIZ1	0x44900B30	This register contains the Transfer Size for the OUT Endpoint 1 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMA1	0x44900B34	This register contains the DMA Address for the OUT Endpoint 1 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMAB1	0x44900B3C	This register contains the DMA Buffer Address for the OUT Endpoint 1 of the Device controller.
USBHS_DWC_otg_intreg_DOEPCTL2	0x44900B40	This register is used to control the characteristics of OUT Endpoint 2 of the Device controller.
USBHS_DWC_otg_intreg_DOEPINT2	0x44900B48	This register contains the interrupts for the OUT Endpoint 2 of the Device controller.
USBHS_DWC_otg_intreg_DOEPTSIZ2	0x44900B50	This register contains the Transfer Size for the OUT Endpoint 2 of the Device controller.

Register name	Address	Description
USBHS_DWC_otg_intreg_DOEPDMA2	0x44900B54	This register contains the DMA Address for the OUT Endpoint 2 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMAB2	0x44900B5C	This register contains the DMA Buffer Address for the OUT Endpoint 2 of the Device controller.
USBHS_DWC_otg_intreg_DOEPCTL3	0x44900B60	This register is used to control the characteristics of OUT Endpoint 3 of the Device controller.
USBHS_DWC_otg_intreg_DOEPINT3	0x44900B68	This register contains the interrupts for the OUT Endpoint 3 of the Device controller.
USBHS_DWC_otg_intreg_DOEPTSIZ3	0x44900B70	This register contains the Transfer Size for the OUT Endpoint 3 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMA3	0x44900B74	This register contains the DMA Address for the OUT Endpoint 3 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMAB3	0x44900B7C	This register contains the DMA Buffer Address for the OUT Endpoint 3 of the Device controller.
USBHS_DWC_otg_intreg_DOEPCTL4	0x44900B80	This register is used to control the characteristics of OUT Endpoint 4 of the Device controller.
USBHS_DWC_otg_intreg_DOEPINT4	0x44900B88	This register contains the interrupts for the OUT Endpoint 4 of the Device controller.
USBHS_DWC_otg_intreg_DOEPTSIZ4	0x44900B90	This register contains the Transfer Size for the OUT Endpoint 4 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMA4	0x44900B94	This register contains the DMA Address for the OUT Endpoint 4 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMAB4	0x44900B9C	This register contains the DMA Buffer Address for the OUT Endpoint 4 of the Device controller.
USBHS_DWC_otg_intreg_DOEPCTL5	0x44900BA0	This register is used to control the characteristics of OUT Endpoint 5 of the Device controller.
USBHS_DWC_otg_intreg_DOEPINT5	0x44900BA8	This register contains the interrupts for the OUT Endpoint 5 of the Device controller.
USBHS_DWC_otg_intreg_DOEPTSIZ5	0x44900BB0	This register contains the Transfer Size for the OUT Endpoint 5 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMA5	0x44900BB4	This register contains the DMA Address for the OUT Endpoint 5 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMAB5	0x44900BBC	This register contains the DMA Buffer Address for the OUT Endpoint 5 of the Device controller.
USBHS_DWC_otg_intreg_DOEPCTL6	0x44900BC0	This register is used to control the characteristics of OUT Endpoint 6 of the Device controller.
USBHS_DWC_otg_intreg_DOEPINT6	0x44900BC8	This register contains the interrupts for the OUT Endpoint 6 of the Device controller.
USBHS_DWC_otg_intreg_DOEPTSIZ6	0x44900BD0	This register contains the Transfer Size for the OUT Endpoint 6 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMA6	0x44900BD4	This register contains the DMA Address for the OUT Endpoint 6 of the Device controller.

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Register name	Address	Description
USBHS_DWC_otg_intreg_DOEPDMAB6	0x44900BDC	This register contains the DMA Buffer Address for the OUT Endpoint 6 of the Device controller.
USBHS_DWC_otg_intreg_DOEPCTL7	0x44900BE0	This register is used to control the characteristics of OUT Endpoint 7 of the Device controller.
USBHS_DWC_otg_intreg_DOEPINT7	0x44900BE8	This register contains the interrupts for the OUT Endpoint 7 of the Device controller.
USBHS_DWC_otg_intreg_DOEPTSIZ7	0x44900BF0	This register contains the Transfer Size for the OUT Endpoint 7 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMA7	0x44900BF4	This register contains the DMA Address for the OUT Endpoint 7 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMAB7	0x44900BFC	This register contains the DMA Buffer Address for the OUT Endpoint 7 of the Device controller.
USBHS_DWC_otg_intreg_DOEPCTL8	0x44900C00	This register is used to control the characteristics of OUT Endpoint 8 of the Device controller.
USBHS_DWC_otg_intreg_DOEPINT8	0x44900C08	This register contains the interrupts for the OUT Endpoint 8 of the Device controller.
USBHS_DWC_otg_intreg_DOEPTSIZ8	0x44900C10	This register contains the Transfer Size for the OUT Endpoint 8 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMA8	0x44900C14	This register contains the DMA Address for the OUT Endpoint 8 of the Device controller.
USBHS_DWC_otg_intreg_DOEPDMAB8	0x44900C1C	This register contains the DMA Buffer Address for the OUT Endpoint 8 of the Device controller.
USBHS_DWC_otg_intreg_PCGCCTL	0x44900E00	This register is used to control the Power and Clock Gating characteristics of the controller.
USBHS_DWC_otg_intreg_PCGCCTL1	0x44900E04	This register is used to control the Power and Clock Gating characteristics of the controller.
USBHS_SS_SUBSYSTEM_CTL	0x44940000	Subsystem level control register
USBHS_SS_PHY_FUNC_CTL_1	0x44940004	Subsystem level- PHY functional mode control register 1
USBHS_SS_PHY_FUNC_CTL_2	0x44940008	Subsystem level- PHY functional mode control register 2
USBHS_SS_PHY_TEST_CTL	0x4494000C	Subsystem level- PHY test mode control register
USBHS_SS_CONTROLLER_DDFT_CTL	0x44940010	Subsystem level- Controller DDFT control register
USBHS_SS_INTR_SS	0x44940014	Subsystem level- Interrupt register
USBHS_SS_INTR_SS_SET	0x44940018	Subsystem level- Interrupt set register
USBHS_SS_INTR_SS_MASK	0x4494001C	Subsystem level- Interrupt mask register
USBHS_SS_INTR_SS_MASKED	0x44940020	Subsystem level- Interrupt masked register

24.1.1 USBHS_DWC_otg_intreg_GOTGCTL

Description: The OTG Control and Status register controls the behavior and reflects the status of the OTG function of the controller.

Address: 0x44900000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	Reserved	
HW Access							Reserved	
Name	BvalidOvVal	BvalidOvEn	AvalidOvVal	AvalidOvEn	VbvalidOv-Val	Vbva-lidOvEn	Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved						
HW Access		Reserved						
Name	DbnceFltr-Bypass	Reserved [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R	RW	R	R	R	R
HW Access	Reserved							
Name	Reserved [23:22]		CurMod	OTGVer	BSesVld	ASesVld	DbncTime	ConIDSts

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access		Reserved						
Name	Testmod-e_cor-r_eUSB2	Reserved [30:24]						

Bits	Name	Description
31	Testmode_corr_eUSB2	UTMI IF correction for eUSB2 PHY during Test mode This bit is used to modify the behavior of UTMI 8-bit interface signals during test J and test K sequences when eUSB2 PHY is used. When this bit is set to 1'b1, the controller asserts utmi_txvalid and utmi_opmode in the same cycle during test J or test K sequence execution. Note: This bit is applicable only if eUSB2 PHY is used with 8-bit UTMI interface. Default Value: 0x0 **0x0: eUSB2_corr_disable :** The controller asserts utmi_txvalid one cycle later than utmi_opmode. **0x1: eUSB2_corr_enable :** The controller asserts utmi_txvalid and utmi_opmode in the same cycle.

24.1.1 USBHS_DWC_otg_intreg_GOTGCTL (continued)

21	CurMod	Current Mode of Operation (CurMod) Mode: Host and Device Indicates the current mode. - 1'b0: Device mode - 1'b1: Host mode Reset: - 1'b1 in Host-only mode (OTG_MODE=5 or 6) - 1'b0 in all other configurations Note: The reset value of this register field can be read only after the PHY clock is stable, or if IDDIG_FILTER is enabled, wait for the filter timer to expire to read the correct reset value which ever event is later. Default Value: 0x0 **0x0: DEVICEMODE :** Current mode is device mode. **0x1: HOSTMODE :** Current mode is host mode.
20	OTGVer	OTG Version (OTGVer) Indicates the OTG revision. - 1'b0: OTG Version 1.3. In this version the core supports Data line pulsing and VBus pulsing for SRP. - 1'b1: OTG Version 2.0. In this version the core supports only Data line pulsing for SRP. Default Value: 0x0 **0x0: VER13 :** Supports OTG Version 1.3 **0x1: VER20 :** Supports OTG Version 2.0
19	BSesVld	Mode: Device only B-Session Valid (BSesVld) Indicates the Device mode transceiver status. - 1'b0: B-session is not valid. - 1'b1: B-session is valid. In OTG mode, you can use this bit to determine if the device is connected or disconnected. Note: - If you do not enable OTG features (such as SRP and HNP), the read reset value will be 1.The vbus assigns the values internally for non- SRP or non-HNP configurations. - In case of OTG_MODE=0, the reset value of this bit is 1'b0. - The reset value of this register field can be read only after the PHY clock is stable, or if IDDIG_-FILTER is enabled, wait for the filter timer to expire to read the correct reset value which ever event is later. Default Value: 0x1 **0x0: NOTVALID :** B-session is not valid. **0x1: VALID :** B-session is valid.

24.1.1 USBHS_DWC_otg_intreg_GOTGCTL (continued)

18	ASesVld	Mode: Host only A-Session Valid (ASesVld) Indicates the Host mode transceiver status. - 1'b0: A-session is not valid - 1'b1: A-session is valid Note: If you do not enabled OTG features (such as SRP and HNP), the read reset value will be 1. The vbus assigns the values internally for non-SRP or non-HNP configurations. In case of OTG_MODE=0, the reset value of this bit is 1'b0. Default Value: 0x1 **0x0: NOTVALID :** A-session is not valid. **0x1: VALID :** A-session is valid.
17	DbncTime	Mode: Host only Long/Short Debounce Time (DbncTime) Indicates the debounce time of a detected connection. - 1'b0: Long debounce time, used for physical connections (100 ms + 2.5 micro-sec) - 1'b1: Short debounce time, used for soft connections (2.5 micro-sec) Default Value: 0x0 **0x0: LONG :** Long debounce time, used for physical connections (100 ms + 2.5 micro-sec) **0x1: SHORT :** Short debounce time, used for soft connections (2.5 micro-sec)
16	ConIDSts	Mode: Host and Device Connector ID Status (ConIDSts) Indicates the connector ID status on a connect event. - 1'b0: The core is in A-Device mode. - 1'b1: The core is in B-Device mode. Note: The reset value of this register field can be read only after the PHY clock is stable, or if IDDIG_-FILTER is enabled, wait for the filter timer to expire to read the correct reset value which ever event is later. Reset: - 1'b0: in host only mode (OTG_MODE = 5 or 6) - 1'b1: in all other configurations Default Value: 0x1 **0x0: MODEA :** The core is in A-Device mode. **0x1: MODEB :** The core is in B-Device mode.
15	DbnceFltrBypass	Mode: Host and Device Debounce Filter Bypass Bypass Debounce filters for avalid, bvalid, vbusvalid, sessend, iddig signals when enabled. - 1'b0: Disabled - 1'b1: Enabled Note: This register bit is valid only when debounce filters are present in core. Default Value: 0x0

24.1.1 USBHS_DWC_otg_intreg_GOTGCTL (continued)

		0x0: DISABLED : Debounce Filter Bypass is disabled. **0x1: ENABLED :** Debounce Filter Bypass is enabled.
7	BvalidOvVal	Mode: Device only B-Peripheral Session Valid OverrideValue (BvalidOvVal) This bit is used to set Override value for Bvalid signal when GOTGCTL.BvalidOvEn is set. - 1'b0 : Bvalid value is 1'b0 when GOTGCTL.BvalidOvEn =1 - 1'b1 : Bvalid value is 1'b1 when GOTGCTL.BvalidOvEn =1 Default Value: 0x0 **0x0: VALUE0 :** Bvalid value when GOTGCTL.BvalidOvEn =1 **0x1: VALUE1 :** Bvalid value when GOTGCTL.BvalidOvEn =1
6	BvalidOvEn	Mode: Device only B-Peripheral Session Valid Override Value (BvalidOvEn) This bit is used to enable/disable the software to override the Bvalid signal using the GOTGCTL.BvalidOvVal. - 1'b1 : Internally Bvalid received from the PHY is overridden with GOTGCTL.BvalidOvVal. - 1'b0 : Override is disabled and bvalid signal from the respective PHY selected is used internally by the force Default Value: 0x0 **0x0: DISABLED :** Override is disabled and bvalid signal from the respective PHY selected is used internally by the core **0x1: ENABLED :** Internally Bvalid received from the PHY is overridden with GOTGCTL.BvalidOvVal
5	AvalidOvVal	Mode: Host only A-Peripheral Session Valid OverrideValue (AvalidOvVal) This bit is used to set Override value for Avalid signal when GOTGCTL.AvalidOvEn is set. - 1'b0 : Avalid value is 1'b0 when GOTGCTL.AvalidOvEn =1 - 1'b1 : Avalid value is 1'b1 when GOTGCTL.AvalidOvEn =1 Default Value: 0x0 **0x0: VALUE0 :** Avalid value is 1'b0 when GOTGCTL.AvalidOvEn =1 **0x1: VALUE1 :** Avalid value is 1'b1 when GOTGCTL.AvalidOvEn =1

24.1.1 USBHS_DWC_otg_intreg_GOTGCTL (continued)

4	AvalidOvEn	Mode: Host only A-Peripheral Session Valid Override Enable (AvalidOvEn) This bit is used to enable/disable the software to override the Avalid signal using the GOTGCTL.AvalidOvVal. - 1'b1: Internally Avalid received from the PHY is overridden with GOTGCTL.AvalidOvVal. - 1'b0: Override is disabled and avalid signal from the respective PHY selected is used internally by the core Default Value: 0x0 **0x0: DISABLED :** Derive AValid from PHY **0x1: ENABLED :** Derive Avalid from GOTGCTL.AvalidOvVal
3	VbvalidOvVal	Mode: Host only VBUS Valid OverrideValue (VbvalidOvVal) This bit is used to set Override value for vbusvalid signal when GOTGCTL.VbvalidOvEn is set. - 1'b0 : vbusvalid value is 1'b0 when GOTGCTL.VbvalidOvEn =1 - 1'b1 : vbusvalid value is 1'b1 when GOTGCTL.VbvalidOvEn =1 Default Value: 0x0 **0x0: SET0 :** vbusvalid value when GOTGCTL.VbvalidOvEn = 1 **0x1: SET1 :** vbusvalid value when GOTGCTL.VbvalidOvEn is 1
2	VbvalidOvEn	Mode: Host only VBUS Valid Override Enable (VbvalidOvEn) This bit is used to enable/disable the software to override the Bvalid signal using the GOTGCTL.VbvalidOvVal. - 1'b1 : Internally Bvalid received from the PHY is overridden with GOTGCTL.VbvalidOvVal. - 1'b0 : Override is disabled and bvalid signal from the respective PHY selected is used internally by the controller. Default Value: 0x0 **0x0: DISABLED :** Override is disabled and bvalid signal from the respective PHY selected is used internally by the controller **0x1: ENABLED :** The vbus-valid signal received from the PHY is overridden with GOTGCTL.VbvalidOvVal

24.1.2 USBHS_DWC_otg_intreg_GOTGINT

Description: The application reads this register whenever there is an OTG interrupt and clears the bits in this register to clear the OTG interrupt.

Address: 0x44900004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	Reserved	
HW Access	Reserved						Reserved	
Name	Reserved [7:3]					SesEndDet	Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	RW
HW Access	Reserved							
Name	Reserved [15:10]						HstNeg-SucStsChng	SesReq-SucStsChng

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW	RW	RW	Reserved
HW Access	Reserved							Reserved
Name	Reserved [23:20]				DbnceDone	ADevTOUT Chg	HstNegDet	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19	DbnceDone	Mode: Host only Debounce Done (DbnceDone) The core sets this bit when the debounce is completed after the device connect. The application can start driving USB reset after seeing this interrupt. This bit is only valid when the HNP Capable or SRP Capable bit is SET in the Core USB Configuration register (GUSBCFG.HNPCap or GUSBCFG.SRPCap, respectively). This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** Debounce completed **0x0: INACTIVE :** After Connect waiting for Debounce to complete
18	ADevTOUTChg	Mode: Host and Device A-Device Timeout Change (ADevTOUTChg) The core sets this bit to indicate that the A-device has timed out while waiting for the B-device to connect.This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0

24.1.2 USBHS_DWC_otg_intreg_GOTGINT (continued)

		0x1: ACTIVE : A-Device Timeout **0x0: INACTIVE :** No A-Device Timeout
17	HstNegDet	Mode:Host and Device Host Negotiation Detected (HstNegDet) The core sets this bit when it detects a host negotiation request on the USB. This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** Active HNP request detected **0x0: INACTIVE :** No Active HNP Request
9	HstNegSucStsChng	Mode: Host and Device Host Negotiation Success Status Change (HstNegSucStsChng) The core sets this bit on the success or failure of a USB host negotiation request. The application must read the Host Negotiation Success bit of the OTG Control and Status register (GOTGCTL.HstNegScs) to check for success or failure. This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** Host Negotiation Status Change **0x0: INACTIVE :** No Change
8	SesReqSucStsChng	Mode: Host and Device Session Request Success Status Change (SesReqSucStsChng) The core sets this bit on the success or failure of a session request. The application must read the Session Request Success bit in the OTG Control and Status register (GOTGCTL.SesReqScs) to check for success or failure. This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** Session Request Status has changed **0x0: INACTIVE :** No Change in Session Request Status
2	SesEndDet	Mode: Host and Device Session End Detected (SesEndDet) The controller sets this bit when the utmiotg_bvalid signal is deasserted. This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0

24.1.2 USBHS_DWC_otg_intreg_GOTGINT (continued)

0x1: ACTIVE :

SessionEnd utmiotg_bvalid signal is deasserted

0x0: INACTIVE :

Session is Active

24.1.3 USBHS_DWC_otg_intreg_GAHBCFG

Description: This register can be used to configure the core after power-on or a change in mode. This register mainly contains AHB system-related configuration parameters. Do not change this register after the initial programming. The application must program this register before starting any transactions on either the AHB or the USB.

Address: 0x44900008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved	RW	RW				RW
HW Access		Reserved						
Name	NPTxFEm-pLvl	Reserved	DMAEn	HBstLen [4:1]				GlblIntrMsk

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							
Name	Reserved [15:9]							PTxFEm-pLvl

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	Reserved				
HW Access				Reserved				
Name	AHBSingle	NotiAllD-maWrit	RemMem-Supp	Reserved [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							
Name	Reserved [31:25]							InvDescEn-dianess

Bits	Name	Description
24	InvDescEndianess	Mode: Host and Device Invert Descriptor Endianess (InvDescEndianess) - 1'b0: Descriptor Endianness is same as AHB Master Endianness. - 1'b1: -- If the AHB Master endianness is Big Endian, the Descriptor Endianness is Little Endian. -- If the AHB Master endianness is Little Endian, the Descriptor Endianness is Big Endian. Default Value: 0x0 **0x0: DISABLE :** Descriptor Endianness is same as AHB Master Endianness **0x1: ENABLE :** Descriptor Endianness is opposite to AHB Master Endianness

24.1.3 USBHS_DWC_otg_intreg_GAHBCFG (continued)

23	AHBSingle	Mode: Host and Device AHB Single Support (AHBSingle) This bit when programmed supports Single transfers for the remaining data in a transfer when the core is operating in DMA mode. - 1'b0: The remaining data in the transfer is sent using INCR burst size. - 1'b1: The remaining data in the transfer is sent using Single burst size. Note: If this feature is enabled, the AHB RETRY and SPLIT transfers still have INCR burst type. Enable this feature when the AHB Slave connected to the core does not support INCR burst (and when Split, and Retry transactions are not being used in the bus). Default Value: 0x0 **0x0: INCRBURST :** The remaining data in the transfer is sent using INCR burst size **0x1: SINGLEBURST :** The remaining data in the transfer is sent using Single burst size
22	NotiAllDmaWrit	Mode: Host and Device Notify All DMA Write Transactions (NotiAllDmaWrit) This bit is programmed to enable the System DMA Done functionality for all the DMA write Transactions corresponding to the Channel/Endpoint. This bit is valid only when GAHBCFG.RemMemSupp is set to 1. - GAHBCFG.NotiAllDmaWrit = 1 The core asserts int_dma_req for all the DMA write transactions on the AHB interface along with int_dma_done, chep_last_transact and chep_number signal informations. The core waits for sys_dma_done signal for all the DMA write transactions in order to complete the transfer of a particular Channel/Endpoint. - GAHBCFG.NotiAllDmaWrit = 0 The core asserts int_dma_req signal only for the last transaction of DMA write transfer corresponding to a particular Channel/Endpoint. Similarly, the core waits for sys_dma_done signal only for that transaction of DMA write to complete the transfer of a particular Channel/Endpoint. Default Value: 0x0 **0x1: ALLTRANS :** The core asserts int_dma_req for all the DMA write transactions on the AHB interface along with int_dma_done, chep_last_transact and chep_number signal informations. The core waits for sys_dma_done signal for all the DMA write transactions in order to complete the transfer of a particular Channel/Endpoint **0x0: LASTTRANS :**
21	RemMemSupp	Mode: Host and Device Remote Memory Support (RemMemSupp) This bit is programmed to enable the functionality to wait for the system DMA Done Signal for the DMA Write Transfers. - GAHBCFG.RemMemSupp=1 The int_dma_req output signal is asserted when the DMA starts write transfer to the external memory. When the core is done with the Transfers it asserts int_dma_done signal to flag the completion of DMA writes from the controller. The core then waits for sys_dma_done signal from the system to proceed further and complete the Data Transfer corresponding to a particular Channel/Endpoint. - GAHBCFG.RemMemSupp=0 The int_dma_req and int_dma_done signals are not asserted and the core proceeds with the assertion of the XferComp interrupt as soon as the DMA write transfer is done at the Core Boundary and it does not wait for the sys_dma_done signal to complete the DATA transfers. Default Value: 0x0 **0x0: DISABLED :** Remote Memory Support Feature disabled

24.1.3 USBHS_DWC_otg_intreg_GAHBCFG (continued)

		0x1: ENABLED : Remote Memory Support Feature enabled
8	PTxFEmpLvl	Mode: Host only Periodic TxFIFO Empty Level (PTxFEmpLvl) Indicates when the Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.PTxFEmp) is triggered. This bit is used only in Slave mode. - 1'b0: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is half empty - 1'b1: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is completely empty Default Value: 0x0 **0x1: EMPTY :** GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is completely empty. **0x0: HALFEMPTY :** GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is half empty.
7	NPTxFEmpLvl	Mode: Host and device Non-Periodic TxFIFO Empty Level (NPTxFEmpLvl) This bit is used only in Slave mode. In host mode and with Shared FIFO with device mode, this bit indicates when the Non-Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.NPTxFEmp) is triggered. With dedicated FIFO in device mode, this bit indicates when IN endpoint Transmit FIFO empty interrupt (DIEPINTn.TxFEmp) is triggered. Host mode and with Shared FIFO with device mode: - 1'b0: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is half empty - 1'b1: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is completely empty Dedicated FIFO in device mode: - 1'b0: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is half empty - 1'b1: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is completely empty Default Value: 0x0 **0x1: EMPTY :** GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is completely empty or that the IN Endpoint TxFIFO is completely empty. **0x0: HALFEMPTY :** DIEPINTn.TxFEmp interrupt indicates that the Non-Periodic TxFIFO is half empty or that the IN Endpoint TxFIFO is half empty.
5	DMAEn	Mode: Host and device DMA Enable (DMAEn) This bit is always 0 when Slave-Only mode has been selected. Reset: 1'b0 Default Value: 0x0 **0x1: DMAMODE :** Core operates in a DMA mode **0x0: SLAVEMODE :** Core operates in Slave mode

24.1.3 USBHS_DWC_otg_intreg_GAHBCFG (continued)

4 : 1	HBstLen	Mode: Host and device Burst Length/Type (HBstLen) This field is used in both External and Internal DMA modes. In External DMA mode, these bits appear on dma_burst[3:0] ports, which can be used by an external wrapper to interface the External DMA Controller interface to Synopsys DW_ahb_dmac or ARM PrimeCell. External DMA Mode defines the DMA burst length in terms of 32-bit words: - 4'b0000: 1 word - 4'b0001: 4 words - 4'b0010: 8 words - 4'b0011: 16 words - 4'b0100: 32 words - 4'b0101: 64 words - 4'b0110: 128 words - 4'b0111: 256 words - Others: Reserved Internal DMA Mode AHB Master burst type: - 4'b0000 Single - 4'b0001 INCR - 4'b0011 INCR4 - 4'b0101 INCR8 - 4'b0111 INCR16 - Others: Reserved Default Value: 0x0 **0x6: WORD128 :** 128 words **0x3: WORD16ORINCR4 :** 16 words or INCR4 **0x0: WORD1ORSINGLE :** 1 word or single **0x7: WORD256ORINCR16 :** 256 words or INCR16 **0x4: WORD32 :** 32 words **0x1: WORD4ORINCR :** 4 words or INCR **0x5: WORD64ORINCR8 :** 64 words or INCR8 **0x2: WORD8 :** 8 words **0x8: WORDX :** Others reserved

24.1.3 USBHS_DWC_otg_intreg_GAHBCFG (continued)

0	GlblIntrMsk	Mode: Host and device Global Interrupt Mask (GlblIntrMsk) The application uses this bit to mask or unmask the interrupt line assertion to itself. Irrespective of this bit's setting, the interrupt status registers are updated by the controller. Default Value: 0x0 **0x0: MASK :** Mask the interrupt assertion to the application **0x1: NOMASK :** Unmask the interrupt assertion to the application.

24.1.4 USBHS_DWC_otg_intreg_GUSBCFG

Description: This register can be used to configure the core after power-on or when changing to Host mode or Device mode. It contains USB and USB-PHY related configuration parameters. The application must program this register before starting any transactions on either the AHB or the USB. If you are using the HSIC interface, HSIC PHY must be in reset while programming this register. Do not make changes to this register after the initial programming.

Address: 0x4490000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R	R	R	R	RW		
HW Access	Reserved							
Name	Reserved	PHYSel	FSIntf	ULPI_UT-MI_Sel	PHYIf	TOutCal [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved	RW				Reserved	
HW Access		Reserved					Reserved	
Name	PhyLPwr-ClkSel	Reserved	USBTrdTim [13:10]				Reserved [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW	Reserved					
HW Access	Reserved		Reserved					
Name	Reserved	TermSelDL-Pulse	Reserved [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	W	RW	RW	RW	Reserved	R	Reserved	
HW Access					Reserved		Reserved	
Name	CorruptTxP-kt	ForceDev-Mode	ForceHst-Mode	TxEndDelay	Reserved	IC_USBCap	Reserved [25:24]	

Bits	Name	Description
31	CorruptTxPkt	Mode: Host and device Corrupt Tx packet (CorruptTxPkt) This bit is for debug purposes only. Never Set this bit to 1. The application should always write 1'b0 to this bit. Default Value: 0x0 **0x1: DEBUG :** Debug Mode **0x0: NODEBUG :** Normal Mode

24.1.4 USBHS_DWC_otg_intreg_GUSBCFG (continued)

30	ForceDevMode	Mode:Host and device Force Device Mode (ForceDevMode) Writing a 1 to this bit forces the controller to device mode irrespective of utmiotg_iddig input pin. - 1'b0 : Normal Mode. - 1'b1 : Force Device Mode. After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 micro sec is sufficient. This bit is valid only when OTG_MODE = 0, 1 or 2. In all other cases, this bit reads 0. Default Value: 0x0 **0x0: DISABLED :** Normal Mode **0x1: ENABLED :** Force Device Mode
29	ForceHstMode	Mode: Host and device Force Host Mode (ForceHstMode) Writing a 1 to this bit forces the core to host mode irrespective of utmiotg_iddig input pin. - 1'b0 : Normal Mode. - 1'b1 : Force Host Mode. After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 micro sec is sufficient. This bit is valid only when OTG_MODE = 0, 1 or 2. In all other cases, this bit reads 0. Default Value: 0x0 **0x0: DISABLED :** Normal Mode **0x1: ENABLED :** Force Host Mode
28	TxEndDelay	Mode: Device only Tx End Delay (TxEndDelay) Writing 1'b1 to this bit enables the controller to follow the TxEndDelay timings as per UTMI+ specification 1.05 section 4.1.5 for opmode signal during remote wakeup. - 1'b0 : Normal Mode. - 1'b1 : Tx End delay. Default Value: 0x0 **0x0: DISABLED :** Normal Mode **0x1: ENABLED :** Tx End delay
26	IC_USBCap	Mode: Host and Device IC_USB-Capable (IC_USBCap) The application uses this bit to control the core's IC_USB capabilities. - 1'b0: IC_USB PHY Interface is not selected. - 1'b1: IC_USB PHY Interface is selected. This bit is writable only if OTG_ENABLE_IC_USB=1 and OTG_FSPHY_INTERFACE!=0. The reset value depends on the configuration parameter OTG_SELECT_IC_USB when OTG_ENABLE_IC_USB = 1. In all other cases, this bit is set to 1'b0 and the bit is read only. Default Value: 0x0

24.1.4 USBHS_DWC_otg_intreg_GUSBCFG (continued)

		0x0: NOTSELECTED : IC_USB PHY Interface is not selected **0x1: SELECTED :** IC_USB PHY Interface is selected
22	TermSelDLPulse	Mode: Device only TermSel DLine Pulsing Selection (TermSelDLPulse) This bit selects utmi_termselect to drive data line pulse during SRP. - 1'b0: Data line pulsing using utmi_txvalid (Default). - 1'b1: Data line pulsing using utmi_termsel. Default Value: 0x0 **0x1: TERMSEL :** Data line pulsing using utmi_termsel **0x0: TXVALID :** Data line pulsing using utmi_txvalid
15	PhyLPwrClkSel	PHY Low-Power Clock Select (PhyLPwrClkSel) Mode: Host and Device Selects either 480-MHz or 48-MHz (low-power) PHY mode. In FS and LS modes, the PHY can usually operate on a 48-MHz clock to save power. - 1'b0: 480-MHz Internal PLL clock - 1'b1: 48-MHz External Clock In 480 MHz mode, the UTMI interface operates at either 60 or 30-MHz, depending upon whether 8- or 16-bit data width is selected. In 48-MHz mode, the UTMI interface operates at 48 MHz in FS mode and at either 48 or 6 MHz in LS mode (depending on the PHY vendor). This bit drives the utmi_fsls_low_power core output signal, and is valid only for UTMI+ PHYs. Default Value: 0x0 **0x1: EXTCLK :** 48-MHz External Clock **0x0: INTPLLCLK :** 480-MHz Internal PLL clock
13 : 10	USBTrdTim	Mode: Device only USB Turnaround Time (USBTrdTim) Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). This must be programmed to - 4'h5 : When the MAC interface is 16-bit UTMI+ - 4'h9 : When the MAC interface is 8-bit UTMI+ Note:Programing Guide Section "Choosing the Value of GUSBCFG.USBTrdTim" consider mis-sampling into account whereas above values are without mis-sampling. During the AHB Clock Frequency selection, it is recommended to consider mis-sampling into account for USBTrdTim. Note: The previous values are calculated for the minimum AHB frequency of 30 MHz. USB turn-around time is critical for certification where long cables and 5-Hubs are used. If you need the AHB to run at less than 30 MHz, and if USB turnaround time is not critical, these bits can be programmed to a larger value. Default Value: 0x5

24.1.4 USBHS_DWC_otg_intreg_GUSBCFG (continued)

0x5: TURNTIME16BIT :

MAC interface is 16-bit UTMI+.

0x9: TURNTIME8BIT :

MAC interface is 8-bit UTMI+.

6	PHYSel	PHYSel Mode: Host and Device USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver Select (PHYSel) The application uses this bit to select either a high-speed UTMI+ or ULPI PHY, or a full-speed transceiver. - 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY - 1'b1: USB 1.1 full-speed serial transceiver If a USB 1.1 Full-Speed Serial Transceiver interface was not selected in, this bit is always 0, with Write Only access. If a high-speed PHY interface was not selected in, this bit is always 1, with Write Only access. If both interface types were selected (parameters have non-zero values), the application uses this bit to select which interface is active, and access is Read and Write. Default Value: 0x0 **0x1: USB11 :** USB 1.1 full-speed serial transceiver is selected **0x0: USB20 :** USB 2.0 high-speed UTMI+ or ULPI PHY is selected
5	FSIntf	Mode: Host and Device Full-Speed Serial Interface Select (FSIntf) The application uses this bit to select either a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. - 1'b0: 6-pin unidirectional full-speed serial interface - 1'b1: 3-pin bidirectional full-speed serial interface If a USB 1.1 Full-Speed Serial Transceiver interface was not selected, this bit is always 0, with Write Only access. If a USB 1.1 FS interface was selected, Then the application can Set this bit to select between the 3- and 6-pin interfaces, and access is Read and Write. Note: For supporting the new 4-pin bi-directional interface, you need to select 6-pin unidirectional FS serial mode, and add an external control to convert it to a 4-pin interface. Default Value: 0x0 **0x1: FS3PIN :** 3-pin bidirectional full-speed serial interface **0x0: FS6PIN :** 6-pin unidirectional full-speed serial interface
4	ULPI_UTMI_Sel	Mode: Host and Device ULPI or UTMI+ Select (ULPI_UTMI_Sel) The application uses this bit to select either a UTMI+ interface or ULPI Interface. - 1'b0: UTMI+ Interface - 1'b1: ULPI Interface Default Value: 0x0 **0x1: ULPI :** ULPI Interface

24.1.4 USBHS_DWC_otg_intreg_GUSBCFG (continued)

		0x0: UTMI : UTMI+ Interface
3	PHYIf	Mode: Host and Device PHY Interface (PHYIf) The application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. When a ULPI PHY is chosen, this must be Set to 8-bit mode. - 1'b0: 8 bits - 1'b1: 16 bits This bit is writable only If UTMI+ and ULPI were selected. Otherwise, this bit returns the value for the power-on interface selected during configuration. Default Value: 0x0 **0x1: BITS16 :** PHY 16bit Mode **0x0: BITS8 :** PHY 8bit Mode
2 : 0	TOutCal	Mode: Host and Device HS/FS Timeout Calibration (TOutCal) The number of PHY clocks that the application programs in this field is added to the high-speed/full-speed interpacket timeout duration in the core to account for any additional delays introduced by the PHY. This can be required, because the delay introduced by the PHY in generating the linestate condition can vary from one PHY to another. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of enumeration. The number of bit times added per PHY clock are as follows: High-speed operation: - One 30-MHz PHY clock = 16 bit times - One 60-MHz PHY clock = 8 bit times Full-speed operation: - One 30-MHz PHY clock = 0.4 bit times - One 60-MHz PHY clock = 0.2 bit times - One 48-MHz PHY clock = 0.25 bit times Default Value: 0x0 **0x5: FIVE :** Add 5 PHY clocks **0x4: FOUR :** Add 4 PHY clocks **0x1: ONE :** Add 1 PHY clocks **0x7: SEVEN :** Add 7 PHY clocks **0x6: SIX :** Add 6 PHY clocks

24.1.4 USBHS_DWC_otg_intreg_GUSBCFG (continued)

0x3: THREE :

Add 3 PHY clocks

0x2: TWO :

Add 2 PHY clocks

0x0: ZERO :

Add 0 PHY clocks

24.1.5 USBHS_DWC_otg_intreg_GRSTCTL

Description: The application uses this register to reset various hardware features inside the controller.

Address: 0x44900010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	Reserved	RW	RW	RW
HW Access					Reserved			
Name	TxFNum [7:6]		TxFFlsh	RxFFlsh	Reserved	FrmCntrRst	PIUFSSf-tRst	CSftRst

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved							
Name	Reserved [15:11]					TxFNum [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	RW	Reserved				
HW Access				Reserved				
Name	AHBIdle	DMAReq	CSftRst-Done	Reserved [28:24]				

Bits	Name	Description
31	AHBIdle	Mode: Host and Device AHB Master Idle (AHBIdle) Indicates that the AHB Master State Machine is in the IDLE condition. Default Value: 0x1 **0x1: ACTIVE :** AHB Master Idle **0x0: INACTIVE :** Not Idle
30	DMAReq	Mode: Host and Device DMA Request Signal (DMAReq) Indicates that the DMA request is in progress. Used for debug. Default Value: 0x0 **0x1: ACTIVE :** DMA request is in progress

24.1.5 USBHS_DWC_otg_intreg_GRSTCTL (continued)

		0x0: INACTIVE : No DMA request
29	CSftRstDone	Mode: Host and Device Core Soft Reset Done (CSftRstDone) The core sets this bit when all the necessary logic is reset in the core.This bit is cleared by the application along with GRSTCTL.CSftRst (bit 0) Default Value: 0x0 **0x1: ACTIVE :** Core Soft Reset is done **0x0: INACTIVE :** No reset
10 : 6	TxFNum	Mode: Host and Device TxFIFO Number (TxFNum) This is the FIFO number that must be flushed using the TxFIFO Flush bit. This field must not be changed until the core clears the TxFIFO Flush bit. - 5'h0: -- Non-periodic TxFIFO flush in Host mode -- Non-periodic TxFIFO flush in device mode when in shared FIFO operation -- Tx FIFO 0 flush in device mode when in dedicated FIFO mode - 5'h1: -- Periodic TxFIFO flush in Host mode -- Periodic TxFIFO 1 flush in Device mode when in shared FIFO operation -- TXFIFO 1 flush in device mode when in dedicated FIFO mode - 5'h2: -- Periodic TxFIFO 2 flush in Device mode when in shared FIFO operation -- TXFIFO 2 flush in device mode when in dedicated FIFO mode ... - 5'hF -- Periodic TxFIFO 15 flush in Device mode when in shared FIFO operation -- TXFIFO 15 flush in device mode when in dedicated FIFO mode - 5'h10: Flush all the transmit FIFOs in device or host mode Default Value: 0x0 **0x0: TXF0 :** :DWC_DESIGN_ID==0>-Periodic TxFIFO flush in host mode -Periodic TxFIFO 0 flush in device mode when in shared FIFO operation -TXFIFO 0 flush in device mode when in dedicated FIFO mode **0x1: TXF1 :** :DWC_DESIGN_ID==0>-Periodic TxFIFO flush in host mode -Periodic TxFIFO 1 flush in device mode when in shared FIFO operation -TXFIFO 1 flush in device mode when in dedicated FIFO mode **0xa: TXF10 :** -Periodic TxFIFO 10 flush in device mode when in shared FIFO operation -TXFIFO 10 flush in device mode when in dedicated FIFO mode **0xb: TXF11 :** -Periodic TxFIFO 11 flush in device mode when in shared FIFO operation -TXFIFO 11 flush in device mode when in dedicated FIFO mode

24.1.5 USBHS_DWC_otg_intreg_GRSTCTL (continued)

0xc: TXF12 :

-Periodic TxFIFO 12 flush in device mode when in shared FIFO operation -TXFIFO 12 flush in device mode when in dedicated FIFO mode

0xd: TXF13 :

-Periodic TxFIFO 13 flush in Device mode when in shared FIFO operation -TXFIFO 13 flush in device mode when in dedicated FIFO mode

0xe: TXF14 :

-Periodic TxFIFO 14 flush in Device mode when in shared FIFO operation -TXFIFO 14 flush in device mode when in dedicated FIFO mode

0xf: TXF15 :

-Periodic TxFIFO 15 flush in Device mode when in shared FIFO operation - TXFIFO 15 flush in device mode when in dedicated FIFO mode

0x10: TXF16 :

Flush all the transmit FIFOs:DWC_DESIGN_ID==0> in device or host mode

0x2: TXF2 :

:DWC_DESIGN_ID==0>-Periodic TxFIFO 2 flush in device mode when in shared FIFO operation -TXFIFO 2 flush in device mode when in dedicated FIFO mode

0x3: TXF3 :

:DWC_DESIGN_ID==0>-Periodic TxFIFO 3 flush in device mode when in shared FIFO operation -TXFIFO 3 flush in device mode when in dedicated FIFO mode

0x4: TXF4 :

:DWC_DESIGN_ID==0>-Periodic TxFIFO 4 flush in device mode when in shared FIFO operation -TXFIFO 4 flush in device mode when in dedicated FIFO mode

0x5: TXF5 :

:DWC_DESIGN_ID==0>-Periodic TxFIFO 5 flush in device mode when in shared FIFO operation -TXFIFO 5 flush in device mode when in dedicated FIFO mode

0x6: TXF6 :

:DWC_DESIGN_ID==0>-Periodic TxFIFO 6 flush in device mode when in shared FIFO operation -TXFIFO 6 flush in device mode when in dedicated FIFO mode

0x7: TXF7 :

:DWC_DESIGN_ID==0>-Periodic TxFIFO 7 flush in device mode when in shared FIFO operation -TXFIFO 7 flush in device mode when in dedicated FIFO mode

0x8: TXF8 :

:DWC_DESIGN_ID==0>-Periodic TxFIFO 8 flush in device mode when in shared FIFO operation -TXFIFO 8 flush in device mode when in dedicated FIFO mode

24.1.5 USBHS_DWC_otg_intreg_GRSTCTL (continued)

		0x9: TXF9 : -Periodic TxFIFO 9 flush in device mode when in shared FIFO operation -TXFIFO 9 flush in device mode when in dedicated FIFO mode
5	TxFFlsh	Mode: Host and Device TxFIFO Flush (TxFFlsh) This bit selectively flushes a single or all transmit FIFOs, but cannot do so If the core is in the midst of a transaction. The application must write this bit only after checking that the core is neither writing to the TxFIFO nor reading from the TxFIFO. Verify using these registers: - ReadNAK Effective Interrupt ensures the core is not reading from the FIFO - WriteGRSTCTL.AHBIdle ensures the core is not writing anything to the FIFO. Flushing is normally recommended when FIFOs are reconfigured or when switching between Shared FIFO and Dedicated Transmit FIFO operation. FIFO flushing is also recommended during device endpoint disable. The application must wait until the core clears this bit before performing any operations. This bit takes eight clocks to clear, using the slower clock of phy_clk or hclk. Default Value: 0x0 **0x1: ACTIVE :** Selectively flushes a single or all transmit FIFOs **0x0: INACTIVE :** No Flush
4	RxFFlsh	Mode: Host and Device RxFIFO Flush (RxFFlsh) The application can flush the entire RxFIFO using this bit, but must first ensure that the core is not in the middle of a transaction. The application must only write to this bit after checking that the controller is neither reading from the RxFIFO nor writing to the RxFIFO. The application must wait until the bit is cleared before performing any other operations. This bit requires eight clocks (slowest of PHY or AHB clock) to clear. Default Value: 0x0 **0x1: ACTIVE :** Flushes the entire RxFIFO **0x0: INACTIVE :** Does not flush the entire RxFIFO
2	FrmCntrRst	Mode: Host only Host Frame Counter Reset (FrmCntrRst) The application writes this bit to reset the (micro)Frame number counter inside the core. When the (micro)Frame counter is reset, the subsequent SOF sent out by the core has a (micro)Frame number of 0. When application writes 1 to the bit, it might not be able to read back the value as it will get cleared by the core in a few clock cycles. Default Value: 0x0 **0x1: ACTIVE :** Host Frame Counter Reset

24.1.5 USBHS_DWC_otg_intreg_GRSTCTL (continued)

		0x0: NOTACTIVE : No reset
1	PIUFSSftRst	Mode: Host and Device PIU FS Dedicated Controller Soft Reset (PIUFSSftRst) Resets the PIU FS Dedicated Controller All module state machines in FS Dedicated Controller of PIU are reset to the IDLE state. Used to reset the FS Dedicated controller in PIU in case of any PHY Errors like Loss of activity or Babble Error resulting in the PHY remaining in RX state for more than one frame boundary. This is a self clearing bit and core clears this bit after all the necessary logic is reset in the core. Default Value: 0x0 **0x1: RESET_ACTIVE :** PIU FS Dedicated Controller Soft Reset **0x0: RESET_INACTIVE :** No Reset
0	CSftRst	Mode: Host and Device Core Soft Reset (CSftRst) Resets the hclk and phy_clock domains as follows: - Clears the interrupts and all the CSR registers except the following register bits: -- PCGCCTL.RstPdwnModule -- PCGCCTL.GateHclk -- PCGCCTL.PwrClmp -- PCGCCTL.StopPPhyLPwrClkSelclk -- GUSBCFG.ForceDevMode -- GUSBCFG.ForceHstMode -- GUSBCFG.PhyLPwrClkSel -- GUSBCFG.DDRSel -- GUSBCFG.PHYSel -- GUSBCFG.FSIntf -- GUSBCFG.ULPI_UTMI_Sel -- GUSBCFG.PHYIf -- GUSBCFG.TxEndDelay -- GUSBCFG.TermSelDLPulse -- GUSBCFG.ULPIClkSusM -- GUSBCFG.ULPIAutoRes -- GUSBCFG.ULPIFsLs -- GGPIO -- GPWRDN -- GADPCTL -- HCFG.FSLSPclkSel -- DCFG.DevSpd -- DCTL.SftDiscon - All module state machines - All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed. - Any transactions on the AHB Master are terminated as soon as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. - When Hibernation or ADP feature is enabled, the PMU module is not reset by the Core Soft Reset. The application can write to this bit any time it wants to reset the core. The application must clear this bit after checking the bit 29 of this regiser (Core Soft Reset Done). Software must also must check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation. Typically software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation. Default Value: 0x0

24.1.5 USBHS_DWC_otg_intreg_GRSTCTL (continued)

0x1: ACTIVE :

Resets hclk and phy_clock domains

0x0: NOTACTIVE :

No reset

24.1.6 USBHS_DWC_otg_intreg_GINTSTS

Description: This register interrupts the application for system-level events in the current mode (Device mode or Host mode). Some of the bits in this register are valid only in Host mode, while others are valid in Device mode only. This register also indicates the current mode. To clear the interrupt status bits of type R_SS_WC, the application must write 1'b1 to the bit. The FIFO status interrupts are read only; once software reads from or writes to the FIFO while servicing these interrupts, FIFO interrupt conditions are cleared automatically. The application must clear the GINTSTS register at initialization before unmasking the interrupt bit to avoid any interrupts generated prior to initialization. Note: Read the reset value of GINTSTS.CurMod only after the following conditions: - If IDDIG_FILTER is disabled, read only after PHY clock is stable. - If IDDIG_FILTER is enabled, read only after the filter timer expires.

Address: 0x44900014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	RW	R	RW	R
HW Access								
Name	GOUT-NakEff	GINNakEff	NPTxFEmp	RxFLvl	Sof	OTGInt	ModeMis	CurMod

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	Reserved	
HW Access							Reserved	
Name	EOPF	ISOOutDrop	EnumDone	USBRst	USBSusp	ErlySusp	Reserved [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	R	R	RW	Reserved
HW Access								Reserved
Name	ResetDet	FetSusp	incomplP	incompISO-IN	OEPInt	IEPInt	EPMis	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	R	R	R
HW Access								
Name	WkUpInt	SessReqInt	DisconnInt	ConIDSt-sChng	LPM_Int	PTxFEmp	HChInt	PrtInt

Bits	Name	Description
31	WkUpInt	Mode: Host and Device Resume/Remote Wakeup Detected Interrupt (WkUpInt) Wakeup Interrupt during Suspend(L2) or LPM(L1) state. - During Suspend(L2): -- Device Mode: This interrupt is asserted only when Host Initiated Resume is detected on USB. -- Host Mode: This interrupt is asserted only when Device Initiated Remote Wakeup is detected on USB. For more information, see 'Partial Power-Down and Clock Gating Programming Model' in the Programming Guide. - During LPM(L1): -- Device Mode: This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. -- Host Mode: This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. For more information, see 'LPM Entry and Exit Programming Model' in the Programming Guide. Default Value: 0x0

24.1.6 USBHS_DWC_otg_intreg_GINTSTS (continued)

		0x1: ACTIVE : Resume or Remote Wakeup Detected Interrupt **0x0: INACTIVE :** Not active
30	SessReqInt	Mode: Host and Device Session Request/New Session Detected Interrupt (SessReqInt) In Host mode, this interrupt is asserted when a session request is detected from the device. In Host mode, this interrupt is asserted when a session request is detected from the device. In Device mode, this interrupt is asserted when the utmisrp_bvalid signal goes high. For more information on how to use this interrupt, see 'Partial Power-Down and Clock Gating Programming Model' in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** Session Request New Session Detected Interrupt **0x0: INACTIVE :** Not active
29	DisconnInt	Mode: Host only Disconnect Detected Interrupt (DisconnInt) Asserted when a device disconnect is detected. Default Value: 0x0 **0x1: ACTIVE :** Disconnect Detected Interrupt **0x0: INACTIVE :** Not active
28	ConIDStsChng	Mode: Host and Device Connector ID Status Change (ConIDStsChng) The core sets this bit when there is a change in connector ID status. Default Value: 0x0 **0x1: ACTIVE :** Connector ID Status Change **0x0: INACTIVE :** Not Active
27	LPM_Int	Mode: Host and Device LPM Transaction Received Interrupt (LPM_Int). - Device Mode: This interrupt is asserted when the device receives an LPM transaction and responds with a non-ERRORed response. - Host Mode: This interrupt is asserted when the device responds to an LPM transaction with a non-ERRORed response or when the host core has completed LPM transactions for the programmed number of times (GLPMCFG.RetryCnt). Default Value: 0x0

24.1.6 USBHS_DWC_otg_intreg_GINTSTS (continued)

		0x1: ACTIVE : LPM Transaction Received Interrupt **0x0: INACTIVE :** Not Active
26	PTxFEmp	Mode: Host only Periodic TxFIFO Empty (PTxFEmp) This interrupt is asserted when the Periodic Transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the Periodic Request Queue. The half or completely empty status is determined by the Periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.PTxFEmpLvl). Default Value: 0x1 **0x1: ACTIVE :** Periodic TxFIFO Empty **0x0: INACTIVE :** Not active
25	HChInt	Mode: Host only Host Channels Interrupt (HChInt) The core sets this bit to indicate that an interrupt is pending on one of the channels of the core (in Host mode). The application must read the Host All Channels Interrupt (HAINT) register to determine the exact number of the channel on which the interrupt occurred, and Then read the corresponding Host Channel-n Interrupt (HCINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the HCINTn register to clear this bit. Default Value: 0x0 **0x1: ACTIVE :** Host Channels Interrupt **0x0: INACTIVE :** Not active
24	PrtInt	Mode: Host only Host Port Interrupt (PrtInt) The core sets this bit to indicate a change in port status of one of the controller ports in Host mode. The application must read the Host Port Control and Status (HPRT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the Host Port Control and Status register to clear this bit. Default Value: 0x0 **0x1: ACTIVE :** Host Port Interrupt **0x0: INACTIVE :** Not active

24.1.6 USBHS_DWC_otg_intreg_GINTSTS (continued)

23	ResetDet	Mode: Device only Reset detected Interrupt (ResetDet) In Device mode, this interrupt is asserted when a reset is detected on the USB in partial power-down mode when the device is in Suspend. In Host mode, this interrupt is not asserted. Default Value: 0x0 **0x1: ACTIVE :** Reset detected Interrupt **0x0: INACTIVE :** Not active
22	FetSusp	Mode: Device only Data Fetch Suspended (FetSusp) This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data. For IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application for an endpoint mismatch algorithm. For example, after detecting an endpoint mismatch, the application: - Sets a Global non-periodic IN NAK handshake - Disables IN endpoints - Flushes the FIFO - Determines the token sequence from the IN Token Sequence Learning Queue - Re-enables the endpoints - Clears the Global non-periodic IN NAK handshake If the Global non-periodic IN NAK is cleared, the core has not yet fetched data for the IN endpoint, and the IN token is received. The core generates an 'IN token received when FIFO empty' interrupt. It then sends the host a NAK response. To avoid this scenario, the application can check the GINTSTS.FetSusp interrupt, which ensures that the FIFO is full before clearing a Global NAK handshake. Alternatively, the application can mask the IN token received when FIFO empty interrupt when clearing a Global IN NAK handshake. Default Value: 0x0 **0x1: ACTIVE :** Data Fetch Suspended **0x0: INACTIVE :** Not active
21	incomplP	Incomplete Periodic Transfer (incomplP) Mode: Host only In Host mode, the core sets this interrupt bit when there are incomplete periodic transactions still pending which are scheduled for the current microframe. Incomplete Isochronous OUT Transfer (incompISOOUT) Mode: Device only The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register. Default Value: 0x0 **0x1: ACTIVE :** Incomplete Periodic Transfer **0x0: INACTIVE :** Not active

24.1.6 USBHS_DWC_otg_intreg_GINTSTS (continued)

20	incompISOIN	Mode: Device only Incomplete Isochronous IN Transfer (incompISOIN) The core sets this interrupt to indicate that there is at least one isochronous IN endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register. Note: This interrupt is not asserted in Scatter/Gather DMA mode. Default Value: 0x0 **0x1: ACTIVE :** Incomplete Isochronous IN Transfer **0x0: INACTIVE :** Not active
19	OEPInt	Mode: Device only OUT Endpoints Interrupt (OEPInt) The controller sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and then read the corresponding Device OUT Endpoint-n Interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DOEPINTn register to clear this bit. Default Value: 0x0 **0x1: ACTIVE :** OUT Endpoints Interrupt **0x0: INACTIVE :** Not active
18	IEPInt	Mode: Device only IN Endpoints Interrupt (IEPInt) The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the IN endpoint on Device IN Endpoint-n Interrupt (DIEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit. Default Value: 0x0 **0x1: ACTIVE :** IN Endpoints Interrupt **0x0: INACTIVE :** Not active
17	EPMis	Mode: Device only Endpoint Mismatch Interrupt (EPMis) Note: This interrupt is valid only in shared FIFO operation. Indicates that an IN token has been received for a non-periodic endpoint, but the data for another endpoint is present in the top of the Non-periodic Transmit FIFO and the IN endpoint mismatch count programmed by the application has expired. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Mismatch Interrupt

24.1.6 USBHS_DWC_otg_intreg_GINTSTS (continued)

		0x0: INACTIVE : Not active
15	EOPF	Mode: Device only End of Periodic Frame Interrupt (EOPF) Indicates that the period specified in the Periodic Frame Interval field of the Device Configuration register (DCFG.PerFrInt) has been reached in the current microframe. In case of Non-Ignore Frame Number Scatter/Gather (Descriptor DMA) mode, the controller internally handles the following scenarios based on EOPF: Read Flush: At the EOPF, the controller checks if there are any pending packets in the FIFO corresponding to the current (micro)Frame. - If there are any pending packets, then the controller initiates read flush, due to which the read pointer is updated to the starting location of the next micro-frame packet. - If there are no pending packets corresponding to the current (micro)Frame, the controller does not take any action. Write Flush: At the EOPF, if the controller is still fetching the current micro-frame data, then the controller stops pushing data into the TXFIFO but keeps fetching the complete packet from the System Memory. After completing the scheduled packet size fetch, the controller updates the Status Quadlet Fields (Transmit Status to BUFFLUSH) and closes the Descriptor. During the descriptor close, the controller initiates write flush, due to which the write pointer is updated to the starting location of the next micro-frame packet. Because the controller stops pushing the packet to the TxFIFO after EOPF, to bring the write pointer to the starting location of the next micro-frame, write flush is done. Default Value: 0x0 **0x1: ACTIVE :** End of Periodic Frame Interrupt **0x0: INACTIVE :** Not active
14	ISOOutDrop	Mode: Device only Isochronous OUT Packet Dropped Interrupt (ISOOutDrop) The controller sets this bit when it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** Isochronous OUT Packet Dropped Interrupt **0x0: INACTIVE :** Not active
13	EnumDone	Mode: Device only Enumeration Done (EnumDone) The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed. Default Value: 0x0 **0x1: ACTIVE :** Enumeration Done **0x0: INACTIVE :** Not active

24.1.6 USBHS_DWC_otg_intreg_GINTSTS (continued)

12	USBRst	Mode: Device only USB Reset (USBRst) The controller sets this bit to indicate that a reset is detected on the USB. Default Value: 0x0 **0x1: ACTIVE :** USB Reset **0x0: INACTIVE :** Not active
11	USBSusp	Mode: Device only USB Suspend (USBSusp) The controller sets this bit to indicate that a suspend was detected on the USB. The controller enters the Suspended state when there is no activity on the linestate signal for an extended period of time. Default Value: 0x0 **0x1: ACTIVE :** USB Suspend **0x0: INACTIVE :** Not Active
10	ErlySusp	Mode: Device only Early Suspend (ErlySusp) The controller sets this bit to indicate that an Idle state has been detected on the USB for 3 ms. Default Value: 0x0 **0x1: ACTIVE :** 3ms of Idle state detected **0x0: INACTIVE :** No Idle state detected
7	GOUTNakEff	Mode: Device only Global OUT NAK Effective (GOUTNakEff) Indicates that the Set Global OUT NAK bit in the Device Control register (DCTL.SGOUTNak), Set by the application, has taken effect in the core. This bit can be cleared by writing the Clear Global OUT NAK bit in the Device Control register (DCTL.CGOUTNak). Default Value: 0x0 **0x1: ACTIVE :** Global OUT NAK Effective **0x0: INACTIVE :** Not Active

24.1.6 USBHS_DWC_otg_intreg_GINTSTS (continued)

6	GINNakEff	Mode: Device only Global IN Non-periodic NAK Effective (GINNakEff) Indicates that the Set Global Non-periodic IN NAK bit in the Device Control register (DCTL.SGNPInNak) set by the application, has taken effect in the core. That is, the core has sampled the Global IN NAK bit Set by the application. This bit can be cleared by clearing the Clear Global Non-periodic IN NAK bit in the Device Control register (DCTL.CGNPInNak). This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit. Default Value: 0x0 **0x1: ACTIVE :** Set Global Non-periodic IN NAK bit **0x0: INACTIVE :** Global Non-periodic IN NAK not active
5	NPTxFEmp	Mode: Host and Device Non-periodic TxFIFO Empty (NPTxFEmp) This interrupt is asserted when the Non-periodic TxFIFO is either half or completely empty, and there is space for at least one Entry to be written to the Non-periodic Transmit Request Queue. The half or completely empty status is determined by the Non-periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl). In host mode, the application can use GINTSTS.NPTxFEmp with the OTG_EN_DED_TX_FIFO parameter set to either 1 or 0. In device mode, the application uses GINTSTS.NPTxFEmp when OTG_EN_DED_TX_FIFO=0. When OTG_EN_DED_TX_FIFO=1, the application uses DIEPINTn.TxFEmp. Default Value: 0x1 **0x1: ACTIVE :** Non-periodic TxFIFO is empty **0x0: INACTIVE :** Non-periodic TxFIFO is not empty
4	RxFLvl	Mode: Host and Device RxFIFO Non-Empty (RxFLvl) Indicates that there is at least one packet pending to be read from the RxFIFO. Default Value: 0x0 **0x1: ACTIVE :** Rx Fifo is not empty **0x0: INACTIVE :** Rx Fifo is empty

24.1.6 USBHS_DWC_otg_intreg_GINTSTS (continued)

3	Sof	Mode: Host and Device Start of (micro)Frame (Sof) In Host mode, the core sets this bit to indicate that an SOF (FS), micro-SOF (HS), or Keep-Alive (LS) is transmitted on the USB. The application must write a 1 to this bit to clear the interrupt. In Device mode, the controller sets this bit to indicate that an SOF token has been received on the USB. The application can read the Device Status register to get the current (micro)Frame number. This interrupt is seen only when the core is operating at either HS or FS. This bit can be set only by the core and the application must write 1 to clear it. Note: This register may return 1'b1 if read immediately after power-on reset. If the register bit reads 1'b1 immediately after power-on reset, it does not indicate that an SOF has been sent (in case of host mode) or SOF has been received (in case of device mode). The read value of this interrupt is valid only after a valid connection between host and device is established. If the bit is set after power on reset the application can clear the bit. Default Value: 0x0 **0x1: ACTIVE :** Start of Frame **0x0: INTACTIVE :** No Start of Frame
2	OTGInt	Mode: Host and Device OTG Interrupt (OTGInt) The controller sets this bit to indicate an OTG protocol event. The application must read the OTG Interrupt Status (GOTGINT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the GOTGINT register to clear this bit. Default Value: 0x0 **0x1: ACTIVE :** OTG Interrupt **0x0: INACTIVE :** No Interrupt
1	ModeMis	Mode: Host and Device Mode Mismatch Interrupt (ModeMis) The core sets this bit when the application is trying to access: - A Host mode register, when the controller is operating in Device mode - A Device mode register, when the controller is operating in Host mode The register access is completed on the AHB with an OKAY response, but is ignored by the controller internally and does not affect the operation of the controller. This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** Mode Mismatch Interrupt **0x0: INACTIVE :** No Mode Mismatch Interrupt

24.1.6 USBHS_DWC_otg_intreg_GINTSTS (continued)

0	CurMod	Mode: Host and Device Current Mode of Operation (CurMod) Indicates the current mode. - 1'b0: Device mode - 1'b1: Host mode Note: The reset value of this register field can be read only after the PHY clock is stable, or if IDDIG_FILTER is enabled, wait for the filter timer to expire to read the correct reset value which ever event is later. Default Value: 0x0 **0x0: DEVICE :** Device mode **0x1: HOST :** Host mode

24.1.7 USBHS_DWC_otg_intreg_GINTMSK

Description: This register works with the Interrupt Register (GINTSTS) to interrupt the application. When an interrupt bit is masked, the interrupt associated with that bit is not generated. However, the GINTSTS register bit corresponding to that interrupt is still set. Note: The fields of this register change depending on host or device mode.

Address: 0x44900018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	Reserved
HW Access								Reserved
Name	GOUT-NakEffMsk	GINNakEf-fMsk	NPTx-FEmpMsk	RxFLvlMsk	SofMsk	OTGIntMsk	Mode-MisMsk	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	Reserved	
HW Access							Reserved	
Name	EOPFMsk	ISOOut-DropMsk	Enum-DoneMsk	USBRstMsk	USBSus-pMsk	ErlySus-pMsk	Reserved [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	Reserved	RW	RW	RW	Reserved
HW Access				Reserved				Reserved
Name	ResetDe-tMsk	FetSus-pMsk	incom-plPMsK	Reserved	OEPIntMsk	IEPIntMsk	EPMisMsk	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	Wk-UpIntMsk	Sess-ReqIntMsk	Discon-nIntMsk	ConIDSt-sChngMsk	LP-M_IntMsk	PTx-FEmpMsk	HChIntMsk	PrtIntMsk

Bits	Name	Description
31	WkUpIntMsk	Mode: Host and Device Resume/Remote Wakeup Detected Interrupt Mask (WkUpIntMsk) The WakeUp bit is used for LPM state wake up in a way similar to that of wake up in suspend state. Default Value: 0x0 **0x0: MASK :** Resume or Remote Wakeup Detected Interrupt Mask **0x1: NOMASK :** Unmask Resume Remote Wakeup Detected Interrupt
30	SessReqIntMsk	Mode: Host and Device Session Request/New Session Detected Interrupt Mask (SessReqIntMsk) Default Value: 0x0 **0x0: MASK :** Session Request or New Session Detected Interrupt Mask

24.1.7 USBHS_DWC_otg_intreg_GINTMSK (continued)

		0x1: NOMASK : No Session Request or New Session Detected Interrupt Mask
29	DisconnIntMsk	Mode: Host and Device Disconnect Detected Interrupt Mask (DisconnIntMsk) Default Value: 0x0 **0x0: MASK :** Disconnect Detected Interrupt Mask **0x1: NOMASK :** No Disconnect Detected Interrupt Mask
28	ConIDStsChngMsk	Mode: Host and Device Connector ID Status Change Mask (ConIDStsChngMsk) Default Value: 0x0 **0x0: MASK :** Connector ID Status Change Mask **0x1: NOMASK :** No Connector ID Status Change Mask
27	LPM_IntMsk	Mode: Host and Device LPM Transaction Received Interrupt (LPM_Int) LPM Transaction received interrupt Mask Default Value: 0x0 **0x0: MASK :** LPM Transaction received interrupt Mask **0x1: NOMASK :** No LPM Transaction received interrupt Mask
26	PTxFEmpMsk	Mode: Host only Periodic TxFIFO Empty Mask (PTxFEmpMsk) Default Value: 0x0 **0x0: MASK :** Periodic TxFIFO Empty Mask **0x1: NOMASK :** No Periodic TxFIFO Empty Mask
25	HChIntMsk	Mode: Host only Host Channels Interrupt Mask (HChIntMsk) Default Value: 0x0 **0x0: MASK :** Host Channels Interrupt Mask

24.1.7 USBHS_DWC_otg_intreg_GINTMSK (continued)

		0x1: NOMASK : No Host Channels Interrupt Mask
24	PrtIntMsk	Mode: Host only Host Port Interrupt Mask (PrtIntMsk) Default Value: 0x0 **0x0: MASK :** Host Port Interrupt Mask **0x1: NOMASK :** No Host Port Interrupt Mask
23	ResetDetMsk	Mode: Device only Reset detected Interrupt Mask (ResetDetMsk) Default Value: 0x0 **0x0: MASK :** Reset detected Interrupt Mask **0x1: NOMASK :** No Reset detected Interrupt Mask
22	FetSuspMsk	Mode: Device only Data Fetch Suspended Mask (FetSuspMsk) Default Value: 0x0 **0x0: MASK :** Data Fetch Suspended Mask **0x1: NOMASK :** No Data Fetch Suspended Mask
21	incomplPMsK	Incomplete Periodic Transfer Mask (incomplPMsk) Mode: Host only Incomplete Isochronous OUT Transfer Interrupt Mask (incompISOOUTMsk) Mode: Device only Default Value: 0x0 **0x0: MASK :** :cbc:1:0> Host mode: Incomplete Periodic Transfer Mask:cbc:1:0> Device mode: Incomplete Isochronous OUT Transfer Mask **0x1: NOMASK :** :cbc:1:0> Host mode: No Incomplete Periodic Transfer Mask:cbc:1:0> Device mode: No Incomplete Isochronous OUT Transfer Mask
19	OEPIntMsk	Mode: Device only OUT Endpoints Interrupt Mask (OEPIntMsk) Default Value: 0x0

24.1.7 USBHS_DWC_otg_intreg_GINTMSK (continued)

		0x0: MASK : OUT Endpoints Interrupt Mask **0x1: NOMASK :** No OUT Endpoints Interrupt Mask
18	IEPIntMsk	Mode: Device only IN Endpoints Interrupt Mask (IEPIntMsk) Default Value: 0x0 **0x0: MASK :** IN Endpoints Interrupt Mask **0x1: NOMASK :** No IN Endpoints Interrupt Mask
17	EPMisMsk	Mode: Device only Endpoint Mismatch Interrupt Mask (EPMisMsk) Default Value: 0x0 **0x0: MASK :** Endpoint Mismatch Interrupt Mask **0x1: NOMASK :** No Endpoint Mismatch Interrupt Mask
15	EOPFMsk	Mode: Device only End of Periodic Frame Interrupt Mask (EOPFMsk) Default Value: 0x0 **0x0: MASK :** End of Periodic Frame Interrupt Mask **0x1: NOMASK :** No End of Periodic Frame Interrupt Mask
14	ISOOutDropMsk	Mode: Device only Isochronous OUT Packet Dropped Interrupt Mask (ISOOutDropMsk) Default Value: 0x0 **0x0: MASK :** Isochronous OUT Packet Dropped Interrupt Mask **0x1: NOMASK :** No Isochronous OUT Packet Dropped Interrupt Mask
13	EnumDoneMsk	Mode: Device only Enumeration Done Mask (EnumDoneMsk) Default Value: 0x0

24.1.7 USBHS_DWC_otg_intreg_GINTMSK (continued)

		0x0: MASK : Enumeration Done Mask **0x1: NOMASK :** No Enumeration Done Mask
12	USBRstMsk	Mode: Device only USB Reset Mask (USBRstMsk) Default Value: 0x0 **0x0: MASK :** USB Reset Mask **0x1: NOMASK :** No USB Reset Mask
11	USBSuspMsk	Mode: Device only USB Suspend Mask (USBSuspMsk) Default Value: 0x0 **0x0: MASK :** USB Suspend Mask **0x1: NOMASK :** No USB Suspend Mask
10	ErlySuspMsk	Mode: Device only Early Suspend Mask (ErlySuspMsk) Default Value: 0x0 **0x0: MASK :** Early Suspend Mask **0x1: NOMASK :** No Early Suspend Mask
7	GOUTNakEffMsk	Mode: Device only Global OUT NAK Effective Mask (GOUTNakEffMsk) Default Value: 0x0 **0x0: MASK :** Global OUT NAK Effective Mask **0x1: NOMASK :** No Global OUT NAK Effective Mask
6	GINNakEffMsk	Mode: Device only, Global Non-periodic IN NAK Effective Mask (GINNakEffMsk) Default Value: 0x0

24.1.7 USBHS_DWC_otg_intreg_GINTMSK (continued)

		0x0: MASK : Global Non-periodic IN NAK Effective Mask **0x1: NOMASK :** No Global Non-periodic IN NAK Effective Mask
5	NPTxFEmpMsk	Mode: Host and Device Non-periodic TxFIFO Empty Mask (NPTxFEmpMsk) Default Value: 0x0 **0x0: MASK :** Non-periodic TxFIFO Empty Mask **0x1: NOMASK :** No Non-periodic TxFIFO Empty Mask
4	RxFLvlMsk	Mode: Host and Device Receive FIFO Non-Empty Mask (RxFLvlMsk) Default Value: 0x0 **0x0: MASK :** Receive FIFO Non-Empty Mask **0x1: NOMASK :** No Receive FIFO Non-Empty Mask
3	SofMsk	Mode: Host and Device Start of (micro)Frame Mask (SofMsk) Default Value: 0x0 **0x0: MASK :** Start of Frame Mask **0x1: NOMASK :** No Start of Frame Mask
2	OTGIntMsk	Mode: Host and Device OTG Interrupt Mask (OTGIntMsk) Default Value: 0x0 **0x0: MASK :** OTG Interrupt Mask **0x1: NOMASK :** No OTG Interrupt Mask
1	ModeMisMsk	Mode: Host and Device Mode Mismatch Interrupt Mask (ModeMisMsk) Default Value: 0x0

24.1.7 USBHS_DWC_otg_intreg_GINTMSK (continued)

0x0: MASK :

Mode Mismatch Interrupt Mask

0x1: NOMASK :

No Mode Mismatch Interrupt Mask

24.1.8 USBHS_DWC_otg_intreg_GRXSTSR

Description: A read to the Receive Status Debug Read register returns the contents of the top of the Receive FIFO. The receive status contents must be interpreted differently in Host and Device modes. The core ignores the receive status read when the receive FIFO is empty and returns a value of 32'h0000_0000. Note: - Use of these fields vary based on whether the core is functioning as a host or a device. - Do not read this register's reset value before configuring the core because the read value is 'X' in the simulation.

Address: 0x4490001C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access								
Name	BCnt [7:4]				ChNum [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access								
Name	DPID	BCnt [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	R			R				R
HW Access								
Name	FN [23:21]			PktSts [20:17]				DPID

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							
Name	Reserved [31:25]							FN

Bits	Name	Description
24 : 21	FN	Mode: Device only Frame Number (FN) This is the least significant 4 bits of the (micro)Frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported. Default Value: 0x0
20 : 17	PktSts	Packet Status (PktSts) indicates the status of the received packet. In host mode, - 4'b0010: IN data packet received - 4'b0011: IN transfer completed (triggers an interrupt) - 4'b0101: Data toggle error (triggers an interrupt) - 4'b0111: Channel halted (triggers an interrupt) - Others: Reserved Reset:4'b0 In device mode, - 4'b0001: Global OUT NAK (triggers an interrupt) - 4'b0010: OUT data packet received - 4'b0011: OUT transfer completed (triggers an interrupt) - 4'b0100: SETUP transaction completed (triggers an interrupt) - 4'b0110: SETUP data packet received - Others: Reserved Reset:4'h0 Default Value: 0x0

24.1.8 USBHS_DWC_otg_intreg_GRXSTSR (continued)

0x7: CHHALT :

Channel halted in host mode (triggers an interrupt)

0x4: DSETUPCOM :

SETUP transaction completed :DWC_DESIGN_ID==0>in device mode (triggers an interrupt)

0x6: DSETUPRX :

SETUP data packet received:DWC_DESIGN_ID==0> in device mode

0x5: DTTOG :

Data toggle error (triggers an interrupt) in host mode

0x2: INOUTDPRX :

:DWC_DESIGN_ID==0>IN data packet received in host mode and OUT data packet received :DWC_DESIGN_ID==0>in device mode

0x3: INOUTTRCOM :

IN or OUT transfer completed :DWC_DESIGN_ID==0>in both host and device mode (triggers an interrupt)

0x1: OUTNAK :

Global OUT NAK :DWC_DESIGN_ID==0>in device mode (triggers an interrupt)

16 : 15 DPID

Data PID (DPID)
In host mode, indicates the Data PID of the received packet. In device mode, indicates the Data PID of the received OUT data packet.
- 2'b00: DATA0
- 2'b10: DATA1
- 2'b01: DATA2
- 2'b11: MDATA

Reset: 2'h0
Default Value: 0x0

0x0: DATA0 :

DATA0

0x2: DATA1 :

DATA1

0x1: DATA2 :

DATA2

0x3: MDATA :

MDATA

24.1.8 USBHS_DWC_otg_intreg_GRXSTSR (continued)

14 : 4	BCnt	Byte Count (BCnt) In host mode, indicates the byte count of the received IN data packet. In device mode, indicates the byte count of the received data packet. Default Value: 0x0
3 : 0	ChNum	Channel Number (ChNum) Mode: Host only Indicates the channel number to which the current received packet belongs. Endpoint Number (EPNum) Mode: Device only Indicates the endpoint number to which the current received packet belongs. Default Value: 0x0 **0x0: CHEP0 :** Channel or EndPoint 0 **0x1: CHEP1 :** Channel or EndPoint 1 **0xa: CHEP10 :** Channel or EndPoint 10 **0xb: CHEP11 :** Channel or EndPoint 11 **0xc: CHEP12 :** Channel or EndPoint 12 **0xd: CHEP13 :** Channel or EndPoint 13 **0xe: CHEP14 :** Channel or EndPoint 14 **0xf: CHEP15 :** Channel or EndPoint 15 **0x2: CHEP2 :** Channel or EndPoint 2 **0x3: CHEP3 :** Channel or EndPoint 3 **0x4: CHEP4 :** Channel or EndPoint 4

24.1.8 USBHS_DWC_otg_intreg_GRXSTSR (continued)

0x5: CHEP5 :

Channel or EndPoint 5

0x6: CHEP6 :

Channel or EndPoint 6

0x7: CHEP7 :

Channel or EndPoint 7

0x8: CHEP8 :

Channel or EndPoint 8

0x9: CHEP9 :

Channel or EndPoint 9

24.1.9 USBHS_DWC_otg_intreg_GRXSTSP

Description: A read to the Receive Status Read and Pop register returns the contents of the top of the Receive FIFO and additionally pops the top data entry out of the RxFIFO. The receive status contents must be interpreted differently in Host and Device modes. The core ignores the receive status pop/read when the receive FIFO is empty and returns a value of 32'h0000_0000. The application must only pop the Receive Status FIFO when the Receive FIFO Non-Empty bit of the Core Interrupt register (GINTSTS.RxFLvl) is asserted. Note: - Use of these fields vary based on whether the core is functioning as a host or a device. - Do not read this register's reset value before configuring the core because the read value is 'X' in the simulation.

Address: 0x44900020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access								
Name	BCnt [7:4]				ChNum [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access								
Name	DPID	BCnt [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	R			R				R
HW Access								
Name	FN [23:21]			PktSts [20:17]				DPID

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							
Name	Reserved [31:25]							FN

Bits	Name	Description
24 : 21	FN	Mode: Device only Frame Number (FN) This is the least significant 4 bits of the (micro)Frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported. Default Value: 0x0
20 : 17	PktSts	Packet Status (PktSts) indicates the status of the received packet. In host mode, - 4'b0010: IN data packet received - 4'b0011: IN transfer completed (triggers an interrupt) - 4'b0101: Data toggle error (triggers an interrupt) - 4'b0111: Channel halted (triggers an interrupt) - Others: Reserved Reset:4'b0 In device mode, - 4'b0001: Global OUT NAK (triggers an interrupt) - 4'b0010: OUT data packet received - 4'b0011: OUT transfer completed (triggers an interrupt) - 4'b0100: SETUP transaction completed (triggers an interrupt) - 4'b0110: SETUP data packet received - Others: Reserved Reset:4'h0 Default Value: 0x0

24.1.9 USBHS_DWC_otg_intreg_GRXSTSP (continued)

		0x4: DSETUPCOM : SETUP transaction completed :DWC_DESIGN_ID==0>in device mode (triggers an interrupt) **0x5: DTTOG :** Data toggle error (triggers an interrupt) in host mode **0x2: INOUTDPRX :** :DWC_DESIGN_ID==0>IN data packet received in host mode and OUT data packet received :DWC_DESIGN_ID==0>in device mode **0x3: INOUTTRCOM :** IN or OUT transfer completed :DWC_DESIGN_ID==0>in both host and device mode (triggers an interrupt) **0x1: OUTNAK :** Global OUT NAK :DWC_DESIGN_ID==0>in device mode (triggers an interrupt)
16 : 15	DPID	Data PID (DPID) In host mode, indicates the Data PID of the received packet. In device mode, indicates the Data PID of the received OUT data packet. - 2'b00: DATA0 - 2'b10: DATA1 - 2'b01: DATA2 - 2'b11: MDATA Reset: 2'h0 Default Value: 0x0 **0x0: DATA0 :** DATA0 **0x2: DATA1 :** DATA1 **0x1: DATA2 :** DATA2 **0x3: MDATA :** MDATA
14 : 4	BCnt	Byte Count (BCnt) In host mode, indicates the byte count of the received IN data packet. In device mode, indicates the byte count of the received data packet. Default Value: 0x0
3 : 0	ChNum	Channel Number (ChNum) Mode: Host only Indicates the channel number to which the current received packet belongs. Endpoint Number (EPNum) Mode: Device only Indicates the endpoint number to which the current received packet belongs. Default Value: 0x0

24.1.9 USBHS_DWC_otg_intreg_GRXSTSP (continued)

0x0: CHEP0 :

Channel or EndPoint 0

0x1: CHEP1 :

Channel or EndPoint 1

0xa: CHEP10 :

Channel or EndPoint 10

0xb: CHEP11 :

Channel or EndPoint 11

0xc: CHEP12 :

Channel or EndPoint 12

0xd: CHEP13 :

Channel or EndPoint 13

0xe: CHEP14 :

Channel or EndPoint 14

0xf: CHEP15 :

Channel or EndPoint 15

0x2: CHEP2 :

Channel or EndPoint 2

0x3: CHEP3 :

Channel or EndPoint 3

0x4: CHEP4 :

Channel or EndPoint 4

0x5: CHEP5 :

Channel or EndPoint 5

0x6: CHEP6 :

Channel or EndPoint 6

0x7: CHEP7 :

Channel or EndPoint 7

24.1.9 USBHS_DWC_otg_intreg_GRXSTSP (continued)

0x8: CHEP8 :

Channel or EndPoint 8

0x9: CHEP9 :

Channel or EndPoint 9

24.1.10 USBHS_DWC_otg_intreg_GRXFSIZ

Description: The application can program the RAM size that must be allocated to the RxFIFO.

Address: 0x44900024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	RxFDep [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [15:10]						RxFDep [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	RxFDep	Mode: Host and Device RxFIFO Depth (RxFDep) This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth during configuration. If Enable Dynamic FIFO Sizing is selected in coreConsultant, these flops are optimized, and reads return the power-on value. If Enable Dynamic FIFO Sizing is selected in coreConsultant, you can write a new value in this field. Programmed values must not exceed the power-on value. Default Value: 0x21F

24.1.11 USBHS_DWC_otg_intreg_GNPTXFSIZ

Description: The application can program the RAM size and the memory start address for the Non-periodic TxFIFO Note: The fields of this register change depending on host or device mode.

Address: 0x44900028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	NPTXFStAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [15:10]						NPTXFStAddr [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	NPTXFDep [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							
Name	Reserved [31:25]							NPTXFDep

Bits	Name	Description
24 : 16	NPTXFDep	Mode: Host only Non-periodic TxFIFO Depth (NPTxFDep) For host mode, this field is always valid. For device mode, this field is valid only when OTG_EN_DED_TX_FIFO=0. This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 This attribute of field is determined during coreConsultant configuration by "Enable Dynamic FIFO Sizing?" (OTG_DFIFO_DYNAMIC): - OTG_DFIFO_DYNAMIC = 0: These flops are optimized, and reads return the power-on value. - OTG_DFIFO_DYNAMIC = 1: The application can write a new value in this field. Programmed values must not exceed the power-on value set in coreConsultant. The power-on reset value of this field is specified during coreConsultant configuration as Largest IN Endpoint FIFO 0 Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_0). Default Value: 0x100
9 : 0	NPTXFStAddr	Non-periodic Transmit RAM Start Address (NPTxFStAddr) For host mode, this field is always valid. This field contains the memory start address for Non-periodic Transmit FIFO RAM. - This field is determined during coreConsultant configuration by "Enable Dynamic FIFO Sizing?" (OTG_DFIFO_DYNAMIC):OTG_DFIFO_DYNAMIC = 0 These flops are optimized, and reads return the power-on value. - OTG_DFIFO_DYNAMIC = 1 The application can write a new value in this field. Programmed values must not exceed the power-on value set in coreConsultant. Programmed values must not exceed the power-on value set in coreConsultant. The power-on reset value of this field is specified during coreConsultant configuration by Largest Rx Data FIFO Depth (parameter OTG_RX_DFIFO_DEPTH). Default Value: 0x21F

24.1.12 USBHS_DWC_otg_intreg_GNPTXSTS

Description: In Device mode, this register is valid only in Shared FIFO operation. This read-only register contains the free space information for the Non-periodic TxFIFO and the Non-periodic Transmit Request Queue.

Address: 0x4490002C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	NPTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	NPTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	NPTxQSpcAvail [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R						
HW Access	Reserved							
Name	Reserved	NPTxQTop [30:24]						

Bits	Name	Description
30 : 24	NPTxQTop	Top of the Non-periodic Transmit Request Queue (NPTxQTop) Entry in the Non-periodic Tx Request Queue that is currently being processed by the MAC. - Bits [30:27]: Channel/endpoint number - Bits [26:25]: - 2'b00: IN/OUT token -- 2'b01: Zero-length transmit packet (device IN/host OUT) -- 2'b10: PING/CSPLIT token -- 2'b11: Channel halt command - Bit [24]: Terminate (last Entry for selected channel/endpoint) Reset: 7'h0 Default Value: 0x0 **0x3: CHNHALT :** Channel halt command **0x0: INOUTTK :** IN/OUT token **0x2: PINGCSPLIT :** PING/CSPLIT token

24.1.12 USBHS_DWC_otg_intreg_GNPTXSTS (continued)

0x1: ZEROTX :

Zero-length transmit packet (device IN/host OUT)

23 : 16	NPTxQSpcAvail	Non-periodic Transmit Request Queue Space Available (NPTxQSpcAvail) Indicates the amount of free space available in the Non-periodic Transmit Request Queue. This queue holds both IN and OUT requests in Host mode. Device mode has only IN requests. - 8'h0: Non-periodic Transmit Request Queue is full - 8'h1: 1 location available - 8'h2: 2 locations available - n: n locations available (0 <= n <= 8) - Others: Reserved Reset: Configurable Default Value: 0x8

0x0: FULL :

Non-periodic Transmit Request Queue is full

0x1: QUE1 :

1 location available

0x2: QUE2 :

2 locations available

0x3: QUE3 :

3 locations available

0x4: QUE4 :

4 locations available

0x5: QUE5 :

5 locations available

0x6: QUE6 :

6 locations available

0x7: QUE7 :

7 locations available

0x8: QUE8 :

8 locations available

24.1.12 USBHS_DWC_otg_intreg_GNPTXSTS (continued)

15 : 0	NPTxFSpcAvail	Non-periodic TxFIFO Space Avail (NPTxFSpcAvail) Indicates the amount of free space available in the Non-periodic TxFIFO. Values are in terms of 32-bit words. - 16'h0: Non-periodic TxFIFO is full - 16'h1: 1 word available - 16'h2: 2 words available - 16'hn: n words available (where 0 <= n <= 32,768) - 16'h8000: 32,768 words available - Others: Reserved Reset: Configurable Default Value: 0x100

24.1.13 USBHS_DWC_otg_intreg_GGPIO

Description: The application can use this register for general purpose input/output ports or for debugging.

Address: 0x44900038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	GPI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	GPI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	GPO [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	GPO [31:24]							

Bits	Name	Description
31 : 16	GPO	General Purpose Output (GPO) This field is driven as an output from the core, gp_o[15:0]. The application can program this field to determine the corresponding value on the gp_o[15:0] output. Default Value: 0x0
15 : 0	GPI	General Purpose Input (GPI) This field's read value reflects the gp_i[15:0] core input value. Default Value: 0x0

24.1.14 USBHS_DWC_otg_intreg_GUID

Description: This is a read/write register containing the User ID. It is implemented only if Remove Optional Features? was deselected during coreConsultant configuration (parameter OTG_RM_OPT_FEATURES = 0). The power-on value for this register is specified as the Power-on Value of User ID Register User Identification Register during coreConsultant configuration (parameter OTG_USERID). This register can be used in the following ways: - To store the version or revision of your system - To store hardware configurations that are outside the DWC_otg core - As a scratch register

Address: 0x4490003C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	GUID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	GUID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	GUID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	GUID [31:24]							

Bits	Name	Description
31 : 0	GUID	User ID (UserID) Application-programmable ID field. Reset value is configurable. Default Value: 0x12345678

24.1.15 USBHS_DWC_otg_intreg_GSNPSID

Description: This read-only register contains the release number of the core being used.

Address: 0x44900040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	SynopsysID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	SynopsysID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	SynopsysID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	SynopsysID [31:24]							

Bits	Name	Description
31 : 0	SynopsysID	Release number of the controller being used currently. Bits [31:16]: - 0x4f54: ASCII Value for OT Bits [15:0]: Current Release Number. For example, 0x400a corresponds to v4.00a Release number. Default Value: 0x4F54420A

24.1.16 USBHS_DWC_otg_intreg_GHWCFG1

Description: This register contains the logical endpoint direction(s) selected using coreConsultant.

Address: 0x44900044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	EpDir [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	EpDir [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	EpDir [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	EpDir [31:24]							

Bits	Name	Description
31 : 0	EpDir	This 32-bit field uses two bits per endpoint to determine the endpoint direction. Endpoint - Bits [31:30]: Endpoint 15 direction - Bits [29:28]: Endpoint 14 direction ... - Bits [3:2]: Endpoint 1 direction - Bits[1:0]: Endpoint 0 direction (always BIDIR) Direction - 2'b00: BIDIR (IN and OUT) endpoint - 2'b01: IN endpoint - 2'b10: OUT endpoint - 2'b11: Reserved Note: This field is configured using the OTG_EP_DIR_1(n) parameter. Default Value: 0x0

24.1.17 USBHS_DWC_otg_intreg_GHWCFG2

Description: This register contains configuration options selected using coreConsultant.

Address: 0x44900048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R	R		R		
HW Access								
Name	HSPhyType [7:6]		SingPnt	OtgArch [4:3]		OtgMode [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	R		R				R	
HW Access								
Name	NumHstChnl [15:14]		NumDevEps [13:10]				FSPhyType [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R		Reserved	R	R	R	R	
HW Access			Reserved					
Name	NPTxQDepth [23:22]		Reserved	MultiProcIn-trpt	DynFifoSiz-ing	PerioSup-port	NumHstChnl [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R					R	
HW Access	Reserved							
Name	Reserved	TknQDepth [30:26]					PTxQDepth [25:24]	

Bits	Name	Description
30 : 26	TknQDepth	Device Mode IN Token Sequence Learning Queue Depth (TknQDepth) Range: 0-30 Note: This field is configured using the OTG_TOKEN_QUEUE_DEPTH parameter. Default Value: 0x8
25 : 24	PTxQDepth	Host Mode Periodic Request Queue Depth (PTxQDepth) - 2'b00: 2 - 2'b01: 4 - 2'b10: 8 - 2'b11:16 Note: This field is configured using the OTG_PERIO_TX_QUEUE_DEPTH parameter. Default Value: 0x2 **0x3: QUE16 :** Queue Depth 16 **0x0: QUE2 :** Queue Depth 2 **0x1: QUE4 :** Queue Depth 4

24.1.17 USBHS_DWC_otg_intreg_GHWCFG2 (continued)

		0x2: QUE8 : Queue Depth 8
23 : 22	NPTxQDepth	Non-periodic Request Queue Depth (NPTxQDepth) - 2'b00: 2 - 2'b01: 4 - 2'b10: 8 - Others: Reserved Note: This field is configured using the OTG_NPERIO_TX_QUEUE_DEPTH parameter. Default Value: 0x2 **0x2: EIGHT :** Queue size 8 **0x1: FOUR :** Queue size 4 **0x0: TWO :** Queue size 2
20	MultiProcIntrpt	Multi Processor Interrupt Enabled (MultiProcIntrpt) - 1'b0: No - 1'b1: Yes Note: This field is configured using the OTG_MULTI_PROC_INTRPT parameter. Default Value: 0x0 **0x0: DISABLED :** No Multi Processor Interrupt Enabled **0x1: ENABLED :** Multi Processor Interrupt Enabled
19	DynFifoSizing	Dynamic FIFO Sizing Enabled (DynFifoSizing) - 1'b0: No - 1'b1: Yes Note: This field is configured using the OTG_DFIFO_DYNAMIC parameter. Default Value: 0x1 **0x0: DISABLED :** Dynamic FIFO Sizing Disabled **0x1: ENABLED :** Dynamic FIFO Sizing Enabled
18	PerioSupport	Periodic OUT Channels Supported in Host Mode (PerioSupport) - 1'b0: No - 1'b1: Yes Note: This field is configured using the OTG_EN_PERIO_HOST parameter. Default Value: 0x1 **0x0: DISABLED :** Periodic OUT Channels is not supported in Host Mode

24.1.17 USBHS_DWC_otg_intreg_GHWCFG2 (continued)

		0x1: ENABLED : Periodic OUT Channels Supported in Host Mode Supported
17 : 14	NumHstChnl	Number of Host Channels (NumHstChnl) Indicates the number of host channels supported by the core in Host mode. The range of this field is 0-15: 0 specifies 1 channel, 15 specifies 16 channels. Note: This field is configured using the OTG_NUM_HOST_CHAN parameter. Default Value: 0xF **0x0: HOSTCH0 :** Host Channel 1 **0x1: HOSTCH1 :** Host Channel 2 **0xa: HOSTCH10 :** Host Channel 11 **0xb: HOSTCH11 :** Host Channel 12 **0xc: HOSTCH12 :** Host Channel 13 **0xd: HOSTCH13 :** Host Channel 14 **0xe: HOSTCH14 :** Host Channel 15 **0xf: HOSTCH15 :** Host Channel 16 **0x2: HOSTCH2 :** Host Channel 3 **0x3: HOSTCH3 :** Host Channel 4 **0x4: HOSTCH4 :** Host Channel 5 **0x5: HOSTCH5 :** Host Channel 6

24.1.17 USBHS_DWC_otg_intreg_GHWCFG2 (continued)

0x6: HOSTCH6 :

Host Channel 7

0x7: HOSTCH7 :

Host Channel 8

0x8: HOSTCH8 :

Host Channel 9

0x9: HOSTCH9 :

Host Channel 10

13 : 10	NumDevEps	Number of Device Endpoints (NumDevEps) Indicates the number of device endpoints supported by the core in Device mode. The range of this field is 0-15. Note: This field is configured using the OTG_NUM_EPS parameter. Default Value: 0x8

0x0: ENDPT0 :

End point 0

0x1: ENDPT1 :

End point 1

0xa: ENDPT10 :

End point 10

0xb: ENDPT11 :

End point 11

0xc: ENDPT12 :

End point 12

0xd: ENDPT13 :

End point 13

0xe: ENDPT14 :

End point 14

0xf: ENDPT15 :

End point 15

0x2: ENDPT2 :

End point 2

24.1.17 USBHS_DWC_otg_intreg_GHWCFG2 (continued)

		0x3: ENDPT3 : End point 3 **0x4: ENDPT4 :** End point 4 **0x5: ENDPT5 :** End point 5 **0x6: ENDPT6 :** End point 6 **0x7: ENDPT7 :** End point 7 **0x8: ENDPT8 :** End point 8 **0x9: ENDPT9 :** End point 9
9 : 8	FSPhyType	Full-Speed PHY Interface Type (FSPhyType) - 2'b00: Full-speed interface not supported - 2'b01: Dedicated full-speed interface - 2'b10: FS pins shared with UTMI+ pins - 2'b11: FS pins shared with ULPI pins Note: This field is configured using the OTG_FSPHY_INTERFACE parameter. Default Value: 0x0 **0x1: FS :** Dedicated full-speed interface is supported **0x3: FSPLUSULPI :** FS pins shared with ULPI pins is supported **0x2: FSPLUSUTMI :** FS pins shared with UTMI+ pins is supported **0x0: NO_FS :** Full-speed interface not supported
7 : 6	HSPhyType	High-Speed PHY Interface Type (HSPhyType) - 2'b00: High-Speed interface not supported - 2'b01: UTMI+ - 2'b10: ULPI - 2'b11: UTMI+ and ULPI Note: This field is configured using the OTG_HSPHY_INTERFACE parameter. Default Value: 0x1

24.1.17 USBHS_DWC_otg_intreg_GHWCFG2 (continued)

		0x0: NOHS : High-Speed interface not supported **0x2: ULPI :** High Speed Interface ULPI is supported **0x1: UTMIPLUS :** High Speed Interface UTMI+ is supported **0x3: UTMIPUSULPI :** High Speed Interfaces UTMI+ and ULPI is supported
5	SingPnt	Point-to-Point (SingPnt) - 1'b0: Multi-point application (hub and split support) - 1'b1: Single-point application (no hub and split support) Note: This field is configured using the OTG_SINGLE_POINT parameter. Default Value: 0x0 **0x0: MULTIPOINT :** Multi-point application (hub and split support) **0x1: SINGLEPOINT :** Single-point application (no hub and split support)
4 : 3	OtgArch	Architecture (OtgArch) - 2'b00: Slave-Only - 2'b01: External DMA - 2'b10: Internal DMA - Others: Reserved Note: This field is configured using the OTG_ARCHITECTURE parameter. Default Value: 0x2 **0x1: EXTERNALDMA :** External DMA Mode **0x2: INTERNALDMA :** Internal DMA Mode **0x0: SLAVEMODE :** Slave Mode
2 : 0	OtgMode	Mode of Operation (OtgMode) - 3'b000: HNP- and SRP-Capable OTG (Host & Device) - 3'b001: SRP-Capable OTG (Host & Device) - 3'b010: Non-HNP and Non-SRP Capable OTG (Host and Device) - 3'b011: SRP-Capable Device - 3'b100: Non-OTG Device - 3'b101: SRP-Capable Host - 3'b110: Non-OTG Host - Others: Reserved Note: This field is configured using the OTG_MODE parameter. Default Value: 0x2

24.1.17 USBHS_DWC_otg_intreg_GHWCFG2 (continued)

0x0: HNPSRP :

HNP- and SRP-Capable OTG (Host and Device)

0x2: NHNPNSRP :

Non-HNP and Non-SRP Capable OTG (Host and Device)

0x4: NONOTGD :

Non-OTG Device

0x6: NONOTGH :

Non-OTG Host

0x3: SRPCAPD :

SRP-Capable Device

0x5: SRPCAPH :

SRP-Capable Host

0x1: SRPOTG :

SRP-Capable OTG (Host and Device)

24.1.18 USBHS_DWC_otg_intreg_GHWCFG3

Description: This register contains configuration options selected using coreConsultant.

Address: 0x4490004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R			R			
HW Access								
Name	OtgEn	PktSizeWidth [6:4]			XferSizeWidth [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access								
Name	LPMMode	BCSupport	HSICMode	ADPSup-port	RstType	OptFeature	VndctlSupt	I2CIntSel

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DfifoDepth [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DfifoDepth [31:24]							

Bits	Name	Description
31 : 16	DfifoDepth	DFIFO Depth (DfifoDepth - EP_LOC_CNT) This value is in terms of 32-bit words. - Minimum value is 32 - Maximum value is 32,768 Note: This field is configured using the OTG_DFIFO_DEPTH parameter. For more information on EP_LOC_CNT, see the "Endpoint Information Controller (EPINFO_CTL)" section. Default Value: 0x1A4F
15	LPMMode	LPM mode specified for Mode of Operation. Default Value: 0x1 **0x0: DISABLED :** LPM disabled **0x1: ENABLED :** LPM enabled
14	BCSupport	This bit indicates the controller support for Battery Charger. - 0 - No Battery Charger Support - 1 - Battery Charger support present Default Value: 0x0

24.1.18 USBHS_DWC_otg_intreg_GHWCFG3 (continued)

		0x0: DISABLED : No Battery Charger Support **0x1: ENABLED :** Battery Charger Support present
13	HSICMode	HSIC mode specified for Mode of Operation Value Range: 0 - 1 - 1: HSIC-capable with shared UTMI PHY interface - 0: Non-HSIC-capable Default Value: 0x0 **0x0: DISABLED :** No HSIC capability **0x1: ENABLED :** HSIC-capable with shared UTMI PHY interface
12	ADPSupport	This bit indicates whether ADP logic is present within or external to the controller - 0: No ADP logic present with the controller - 1: ADP logic is present along with the controller. Default Value: 0x0 **0x0: DISABLED :** ADP logic is not present along with the controller **0x1: ENABLED :** ADP logic is present along with the controller
11	RstType	Reset Style for Clocked always Blocks in RTL (RstType) - 1'b0: Asynchronous reset is used in the controller - 1'b1: Synchronous reset is used in the controller Note: This field is configured using the OTG_SYNC_RESET_TYPE parameter. Default Value: 0x0 **0x0: ASYNCRST :** Asynchronous reset is used in the core **0x1: SYNCRST :** Synchronous reset is used in the core
10	OptFeature	Optional Features Removed (OptFeature) Indicates whether the User ID register, GPIO interface ports, and SOF toggle and counter ports were removed for gate count optimization by enabling Remove Optional Features. - 1'b0: No - 1'b1: Yes Note: This field is configured using the OTG_RM_OPT_FEATURES parameter. Default Value: 0x0 **0x0: DISABLED :** Optional features were not Removed

24.1.18 USBHS_DWC_otg_intreg_GHWCFG3 (continued)

		0x1: ENABLED : Optional Features have been Removed
9	VndctlSupt	Vendor Control Interface Support (VndctlSupt) - 1'b0: Vendor Control Interface is not available on the core. - 1'b1: Vendor Control Interface is available. Note: This field is configured using the OTG_VENDOR_CTL_INTERFACE parameter. Default Value: 0x0 **0x0: DISABLED :** Vendor Control Interface is not available. **0x1: ENABLED :** Vendor Control Interface is available.
8	I2CIntSel	I2C Selection (I2CIntSel) - 1'b0: I2C Interface is not available on the controller. - 1'b1: I2C Interface is available on the controller. Note: This field is configured using the OTG_I2C_INTERFACE parameter. Default Value: 0x0 **0x0: DISABLED :** I2C Interface is not available **0x1: ENABLED :** I2C Interface is available
7	OtgEn	OTG Function Enabled (OtgEn) The application uses this bit to indicate the OTG capabilities of the controller . - 1'b0: Not OTG capable - 1'b1: OTG Capable Note: This field is configured using the OTG_MODE parameter. Default Value: 0x1 **0x0: DISABLED :** Not OTG Capable **0x1: ENABLED :** OTG Capable
6 : 4	PktSizeWidth	Width of Packet Size Counters (PktSizeWidth) - 3'b000: 4 bits - 3'b001: 5 bits - 3'b010: 6 bits - 3'b011: 7 bits - 3'b100: 8 bits - 3'b101: 9 bits - 3'b110: 10 bits - Others: Reserved Note: This field is configured using the OTG_PACKET_COUNT_WIDTH parameter. Default Value: 0x6 **0x6: BITS10 :** Width of Packet Size Counter 10

24.1.18 USBHS_DWC_otg_intreg_GHWCFG3 (continued)

0x0: BITS4 :

Width of Packet Size Counter 4

0x1: BITS5 :

Width of Packet Size Counter 5

0x2: BITS6 :

Width of Packet Size Counter 6

0x3: BITS7 :

Width of Packet Size Counter 7

0x4: BITS8 :

Width of Packet Size Counter 8

0x5: BITS9 :

Width of Packet Size Counter 9

3 : 0	XferSizeWidth	Width of Transfer Size Counters (XferSizeWidth) - 4'b0000: 11 bits - 4'b0001: 12 bits ... - 4'b1000: 19 bits - Others: Reserved Note: This field is configured using the OTG_PACKET_COUNT_WIDTH parameter. Default Value: 0x8

0x0: WIDTH11 :

Width of Transfer Size Counter 11 bits

0x1: WIDTH12 :

Width of Transfer Size Counter 12 bits

0x2: WIDTH13 :

Width of Transfer Size Counter 13 bits

0x3: WIDTH14 :

Width of Transfer Size Counter 14 bits

0x4: WIDTH15 :

Width of Transfer Size Counter 15 bits

0x5: WIDTH16 :

Width of Transfer Size Counter 16 bits

24.1.18 USBHS_DWC_otg_intreg_GHWCFG3 (continued)

0x6: WIDTH17 :

Width of Transfer Size Counter 17 bits

0x7: WIDTH18 :

Width of Transfer Size Counter 18 bits

0x8: WIDTH19 :

Width of Transfer Size Counter 19 bits

24.1.19 USBHS_DWC_otg_intreg_GHWCFG4

Description: This register contains configuration options selected using coreConsultant. Note: Bit [31] is available only when Scatter/Gather DMA mode is enabled. When Scatter/Gather DMA mode is disabled, this field is reserved.

Address: 0x44900050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R			
HW Access								
Name	ExtendedHi-bernation	Hibernation	AhbFreq	PartialP-wrDn	NumDevPerioEps [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R		R	R	R	R	R	Reserved
HW Access								Reserved
Name	PhyDataWidth [15:14]		En-hancedLPM Supt	ACGSupt	ipgisocSupt	ServIntFlow	En-hancedLPM Supt1	Reserved

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R			
HW Access								
Name	BValidFltr	AValidFltr	VBusValid-Fltr	IddgFltr	NumCtlEps [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R				R	R
HW Access								
Name	DescDMA	DescD-MAEnabled	INEps [29:26]				DedFifo-Mode	SessEndFltr

Bits	Name	Description
31	DescDMA	Scatter/Gather DMA configuration - 1'b0: Non Dynamic configuration - 1'b1: Dynamic configuration Note: This field is configured using the OTG_EN_DESC_DMA parameter. Default Value: 0x1 **0x0: CONFIG1 :** Non Dynamic configuration **0x1: CONFIG2 :** Dynamic configuration
30	DescDMAEnabled	Scatter/Gather DMA configuration - 1'b0: Non-Scatter/Gather DMA configuration - 1'b1: Scatter/Gather DMA configuration Default Value: 0x1

24.1.19 USBHS_DWC_otg_intreg_GHWCFG4 (continued)

0x0: DISABLE :

Non-Scatter/Gather DMA configuration

0x1: ENABLE :

Scatter/Gather DMA configuration

29 : 26 INEps

Number of Device Mode IN Endpoints Including Control Endpoints (INEps)
- 0: 1 IN Endpoint
- 1: 2 IN Endpoints
....
- 15: 16 IN Endpoints

Default Value: 0x8

0x0: ENDPT1 :

1 IN Endpoint

0x9: ENDPT10 :

10 IN Endpoints

0xa: ENDPT11 :

11 IN Endpoints

0xb: ENDPT12 :

12 IN Endpoints

0xc: ENDPT13 :

13 IN Endpoints

0xd: ENDPT14 :

14 IN Endpoints

0xe: ENDPT15 :

15 IN Endpoints

0xf: ENDPT16 :

16 IN Endpoints

0x1: ENDPT2 :

2 IN Endpoints

0x2: ENDPT3 :

3 IN Endpoints

0x3: ENDPT4 :

4 IN Endpoints

24.1.19 USBHS_DWC_otg_intreg_GHWCFG4 (continued)

		0x4: ENDPT5 : 5 IN Endpoints **0x5: ENDPT6 :** 6 IN Endpoints **0x6: ENDPT7 :** 7 IN Endpoints **0x7: ENDPT8 :** 8 IN Endpoints **0x8: ENDPT9 :** 9 IN Endpoints
25	DedFifoMode	Enable Dedicated Transmit FIFO for device IN Endpoints (DedFifoMode) - 1'b0 : Dedicated Transmit FIFO Operation not enabled. - 1'b1 : Dedicated Transmit FIFO Operation enabled. Default Value: 0x1 **0x0: DISABLED :** Dedicated Transmit FIFO Operation not enabled **0x1: ENABLED :** Dedicated Transmit FIFO Operation enabled
24	SessEndFltr	session_end Filter Enabled (SessEndFltr) - 1'b0: No filter - 1'b1: Filter Default Value: 0x0 **0x0: DISABLED :** No filter **0x1: ENABLED :** Filter
23	BValidFltr	b_valid Filter Enabled (BValidFltr) - 1'b0: No filter - 1'b1: Filter Default Value: 0x0 **0x0: DISABLED :** No Filter **0x1: ENABLED :** Filter

24.1.19 USBHS_DWC_otg_intreg_GHWCFG4 (continued)

22	AValidFltr	a_valid Filter Enabled (AValidFltr) - 1'b0: No filter - 1'b1: Filter Default Value: 0x0 **0x0: DISABLED :** No filter **0x1: ENABLED :** Filter
21	VBusValidFltr	VBUS Valid Filter Enabled (VBusValidFltr) - 1'b0: No filter - 1'b1: Filter Default Value: 0x0 **0x0: DISABLED :** Vbus Valid Filter Disabled **0x1: ENABLED :** Vbus Valid Filter Enabled
20	IddgFltr	IDDIG Filter Enable (IddgFltr) - 1'b0: No filter - 1'b1: Filter Default Value: 0x1 **0x0: DISABLED :** Iddig Filter Disabled **0x1: ENABLED :** Iddig Filter Enabled
19 : 16	NumCtlEps	Number of Device Mode Control Endpoints in Addition to Endpoint 0 (NumCtlEps) Range: 0-15 Default Value: 0x0 **0x0: ENDPT0 :** End point 0 **0x1: ENDPT1 :** End point 1 **0xa: ENDPT10 :** End point 10 **0xb: ENDPT11 :** End point 11

24.1.19 USBHS_DWC_otg_intreg_GHWCFG4 (continued)

0xc: ENDPT12 :

End point 12

0xd: ENDPT13 :

End point 13

0xe: ENDPT14 :

End point 14

0xf: ENDPT15 :

End point 15

0x2: ENDPT2 :

End point 2

0x3: ENDPT3 :

End point 3

0x4: ENDPT4 :

End point 4

0x5: ENDPT5 :

End point 5

0x6: ENDPT6 :

End point 6

0x7: ENDPT7 :

End point 7

0x8: ENDPT8 :

End point 8

0x9: ENDPT9 :

End point 9

15 : 14	PhyDataWidth	UTMI+ PHY/ULPI-to-Internal UTMI+ Wrapper Data Width (PhyDataWidth)When a ULPI PHY is used, an internal wrapper converts ULPI to UTMI+. - 2'b00: 8 bits - 2'b01: 16 bits - 2'b10: 8/16 bits, software selectable - Others: Reserved Default Value: 0x0

24.1.19 USBHS_DWC_otg_intreg_GHWCFG4 (continued)

		0x0: WIDTH1 : 8 bits **0x1: WIDTH2 :** 16 bits **0x2: WIDTH3 :** 8/16 bits, software selectable
13	EnhancedLPMSupt	Enhanced LPM Support (EnhancedLPMSupt) This bit indicates that the controller supports the following behavior: L1 Entry Behavior based on FIFO Status - TX FIFO - Accept L1 Request even if ISOC IN TX FIFO is not empty. - Reject L1 Request if Non-Periodic TX FIFO is not empty. - Ensure application can flush the TX FIFO while the Controller is in L1. - RX FIFO - Accept L1 Request even if RX FIFO (common to Periodic and Non-Periodic) is not empty. - Accept L1 Request but delay SLEEPM assertion until RX SINK Buffer is empty. Prevent L1 Entry if a Control Transfer is in progress on any Control Endpoint. Ability to Flush TxFIFO even if PHY Clock is gated. Default Value: 0x1 **0x1: ENABLED :** Enhanced LPM Support is enabled
12	ACGSupt	Active Clock Gating Support This bit indicates that the controller supports the Dynamic (Switching) Power Reduction during periods when there is no USB and AHB Traffic. - 1'b0: Active Clock Gating is not enabled. - 1'b1: Active Clock Gating Enabled. Default Value: 0x1 **0x0: DISABLED :** **0x1: ENABLED :** Active Clock Gating Support
11	ipgisocSupt	Interpacket Gap ISOC OUT Worst-case Support (ipgisocSupt) This bit indicates that the controller supports the worst-case scenario of Rx followed by Rx Inter Packet Gap (IPG) (32-bit times) as per the UTMI Specification for any token following an ISOC OUT token. Without this support, when any token follows an ISOC OUT token with the worst-case IPG, the controller will not detect the followed token. The worst-case IPG of the controller without this support depends on the AHB and PHY clock frequency.By default IPG Support is enabled. Default Value: 0x1 **0x0: DISABLED :** Interpacket Gap ISOC OUT Worst-case Support is Disabled **0x1: ENABLED :** Interpacket Gap ISOC OUT Worst-case Support is Enabled (Default)

24.1.19 USBHS_DWC_otg_intreg_GHWCFG4 (continued)

10	ServIntFlow	Service Interval Flow This bit indicates that the controller supports Service-Interval based scheduling flow for ISOC IN EPs. Default Value: 0x0 **0x0: DISABLED :** Service Interval Flow not supported **0x1: ENABLED :** Service Interval Flow supported
9	EnhancedLPMSupt1	Enhanced LPM Support1 (EnhancedLPMSupt1) - This bit indicates that the controller supports L1 entry based on FIFO status. - Accept L1 Request even if Bulk/Interrupt TxFIFO is not empty. Default Value: 0x1 **0x0: DISABLED :** Reject L1 Request even if Non-Periodic (Bulk/Interrupt) TxFIFO is not empty. **0x1: ENABLED :** Accept L1 Request even if Non-Periodic (Bulk/Interrupt) TxFIFO is not empty
7	ExtendedHibernation	Enable Hibernation - 1'b0: Extended Hibernation feature not enabled - 1'b1: Extended Hibernation feature enabled Default Value: 0x0 **0x0: DISABLED :** Extended Hibernation feature not enabled **0x1: ENABLED :** Extended Hibernation feature enabled
6	Hibernation	Enable Hibernation (Hibernation) - 1'b0: Hibernation feature not enabled - 1'b1: Hibernation feature enabled Default Value: 0x0 **0x0: DISABLED :** Hibernation feature disabled **0x1: ENABLED :** Hibernation feature enabled
5	AhbFreq	Minimum AHB Frequency Less Than 60 MHz (AhbFreq) - 1'b0: No - 1'b1: Yes Default Value: 0x1 **0x0: DISABLED :** Minimum AHB Frequency More Than 60 MHz

24.1.19 USBHS_DWC_otg_intreg_GHWCFG4 (continued)

		0x1: ENABLED : Minimum AHB Frequency Less Than 60 MHz
4	PartialPwrDn	Enable Partial Power Down (PartialPwrDn) - 1'b0: Partial Power Down Not Enabled - 1'b1: Partial Power Down Enabled Default Value: 0x0 **0x0: DISABLED :** Partial Power Down disabled **0x1: ENABLED :** Partial Power Down enabled
3 : 0	NumDevPerioEps	Number of Device Mode Periodic IN Endpoints (NumDevPerioEps) Range: 0-15 Default Value: 0x0 **0x0: Value0 :** Number of Periodic IN EPs is 0 **0x1: Value1 :** Number of Periodic IN EPs is 1 **0xa: Value10 :** Number of Periodic IN EPs is 10 **0xb: Value11 :** Number of Periodic IN EPs is 11 **0xc: Value12 :** Number of Periodic IN EPs is 12 **0xd: Value13 :** Number of Periodic IN EPs is 13 **0xe: Value14 :** Number of Periodic IN EPs is 14 **0xf: Value15 :** Number of Periodic IN EPs is 15 **0x2: Value2 :** Number of Periodic IN EPs is 2

24.1.19 USBHS_DWC_otg_intreg_GHWCFG4 (continued)

0x3: Value3 :

Number of Periodic IN EPs is 3

0x4: Value4 :

Number of Periodic IN EPs is 4

0x5: Value5 :

Number of Periodic IN EPs is 5

0x6: Value6 :

Number of Periodic IN EPs is 6

0x7: Value7 :

Number of Periodic IN EPs is 7

0x8: Value8 :

Number of Periodic IN EPs is 8

0x9: Value9 :

Number of Periodic IN EPs is 9

24.1.20 USBHS_DWC_otg_intreg_GLPMCFG

Description: Register to control the LPM functionality of the controller.

Address: 0x44900054

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW				RW	RW
HW Access								
Name	EnblSlpM	bRe-moteWake	HIRD [5:2]				AppL1Res	LPMCap

Bits	15	14	13	12	11	10	9	8
SW Access	R	R		RW				
HW Access								
Name	SlpSts	CoreL1Res [14:13]		HIRD_Thres [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW				R
HW Access								
Name	LPM_Retry_Cnt [23:21]			LPM_Chnl_Indx [20:17]				L1Re-sumeOK

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	R			RW
HW Access	Reserved							
Name	Reserved [31:30]		LPM_Re-storeSlpSts	LPM_En-BESL	LPM_RetryCnt_Sts [27:25]			SndLPM

Bits	Name	Description
29	LPM_RestoreSlpSts	LPM Restore Sleep Status (LPM_RestoreSlpSts) When the application power gates the core (Partial Power Down / Hibernation) the application needs to program this bit to restore the LPM status in the core. The application needs to program this bit, during restore process, based on whether it had decided to go into Shallow Sleep (Clock Gating Only) or Deep Sleep (Power Gating) based on the BESL value received from the Host - 1'b0: The application puts the core in Shallow Sleep based on BESL value from the Host - 1'b1: The application puts the core in Deep Sleep based on BESL value from the Host Default Value: 0x0 **0x0: DISABLED :** Puts the core in Shallow Sleep mode based on the BESL value from the Host **0x1: ENABLED :** Puts the core in Deep Sleep mode based on the BESL value from the Host
28	LPM_EnBESL	LPM Enable BESL (LPM_EnBESL) This bit enables the BESL feature as defined in LPM Errata - 1'b0: The core works as per USB 2.0 Link Power Management Addendum Engineering Change Notice to the USB 2.0 specification as of July 16, 2007 - 1'b1: The core works as per the LPM Errata Default Value: 0x0

24.1.20 USBHS_DWC_otg_intreg_GLPMCFG (continued)

0x0: DISABLED :

BESL is disabled

0x1: ENABLED :

BESL is enabled as defined in LPM Errata

27 : 25 LPM_RetryCnt_Sts

LPM Retry Count Status (LPM_RetryCnt_Sts)
Host Mode: Number of LPM Host Retries still remaining to be transmitted for the current LPM sequence.
Default Value: 0x0

0x0: RETRY_REM0 :

Zero LPM retries remaining

0x1: RETRY_REM1 :

One LPM retry remaining

0x2: RETRY_REM2 :

Two LPM retries remaining

0x3: RETRY_REM3 :

Three LPM retries remaining

0x4: RETRY_REM4 :

Four LPM retries remaining

0x5: RETRY_REM5 :

Five LPM retries remaining

0x6: RETRY_REM6 :

Six LPM retries remaining

0x7: RETRY_REM7 :

Seven LPM retries remaining

24 SndLPM

Send LPM Transaction (SndLPM)
Host Mode:
When set by application software, an LPM transaction containing two tokens, EXT & LPM is sent. Cleared by the hardware once a valid response (STALL./NYET/ACK) is received from the Device or the core had finished transmitting the programmed number of LPM retries. Note that this bit should be set only when the host is connected to local port.
Default Value: 0x0

0x0: DISABLED :

In host-only mode: Received the response from the device for the LPM transaction

24.1.20 USBHS_DWC_otg_intreg_GLPMCFG (continued)

0x1: ENABLED :

In host-only mode: Sending LPM transaction containing EXT and LPM tokens

23 : 21	LPM_Retry_Cnt	LPM Retry Count (LPM_Retry_Cnt) Host Mode: Number of additional LPM retries that the HOST would perform if the Device Response was an ERROR until a valid device response is received (STALL/NYET/ACK). Device Mode: LPM Accept Control (LPM_Accept_Ctrl) LPM_Accept_Ctrl[1]: The application can use this bit to reject an LPM token (NYET) between multiple stages of a single control transfer - 1'b0: Accept(ACK) LPM token during Setup, Data and Status stage of control transfer. - 1'b1: Reject(NYET) LPM token during Setup, Data and Status stage of control transfer. LPM_Accept_Ctrl[2]: The application can use this bit to accept an LPM token even if data is present in the ISOC endpoint TxFIFO. This bit is applicable only for Dedicated TxFIFO configurations (OTG_EN_DED_TX_FIFO=1). - 1'b0: Reject (NYET) LPM token, when data is present in TxFIFO for ISOC endpoints. - 1'b1: Accept(ACK) LPM token, when data is present in TxFIFO for ISOC endpoints. LPM_Accept_Ctrl[3]: The application can use this bit to accept an LPM token even if data is present in the BULK endpoint TxFIFO. This bit is applicable only for Dedicated TxFIFO configurations (OTG_EN_DED_TX_FIFO=1). - 1'b0: Reject (NYET) LPM token, when data is present in TxFIFO for BULK endpoints. - 1'b1: Accept(ACK) LPM token, when data is present in TxFIFO for BULK endpoints. Default Value: 0x0 **0x0: RETRY0 :** Zero LPM retries **0x1: RETRY1 :** One LPM retry **0x2: RETRY2 :** Two LPM retries **0x3: RETRY3 :** Three LPM retries **0x4: RETRY4 :** Four LPM retries **0x5: RETRY5 :** Five LPM retries **0x6: RETRY6 :** Six LPM retries **0x7: RETRY7 :** Seven LPM retries

24.1.20 USBHS_DWC_otg_intreg_GLPMCFG (continued)

20 : 17	LPM_Chnl_Indx	LPM Channel Index Host Mode: The channel number on which the LPM transaction has to be applied while sending an LPM transaction to the local device. Based on the LPM channel index, the core automatically inserts the device address and end point number programmed in the corresponding channel into the LPM transaction. Device Mode: LPM Accept Control (LPM_Accept_Ctrl) LPM_Accept_Ctrl[0] (LPM_Chnl_Indx[3]): The application can use this bit to accept an LPM token even if data is present in the INTR endpoint TxFIFO. This bit is applicable only for Dedicated TX FIFO configurations (OTG_EN_DED_TX_FIFO=1). - 1'b0:Reject (NYET) LPM token, when data is present in txfifo for INTR endpoints. - 1'b1:Accept(ACK) LPM token, when data is present in txfifo for INTR endpoints. Default Value: 0x0 **0x0: CH0 :** Channel 0 **0x1: CH1 :** Channel 1 **0xa: CH10 :** Channel 10 **0xb: CH11 :** Channel 11 **0xc: CH12 :** Channel 12 **0xd: CH13 :** Channel 13 **0xe: CH14 :** Channel 14 **0xf: CH15 :** Channel15 **0x2: CH2 :** Channel 2 **0x3: CH3 :** Channel 3 **0x4: CH4 :** Channel 4

24.1.20 USBHS_DWC_otg_intreg_GLPMCFG (continued)

0x5: CH5 :

Channel 5

0x6: CH6 :

Channel 6

0x7: CH7 :

Channel 7

0x8: CH8 :

Channel 8

0x9: CH9 :

Channel 9

16 L1ResumeOK

Sleep State Resume OK (L1ResumeOK)
Device and Host Mode:
Indicates that the application or host can start resume from Sleep state. This bit is valid in LPM sleep (L1) state. It is set in sleep mode after a delay of 50 micro sec (TL1Residency). The bit is reset when SlpSts is 0.
- 1'b0: The application/core cannot start resume from Sleep state.
- 1'b1: The application/core can start resume from Sleep state.
Default Value: 0x0

0x0: NOTOK :

The application/core cannot start Resume from Sleep state

0x1: OK :

The application/core can start Resume from Sleep state

15 SlpSts

Port Sleep Status (SlpSts)
Device Mode: This bit is set as long as a Sleep condition is present on the USB bus.
The core enters the Sleep state when an ACK response is sent to an LPM transaction and the TL1TokenRetry timer has expired. To stop the PHY clock, the application must set the Port Clock Stop bit, which asserts the PHY Suspend input signal. The application must rely on SlpSts and not ACK in CoreL1Res to confirm transition into sleep.
The core comes out of sleep:
- When there is any activity on the USB line_state
- When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig) or when the application resets or soft-disconnects the device.
Host Mode: The host transitions to Sleep (L1) state as a side-effect of a successful LPM transaction by the core to the local port with ACK response from the device. The read value of this bit reflects the current Sleep status of the port.
The core clears this bit after:
- The core detects a remote L1 Wakeup signal;
- The application sets the Port Reset bit or the Port L1Resume bit in the HPRT register; or
- The application sets the L1Resume/ Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register (GINTSTS.L1WkUpInt or GINTSTS.DisconnInt, respectively).
Default Value: 0x0

24.1.20 USBHS_DWC_otg_intreg_GLPMCFG (continued)

		0x1: CORE_IN_L1 : :DWC_DESIGN_ID==0>In Host mode, this bit indicates the core transitions to Sleep state as a successful LPM transaction. In Device mode, the core enters the Sleep state when an ACK response is sent to an LPM transaction **0x0: CORE_NOT_IN_L1 :** In :DWC_DESIGN_ID==0>Host or Device mode, this bit indicates core is not in L1
14 : 13	CoreL1Res	LPM Response (CoreL1Res) Device Mode: The response of the core to LPM transaction received is reflected in these two bits. Host Mode: Handshake response received from local device for LPM transaction - 11 - ACK - 10 - NYET - 01 - STALL - 00 - ERROR (No handshake response) Default Value: 0x0 **0x0: LPMRESP1 :** ERROR : No handshake response **0x1: LPMRESP2 :** STALL response **0x2: LPMRESP3 :** NYET response **0x3: LPMRESP4 :** ACK response

24.1.20 USBHS_DWC_otg_intreg_GLPMCFG (continued)

12 : 8	HIRD_Thres	BESL/HIRD Threshold (HIRD_Thres) Device Mode: Note: When a ULPI/UTMI PHY associated with the controller (Host or device) does not support the LPM sleep feature clock gating, it is recommended to keep the HIRD_Thres[12] bit in disabled state (= 1'b0). This ensures the ULPI wrapper is in enabled mode and detects any wakeup events. - EnBESL = 1'b0: The core puts the PHY into deep low power mode in L1 (by core asserting L1SuspendM) when HIRD value is greater than or equal to the value defined in this field HIRD_Thres[3:0] and HIRD_Thres[4] is set to 1b1. - EnBESL = 1'b1: The core puts the PHY into deep low power mode in L1 (by core asserting L1SuspendM) when BESL value is greater than or equal to the value defined in this field BESL_Thres[3:0] and BESL_Thres [4] is set to 1'b1. - DCTL.DeepSleepBESLReject = 1'b1: In device initiated resume, the core expects the Host to resume service to the device within the BESL value corresponding to L1 exit time specified in HIRD_Thres[3:0]. The Device sends a NYET response when the received HIRD in LPM token is greater than HIRD threshold. Host Mode: The core puts the PHY into deep low power mode in L1 (by core asserting L1SuspendM) when HIRD_Thres[4] is set to 1'b1. HIRD_Thres[3:0] specifies the time for which resume signaling is to be reflected by host (TL1HubDrvResume2) on the USB bus when it detects device initiated resume. To differentiate between Deep Sleep and Shallow Sleep, HIRD greater than or equal to HIRD threshold comparison is done. For differentiating between NYET or ACK response for LPM token HIRD greater than HIRD Threshold comparison is used. - When EnBESL = 1'b0, HIRD_Thres should not be programmed with a value greater than 4'b1100 in host mode since this will exceed maximum TL1HubDrvResume2. - When EnBESL = 1'b1, HIRD_Thres should not be programmed with a value greater than 4'b0110 in host mode since this will exceed maximum TL1HubDrvResume2. For additional details, see the "Additional Details on GLPMCFG.HIRD_Thres Register Field" section in the databook. Default Value: 0x0
7	EnblSlpM	Enable utmi_sleep_n (EnblSlpM) Mode: Host and Device For ULPI interface: The application uses this bit to control the utmi_sleep_n assertion to the PHY when in L1 state. For the host, this bit is valid only in Local Device mode. - 1'b0: utmi_sleep_n assertion from the core is not transferred to the external PHY. - 1'b1: utmi_sleep_n assertion from the core is transferred to the external PHY. Note: - When a ULPI interface is configured, enabling this bit results in a write to Bit 7 of the ULPI Function Control register. The Synopsys ULPI PHY supports writing to this bit, and in the L1 state asserts SleepM when utmi_l1_suspend_n cannot be asserted. - When a ULPI/UTMI PHY associated with the controller (Host or device) does not support the LPM sleep feature clock gating, it is recommended to keep the EnblSlpM bit in disabled state (= 1'b0). This ensures the ULPI wrapper is in enabled mode and detects any wakeup events. For all other interfaces: The application uses this bit to control utmi_sleep_n assertion to the PHY in the L1 state. For the host, this bit is valid only in Local Device mode. - 1'b0: utmi_sleep_n assertion from the core is not transferred to the external PHY. - 1'b1: utmi_sleep_n assertion from the core is transferred to the external PHY when utmi_l1_suspend_n cannot be asserted. Default Value: 0x0 **0x0: DISABLED :** utmi_sleep_n assertion from the core is not transferred to the external PHY **0x1: ENABLED :** utmi_sleep_n assertion from the core is transferred to the external PHY when utmi_l1_suspend_n cannot be asserted

24.1.20 USBHS_DWC_otg_intreg_GLPMCFG (continued)

6	bRemoteWake	RemoteWakeEnable (bRemoteWake) Mode: Host and Device Host Mode: The value of remote wake up to be sent in wIndex field of LPM transaction. Device Mode: This field is read only. It is updated with the Received LPM Token bRemoteWake bmAttribute when an ACK/NYET/STALL response is sent to an LPM transaction. Default Value: 0x0 **0x0: DISABLED :** Remote Wakeup is disabled **0x1: ENABLED :** In :DWC_DESIGN_ID==0>Host or device mode, this field takes the value of remote wake up
5 : 2	HIRD	Host-Initiated Resume Duration (HIRD) EnBESL = 1'b0 Host Initiated Resume Duration. - Host Mode: The value of HIRD to be sent in an LPM transaction. This value is also used to initiate resume for a duration TL1HubDrvResume1 for host-initiated resume. - Device Mode: This field is read only and is updated with the Received LPM Token HIRD bmAttribute when an ACK/NYET/STALL response is sent to an LPM transaction. If HIRD[3:0], - 4'b0000, THIRD(us) = 50 - 4'b0001, THIRD(us) = 125 - 4'b0010, THIRD(us) = 200 - 4'b0011, THIRD(us) = 275 - 4'b0100, THIRD(us) = 350 - 4'b0101, THIRD(us) = 425 - 4'b0110, THIRD(us) = 500 - 4'b0111, THIRD(us) = 575 - 4'b1000, THIRD(us) = 650 - 4'b1001, THIRD(us) = 725 - 4'b1010, THIRD(us) = 800 - 4'b1011, THIRD(us) = 875 - 4'b1100, THIRD(us) = 950 - 4'b1101, THIRD(us) = 1025 - 4'b1110, THIRD(us) = 1100 - 4'b1111, THIRD(us) = 1175 EnBESL = 1'b1 Best Effort Service Latency (BESL). - Host Mode: The value of BESL to be sent in an LPM transaction. This value is also used to initiate resume for a duration TL1HubDrvResume1 for host-initiated resume. - Device Mode: This field is updated with the Received LPM Token BESL bmAttribute when an ACK/NYET/STALL response is sent to an LPM transaction. If BESL[3:0], - 4'b0000, TBESL(us) = 125 - 4'b0001, TBESL(us) = 150 - 4'b0010, TBESL(us) = 200 - 4'b0011, TBESL(us) = 300 - 4'b0100, TBESL(us) = 400 - 4'b0101, TBESL(us) = 500 - 4'b0110, TBESL(us) = 1000 - 4'b0111, TBESL(us) = 2000 - 4'b1000, TBESL(us) = 3000 - 4'b1001, TBESL(us) = 4000 - 4'b1010, TBESL(us) = 5000 - 4'b1011, TBESL(us) = 6000 - 4'b1100, TBESL(us) = 7000 - 4'b1101, TBESL(us) = 8000 - 4'b1110, TBESL(us) = 9000 - 4'b1111, TBESL(us) = 10000 Default Value: 0x0

24.1.20 USBHS_DWC_otg_intreg_GLPMCFG (continued)

1	AppL1Res	Mode: Device only LPM response programmed by application (AppL1Res) Handshake response to LPM token pre-programmed by device application software. The response depends on GLPMCFG.LPMCap. If GLPMCFG.LPMCap is 1'b0, the core operates as a non-LPM-capable Device and does not respond to any LPM transactions. If GLPMCFG.LPMCap is 1'b1, the core responds as follows: - 1: ACK Even though an ACK is pre-programmed, the core responds with an ACK only on a successful LPM transaction. The LPM transaction is successful if: -- There are no PID/CRC5 errors in both the EXT token and the LPM token (else ERROR) -- A valid bLinkState = 0001B (L1) is received in the LPM transaction (else STALL) -- No data is pending in the Transmit queue (else NYET) - 0: NYET The pre-programmed software bit is overridden for response to LPM token when: -- The received bLinkState is not L1 (STALL response) -- An error is detected in either of the LPM token packets due to corruption (ERROR response). Default Value: 0x0 **0x1: ACK_RESP :** The core responds with an ACK only on a successful LPM transaction **0x0: NYET_RESP :** The core responds with a NYET when an error is detected in either of the LPM token packets due to corruption
0	LPMCap	LPM-Capable (LPMCap) The application uses this bit to control the controller LPM capabilities. If the core operates as a non-LPM-capable host, it cannot request the connected device/hub to activate LPM mode. If the core operates as a non-LPM-capable device, it cannot respond to any LPM transactions. If GLPMCFG.LPMCap is 1'b0, the software must not set any of the remaining fields in the GLPMCFG register and these fields should hold their Reset values. - 1'b0: LPM capability is not enabled. - 1'b1: LPM capability is enabled. Default Value: 0x0 **0x0: DISABLED :** LPM capability is not enabled **0x1: ENABLED :** LPM capability is enabled

24.1.21 USBHS_DWC_otg_intreg_GDFIFOCFG

Description: Register to configure the DFIFOs for the controller.

Address: 0x4490005C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	GDFIFOCfg [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	GDFIFOCfg [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	EPInfoBaseAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	EPInfoBaseAddr [31:24]							

Bits	Name	Description
31 : 16	EPInfoBaseAddr	EPInfoBaseAddr This field provides the start address of the EP info controller. Default Value: 0x1A4F
15 : 0	GDFIFOCfg	GDFIFOCfg This field is for dynamic programming of the DFIFO Size. This value takes effect only when the application programs a non zero value to this register. The value programmed must conform to the guidelines described in 'FIFO RAM Allocation'. The core does not have any corrective logic if the FIFO sizes are programmed incorrectly. Default Value: 0x1A97

24.1.22 USBHS_DWC_otg_intreg_GINTMSK2

Description: This register works with the Interrupt Register (GINTSTS2) to interrupt the application. When an interrupt bit is masked, the interrupt associated with that bit is not generated. However, the GINTSTS2 register bit corresponding to that interrupt is still set. Note: The fields of this register change depending on host or device mode.

Address: 0x44900068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	GINTMSK2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	GINTMSK2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	GINTMSK2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	GINTMSK2 [31:24]							

Bits	Name	Description
31 : 0	GINTMSK2	Default Value: 0x0

24.1.23 USBHS_DWC_otg_intreg_GINTSTS2

Description: This register interrupts the application for system-level events in the current mode (Device mode or Host mode). Some of the bits in this register are valid only in Host mode, while others are valid in Device mode only. This register also indicates the current mode. To clear the interrupt status bits of type R_SS_WC, the application must write 1'b1 to the bit. The application must clear the GINTSTS2 register at initialization before unmasking the interrupt bit to avoid any interrupts generated prior to initialization.

Address: 0x4490006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	GINTSTS2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	GINTSTS2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	GINTSTS2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	GINTSTS2 [31:24]							

Bits	Name	Description
31 : 0	GINTSTS2	Default Value: 0x0

24.1.24 USBHS_DWC_otg_intreg_HPTXFSIZ

Description: This register holds the size and the memory start address of the Periodic TxFIFO. Note: Read the reset value of this register only after the following conditions: - If IDDIG_FILTER is disabled, read only after PHY clock is stable. - If IDDIG_FILTER is enabled, read only after the filter timer expires.

Address: 0x44900100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	PTxFStAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [15:10]						PTxFStAddr [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	PTxFSize [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved							
Name	Reserved [31:27]					PTxFSize [26:24]		

Bits	Name	Description
26 : 16	PTxFSize	Host Periodic TxFIFO Depth (PTxFSize) This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 The power-on reset value of this register is specified as the Largest Host Mode Periodic Tx Data FIFO Depth. - If Enable Dynamic FIFO Sizing? was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. - If Enable Dynamic FIFO Sizing? was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value set in coreConsultant. Default Value: 0x400
9 : 0	PTxFStAddr	Host Periodic TxFIFO Start Address (PTxFStAddr) The power-on reset value of this register is the sum of the Largest Rx Data FIFO Depth and Largest Non-periodic Tx Data FIFO Depth.These parameters are: In shared FIFO operation: - OTG_RX_DFIFO_DEPTH + OTG_TX_NPERIO_DFIFO_DEPTH In dedicated FIFO mode: - OTG_RX_DFIFO_DEPTH + OTG_TX_HNPERIO_DFIFO_DEPTH If Enable Dynamic FIFO Sizing? was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. If Enable Dynamic FIFO Sizing? was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value set in coreConsultant. Default Value: 0x31F

24.1.25 USBHS_DWC_otg_intreg_DIEPTXF1

Description: This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.

Address: 0x44900104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	INEPnTxFStAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [15:10]						INEPnTxFStAddr [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	INEPnTxFDep [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [31:26]						INEPnTxFDep [25:24]	

Bits	Name	Description
25 : 16	INEPnTxFDep	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n) during coreConsultant configuration (0 < i <= 15). - If "Enable Dynamic FIFO Sizing?" was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. - If "Enable Dynamic FIFO Sizing?" was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value. Default Value: 0x300

24.1.25 USBHS_DWC_otg_intreg_DIEPTXF1 (continued)

9 : 0	INEPnTxFStAddr	IN Endpoint FIFOn Transmit RAM Start Address (INEPnTxFStAddr) This field contains the memory start address for IN endpoint Transmit FIFOn (0< = 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. The power-on reset value of this register is calculated according to the following formula: OTG_RX-_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'i' (where x = 0 to n 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OT-G_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFI-FO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1. - If Enable Dynamic FIFO Sizing is deselected in coreConsultant (OTG_DFIFO_DYNAMIC = 0), this field is read-only and read value is the power-on reset value. - If Enable Dynamic FIFO Sizing is selected in coreConsultant (OTG_DFIFO_DYNAMIC = 1), and you have calculated or programmed a new value for RxFIFO depth or TX FIFO depths, you can program their values according to the above formula. Programmed values must not exceed the power-on value set in coreConsultant. Default Value: 0x25F

24.1.26 USBHS_DWC_otg_intreg_DIEPTXF2

Description: This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.

Address: 0x44900108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	INEPnTxFStAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved							
Name	Reserved [15:11]					INEPnTxFStAddr [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	INEPnTxFDep [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [31:26]						INEPnTxFDep [25:24]	

Bits	Name	Description
25 : 16	INEPnTxFDep	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n) during coreConsultant configuration (0 < i <= 15). - If "Enable Dynamic FIFO Sizing?" was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. - If "Enable Dynamic FIFO Sizing?" was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value. Default Value: 0x300

24.1.26 USBHS_DWC_otg_intreg_DIEPTXF2 (continued)

10 : 0	INEPnTxFStAddr	IN Endpoint FIFOn Transmit RAM Start Address (INEPnTxFStAddr) This field contains the memory start address for IN endpoint Transmit FIFOn (0< = 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. The power-on reset value of this register is calculated according to the following formula: OTG_RX-_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'i' (where x = 0 to n 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OT-G_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFI-FO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1. - If Enable Dynamic FIFO Sizing is deselected in coreConsultant (OTG_DFIFO_DYNAMIC = 0), this field is read-only and read value is the power-on reset value. - If Enable Dynamic FIFO Sizing is selected in coreConsultant (OTG_DFIFO_DYNAMIC = 1), and you have calculated or programmed a new value for RxFIFO depth or TX FIFO depths, you can program their values according to the above formula. Programmed values must not exceed the power-on value set in coreConsultant. Default Value: 0x55F

24.1.27 USBHS_DWC_otg_intreg_DIEPTXF3

Description: This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.

Address: 0x4490010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	INEPnTxFStAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved							
Name	Reserved [15:12]				INEPnTxFStAddr [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	INEPnTxFDep [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [31:26]						INEPnTxFDep [25:24]	

Bits	Name	Description
25 : 16	INEPnTxFDep	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n) during coreConsultant configuration (0 < i <= 15). - If "Enable Dynamic FIFO Sizing?" was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. - If "Enable Dynamic FIFO Sizing?" was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value. Default Value: 0x300

24.1.27 USBHS_DWC_otg_intreg_DIEPTXF3 (continued)

11 : 0	INEPnTxFStAddr	IN Endpoint FIFOn Transmit RAM Start Address (INEPnTxFStAddr) This field contains the memory start address for IN endpoint Transmit FIFOn (0< = 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. The power-on reset value of this register is calculated according to the following formula: OTG_RX-_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'i' (where x = 0 to n 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OT-G_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFI-FO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1. - If Enable Dynamic FIFO Sizing is deselected in coreConsultant (OTG_DFIFO_DYNAMIC = 0), this field is read-only and read value is the power-on reset value. - If Enable Dynamic FIFO Sizing is selected in coreConsultant (OTG_DFIFO_DYNAMIC = 1), and you have calculated or programmed a new value for RxFIFO depth or TX FIFO depths, you can program their values according to the above formula. Programmed values must not exceed the power-on value set in coreConsultant. Default Value: 0x85F

24.1.28 USBHS_DWC_otg_intreg_DIEPTXF4

Description: This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.

Address: 0x44900110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	INEPnTxFStAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved							
Name	Reserved [15:12]				INEPnTxFStAddr [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	INEPnTxFDep [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [31:26]						INEPnTxFDep [25:24]	

Bits	Name	Description
25 : 16	INEPnTxFDep	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n) during coreConsultant configuration (0 < i <= 15). - If "Enable Dynamic FIFO Sizing?" was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. - If "Enable Dynamic FIFO Sizing?" was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value. Default Value: 0x300

24.1.28 USBHS_DWC_otg_intreg_DIEPTXF4 (continued)

11 : 0	INEPnTxFStAddr	IN Endpoint FIFOn Transmit RAM Start Address (INEPnTxFStAddr) This field contains the memory start address for IN endpoint Transmit FIFOn (0< = 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. The power-on reset value of this register is calculated according to the following formula: OTG_RX-_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'i' (where x = 0 to n 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OT-G_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFI-FO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1. - If Enable Dynamic FIFO Sizing is deselected in coreConsultant (OTG_DFIFO_DYNAMIC = 0), this field is read-only and read value is the power-on reset value. - If Enable Dynamic FIFO Sizing is selected in coreConsultant (OTG_DFIFO_DYNAMIC = 1), and you have calculated or programmed a new value for RxFIFO depth or TX FIFO depths, you can program their values according to the above formula. Programmed values must not exceed the power-on value set in coreConsultant. Default Value: 0xB5F

24.1.29 USBHS_DWC_otg_intreg_DIEPTXF5

Description: This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.

Address: 0x44900114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	INEPnTxFStAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved							
Name	Reserved [15:12]				INEPnTxFStAddr [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	INEPnTxFDep [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [31:26]						INEPnTxFDep [25:24]	

Bits	Name	Description
25 : 16	INEPnTxFDep	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n) during coreConsultant configuration (0 < i <= 15). - If "Enable Dynamic FIFO Sizing?" was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. - If "Enable Dynamic FIFO Sizing?" was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value. Default Value: 0x300

24.1.29 USBHS_DWC_otg_intreg_DIEPTXF5 (continued)

11 : 0	INEPnTxFStAddr	IN Endpoint FIFOn Transmit RAM Start Address (INEPnTxFStAddr) This field contains the memory start address for IN endpoint Transmit FIFOn (0< = 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. The power-on reset value of this register is calculated according to the following formula: OTG_RX-_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'i' (where x = 0 to n 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OT-G_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFI-FO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1. - If Enable Dynamic FIFO Sizing is deselected in coreConsultant (OTG_DFIFO_DYNAMIC = 0), this field is read-only and read value is the power-on reset value. - If Enable Dynamic FIFO Sizing is selected in coreConsultant (OTG_DFIFO_DYNAMIC = 1), and you have calculated or programmed a new value for RxFIFO depth or TX FIFO depths, you can program their values according to the above formula. Programmed values must not exceed the power-on value set in coreConsultant. Default Value: 0xE5F

24.1.30 USBHS_DWC_otg_intreg_DIEPTXF6

Description: This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.

Address: 0x44900118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	INEPnTxFStAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved							
Name	Reserved [15:13]			INEPnTxFStAddr [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	INEPnTxFDep [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [31:26]						INEPnTxFDep [25:24]	

Bits	Name	Description
25 : 16	INEPnTxFDep	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n) during coreConsultant configuration (0 < i <= 15). - If "Enable Dynamic FIFO Sizing?" was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. - If "Enable Dynamic FIFO Sizing?" was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value. Default Value: 0x300

24.1.30 USBHS_DWC_otg_intreg_DIEPTXF6 (continued)

12 : 0	INEPnTxFStAddr	IN Endpoint FIFOn Transmit RAM Start Address (INEPnTxFStAddr) This field contains the memory start address for IN endpoint Transmit FIFOn (0< = 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. The power-on reset value of this register is calculated according to the following formula: OTG_RX-_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'i' (where x = 0 to n 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OT-G_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFI-FO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1. - If Enable Dynamic FIFO Sizing is deselected in coreConsultant (OTG_DFIFO_DYNAMIC = 0), this field is read-only and read value is the power-on reset value. - If Enable Dynamic FIFO Sizing is selected in coreConsultant (OTG_DFIFO_DYNAMIC = 1), and you have calculated or programmed a new value for RxFIFO depth or TX FIFO depths, you can program their values according to the above formula. Programmed values must not exceed the power-on value set in coreConsultant. Default Value: 0x115F

24.1.31 USBHS_DWC_otg_intreg_DIEPTXF7

Description: This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.

Address: 0x4490011C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	INEPnTxFStAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved							
Name	Reserved [15:13]			INEPnTxFStAddr [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	INEPnTxFDep [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [31:26]						INEPnTxFDep [25:24]	

Bits	Name	Description
25 : 16	INEPnTxFDep	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n) during coreConsultant configuration (0 < i <= 15). - If "Enable Dynamic FIFO Sizing?" was deselected in coreConsultant (parameter OTG_DFI-FO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. - If "Enable Dynamic FIFO Sizing?" was selected in coreConsultant (parameter OTG_DFIFO_-DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value. Default Value: 0x300

24.1.31 USBHS_DWC_otg_intreg_DIEPTXF7 (continued)

12 : 0	INEPnTxFStAddr	IN Endpoint FIFOn Transmit RAM Start Address (INEPnTxFStAddr) This field contains the memory start address for IN endpoint Transmit FIFOn (0< = 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. The power-on reset value of this register is calculated according to the following formula: OTG_RX-_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'i' (where x = 0 to n 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OT-G_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFI-FO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1. - If Enable Dynamic FIFO Sizing is deselected in coreConsultant (OTG_DFIFO_DYNAMIC = 0), this field is read-only and read value is the power-on reset value. - If Enable Dynamic FIFO Sizing is selected in coreConsultant (OTG_DFIFO_DYNAMIC = 1), and you have calculated or programmed a new value for RxFIFO depth or TX FIFO depths, you can program their values according to the above formula. Programmed values must not exceed the power-on value set in coreConsultant. Default Value: 0x145F

24.1.32 USBHS_DWC_otg_intreg_DIEPTXF8

Description: This register is valid only in dedicated FIFO mode (OTG_EN_DED_TX_FIFO=1). It holds the size and memory start address of IN endpoint TxFIFOs implemented in Device mode. Each FIFO holds the data for one IN endpoint. This register is repeated for instantiated IN endpoint FIFOs 1 to 15. For IN endpoint FIFO 0, use GNPTXFSIZ register for programming the size and memory start address.

Address: 0x44900120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	INEPnTxFStAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved							
Name	Reserved [15:13]			INEPnTxFStAddr [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	INEPnTxFDep [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [31:26]						INEPnTxFDep [25:24]	

Bits	Name	Description
25 : 16	INEPnTxFDep	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. - Minimum value is 16 - Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n) during coreConsultant configuration (0 < i <= 15). - If "Enable Dynamic FIFO Sizing?" was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. - If "Enable Dynamic FIFO Sizing?" was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value. Default Value: 0x300

24.1.32 USBHS_DWC_otg_intreg_DIEPTXF8 (continued)

12 : 0	INEPnTxFStAddr	IN Endpoint FIFOn Transmit RAM Start Address (INEPnTxFStAddr) This field contains the memory start address for IN endpoint Transmit FIFOn (0< = 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. The power-on reset value of this register is calculated according to the following formula: OTG_RX-_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'i' (where x = 0 to n 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OT-G_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFI-FO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1. - If Enable Dynamic FIFO Sizing is deselected in coreConsultant (OTG_DFIFO_DYNAMIC = 0), this field is read-only and read value is the power-on reset value. - If Enable Dynamic FIFO Sizing is selected in coreConsultant (OTG_DFIFO_DYNAMIC = 1), and you have calculated or programmed a new value for RxFIFO depth or TX FIFO depths, you can program their values according to the above formula. Programmed values must not exceed the power-on value set in coreConsultant. Default Value: 0x175F

24.1.33 USBHS_DWC_otg_intreg_HCFG

Description: This register is used to configure the controller in Host mode.

Address: 0x44900400

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved				RW	RW	
HW Access		Reserved						
Name	Ena32KHzS	Reserved [6:3]				FSLSSupp	FSLSPclkSel [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ResValid [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	Reserved						RW
HW Access		Reserved						
Name	DescDMA	Reserved [22:17]						dis_tx_ip-gap_dly_-check

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved				RW	RW	
HW Access		Reserved						
Name	ModeChTi-mEn	Reserved [30:27]				PerSchedE-na	FrListEn [25:24]	

Bits	Name	Description
31	ModeChTimEn	Mode Change Ready Timer Enable (ModeChTimEn) This bit is used to enable/disable the Host core to wait 200 PHY clock cycles at the end of Resume to change the opmode signal to the PHY to 00 after Suspend or LPM. - 1'b0 : The Host core waits for either 200 PHY clock cycles or a linestate of SE0 at the end of resume to the change the opmode from 2'b10 to 2'b00 - 1'b1 : The Host core waits only for a linstate of SE0 at the end of resume to change the opmode from 2'b10 to 2'b00. Default Value: 0x0 **0x1: DISABLED :** The Host core waits only for a linestate of SE0 at the end of resume to change the opmode from 0x2 to 0x0 **0x0: ENABLED :** The Host core waits for either 200 PHY clock cycles or a linestate of SE0 at the end of resume to change the opmode from 0x2 to 0x0

24.1.33 USBHS_DWC_otg_intreg_HCFG (continued)

26	PerSchedEna	Enable Periodic Scheduling (PerSchedEna): Applicable in host DDMA mode only. Enables periodic scheduling within the core. Initially, the bit is reset. The core will not process any periodic channels. As soon as this bit is set, the core will get ready to start scheduling periodic channels and sets HCFG.PerSchedStat. The setting of HCFG.PerSchedStat indicates the core has enabled periodic scheduling. Once HCFG.PerSchedEna is set, the application is not supposed to again reset the bit unless HCFG.PerSchedStat is set. As soon as this bit is reset, the core will get ready to stop scheduling periodic channels and resets HCFG.PerSchedStat. Default Value: 0x0 **0x0: DISABLED :** Disables periodic scheduling within the core **0x1: ENABLED :** Enables periodic scheduling within the core
25 : 24	FrListEn	Frame List Entries(FrListEn) The value in the register specifies the number of entries in the Frame list. This field is valid only in Scatter/Gather DMA mode. - 2'b00: 8 Entries - 2'b01: 16 Entries - 2'b10: 32 Entries - 2'b11: 64 Entries Default Value: 0x0 **0x1: ENTRY16 :** 16 Entries **0x2: ENTRY32 :** 32 Entries **0x3: ENTRY63 :** 64 Entries **0x0: ENTRY8 :** 8 Entries
23	DescDMA	Enable Scatter/gather DMA in Host mode (DescDMA) When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. Note: This bit must be modified only once after a reset. The following combinations are available for programming: - GAHBCFG.DMAEn=0,HCFG.DescDMA=0 => Slave mode - GAHBCFG.DMAEn=0,HCFG.DescDMA=1 => Invalid - GAHBCFG.DMAEn=1,HCFG.DescDMA=0 => Buffered DMA mode - GAHBCFG.DMAEn=1,HCFG.DescDMA=1 => Scatter/Gather DMA mode Default Value: 0x0 **0x0: DISABLED :** Scatter/Gather DMA in Host mode is disabled

24.1.33 USBHS_DWC_otg_intreg_HCFG (continued)

		0x1: ENABLED : Scatter/Gather DMA selected
16	dis_tx_ipgap_dly_check	Disable Linestate check for Token to Token/Data interpacket gap delay calculation (dis_tx_ipgap_dly_check) Applicable only in HS mode of operation. When enabled, the controller implements counter based logic to detect the end of token transmission, otherwise controller monitors the linestate for end of token transmission,to start the Token to Token and Token to Data interpacket delay counter. Default Value: 0x0 **0x0: DISABLE :** Enable Linestate check **0x1: ENABLE :** Disable Linestate check
15 : 8	ResValid	Resume Validation Period (ResValid) This field is effective only when HCFG.Ena32KHzS is set. It will control the resume period when the core resumes from suspend. The core counts for 'ResValid' number of clock cycles to detect a valid resume when this is set. Default Value: 0x2
7	Ena32KHzS	Enable 32 KHz Suspend mode (Ena32KHzS) This bit can be set only in FS PHY interface is selected. Else, this bit needs to be set to zero. When FS PHY interface is chosen and this bit is set, the core expects that the PHY clock during Suspend is switched from 48 MHz to 32 KHz. Default Value: 0x0 **0x0: DISABLED :** 32 KHz Suspend mode disabled **0x1: ENABLED :** 32 KHz Suspend mode enabled
2	FSLSSupp	FS- and LS-Only Support (FSLSSupp) The application uses this bit to control the core's enumeration speed. Using this bit, the application can make the core enumerate as a FS host, even If the connected device supports HS traffic. Do not make changes to this field after initial programming. - 1'b0: HS/FS/LS, based on the maximum speed supported by the connected device - 1'b1: FS/LS-only, even If the connected device can support HS Default Value: 0x0 **0x1: FSLS :** FS/LS-only, even if the connected device can support HS **0x0: HSFSLS :** HS/FS/LS, based on the maximum speed supported by the connected device

24.1.33 USBHS_DWC_otg_intreg_HCFG (continued)

1 : 0	FSLSPclkSel	FS/LS PHY Clock Select (FSLSPclkSel) When the core is in FS Host mode - 2'b00: PHY clock is running at 30/60 MHz - 2'b01: PHY clock is running at 48 MHz - Others: Reserved When the core is in LS Host mode - 2'b00: PHY clock is running at 30/60 MHz. When the UTMI+/ULPI PHY Low Power mode is not selected, use 30/60 MHz. - 2'b01: PHY clock is running at 48 MHz. When the UTMI+ PHY Low Power mode is selected, use 48MHz If the PHY supplies a 48 MHz clock during LS mode. - 2'b10: PHY clock is running at 6 MHz. In USB 1.1 FS mode, use 6 MHz when the UTMI+ PHY Low Power mode is selected and the PHY supplies a 6 MHz clock during LS mode. If you select a 6 MHz clock during LS mode, you must do a soft reset. - 2'b11: Reserved Notes: - When Core in FS mode, the internal and external clocks have the same frequency. - When Core in LS mode, -- If FSLSPclkSel = 2'b00: Internal and external clocks have the same frequency -- If FSLSPclkSel = 2'b10: Internal clock is the divided by eight version of external 48 MHz clock Default Value: 0x0 **0x0: CLK3060 :** PHY clock is running at 30/60 MHz **0x1: CLK48 :** PHY clock is running at 48 MHz **0x2: CLK6 :** PHY clock is running at 6 MHz

24.1.34 USBHS_DWC_otg_intreg_HFIR

Description: This register is used to control the interval between two consecutive SOFs.

Address: 0x44900404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	FrInt [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	FrInt [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							
Name	Reserved [23:17]							HFIRRldCtrl

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	HFIRRldCtrl	Reload Control (HFIRRldCtrl) This bit allows dynamic reloading of the HFIR register during run time. - 1'b0 : The HFIR cannot be reloaded dynamically - 1'b1: the HFIR can be dynamically reloaded during runtime. This bit needs to be programmed during initial configuration and its value should not be changed during runtime. Default Value: 0x0 **0x0: DISABLED :** The HFIR cannot be reloaded dynamically **0x1: ENABLED :** The HFIR can be dynamically reloaded during runtime

24.1.34 USBHS_DWC_otg_intreg_HFIR (continued)

15 : 0	FrInt	Frame Interval (FrInt) The value that the application programs to this field specifies the interval between two consecutive SOFs (FS) or micro-SOFs (HS) or Keep-Alive tokens (HS). This field contains the number of PHY clocks that constitute the required frame interval. The Default value set in this field is for FS operation when the PHY clock frequency is 60 MHz. The application can write a value to this register only after the Port Enable bit of the Host Port Control and Status register (HPRT.PrtEnaPort) has been Set. If no value is programmed, the core calculates the value based on the PHY clock specified in the FS/LS PHY Clock Select field of the Host Configuration register (HCFG.FSLSPclkSel). Do not change the value of this field after the initial configuration. - 125 s * (PHY clock frequency for HS) - 1 ms * (PHY clock frequency for FS/LS) Default Value: 0xEA60

24.1.35 USBHS_DWC_otg_intreg_HFNUM

Description: This register indicates the current frame number. It also indicates the time remaining (in terms of the number of PHY clocks) in the current (micro)frame. Note: Read the reset value of this register only after the following conditions: - If IDDIG_FILTER is disabled, read only when the PHY clock is stable. - If IDDIG_FILTER is enabled, read only after the filter timer expires.

Address: 0x44900408

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	FrNum [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	FrNum [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	FrRem [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	FrRem [31:24]							

Bits	Name	Description
31 : 16	FrRem	Frame Time Remaining (FrRem) Indicates the amount of time remaining in the current microframe (HS) or Frame (FS/LS), in terms of PHY clocks. This field decrements on each PHY clock. When it reaches zero, this field is reloaded with the value in the Frame Interval register and a new SOF is transmitted on the USB. Default Value: 0x0
15 : 0	FrNum	Frame Number (FrNum) This field increments when a new SOF is transmitted on the USB, and is reset to 0 when it reaches 16'h3FFF. Default Value: 0x3FFF **0x1: ACTIVE :** SOF is transmitted **0x0: INACTIVE :** No SOF is transmitted

24.1.36 USBHS_DWC_otg_intreg_HPTXSTS

Description: This register contains information about the Periodic Transmit Queue in the Host controller.

Address: 0x44900410

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	PTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	PTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R	R						
HW Access								
Name	PTxQTop	PTxQSpcAvail [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	PTxQTop [31:24]							

Bits	Name	Description
31 : 23	PTxQTop	Top of the Periodic Transmit Request Queue (PTxQTop) This indicates the Entry in the Periodic Tx Request Queue that is currently being processed by the MAC. This register is used for debugging. - Bit [31]: Odd/Even (micro)Frame -- 1'b0: send in even (micro)Frame -- 1'b1: send in odd (micro)Frame - Bits [30:27]: Channel/endpoint number - Bits [26:25]: Type -- 2'b00: IN/OUT -- 2'b01: Zero-length packet -- 2'b10: CSPLIT -- 2'b11: Disable channel command - Bit [24]: Last Periodic Entry for the selected periodic channel/endpoint - Bit [23]: Terminate (last Entry for the selected channel/endpoint) Default Value: 0x0
22 : 16	PTxQSpcAvail	Periodic Transmit Request Queue Space Available (PTxQSpcAvail) Indicates the number of free locations available to be written in the Periodic Transmit Request Queue. This queue holds both IN and OUT requests. - 7'h0: Periodic Transmit Request Queue is full - 7'h1: 1 location available - 7'h2: 2 locations available - n: n locations available (0 <= n <= 16) - Others: Reserved Default Value: 0x8

24.1.36 USBHS_DWC_otg_intreg_HPTXSTS (continued)

0x1: FREE1 :

1 location available

0xa: FREE10 :

10 locations available

0xb: FREE11 :

11 locations available

0xc: FREE12 :

12 locations available

0xd: FREE13 :

13 locations available

0xe: FREE14 :

14 locations available

0xf: FREE15 :

15 locations available

0x2: FREE2 :

2 locations available

0x3: FREE3 :

3 locations available

0x4: FREE4 :

4 locations available

0x5: FREE5 :

5 locations available

0x6: FREE6 :

6 locations available

0x7: FREE7 :

7 locations available

0x8: FREE8 :

8 locations available

24.1.36 USBHS_DWC_otg_intreg_HPTXSTS (continued)

		0x9: FREE9 : 9 locations available **0x0: FULL :** Periodic Transmit Request Queue is full
15 : 0	PTxFSpcAvail	Periodic Transmit Data FIFO Space Available (PTxFSpcAvail) Indicates the number of free locations available to be written to in the Periodic TxFIFO. Values are in terms of 32-bit words - 16'h0 : Periodic TxFIFO is full - 16'h1 : 1 word available - 16'h2 : 2 words available - 16'hn : n words available (where 0 n 32,768) - 16'h8000 : 32,768 words - Others : Reserved Default Value: 0x400

24.1.37 USBHS_DWC_otg_intreg_HAINT

Description: When a significant event occurs on a channel, the Host All Channels Interrupt register interrupts the application using the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt). This is shown in the "Interrupt Hierarchy" figure in the databook. There is one interrupt bit per channel, up to a maximum of 16 bits. Bits in this register are set and cleared when the application sets and clears bits in the corresponding Host Channel-n Interrupt register.

Address: 0x44900414

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	HAINT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	HAINT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	HAINT	Channel Interrupt for channel no. Default Value: 0x0 **0x1: ACTIVE :** Host Channel Interrupt **0x0: INACTIVE :** Not active

24.1.38 USBHS_DWC_otg_intreg_HAINTMSK

Description: The Host All Channel Interrupt Mask register works with the Host All Channel Interrupt register to interrupt the application when an event occurs on a channel. There is one interrupt mask bit per channel, up to a maximum of 16 bits.

Address: 0x44900418

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	HAINTMsk [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	HAINTMsk [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	HAINTMsk	Channel Interrupt Mask (HAINTMsk) One bit per channel: Bit 0 for channel 0, bit 15 for channel 15 Default Value: 0x0 **0x1: MASK :** Mask Channel interrupt **0x0: UNMASK :** Unmask Channel interrupt

24.1.39 USBHS_DWC_otg_intreg_HFLBAddr

Description: This register is present only in case of Scatter/Gather DMA. It is implemented as flops. This register holds the starting address of the Frame list information.

Address: 0x4490041C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	HFLBAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	HFLBAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	HFLBAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	HFLBAddr [31:24]							

Bits	Name	Description
31 : 0	HFLBAddr	The starting address of the Frame list. This register is used only for Isochronous and Interrupt Channels. Default Value: 0x0

24.1.40 USBHS_DWC_otg_intreg_HPRT

Description: This register is available only in Host mode. Currently, the OTG Host supports only one port. A single register holds USB port-related information such as USB reset, enable, suspend, resume, connect status, and test mode for each port. It is shown in the "Interrupt Hierarchy" figure in the databook. The R_SS_WC bits in this register can trigger an interrupt to the application through the Host Port Interrupt bit of the Core Interrupt register (GINTSTS.PrtInt). On a Port Interrupt, the application must read this register and clear the bit that caused the interrupt. For the R_SS_WC bits, the application must write a 1 to the bit to clear the interrupt.

Address: 0x44900440

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	R	RW	RW	RW	R
HW Access								
Name	PrtSusp	PrtRes	PrtOvrCur-rChng	PrtOvrCur-rAct	PrtEnChng	PrtEna	PrtConnDet	PrtConnSts

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	R		Reserved	RW
HW Access							Reserved	
Name	PrtTstCtl [15:13]			PrtPwr	PrtLnSts [11:10]		Reserved	PrtRst

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					R		RW
HW Access	Reserved							
Name	Reserved [23:19]					PrtSpd [18:17]		PrtTstCtl

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18 : 17	PrtSpd	Port Speed (PrtSpd) Indicates the speed of the device attached to this port. - 2'b00: High speed - 2'b01: Full speed - 2'b10: Low speed - 2'b11: Reserved Default Value: 0x0 **0x1: FULLSPD :** Full speed **0x0: HIGHSPD :** High speed **0x2: LOWSPD :** Low speed

24.1.40 USBHS_DWC_otg_intreg_HPRT (continued)

0x3: RESERVEDPrtSpdHPRT :

Reserved

16 : 13	PrtTstCtl	Port Test Control (PrtTstCtl) The application writes a nonzero value to this field to put the port into a Test mode, and the corresponding pattern is signaled on the port. - 4'b0000: Test mode disabled - 4'b0001: Test_J mode - 4'b0010: Test_K mode - 4'b0011: Test_SE0_NAK mode - 4'b0100: Test_Packet mode - 4'b0101: Test_Force_Enable - Others: Reserved To move the DWC_otg controller to test mode, you must set this field. Complete the following steps to move the DWC_otg core to test mode: - 1. Power on the core. - 2. Load the DWC_otg driver. - 3. Connect an HS device and enumerate to HS mode. - 4. Access the HPRT register to send test packets. - 5. Remove the device and connect to fixture (OPT) port. The DWC_otg host core continues sending out test packets. - 6. Test the eye diagram. Default Value: 0x0 **0x0: DISABLED :** Test mode disabled **0x5: TESTFENB :** Test_force_Enable **0x1: TESTJ :** Test_J mode **0x2: TESTK :** Test_K mode **0x4: TESTPM :** Test_Packet mode **0x3: TESTSN :** Test_SE0_NAK mode
12	PrtPwr	Port Power (PrtPwr) The application uses this field to control power to this port (write 1'b1 to set to 1'b1 and write 1'b0 to set to 1'b0), and the core can clear this bit on an over current condition. - 1'b0: Power off - 1'b1: Power on Note: This bit is interface independent. The application needs to program this bit for all interfaces as described in the host programming flow in the Programming Guide. Default Value: 0x0

24.1.40 USBHS_DWC_otg_intreg_HPRT (continued)

		0x0: OFF : Power off **0x1: ON :** Power on
11 : 10	PrtLnSts	Port Line Status (PrtLnSts) Indicates the current logic level USB data lines - Bit [10]: Logic level of D+ - Bit [11]: Logic level of D- Default Value: 0x0 **0x2: MINUSD :** Logic level of D- **0x1: PLUSD :** Logic level of D+
8	PrtRst	Port Reset (PrtRst) When the application sets this bit, a reset sequence is started on this port. The application must time the reset period and clear this bit after the reset sequence is complete. - 1'b0: Port not in reset - 1'b1: Port in reset The application must leave this bit set for at least a minimum duration mentioned below to start a reset on the port. The application can leave it set for another 10 ms in addition to the required minimum duration, before clearing the bit, even though there is no maximum limit Set by the USB standard.This bit is cleared by the core even if there is no device connected to the Host. - High speed: 50 ms - Full speed/Low speed: 10 ms Default Value: 0x0 **0x0: DISABLED :** Port not in reset **0x1: ENABLED :** Port in reset

24.1.40 USBHS_DWC_otg_intreg_HPRT (continued)

7	PrtSusp	Port Suspend (PrtSusp) The application sets this bit to put this port in Suspend mode. The core only stops sending SOFs when this is Set. To stop the PHY clock, the application must Set the Port Clock Stop bit, which asserts the suspend input pin of the PHY. The read value of this bit reflects the current suspend status of the port. This bit is cleared by the core after a remote wakeup signal is detected or the application sets the Port Reset bit or Port Resume bit in this register or the Resume/Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register (GINTSTS.WkUpInt or GINTSTS.DisconnInt, respectively).This bit is cleared by the core even if there is no device connected to the Host. - 1'b0: Port not in Suspend mode - 1'b1: Port in Suspend mode Default Value: 0x0 **0x1: ACTIVE :** Port in Suspend mode **0x0: INACTIVE :** Port not in Suspend mode
6	PrtRes	Port Resume (PrtRes) The application sets this bit to drive resume signaling on the port. The core continues to drive the resume signal until the application clears this bit. If the core detects a USB remote wakeup sequence, as indicated by the Port Resume/Remote Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.WkUpInt), the core starts driving resume signaling without application intervention and clears this bit when it detects a disconnect condition. The read value of this bit indicates whether the core is currently driving resume signaling. - 1'b0: No resume driven - 1'b1: Resume driven When LPM is enabled, In L1 state the behavior of this bit is as follows: The application sets this bit to drive resume signaling on the port. The core continues to drive the resume signal until a pre-determined time specified in GLPMCFG.HIRD_Thres[3:0] field. If the core detects a USB remote wakeup sequence, as indicated by the Port L1Resume/Remote L1Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.L1WkUpInt), the core starts driving resume signaling without application intervention and clears this bit at the end of resume.This bit can be set by both core or application and also cleared by core or application. This bit is cleared by the core even if there is no device connected to the Host. Default Value: 0x0 **0x0: NORESUME :** No resume driven **0x1: RESUME :** Resume driven

24.1.40 USBHS_DWC_otg_intreg_HPRT (continued)

5	PrtOvrCurrChng	Port Overcurrent Change (PrtOvrCurrChng) The core sets this bit when the status of the Port Overcurrent Active bit (bit 4) in this register changes.This bit can be set only by the core and the application should write 1 to clear it Default Value: 0x0 **0x1: ACTIVE :** Status of port overcurrent changed **0x0: INACTIVE :** Status of port overcurrent status is not changed
4	PrtOvrCurrAct	Port Overcurrent Active (PrtOvrCurrAct) Indicates the overcurrent condition of the port. - 1'b0: No overcurrent condition - 1'b1: Overcurrent condition Default Value: 0x0 **0x1: ACTIVE :** Overcurrent condition **0x0: INACTIVE :** No overcurrent condition
3	PrtEnChng	Port Enable/Disable Change (PrtEnChng) The core sets this bit when the status of the Port Enable bit [2] of this register changes.This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** Port Enable bit 2 changed **0x0: INACTIVE :** Port Enable bit 2 has not changed
2	PrtEna	Port Enable (PrtEna) A port is enabled only by the core after a reset sequence, and is disabled by an overcurrent condition, a disconnect condition, or by the application clearing this bit. The application cannot Set this bit by a register write. It can only clear it to disable the port by writing 1. This bit does not trigger any interrupt to the application. - 1'b0: Port disabled - 1'b1: Port enabled Default Value: 0x0 **0x0: DISABLED :** Port disabled **0x1: ENABLED :** Port enabled

24.1.40 USBHS_DWC_otg_intreg_HPRT (continued)

1	PrtConnDet	Port Connect Detected (PrtConnDet) The core sets this bit when a device connection is detected to trigger an interrupt to the application using the Host Port Interrupt bit of the Core Interrupt register (GINTSTS.PrtInt).This bit can be set only by the core and the application should write 1 to clear it.The application must write a 1 to this bit to clear the interrupt. Default Value: 0x0 **0x1: ACTIVE :** Device connection detected **0x0: INACTIVE :** No device connection detected
0	PrtConnSts	Port Connect Status (PrtConnSts) - 0: No device is attached to the port. - 1: A device is attached to the port. Default Value: 0x0 **0x1: ATTACHED :** A device is attached to the port **0x0: NOTATTACHED :** No device is attached to the port

24.1.41 USBHS_DWC_otg_intreg_HCCHAR0

Description: This register contains the characteristics of the Host Channel.

Address: 0x44900500

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW				RW		
HW Access								
Name	EPDir	EPNum [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	Reserved
HW Access								Reserved
Name	DevAddr [23:22]		EC [21:20]		EPType [19:18]		LSpdDev	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW				
HW Access								
Name	ChEna	ChDis	OddFrm	DevAddr [28:24]				

Bits	Name	Description
31	ChEna	Channel Enable (ChEna) When Scatter/Gather mode is enabled - 1'b0: Indicates that the descriptor structure is not yet ready. - 1'b1: Indicates that the descriptor structure and data buffer with data is setup and this channel can access the descriptor. When Scatter/Gather mode is disabled This field is set by the application and cleared by the OTG host. - 1'b0: Channel disabled - 1'b1: Channel enabled Default Value: 0x0 **0x0: DISABLED :** If Scatter/Gather mode is enabled, indicates that the descriptor structure is not yet ready. If Scatter/Gather mode is disabled, indicates that the channel is disabled. **0x1: ENABLED :** If Scatter/Gather mode is enabled, indicates that the descriptor structure and data buffer with data is set up and this channel can access the descriptor. If Scatter/Gather mode is disabled, indicates that the channel is enabled.

24.1.41 USBHS_DWC_otg_intreg_HCCHAR0 (continued)

30	ChDis	Channel Disable (ChDis) The application sets this bit to stop transmitting/receiving data on a channel, even before the transfer for that channel is complete. The application must wait for the Channel Disabled interrupt before treating the channel as disabled. Default Value: 0x0 **0x1: ACTIVE :** Stop transmitting/receiving data on channel **0x0: INACTIVE :** Transmit/Recieve normal
29	OddFrm	Odd Frame (OddFrm) This field is set (reset) by the application to indicate that the OTG host must perform a transfer in an odd (micro)Frame. This field is applicable for only periodic (isochronous and interrupt) transactions. - 1'b0: Even (micro)Frame - 1'b1: Odd (micro)Frame Default Value: 0x0 **0x0: EFRAME :** Even Frame Transfer **0x1: OFRAME :** Odd Frame Transfer
28 : 22	DevAddr	Device Address (DevAddr) This field selects the specific device serving as the data source or sink. Default Value: 0x0
21 : 20	EC	Multi Count (MC) / Error Count (EC) When the Split Enable bit of the Host Channel-n Split Control register (HCSPLTn.SpltEna) is reset (1'b0), this field indicates to the host the number of transactions that must be executed per microframe for this periodic endpoint. For non periodic transfers, this field is used only in DMA mode, and specifies the number packets to be fetched for this channel before the internal DMA engine changes arbitration. - 2'b00: Reserved This field yields undefined results. - 2'b01: 1 transaction - 2'b10: 2 transactions to be issued for this endpoint per microframe - 2'b11: 3 transactions to be issued for this endpoint per microframe When HCSPLTn.SpltEna is Set (1'b1), this field indicates the number of immediate retries to be performed for a periodic split transactions on transaction errors. This field must be Set to at least 2'b01. Default Value: 0x0 **0x0: RESERVEDECHCCHAR0 :** Reserved. This field yields undefined result **0x1: TRANSONE :** 1 transaction

24.1.41 USBHS_DWC_otg_intreg_HCCHAR0 (continued)

		0x3: TRANSTHREE : 3 transactions to be issued for this endpoint per microframe **0x2: TRANSTWO :** 2 transactions to be issued for this endpoint per microframe
19 : 18	EPType	Endpoint Type (EPType) Indicates the transfer type selected. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CTRL :** Control **0x3: INTERR :** Interrupt **0x1: ISOC :** Isochronous
17	LSpdDev	Low-Speed Device (LSpdDev) This field is Set by the application to indicate that this channel is communicating to a low-speed device. The application must program this bit when a low speed device is connected to the host through an FS HUB. The DWC_otg Host core uses this field to drive the XCVR_SELECT signal to 2'b11 while communicating to the LS Device through the FS hub. Note: In a peer to peer setup, the DWC_otg Host core ignores this bit even if it is set by the application software. Default Value: 0x0 **0x0: DISABLED :** Not Communicating with low speed device **0x1: ENABLED :** Communicating with low speed device
15	EPDir	Endpoint Direction (EPDir) Indicates whether the transaction is IN or OUT. - 1'b0: OUT - 1'b1: IN Default Value: 0x0 **0x1: IN :** IN Direction

24.1.41 USBHS_DWC_otg_intreg_HCCHAR0 (continued)

0x0: OUT :

OUT Direction

14 : 11	EPNum	Endpoint Number (EPNum) Indicates the endpoint number on the device serving as the data source or sink. Default Value: 0x0

0x0: ENDPT0 :

End point 0

0x1: ENDPT1 :

End point 1

0xa: ENDPT10 :

End point 10

0xb: ENDPT11 :

End point 11

0xc: ENDPT12 :

End point 12

0xd: ENDPT13 :

End point 13

0xe: ENDPT14 :

End point 14

0xf: ENDPT15 :

End point 15

0x2: ENDPT2 :

End point 2

0x3: ENDPT3 :

End point 3

0x4: ENDPT4 :

End point 4

0x5: ENDPT5 :

End point 5

24.1.41 USBHS_DWC_otg_intreg_HCCHAR0 (continued)

0x6: ENDPT6 :

End point 6

0x7: ENDPT7 :

End point 7

0x8: ENDPT8 :

End point 8

0x9: ENDPT9 :

End point 9

10 : 0	MPS	Maximum Packet Size (MPS) Indicates the maximum packet size of the associated endpoint. Default Value: 0x0

24.1.42 USBHS_DWC_otg_intreg_HCSPLT0

Description: This register contains the Split characteristics of the Host Channel.

Address: 0x44900504

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access								
Name	HubAddr	PrtAddr [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access								
Name	XactPos [15:14]		HubAddr [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							
Name	Reserved [23:17]							CompSplt

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access		Reserved						
Name	SpltEna	Reserved [30:24]						

Bits	Name	Description
31	SpltEna	Split Enable (SpltEna) The application sets this field to indicate that this channel is enabled to perform split transactions. Default Value: 0x0 **0x0: DISABLED :** Split not enabled **0x1: ENABLED :** Split enabled
16	CompSplt	Do Complete Split (CompSplt) The application sets this field to request the OTG host to perform a complete split transaction. Default Value: 0x0 **0x0: NOSPLIT :** No complete split transaction **0x1: SPLIT :** Complete Split transaction

24.1.42 USBHS_DWC_otg_intreg_HCSPLT0 (continued)

15 : 14	XactPos	Transaction Position (XactPos) This field is used to determine whether to send all, first, middle, or last payloads with each OUT transaction. - 2'b11: All. This is the entire data payload is of this transaction (which is less than or equal to 188 bytes). - 2'b10: Begin. This is the first data payload of this transaction (which is larger than 188 bytes). - 2'b00: Mid. This is the middle payload of this transaction (which is larger than 188 bytes). - 2'b01: End. This is the last payload of this transaction (which is larger than 188 bytes). Default Value: 0x0 **0x3: ALL :** All. This is the entire data payload of this transaction (which is less than or equal to 188 bytes) **0x2: BEGIN :** Begin. This is the first data payload of this transaction (which is larger than 188 bytes) **0x1: END :** End. This is the last payload of this transaction (which is larger than 188 bytes) **0x0: MIDDLE :** Mid. This is the middle payload of this transaction (which is larger than 188 bytes)
13 : 7	HubAddr	Hub Address (HubAddr) This field holds the device address of the transaction translator's hub. Default Value: 0x0
6 : 0	PrtAddr	Port Address (PrtAddr) This field is the port number of the recipient transaction translator. Default Value: 0x0

24.1.43 USBHS_DWC_otg_intreg_HCINT0

Description: This register indicates the status of a channel with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the Host Channels Interrupt bit of the Core Interrupt register (GINTSTS.HChInt) is set. Before the application can read this register, it must first read the Host All Channels Interrupt (HAINT) register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers.

Address: 0x44900508

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	XactErr	NYET	ACK	NAK	STALL	AHBErr	ChHltd	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved [15:14]		DESC_LST_ROLLIntr	XCS_XACT_ERR	BNAIntr	DataTglErr	FrmOvrun	BblErr

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
13	DESC_LST_ROLLIntr	Descriptor rollover interrupt (DESC_LST_ROLLIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when the corresponding channel's descriptor list rolls over. For non Scatter/Gather DMA mode, this bit is reserved. Default Value: 0x0 **0x1: ACTIVE :** Descriptor rollover interrupt **0x0: INACTIVE :** No Descriptor rollover interrupt
12	XCS_XACT_ERR	Excessive Transaction Error (XCS_XACT_ERR) This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when 3 consecutive transaction errors occurred on the USB bus. XCS_XACT_ERR will not be generated for Isochronous channels. For non Scatter/Gather DMA mode, this bit is reserved. Default Value: 0x0

24.1.43 USBHS_DWC_otg_intreg_HCINT0 (continued)

		0x1: ACTIVE : Excessive Transaction Error **0x0: INACTIVE :** No Excessive Transaction Error
11	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process. BNA will not be generated for Isochronous channels. For non Scatter/Gather DMA mode, this bit is reserved. Default Value: 0x0 **0x1: ACTIVE :** BNA Interrupt **0x0: INACTIVE :** No BNA Interrupt
10	DataTglErr	Data Toggle Error (DataTglErr).This bit can be set only by the core and the application should write 1 to clear it.In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core. Default Value: 0x0 **0x1: ACTIVE :** Data Toggle Error **0x0: INACTIVE :** No Data Toggle Error
9	FrmOvrun	Frame Overrun (FrmOvrun). In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core. This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** Frame Overrun **0x0: INACTIVE :** No Frame Overrun
8	BblErr	Babble Error (BblErr) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core. This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** Babble Error

24.1.43 USBHS_DWC_otg_intreg_HCINT0 (continued)

		0x0: INACTIVE : No Babble Error
7	XactErr	Transaction Error (XactErr) Indicates one of the following errors occurred on the USB. - CRC check failure - Timeout - Bit stuff error - False EOP In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** Transaction Error **0x0: INACTIVE :** No Transaction Error
6	NYET	NYET Response Received Interrupt (NYET) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** NYET Response Received Interrupt **0x0: INACTIVE :** No NYET Response Received Interrupt
5	ACK	ACK Response Received/Transmitted Interrupt (ACK) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** ACK Response Received or Transmitted Interrup **0x0: INACTIVE :** No ACK Response Received or Transmitted Interrupt
4	NAK	NAK Response Received Interrupt (NAK) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** NAK Response Received Interrupt **0x0: INACTIVE :** No NAK Response Received Interrupt

24.1.43 USBHS_DWC_otg_intreg_HCINT0 (continued)

3	STALL	STALL Response Received Interrupt (STALL) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.This bit can be set only by the core and the application should write 1 to clear it. Default Value: 0x0 **0x1: ACTIVE :** Stall Response Received Interrupt **0x0: INACTIVE :** No Stall Response Received Interrupt
2	AHBErr	AHB Error (AHBErr) This is generated only in Internal DMA mode when there is an AHB error during AHB read/write. The application can read the corresponding channel's DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB error during AHB read/write **0x0: INACTIVE :** No AHB error
1	ChHltd	Channel Halted (ChHltd) In non Scatter/Gather DMA mode, it indicates the transfer completed abnormally either because of any USB transaction error or in response to disable request by the application or because of a completed transfer. In Scatter/gather DMA mode, this indicates that transfer completed due to any of the following - EOL being set in descriptor - AHB error - Excessive transaction errors - Babble - Stall Default Value: 0x0 **0x1: ACTIVE :** Channel Halted **0x0: INACTIVE :** Channel not halted
0	XferCompl	Transfer Completed (XferCompl) Transfer completed normally without any errors.This bit can be set only by the core and the application should write 1 to clear it. - For Scatter/Gather DMA mode, it indicates that current descriptor processing got completed with IOC bit set in its descriptor. - In non Scatter/Gather DMA mode, it indicates that Transfer completed normally without any errors. Default Value: 0x0 **0x1: ACTIVE :** Transfer completed normally without any errors

24.1.43 USBHS_DWC_otg_intreg_HCINT0 (continued)

0x0: INACTIVE :

Transfer in progress or No Active Transfer

24.1.44 USBHS_DWC_otg_intreg_HCINTMSK0

Description: This register reflects the mask for each channel status described in the previous section.

Address: 0x4490050C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved							
Name	Reserved [7:3]					AHBErrMsk	ChHltdMsk	XferCom-plMsk

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW	Reserved	RW	Reserved		
HW Access	Reserved			Reserved		Reserved		
Name	Reserved [15:14]		DESC_L-ST_ROL-LIntrMsk	Reserved	BNAIntrMsk	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
13	DESC_LST_ROLLIntrMsk	Descriptor List rollover interrupt Mask register(DESC_LST_ROLLIntrMsk) This bit is valid only when Scatter/Gather DMA mode is enabled. Default Value: 0x0 **0x0: MASK :** Descriptor Rollover Interrupt Mask **0x1: NOMASK :** Descriptor Rollover Interrupt not masked
11	BNAIntrMsk	BNA (Buffer Not Available) Interrupt mask register (BNAIntrMsk) This bit is valid only when Scatter/Gather DMA mode is enabled. Default Value: 0x0 **0x0: MASK :** BNA Interrupt Masked **0x1: NOMASK :** BNA Interrupt not masked

24.1.44 USBHS_DWC_otg_intreg_HCINTMSK0 (continued)

2	AHBErrMsk	AHB Error Mask (AHBErrMsk) In scatter/gather DMA mode for host, interrupts will not be generated due to the corresponding bits set in HCINTn. Default Value: 0x0 **0x0: MASK :** AHB Error Mask **0x1: NOMASK :** No AHB Error Mask
1	ChHltdMsk	Channel Halted Mask (ChHltdMsk) Default Value: 0x0 **0x0: MASK :** Channel Halted Mask **0x1: NOMASK :** No Channel Halted Mask
0	XferComplMsk	Transfer Completed Mask (XferComplMsk) Default Value: 0x0 **0x0: MASK :** Transfer Completed Mask **0x1: NOMASK :** No Transfer Completed Mask

24.1.45 USBHS_DWC_otg_intreg_HCTSIZ0

Description: This register reflects the transfer size for the Host Channel.

Address: 0x44900510

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW		RW				
HW Access								
Name	DoPng	Pid [30:29]		PktCnt [28:24]				

Bits	Name	Description
31	DoPng	Do Ping (DoPng) This bit is used only for OUT transfers. Setting this field to 1 directs the host to do PING protocol. Note: Do not set this bit for IN transfers. If this bit is set for for IN transfers it disables the channel. Default Value: 0x0 **0x0: NOPING :** No ping protocol **0x1: PING :** Ping protocol
30 : 29	Pid	PID (Pid) The application programs this field with the type of PID to use for the initial transaction. The host maintains this field for the rest of the transfer. - 2'b00: DATA0 - 2'b01: DATA2 - 2'b10: DATA1 - 2'b11: MDATA (non-control)/SETUP (control) Default Value: 0x0 **0x0: DATA0 :** DATA0

24.1.45 USBHS_DWC_otg_intreg_HCTSIZ0 (continued)

		0x2: DATA1 : DATA1 **0x1: DATA2 :** DATA2 **0x3: MDATA :** MDATA (non-control)/SETUP (control)
28 : 19	PktCnt	Non-Scatter/Gather DMA Mode: Packet Count (PktCnt) This field is programmed by the application with the expected number of packets to be transmitted (OUT) or received (IN). The host decrements this count on every successful transmission or reception of an OUT/IN packet. Once this count reaches zero, the application is interrupted to indicate normal completion. The width of this counter is specified as Width of Packet Counters during coreConsultant configuration (parameter OTG_PACKET_COUNT_WIDTH). Scatter/Gather DMA Mode: [28:19]: Reserved Default Value: 0x0

24.1.45 USBHS_DWC_otg_intreg_HCTSIZ0 (continued)

18 : 0	XferSize	Non-Scatter/Gather DMA Mode: Transfer Size (XferSize) For an OUT, this field is the number of data bytes the host sends during the transfer. For an IN, this field is the buffer size that the application has Reserved for the transfer. The application is expected to program this field as an integer multiple of the maximum packet size for IN transactions (periodic and non-periodic). The width of this counter is specified as Width of Transfer Size Counters during coreConsultant configuration (parameter OTG_TRANS_COUNT_WIDTH). Scatter/Gather DMA Mode: [18:16]: Reserved [15:8]: NTD (Number of Transfer Descriptors) (Non Isochronous) This value is in terms of number of descriptors. Maximum number of descriptor that can be present in the list is 64. The values can be from 0 to 63. - 0: 1 descriptor - 63: 64 descriptors This field indicates the total number of descriptors present in that list. The core will wrap around after servicing NTD number of descriptors for that list. (Isochronous) This field indicates the number of descriptors present in that list microframe. The possible values for FS are - 1: 2 descriptors - 3: 4 descriptors - 7: 8 descriptors - 15: 16 descriptors - 31: 32 descriptors - 63: 64 descriptors The possible values for HS are - 7: 8 descriptors - 15: 16 descriptors - 31: 32 descriptors - 63: 64 descriptors - 127: 128 descriptors - 255: 256 descriptors [7:0]: SCHED_INFO (Schedule information) Every bit in this 8 bit register indicates scheduling for that microframe. Bit 0 indicates scheduling for 1st microframe and bit 7 indicates scheduling for 8th microframe in that frame. A value of 8'b11111111 indicates that the corresponding interrupt channel is scheduled to issue a token every microframe in that frame. A value of 8'b10101010 indicates that the corresponding interrupt channel is scheduled to issue a token every alternate microframe starting with second microframe. Note that this field is applicable only for periodic (Isochronous and Interrupt) channels. Default Value: 0x0

24.1.46 USBHS_DWC_otg_intreg_HCDMA0

Description: This register is used by the OTG host in the internal DMA mode to maintain the current buffer pointer for IN/OUT transactions. The starting DMA address must be DWORD-aligned.

Address: 0x44900514

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description

24.1.46 USBHS_DWC_otg_intreg_HCDMA0 (continued)

31 : 0	DMAAddr	In Buffer DMA Mode: [31:0]: DMA Address (DMAAddr) This field holds the start address in the external memory from which the data for the endpoint must be fetched or to which it must be stored. This register is incremented on every AHB transaction. Reset: X if not programmed as the register is in SPRAM. In Scatter-Gather DMA (DescDMA) Mode for Non-Isochronous: [31:9]: DMA Address (DMAAddr) The start address must be 512-bytes aligned. This field holds the start address of the 512 bytes page. The first descriptor in the list should be located in this address. The first descriptor may be or may not be ready. The core starts processing the list from the CTD value. [8:3]: Current Transfer Desc(CTD) This value is in terms of number of descriptors. The values can be from 0 to 63. - 0 - 1 descriptor. - 63 - 64 descriptors. This field indicates the current descriptor processed in the list. This field is updated both by application and the core. For example, if the application enables the channel after programming CTD=5, then the core will start processing the sixth descriptor. The address is obtained by adding a value of (8bytes*5=) 40(decimal) to DMAAddr. Reset: 6'h0 [2:0]: Reserved In Scatter-Gather DMA (DescDMA) Mode for Isochronous: [31:N]: DMA Address (DMAAddr) The start address must be 512-bytes aligned. This field holds the address of the 2*(nTD+1) bytes of locations in which the isochronous descriptors are present where N is based on nTD as follows: - [31:N]: Base Address - [N-1:3]: Offset - [2:0]: 000 For HS ISOC, if nTD is, - 7, N=6 - 15, N=7 - 31, N=8 - 63, N=9 - 127, N=10 - 255, N=11 For FS ISOC, if nTD is, - 1, N=4 - 3, N=5 - 7, N=6 - 15, N=7 - 31, N=8 - 63, N=9 [N-1:3]: Current Transfer Desc(CTD) CTD for isochronous is based on the current frame/(micro)frame value. Need to be set to zero by application. Reset: (N+1:3)'h0 [2:0]: Reserved Default Value: 0x0

24.1.47 USBHS_DWC_otg_intreg_HCDMAB0

Description: This register is present only in case of Scatter/Gather DMA. It is implemented in RAM instead of flop-based implementation. This register holds the current buffer address.

Address: 0x4490051C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	HCDMAB [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	HCDMAB [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	HCDMAB [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	HCDMAB [31:24]							

Bits	Name	Description
31 : 0	HCDMAB	Holds the current buffer address. This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: 0x0

24.1.48 USBHS_DWC_otg_intreg_DCFG

Description: This register configures the core in Device mode after power-on or after certain control commands or enumeration. Do not make changes to this register after initial programming.

Address: 0x44900800

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW	RW	RW	
HW Access								
Name	DevAddr [7:4]				Ena32KHz-Susp	NZSt-sOUTHShk	DevSpd [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW		RW		
HW Access								
Name	Erra-ticIntMsk	XCVRDLY	EnDevOut-Nak	PerFrInt [12:11]		DevAddr [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	Reserved					RW	Reserved
HW Access		Reserved						Reserved
Name	DescDMA	Reserved [22:18]					ipgisocSupt	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	RW						RW	
HW Access								
Name	ResValid [31:26]						PerSchIntvl [25:24]	

Bits	Name	Description
31 : 26	ResValid	Resume Validation Period (ResValid) This field is effective only when DCFG.Ena32KHzSusp is set. It controls the resume period when the core resumes from suspend. The core counts for ResValid number of clock cycles to detect a valid resume when this bit is set Default Value: 0x2
25 : 24	PerSchIntvl	Periodic Scheduling Interval (PerSchIntvl) PerSchIntvl must be programmed for Scatter/Gather DMA mode. This field specifies the amount of time the Internal DMA engine must allocate for fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25,50 or 75% of (micro)Frame. - When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data . - When no periodic endpoints are active, Then the internal DMA engine services non-periodic endpoints, ignoring this field. - After the specified time within a (micro)Frame, the DMA switches to fetching for non-periodic endpoints. -- 2'b00: 25% of (micro)Frame. -- 2'b01: 50% of (micro)Frame. -- 2'b10: 75% of (micro)Frame. -- 2'b11: Reserved. Reset: 2'b00 Default Value: 0x0

24.1.48 USBHS_DWC_otg_intreg_DCFG (continued)

		0x0: MF25 : 25% of :DWC_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame **0x1: MF50 :** 50% of :DWC_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame **0x2: MF75 :** 75% of :DWC_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame **0x3: RESERVEDPerSchIntvlDCFG :** Reserved
23	DescDMA	Enable Scatter/gather DMA in device mode (DescDMA). When the Scatter/Gather DMA option selected during configuration of the RTL, the application can Set this bit during initialization to enable the Scatter/Gather DMA operation. Note: This bit must be modified only once after a reset. The following combinations are available for programming: - GAHBCFG.DMAEn=0,DCFG.DescDMA=0 => Slave mode - GAHBCFG.DMAEn=0,DCFG.DescDMA=1 => Invalid - GAHBCFG.DMAEn=1,DCFG.DescDMA=0 => Buffered DMA mode - GAHBCFG.DMAEn=1,DCFG.DescDMA=1 => Scatter/Gather DMA mode Default Value: 0x0 **0x0: DISABLED :** Disable Scatter/Gather DMA **0x1: ENABLED :** Enable Scatter/Gather DMA
17	ipgisocSupt	Worst-Case Inter-Packet Gap ISOC OUT Support (ipgisocSupt) This bit indicates that the controller supports the worst-case scenario of Rx followed by Rx Inter-Packet Gap (IPG) (32 bit times) as per the UTMI Specification for any token following an ISOC OUT token. Without this support, when any token follows an ISOC OUT token with the worst-case IPG, the controller will not detect the followed token. The worst-case IPG of the controller without this support depends on the AHB and PHY clock frequency. Default Value: 0x1 **0x0: DISABLED :** Worst-Case Inter-Packet Gap ISOC OUT Support is disabled **0x1: ENABLED :** Worst-Case Inter-Packet Gap ISOC OUT Support is enabled
15	ErraticIntMsk	Erratic Error Interrupt Mask Default Value: 0x0 **0x1: MASK :** Mask early suspend interrupt on erratic error

24.1.48 USBHS_DWC_otg_intreg_DCFG (continued)

		0x0: NOMASK : Early suspend interrupt is generated on erratic error
14	XCVRDLY	XCVRDLY Enables or disables delay between xcvr_sel and txvalid during device chirp Default Value: 0x0 **0x0: DISABLE :** No delay between xcvr_sel and txvalid during Device chirp **0x1: ENABLE :** Enable delay between xcvr_sel and txvalid during Device chirp
13	EnDevOutNak	Enable Device OUT NAK (EnDevOutNak) This bit enables setting NAK for Bulk OUT endpoints after the transfer is completed for Device mode Descriptor DMA - 1'b0 : The core does not set NAK after Bulk OUT transfer complete - 1'b1 : The core sets NAK after Bulk OUT transfer complete This bit is one time programmable after reset like any other DCFG register bits. Default Value: 0x0 **0x0: DISABLED :** The core does not set NAK after Bulk OUT transfer complete **0x1: ENABLED :** The core sets NAK after Bulk OUT transfer complete
12 : 11	PerFrInt	Periodic Frame Interval (PerFrInt) Indicates the time within a (micro)Frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine If all the isochronous traffic for that (micro)Frame is complete. - 2'b00: 80% of the (micro)Frame interval - 2'b01: 85% of the (micro)Frame interval - 2'b10: 90% of the (micro)Frame interval - 2'b11: 95% of the (micro)Frame interval Default Value: 0x0 **0x0: EOPF80 :** 80% of the :DWC_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame interval **0x1: EOPF85 :** 85% of the :DWC_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame interval **0x2: EOPF90 :** 90% of the :DWC_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame interval **0x3: EOPF95 :** 95% of the :DWC_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame interval

24.1.48 USBHS_DWC_otg_intreg_DCFG (continued)

10 : 4	DevAddr	Device Address (DevAddr) The application must program this field after every SetAddress control command. Default Value: 0x0
3	Ena32KHzSusp	Enable 32 KHz Suspend mode (Ena32KHzSusp) This bit can be set only if FS PHY interface is selected. Otherwise, this bit needs to be set to zero. If FS PHY interface is chosen and this bit is set, the PHY clock during Suspend must be switched from 48 MHz to 32 KHz. Default Value: 0x0 **0x0: DISABLED :** USB 1.1 Full-Speed Serial Transceiver not selected **0x1: ENABLED :** USB 1.1 Full-Speed Serial Transceiver Interface selected
2	NZStsOUTHShk	Non-Zero-Length Status OUT Handshake (NZStsOUTHShk) The application can use this field to select the handshake the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage. - 1'b1: Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application. - 1'b0: Send the received OUT packet to the application (zerolength or nonzero-length) and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register. Default Value: 0x0 **0x0: SENDOUT :** Send the received OUT packet to the application (zero-length or non-zero length) and send a handshake based on NAK and STALL bits for the endpoint in the Devce Endpoint Control Register **0x1: SENDSTALL :** Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application
1 : 0	DevSpd	Device Speed (DevSpd) Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application can support. However, the actual bus speed is determined only after the connect sequence is completed, and is based on the speed of the USB host to which the core is connected. Default Value: 0x0 **0x3: USBFS1148 :** Full speed USB 1.1 transceiver clock is 48 MHz **0x1: USBFS20 :** Full speed USB 2.0 PHY clock is 30 MHz or 60 MHz **0x0: USBHS20 :** High speed USB 2.0 PHY clock is 30 MHz or 60 MHz **0x2: USBLS116 :** Low speed USB 1.1 transceiver clock is 6 MHz

24.1.49 USBHS_DWC_otg_intreg_DCTL

Description: This register is used to control the characteristics of the Device controller.

Address: 0x44900804

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	RW			R	R	RW	RW
HW Access								
Name	SGNPInNak	TstCtl [6:4]			GOUT-NakSts	GNPIN-NakSts	SftDiscon	RmtWk-UpSig

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		Reserved	RW	W	W	W
HW Access				Reserved				
Name	IgnrFrm-Num	GMC [14:13]		Reserved	PWROn-PrgDone	CGOUTNak	SGOUTNak	CGNPInNak

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved [23:20]				ServInt	DeepSleep-BESLReject	EnCon-tOnBNA	NakOnBble

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19	ServInt	Service Interval based scheduling for Isochronous IN Endpoints This field is used to enable service interval based scheduling feature for ISOC IN EPs. Note: This bit is applicable only in device mode and when Scatter/Gather DMA mode is used. This feature should not be enabled along with DCTL.IgnrFrmNum. Scatter/Gather DMA Mode (GAHBCFG.DMAEn=1,DCFG.DescDMA=1): When this bit is enabled, the frame number field in the ISOC IN descriptor structure is interpreted as the last frame of the service interval. In Scatter/Gather DMA mode, if this bit is enabled, the pending packets are flushed by the controller at the last frame of the service interval. Default Value: 0x0 **0x0: DISABLED :** The controller behavior depends on DCTL.IgnrFrmNum field. **0x1: ENABLED :** :DWC_DESIGN_ID==0>Scatter/Gather DMA Mode: The controller can transmit the packets in any frame of the service interval.

24.1.49 USBHS_DWC_otg_intreg_DCTL (continued)

18	DeepSleepBESLReject	DeepSleepBESLReject - 1: Deep Sleep BESL Reject feature is enabled - 0: Deep Sleep BESL Reject feature is disabled Core rejects LPM request with HIRD value greater than HIRD threshold programmed. NYET response is sent for LPM tokens with HIRD value greater than HIRD threshold. By default, the Deep Sleep BESL Reject feature is disabled. Default Value: 0x0 **0x0: DISABLED :** Deep Sleep BESL Reject feature is disabled **0x1: ENABLED :** Deep Sleep BESL Reject feature is enabled
17	EnContOnBNA	Enable Continue on BNA (EnContOnBNA) This bit enables the core to continue on BNA for Bulk OUT endpoints. With this feature enabled, when a Bulk OUT or INTR OUT endpoint receives a BNA interrupt the core starts processing the descriptor that caused the BNA interrupt after the endpoint re-enables the endpoint. - 1'b0: After receiving BNA interrupt,the core disables the endpoint. When the endpoint is re-enabled by the application, the core starts processing from the DOEPDMA descriptor. - 1'b1: After receiving BNA interrupt, the core disables the endpoint. When the endpoint is re-enabled by the application, the core starts processing from the descriptor that received the BNA interrupt. This bit is valid only when OTG_EN_DESC_DMA == 1'b1. It is a one-time programmable after reset bit like any other DCTL register bits. Default Value: 0x0 **0x0: DISABLED :** Core disables the endpoint after receiving BNA interrupt. When application re-enables the endpoint, core starts processing from the DOEPDMA descriptor **0x1: ENABLED :** Core disables the endpoint after receiving BNA interrupt. When application re-enables the endpoint, core starts processing from the descriptor that received the BNA interrupt.
16	NakOnBble	NAK on Babble Error (NakOnBble) Set NAK automatically on babble (NakOnBble). The core sets NAK automatically for the endpoint on which babble is received. Default Value: 0x0 **0x0: DISABLED :** Disable NAK on Babble Error **0x1: ENABLED :** NAK on Babble Error

24.1.49 USBHS_DWC_otg_intreg_DCTL (continued)

15	IgnrFrmNum	Ignore Frame Number Feature for Isochronous Endpoints (IgnrFrmNum) This field is also used to control the Periodic Transfer Interrupt (PTI) feature. Note: Do not program IgnrFrmNum bit to 1'b1 when the core is operating in threshold mode. Slave Mode (GAHBCFG.DMAEn=0): This bit is not valid in Slave mode and should not be programmed to 1. Scatter/Gather DMA Mode (GAHBCFG.DMAEn=1,DCFG.DescDMA=1): Note: When Scatter/Gather DMA mode is enabled this feature is not applicable to High Speed, High bandwidth transfers. When this bit is enabled, there must be only one packet per descriptor. - 0: The core transmits the packets only in the frame number in which they are intended to be transmitted. - 1: The core ignores the frame number, sending packets immediately as the packets are ready. In Scatter/Gather DMA mode, if this bit is enabled, the packets are not flushed when a ISOC IN token is received for an elapsed frame. Non-Scatter/Gather DMA Mode, that is, Buffer DMA Mode (GAHBCFG.DMAEn=1,DCFG.DescDMA=0): When Scatter/Gather DMA mode is disabled, this field is used by the application to enable Periodic Transfer Interrupt (PTI) Mode. The application can program Periodic Endpoint transfers for multiple (micro)Frames. - 0: Periodic Transfer Interrupt feature is disabled, application needs to program transfers for periodic endpoints every (micro)Frame - 1: Periodic Transfer Interrupt feature is enabled, application can program transfers for multiple (micro)Frames for periodic endpoints. In the PTI mode, the application will receive Transfer Complete Interrupt after transfers for multiple (micro)Frames are completed. Default Value: 0x0 **0x0: DISABLED :** :DWC_DESIGN_ID==0>Scatter/Gather DMA Mode: The core transmits the packets only in the frame number in which they are intended to be transmitted.:DWC_DESIGN_ID==0> Non-Scatter/Gather DMA Mode: Periodic Transfer Interrupt feature is disabled. **0x1: ENABLED :** :DWC_DESIGN_ID==0>Scatter/Gather DMA Mode: The core ignores the frame number, sending packets immediately as the packets are ready.:DWC_DESIGN_ID==0> Non-Scatter/Gather DMA Mode: Periodic Transfer Interrupt feature is enabled.
14 : 13	GMC	Global Multi Count (GMC) GMC must be programmed only once after initialization. Applicable only for Scatter/Gather DMA mode. This indicates the number of packets to be serviced for that end point before moving to the next end point. It is only for non-periodic endpoints. - 2'b00: Invalid. - 2'b01: 1 packet. - 2'b10: 2 packets. - 2'b11: 3 packets. The value of this field automatically changes to 2'h1 when DCFG.DescDMA is set to 1. When Scatter/Gather DMA mode is disabled, this field is reserved. and reads 2'b00. Default Value: 0x0 **0x0: NOTVALID :** Invalid **0x1: ONEPACKET :** 1 packet **0x3: THREEPACKET :** 3 packets

24.1.49 USBHS_DWC_otg_intreg_DCTL (continued)

		0x2: TWOPACKET : 2 packets
11	PWROnPrgDone	Power-On Programming Done (PWROnPrgDone) The application uses this bit to indicate that register programming is completed after a wake-up from Power Down mode. Default Value: 0x0 **0x1: DONE :** Power-On Programming Done **0x0: NOTDONE :** Power-On Programming not done
10	CGOUTNak	Clear Global OUT NAK (CGOUTNak) A write to this field clears the Global OUT NAK. Default Value: 0x0 **0x0: DISABLED :** Disable Clear Global OUT NAK **0x1: ENABLED :** Clear Global OUT NAK
9	SGOUTNak	Set Global OUT NAK (SGOUTNak) A write to this field sets the Global OUT NAK. The application uses this bit to send a NAK handshake on all OUT endpoints. The application must set the this bit only after making sure that the Global OUT NAK Effective bit in the Core Interrupt Register (GINTSTS.GOUTNakEff) is cleared. Default Value: 0x0 **0x0: DISABLED :** Disable Global OUT NAK **0x1: ENABLED :** Set Global OUT NAK
8	CGNPInNak	Clear Global Non-periodic IN NAK (CGNPInNak) A write to this field clears the Global Non-periodic IN NAK. Default Value: 0x0 **0x0: DISABLE :** Disable Global Non-periodic IN NAK **0x1: ENABLE :** Clear Global Non-periodic IN NAK

24.1.49 USBHS_DWC_otg_intreg_DCTL (continued)

7	SGNPInNak	Set Global Non-periodic IN NAK (SGNPInNak) A write to this field sets the Global Non-periodic IN NAK.The application uses this bit to send a NAK handshake on all non-periodic IN endpoints. The core can also Set this bit when a timeout condition is detected on a non-periodic endpoint in shared FIFO operation. The application must Set this bit only after making sure that the Global IN NAK Effective bit in the Core Interrupt Register (GINTSTS.GINNakEff) is cleared Default Value: 0x0 **0x0: DISABLE :** Disable Global Non-periodic IN NAK **0x1: ENABLE :** Set Global Non-periodic IN NAK
6 : 4	TstCtl	Test Control (TstCtl) - 3'b000: Test mode disabled - 3'b001: Test_J mode - 3'b010: Test_K mode - 3'b011: Test_SE0_NAK mode - 3'b100: Test_Packet mode - 3'b101: Test_Force_Enable - Others: Reserved Default Value: 0x0 **0x0: DISABLED :** Test mode disabled **0x5: TESTFE :** Test_force_Enable **0x1: TESTJ :** Test_J mode **0x2: TESTK :** Test_K mode **0x4: TESTPM :** Test_Packet mode **0x3: TESTSN :** Test_SE0_NAK mode
3	GOUTNakSts	Global OUT NAK Status (GOUTNakSts) - 1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. - 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped. Default Value: 0x0 **0x1: ACTIVE :** No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped.

24.1.49 USBHS_DWC_otg_intreg_DCTL (continued)

0x0: INACTIVE :

A handshake is sent based on the FIFO Status and the NAK and STALL bit settings.

2	GNPINNakSts	Global Non-periodic IN NAK Status (GNPINNakSts) - 1'b0: A handshake is sent out based on the data availability in the transmit FIFO. - 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO. Default Value: 0x0 **0x1: ACTIVE :** A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO. **0x0: INACTIVE :** A handshake is sent out based on the data availability in the transmit FIFO
1	SftDiscon	Soft Disconnect (SftDiscon) The application uses this bit to signal the controller to do a soft disconnect. As long as this bit is set, the host does not see that the device is connected, and the device does not receive signals on the USB. The core stays in the disconnected state until the application clears this bit. - 1'b0: Normal operation. When this bit is cleared after a soft disconnect, the core drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. When the device is reconnected, the USB host restarts device enumeration. - 1'b1: The core drives the phy_opmode_o signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host. The following is the minimum duration under various conditions for which this bit must be set for the USB host to detect a device disconnect. To accommodate clock jitter, it is recommended that the application adds some extra delay to the specified minimum duration. For high speed, if the device state is, - Suspended, the minimum duration is 1ms + 2.5us - Idle, the minimum duration is 3ms + 2.5us - Not Idle or Suspended (performing transactions), the minimum duration 125 us For full speed/low speed, if the device state is, - Suspended, the minimum duration is 1ms + 2.5us - Idle, the minimum duration is 2.5us - Not Idle or Suspended (performing transactions), the minimum duration 125 us Note: - This bit can be also used for ULPI/FS Serial interfaces. - This bit is not impacted by a soft reset. Default Value: 0x1 **0x1: DISCONNECT :** The core :DWC_DESIGN_ID!=1>drives the phy_opmode_o signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host **0x0: NODISCONNECT :** The core :DWC_DESIGN_ID!=1>drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host

24.1.49 USBHS_DWC_otg_intreg_DCTL (continued)

0	RmtWkUpSig	Remote Wakeup Signaling (RmtWkUpSig) When the application sets this bit, the core initiates remote signaling to wake up the USB host. The application must Set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1-15 ms after setting it. If LPM is enabled and the core is in the L1 (Sleep) state, when the application sets this bit, the core initiates L1 remote signaling to wake up the USB host. The application must set this bit to instruct the core to exit the Sleep state. As specified in the LPM specification, the hardware automatically clears this bit 50 microseconds (TL1DevDrvResume) after being set by the application. The application must not set this bit when GLPMCFG bRemoteWake from the previous LPM transaction is zero. Default Value: 0x0 **0x0: DISABLEDRMWKUP :** Core does not send Remote Wakeup Signaling **0x1: ENABLERMWKUP :** Core sends Remote Wakeup Signaling

24.1.50 USBHS_DWC_otg_intreg_DSTS

Description: This register indicates the status of the core with respect to USB-related events. It must be read on interrupts from Device All Interrupts (DAINT) register.

Address: 0x44900808

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R		R
HW Access	Reserved							
Name	Reserved [7:4]				ErrticErr	EnumSpd [2:1]		SuspSts

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	SOFFN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R		R					
HW Access								
Name	DevLnSts [23:22]		SOFFN [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 22	DevLnSts	Device Line Status (DevLnSts) Indicates the current logic level USB data lines - DevLnSts[1]: Logic level of D+ - DevLnSts[0]: Logic level of D- Default Value: 0x0
21 : 8	SOFFN	Frame or Microframe Number of the Received SOF (SOFFN) When the core is operating at high speed, this field contains a microframe number. When the core is operating at full or low speed, this field contains a Frame number. Note: This register may return a non-zero value if read immediately after power-on reset. In case the register bit reads non-zero immediately after power-on reset, it does not indicate that SOF has been received from the host. The read value of this interrupt is valid only after a valid connection between host and device is established. Default Value: 0x0
3	ErrticErr	Erratic Error (ErrticErr) The core sets this bit to report any erratic errors (phy_rxvalid_i/phy_rxvldh_i or phy_rxactive_i is asserted for at least 2 ms, due to PHY error) seen on the UTMI+. Due to erratic errors, the core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register (GINTSTS.ErlySusp). If the early suspend is asserted due to an erratic error, the application can only perform a soft disconnect recover. Default Value: 0x0

24.1.50 USBHS_DWC_otg_intreg_DSTS (continued)

		0x1: ACTIVE : Erratic Error **0x0: INACTIVE :** No Erratic Error
2 : 1	EnumSpd	Enumerated Speed (EnumSpd) Indicates the speed at which the controller has come up after speed detection through a connect or reset sequence. - 2'b00: High speed (PHY clock is running at 30 or 60 MHz) - 2'b01: Full speed (PHY clock is running at 30 or 60 MHz) - 2'b10: Low speed (PHY clock is running at 6 MHz) - 2'b11: Full speed (PHY clock is running at 48 MHz) Low speed is not supported for devices using a UTMI+ PHY. Default Value: 0x1 **0x1: FS3060 :** Full speed (PHY clock is running at 30 or 60 MHz) **0x3: FS48 :** Full speed (PHY clock is running at 48 MHz) **0x0: HS3060 :** High speed (PHY clock is running at 30 or 60 MHz) **0x2: LS6 :** Low speed (PHY clock is running at 6 MHz)
0	SuspSts	Suspend Status (SuspSts) In Device mode, this bit is set as long as a Suspend condition is detected on the USB. The core enters the Suspend state when there is no activity on the phy_line_state_i signal for an extended period of time. The core comes out of the suspend under the following conditions : - If there is any activity on the phy_line_state_i signal, or - If the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig). When the core comes out of the suspend, this bit is set to 1'b0. Default Value: 0x0 **0x1: ACTIVE :** Suspend state **0x0: INACTIVE :** No suspend state

24.1.51 USBHS_DWC_otg_intreg_DIEPMSK

Description: This register works with each of the Device IN Endpoint Interrupt (DIEPINTn) registers for all endpoints to generate an interrupt per IN endpoint. The IN endpoint interrupt for a specific status in the DIEPINTn register can be masked by writing to the corresponding bit in this register. Status bits are masked by default.

Address: 0x44900810

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	INEPNakEf-fMsk	INTknEP-MisMsk	INTknTX-FEmpMsk	Time-OUTMsk	AHBErrMsk	EPDis-bldMsk	XferCom-plMsk

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW	Reserved			RW	RW
HW Access	Reserved			Reserved				
Name	Reserved [15:14]		NAKMsk	Reserved [12:10]			BNAInIn-trMsk	TxfifoUnd-rnMsk

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
13	NAKMsk	NAK interrupt Mask (NAKMsk) Default Value: 0x0 **0x0: MASK :** Mask NAK Interrupt **0x1: NOMASK :** No Mask NAK Interrupt
9	BNAInIntrMsk	BNA interrupt Mask (BNAInIntrMsk) Default Value: 0x0 **0x0: MASK :** Mask BNA Interrupt **0x1: NOMASK :** No BNA Interrupt Mask

24.1.51 USBHS_DWC_otg_intreg_DIEPMSK (continued)

8	TxfifoUndrnMsk	Fifo Underrun Mask (TxfifoUndrnMsk) Default Value: 0x0 **0x0: MASK :** Mask Fifo Underrun Interrupt **0x1: NOMASK :** No Fifo Underrun Interrupt Mask
6	INEPNakEffMsk	IN Endpoint NAK Effective Mask (INEPNakEffMsk) Default Value: 0x0 **0x0: MASK :** Mask IN Endpoint NAK Effective Interrupt **0x1: NOMASK :** No IN Endpoint NAK Effective Interrupt Mask
5	INTknEPMisMsk	IN Token received with EP Mismatch Mask (INTknEPMisMsk) Default Value: 0x0 **0x0: MASK :** Mask IN Token received with EP Mismatch Interrupt **0x1: NOMASK :** No Mask IN Token received with EP Mismatch Interrupt
4	INTknTXFEmpMsk	IN Token Received When TxFIFO Empty Mask (INTknTXFEmpMsk) Default Value: 0x0 **0x0: MASK :** Mask IN Token Received When TxFIFO Empty Interrupt **0x1: NOMASK :** No IN Token Received When TxFIFO Empty Interrupt
3	TimeOUTMsk	Timeout Condition Mask (TimeOUTMsk) (Non-isochronous endpoints) Default Value: 0x0 **0x0: MASK :** Mask Timeout Condition Interrupt **0x1: NOMASK :** No Timeout Condition Interrupt Mask
2	AHBErrMsk	AHB Error Mask (AHBErrMsk) Default Value: 0x0 **0x0: MASK :** Mask AHB Error Interrupt

24.1.51 USBHS_DWC_otg_intreg_DIEPMSK (continued)

		0x1: NOMASK : No AHB Error Interrupt Mask
1	EPDisbldMsk	Endpoint Disabled Interrupt Mask (EPDisbldMsk) Default Value: 0x0 **0x0: MASK :** Mask Endpoint Disabled Interrupt **0x1: NOMASK :** No Endpoint Disabled Interrupt Mask
0	XferComplMsk	Transfer Completed Interrupt Mask (XferComplMsk) Default Value: 0x0 **0x0: MASK :** Mask Transfer Completed Interrupt **0x1: NOMASK :** No Transfer Completed Interrupt Mask

24.1.52 USBHS_DWC_otg_intreg_DOEPMSK

Description: This register works with each of the Device OUT Endpoint Interrupt (DOEPINTn) registers for all endpoints to generate an interrupt per OUT endpoint. The OUT endpoint interrupt for a specific status in the DOEPINTn register can be masked by writing into the corresponding bit in this register. Status bits are masked by default.

Address: 0x44900814

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	Back2Back-SETup	StsPhseRc-vdMsk	OUTTknEP-disMsk	SetUPMsk	AHBErrMsk	EPDis-bldMsk	XferCom-plMsk

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	Reserved		RW	RW
HW Access	Reserved				Reserved			
Name	Reserved	NYETMsk	NAKMsk	BbleErrMsk	Reserved [11:10]		BnaOutIn-trMsk	OutPktEr-rMsk

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	NYETMsk	NYET interrupt Mask (NYETMsk) Default Value: 0x0 **0x0: MASK :** Mask NYET Interrupt **0x1: NOMASK :** No NYET Interrupt Mask
13	NAKMsk	NAK interrupt Mask (NAKMsk) Default Value: 0x0 **0x0: MASK :** Mask NAK Interrupt **0x1: NOMASK :** No NAK Interrupt Mask

24.1.52 USBHS_DWC_otg_intreg_DOEPMSK (continued)

12	BbleErrMsk	Babble Error interrupt Mask (BbleErrMsk) Default Value: 0x0 **0x0: MASK :** Mask Babble Error Interrupt **0x1: NOMASK :** No Babble Error Interrupt Mask
9	BnaOutIntrMsk	BNA interrupt Mask (BnaOutIntrMsk) Default Value: 0x0 **0x0: MASK :** Mask BNA Interrupt **0x1: NOMASK :** No BNA Interrupt Mask
8	OutPktErrMsk	OUT Packet Error Mask (OutPktErrMsk) Default Value: 0x0 **0x0: MASK :** Mask OUT Packet Error Interrupt **0x1: NOMASK :** No OUT Packet Error Interrupt Mask
6	Back2BackSETup	Back-to-Back SETUP Packets Received Mask (Back2BackSETup) Applies to control OUT endpoints only. Default Value: 0x0 **0x0: MASK :** Mask Back-to-Back SETUP Packets Received Interrupt **0x1: NOMASK :** No Back-to-Back SETUP Packets Received Interrupt Mask
5	StsPhseRcvdMsk	Status Phase Received Mask (StsPhseRcvdMsk) Applies to control OUT endpoints only. Default Value: 0x0 **0x0: MASK :** Status Phase Received Mask **0x1: NOMASK :** No Status Phase Received Mask
4	OUTTknEPdisMsk	OUT Token Received when Endpoint Disabled Mask (OUTTknEPdisMsk) Applies to control OUT endpoints only. Default Value: 0x0

24.1.52 USBHS_DWC_otg_intreg_DOEPMSK (continued)

		0x0: MASK : Mask OUT Token Received when Endpoint Disabled Interrupt **0x1: NOMASK :** No OUT Token Received when Endpoint Disabled Interrupt Mask
3	SetUPMsk	SETUP Phase Done Mask (SetUPMsk) Applies to control endpoints only. Default Value: 0x0 **0x0: MASK :** Mask SETUP Phase Done Interrupt **0x1: NOMASK :** No SETUP Phase Done Interrupt Mask
2	AHBErrMsk	AHB Error (AHBErrMsk) Default Value: 0x0 **0x0: MASK :** Mask AHB Error Interrupt **0x1: NOMASK :** No AHB Error Interrupt Mask
1	EPDisbldMsk	Endpoint Disabled Interrupt Mask (EPDisbldMsk) Default Value: 0x0 **0x0: MASK :** Mask Endpoint Disabled Interrupt **0x1: NOMASK :** No Endpoint Disabled Interrupt Mask
0	XferComplMsk	Transfer Completed Interrupt Mask (XferComplMsk) Default Value: 0x0 **0x0: MASK :** Mask Transfer Completed Interrupt **0x1: NOMASK :** No Transfer Completed Interrupt Mask

24.1.53 USBHS_DWC_otg_intreg_DAINT

Description: When a significant event occurs on an endpoint, a Device All Endpoints Interrupt register interrupts the application using the Device OUT Endpoints Interrupt bit or Device IN Endpoints Interrupt bit of the Core Interrupt register (GINTSTS.OEPInt or GINTSTS.IEPInt, respectively). This is shown in Figure 5-2. There is one interrupt bit per endpoint, up to a maximum of 16 bits for OUT endpoints and 16 bits for IN endpoints. For a bidirectional endpoint, the corresponding IN and OUT interrupt bits are used. Bits in this register are set and cleared when the application sets and clears bits in the corresponding Device Endpoint-n Interrupt register (DIEPINTn/DOEPINTn).

Address: 0x44900818

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access								
Name	InEpInt7	InEpInt6	InEpInt5	InEpInt4	InEpInt3	InEpInt2	InEpInt1	InEpInt0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							
Name	Reserved [15:9]							InEpInt8

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access								
Name	OutEPInt7	OutEPInt6	OutEPInt5	OutEPInt4	OutEPInt3	OutEPInt2	OutEPInt1	OutEPInt0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							
Name	Reserved [31:25]							OutEPInt8

Bits	Name	Description
24	OutEPInt8	OUT Endpoint 8 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the OUT EP **0x0: INACTIVE :** No Interrupt
23	OutEPInt7	OUT Endpoint 7 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the OUT EP **0x0: INACTIVE :** No Interrupt

24.1.53 USBHS_DWC_otg_intreg_DAINT (continued)

22	OutEPInt6	OUT Endpoint 6 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the OUT EP **0x0: INACTIVE :** No Interrupt
21	OutEPInt5	OUT Endpoint 5 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the OUT EP **0x0: INACTIVE :** No Interrupt
20	OutEPInt4	OUT Endpoint 4 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the OUT EP **0x0: INACTIVE :** No Interrupt
19	OutEPInt3	OUT Endpoint 3 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the OUT EP **0x0: INACTIVE :** No Interrupt
18	OutEPInt2	OUT Endpoint 2 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the OUT EP **0x0: INACTIVE :** No Interrupt
17	OutEPInt1	OUT Endpoint 1 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the OUT EP

24.1.53 USBHS_DWC_otg_intreg_DAINT (continued)

		0x0: INACTIVE : No Interrupt
16	OutEPInt0	OUT Endpoint 0 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for OUT EP0 **0x0: INACTIVE :** No Interrupt
8	InEpInt8	IN Endpoint 8 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the IN EP **0x0: INACTIVE :** No Interrupt
7	InEpInt7	IN Endpoint 7 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the IN EP **0x0: INACTIVE :** No Interrupt
6	InEpInt6	IN Endpoint 6 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the IN EP **0x0: INACTIVE :** No Interrupt
5	InEpInt5	IN Endpoint 5 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the IN EP **0x0: INACTIVE :** No Interrupt
4	InEpInt4	IN Endpoint 4 Interrupt Bit Default Value: 0x0

24.1.53 USBHS_DWC_otg_intreg_DAINT (continued)

		0x1: ACTIVE : Interrupt is active for the IN EP **0x0: INACTIVE :** No Interrupt
3	InEpInt3	IN Endpoint 3 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the IN EP **0x0: INACTIVE :** No Interrupt
2	InEpInt2	IN Endpoint 2 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the IN EP **0x0: INACTIVE :** No Interrupt
1	InEpInt1	IN Endpoint 1 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for the IN EP **0x0: INACTIVE :** No Interrupt
0	InEpInt0	IN Endpoint 0 Interrupt Bit Default Value: 0x0 **0x1: ACTIVE :** Interrupt is active for IN EP0 **0x0: INACTIVE :** No Interrupt

24.1.54 USBHS_DWC_otg_intreg_DAINTMSK

Description: The Device Endpoint Interrupt Mask register works with the Device Endpoint Interrupt register to interrupt the application when an event occurs on a device endpoint. However, the Device All Endpoints Interrupt (DAINT) register bit corresponding to that interrupt is still set.

Address: 0x4490081C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	InEpMsk7	InEpMsk6	InEpMsk5	InEpMsk4	InEpMsk3	InEpMsk2	InEpMsk1	InEpMsk0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							
Name	Reserved [15:9]							InEpMsk8

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	OutEPMsk7	OutEPMsk6	OutEPMsk5	OutEPMsk4	OutEPMsk3	OutEPMsk2	OutEPMsk1	OutEPMsk0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							RW
HW Access	Reserved							
Name	Reserved [31:25]							OutEPMsk8

Bits	Name	Description
24	OutEPMsk8	OUT Endpoint 8 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask OUT Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
23	OutEPMsk7	OUT Endpoint 7 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask OUT Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
22	OutEPMsk6	OUT Endpoint 6 Interrupt mask Bit Default Value: 0x0

24.1.54 USBHS_DWC_otg_intreg_DAINTMSK (continued)

		0x0: MASK : Mask OUT Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
21	OutEPMsk5	OUT Endpoint 5 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask OUT Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
20	OutEPMsk4	OUT Endpoint 4 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask OUT Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
19	OutEPMsk3	OUT Endpoint 3 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask OUT Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
18	OutEPMsk2	OUT Endpoint 2 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask OUT Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
17	OutEPMsk1	OUT Endpoint 1 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask OUT Endpoint Interrupt

24.1.54 USBHS_DWC_otg_intreg_DAINTMSK (continued)

		0x1: NOMASK : No Interrupt mask
16	OutEPMsk0	OUT Endpoint 0 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask OUT Endpoint 0 Interrupt **0x1: NOMASK :** No Interrupt mask
8	InEpMsk8	IN Endpoint 8 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask IN Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
7	InEpMsk7	IN Endpoint 7 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask IN Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
6	InEpMsk6	IN Endpoint 6 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask IN Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
5	InEpMsk5	IN Endpoint 5 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask IN Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
4	InEpMsk4	IN Endpoint 4 Interrupt mask Bit Default Value: 0x0

24.1.54 USBHS_DWC_otg_intreg_DAINTMSK (continued)

		0x0: MASK : Mask IN Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
3	InEpMsk3	IN Endpoint 3 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask IN Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
2	InEpMsk2	IN Endpoint 2 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask IN Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
1	InEpMsk1	IN Endpoint 1 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask IN Endpoint Interrupt **0x1: NOMASK :** No Interrupt mask
0	InEpMsk0	IN Endpoint 0 Interrupt mask Bit Default Value: 0x0 **0x0: MASK :** Mask IN Endpoint 0 Interrupt **0x1: NOMASK :** No Interrupt mask

24.1.55 USBHS_DWC_otg_intreg_DVBUSDIS

Description: This register specifies the VBUS discharge time after VBUS pulsing during SRP.

Address: 0x44900828

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DVBUSDis [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DVBUSDis [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	DVBUSDis	Device VBUS Discharge Time (DVBUSDis) Specifies the VBUS discharge time after VBUS pulsing during SRP. This value equals (VBUS discharge time in PHY clocks) / 1, 024. The value you use depends whether the PHY is operating at 30MHz (16-bit data width) or 60 MHz (8-bit data width). Depending on your VBUS load, this value can need adjustment. Default Value: 0x17D7

24.1.56 USBHS_DWC_otg_intreg_DVBUSPULSE

Description: This register contains the VBUS pulsing time during SRP.

Address: 0x4490082C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DVBUSPulse [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved							
Name	Reserved [15:12]				DVBUSPulse [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11 : 0	DVBUSPulse	Device VBUS Pulsing Time (DVBUSPulse) Specifies the VBUS pulsing time during SRP. This value equals (VBUS pulsing time in PHY clocks) / 1, 024 The value you use depends whether the PHY is operating at 30MHz (16-bit data width) or 60 MHz (8-bit data width). Default Value: 0x5B8

24.1.57 USBHS_DWC_otg_intreg_DTHRCTL

Description: This register contains the Receive and Transmit Threshold characteristics of the Device controller.

Address: 0x44900830

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						RW	RW
HW Access								
Name	TxThrLen [7:2]						ISOThrEn	NonISO-ThrEn

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW		RW		
HW Access	Reserved							
Name	Reserved [15:13]			AHBThrRatio [12:11]		TxThrLen [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							RW
HW Access								
Name	RxThrLen [23:17]							RxThrEn

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW	Reserved	RW	
HW Access	Reserved					Reserved		
Name	Reserved [31:28]				ArbPrkEn	Reserved	RxThrLen [25:24]	

Bits	Name	Description
27	ArbPrkEn	Arbiter Parking Enable (ArbPrkEn) This bit controls internal DMA arbiter parking for IN endpoints. If thresholding is enabled and this bit is set to one, then the arbiter parks on the IN endpoint for which there is a token received on the USB. This is done to avoid getting into underrun conditions. By default, arbiter parking is enabled. Default Value: 0x1 **0x0: DISABLED :** Disable DMA arbiter parking **0x1: ENABLED :** Enable DMA arbiter parking for IN endpoints
25 : 17	RxThrLen	Receive Threshold Length (RxThrLen) This field specifies Receive thresholding size in DWORDS. This field also specifies the amount of data received on the USB before the core can start transmitting on the AHB. The threshold length has to be at least eight DWORDS. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen). Default Value: 0x8

24.1.57 USBHS_DWC_otg_intreg_DTHRCTL (continued)

16	RxThrEn	Receive Threshold Enable (RxThrEn) When this bit is set, the core enables thresholding in the receive direction. Note: We recommends that you do not enable RxThrEn, because it may cause issues in the Rx-FIFO especially during error conditions such as RxError and Babble. Default Value: 0x0 **0x0: DISABLED :** Disable thresholding **0x1: ENABLED :** Enable thresholding in the receive direction
12 : 11	AHBThrRatio	AHB Threshold Ratio (AHBThrRatio) These bits define the ratio between the AHB threshold and the MAC threshold for the transmit path only. The AHB threshold always remains less than or equal to the USB threshold, because this does not increase overhead. Both the AHB and the MAC threshold must be DWORD-aligned. The application needs to program TxThrLen and the AHBThrRatio to make the AHB Threshold value DWORD aligned. If the AHB threshold value is not DWORD aligned, the core might not behave correctly. When programming the TxThrLen and AHBThrRatio, the application must ensure that the minimum AHB threshold value does not go below 8 DWORDS to meet the USB turnaround time requirements. - 2'b00: AHB threshold = MAC threshold - 2'b01: AHB threshold = MAC threshold / 2 - 2'b10: AHB threshold = MAC threshold / 4 - 2'b11: AHB threshold = MAC threshold / 8 Default Value: 0x0 **0x1: THRESONE :** AHB threshold = MAC threshold /2 **0x3: THRESTHREE :** AHB threshold = MAC threshold /8 **0x2: THRESTWO :** AHB threshold = MAC threshold /4 **0x0: THRESZERO :** AHB threshold = MAC threshold
10 : 2	TxThrLen	Transmit Threshold Length (TxThrLen) This field specifies Transmit thresholding size in DWORDS. This also forms the MAC threshold and specifies the amount of data in bytes to be in the corresponding endpoint transmit FIFO, before the core can start transmit on the USB. The threshold length has to be at least eight DWORDS when the value of AHBThrRatio is 2'h00. In case the AHBThrRatio is non zero the application needs to ensure that the AHB Threshold value does not go below the recommended eight DWORD. This field controls both isochronous and non-isochronous IN endpoint thresholds. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen). Note: - When OTG_ARCHITECTURE=0, the reset value of this register field is 0. - When OTG_ARCHITECTURE=2, the reset value of this register field is 8. Default Value: 0x8

24.1.57 USBHS_DWC_otg_intreg_DTHRCTL (continued)

1	ISOThrEn	ISO IN Endpoints Threshold Enable. (ISOThrEn) When this bit is Set, the core enables thresholding for isochronous IN endpoints. Default Value: 0x0 **0x0: DISABLED :** No thresholding **0x1: ENABLED :** Enables thresholding for isochronous IN endpoints
0	NonISOThrEn	Non-ISO IN Endpoints Threshold Enable. (NonISOThrEn) When this bit is Set, the core enables thresholding for Non Isochronous IN endpoints. Default Value: 0x0 **0x0: DISABLED :** No thresholding **0x1: ENABLED :** Enable thresholding for non-isochronous IN endpoints

24.1.58 USBHS_DWC_otg_intreg_DIEPEMPMSK

Description: This register is valid only in Dedicated FIFO operation (OTG_EN_DED_TX_FIFO = 1). This register is used to control the IN endpoint FIFO empty interrupt generation (DIEPINTn.TxfEmp).

Address: 0x44900834

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	InEpTxfEmpMsk [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	InEpTxfEmpMsk [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	InEpTxfEmpMsk	IN EP Tx FIFO Empty Interrupt Mask Bits (InEpTxfEmpMsk) These bits acts as mask bits for DIEPINTn.TxFEmp interrupt, one bit per IN Endpoint: Bit 0 for IN EP 0, bit 15 for IN EP 15 Default Value: 0x0 **0x1: EP0_MASK :** Mask IN EP0 Tx FIFO Empty Interrupt **0x400: EP10_MASK :** Mask IN EP10 Tx FIFO Empty Interrupt **0x800: EP11_MASK :** Mask IN EP11 Tx FIFO Empty Interrupt **0x1000: EP12_MASK :** Mask IN EP12 Tx FIFO Empty Interrupt **0x2000: EP13_MASK :** Mask IN EP13 Tx FIFO Empty Interrupt

24.1.58 USBHS_DWC_otg_intreg_DIEPEMPMSK (continued)

0x4000: EP14_MASK :

Mask IN EP14 Tx FIFO Empty Interrupt

0x8000: EP15_MASK :

Mask IN EP15 Tx FIFO Empty Interrupt

0x2: EP1_MASK :

Mask IN EP1 Tx FIFO Empty Interrupt

0x4: EP2_MASK :

Mask IN EP2 Tx FIFO Empty Interrupt

0x8: EP3_MASK :

Mask IN EP3 Tx FIFO Empty Interrupt

0x10: EP4_MASK :

Mask IN EP4 Tx FIFO Empty Interrupt

0x20: EP5_MASK :

Mask IN EP5 Tx FIFO Empty Interrupt

0x40: EP6_MASK :

Mask IN EP6 Tx FIFO Empty Interrupt

0x80: EP7_MASK :

Mask IN EP7 Tx FIFO Empty Interrupt

0x100: EP8_MASK :

Mask IN EP8 Tx FIFO Empty Interrupt

0x200: EP9_MASK :

Mask IN EP9 Tx FIFO Empty Interrupt

24.1.59 USBHS_DWC_otg_intreg_DIEPCTL0

Description: This register is used to control the characteristics of the IN Endpoint 0 of the Device controller.

Address: 0x44900900

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved							
Name	Reserved [7:2]						MPS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R	Reserved						
HW Access		Reserved						
Name	USBActEP	Reserved [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	Reserved	R		R	Reserved
HW Access				Reserved				Reserved
Name	TxFNum [23:22]		Stall	Reserved	EPType [19:18]		NAKSts	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved		W	W	RW	
HW Access			Reserved					
Name	EPEna	EPDis	Reserved [29:28]		SNAK	CNAK	TxFNum [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) When Scatter/Gather DMA mode is enabled for IN endpoints, this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. When Scatter/Gather DMA mode is disabled (such as in buffer pointer based DMA mode) this bit indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting the following interrupts on this endpoint: - Endpoint Disabled - Transfer Completed Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No action
30	EPDis	Endpoint Disable (EPDis) The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must Set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0

24.1.59 USBHS_DWC_otg_intreg_DIEPCTL0 (continued)

		0x1: ACTIVE : Disabled Endpoint **0x0: INACTIVE :** No action
27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x0: NOSET :** No action **0x1: SET :** Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: CLEAR :** Clear NAK **0x0: NOCLEAR :** No action
25 : 22	TxFNum	TxFIFO Number (TxFNum) - For Shared FIFO operation, this value is always set to 0, indicating that control IN endpoint 0 data is always written in the Non-Periodic Transmit FIFO. - For Dedicated FIFO operation, this value is set to the FIFO number that is assigned to IN Endpoint. Default Value: 0x0 **0x0: TXFIFO0 :** Tx FIFO 0 **0x1: TXFIFO1 :** Tx FIFO 1 **0xa: TXFIFO10 :** Tx FIFO 10 **0xb: TXFIFO11 :** Tx FIFO 11

24.1.59 USBHS_DWC_otg_intreg_DIEPCTL0 (continued)

0xc: TXFIFO12 :

Tx FIFO 12

0xd: TXFIFO13 :

Tx FIFO 13

0xe: TXFIFO14 :

Tx FIFO 14

0xf: TXFIFO15 :

Tx FIFO 15

0x2: TXFIFO2 :

Tx FIFO 2

0x3: TXFIFO3 :

Tx FIFO 3

0x4: TXFIFO4 :

Tx FIFO 4

0x5: TXFIFO5 :

Tx FIFO 5

0x6: TXFIFO6 :

Tx FIFO 6

0x7: TXFIFO7 :

Tx FIFO 7

0x8: TXFIFO8 :

Tx FIFO 8

0x9: TXFIFO9 :

Tx FIFO 9

21	Stall	STALL Handshake (Stall) The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Nonperiodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Default Value: 0x0 **0x1: ACTIVE :** Stall Handshake

24.1.59 USBHS_DWC_otg_intreg_DIEPCTL0 (continued)

		0x0: INACTIVE : No Stall
19 : 18	EPType	Endpoint Type (EPType) Hardcoded to 00 for control. Default Value: 0x0 **0x0: ACTIVE :** Endpoint Control 0
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status - 1'b1: The core is transmitting NAK handshakes on this endpoint. When this bit is set, either by the application or core, the core stops transmitting data, even If there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** The core is transmitting NAK handshakes on this endpoint **0x0: INACTIVE :** The core is transmitting non-NAK handshakes based on the FIFO status
15	USBActEP	USB Active Endpoint (USBActEP) This bit is always SET to 1, indicating that control endpoint 0 is always active in all configurations and interfaces. Default Value: 0x1 **0x1: ACTIVE0 :** Control endpoint is always active
1 : 0	MPS	Maximum Packet Size (MPS) Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical end-point. - 2'b00: 64 bytes - 2'b01: 32 bytes - 2'b10: 16 bytes - 2'b11: 8 bytes Default Value: 0x0 **0x2: BYTES16 :** 16 bytes **0x1: BYTES32 :** 32 bytes **0x0: BYTES64 :** 64 bytes

24.1.59 USBHS_DWC_otg_intreg_DIEPCTL0 (continued)

0x3: BYTES8 :

8 bytes

24.1.60 USBHS_DWC_otg_intreg_DIEPINT0

Description: This register indicates the status of an endpoint with respect to USB- and AHB-related events. It is shown in the "Interrupt Hierarchy" figure in the databook. The application must read this register when the OUT Endpoints Interrupt bit or IN Endpoints Interrupt bit of the Core Interrupt register (GINTSTS.OEPInt or GINTSTS.IEPInt, respectively) is set. Before the application can read this register, it must first read the Device All Endpoints Interrupt (DAINT) register to get the exact endpoint number for the Device Endpoint-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the DAINT and GINTSTS registers

Address: 0x44900908

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	TxFEmp	INEPNakEff	INTknEP-Mis	INTknTX-FEmp	TimeOUT	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	Reserved	RW	RW
HW Access	Reserved					Reserved		
Name	Reserved	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. : 0x0 **0x1: ACTIVE :** NAK Interrupt

24.1.60 USBHS_DWC_otg_intreg_DIEPINT0 (continued)

		0x0: INACTIVE : No interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Default Value: 0x0 **0x1: ACTIVE :** BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	TxfifoUndrn	Fifo Underrun (TxfifoUndrn) Applies to IN endpoints only. The core generates this interrupt when it detects a transmit FIFO underrun condition in threshold mode for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Fifo Underrun interrupt **0x0: INACTIVE :** No Fifo Underrun interrupt

24.1.60 USBHS_DWC_otg_intreg_DIEPINT0 (continued)

7	TxFEmp	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN Endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)). Default Value: 0x1 **0x1: ACTIVE :** Transmit FIFO Empty interrupt **0x0: INACTIVE :** No Transmit FIFO Empty interrupt
6	INEPNakEff	IN Endpoint NAK Effective (INEPNakEff) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCT-Ln.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. Default Value: 0x0 **0x1: ACTIVE :** IN Endpoint NAK Effective interrupt **0x0: INACTIVE :** No IN Endpoint NAK Effective interrupt
5	INTknEPMis	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received with EP Mismatch interrupt **0x0: INACTIVE :** No IN Token Received with EP Mismatch interrupt
4	INTknTXFEmp	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received when TxFIFO Empty Interrupt

24.1.60 USBHS_DWC_otg_intreg_DIEPINT0 (continued)

		0x0: INACTIVE : No IN Token Received when TxFIFO Empty interrupt
3	TimeOUT	Timeout Condition (TimeOUT) - In shared TX FIFO mode, applies to non-isochronous IN endpoints only. - In dedicated FIFO mode, applies only to Control IN endpoints. - In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Timeout interrupt **0x0: INACTIVE :** No Timeout interrupt
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt
0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0

24.1.60 USBHS_DWC_otg_intreg_DIEPINT0 (continued)

0x1: ACTIVE :

Transfer Completed Interrupt

0x0: INACTIVE :

No Transfer Complete Interrupt

24.1.61 USBHS_DWC_otg_intreg_DIEPTSIZ0

Description: The application must modify this register before enabling endpoint 0. Once endpoint 0 is enabled using Endpoint Enable bit of the Device Control Endpoint 0 Control registers (DIEPCTL0.EPEna/DOEPCTL0.EPEna), the core modifies this register. The application can only read this register once the core has cleared the Endpoint Enable bit. Nonzero endpoints use the registers for endpoints 115. When Scatter/Gather DMA mode is enabled, this register must not be programmed by the application. If the application reads this register when Scatter/Gather DMA mode is enabled, the core returns all zeros.

Address: 0x44900910

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved							
Name	Reserved	XferSize [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW		Reserved		
HW Access	Reserved					Reserved		
Name	Reserved [23:21]			PktCnt [20:19]		Reserved [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20 : 19	PktCnt	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. - IN Endpoints : This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. - OUT Endpoints: This field is decremented every time a packet (maximum size or short packet) is written to the RxFIFO. Default Value: 0x0
6 : 0	XferSize	Transfer Size (XferSize) This field contains the transfer size in bytes for the current endpoint. The transfer size (XferSize) = Sum of buffer sizes across all descriptors in the list for the endpoint. In Buffer DMA, the core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. - IN Endpoints: The core decrements this field every time a packet from the external memory is written to the TxFIFO. - OUT Endpoints: The core decrements this field every time a packet is read from the RxFIFO and written to the external memory. Default Value: 0x0

24.1.62 USBHS_DWC_otg_intreg_DIEPDMA0

Description: This register contains the DMA Address for the IN Endpoint 0 of the Device controller.

Address: 0x44900914

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	DMAAddr This field holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.63 USBHS_DWC_otg_intreg_DTXFSTS0

Description: This register contains information about the IN Endpoint Transmit FIFO of the Device controller.

Address: 0x44900918

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	INEPTxFSpcAvail	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. - 16'h0: Endpoint TxFIFO is full - 16'h1: 1 word available - 16'h2: 2 words available - 16'hn: n words available (where 0 n 32,768) - 16'h8000: 32,768 words available - Others: Reserved In DRD configurations (OTG_MODE = 0, 1, or 2) with dynamic FIFO sizing feature enabled (OTG_DFIFO_DYNAMIC = 1), the value of this field is, - the maximum value of (OTG_TX_HNPERIO_DFIFO_DEPTH, OTG_TX_DINEP_DFIFO_DEPTH_0) during reset, and - OTG_TX_DINEP_DFIFO_DEPTH_0, immediately after reset deassertion Default Value: 0x100

24.1.64 USBHS_DWC_otg_intreg_DIEPDMAB0

Description: This register contains the DMA Buffer Address for the IN Endpoint 0 of the Device controller.

Address: 0x4490091C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.65 USBHS_DWC_otg_intreg_DIEPCTL1

Description: This register is used to control the characteristics of Endpoint 1. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900920

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	Reserved	RW		R	R
HW Access				Reserved				
Name	TxFNum [23:22]		Stall	Reserved	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	RW	
HW Access								
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled, -- For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. -- For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. - When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: -- For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. -- For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: -- SETUP Phase Done -- Endpoint Disabled -- Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.65 USBHS_DWC_otg_intreg_DIEPCTL1 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	SetD1PID - Set DATA1 PID (SetD1PID) -- Applies to interrupt and bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. -- This field is applicable both for Scatter-Gather DMA mode and non Scatter-Gather DMA mode. - Set odd (micro)Frame (SetOddFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the even and odd (micro)Frame (EO_FrNum) field to odd (micro)Frame. -- This field is not applicable for Scatter-Gather DMA mode. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID **0x1: ENABLED :** Enables Set DATA1 PID
28	SetD0PID	SetD0PID - Set DATA0 PID (SetD0PID) -- Applies to interrupt/bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. -- This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)Frame (SetEvenFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the Even/Odd (micro)Frame (EO_FrNum) field to even (micro)Frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID **0x1: ENABLED :** Endpoint Data PID to DATA0)

24.1.65 USBHS_DWC_otg_intreg_DIEPCTL1 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
25 : 22	TxFNum	TxFIFO Number (TxFNum) Shared FIFO Operation non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. - 4'h0: Non-Periodic TxFIFO - Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: These bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints. Default Value: 0x0 **0x0: TXFIFO0 :** Tx FIFO 0 **0x1: TXFIFO1 :** Tx FIFO 1 **0xa: TXFIFO10 :** Tx FIFO 10 **0xb: TXFIFO11 :** Tx FIFO 11 **0xc: TXFIFO12 :** Tx FIFO 12

24.1.65 USBHS_DWC_otg_intreg_DIEPCTL1 (continued)

		0xd: TXFIFO13 : Tx FIFO 13 **0xe: TXFIFO14 :** Tx FIFO 14 **0xf: TXFIFO15 :** Tx FIFO 15 **0x2: TXFIFO2 :** Tx FIFO 2 **0x3: TXFIFO3 :** Tx FIFO 3 **0x4: TXFIFO4 :** Tx FIFO 4 **0x5: TXFIFO5 :** Tx FIFO 5 **0x6: TXFIFO6 :** Tx FIFO 6 **0x7: TXFIFO7 :** Tx FIFO 7 **0x8: TXFIFO8 :** Tx FIFO 8 **0x9: TXFIFO9 :** Tx FIFO 9
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

24.1.65 USBHS_DWC_otg_intreg_DIEPCTL1 (continued)

		0x1: ACTIVE : STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUP :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.65 USBHS_DWC_otg_intreg_DIEPCTL1 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. - 1'b0: Even (micro)frame - 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Default Value: 0x0 **0x0: DATA0EVENFRM :** DATA0 or Even Frame **0x1: DATA1ODDFRM :** DATA1 or Odd Frame
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical end-point. This value is in bytes. Default Value: 0x0

24.1.66 USBHS_DWC_otg_intreg_DIEPINT1

Description: This register contains the interrupts for the IN Endpoint 1 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900928

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	TxFEmp	INEPNakEff	INTknEP-Mis	INTknTX-FEmp	TimeOUT	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	Reserved	RW	RW
HW Access	Reserved					Reserved		
Name	Reserved	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt

24.1.66 USBHS_DWC_otg_intreg_DIEPINT1 (continued)

		0x0: INACTIVE : No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Default Value: 0x0 **0x1: ACTIVE :** BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	TxfifoUndrn	Fifo Underrun (TxfifoUndrn) Applies to IN endpoints Only This bit is valid only If thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** TxFIFO Underrun interrupt **0x0: INACTIVE :** No Tx FIFO Underrun interrupt

24.1.66 USBHS_DWC_otg_intreg_DIEPINT1 (continued)

7	TxFEmp	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)). Default Value: 0x1 **0x1: ACTIVE :** Transmit FIFO Empty interrupt **0x0: INACTIVE :** No Transmit FIFO Empty interrupt
6	INEPNakEff	IN Endpoint NAK Effective (INEPNakEff) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCT-Ln.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. Default Value: 0x0 **0x1: ACTIVE :** IN Endpoint NAK Effective interrupt **0x0: INACTIVE :** No Endpoint NAK Effective interrupt
5	INTknEPMis	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received with EP Mismatch interrupt **0x0: INACTIVE :** No IN Token Received with EP Mismatch interrupt
4	INTknTXFEmp	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received Interrupt

24.1.66 USBHS_DWC_otg_intreg_DIEPINT1 (continued)

		0x0: INACTIVE : No IN Token Received interrupt
3	TimeOUT	Timeout Condition (TimeOUT) - In shared TX FIFO mode, applies to non-isochronous IN endpoints only. - In dedicated FIFO mode, applies only to Control IN endpoints. - In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Timeout interrupt **0x0: INACTIVE :** No Timeout interrupt
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt
0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0

24.1.66 USBHS_DWC_otg_intreg_DIEPINT1 (continued)

0x1: ACTIVE :

Transfer Complete Interrupt

0x0: INACTIVE :

No Transfer Complete Interrupt

24.1.67 USBHS_DWC_otg_intreg_DIEPTSIZ1

Description: This register reflects the Transfer Size of the IN Endpoint 1 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900930

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW		RW				
HW Access	Reserved							
Name	Reserved	MC [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	MC	MC Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetchfor an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp) Default Value: 0x0 **0x1: PACKETONE :** 1 packet **0x3: PACKETTHREE :** 3 packets **0x2: PACKETTWO :** 2 packets

24.1.67 USBHS_DWC_otg_intreg_DIEPTSIZ1 (continued)

28 : 19	PktCnt	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO. Default Value: 0x0

24.1.68 USBHS_DWC_otg_intreg_DIEPDMA1

Description: This register contains the DMA Address for the IN Endpoint 1 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900934

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.69 USBHS_DWC_otg_intreg_DTXFSTS1

Description: This register reflects the status of the IN Endpoint Transmit FIFO Status Register 1 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900938

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	INEPTxFSpcAvail	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. - 16'h0: Endpoint TxFIFO is full - 16'h1: 1 word available - 16'h2: 2 words available - 16'hn: n words available (where 0 n 32,768) - 16'h8000: 32,768 words available - Others: Reserved In DRD configurations (OTG_MODE = 0, 1, or 2) with dynamic fifo sizing feature enabled (OTG_DFIFO_DYNAMIC=1), the value of this field is, - the maximum value of (OTG_TX_HNPERIO_DFIFO_DEPTH, OTG_TX_DINEP_DFIFO_DEPTH_0) during reset, and - OTG_TX_DINEP_DFIFO_DEPTH_0, immediately after reset deassertion Default Value: 0x100

24.1.70 USBHS_DWC_otg_intreg_DIEPDMAB1

Description: This register contains the DMA Buffer Address of the IN Endpoint 1 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x4490093C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.71 USBHS_DWC_otg_intreg_DIEPCTL2

Description: This register is used to control the characteristics of Endpoint 2. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900940

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	Reserved	RW		R	R
HW Access				Reserved				
Name	TxFNum [23:22]		Stall	Reserved	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	RW	
HW Access								
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled, -- For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. -- For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. - When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: -- For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. -- For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: -- SETUP Phase Done -- Endpoint Disabled -- Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.71 USBHS_DWC_otg_intreg_DIEPCTL2 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	SetD1PID - Set DATA1 PID (SetD1PID) -- Applies to interrupt and bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. -- This field is applicable both for Scatter-Gather DMA mode and non Scatter-Gather DMA mode. - Set odd (micro)Frame (SetOddFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the even and odd (micro)Frame (EO_FrNum) field to odd (micro)Frame. -- This field is not applicable for Scatter-Gather DMA mode. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID **0x1: ENABLED :** Enables Set DATA1 PID
28	SetD0PID	SetD0PID - Set DATA0 PID (SetD0PID) -- Applies to interrupt/bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. -- This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)Frame (SetEvenFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the Even/Odd (micro)Frame (EO_FrNum) field to even (micro)Frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID **0x1: ENABLED :** Endpoint Data PID to DATA0)

24.1.71 USBHS_DWC_otg_intreg_DIEPCTL2 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
25 : 22	TxFNum	TxFIFO Number (TxFNum) Shared FIFO Operation non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. - 4'h0: Non-Periodic TxFIFO - Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: These bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints. Default Value: 0x0 **0x0: TXFIFO0 :** Tx FIFO 0 **0x1: TXFIFO1 :** Tx FIFO 1 **0xa: TXFIFO10 :** Tx FIFO 10 **0xb: TXFIFO11 :** Tx FIFO 11 **0xc: TXFIFO12 :** Tx FIFO 12

24.1.71 USBHS_DWC_otg_intreg_DIEPCTL2 (continued)

		0xd: TXFIFO13 : Tx FIFO 13 **0xe: TXFIFO14 :** Tx FIFO 14 **0xf: TXFIFO15 :** Tx FIFO 15 **0x2: TXFIFO2 :** Tx FIFO 2 **0x3: TXFIFO3 :** Tx FIFO 3 **0x4: TXFIFO4 :** Tx FIFO 4 **0x5: TXFIFO5 :** Tx FIFO 5 **0x6: TXFIFO6 :** Tx FIFO 6 **0x7: TXFIFO7 :** Tx FIFO 7 **0x8: TXFIFO8 :** Tx FIFO 8 **0x9: TXFIFO9 :** Tx FIFO 9
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

24.1.71 USBHS_DWC_otg_intreg_DIEPCTL2 (continued)

		0x1: ACTIVE : STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUP :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.71 USBHS_DWC_otg_intreg_DIEPCTL2 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. - 1'b0: Even (micro)frame - 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Default Value: 0x0 **0x0: DATA0EVENFRM :** DATA0 or Even Frame **0x1: DATA1ODDFRM :** DATA1 or Odd Frame
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical end-point. This value is in bytes. Default Value: 0x0

24.1.72 USBHS_DWC_otg_intreg_DIEPINT2

Description: This register contains the interrupts for the IN Endpoint 2 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900948

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	TxFEmp	INEPNakEff	INTknEP-Mis	INTknTX-FEmp	TimeOUT	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	Reserved	RW	RW
HW Access	Reserved					Reserved		
Name	Reserved	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt

24.1.72 USBHS_DWC_otg_intreg_DIEPINT2 (continued)

		0x0: INACTIVE : No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Default Value: 0x0 **0x1: ACTIVE :** BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	TxfifoUndrn	Fifo Underrun (TxfifoUndrn) Applies to IN endpoints Only This bit is valid only If thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** TxFIFO Underrun interrupt **0x0: INACTIVE :** No Tx FIFO Underrun interrupt

24.1.72 USBHS_DWC_otg_intreg_DIEPINT2 (continued)

7	TxFEmp	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)). Default Value: 0x1 **0x1: ACTIVE :** Transmit FIFO Empty interrupt **0x0: INACTIVE :** No Transmit FIFO Empty interrupt
6	INEPNakEff	IN Endpoint NAK Effective (INEPNakEff) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCT-Ln.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. Default Value: 0x0 **0x1: ACTIVE :** IN Endpoint NAK Effective interrupt **0x0: INACTIVE :** No Endpoint NAK Effective interrupt
5	INTknEPMis	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received with EP Mismatch interrupt **0x0: INACTIVE :** No IN Token Received with EP Mismatch interrupt
4	INTknTXFEmp	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received Interrupt

24.1.72 USBHS_DWC_otg_intreg_DIEPINT2 (continued)

		0x0: INACTIVE : No IN Token Received interrupt
3	TimeOUT	Timeout Condition (TimeOUT) - In shared TX FIFO mode, applies to non-isochronous IN endpoints only. - In dedicated FIFO mode, applies only to Control IN endpoints. - In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Timeout interrupt **0x0: INACTIVE :** No Timeout interrupt
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt
0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0

24.1.72 USBHS_DWC_otg_intreg_DIEPINT2 (continued)

0x1: ACTIVE :

Transfer Complete Interrupt

0x0: INACTIVE :

No Transfer Complete Interrupt

24.1.73 USBHS_DWC_otg_intreg_DIEPTSIZ2

Description: This register reflects the Transfer Size of the IN Endpoint 2 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900950

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW		RW				
HW Access	Reserved							
Name	Reserved	MC [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	MC	MC Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetchfor an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp) Default Value: 0x0 **0x1: PACKETONE :** 1 packet **0x3: PACKETTHREE :** 3 packets **0x2: PACKETTWO :** 2 packets

24.1.73 USBHS_DWC_otg_intreg_DIEPTSIZ2 (continued)

28 : 19	PktCnt	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO. Default Value: 0x0

24.1.74 USBHS_DWC_otg_intreg_DIEPDMA2

Description: This register contains the DMA Address for the IN Endpoint 2 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900954

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.75 USBHS_DWC_otg_intreg_DTXFSTS2

Description: This register reflects the status of the IN Endpoint Transmit FIFO Status Register 2 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900958

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	INEPTxFSpcAvail	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. - 16'h0: Endpoint TxFIFO is full - 16'h1: 1 word available - 16'h2: 2 words available - 16'hn: n words available (where 0 n 32,768) - 16'h8000: 32,768 words available - Others: Reserved In DRD configurations (OTG_MODE = 0, 1, or 2) with dynamic fifo sizing feature enabled (OTG_DFIFO_DYNAMIC=1), the value of this field is, - the maximum value of (OTG_TX_HNPERIO_DFIFO_DEPTH, OTG_TX_DINEP_DFIFO_DEPTH_0) during reset, and - OTG_TX_DINEP_DFIFO_DEPTH_0, immediately after reset deassertion Default Value: 0x100

24.1.76 USBHS_DWC_otg_intreg_DIEPDMAB2

Description: This register contains the DMA Buffer Address of the IN Endpoint 2 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x4490095C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.77 USBHS_DWC_otg_intreg_DIEPCTL3

Description: This register is used to control the characteristics of Endpoint 3. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900960

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	Reserved	RW		R	R
HW Access				Reserved				
Name	TxFNum [23:22]		Stall	Reserved	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	RW	
HW Access								
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled, -- For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. -- For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. - When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: -- For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. -- For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: -- SETUP Phase Done -- Endpoint Disabled -- Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.77 USBHS_DWC_otg_intreg_DIEPCTL3 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	SetD1PID - Set DATA1 PID (SetD1PID) -- Applies to interrupt and bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. -- This field is applicable both for Scatter-Gather DMA mode and non Scatter-Gather DMA mode. - Set odd (micro)Frame (SetOddFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the even and odd (micro)Frame (EO_FrNum) field to odd (micro)Frame. -- This field is not applicable for Scatter-Gather DMA mode. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID **0x1: ENABLED :** Enables Set DATA1 PID
28	SetD0PID	SetD0PID - Set DATA0 PID (SetD0PID) -- Applies to interrupt/bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. -- This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)Frame (SetEvenFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the Even/Odd (micro)Frame (EO_FrNum) field to even (micro)Frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID **0x1: ENABLED :** Endpoint Data PID to DATA0)

24.1.77 USBHS_DWC_otg_intreg_DIEPCTL3 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
25 : 22	TxFNum	TxFIFO Number (TxFNum) Shared FIFO Operation non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. - 4'h0: Non-Periodic TxFIFO - Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: These bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints. Default Value: 0x0 **0x0: TXFIFO0 :** Tx FIFO 0 **0x1: TXFIFO1 :** Tx FIFO 1 **0xa: TXFIFO10 :** Tx FIFO 10 **0xb: TXFIFO11 :** Tx FIFO 11 **0xc: TXFIFO12 :** Tx FIFO 12

24.1.77 USBHS_DWC_otg_intreg_DIEPCTL3 (continued)

		0xd: TXFIFO13 : Tx FIFO 13 **0xe: TXFIFO14 :** Tx FIFO 14 **0xf: TXFIFO15 :** Tx FIFO 15 **0x2: TXFIFO2 :** Tx FIFO 2 **0x3: TXFIFO3 :** Tx FIFO 3 **0x4: TXFIFO4 :** Tx FIFO 4 **0x5: TXFIFO5 :** Tx FIFO 5 **0x6: TXFIFO6 :** Tx FIFO 6 **0x7: TXFIFO7 :** Tx FIFO 7 **0x8: TXFIFO8 :** Tx FIFO 8 **0x9: TXFIFO9 :** Tx FIFO 9
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

24.1.77 USBHS_DWC_otg_intreg_DIEPCTL3 (continued)

		0x1: ACTIVE : STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUP :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.77 USBHS_DWC_otg_intreg_DIEPCTL3 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. - 1'b0: Even (micro)frame - 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Default Value: 0x0 **0x0: DATA0EVENFRM :** DATA0 or Even Frame **0x1: DATA1ODDFRM :** DATA1 or Odd Frame
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical end-point. This value is in bytes. Default Value: 0x0

24.1.78 USBHS_DWC_otg_intreg_DIEPINT3

Description: This register contains the interrupts for the IN Endpoint 3 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900968

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	TxFEmp	INEPNakEff	INTknEP-Mis	INTknTX-FEmp	TimeOUT	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	Reserved	RW	RW
HW Access	Reserved					Reserved		
Name	Reserved	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt

24.1.78 USBHS_DWC_otg_intreg_DIEPINT3 (continued)

		0x0: INACTIVE : No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Default Value: 0x0 **0x1: ACTIVE :** BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	TxfifoUndrn	Fifo Underrun (TxfifoUndrn) Applies to IN endpoints Only This bit is valid only If thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** TxFIFO Underrun interrupt **0x0: INACTIVE :** No Tx FIFO Underrun interrupt

24.1.78 USBHS_DWC_otg_intreg_DIEPINT3 (continued)

7	TxFEmp	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)). Default Value: 0x1 **0x1: ACTIVE :** Transmit FIFO Empty interrupt **0x0: INACTIVE :** No Transmit FIFO Empty interrupt
6	INEPNakEff	IN Endpoint NAK Effective (INEPNakEff) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCT-Ln.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. Default Value: 0x0 **0x1: ACTIVE :** IN Endpoint NAK Effective interrupt **0x0: INACTIVE :** No Endpoint NAK Effective interrupt
5	INTknEPMis	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received with EP Mismatch interrupt **0x0: INACTIVE :** No IN Token Received with EP Mismatch interrupt
4	INTknTXFEmp	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received Interrupt

24.1.78 USBHS_DWC_otg_intreg_DIEPINT3 (continued)

		0x0: INACTIVE : No IN Token Received interrupt
3	TimeOUT	Timeout Condition (TimeOUT) - In shared TX FIFO mode, applies to non-isochronous IN endpoints only. - In dedicated FIFO mode, applies only to Control IN endpoints. - In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Timeout interrupt **0x0: INACTIVE :** No Timeout interrupt
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt
0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0

24.1.78 USBHS_DWC_otg_intreg_DIEPINT3 (continued)

0x1: ACTIVE :

Transfer Complete Interrupt

0x0: INACTIVE :

No Transfer Complete Interrupt

24.1.79 USBHS_DWC_otg_intreg_DIEPTSIZ3

Description: This register reflects the Transfer Size of the IN Endpoint 3 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900970

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW		RW				
HW Access	Reserved							
Name	Reserved	MC [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	MC	MC Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetchfor an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp) Default Value: 0x0 **0x1: PACKETONE :** 1 packet **0x3: PACKETTHREE :** 3 packets **0x2: PACKETTWO :** 2 packets

24.1.79 USBHS_DWC_otg_intreg_DIEPTSIZ3 (continued)

28 : 19	PktCnt	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO. Default Value: 0x0

24.1.80 USBHS_DWC_otg_intreg_DIEPDMA3

Description: This register contains the DMA Address for the IN Endpoint 3 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900974

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.81 USBHS_DWC_otg_intreg_DTXFSTS3

Description: This register reflects the status of the IN Endpoint Transmit FIFO Status Register 3 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900978

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	INEPTxFSpcAvail	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. - 16'h0: Endpoint TxFIFO is full - 16'h1: 1 word available - 16'h2: 2 words available - 16'hn: n words available (where 0 n 32,768) - 16'h8000: 32,768 words available - Others: Reserved In DRD configurations (OTG_MODE = 0, 1, or 2) with dynamic fifo sizing feature enabled (OTG_DFIFO_DYNAMIC=1), the value of this field is, - the maximum value of (OTG_TX_HNPERIO_DFIFO_DEPTH, OTG_TX_DINEP_DFIFO_DEPTH_0) during reset, and - OTG_TX_DINEP_DFIFO_DEPTH_0, immediately after reset deassertion Default Value: 0x100

24.1.82 USBHS_DWC_otg_intreg_DIEPDMAB3

Description: This register contains the DMA Buffer Address of the IN Endpoint 3 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x4490097C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.83 USBHS_DWC_otg_intreg_DIEPCTL4

Description: This register is used to control the characteristics of Endpoint 4. Note: This register exists for an endpoint i if the OT-G_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900980

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	Reserved	RW		R	R
HW Access				Reserved				
Name	TxFNum [23:22]		Stall	Reserved	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	RW	
HW Access								
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled, -- For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. -- For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. - When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: -- For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. -- For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: -- SETUP Phase Done -- Endpoint Disabled -- Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.83 USBHS_DWC_otg_intreg_DIEPCTL4 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	SetD1PID - Set DATA1 PID (SetD1PID) -- Applies to interrupt and bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. -- This field is applicable both for Scatter-Gather DMA mode and non Scatter-Gather DMA mode. - Set odd (micro)Frame (SetOddFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the even and odd (micro)Frame (EO_FrNum) field to odd (micro)Frame. -- This field is not applicable for Scatter-Gather DMA mode. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID **0x1: ENABLED :** Enables Set DATA1 PID
28	SetD0PID	SetD0PID - Set DATA0 PID (SetD0PID) -- Applies to interrupt/bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. -- This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)Frame (SetEvenFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the Even/Odd (micro)Frame (EO_FrNum) field to even (micro)Frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID **0x1: ENABLED :** Endpoint Data PID to DATA0)

24.1.83 USBHS_DWC_otg_intreg_DIEPCTL4 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
25 : 22	TxFNum	TxFIFO Number (TxFNum) Shared FIFO Operation non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. - 4'h0: Non-Periodic TxFIFO - Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: These bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints. Default Value: 0x0 **0x0: TXFIFO0 :** Tx FIFO 0 **0x1: TXFIFO1 :** Tx FIFO 1 **0xa: TXFIFO10 :** Tx FIFO 10 **0xb: TXFIFO11 :** Tx FIFO 11 **0xc: TXFIFO12 :** Tx FIFO 12

24.1.83 USBHS_DWC_otg_intreg_DIEPCTL4 (continued)

		0xd: TXFIFO13 : Tx FIFO 13 **0xe: TXFIFO14 :** Tx FIFO 14 **0xf: TXFIFO15 :** Tx FIFO 15 **0x2: TXFIFO2 :** Tx FIFO 2 **0x3: TXFIFO3 :** Tx FIFO 3 **0x4: TXFIFO4 :** Tx FIFO 4 **0x5: TXFIFO5 :** Tx FIFO 5 **0x6: TXFIFO6 :** Tx FIFO 6 **0x7: TXFIFO7 :** Tx FIFO 7 **0x8: TXFIFO8 :** Tx FIFO 8 **0x9: TXFIFO9 :** Tx FIFO 9
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

24.1.83 USBHS_DWC_otg_intreg_DIEPCTL4 (continued)

		0x1: ACTIVE : STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUP :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.83 USBHS_DWC_otg_intreg_DIEPCTL4 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. - 1'b0: Even (micro)frame - 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Default Value: 0x0 **0x0: DATA0EVENFRM :** DATA0 or Even Frame **0x1: DATA1ODDFRM :** DATA1 or Odd Frame
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical end-point. This value is in bytes. Default Value: 0x0

24.1.84 USBHS_DWC_otg_intreg_DIEPINT4

Description: This register contains the interrupts for the IN Endpoint 4 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900988

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	TxFEmp	INEPNakEff	INTknEP-Mis	INTknTX-FEmp	TimeOUT	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	Reserved	RW	RW
HW Access	Reserved					Reserved		
Name	Reserved	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt

24.1.84 USBHS_DWC_otg_intreg_DIEPINT4 (continued)

		0x0: INACTIVE : No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Default Value: 0x0 **0x1: ACTIVE :** BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	TxfifoUndrn	Fifo Underrun (TxfifoUndrn) Applies to IN endpoints Only This bit is valid only If thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** TxFIFO Underrun interrupt **0x0: INACTIVE :** No Tx FIFO Underrun interrupt

24.1.84 USBHS_DWC_otg_intreg_DIEPINT4 (continued)

7	TxFEmp	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)). Default Value: 0x1 **0x1: ACTIVE :** Transmit FIFO Empty interrupt **0x0: INACTIVE :** No Transmit FIFO Empty interrupt
6	INEPNakEff	IN Endpoint NAK Effective (INEPNakEff) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCT-Ln.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. Default Value: 0x0 **0x1: ACTIVE :** IN Endpoint NAK Effective interrupt **0x0: INACTIVE :** No Endpoint NAK Effective interrupt
5	INTknEPMis	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received with EP Mismatch interrupt **0x0: INACTIVE :** No IN Token Received with EP Mismatch interrupt
4	INTknTXFEmp	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received Interrupt

24.1.84 USBHS_DWC_otg_intreg_DIEPINT4 (continued)

		0x0: INACTIVE : No IN Token Received interrupt
3	TimeOUT	Timeout Condition (TimeOUT) - In shared TX FIFO mode, applies to non-isochronous IN endpoints only. - In dedicated FIFO mode, applies only to Control IN endpoints. - In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Timeout interrupt **0x0: INACTIVE :** No Timeout interrupt
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt
0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0

24.1.84 USBHS_DWC_otg_intreg_DIEPINT4 (continued)

0x1: ACTIVE :

Transfer Complete Interrupt

0x0: INACTIVE :

No Transfer Complete Interrupt

24.1.85 USBHS_DWC_otg_intreg_DIEPTSIZ4

Description: This register reflects the Transfer Size of the IN Endpoint 4 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900990

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW		RW				
HW Access	Reserved							
Name	Reserved	MC [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	MC	MC Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetchfor an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp) Default Value: 0x0 **0x1: PACKETONE :** 1 packet **0x3: PACKETTHREE :** 3 packets **0x2: PACKETTWO :** 2 packets

24.1.85 USBHS_DWC_otg_intreg_DIEPTSIZ4 (continued)

28 : 19	PktCnt	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO. Default Value: 0x0

24.1.86 USBHS_DWC_otg_intreg_DIEPDMA4

Description: This register contains the DMA Address for the IN Endpoint 4 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900994

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.87 USBHS_DWC_otg_intreg_DTXFSTS4

Description: This register reflects the status of the IN Endpoint Transmit FIFO Status Register 4 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900998

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	INEPTxFSpcAvail	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. - 16'h0: Endpoint TxFIFO is full - 16'h1: 1 word available - 16'h2: 2 words available - 16'hn: n words available (where 0 n 32,768) - 16'h8000: 32,768 words available - Others: Reserved In DRD configurations (OTG_MODE = 0, 1, or 2) with dynamic fifo sizing feature enabled (OTG_DFIFO_DYNAMIC=1), the value of this field is, - the maximum value of (OTG_TX_HNPERIO_DFIFO_DEPTH, OTG_TX_DINEP_DFIFO_DEPTH_0) during reset, and - OTG_TX_DINEP_DFIFO_DEPTH_0, immediately after reset deassertion Default Value: 0x100

24.1.88 USBHS_DWC_otg_intreg_DIEPDMAB4

Description: This register contains the DMA Buffer Address of the IN Endpoint 4 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x4490099C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.89 USBHS_DWC_otg_intreg_DIEPCTL5

Description: This register is used to control the characteristics of Endpoint 5. Note: This register exists for an endpoint i if the OT-G_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	Reserved	RW		R	R
HW Access				Reserved				
Name	TxFNum [23:22]		Stall	Reserved	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	RW	
HW Access								
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled, -- For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. -- For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. - When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: -- For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. -- For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: -- SETUP Phase Done -- Endpoint Disabled -- Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.89 USBHS_DWC_otg_intreg_DIEPCTL5 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	SetD1PID - Set DATA1 PID (SetD1PID) -- Applies to interrupt and bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. -- This field is applicable both for Scatter-Gather DMA mode and non Scatter-Gather DMA mode. - Set odd (micro)Frame (SetOddFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the even and odd (micro)Frame (EO_FrNum) field to odd (micro)Frame. -- This field is not applicable for Scatter-Gather DMA mode. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID **0x1: ENABLED :** Enables Set DATA1 PID
28	SetD0PID	SetD0PID - Set DATA0 PID (SetD0PID) -- Applies to interrupt/bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. -- This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)Frame (SetEvenFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the Even/Odd (micro)Frame (EO_FrNum) field to even (micro)Frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID **0x1: ENABLED :** Endpoint Data PID to DATA0)

24.1.89 USBHS_DWC_otg_intreg_DIEPCTL5 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
25 : 22	TxFNum	TxFIFO Number (TxFNum) Shared FIFO Operation non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. - 4'h0: Non-Periodic TxFIFO - Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: These bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints. Default Value: 0x0 **0x0: TXFIFO0 :** Tx FIFO 0 **0x1: TXFIFO1 :** Tx FIFO 1 **0xa: TXFIFO10 :** Tx FIFO 10 **0xb: TXFIFO11 :** Tx FIFO 11 **0xc: TXFIFO12 :** Tx FIFO 12

24.1.89 USBHS_DWC_otg_intreg_DIEPCTL5 (continued)

		0xd: TXFIFO13 : Tx FIFO 13 **0xe: TXFIFO14 :** Tx FIFO 14 **0xf: TXFIFO15 :** Tx FIFO 15 **0x2: TXFIFO2 :** Tx FIFO 2 **0x3: TXFIFO3 :** Tx FIFO 3 **0x4: TXFIFO4 :** Tx FIFO 4 **0x5: TXFIFO5 :** Tx FIFO 5 **0x6: TXFIFO6 :** Tx FIFO 6 **0x7: TXFIFO7 :** Tx FIFO 7 **0x8: TXFIFO8 :** Tx FIFO 8 **0x9: TXFIFO9 :** Tx FIFO 9
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

24.1.89 USBHS_DWC_otg_intreg_DIEPCTL5 (continued)

0x1: ACTIVE :

STALL All Active Tokens

0x0: INACTIVE :

STALL All non-active tokens

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0

0x2: BULK :

Bulk

0x0: CONTROL :

Control

0x3: INTERRUP :

Interrupt

0x1: ISOCHRONOUS :

Isochronous

17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

0x1: NAK :

The core is transmitting NAK handshakes on this endpoint

0x0: NONNAK :

The core is transmitting non-NAK handshakes based on the FIFO status

24.1.89 USBHS_DWC_otg_intreg_DIEPCTL5 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. - 1'b0: Even (micro)frame - 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Default Value: 0x0 **0x0: DATA0EVENFRM :** DATA0 or Even Frame **0x1: DATA1ODDFRM :** DATA1 or Odd Frame
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical end-point. This value is in bytes. Default Value: 0x0

24.1.90 USBHS_DWC_otg_intreg_DIEPINT5

Description: This register contains the interrupts for the IN Endpoint 5 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	TxFEmp	INEPNakEff	INTknEP-Mis	INTknTX-FEmp	TimeOUT	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	Reserved	RW	RW
HW Access	Reserved					Reserved		
Name	Reserved	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt

24.1.90 USBHS_DWC_otg_intreg_DIEPINT5 (continued)

		0x0: INACTIVE : No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Default Value: 0x0 **0x1: ACTIVE :** BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	TxfifoUndrn	Fifo Underrun (TxfifoUndrn) Applies to IN endpoints Only This bit is valid only If thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** TxFIFO Underrun interrupt **0x0: INACTIVE :** No Tx FIFO Underrun interrupt

24.1.90 USBHS_DWC_otg_intreg_DIEPINT5 (continued)

7	TxFEmp	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)). Default Value: 0x1 **0x1: ACTIVE :** Transmit FIFO Empty interrupt **0x0: INACTIVE :** No Transmit FIFO Empty interrupt
6	INEPNakEff	IN Endpoint NAK Effective (INEPNakEff) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCT-Ln.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. Default Value: 0x0 **0x1: ACTIVE :** IN Endpoint NAK Effective interrupt **0x0: INACTIVE :** No Endpoint NAK Effective interrupt
5	INTknEPMis	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received with EP Mismatch interrupt **0x0: INACTIVE :** No IN Token Received with EP Mismatch interrupt
4	INTknTXFEmp	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received Interrupt

24.1.90 USBHS_DWC_otg_intreg_DIEPINT5 (continued)

		0x0: INACTIVE : No IN Token Received interrupt
3	TimeOUT	Timeout Condition (TimeOUT) - In shared TX FIFO mode, applies to non-isochronous IN endpoints only. - In dedicated FIFO mode, applies only to Control IN endpoints. - In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Timeout interrupt **0x0: INACTIVE :** No Timeout interrupt
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt
0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0

24.1.90 USBHS_DWC_otg_intreg_DIEPINT5 (continued)

0x1: ACTIVE :

Transfer Complete Interrupt

0x0: INACTIVE :

No Transfer Complete Interrupt

24.1.91 USBHS_DWC_otg_intreg_DIEPTSIZ5

Description: This register reflects the Transfer Size of the IN Endpoint 5 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW		RW				
HW Access	Reserved							
Name	Reserved	MC [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	MC	MC Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetchfor an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp) Default Value: 0x0 **0x1: PACKETONE :** 1 packet **0x3: PACKETTHREE :** 3 packets **0x2: PACKETTWO :** 2 packets

24.1.91 USBHS_DWC_otg_intreg_DIEPTSIZ5 (continued)

28 : 19	PktCnt	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO. Default Value: 0x0

24.1.92 USBHS_DWC_otg_intreg_DIEPDMA5

Description: This register contains the DMA Address for the IN Endpoint 5 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.93 USBHS_DWC_otg_intreg_DTXFSTS5

Description: This register reflects the status of the IN Endpoint Transmit FIFO Status Register 5 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	INEPTxFSpcAvail	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. - 16'h0: Endpoint TxFIFO is full - 16'h1: 1 word available - 16'h2: 2 words available - 16'hn: n words available (where 0 n 32,768) - 16'h8000: 32,768 words available - Others: Reserved In DRD configurations (OTG_MODE = 0, 1, or 2) with dynamic fifo sizing feature enabled (OTG_DFIFO_DYNAMIC=1), the value of this field is, - the maximum value of (OTG_TX_HNPERIO_DFIFO_DEPTH, OTG_TX_DINEP_DFIFO_DEPTH_0) during reset, and - OTG_TX_DINEP_DFIFO_DEPTH_0, immediately after reset deassertion Default Value: 0x100

24.1.94 USBHS_DWC_otg_intreg_DIEPDMAB5

Description: This register contains the DMA Buffer Address of the IN Endpoint 5 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.95 USBHS_DWC_otg_intreg_DIEPCTL6

Description: This register is used to control the characteristics of Endpoint 6. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	Reserved	RW		R	R
HW Access				Reserved				
Name	TxFNum [23:22]		Stall	Reserved	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	RW	
HW Access								
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled, -- For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. -- For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. - When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: -- For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. -- For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: -- SETUP Phase Done -- Endpoint Disabled -- Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.95 USBHS_DWC_otg_intreg_DIEPCTL6 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	SetD1PID - Set DATA1 PID (SetD1PID) -- Applies to interrupt and bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. -- This field is applicable both for Scatter-Gather DMA mode and non Scatter-Gather DMA mode. - Set odd (micro)Frame (SetOddFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the even and odd (micro)Frame (EO_FrNum) field to odd (micro)Frame. -- This field is not applicable for Scatter-Gather DMA mode. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID **0x1: ENABLED :** Enables Set DATA1 PID
28	SetD0PID	SetD0PID - Set DATA0 PID (SetD0PID) -- Applies to interrupt/bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. -- This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)Frame (SetEvenFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the Even/Odd (micro)Frame (EO_FrNum) field to even (micro)Frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID **0x1: ENABLED :** Endpoint Data PID to DATA0)

24.1.95 USBHS_DWC_otg_intreg_DIEPCTL6 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
25 : 22	TxFNum	TxFIFO Number (TxFNum) Shared FIFO Operation non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. - 4'h0: Non-Periodic TxFIFO - Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: These bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints. Default Value: 0x0 **0x0: TXFIFO0 :** Tx FIFO 0 **0x1: TXFIFO1 :** Tx FIFO 1 **0xa: TXFIFO10 :** Tx FIFO 10 **0xb: TXFIFO11 :** Tx FIFO 11 **0xc: TXFIFO12 :** Tx FIFO 12

24.1.95 USBHS_DWC_otg_intreg_DIEPCTL6 (continued)

		0xd: TXFIFO13 : Tx FIFO 13 **0xe: TXFIFO14 :** Tx FIFO 14 **0xf: TXFIFO15 :** Tx FIFO 15 **0x2: TXFIFO2 :** Tx FIFO 2 **0x3: TXFIFO3 :** Tx FIFO 3 **0x4: TXFIFO4 :** Tx FIFO 4 **0x5: TXFIFO5 :** Tx FIFO 5 **0x6: TXFIFO6 :** Tx FIFO 6 **0x7: TXFIFO7 :** Tx FIFO 7 **0x8: TXFIFO8 :** Tx FIFO 8 **0x9: TXFIFO9 :** Tx FIFO 9
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

24.1.95 USBHS_DWC_otg_intreg_DIEPCTL6 (continued)

		0x1: ACTIVE : STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUP :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.95 USBHS_DWC_otg_intreg_DIEPCTL6 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. - 1'b0: Even (micro)frame - 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Default Value: 0x0 **0x0: DATA0EVENFRM :** DATA0 or Even Frame **0x1: DATA1ODDFRM :** DATA1 or Odd Frame
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical end-point. This value is in bytes. Default Value: 0x0

24.1.96 USBHS_DWC_otg_intreg_DIEPINT6

Description: This register contains the interrupts for the IN Endpoint 6 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	TxFEmp	INEPNakEff	INTknEP-Mis	INTknTX-FEmp	TimeOUT	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	Reserved	RW	RW
HW Access	Reserved					Reserved		
Name	Reserved	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt

24.1.96 USBHS_DWC_otg_intreg_DIEPINT6 (continued)

		0x0: INACTIVE : No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Default Value: 0x0 **0x1: ACTIVE :** BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	TxfifoUndrn	Fifo Underrun (TxfifoUndrn) Applies to IN endpoints Only This bit is valid only If thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** TxFIFO Underrun interrupt **0x0: INACTIVE :** No Tx FIFO Underrun interrupt

24.1.96 USBHS_DWC_otg_intreg_DIEPINT6 (continued)

7	TxFEmp	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)). Default Value: 0x1 **0x1: ACTIVE :** Transmit FIFO Empty interrupt **0x0: INACTIVE :** No Transmit FIFO Empty interrupt
6	INEPNakEff	IN Endpoint NAK Effective (INEPNakEff) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCT-Ln.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. Default Value: 0x0 **0x1: ACTIVE :** IN Endpoint NAK Effective interrupt **0x0: INACTIVE :** No Endpoint NAK Effective interrupt
5	INTknEPMis	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received with EP Mismatch interrupt **0x0: INACTIVE :** No IN Token Received with EP Mismatch interrupt
4	INTknTXFEmp	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received Interrupt

24.1.96 USBHS_DWC_otg_intreg_DIEPINT6 (continued)

		0x0: INACTIVE : No IN Token Received interrupt
3	TimeOUT	Timeout Condition (TimeOUT) - In shared TX FIFO mode, applies to non-isochronous IN endpoints only. - In dedicated FIFO mode, applies only to Control IN endpoints. - In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Timeout interrupt **0x0: INACTIVE :** No Timeout interrupt
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt
0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0

24.1.96 USBHS_DWC_otg_intreg_DIEPINT6 (continued)

0x1: ACTIVE :

Transfer Complete Interrupt

0x0: INACTIVE :

No Transfer Complete Interrupt

24.1.97 USBHS_DWC_otg_intreg_DIEPTSIZ6

Description: This register reflects the Transfer Size of the IN Endpoint 6 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW		RW				
HW Access	Reserved							
Name	Reserved	MC [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	MC	MC Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetchfor an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp) Default Value: 0x0 **0x1: PACKETONE :** 1 packet **0x3: PACKETTHREE :** 3 packets **0x2: PACKETTWO :** 2 packets

24.1.97 USBHS_DWC_otg_intreg_DIEPTSIZ6 (continued)

28 : 19	PktCnt	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO. Default Value: 0x0

24.1.98 USBHS_DWC_otg_intreg_DIEPDMA6

Description: This register contains the DMA Address for the IN Endpoint 6 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.99 USBHS_DWC_otg_intreg_DTXFSTS6

Description: This register reflects the status of the IN Endpoint Transmit FIFO Status Register 6 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	INEPTxFSpcAvail	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. - 16'h0: Endpoint TxFIFO is full - 16'h1: 1 word available - 16'h2: 2 words available - 16'hn: n words available (where 0 n 32,768) - 16'h8000: 32,768 words available - Others: Reserved In DRD configurations (OTG_MODE = 0, 1, or 2) with dynamic fifo sizing feature enabled (OTG_DFIFO_DYNAMIC=1), the value of this field is, - the maximum value of (OTG_TX_HNPERIO_DFIFO_DEPTH, OTG_TX_DINEP_DFIFO_DEPTH_0) during reset, and - OTG_TX_DINEP_DFIFO_DEPTH_0, immediately after reset deassertion Default Value: 0x100

24.1.100 USBHS_DWC_otg_intreg_DIEPDMAB6

Description: This register contains the DMA Buffer Address of the IN Endpoint 6 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.101 USBHS_DWC_otg_intreg_DIEPCTL7

Description: This register is used to control the characteristics of Endpoint 7. Note: This register exists for an endpoint i if the OT-G_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	Reserved	RW		R	R
HW Access				Reserved				
Name	TxFNum [23:22]		Stall	Reserved	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	RW	
HW Access								
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled, -- For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. -- For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. - When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: -- For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. -- For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: -- SETUP Phase Done -- Endpoint Disabled -- Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.101 USBHS_DWC_otg_intreg_DIEPCTL7 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	SetD1PID - Set DATA1 PID (SetD1PID) -- Applies to interrupt and bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. -- This field is applicable both for Scatter-Gather DMA mode and non Scatter-Gather DMA mode. - Set odd (micro)Frame (SetOddFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the even and odd (micro)Frame (EO_FrNum) field to odd (micro)Frame. -- This field is not applicable for Scatter-Gather DMA mode. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID **0x1: ENABLED :** Enables Set DATA1 PID
28	SetD0PID	SetD0PID - Set DATA0 PID (SetD0PID) -- Applies to interrupt/bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. -- This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)Frame (SetEvenFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the Even/Odd (micro)Frame (EO_FrNum) field to even (micro)Frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID **0x1: ENABLED :** Endpoint Data PID to DATA0)

24.1.101 USBHS_DWC_otg_intreg_DIEPCTL7 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
25 : 22	TxFNum	TxFIFO Number (TxFNum) Shared FIFO Operation non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. - 4'h0: Non-Periodic TxFIFO - Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: These bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints. Default Value: 0x0 **0x0: TXFIFO0 :** Tx FIFO 0 **0x1: TXFIFO1 :** Tx FIFO 1 **0xa: TXFIFO10 :** Tx FIFO 10 **0xb: TXFIFO11 :** Tx FIFO 11 **0xc: TXFIFO12 :** Tx FIFO 12

24.1.101 USBHS_DWC_otg_intreg_DIEPCTL7 (continued)

		0xd: TXFIFO13 : Tx FIFO 13 **0xe: TXFIFO14 :** Tx FIFO 14 **0xf: TXFIFO15 :** Tx FIFO 15 **0x2: TXFIFO2 :** Tx FIFO 2 **0x3: TXFIFO3 :** Tx FIFO 3 **0x4: TXFIFO4 :** Tx FIFO 4 **0x5: TXFIFO5 :** Tx FIFO 5 **0x6: TXFIFO6 :** Tx FIFO 6 **0x7: TXFIFO7 :** Tx FIFO 7 **0x8: TXFIFO8 :** Tx FIFO 8 **0x9: TXFIFO9 :** Tx FIFO 9
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

24.1.101 USBHS_DWC_otg_intreg_DIEPCTL7 (continued)

0x1: ACTIVE :

STALL All Active Tokens

0x0: INACTIVE :

STALL All non-active tokens

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0

0x2: BULK :

Bulk

0x0: CONTROL :

Control

0x3: INTERRUP :

Interrupt

0x1: ISOCHRONOUS :

Isochronous

17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

0x1: NAK :

The core is transmitting NAK handshakes on this endpoint

0x0: NONNAK :

The core is transmitting non-NAK handshakes based on the FIFO status

24.1.101 USBHS_DWC_otg_intreg_DIEPCTL7 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. - 1'b0: Even (micro)frame - 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Default Value: 0x0 **0x0: DATA0EVENFRM :** DATA0 or Even Frame **0x1: DATA1ODDFRM :** DATA1 or Odd Frame
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical end-point. This value is in bytes. Default Value: 0x0

24.1.102 USBHS_DWC_otg_intreg_DIEPINT7

Description: This register contains the interrupts for the IN Endpoint 7 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	TxFEmp	INEPNakEff	INTknEP-Mis	INTknTX-FEmp	TimeOUT	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	Reserved	RW	RW
HW Access	Reserved					Reserved		
Name	Reserved	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt

24.1.102 USBHS_DWC_otg_intreg_DIEPINT7 (continued)

		0x0: INACTIVE : No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Default Value: 0x0 **0x1: ACTIVE :** BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	TxfifoUndrn	Fifo Underrun (TxfifoUndrn) Applies to IN endpoints Only This bit is valid only If thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** TxFIFO Underrun interrupt **0x0: INACTIVE :** No Tx FIFO Underrun interrupt

24.1.102 USBHS_DWC_otg_intreg_DIEPINT7 (continued)

7	TxFEmp	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)). Default Value: 0x1 **0x1: ACTIVE :** Transmit FIFO Empty interrupt **0x0: INACTIVE :** No Transmit FIFO Empty interrupt
6	INEPNakEff	IN Endpoint NAK Effective (INEPNakEff) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCT-Ln.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. Default Value: 0x0 **0x1: ACTIVE :** IN Endpoint NAK Effective interrupt **0x0: INACTIVE :** No Endpoint NAK Effective interrupt
5	INTknEPMis	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received with EP Mismatch interrupt **0x0: INACTIVE :** No IN Token Received with EP Mismatch interrupt
4	INTknTXFEmp	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received Interrupt

24.1.102 USBHS_DWC_otg_intreg_DIEPINT7 (continued)

		0x0: INACTIVE : No IN Token Received interrupt
3	TimeOUT	Timeout Condition (TimeOUT) - In shared TX FIFO mode, applies to non-isochronous IN endpoints only. - In dedicated FIFO mode, applies only to Control IN endpoints. - In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Timeout interrupt **0x0: INACTIVE :** No Timeout interrupt
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt
0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0

24.1.102 USBHS_DWC_otg_intreg_DIEPINT7 (continued)

0x1: ACTIVE :

Transfer Complete Interrupt

0x0: INACTIVE :

No Transfer Complete Interrupt

24.1.103 USBHS_DWC_otg_intreg_DIEPTSIZ7

Description: This register reflects the Transfer Size of the IN Endpoint 7 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW		RW				
HW Access	Reserved							
Name	Reserved	MC [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	MC	MC Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetchfor an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp) Default Value: 0x0 **0x1: PACKETONE :** 1 packet **0x3: PACKETTHREE :** 3 packets **0x2: PACKETTWO :** 2 packets

24.1.103 USBHS_DWC_otg_intreg_DIEPTSIZ7 (continued)

28 : 19	PktCnt	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO. Default Value: 0x0

24.1.104 USBHS_DWC_otg_intreg_DIEPDMA7

Description: This register contains the DMA Address for the IN Endpoint 7 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.105 USBHS_DWC_otg_intreg_DTXFSTS7

Description: This register reflects the status of the IN Endpoint Transmit FIFO Status Register 7 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009F8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	INEPTxFSpcAvail	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. - 16'h0: Endpoint TxFIFO is full - 16'h1: 1 word available - 16'h2: 2 words available - 16'hn: n words available (where 0 n 32,768) - 16'h8000: 32,768 words available - Others: Reserved In DRD configurations (OTG_MODE = 0, 1, or 2) with dynamic fifo sizing feature enabled (OTG_DFIFO_DYNAMIC=1), the value of this field is, - the maximum value of (OTG_TX_HNPERIO_DFIFO_DEPTH, OTG_TX_DINEP_DFIFO_DEPTH_0) during reset, and - OTG_TX_DINEP_DFIFO_DEPTH_0, immediately after reset deassertion Default Value: 0x100

24.1.106 USBHS_DWC_otg_intreg_DIEPDMAB7

Description: This register contains the DMA Buffer Address of the IN Endpoint 7 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x449009FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.107 USBHS_DWC_otg_intreg_DIEPCTL8

Description: This register is used to control the characteristics of Endpoint 8. Note: This register exists for an endpoint i if the OT-G_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900A00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	Reserved	RW		R	R
HW Access				Reserved				
Name	TxFNum [23:22]		Stall	Reserved	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	RW	
HW Access								
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled, -- For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. -- For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. - When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: -- For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. -- For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: -- SETUP Phase Done -- Endpoint Disabled -- Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.107 USBHS_DWC_otg_intreg_DIEPCTL8 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	SetD1PID - Set DATA1 PID (SetD1PID) -- Applies to interrupt and bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. -- This field is applicable both for Scatter-Gather DMA mode and non Scatter-Gather DMA mode. - Set odd (micro)Frame (SetOddFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the even and odd (micro)Frame (EO_FrNum) field to odd (micro)Frame. -- This field is not applicable for Scatter-Gather DMA mode. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID **0x1: ENABLED :** Enables Set DATA1 PID
28	SetD0PID	SetD0PID - Set DATA0 PID (SetD0PID) -- Applies to interrupt/bulk IN and OUT endpoints only. -- Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. -- This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)Frame (SetEvenFr) -- Applies to isochronous IN and OUT endpoints only. -- Writing to this field sets the Even/Odd (micro)Frame (EO_FrNum) field to even (micro)Frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID **0x1: ENABLED :** Endpoint Data PID to DATA0)

24.1.107 USBHS_DWC_otg_intreg_DIEPCTL8 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
25 : 22	TxFNum	TxFIFO Number (TxFNum) Shared FIFO Operation non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. - 4'h0: Non-Periodic TxFIFO - Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: These bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints. Default Value: 0x0 **0x0: TXFIFO0 :** Tx FIFO 0 **0x1: TXFIFO1 :** Tx FIFO 1 **0xa: TXFIFO10 :** Tx FIFO 10 **0xb: TXFIFO11 :** Tx FIFO 11 **0xc: TXFIFO12 :** Tx FIFO 12

24.1.107 USBHS_DWC_otg_intreg_DIEPCTL8 (continued)

		0xd: TXFIFO13 : Tx FIFO 13 **0xe: TXFIFO14 :** Tx FIFO 14 **0xf: TXFIFO15 :** Tx FIFO 15 **0x2: TXFIFO2 :** Tx FIFO 2 **0x3: TXFIFO3 :** Tx FIFO 3 **0x4: TXFIFO4 :** Tx FIFO 4 **0x5: TXFIFO5 :** Tx FIFO 5 **0x6: TXFIFO6 :** Tx FIFO 6 **0x7: TXFIFO7 :** Tx FIFO 7 **0x8: TXFIFO8 :** Tx FIFO 8 **0x9: TXFIFO9 :** Tx FIFO 9
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

24.1.107 USBHS_DWC_otg_intreg_DIEPCTL8 (continued)

0x1: ACTIVE :

STALL All Active Tokens

0x0: INACTIVE :

STALL All non-active tokens

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0

0x2: BULK :

Bulk

0x0: CONTROL :

Control

0x3: INTERRUP :

Interrupt

0x1: ISOCHRONOUS :

Isochronous

17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0

0x1: NAK :

The core is transmitting NAK handshakes on this endpoint

0x0: NONNAK :

The core is transmitting non-NAK handshakes based on the FIFO status

24.1.107 USBHS_DWC_otg_intreg_DIEPCTL8 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. - 1'b0: Even (micro)frame - 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Default Value: 0x0 **0x0: DATA0EVENFRM :** DATA0 or Even Frame **0x1: DATA1ODDFRM :** DATA1 or Odd Frame
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical end-point. This value is in bytes. Default Value: 0x0

24.1.108 USBHS_DWC_otg_intreg_DIEPINT8

Description: This register contains the interrupts for the IN Endpoint 8 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900A08

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access								
Name	TxFEmp	INEPNakEff	INTknEP-Mis	INTknTX-FEmp	TimeOUT	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW	RW	RW	RW	Reserved	RW	RW
HW Access	Reserved					Reserved		
Name	Reserved	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt

24.1.108 USBHS_DWC_otg_intreg_DIEPINT8 (continued)

		0x0: INACTIVE : No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Default Value: 0x0 **0x1: ACTIVE :** BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	TxfifoUndrn	Fifo Underrun (TxfifoUndrn) Applies to IN endpoints Only This bit is valid only If thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** TxFIFO Underrun interrupt **0x0: INACTIVE :** No Tx FIFO Underrun interrupt

24.1.108 USBHS_DWC_otg_intreg_DIEPINT8 (continued)

7	TxFEmp	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)). Default Value: 0x1 **0x1: ACTIVE :** Transmit FIFO Empty interrupt **0x0: INACTIVE :** No Transmit FIFO Empty interrupt
6	INEPNakEff	IN Endpoint NAK Effective (INEPNakEff) Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCT-Ln.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. Default Value: 0x0 **0x1: ACTIVE :** IN Endpoint NAK Effective interrupt **0x0: INACTIVE :** No Endpoint NAK Effective interrupt
5	INTknEPMis	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received with EP Mismatch interrupt **0x0: INACTIVE :** No IN Token Received with EP Mismatch interrupt
4	INTknTXFEmp	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. Default Value: 0x0 **0x1: ACTIVE :** IN Token Received Interrupt

24.1.108 USBHS_DWC_otg_intreg_DIEPINT8 (continued)

		0x0: INACTIVE : No IN Token Received interrupt
3	TimeOUT	Timeout Condition (TimeOUT) - In shared TX FIFO mode, applies to non-isochronous IN endpoints only. - In dedicated FIFO mode, applies only to Control IN endpoints. - In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Timeout interrupt **0x0: INACTIVE :** No Timeout interrupt
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt
0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0

24.1.108 USBHS_DWC_otg_intreg_DIEPINT8 (continued)

0x1: ACTIVE :

Transfer Complete Interrupt

0x0: INACTIVE :

No Transfer Complete Interrupt

24.1.109 USBHS_DWC_otg_intreg_DIEPTSIZ8

Description: This register reflects the Transfer Size of the IN Endpoint 8 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900A10

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW		RW				
HW Access	Reserved							
Name	Reserved	MC [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	MC	MC Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetchfor an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp) Default Value: 0x0 **0x1: PACKETONE :** 1 packet **0x3: PACKETTHREE :** 3 packets **0x2: PACKETTWO :** 2 packets

24.1.109 USBHS_DWC_otg_intreg_DIEPTSIZ8 (continued)

28 : 19	PktCnt	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO. Default Value: 0x0

24.1.110 USBHS_DWC_otg_intreg_DIEPDMA8

Description: This register contains the DMA Address for the IN Endpoint 8 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900A14

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.111 USBHS_DWC_otg_intreg_DTXFSTS8

Description: This register reflects the status of the IN Endpoint Transmit FIFO Status Register 8 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900A18

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	INEPTxFSpcAvail [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	INEPTxFSpcAvail	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. - 16'h0: Endpoint TxFIFO is full - 16'h1: 1 word available - 16'h2: 2 words available - 16'hn: n words available (where 0 n 32,768) - 16'h8000: 32,768 words available - Others: Reserved In DRD configurations (OTG_MODE = 0, 1, or 2) with dynamic fifo sizing feature enabled (OTG_DFIFO_DYNAMIC=1), the value of this field is, - the maximum value of (OTG_TX_HNPERIO_DFIFO_DEPTH, OTG_TX_DINEP_DFIFO_DEPTH_0) during reset, and - OTG_TX_DINEP_DFIFO_DEPTH_0, immediately after reset deassertion Default Value: 0x100

24.1.112 USBHS_DWC_otg_intreg_DIEPDMAB8

Description: This register contains the DMA Buffer Address of the IN Endpoint 8 of the Device controller. Note: This register exists for an endpoint i if the OTG_EP_DIR_i parameter is 0 or 1 for that endpoint.

Address: 0x44900A1C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.113 USBHS_DWC_otg_intreg_DOEPCTL0

Description: This register is used to control the characteristics of the OUT Endpoint 0 of the Device controller.

Address: 0x44900B00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	
HW Access	Reserved							
Name	Reserved [7:2]						MPS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R	Reserved						
HW Access		Reserved						
Name	USBActEP	Reserved [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW	RW	R		R	Reserved
HW Access	Reserved							Reserved
Name	Reserved [23:22]		Stall	Snp	EPType [19:18]		NAKSts	Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	Reserved		W	W	Reserved	
HW Access			Reserved				Reserved	
Name	EPEna	EPDis	Reserved [29:28]		SNAK	CNAK	Reserved [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) - When Scatter/Gather DMA mode is enabled, for OUT endpoints this bit indicates that the descriptor structure and data buffer to receive data is setup. - When Scatter/Gather DMA mode is disabled (such as for buffer-pointer based DMA mode)this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: -- SETUP Phase Done -- Endpoint Disabled -- Transfer Completed Note: In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory and it will not be cleared on Transfer Completed interrupt of SETUP packet. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No action
30	EPDis	Endpoint Disable (EPDis) The application cannot disable control OUT endpoint 0. Default Value: 0x0

24.1.113 USBHS_DWC_otg_intreg_DOEPCTL0 (continued)

		0x0: INACTIVE : No Endpoint disable
27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint. Default Value: 0x0 **0x0: NOSET :** No action **0x1: SET :** Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: CLEAR :** Clear NAK **0x0: NOCLEAR :** No action
21	Stall	STALL Handshake (Stall) The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is Set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** Stall Handshake **0x0: INACTIVE :** No Stall
20	Snp	RESERVED Default Value: 0x0 **0x0: RESERVED0SnpDOEPCTL0 :** Reserved 0 **0x1: RESERVED1SnpDOEPCTL0 :** Reserved 1
19 : 18	EPType	Endpoint Type (EPType) Hardcoded to 2'b00 for control. Default Value: 0x0

24.1.113 USBHS_DWC_otg_intreg_DOEPCTL0 (continued)

		0x0: ACTIVE : Endpoint Control 0
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even If there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** The core is transmitting NAK handshakes on this endpoint **0x0: INACTIVE :** The core is transmitting non-NAK handshakes based on the FIFO status
15	USBActEP	USB Active Endpoint (USBActEP) This bit is always set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces. Default Value: 0x1 **0x1: ACTIVE :** USB Active Endpoint 0
1 : 0	MPS	Maximum Packet Size (MPS) The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. - 2'b00: 64 bytes - 2'b01: 32 bytes - 2'b10: 16 bytes - 2'b11: 8 bytes Default Value: 0x0 **0x2: BYTE16 :** 16 bytes **0x1: BYTE32 :** 32 bytes **0x0: BYTE64 :** 64 bytes **0x3: BYTE8 :** 8 bytes

24.1.114 USBHS_DWC_otg_intreg_DOEPINT0

Description: This register contains the interrupts for the OUT Endpoint 0 of the Device controller.

Address: 0x44900B08

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	Back2Back-SETup	StsPhseRc-vd	OUTTknEP-dis	SetUp	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved	RW	RW
HW Access						Reserved		
Name	StupPktRc-vd	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	OutPktErr

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	StupPktRcvd	Setup Packet Received Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the controller, this bit indicates that this buffer holds 8 bytes of setup data. There is only one Setup packet per buffer. On receiving a Setup packet, the controller closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behavior, the controller can receive any number of back to back setup packets and one buffer for every setup packet is used. - 1'b0: No Setup packet received - 1'b1: Setup packet received Reset: 1'b0 Default Value: 0x0 **0x0: NOT_RCVD :** No Setup packet received **0x1: RCVD :** Setup packet received

24.1.114 USBHS_DWC_otg_intreg_DOEPINT0 (continued)

14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt **0x0: INACTIVE :** No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No BbleErr interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the core to process, such as Host busy or DMA done. Default Value: 0x0

24.1.114 USBHS_DWC_otg_intreg_DOEPINT0 (continued)

		0x1: ACTIVE : BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	OutPktErr	OUT Packet Error (OutPktErr) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet. Default Value: 0x0 **0x1: ACTIVE :** OUT Packet Error **0x0: INACTIVE :** No OUT Packet Error
6	Back2BackSETup	Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt, Default Value: 0x0 **0x1: ACTIVE :** Back-to-Back SETUP Packets Received **0x0: INACTIVE :** No Back-to-Back SETUP Packets Received
5	StsPhseRcvd	Status Phase Received for Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in case of Scatter Gather DMA mode. Default Value: 0x0 **0x1: ACTIVE :** Status Phase Received for Control Write **0x0: INACTIVE :** No Status Phase Received for Control Write

24.1.114 USBHS_DWC_otg_intreg_DOEPINT0 (continued)

4	OUTTknEPdis	OUT Token Received When Endpoint Disabled (OUTTknEPdis) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received. Default Value: 0x0 **0x1: ACTIVE :** OUT Token Received When Endpoint Disabled **0x0: INACTIVE :** No OUT Token Received When Endpoint Disabled
3	SetUp	SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet. Default Value: 0x0 **0x1: ACTIVE :** SETUP Phase Done **0x0: INACTIVE :** No SETUP Phase Done
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" section in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt

24.1.114 USBHS_DWC_otg_intreg_DOEPINT0 (continued)

0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled - For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. - For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. Note: In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Transfer Complete Interrupt **0x0: INACTIVE :** No Transfer Complete Interrupt

24.1.115 USBHS_DWC_otg_intreg_DOEPTSIZ0

Description: This register contains the Transfer Size for the OUT Endpoint 0 of the Device controller.

Address: 0x44900B10

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved							
Name	Reserved	XferSize [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW	Reserved		
HW Access	Reserved					Reserved		
Name	Reserved [23:20]				PktCnt	Reserved [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW		Reserved				
HW Access	Reserved			Reserved				
Name	Reserved	SUPCnt [30:29]		Reserved [28:24]				

Bits	Name	Description
30 : 29	SUPCnt	SETUP Packet Count (SUPCnt) This field specifies the number of back-to-back SETUP data packets the endpoint can receive. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets Default Value: 0x0 **0x1: ONEPACKET :** 1 packet **0x3: THREEPACKET :** 3 packets **0x2: TWOPACKET :** 2 packets
19	PktCnt	Packet Count (PktCnt) This field is decremented to zero after a packet is written into the RxFIFO. Default Value: 0x0

24.1.115 USBHS_DWC_otg_intreg_DOEPTSIZ0 (continued)

6 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory. Default Value: 0x0

24.1.116 USBHS_DWC_otg_intreg_DOEPDMA0

Description: This register contains the DMA Address for the OUT Endpoint 0 of the Device controller.

Address: 0x44900B14

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.117 USBHS_DWC_otg_intreg_DOEPDMAB0

Description: This register contains the DMA Buffer Address for the OUT Endpoint 0 of the Device controller.

Address: 0x44900B1C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.118 USBHS_DWC_otg_intreg_DOEPCTL1

Description: This register is used to control the characteristics of OUT Endpoint 1 of the Device controller.

Address: 0x44900B20

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW	RW	RW		R	R
HW Access	Reserved							
Name	Reserved [23:22]		Stall	Snp	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	Reserved	
HW Access							Reserved	
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	Reserved [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, - For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. - For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Completed Note: For control endpoints in DMA mode, this bit must be set for the controller to transfer SETUP data packets to the memory. This bit will not be cleared on Transfer Completed interrupt of the SETUP packet. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.118 USBHS_DWC_otg_intreg_DOEPCTL1 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	Set DATA1 PID (SetD1PID) - Applies to interrupt and bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. - This field is applicable both for scatter-gather DMA mode and non scatter-gather DMA mode. Reset: 1'b0 Set Odd (micro)frame (SetOddFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the even and odd (micro)frame (EO_FrNum) field to odd (micro)frame. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID or Do not force Odd Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA1 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame
28	SetD0PID	Set DATA0 PID (SetD0PID) - Applies to interrupt/bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. - This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to even (micro)frame. - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID or Do not force Even Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA0 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame

24.1.118 USBHS_DWC_otg_intreg_DOEPCTL1 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
20	Snp	RESERVED Default Value: 0x0 **0x0: RESERVED0SnpDOEPCTL1 :** Reserved 0 **0x1: RESERVED1SnpDOEPCTL1 :** Reserved 1

24.1.118 USBHS_DWC_otg_intreg_DOEPCTL1 (continued)

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUPT :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.118 USBHS_DWC_otg_intreg_DOEPCTL1 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable for both Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: - Applies to isochronous IN and OUT endpoints only. - Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. -- 1'b0: Even (micro)frame -- 1'b1: Odd (micro)frame - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x1: ACTIVE :** Endpoint Data PID active **0x0: INACTIVE :** Endpoint Data PID not active
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes. Default Value: 0x0

24.1.119 USBHS_DWC_otg_intreg_DOEPINT1

Description: This register contains the interrupts for the OUT Endpoint 1 of the Device controller.

Address: 0x44900B28

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	Back2Back-SETup	StsPhseRc-vd	OUTTknEP-dis	SetUp	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved	RW	RW
HW Access						Reserved		
Name	StupPktRc-vd	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	OutPktErr

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	StupPktRcvd	Setup Packet Received Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the controller, this bit indicates that this buffer holds 8 bytes of setup data. There is only one Setup packet per buffer. On receiving a Setup packet, the controller closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behavior, the controller can receive any number of back to back setup packets and one buffer for every setup packet is used. - 1'b0: No Setup packet received - 1'b1: Setup packet received Reset: 1'b0 Default Value: 0x0 **0x0: NOT_RCVD :** No Setup packet received **0x1: RCVD :** Setup packet received

24.1.119 USBHS_DWC_otg_intreg_DOEPINT1 (continued)

14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt **0x0: INACTIVE :** No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No BbleErr interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done Default Value: 0x0

24.1.119 USBHS_DWC_otg_intreg_DOEPINT1 (continued)

		0x1: ACTIVE : BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	OutPktErr	OUT Packet Error (OutPktErr) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet. Default Value: 0x0 **0x1: ACTIVE :** OUT Packet Error **0x0: INACTIVE :** No OUT Packet Error
6	Back2BackSETup	Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt, Default Value: 0x0 **0x1: ACTIVE :** Back-to-Back SETUP Packets Received **0x0: INACTIVE :** No Back-to-Back SETUP Packets Received
5	StsPhseRcvd	Status Phase Received for Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode. Default Value: 0x0 **0x1: ACTIVE :** Status Phase Received for Control Write **0x0: INACTIVE :** No Status Phase Received for Control Write
4	OUTTknEPdis	OUT Token Received When Endpoint Disabled (OUTTknEPdis) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received. Default Value: 0x0

24.1.119 USBHS_DWC_otg_intreg_DOEPINT1 (continued)

		0x1: ACTIVE : OUT Token Received When Endpoint Disabled **0x0: INACTIVE :** No OUT Token Received When Endpoint Disabled
3	SetUp	SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet. Default Value: 0x0 **0x1: ACTIVE :** SETUP Phase Done **0x0: INACTIVE :** No SETUP Phase Done
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" section in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt

24.1.119 USBHS_DWC_otg_intreg_DOEPINT1 (continued)

0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Transfer Complete Interrupt **0x0: INACTIVE :** No Transfer Complete Interrupt

24.1.120 USBHS_DWC_otg_intreg_DOEPTSIZ1

Description: This register contains the Transfer Size for the OUT Endpoint 1 of the Device controller.

Address: 0x44900B30

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R		RW				
HW Access	Reserved							
Name	Reserved	RxDPID [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	RxDPID	RxDPID Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. - 2'b00: DATA0 - 2'b01: DATA2 - 2'b10: DATA1 - 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets Default Value: 0x0 **0x0: DATA0 :** DATA0 **0x2: DATA1PACKET2 :** DATA1 or 2 packets

24.1.120 USBHS_DWC_otg_intreg_DOEPTSIZ1 (continued)

		0x1: DATA2PACKET1 : DATA2 or 1 packet **0x3: MDATAPACKET3 :** MDATA or 3 packets
28 : 19	PktCnt	Packet Count (PktCnt) This field is decremented to zero after a packet is written into the RxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory. Default Value: 0x0

24.1.121 USBHS_DWC_otg_intreg_DOEPDMA1

Description: This register contains the DMA Address for the OUT Endpoint 1 of the Device controller.

Address: 0x44900B34

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.122 USBHS_DWC_otg_intreg_DOEPDMAB1

Description: This register contains the DMA Buffer Address for the OUT Endpoint 1 of the Device controller.

Address: 0x44900B3C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.123 USBHS_DWC_otg_intreg_DOEPCTL2

Description: This register is used to control the characteristics of OUT Endpoint 2 of the Device controller.

Address: 0x44900B40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW	RW	RW		R	R
HW Access	Reserved							
Name	Reserved [23:22]		Stall	Snp	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	Reserved	
HW Access							Reserved	
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	Reserved [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, - For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. - For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Completed Note: For control endpoints in DMA mode, this bit must be set for the controller to transfer SETUP data packets to the memory. This bit will not be cleared on Transfer Completed interrupt of the SETUP packet. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.123 USBHS_DWC_otg_intreg_DOEPCTL2 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	Set DATA1 PID (SetD1PID) - Applies to interrupt and bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. - This field is applicable both for scatter-gather DMA mode and non scatter-gather DMA mode. Reset: 1'b0 Set Odd (micro)frame (SetOddFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the even and odd (micro)frame (EO_FrNum) field to odd (micro)frame. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID or Do not force Odd Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA1 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame
28	SetD0PID	Set DATA0 PID (SetD0PID) - Applies to interrupt/bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. - This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to even (micro)frame. - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID or Do not force Even Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA0 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame

24.1.123 USBHS_DWC_otg_intreg_DOEPCTL2 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
20	Snp	RESERVED Default Value: 0x0 **0x0: RESERVED0SnpDOEPCTL2 :** Reserved 0 **0x1: RESERVED1SnpDOEPCTL2 :** Reserved 1

24.1.123 USBHS_DWC_otg_intreg_DOEPCTL2 (continued)

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUPT :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.123 USBHS_DWC_otg_intreg_DOEPCTL2 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable for both Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: - Applies to isochronous IN and OUT endpoints only. - Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. -- 1'b0: Even (micro)frame -- 1'b1: Odd (micro)frame - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x1: ACTIVE :** Endpoint Data PID active **0x0: INACTIVE :** Endpoint Data PID not active
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes. Default Value: 0x0

24.1.124 USBHS_DWC_otg_intreg_DOEPINT2

Description: This register contains the interrupts for the OUT Endpoint 2 of the Device controller.

Address: 0x44900B48

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	Back2Back-SETup	StsPhseRc-vd	OUTTknEP-dis	SetUp	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved	RW	RW
HW Access						Reserved		
Name	StupPktRc-vd	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	OutPktErr

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	StupPktRcvd	Setup Packet Received Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the controller, this bit indicates that this buffer holds 8 bytes of setup data. There is only one Setup packet per buffer. On receiving a Setup packet, the controller closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behavior, the controller can receive any number of back to back setup packets and one buffer for every setup packet is used. - 1'b0: No Setup packet received - 1'b1: Setup packet received Reset: 1'b0 Default Value: 0x0 **0x0: NOT_RCVD :** No Setup packet received **0x1: RCVD :** Setup packet received

24.1.124 USBHS_DWC_otg_intreg_DOEPINT2 (continued)

14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt **0x0: INACTIVE :** No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No BbleErr interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done Default Value: 0x0

24.1.124 USBHS_DWC_otg_intreg_DOEPINT2 (continued)

		0x1: ACTIVE : BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	OutPktErr	OUT Packet Error (OutPktErr) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet. Default Value: 0x0 **0x1: ACTIVE :** OUT Packet Error **0x0: INACTIVE :** No OUT Packet Error
6	Back2BackSETup	Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt, Default Value: 0x0 **0x1: ACTIVE :** Back-to-Back SETUP Packets Received **0x0: INACTIVE :** No Back-to-Back SETUP Packets Received
5	StsPhseRcvd	Status Phase Received for Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode. Default Value: 0x0 **0x1: ACTIVE :** Status Phase Received for Control Write **0x0: INACTIVE :** No Status Phase Received for Control Write
4	OUTTknEPdis	OUT Token Received When Endpoint Disabled (OUTTknEPdis) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received. Default Value: 0x0

24.1.124 USBHS_DWC_otg_intreg_DOEPINT2 (continued)

		0x1: ACTIVE : OUT Token Received When Endpoint Disabled **0x0: INACTIVE :** No OUT Token Received When Endpoint Disabled
3	SetUp	SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet. Default Value: 0x0 **0x1: ACTIVE :** SETUP Phase Done **0x0: INACTIVE :** No SETUP Phase Done
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" section in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt

24.1.124 USBHS_DWC_otg_intreg_DOEPINT2 (continued)

0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Transfer Complete Interrupt **0x0: INACTIVE :** No Transfer Complete Interrupt

24.1.125 USBHS_DWC_otg_intreg_DOEPTSIZ2

Description: This register contains the Transfer Size for the OUT Endpoint 2 of the Device controller.

Address: 0x44900B50

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R		RW				
HW Access	Reserved							
Name	Reserved	RxDPID [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	RxDPID	RxDPID Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. - 2'b00: DATA0 - 2'b01: DATA2 - 2'b10: DATA1 - 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets Default Value: 0x0 **0x0: DATA0 :** DATA0 **0x2: DATA1PACKET2 :** DATA1 or 2 packets

24.1.125 USBHS_DWC_otg_intreg_DOEPTSIZ2 (continued)

		0x1: DATA2PACKET1 : DATA2 or 1 packet **0x3: MDATAPACKET3 :** MDATA or 3 packets
28 : 19	PktCnt	Packet Count (PktCnt) This field is decremented to zero after a packet is written into the RxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory. Default Value: 0x0

24.1.126 USBHS_DWC_otg_intreg_DOEPDMA2

Description: This register contains the DMA Address for the OUT Endpoint 2 of the Device controller.

Address: 0x44900B54

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.127 USBHS_DWC_otg_intreg_DOEPDMAB2

Description: This register contains the DMA Buffer Address for the OUT Endpoint 2 of the Device controller.

Address: 0x44900B5C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.128 USBHS_DWC_otg_intreg_DOEPCTL3

Description: This register is used to control the characteristics of OUT Endpoint 3 of the Device controller.

Address: 0x44900B60

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW	RW	RW		R	R
HW Access	Reserved							
Name	Reserved [23:22]		Stall	Snp	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	Reserved	
HW Access							Reserved	
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	Reserved [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, - For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. - For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Completed Note: For control endpoints in DMA mode, this bit must be set for the controller to transfer SETUP data packets to the memory. This bit will not be cleared on Transfer Completed interrupt of the SETUP packet. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.128 USBHS_DWC_otg_intreg_DOEPCTL3 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	Set DATA1 PID (SetD1PID) - Applies to interrupt and bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. - This field is applicable both for scatter-gather DMA mode and non scatter-gather DMA mode. Reset: 1'b0 Set Odd (micro)frame (SetOddFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the even and odd (micro)frame (EO_FrNum) field to odd (micro)frame. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID or Do not force Odd Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA1 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame
28	SetD0PID	Set DATA0 PID (SetD0PID) - Applies to interrupt/bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. - This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to even (micro)frame. - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID or Do not force Even Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA0 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame

24.1.128 USBHS_DWC_otg_intreg_DOEPCTL3 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
20	Snp	RESERVED Default Value: 0x0 **0x0: RESERVED0SnpDOEPCTL3 :** Reserved 0 **0x1: RESERVED1SnpDOEPCTL3 :** Reserved 1

24.1.128 USBHS_DWC_otg_intreg_DOEPCTL3 (continued)

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUPT :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.128 USBHS_DWC_otg_intreg_DOEPCTL3 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable for both Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: - Applies to isochronous IN and OUT endpoints only. - Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. -- 1'b0: Even (micro)frame -- 1'b1: Odd (micro)frame - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x1: ACTIVE :** Endpoint Data PID active **0x0: INACTIVE :** Endpoint Data PID not active
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes. Default Value: 0x0

24.1.129 USBHS_DWC_otg_intreg_DOEPINT3

Description: This register contains the interrupts for the OUT Endpoint 3 of the Device controller.

Address: 0x44900B68

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	Back2Back-SETup	StsPhseRc-vd	OUTTknEP-dis	SetUp	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved	RW	RW
HW Access						Reserved		
Name	StupPktRc-vd	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	OutPktErr

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	StupPktRcvd	Setup Packet Received Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the controller, this bit indicates that this buffer holds 8 bytes of setup data. There is only one Setup packet per buffer. On receiving a Setup packet, the controller closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behavior, the controller can receive any number of back to back setup packets and one buffer for every setup packet is used. - 1'b0: No Setup packet received - 1'b1: Setup packet received Reset: 1'b0 Default Value: 0x0 **0x0: NOT_RCVD :** No Setup packet received **0x1: RCVD :** Setup packet received

24.1.129 USBHS_DWC_otg_intreg_DOEPINT3 (continued)

14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt **0x0: INACTIVE :** No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No BbleErr interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done Default Value: 0x0

24.1.129 USBHS_DWC_otg_intreg_DOEPINT3 (continued)

		0x1: ACTIVE : BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	OutPktErr	OUT Packet Error (OutPktErr) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet. Default Value: 0x0 **0x1: ACTIVE :** OUT Packet Error **0x0: INACTIVE :** No OUT Packet Error
6	Back2BackSETup	Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt, Default Value: 0x0 **0x1: ACTIVE :** Back-to-Back SETUP Packets Received **0x0: INACTIVE :** No Back-to-Back SETUP Packets Received
5	StsPhseRcvd	Status Phase Received for Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode. Default Value: 0x0 **0x1: ACTIVE :** Status Phase Received for Control Write **0x0: INACTIVE :** No Status Phase Received for Control Write
4	OUTTknEPdis	OUT Token Received When Endpoint Disabled (OUTTknEPdis) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received. Default Value: 0x0

24.1.129 USBHS_DWC_otg_intreg_DOEPINT3 (continued)

		0x1: ACTIVE : OUT Token Received When Endpoint Disabled **0x0: INACTIVE :** No OUT Token Received When Endpoint Disabled
3	SetUp	SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet. Default Value: 0x0 **0x1: ACTIVE :** SETUP Phase Done **0x0: INACTIVE :** No SETUP Phase Done
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" section in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt

24.1.129 USBHS_DWC_otg_intreg_DOEPINT3 (continued)

0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Transfer Complete Interrupt **0x0: INACTIVE :** No Transfer Complete Interrupt

24.1.130 USBHS_DWC_otg_intreg_DOEPTSIZ3

Description: This register contains the Transfer Size for the OUT Endpoint 3 of the Device controller.

Address: 0x44900B70

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R		RW				
HW Access	Reserved							
Name	Reserved	RxDPID [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	RxDPID	RxDPID Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. - 2'b00: DATA0 - 2'b01: DATA2 - 2'b10: DATA1 - 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets Default Value: 0x0 **0x0: DATA0 :** DATA0 **0x2: DATA1PACKET2 :** DATA1 or 2 packets

24.1.130 USBHS_DWC_otg_intreg_DOEPTSIZ3 (continued)

		0x1: DATA2PACKET1 : DATA2 or 1 packet **0x3: MDATAPACKET3 :** MDATA or 3 packets
28 : 19	PktCnt	Packet Count (PktCnt) This field is decremented to zero after a packet is written into the RxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory. Default Value: 0x0

24.1.131 USBHS_DWC_otg_intreg_DOEPDMA3

Description: This register contains the DMA Address for the OUT Endpoint 3 of the Device controller.

Address: 0x44900B74

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.132 USBHS_DWC_otg_intreg_DOEPDMAB3

Description: This register contains the DMA Buffer Address for the OUT Endpoint 3 of the Device controller.

Address: 0x44900B7C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.133 USBHS_DWC_otg_intreg_DOEPCTL4

Description: This register is used to control the characteristics of OUT Endpoint 4 of the Device controller.

Address: 0x44900B80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW	RW	RW		R	R
HW Access	Reserved							
Name	Reserved [23:22]		Stall	Snp	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	Reserved	
HW Access							Reserved	
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	Reserved [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, - For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. - For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Completed Note: For control endpoints in DMA mode, this bit must be set for the controller to transfer SETUP data packets to the memory. This bit will not be cleared on Transfer Completed interrupt of the SETUP packet. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.133 USBHS_DWC_otg_intreg_DOEPCTL4 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	Set DATA1 PID (SetD1PID) - Applies to interrupt and bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. - This field is applicable both for scatter-gather DMA mode and non scatter-gather DMA mode. Reset: 1'b0 Set Odd (micro)frame (SetOddFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the even and odd (micro)frame (EO_FrNum) field to odd (micro)frame. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID or Do not force Odd Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA1 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame
28	SetD0PID	Set DATA0 PID (SetD0PID) - Applies to interrupt/bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. - This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to even (micro)frame. - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID or Do not force Even Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA0 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame

24.1.133 USBHS_DWC_otg_intreg_DOEPCTL4 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
20	Snp	RESERVED Default Value: 0x0 **0x0: RESERVED0SnpDOEPCTL4 :** Reserved 0 **0x1: RESERVED1SnpDOEPCTL4 :** Reserved 1

24.1.133 USBHS_DWC_otg_intreg_DOEPCTL4 (continued)

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUPT :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.133 USBHS_DWC_otg_intreg_DOEPCTL4 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable for both Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: - Applies to isochronous IN and OUT endpoints only. - Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. -- 1'b0: Even (micro)frame -- 1'b1: Odd (micro)frame - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x1: ACTIVE :** Endpoint Data PID active **0x0: INACTIVE :** Endpoint Data PID not active
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes. Default Value: 0x0

24.1.134 USBHS_DWC_otg_intreg_DOEPINT4

Description: This register contains the interrupts for the OUT Endpoint 4 of the Device controller.

Address: 0x44900B88

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	Back2Back-SETup	StsPhseRc-vd	OUTTknEP-dis	SetUp	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved	RW	RW
HW Access						Reserved		
Name	StupPktRc-vd	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	OutPktErr

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	StupPktRcvd	Setup Packet Received Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the controller, this bit indicates that this buffer holds 8 bytes of setup data. There is only one Setup packet per buffer. On receiving a Setup packet, the controller closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behavior, the controller can receive any number of back to back setup packets and one buffer for every setup packet is used. - 1'b0: No Setup packet received - 1'b1: Setup packet received Reset: 1'b0 Default Value: 0x0 **0x0: NOT_RCVD :** No Setup packet received **0x1: RCVD :** Setup packet received

24.1.134 USBHS_DWC_otg_intreg_DOEPINT4 (continued)

14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt **0x0: INACTIVE :** No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No BbleErr interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done Default Value: 0x0

24.1.134 USBHS_DWC_otg_intreg_DOEPINT4 (continued)

		0x1: ACTIVE : BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	OutPktErr	OUT Packet Error (OutPktErr) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet. Default Value: 0x0 **0x1: ACTIVE :** OUT Packet Error **0x0: INACTIVE :** No OUT Packet Error
6	Back2BackSETup	Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt, Default Value: 0x0 **0x1: ACTIVE :** Back-to-Back SETUP Packets Received **0x0: INACTIVE :** No Back-to-Back SETUP Packets Received
5	StsPhseRcvd	Status Phase Received for Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode. Default Value: 0x0 **0x1: ACTIVE :** Status Phase Received for Control Write **0x0: INACTIVE :** No Status Phase Received for Control Write
4	OUTTknEPdis	OUT Token Received When Endpoint Disabled (OUTTknEPdis) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received. Default Value: 0x0

24.1.134 USBHS_DWC_otg_intreg_DOEPINT4 (continued)

		0x1: ACTIVE : OUT Token Received When Endpoint Disabled **0x0: INACTIVE :** No OUT Token Received When Endpoint Disabled
3	SetUp	SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet. Default Value: 0x0 **0x1: ACTIVE :** SETUP Phase Done **0x0: INACTIVE :** No SETUP Phase Done
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" section in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt

24.1.134 USBHS_DWC_otg_intreg_DOEPINT4 (continued)

0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Transfer Complete Interrupt **0x0: INACTIVE :** No Transfer Complete Interrupt

24.1.135 USBHS_DWC_otg_intreg_DOEPTSIZ4

Description: This register contains the Transfer Size for the OUT Endpoint 4 of the Device controller.

Address: 0x44900B90

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R		RW				
HW Access	Reserved							
Name	Reserved	RxDPID [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	RxDPID	RxDPID Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. - 2'b00: DATA0 - 2'b01: DATA2 - 2'b10: DATA1 - 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets Default Value: 0x0 **0x0: DATA0 :** DATA0 **0x2: DATA1PACKET2 :** DATA1 or 2 packets

24.1.135 USBHS_DWC_otg_intreg_DOEPTSIZ4 (continued)

		0x1: DATA2PACKET1 : DATA2 or 1 packet **0x3: MDATAPACKET3 :** MDATA or 3 packets
28 : 19	PktCnt	Packet Count (PktCnt) This field is decremented to zero after a packet is written into the RxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory. Default Value: 0x0

24.1.136 USBHS_DWC_otg_intreg_DOEPDMA4

Description: This register contains the DMA Address for the OUT Endpoint 4 of the Device controller.

Address: 0x44900B94

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.137 USBHS_DWC_otg_intreg_DOEPDMAB4

Description: This register contains the DMA Buffer Address for the OUT Endpoint 4 of the Device controller.

Address: 0x44900B9C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.138 USBHS_DWC_otg_intreg_DOEPCTL5

Description: This register is used to control the characteristics of OUT Endpoint 5 of the Device controller.

Address: 0x44900BA0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW	RW	RW		R	R
HW Access	Reserved							
Name	Reserved [23:22]		Stall	Snp	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	Reserved	
HW Access							Reserved	
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	Reserved [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, - For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. - For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Completed Note: For control endpoints in DMA mode, this bit must be set for the controller to transfer SETUP data packets to the memory. This bit will not be cleared on Transfer Completed interrupt of the SETUP packet. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.138 USBHS_DWC_otg_intreg_DOEPCTL5 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	Set DATA1 PID (SetD1PID) - Applies to interrupt and bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. - This field is applicable both for scatter-gather DMA mode and non scatter-gather DMA mode. Reset: 1'b0 Set Odd (micro)frame (SetOddFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the even and odd (micro)frame (EO_FrNum) field to odd (micro)frame. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID or Do not force Odd Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA1 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame
28	SetD0PID	Set DATA0 PID (SetD0PID) - Applies to interrupt/bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. - This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to even (micro)frame. - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID or Do not force Even Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA0 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame

24.1.138 USBHS_DWC_otg_intreg_DOEPCTL5 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
20	Snp	RESERVED Default Value: 0x0 **0x0: RESERVED0SnpDOEPCTL5 :** Reserved 0 **0x1: RESERVED1SnpDOEPCTL5 :** Reserved 1

24.1.138 USBHS_DWC_otg_intreg_DOEPCTL5 (continued)

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUPT :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.138 USBHS_DWC_otg_intreg_DOEPCTL5 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable for both Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: - Applies to isochronous IN and OUT endpoints only. - Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. -- 1'b0: Even (micro)frame -- 1'b1: Odd (micro)frame - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x1: ACTIVE :** Endpoint Data PID active **0x0: INACTIVE :** Endpoint Data PID not active
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes. Default Value: 0x0

24.1.139 USBHS_DWC_otg_intreg_DOEPINT5

Description: This register contains the interrupts for the OUT Endpoint 5 of the Device controller.

Address: 0x44900BA8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	Back2Back-SETup	StsPhseRc-vd	OUTTknEP-dis	SetUp	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved	RW	RW
HW Access						Reserved		
Name	StupPktRc-vd	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	OutPktErr

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	StupPktRcvd	Setup Packet Received Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the controller, this bit indicates that this buffer holds 8 bytes of setup data. There is only one Setup packet per buffer. On receiving a Setup packet, the controller closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behavior, the controller can receive any number of back to back setup packets and one buffer for every setup packet is used. - 1'b0: No Setup packet received - 1'b1: Setup packet received Reset: 1'b0 Default Value: 0x0 **0x0: NOT_RCVD :** No Setup packet received **0x1: RCVD :** Setup packet received

24.1.139 USBHS_DWC_otg_intreg_DOEPINT5 (continued)

14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt **0x0: INACTIVE :** No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No BbleErr interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done Default Value: 0x0

24.1.139 USBHS_DWC_otg_intreg_DOEPINT5 (continued)

		0x1: ACTIVE : BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	OutPktErr	OUT Packet Error (OutPktErr) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet. Default Value: 0x0 **0x1: ACTIVE :** OUT Packet Error **0x0: INACTIVE :** No OUT Packet Error
6	Back2BackSETup	Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt, Default Value: 0x0 **0x1: ACTIVE :** Back-to-Back SETUP Packets Received **0x0: INACTIVE :** No Back-to-Back SETUP Packets Received
5	StsPhseRcvd	Status Phase Received for Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode. Default Value: 0x0 **0x1: ACTIVE :** Status Phase Received for Control Write **0x0: INACTIVE :** No Status Phase Received for Control Write
4	OUTTknEPdis	OUT Token Received When Endpoint Disabled (OUTTknEPdis) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received. Default Value: 0x0

24.1.139 USBHS_DWC_otg_intreg_DOEPINT5 (continued)

		0x1: ACTIVE : OUT Token Received When Endpoint Disabled **0x0: INACTIVE :** No OUT Token Received When Endpoint Disabled
3	SetUp	SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet. Default Value: 0x0 **0x1: ACTIVE :** SETUP Phase Done **0x0: INACTIVE :** No SETUP Phase Done
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" section in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt

24.1.139 USBHS_DWC_otg_intreg_DOEPINT5 (continued)

0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Transfer Complete Interrupt **0x0: INACTIVE :** No Transfer Complete Interrupt

24.1.140 USBHS_DWC_otg_intreg_DOEPTSIZ5

Description: This register contains the Transfer Size for the OUT Endpoint 5 of the Device controller.

Address: 0x44900BB0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R		RW				
HW Access	Reserved							
Name	Reserved	RxDPID [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	RxDPID	RxDPID Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. - 2'b00: DATA0 - 2'b01: DATA2 - 2'b10: DATA1 - 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets Default Value: 0x0 **0x0: DATA0 :** DATA0 **0x2: DATA1PACKET2 :** DATA1 or 2 packets

24.1.140 USBHS_DWC_otg_intreg_DOEPTSIZ5 (continued)

		0x1: DATA2PACKET1 : DATA2 or 1 packet **0x3: MDATAPACKET3 :** MDATA or 3 packets
28 : 19	PktCnt	Packet Count (PktCnt) This field is decremented to zero after a packet is written into the RxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory. Default Value: 0x0

24.1.141 USBHS_DWC_otg_intreg_DOEPDMA5

Description: This register contains the DMA Address for the OUT Endpoint 5 of the Device controller.

Address: 0x44900BB4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.142 USBHS_DWC_otg_intreg_DOEPDMAB5

Description: This register contains the DMA Buffer Address for the OUT Endpoint 5 of the Device controller.

Address: 0x44900BBC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.143 USBHS_DWC_otg_intreg_DOEPCTL6

Description: This register is used to control the characteristics of OUT Endpoint 6 of the Device controller.

Address: 0x44900BC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW	RW	RW		R	R
HW Access	Reserved							
Name	Reserved [23:22]		Stall	Snp	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	Reserved	
HW Access							Reserved	
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	Reserved [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, - For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. - For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Completed Note: For control endpoints in DMA mode, this bit must be set for the controller to transfer SETUP data packets to the memory. This bit will not be cleared on Transfer Completed interrupt of the SETUP packet. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.143 USBHS_DWC_otg_intreg_DOEPCTL6 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	Set DATA1 PID (SetD1PID) - Applies to interrupt and bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. - This field is applicable both for scatter-gather DMA mode and non scatter-gather DMA mode. Reset: 1'b0 Set Odd (micro)frame (SetOddFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the even and odd (micro)frame (EO_FrNum) field to odd (micro)frame. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID or Do not force Odd Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA1 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame
28	SetD0PID	Set DATA0 PID (SetD0PID) - Applies to interrupt/bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. - This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to even (micro)frame. - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID or Do not force Even Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA0 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame

24.1.143 USBHS_DWC_otg_intreg_DOEPCTL6 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
20	Snp	RESERVED Default Value: 0x0 **0x0: RESERVED0SnpDOEPCTL6 :** Reserved 0 **0x1: RESERVED1SnpDOEPCTL6 :** Reserved 1

24.1.143 USBHS_DWC_otg_intreg_DOEPCTL6 (continued)

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUPT :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.143 USBHS_DWC_otg_intreg_DOEPCTL6 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable for both Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: - Applies to isochronous IN and OUT endpoints only. - Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. -- 1'b0: Even (micro)frame -- 1'b1: Odd (micro)frame - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x1: ACTIVE :** Endpoint Data PID active **0x0: INACTIVE :** Endpoint Data PID not active
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes. Default Value: 0x0

24.1.144 USBHS_DWC_otg_intreg_DOEPINT6

Description: This register contains the interrupts for the OUT Endpoint 6 of the Device controller.

Address: 0x44900BC8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	Back2Back-SETup	StsPhseRc-vd	OUTTknEP-dis	SetUp	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved	RW	RW
HW Access						Reserved		
Name	StupPktRc-vd	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	OutPktErr

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	StupPktRcvd	Setup Packet Received Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the controller, this bit indicates that this buffer holds 8 bytes of setup data. There is only one Setup packet per buffer. On receiving a Setup packet, the controller closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behavior, the controller can receive any number of back to back setup packets and one buffer for every setup packet is used. - 1'b0: No Setup packet received - 1'b1: Setup packet received Reset: 1'b0 Default Value: 0x0 **0x0: NOT_RCVD :** No Setup packet received **0x1: RCVD :** Setup packet received

24.1.144 USBHS_DWC_otg_intreg_DOEPINT6 (continued)

14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt **0x0: INACTIVE :** No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No BbleErr interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done Default Value: 0x0

24.1.144 USBHS_DWC_otg_intreg_DOEPINT6 (continued)

		0x1: ACTIVE : BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	OutPktErr	OUT Packet Error (OutPktErr) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet. Default Value: 0x0 **0x1: ACTIVE :** OUT Packet Error **0x0: INACTIVE :** No OUT Packet Error
6	Back2BackSETup	Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt, Default Value: 0x0 **0x1: ACTIVE :** Back-to-Back SETUP Packets Received **0x0: INACTIVE :** No Back-to-Back SETUP Packets Received
5	StsPhseRcvd	Status Phase Received for Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode. Default Value: 0x0 **0x1: ACTIVE :** Status Phase Received for Control Write **0x0: INACTIVE :** No Status Phase Received for Control Write
4	OUTTknEPdis	OUT Token Received When Endpoint Disabled (OUTTknEPdis) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received. Default Value: 0x0

24.1.144 USBHS_DWC_otg_intreg_DOEPINT6 (continued)

		0x1: ACTIVE : OUT Token Received When Endpoint Disabled **0x0: INACTIVE :** No OUT Token Received When Endpoint Disabled
3	SetUp	SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet. Default Value: 0x0 **0x1: ACTIVE :** SETUP Phase Done **0x0: INACTIVE :** No SETUP Phase Done
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" section in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt

24.1.144 USBHS_DWC_otg_intreg_DOEPINT6 (continued)

0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Transfer Complete Interrupt **0x0: INACTIVE :** No Transfer Complete Interrupt

24.1.145 USBHS_DWC_otg_intreg_DOEPTSIZ6

Description: This register contains the Transfer Size for the OUT Endpoint 6 of the Device controller.

Address: 0x44900BD0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R		RW				
HW Access	Reserved							
Name	Reserved	RxDPID [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	RxDPID	RxDPID Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. - 2'b00: DATA0 - 2'b01: DATA2 - 2'b10: DATA1 - 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets Default Value: 0x0 **0x0: DATA0 :** DATA0 **0x2: DATA1PACKET2 :** DATA1 or 2 packets

24.1.145 USBHS_DWC_otg_intreg_DOEPTSIZ6 (continued)

		0x1: DATA2PACKET1 : DATA2 or 1 packet **0x3: MDATAPACKET3 :** MDATA or 3 packets
28 : 19	PktCnt	Packet Count (PktCnt) This field is decremented to zero after a packet is written into the RxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory. Default Value: 0x0

24.1.146 USBHS_DWC_otg_intreg_DOEPDMA6

Description: This register contains the DMA Address for the OUT Endpoint 6 of the Device controller.

Address: 0x44900BD4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.147 USBHS_DWC_otg_intreg_DOEPDMAB6

Description: This register contains the DMA Buffer Address for the OUT Endpoint 6 of the Device controller.

Address: 0x44900BDC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.148 USBHS_DWC_otg_intreg_DOEPCTL7

Description: This register is used to control the characteristics of OUT Endpoint 7 of the Device controller.

Address: 0x44900BE0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW	RW	RW		R	R
HW Access	Reserved							
Name	Reserved [23:22]		Stall	Snp	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	Reserved	
HW Access							Reserved	
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	Reserved [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, - For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. - For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Completed Note: For control endpoints in DMA mode, this bit must be set for the controller to transfer SETUP data packets to the memory. This bit will not be cleared on Transfer Completed interrupt of the SETUP packet. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.148 USBHS_DWC_otg_intreg_DOEPCTL7 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	Set DATA1 PID (SetD1PID) - Applies to interrupt and bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. - This field is applicable both for scatter-gather DMA mode and non scatter-gather DMA mode. Reset: 1'b0 Set Odd (micro)frame (SetOddFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the even and odd (micro)frame (EO_FrNum) field to odd (micro)frame. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID or Do not force Odd Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA1 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame
28	SetD0PID	Set DATA0 PID (SetD0PID) - Applies to interrupt/bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. - This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to even (micro)frame. - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID or Do not force Even Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA0 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame

24.1.148 USBHS_DWC_otg_intreg_DOEPCTL7 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
20	Snp	RESERVED Default Value: 0x0 **0x0: RESERVED0SnpDOEPCTL7 :** Reserved 0 **0x1: RESERVED1SnpDOEPCTL7 :** Reserved 1

24.1.148 USBHS_DWC_otg_intreg_DOEPCTL7 (continued)

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUPT :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.148 USBHS_DWC_otg_intreg_DOEPCTL7 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable for both Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: - Applies to isochronous IN and OUT endpoints only. - Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. -- 1'b0: Even (micro)frame -- 1'b1: Odd (micro)frame - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x1: ACTIVE :** Endpoint Data PID active **0x0: INACTIVE :** Endpoint Data PID not active
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes. Default Value: 0x0

24.1.149 USBHS_DWC_otg_intreg_DOEPINT7

Description: This register contains the interrupts for the OUT Endpoint 7 of the Device controller.

Address: 0x44900BE8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	Back2Back-SETup	StsPhseRc-vd	OUTTknEP-dis	SetUp	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved	RW	RW
HW Access						Reserved		
Name	StupPktRc-vd	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	OutPktErr

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	StupPktRcvd	Setup Packet Received Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the controller, this bit indicates that this buffer holds 8 bytes of setup data. There is only one Setup packet per buffer. On receiving a Setup packet, the controller closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behavior, the controller can receive any number of back to back setup packets and one buffer for every setup packet is used. - 1'b0: No Setup packet received - 1'b1: Setup packet received Reset: 1'b0 Default Value: 0x0 **0x0: NOT_RCVD :** No Setup packet received **0x1: RCVD :** Setup packet received

24.1.149 USBHS_DWC_otg_intreg_DOEPINT7 (continued)

14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt **0x0: INACTIVE :** No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No BbleErr interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done Default Value: 0x0

24.1.149 USBHS_DWC_otg_intreg_DOEPINT7 (continued)

		0x1: ACTIVE : BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	OutPktErr	OUT Packet Error (OutPktErr) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet. Default Value: 0x0 **0x1: ACTIVE :** OUT Packet Error **0x0: INACTIVE :** No OUT Packet Error
6	Back2BackSETup	Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt, Default Value: 0x0 **0x1: ACTIVE :** Back-to-Back SETUP Packets Received **0x0: INACTIVE :** No Back-to-Back SETUP Packets Received
5	StsPhseRcvd	Status Phase Received for Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode. Default Value: 0x0 **0x1: ACTIVE :** Status Phase Received for Control Write **0x0: INACTIVE :** No Status Phase Received for Control Write
4	OUTTknEPdis	OUT Token Received When Endpoint Disabled (OUTTknEPdis) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received. Default Value: 0x0

24.1.149 USBHS_DWC_otg_intreg_DOEPINT7 (continued)

		0x1: ACTIVE : OUT Token Received When Endpoint Disabled **0x0: INACTIVE :** No OUT Token Received When Endpoint Disabled
3	SetUp	SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet. Default Value: 0x0 **0x1: ACTIVE :** SETUP Phase Done **0x0: INACTIVE :** No SETUP Phase Done
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" section in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt

24.1.149 USBHS_DWC_otg_intreg_DOEPINT7 (continued)

0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Transfer Complete Interrupt **0x0: INACTIVE :** No Transfer Complete Interrupt

24.1.150 USBHS_DWC_otg_intreg_DOEPTSIZ7

Description: This register contains the Transfer Size for the OUT Endpoint 7 of the Device controller.

Address: 0x44900BF0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R		RW				
HW Access	Reserved							
Name	Reserved	RxDPID [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	RxDPID	RxDPID Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. - 2'b00: DATA0 - 2'b01: DATA2 - 2'b10: DATA1 - 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets Default Value: 0x0 **0x0: DATA0 :** DATA0 **0x2: DATA1PACKET2 :** DATA1 or 2 packets

24.1.150 USBHS_DWC_otg_intreg_DOEPTSIZ7 (continued)

		0x1: DATA2PACKET1 : DATA2 or 1 packet **0x3: MDATAPACKET3 :** MDATA or 3 packets
28 : 19	PktCnt	Packet Count (PktCnt) This field is decremented to zero after a packet is written into the RxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory. Default Value: 0x0

24.1.151 USBHS_DWC_otg_intreg_DOEPDMA7

Description: This register contains the DMA Address for the OUT Endpoint 7 of the Device controller.

Address: 0x44900BF4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.152 USBHS_DWC_otg_intreg_DOEPDMAB7

Description: This register contains the DMA Buffer Address for the OUT Endpoint 7 of the Device controller.

Address: 0x44900BFC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.153 USBHS_DWC_otg_intreg_DOEPCTL8

Description: This register is used to control the characteristics of OUT Endpoint 8 of the Device controller.

Address: 0x44900C00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	Reserved				RW		
HW Access		Reserved						
Name	USBActEP	Reserved [14:11]				MPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW	RW	RW		R	R
HW Access	Reserved							
Name	Reserved [23:22]		Stall	Snp	EPType [19:18]		NAKSts	DPID

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	W	W	W	W	Reserved	
HW Access							Reserved	
Name	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	Reserved [25:24]	

Bits	Name	Description
31	EPEna	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, - For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. - For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Completed Note: For control endpoints in DMA mode, this bit must be set for the controller to transfer SETUP data packets to the memory. This bit will not be cleared on Transfer Completed interrupt of the SETUP packet. Default Value: 0x0 **0x1: ACTIVE :** Enable Endpoint **0x0: INACTIVE :** No Action

24.1.153 USBHS_DWC_otg_intreg_DOEPCTL8 (continued)

30	EPDis	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Disable Endpoint **0x0: INACTIVE :** No Action
29	SetD1PID	Set DATA1 PID (SetD1PID) - Applies to interrupt and bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. - This field is applicable both for scatter-gather DMA mode and non scatter-gather DMA mode. Reset: 1'b0 Set Odd (micro)frame (SetOddFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the even and odd (micro)frame (EO_FrNum) field to odd (micro)frame. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA1 PID or Do not force Odd Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA1 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame
28	SetD0PID	Set DATA0 PID (SetD0PID) - Applies to interrupt/bulk IN and OUT endpoints only. - Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. - This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) - Applies to isochronous IN and OUT endpoints only. - Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to even (micro)frame. - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x0: DISABLED :** Disables Set DATA0 PID or Do not force Even Frame **0x1: ENABLED :** Set Endpoint Data PID to DATA0 or Sets EO_FrNum field to odd :DW-C_DESIGN_ID==1>frame:DWC_DESIGN_ID!=1>(micro)Frame

24.1.153 USBHS_DWC_otg_intreg_DOEPCTL8 (continued)

27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint. Default Value: 0x0 **0x1: ACTIVE :** Set NAK **0x0: INACTIVE :** No Set NAK
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** Clear NAK **0x0: INACTIVE :** No Clear NAK
21	Stall	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: ACTIVE :** STALL All Active Tokens **0x0: INACTIVE :** STALL All non-active tokens
20	Snp	RESERVED Default Value: 0x0 **0x0: RESERVED0SnpDOEPCTL8 :** Reserved 0 **0x1: RESERVED1SnpDOEPCTL8 :** Reserved 1

24.1.153 USBHS_DWC_otg_intreg_DOEPCTL8 (continued)

19 : 18	EPType	Endpoint Type (EPType) This is the transfer type supported by this logical endpoint. - 2'b00: Control - 2'b01: Isochronous - 2'b10: Bulk - 2'b11: Interrupt Default Value: 0x0 **0x2: BULK :** Bulk **0x0: CONTROL :** Control **0x3: INTERRUPT :** Interrupt **0x1: ISOCHRONOUS :** Isochronous
17	NAKSts	NAK Status (NAKSts) Indicates the following: - 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. - 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: - The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. - For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. - For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake. Default Value: 0x0 **0x1: NAK :** The core is transmitting NAK handshakes on this endpoint **0x0: NONNAK :** The core is transmitting non-NAK handshakes based on the FIFO status

24.1.153 USBHS_DWC_otg_intreg_DOEPCTL8 (continued)

16	DPID	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. - 1'b0: DATA0 - 1'b1: DATA1 This field is applicable for both Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Reset: 1'b0 Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: - Applies to isochronous IN and OUT endpoints only. - Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro)frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. -- 1'b0: Even (micro)frame -- 1'b1: Odd (micro)frame - When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure. Reset: 1'b0 Default Value: 0x0 **0x1: ACTIVE :** Endpoint Data PID active **0x0: INACTIVE :** Endpoint Data PID not active
15	USBActEP	USB Active Endpoint (USBActEP) Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit. Default Value: 0x0 **0x0: DISABLED :** Not Active **0x1: ENABLED :** USB Active Endpoint
10 : 0	MPS	Maximum Packet Size (MPS) The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes. Default Value: 0x0

24.1.154 USBHS_DWC_otg_intreg_DOEPINT8

Description: This register contains the interrupts for the OUT Endpoint 8 of the Device controller.

Address: 0x44900C08

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW	RW	RW
HW Access	Reserved							
Name	Reserved	Back2Back-SETup	StsPhseRc-vd	OUTTknEP-dis	SetUp	AHBErr	EPDisbld	XferCompl

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	Reserved	RW	RW
HW Access						Reserved		
Name	StupPktRc-vd	NYETIntrpt	NAKIntrpt	BbleErr	PktDrpSts	Reserved	BNAIntr	OutPktErr

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	StupPktRcvd	Setup Packet Received Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the controller, this bit indicates that this buffer holds 8 bytes of setup data. There is only one Setup packet per buffer. On receiving a Setup packet, the controller closes the buffer and disables the corresponding endpoint. The application has to re-enable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behavior, the controller can receive any number of back to back setup packets and one buffer for every setup packet is used. - 1'b0: No Setup packet received - 1'b1: Setup packet received Reset: 1'b0 Default Value: 0x0 **0x0: NOT_RCVD :** No Setup packet received **0x1: RCVD :** Setup packet received

24.1.154 USBHS_DWC_otg_intreg_DOEPINT8 (continued)

14	NYETIntrpt	NYET Interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. Default Value: 0x0 **0x1: ACTIVE :** NYET Interrupt **0x0: INACTIVE :** No NYET interrupt
13	NAKIntrpt	NAK Interrupt (NAKInterrupt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. Default Value: 0x0 **0x1: ACTIVE :** NAK Interrupt **0x0: INACTIVE :** No NAK interrupt
12	BbleErr	NAK Interrupt (BbleErr) The core generates this interrupt when babble is received for the endpoint. Default Value: 0x0 **0x1: ACTIVE :** BbleErr interrupt **0x0: INACTIVE :** No BbleErr interrupt
11	PktDrpSts	Packet Drop Status (PktDrpSts) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected. Default Value: 0x0 **0x1: ACTIVE :** Packet Drop Status interrupt **0x0: INACTIVE :** No interrupt
9	BNAIntr	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done Default Value: 0x0

24.1.154 USBHS_DWC_otg_intreg_DOEPINT8 (continued)

		0x1: ACTIVE : BNA interrupt **0x0: INACTIVE :** No BNA interrupt
8	OutPktErr	OUT Packet Error (OutPktErr) Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet. Default Value: 0x0 **0x1: ACTIVE :** OUT Packet Error **0x0: INACTIVE :** No OUT Packet Error
6	Back2BackSETup	Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt, Default Value: 0x0 **0x1: ACTIVE :** Back-to-Back SETUP Packets Received **0x0: INACTIVE :** No Back-to-Back SETUP Packets Received
5	StsPhseRcvd	Status Phase Received for Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode. Default Value: 0x0 **0x1: ACTIVE :** Status Phase Received for Control Write **0x0: INACTIVE :** No Status Phase Received for Control Write
4	OUTTknEPdis	OUT Token Received When Endpoint Disabled (OUTTknEPdis) Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received. Default Value: 0x0

24.1.154 USBHS_DWC_otg_intreg_DOEPINT8 (continued)

		0x1: ACTIVE : OUT Token Received When Endpoint Disabled **0x0: INACTIVE :** No OUT Token Received When Endpoint Disabled
3	SetUp	SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet. Default Value: 0x0 **0x1: ACTIVE :** SETUP Phase Done **0x0: INACTIVE :** No SETUP Phase Done
2	AHBErr	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/ write. The application can read the corresponding endpoint DMA address register to get the error address. For details, see "AHB Error Handling" section in the Programming Guide. Default Value: 0x0 **0x1: ACTIVE :** AHB Error interrupt **0x0: INACTIVE :** No AHB Error Interrupt
1	EPDisbld	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. Default Value: 0x0 **0x1: ACTIVE :** Endpoint Disabled Interrupt **0x0: INACTIVE :** No Endpoint Disabled Interrupt

24.1.154 USBHS_DWC_otg_intreg_DOEPINT8 (continued)

0	XferCompl	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. - When Scatter/Gather DMA mode is enabled -- For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. -- For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is Set. - When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint. Default Value: 0x0 **0x1: ACTIVE :** Transfer Complete Interrupt **0x0: INACTIVE :** No Transfer Complete Interrupt

24.1.155 USBHS_DWC_otg_intreg_DOEPTSIZ8

Description: This register contains the Transfer Size for the OUT Endpoint 8 of the Device controller.

Address: 0x44900C10

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	XferSize [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	XferSize [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW		
HW Access								
Name	PktCnt [23:19]					XferSize [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	R		RW				
HW Access	Reserved							
Name	Reserved	RxDPID [30:29]		PktCnt [28:24]				

Bits	Name	Description
30 : 29	RxDPID	RxDPID Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. - 2'b00: DATA0 - 2'b01: DATA2 - 2'b10: DATA1 - 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive. - 2'b01: 1 packet - 2'b10: 2 packets - 2'b11: 3 packets Default Value: 0x0 **0x0: DATA0 :** DATA0 **0x2: DATA1PACKET2 :** DATA1 or 2 packets

24.1.155 USBHS_DWC_otg_intreg_DOEPTSIZ8 (continued)

		0x1: DATA2PACKET1 : DATA2 or 1 packet **0x3: MDATAPACKET3 :** MDATA or 3 packets
28 : 19	PktCnt	Packet Count (PktCnt) This field is decremented to zero after a packet is written into the RxFIFO. Default Value: 0x0
18 : 0	XferSize	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory. Default Value: 0x0

24.1.156 USBHS_DWC_otg_intreg_DOEPDMA8

Description: This register contains the DMA Address for the OUT Endpoint 8 of the Device controller.

Address: 0x44900C14

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DMAAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DMAAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DMAAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DMAAddr [31:24]							

Bits	Name	Description
31 : 0	DMAAddr	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. - When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. - When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list. Default Value: X

24.1.157 USBHS_DWC_otg_intreg_DOEPDMAB8

Description: This register contains the DMA Buffer Address for the OUT Endpoint 8 of the Device controller.

Address: 0x44900C1C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	DMABufferAddr [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	DMABufferAddr [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	DMABufferAddr [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DMABufferAddr [31:24]							

Bits	Name	Description
31 : 0	DMABufferAddr	Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved. Default Value: X

24.1.158 USBHS_DWC_otg_intreg_PCGCCTL

Description: This register is used to control the Power and Clock Gating characteristics of the controller.

Address: 0x44900E00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	RW	Reserved	RW	Reserved		RW
HW Access				Reserved		Reserved		
Name	L1Suspend-ed	PhySleep	Enbl_L1-Gating	Reserved	RstPdwn-Module	Reserved [2:1]		StopPclk

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	L1Suspended	L1 Deep Sleep Indicates that the PHY is in deep sleep when in L1 state. Default Value: 0x0 **0x1: ACTIVE :** Deep Sleep **0x0: INACTIVE :** Non Deep Sleep
6	PhySleep	PHY In Sleep Indicates that the PHY is in Sleep State. Default Value: 0x0 **0x1: ACTIVE :** Phy in Sleep state **0x0: INACTIVE :** Phy not in Sleep state

24.1.158 USBHS_DWC_otg_intreg_PCGCCTL (continued)

5	Enbl_L1Gating	Enable Sleep Clock Gating If this bit is set, core internal clock gating is enabled sleep state if utmi_l1_suspend_n cannot be asserted by the core. The PHY clock will not be gated in sleep state if Enbl_L1Gating is not set. Default Value: 0x0 **0x0: DISABLED :** The PHY clock is not gated in Sleep state **0x1: ENABLED :** The Core internal clock gating is enabled in Sleep state
3	RstPdwnModule	Reset Power-Down Modules (RstPdwnModule) This bit is valid only in Partial Power-Down mode. - The application sets this bit when the power is turned off. - The application clears this bit after the power is turned on and the PHY clock is up. Note: The R/W of all core registers are possible only when this bit is set to 1b0. Default Value: 0x0 **0x1: OFF :** Power is turned off **0x0: ON :** Power is turned on
0	StopPclk	Stop Pclk (StopPclk) - The application sets this bit to stop the PHY clock (phy_clk) when the USB is suspended, the session is not valid, or the device is disconnected. - The application clears this bit when the USB is resumed or a new session starts. Default Value: 0x0 **0x0: DISABLED :** Disable Stop Pclk **0x1: ENABLED :** Enable Stop Pclk

24.1.159 USBHS_DWC_otg_intreg_PCGCCTL1

Description: This register is used to control the Power and Clock Gating characteristics of the controller.

Address: 0x44900E04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				RW	RW		RW
HW Access								
Name	RESERVED [7:4]				RAMGa-teEN	counter [2:1]		GateEN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	RESERVED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	RESERVED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	RESERVED [31:24]							

Bits	Name	Description
31 : 4	RESERVED	RESERVED Default Value: 0x0
3	RAMGateEN	RAM Clock Gating Enable (RAMGateEn) The application programs RAMGateEn to enable RAM Clock Gating in the ACG feature. - 1b0: Disable RAM Clock Gating (Default) - 1b1: Enable RAM Clock Gating Default Value: 0x0 **0x0: DISABLED :** RAM Clock Gating disable **0x1: ENABLED :** RAM Clock Gating enable
2 : 1	counter	Count to Gate Clock (CntGateClk) CntGateClk indicates to the Controller how many PHY Clock cycles and AHB Clock cycles of 'IDLE' (no activity) the Controller will wait for before Gating the respective PHY and AHB clocks internal to the Controller. - 2b00: 64 clocks (Default). - 2b01: 128 clocks Default Value: 0x0

24.1.159 USBHS_DWC_otg_intreg_PCGCCTL1 (continued)

		0x1: CLOCKS128 : CLOCKS128 **0x0: CLOCKS64 :** CLOCKS64
0	GateEN	Enable Active Clock Gating (GateEn) The application programs GateEn to enable Active Clock Gating feature for the PHY and AHB clocks. - 1b0: Disable Active Clock Gating (Default) - 1b1: Enable Active Clock Gating Default Value: 0x0 **0x0: DISABLED :** ACG disable **0x1: ENABLED :** ACG enable

24.1.160 USBHS_SS_SUBSYSTEM_CTL

Description: Subsystem level control register

Address: 0x44940000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	RSVD_1	SS_-FORCED_SHUTDOWN	USB_CTRL_SCALE-DOWN_MODE [5:4]		AHB_MAS-TER_SYNC	USB_-PHY_POW-ER_DOWN	USB_-MODE	SS_EN-ABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RSVD_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RSVD_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RSVD_1 [31:24]							

Bits	Name	Description
31 : 7	RSVD_1	Reserved Default Value: 0x0
6	SS_FORCED_SHUT-DOWN	1'b1: Forces shutdown of Controller resulting in data corruption from/to of Controller to the PHY resulting in USBHS moving to Q-state by accepting Q-channel request. 1'b0: Subsystem in normal operational mode. Default Value: 0x0
5 : 4	USB_CTRL_SCALE-DOWN_MODE	2'b00: Disables all scale-downs,actual timing value are used for synthesis.2'b01:Enables scale-down of all timing except Device mode.2'b10:Enables scale-down of Device mode suspend and resume timing values only.2'b11:Enables bit 0 and 1 scale-down timing values useful for simulations Default Value: 0x3
3	AHB_MASTER_SYNC	1'b1:Enables AHB Master interface of Controller synchronisation to "mmio_clk_hf" clock.1'b0: Disables AHB5 Master interface synchronisation such that 100 MHz generated out of "clk_hf" is used. Default Value: 0x0
2	USB_PHY_POW-ER_DOWN	1'b1:In the PHY during Sleep , the bias,PLL blocks are powered down and in Suspend , REF-CLK_LOGIC also powered down. 1'b0:All the three blocks remain powered during Sleep and Suspend modes. Default Value: 0x0
1	USB_MODE	1'b1:USB Subsystem is set to Host mode.1'b0: Subsystem is set to Device mode. Default Value: 0x1

24.1.160 USBHS_SS_SUBSYSTEM_CTL (continued)

0	SS_ENABLE	1'b1: Subsystem enable after power on reset to indicate both analog and digital power supply,all top level clocks,resets are stable to configure Controller core mode. 1'b0: Subsystem disable Default Value: 0x0

24.1.161 USBHS_SS_PHY_FUNC_CTL_1

Description: Subsystem level- PHY functional mode control register 1

Address: 0x44940004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	SQUELCH_THRESH-OLD	DISCONNECT_THRESHOLD [6:4]			PLL_FSEL [3:1]			PLL_B_TUNE

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	FS_LS_SOURCE_IMPED-ANCE [15:14]		TX_HS_CROSSOVER [13:12]		CHARGER_TYPE_DE-TECTION [11:10]		SQUELCH_THRESHOLD [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW				RW	
HW Access	R		R				R	
Name	HS_TX_RISETUNE [23:22]		HS_DC_VOLTAGE [21:18]				FS_LS_SOURCE_IMPED-ANCE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	PLL_I_TUNE [31:30]		PORT_RE-SET	HS_TX-_PRE_EM-PHASIS_DURATION	HS_TX_PRE_EMPHA-SIS_CURRENT [27:26]		USB_SOURCE_IMPED-ANCE [25:24]	

Bits	Name	Description
31 : 30	PLL_I_TUNE	PHY PLL Integral path tune.2'b00:1.0x ,2'b01:2.0x,2'b10:3.0x,2'b11:4.0x Default Value: 0x0
29	PORT_RESET	PHY port reset. 1'b0:Transmitter ,Receiver FSMs are operational and line_state becomes sequential after 11 PHY clock cycles. 1'b1:Transmitter ,Receiver FSMs are reset and line_state combinatorily reflects the state of SE-receivers. Default Value: 0x0
28	HS_TX_PRE_EMPHA-SIS_DURATION	HS transmitter pre-emphasis duration control. 1'b0:2x long pre-emphasis, 1'b1:1x short pre-emphasis. Default Value: 0x0
27 : 26	HS_TX_PRE_EMPHA-SIS_CURRENT	HS transmitter pre-emphasis current control. 2'b00:0 ,2'b01:1x,2'b10:2x,2'b11:3x Default Value: 0x0
25 : 24	USB_SOURCE_IMPED-ANCE	USB source impedance (Ohm). 2'b00:+3.01, 2'b01:0, 2'b10:2.68, 2'b11:5.01 Default Value: 0x1
23 : 22	HS_TX_RISETUNE	HS transmitter rise/fall time(%).2'b00:+1.06, 2'b01:0, 2'b10:-1.9, 2'b11:-2.33 Default Value: 0x1
21 : 18	HS_DC_VOLTAGE	HS DC voltage(%) level adjustment.4'b000:-6.06,4'b0001:-4.04,4'b0010:-2.03,4'b0011:0 Default Value: 0x3

24.1.161 USBHS_SS_PHY_FUNC_CTL_1 (continued)

17 : 14	FS_LS_-SOURCE_IMPEDANCE	LS and HS single-ended source impedance adjustment.4'b0000:+14.56%,4'b0001:+6.79%, 4'b0011:0%, 4'b0111: -5.93%, 4'b1111: -11.18%. Other bits are Reserved. Default Value: 0x3
13 : 12	TX_HS_CROSSOVER	Voltage(mV) at which DP0 ,DM0 crossover during HS transmission.2'b01:-14.71 ,2'b10:+13.98, 2'b11: 0, 2'b00:Reserved Default Value: 0x3
11 : 10	CHARGER_TYPE_DE-TECTION	Data detect voltage threshold adjustment during charger type detection. 2'b00:+10.2% , 2'b01:0 %, 2'b10:-10.2%, 2'b11: -20.75% Default Value: 0x1
9 : 7	SQUELCH_THRESHOLD	Voltage level threshold to detect valid High-Speed data. 3'b000 : +16.9 % , 3'b001: +10.95 % , 3'b010: +5.86%, 3'b011:0%,3'b100: -5.03%, 3'b101: -11.41%, 3'b110 : -16.92% ,3'b111: -22.75%. Default Value: 0x3
6 : 4	DISCONNECT_THRESH-OLD	Voltage level threshold to detect a disconnect event. 3'b000 : -4.33 % , 3'b001: -2.93 % , 3'b010: -1.48%, 3'b011:0%,3'b100: +1.36%, 3'b101: + 2.98%, 3'b110 : +4.67% ,3'b111: +6.45%. Default Value: 0x3
3 : 1	PLL_FSEL	PHY PLL reference clock frequency selection(MHz). If BANDWIDTH_TUNE is 1'b0 ,then 3'b000 is 9.6, 3'b001 is 10, 3'b010 is 12 and 3'b111 is 50 .Else 3'b000 is 19.2, 3'b001 is 20, 3'b010 is 24. Other combination of values are invlaid. Default Value: 0x7
0	PLL_B_TUNE	PHY PLL reference clock frequency tuning enable to double bandwidth of the PLL 1'b1: Enable ,1'b0: Disable Default Value: 0x0

24.1.162 USBHS_SS_PHY_FUNC_CTL_2

Description: Subsystem level- PHY functional mode control register 2

Address: 0x44940008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RES_TUNING_CODE	OTG_TUNE [6:4]			PLL_P_TUNE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW	RW		
HW Access	R			R	R	R		
Name	RSVD_2 [15:13]			EFUSE_SEL	RES_TUNING_SEL	RES_TUNING_CODE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RSVD_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RSVD_2 [31:24]							

Bits	Name	Description
31 : 13	RSVD_2	Reserved Default Value: 0x0
12	EFUSE_SEL	This signal selects the tuning method for the high-speed DP0 and DM0 source impedance of the USB 2.0 femtoPHY.1: Internal digital calibration code is used for tuning the high-speed source impedance.0: The RCALCODE0[3:0] value is used for tuning the high-speed source impedance. Default Value: 0x0
11	RES_TUNING_SEL	This signal selects the tuning method for the high-speed DP0 and DM0 source impedance of the USB 2.0 femtoPHY.1: Internal digital calibration code is used for tuning the high-speed source impedance.0: The RCALCODE0[3:0] value is used for tuning the high-speed source impedance. Default Value: 0x0
10 : 7	RES_TUNING_CODE	This bus is the resistor tuning code for the high-speed DP0 and DM0 source impedance of the USB 2.0 femtoPHY. The input values for this bus could be driven by ATE during characterization or production, and by an EFUSE block during product operation. All values from 4'b1111 to 4'b0000 are valid.4'b1111: provides lowest impedance on DP0 and DM0.4'b0000: provides the highest impedance on DP0 and DM0 Default Value: 0xF
6 : 4	OTG_TUNE	VBUS Valid Threshold Adjustment.3'b011: 0, (design default) Default Value: 0x3
3 : 0	PLL_P_TUNE	PHY PLL Proportioanl path tune.4'b1100:10.0x(design default) Default Value: 0xC

24.1.163 USBHS_SS_PHY_TEST_CTL

Description: Subsystem level- PHY test mode control register

Address: 0x4494000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						RW	RW
HW Access	R						R	R
Name	TEST_DATAIN0 [7:2]						TEST_-DATAOUT_-SEL0	TEST_-PULSE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW				RW	
HW Access	R	R	R				R	
Name	TEST_S-CAN_EN	TEST_BURNIN	TEST_ADDR0 [13:10]				TEST_DATAIN0 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW	RW		RW	RW
HW Access	R			R	R		R	R
Name	RSVD_3 [23:21]			TEST_A-TERESET	TEST_ANALOGPIN_SEL [19:18]		TEST_LOOPBACK_EN	TEST_ID-DQ_EN

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RSVD_3 [31:24]							

Bits	Name	Description
31 : 21	RSVD_3	Reserved Default Value: 0x0
20	TEST_ATERESET	USB PHY test mode ATE reset. 1'b1 : Disables PHYCLOCK0 ,FREECLK outputs. 1'b0:PHY-CLOCK0 ,FREECLK outputs are available within(maximum duration) 16.33 ns if UTMI+ interface is 8 bits else 24.66 ns Default Value: 0x0
19 : 18	TEST_ANALOGPIN_SEL	USB PHY analog test pin selection. Valid value: 2'b10,2'b11(Reserved as default to disable probing) Default Value: 0x3
17	TEST_LOOPBACK_EN	USB PHY loopback test control 1'b1: Enable.1'b0:Disable Default Value: 0x0
16	TEST_IDDQ_EN	USB PHY IDDQ test control 1'b1: Enable.1'b0:Disable Default Value: 0x0
15	TEST_SCAN_EN	USB PHY scan test (at-speed and stuck-at fault)mode. 1'b1: Enable.1'b0:Disable Default Value: 0x0
14	TEST_BURNIN	USB PHY test mode burn-in control. 1'b1: Enable(PHY performs power on reset,enters HS loop-back mode to transmit alternate 1's and 0's until disabled. 1'b0:Disable Default Value: 0x0
13 : 10	TEST_ADDR0	USB PHY test mode register address bus. Default Value: 0x0

24.1.163 USBHS_SS_PHY_TEST_CTL (continued)

9 : 2	TEST_DATAIN0	USB PHY test mode data write bus. Bits 0 to 3 are data, 4 to 7 are corresponding write enables Default Value: 0x0
1	TEST_DATAOUT_SEL0	USB PHY test mode data output selection. 1'b1: Mode-defined test register contents are output. 1'b0:Mode-defined, internally generated signals are ouptut. Default Value: 0x0
0	TEST_PULSE	USB PHY test mode non-continous clocking signal Default Value: 0x0

24.1.164 USBHS_SS_CONTROLLER_DDFT_CTL

Description: Subsystem level- Controller DDFT control register

Address: 0x44940010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	DEBUG_P-CLK_PROBES_COUNT [7:6]		DEBUG_HCLK_PROBES_COUNT [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	RSVD_4 [15:14]		DEBUG_PCLK_PROBES_COUNT [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RSVD_4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RSVD_4 [31:24]							

Bits	Name	Description
31 : 14	RSVD_4	Reserved Default Value: 0x0
13 : 6	DEBUG_P-CLK_PROBES_COUNT	USB Controller PHY clock domain internal signal probe counter value for debug[8'd0 to 8'd218] Default Value: 0x0
5 : 0	DEBUG_H-CLK_PROBES_COUNT	USB Controller AHB clock domain internal signal probe counter value for debug[6'd0 to 6'd61] Default Value: 0x0

24.1.165 USBHS_SS_INTR_SS

Description: Subsystem level- Interrupt register

Address: 0x44940014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1C	RW1C
HW Access	Reserved						RW1S	RW1S
Name	Reserved [7:2]						QCH_REQ_ERR	QCH_HCLK_GATED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	QCH_REQ_ERR	Subsystem and USB Controller AHB clock are gated after Q-state request is accepted either after end of transfer or forceful shutdown request from APPCPUSS Default Value: 0x0
0	QCH_HCLK_GATED	Subsystem and USB Controller AHB clock are gated after Q-state request is accepted either after end of transfer or forceful shutdown request from APPCPUSS Default Value: 0x0

24.1.166 USBHS_SS_INTR_SS_SET

Description: Subsystem level- Interrupt set register

Address: 0x44940018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1S	RW1S
HW Access	Reserved						A	A
Name	Reserved [7:2]						QCH_REQ_ERR	QCH_HCLK_GATED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	QCH_REQ_ERR	Write 1'b1 to set corresponding bit in interrupt register. Default Value: 0x0
0	QCH_HCLK_GATED	Write 1'b1 to set corresponding bit in interrupt register. Default Value: 0x0

24.1.167 USBHS_SS_INTR_SS_MASK

Description: Subsystem level- Interrupt mask register

Address: 0x4494001C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						QCH_REQ_ERR	QCH_HCLK_GATED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	QCH_REQ_ERR	Mask bit for corresponding bit in interrupt register. Default Value: 0x0
0	QCH_HCLK_GATED	Mask bit for corresponding bit in interrupt register. Default Value: 0x0

24.1.168 USBHS_SS_INTR_SS_MASKED

Description: Subsystem level- Interrupt masked register

Address: 0x44940020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						QCH_REQ_ERR	QCH_HCLK_GATED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	QCH_REQ_ERR	Logical and of corresponding interrupt and mask bits. Default Value: 0x0
0	QCH_HCLK_GATED	Logical and of corresponding interrupt and mask bits.SW need to set CTL.SS_FORCED_SHUTDOWN bit one clk_pwr cycle before PERI asserts Qrequest otherwise subsystem will deny the Qrequest. This interrupt indicates Subsystem accepts Q-state request and its functional clock (mmio_clk_sys) is internally gated and is in DEEPSLEEP power mode. Its PERI/SRSS responsbility to gate clk_pwr,clk_phy_pll_ref and assert rst_pwr_act_n as required. Renabling Subsystem requires first QExit->QEntry from PERI then Subsystem programming. Default Value: 0x0

25 Ethernet registers

This section discusses the Ethernet registers. It lists all the registers in mapping tables, in address order.

25.1 Register details

Register name	Address	Description
ETH0_CTL	0x42C10000	EMAC Control Register
ETH0_STATUS	0x42C10004	EMAC Status Register
ETH0_NETWORK_CONTROL	0x42C11000	The network control register contains general MAC control functions for both receiver and transmitter.
ETH0_NETWORK_CONFIG	0x42C11004	The network configuration register contains functions for setting the mode of operation for the Gigabit Ethernet MAC.
ETH0_NETWORK_STATUS	0x42C11008	The network status register returns status information with respect to the PHY management interface.
ETH0_USER_IO_REGISTER	0x42C1100C	Not presents. Access to the register will return AHB error.
ETH0_DMA_CONFIG	0x42C11010	DMA Configuration Register
ETH0_TRANSMIT_STATUS	0x42C11014	This register, when read, provides details of the status of a transmit. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register.
ETH0_RECEIVE_Q_PTR	0x42C11018	This register holds the start address of the receive buffer queue (receive buffers descriptor list). The receive buffer queue base address must be initialized before receive is enabled through bit 2 of the network control register. Once reception is enabled, any write to the receive buffer queue base address register is ignored. Reading this register returns the location of the descriptor currently being accessed. This value increments as buffers are used. Software should not use this register for determining where to remove received frames from the queue as it constantly changes as new frames are received. Software should instead work its way through the buffer descriptor queue checking the used bits. In terms of AMBA (AXI) operation, the receive descriptors are read from memory using a single 32bit AXI access. When the datapath is configured at 64bit, the receive descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is written to using a single 64bit AXI access.

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Register name	Address	Description
ETH0_TRANSMIT_Q_PTR	0x42C1101C	This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit, the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.
ETH0_RECEIVE_STATUS	0x42C11020	This register, when read provides details of the status of a receive. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register.
ETH0_INT_STATUS	0x42C11024	If not configured for priority queueing, the GEM generates a single interrupt. This register indicates the source of this interrupt. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the ethernet_int signal will be asserted. For test purposes each bit can be set or reset by writing to the interrupt mask register. The default configuration is shown below whereby all bits are reset to zero on read. Changing the validity of the `gem_irq_read_clear define will instead require a one to be written to the appropriate bit in order to clear it. In this mode reading has no affect on the status of the bit.
ETH0_INT_ENABLE	0x42C11028	At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero.
ETH0_INT_DISABLE	0x42C1102C	Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero.

Ethernet registers

Register name	Address	Description
ETH0_INT_MASK	0x42C11030	The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register.
ETH0_PHY_MANAGEMENT	0x42C11034	The PHY maintenance register is implemented as a shift register. Writing to the register starts a shift operation which is signalled as complete when bit-2 is set in the network status register. It takes about 2000 pclk cycles to complete, when MDC is set for pclk divide by 32 in the network configuration register. An interrupt is generated upon completion. During this time, the MSB of the register is output on the MDIO pin and the LSB updated from the MDIO pin with each MDC cycle. This causes transmission of a PHY management frame on MDIO. See Section 22.2.4.5 of the IEEE 802.3 standard. Reading during the shift operation will return the current contents of the shift register. At the end of management operation, the bits will have shifted back to their original locations. For a read operation, the data bits will be updated with data read from the PHY. It is important to write the correct values to the register to ensure a valid PHY management frame is produced. The MDIO interface can read IEEE 802.3 clause 45 PHYs as well as clause 22 PHYs. To read clause 45 PHYs, bit 30 should be written with a 0 rather than a 1. For a description of MDC generation, see Network Configuration Register.
ETH0_PAUSE_TIME	0x42C11038	Received Pause Quantum Register
ETH0_TX_PAUSE_QUANTUM	0x42C1103C	Transmit Pause Quantum Register
ETH0_PBUF_TXCUTTHRU	0x42C11040	Partial store and forward is only applicable when using the DMA configured in SRAM based packet buffer mode. It is also not available when using multi buffer frames. TX Partial Store and Forward
ETH0_PBUF_RXCUTTHRU	0x42C11044	RX Partial Store and Forward
ETH0_JUMBO_MAX_LENGTH	0x42C11048	Maximum Jumbo Frame Size.
ETH0_EXTERNAL_FIFO_INTERFACE	0x42C1104C	Not presents.
ETH0_RSC_CONTROL	0x42C11058	Not presents. Access to the register will return AHB error.

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Register name	Address	Description
ETH0_INT_MODERATION	0x42C1105C	Used to moderate the number of transmit and receive complete interrupts issued. With interrupt moderation enabled receive and transmit interrupts are not generated immediately a frame is transmitted or received. Instead when a receive or transmit event occurs a timer is started and the interrupt is asserted after it times out. This limits the frequency with which the CPU receives interrupts. When interrupt moderation is enabled interrupt status bit one is always used for receive and bit 7 is always used for transmit even when priority queuing is enabled. With interrupt moderation 800ns periods are counted. GEM determines what constitutes an 800ns period by looking at the tbi (bit 11), gigabit bit (10) and speed (bit 0) bits in the network configuration register and counting tx_clk cycles. Bit 0 needs to be set to 1 for 100M operation.
ETH0_SYS_WAKE_TIME	0x42C11060	Used to pause transmission after deassertion of tx_lpi_en. Each unit in this register corresponds to 64ns in gigabit mode, 320ns in 100M mode and 3200ns at 10M. After tx_lpi_en is deasserted transmission will pause for the set time.
ETH0_HASH_BOTTOM	0x42C11080	The unicast hash enable and the multicast hash enable bits in the network configuration register enable the reception of hash matched frames. Hash Register Bottom (31 to 0 bits)
ETH0_HASH_TOP	0x42C11084	Hash Register Top (63 to 32 bits)
ETH0_SPEC_ADD1_BOTTOM	0x42C11088	The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written.
ETH0_SPEC_ADD1_TOP	0x42C1108C	Specific Address Top
ETH0_SPEC_ADD2_BOTTOM	0x42C11090	The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written.
ETH0_SPEC_ADD2_TOP	0x42C11094	Specific Address Top
ETH0_SPEC_ADD3_BOTTOM	0x42C11098	The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. See ETH0_SPEC_ADD2_BOTTOM for the details of bit fields.
ETH0_SPEC_ADD3_TOP	0x42C1109C	Specific Address Top. See ETH0_SPEC_ADD2_TOP for the details of bit fields.

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Register name	Address	Description
ETH0_SPEC_ADD4_BOTTOM	0x42C110A0	The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. See ETH0_SPEC_ADD2_BOTTOM for the details of bit fields.
ETH0_SPEC_ADD4_TOP	0x42C110A4	Specific Address Top. See ETH0_SPEC_ADD2_TOP for the details of bit fields.
ETH0_SPEC_TYPE1	0x42C110A8	Type ID Match 1
ETH0_SPEC_TYPE2	0x42C110AC	Type ID Match 2
ETH0_SPEC_TYPE3	0x42C110B0	Type ID Match 3
ETH0_SPEC_TYPE4	0x42C110B4	Type ID Match 4
ETH0_WOL_REGISTER	0x42C110B8	Wake on LAN Register. Presents in design, but feature is not supported.
ETH0_STRETCH_RATIO	0x42C110BC	IPG stretch register
ETH0_STACKED_VLAN	0x42C110C0	Stacked VLAN Register
ETH0_TX_PFC_PAUSE	0x42C110C4	Transmit PFC Pause Register
ETH0_MASK_ADD1_BOTTOM	0x42C110C8	Specific Address Mask 1 Bottom (31 to 0 bits)
ETH0_MASK_ADD1_TOP	0x42C110CC	Specific Address Mask 1 Top (47 to 32 bits)
ETH0_DMA_ADDR_OR_MASK	0x42C110D0	Receive DMA Data Buffer Address Mask
ETH0_RX_PTP_UNICAST	0x42C110D4	PTP RX unicast IP destination address
ETH0_TX_PTP_UNICAST	0x42C110D8	PTP TX unicast IP destination address
ETH0_TSU_NSEC_CMP	0x42C110DC	TSU timer comparison value nanoseconds
ETH0_TSU_SEC_CMP	0x42C110E0	TSU timer comparison value seconds (31 to 0 bits)
ETH0_TSU_MSB_SEC_CMP	0x42C110E4	TSU timer comparison value seconds (47 to 32 bits)
ETH0_TSU_PTP_TX_MSB_SEC	0x42C110E8	PTP Event Frame Transmitted Seconds Register (47 to 32 bits)
ETH0_TSU_PTP_RX_MSB_SEC	0x42C110EC	PTP Event Frame Received Seconds Register (47 to 32 bits)
ETH0_TSU_PEER_TX_MSB_SEC	0x42C110F0	PTP Peer Event Frame Transmitted Seconds Register (47 to 32 bits)
ETH0_TSU_PEER_RX_MSB_SEC	0x42C110F4	PTP Peer Event Frame Received Seconds Register (47 to 32 bits)
ETH0_DPRAM_FILL_DBG	0x42C110F8	The fill levels for the TX & RX packet buffers can be read using this register, including the fill level for each queue in the TX direction.
ETH0_REVISION_REG	0x42C110FC	This register indicates a Cadence module identification number and module revision. The value of this register is read only as defined by `gem_revision_reg_value
ETH0_OCTETS_TXED_BOTTOM	0x42C11100	Octets Transmitted lower bits (31 to 0 bits)
ETH0_OCTETS_TXED_TOP	0x42C11104	Octets Transmitted higher bits (47 to 32 bits)
ETH0_FRAMES_TXED_OK	0x42C11108	Frames Transmitted

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Register name	Address	Description
ETH0_BROADCAST_TXED	0x42C1110C	Broadcast Frames Transmitted
ETH0_MULTICAST_TXED	0x42C11110	Multicast Frames Transmitted
ETH0_PAUSE_FRAMES_TXED	0x42C11114	Pause Frames Transmitted
ETH0_FRAMES_TXED_64	0x42C11118	64 Byte Frames Transmitted
ETH0_FRAMES_TXED_65	0x42C1111C	65 to 127 Byte Frames Transmitted
ETH0_FRAMES_TXED_128	0x42C11120	128 to 255 Byte Frames Transmitted
ETH0_FRAMES_TXED_256	0x42C11124	256 to 511 Byte Frames Transmitted
ETH0_FRAMES_TXED_512	0x42C11128	512 to 1023 Byte Frames Transmitted
ETH0_FRAMES_TXED_1024	0x42C1112C	1024 to 1518 Byte Frames Transmitted
ETH0_FRAMES_TXED_1519	0x42C11130	Greater Than 1518 Byte Frames Transmitted
ETH0_TX_UNDERRUNS	0x42C11134	Transmit Under Runs
ETH0_SINGLE_COLLISIONS	0x42C11138	Single Collision Frames. Presents in design but not support.
ETH0_MULTIPLE_COLLISIONS	0x42C1113C	Multiple Collision Frames. Presents in design but not support.
ETH0_EXCESSIVE_COLLISIONS	0x42C11140	Excessive Collisions. Presents in design but not support.
ETH0_LATE_COLLISIONS	0x42C11144	Late Collisions. Presents in design but not support.
ETH0_DEFERRED_FRAMES	0x42C11148	Deferred Transmission Frames. Presents in design but not support.
ETH0_CRS_ERRORS	0x42C1114C	Carrier Sense Errors. Presents in design but not support.
ETH0_OCTETS_RXED_BOTTOM	0x42C11150	Octets Received (31 to 0 bits)
ETH0_OCTETS_RXED_TOP	0x42C11154	Octets Received (47 to 32 bits)
ETH0_FRAMES_RXED_OK	0x42C11158	Frames Received
ETH0_BROADCAST_RXED	0x42C1115C	Broadcast Frames Received
ETH0_MULTICAST_RXED	0x42C11160	Multicast Frames Received
ETH0_PAUSE_FRAMES_RXED	0x42C11164	Pause Frames Received
ETH0_FRAMES_RXED_64	0x42C11168	64 Byte Frames Received
ETH0_FRAMES_RXED_65	0x42C1116C	65 to 127 Byte Frames Received
ETH0_FRAMES_RXED_128	0x42C11170	128 to 255 Byte Frames Received
ETH0_FRAMES_RXED_256	0x42C11174	256 to 511 Byte Frames Received
ETH0_FRAMES_RXED_512	0x42C11178	512 to 1023 Byte Frames Received
ETH0_FRAMES_RXED_1024	0x42C1117C	1024 to 1518 Byte Frames Received
ETH0_FRAMES_RXED_1519	0x42C11180	1519 to maximum Byte Frames Received
ETH0_UNDERSIZE_FRAMES	0x42C11184	Undersized Frames Received
ETH0_EXCESSIVE_RX_LENGTH	0x42C11188	Oversize Frames Received
ETH0_RX_JABBERS	0x42C1118C	Jabbers Received
ETH0_FCS_ERRORS	0x42C11190	Frame Check Sequence Errors
ETH0_RX_LENGTH_ERRORS	0x42C11194	Length Field Frame Errors

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Register name	Address	Description
ETH0_RX_SYMBOL_ERRORS	0x42C11198	Receive Symbol Errors
ETH0_ALIGNMENT_ERRORS	0x42C1119C	Alignment Errors
ETH0_RX_RESOURCE_ERRORS	0x42C111A0	Receive Resource Errors
ETH0_RX_OVERRUNS	0x42C111A4	Receive Overruns
ETH0_RX_IP_CK_ERRORS	0x42C111A8	IP Header Checksum Errors
ETH0_RX_TCP_CK_ERRORS	0x42C111AC	TCP Checksum Errors
ETH0_RX_UDP_CK_ERRORS	0x42C111B0	UDP Checksum Errors
ETH0_AUTO_FLUSHED_PKTS	0x42C111B4	Receive DMA Flushed Packets
ETH0_TSU_TIMER_INCR_SUB_NSEC	0x42C111BC	1588 Timer Increment Register sub nsec
ETH0_TSU_TIMER_MSB_SEC	0x42C111C0	1588 Timer Seconds Register (47 to 32 bits)
ETH0_TSU_STROBE_MSB_SEC	0x42C111C4	1588 Timer Sync Strobe Seconds Register (47 to 32 bits)
ETH0_TSU_STROBE_SEC	0x42C111C8	1588 Timer Sync Strobe Seconds Register (31 to 0 bits)
ETH0_TSU_STROBE_NSEC	0x42C111CC	1588 Timer Sync Strobe Nanoseconds Register
ETH0_TSU_TIMER_SEC	0x42C111D0	1588 Timer Seconds Register (31 to 0 bits)
ETH0_TSU_TIMER_NSEC	0x42C111D4	1588 Timer Nanoseconds Register
ETH0_TSU_TIMER_ADJUST	0x42C111D8	This register is used to adjust the value of the timer in the TSU. It allows an integral number of nanoseconds to be added or subtracted from the timer in a one-off operation. This register returns all zeroes when read.
ETH0_TSU_TIMER_INCR	0x42C111DC	1588 Timer Increment Register
ETH0_TSU_PTP_TX_SEC	0x42C111E0	PTP Event Frame Transmitted Seconds Register (31 to 0 bits)
ETH0_TSU_PTP_TX_NSEC	0x42C111E4	PTP Event Frame Transmitted Nanoseconds Register
ETH0_TSU_PTP_RX_SEC	0x42C111E8	PTP Event Frame Received Seconds Register (31 to 0 bits)
ETH0_TSU_PTP_RX_NSEC	0x42C111EC	PTP Event Frame Received Nanoseconds Register
ETH0_TSU_PEER_TX_SEC	0x42C111F0	PTP Peer Event Frame Transmitted Seconds Register (31 to 0 bits)
ETH0_TSU_PEER_TX_NSEC	0x42C111F4	PTP Peer Event Frame Transmitted Nanoseconds Register
ETH0_TSU_PEER_RX_SEC	0x42C111F8	PTP Peer Event Frame Received Seconds Register (31 to 0 bits)
ETH0_TSU_PEER_RX_NSEC	0x42C111FC	PTP Peer Event Frame Received Nanoseconds Register
ETH0_PCS_CONTROL	0x42C11200	Not presents. Access to the register returns AHB error.
ETH0_PCS_STATUS	0x42C11204	Not presents. Access to the register returns AHB error. See ETH0_PCS_CONTROL for the details of bit fields.
ETH0_PCS_AN_ADV	0x42C11210	Not presents. Access to the register returns AHB error. See ETH0_PCS_CONTROL for the details of bit fields.
ETH0_PCS_AN_LP_BASE	0x42C11214	Not presents. Access to the register returns AHB error. See ETH0_PCS_CONTROL for the details of bit fields.

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Register name	Address	Description
ETH0_PCS_AN_EXP	0x42C11218	Not presents. Access to the register returns AHB error. See ETH0_PCS_CONTROL for the details of bit fields.
ETH0_PCS_AN_NP_TX	0x42C1121C	Not presents. Access to the register returns AHB error. See ETH0_PCS_CONTROL for the details of bit fields.
ETH0_PCS_AN_LP_NP	0x42C11220	Not presents. Access to the register returns AHB error. See ETH0_PCS_CONTROL for the details of bit fields.
ETH0_PCS_AN_EXT_STATUS	0x42C1123C	Not presents. Access to the register returns AHB error. See ETH0_PCS_CONTROL for the details of bit fields.
ETH0_TX_PAUSE_QUANTUM1	0x42C11260	Transmit Pause Quantum Register 1
ETH0_TX_PAUSE_QUANTUM2	0x42C11264	Transmit Pause Quantum Register 2
ETH0_TX_PAUSE_QUANTUM3	0x42C11268	Transmit Pause Quantum Register 3
ETH0_RX_LPI	0x42C11270	Received LPI transitions
ETH0_RX_LPI_TIME	0x42C11274	Received LPI time
ETH0_TX_LPI	0x42C11278	Transmit LPI transitions
ETH0_TX_LPI_TIME	0x42C1127C	Transmit LPI time
ETH0_DESIGNCFG_DEBUG1	0x42C11280	Design Configuration Register 1
ETH0_DESIGNCFG_DEBUG2	0x42C11284	Design Configuration Register 2
ETH0_DESIGNCFG_DEBUG3	0x42C11288	Design Configuration Register 3
ETH0_DESIGNCFG_DEBUG4	0x42C1128C	Design Configuration Register 4
ETH0_DESIGNCFG_DEBUG5	0x42C11290	Design Configuration Register 5
ETH0_DESIGNCFG_DEBUG6	0x42C11294	Design Configuration Register 6
ETH0_DESIGNCFG_DEBUG7	0x42C11298	Design Configuration Register 7
ETH0_DESIGNCFG_DEBUG8	0x42C1129C	Design Configuration Register 8
ETH0_DESIGNCFG_DEBUG9	0x42C112A0	Design Configuration Register 9
ETH0_DESIGNCFG_DEBUG10	0x42C112A4	Design Configuration Register 10
ETH0_SPEC_ADD5_BOTTOM	0x42C11300	Specific address registers 5 ~ 36 doesn't present. Access to the register returns AHB error.
ETH0_SPEC_ADD5_TOP	0x42C11304	Specific address registers 5 ~ 36 doesn't present. Access to the register returns AHB error. See ETH0_SPEC_ADD5_BOTTOM for the details of bit fields.
ETH0_SPEC_ADD36_BOTTOM	0x42C113F8	Not presents.
ETH0_SPEC_ADD36_TOP	0x42C113FC	Not presents. See ETH0_SPEC_ADD36_BOTTOM for the details of bit fields.
ETH0_INT_Q1_STATUS	0x42C11400	Priority queue Interrupt Status Register
ETH0_INT_Q2_STATUS	0x42C11404	Priority queue Interrupt Status Register. See ETH0_INT_Q1_STATUS for the details of bit fields.
ETH0_INT_Q3_STATUS	0x42C11408	int_q3_status to int_q15_status doesn't present. Access to the register returns AHB error.
ETH0_INT_Q15_STATUS	0x42C11438	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.

Ethernet registers

Register name	Address	Description
ETH0_TRANSMIT_Q1_PTR	0x42C11440	This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.
ETH0_TRANSMIT_Q2_PTR	0x42C11444	This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.
ETH0_TRANSMIT_Q3_PTR	0x42C11448	transmit_q3_ptr to transmit_q15_ptr doesn't present. Access to the register returns AHB error.

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Register name	Address	Description
ETH0_TRANSMIT_Q15_PTR	0x42C11478	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.
ETH0_RECEIVE_Q1_PTR	0x42C11480	This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.

Ethernet registers

Register name	Address	Description
ETH0_RECEIVE_Q2_PTR	0x42C11484	This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access. See ETH0_RECEIVE_Q1_PTR for the details of bit fields.
ETH0_RECEIVE_Q3_PTR	0x42C11488	Not presents. Start address register doesn't present for queue3 ~ queue7.
ETH0_RECEIVE_Q7_PTR	0x42C11498	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.
ETH0_DMA_RXBUF_SIZE_Q1	0x42C114A0	Receive Buffer queue 1 Size
ETH0_DMA_RXBUF_SIZE_Q2	0x42C114A4	Receive Buffer queue 2 Size
ETH0_DMA_RXBUF_SIZE_Q3	0x42C114A8	dma_rxbuf_size_q3 to dma_rxbuf_size_q7 doesn't present.
ETH0_DMA_RXBUF_SIZE_Q7	0x42C114B8	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.

Ethernet registers

Register name	Address	Description
ETH0_CBS_CONTROL	0x42C114BC	The IdleSlope value is defined as the rate of change of credit when a packet is waiting to be sent. This must not exceed the portTransmitRate which is dependent on the speed of operation, eg, portTranmsitRate. 1Gb/s = 32'h07735940 (125 Mbytes/s), 100Mb/sec = 32'h017D7840 (25 Mnibbles/s), 10Mb/sec = 32'h002625A0 (2.5 Mnibbles/s). If 50% of bandwidth was to be allocated to a particular queue in 1Gb/sec mode then the IdleSlope value for that queue would be calculated as 32'h07735940/2. Note that Credit-Based Shaping should be disabled prior to updating the IdleSlope values. As another example, for a 1722 audio packet with a payload of 6 samples per channel, the packet size would be 7 (preamble) + 1 (SFD) + 50 (packet header) + 6x4x2(payload) + 4 (CRC) = 110 bytes. For a rate of 8000 packets per second, the desired rate would 110 x 8000 bytes per second, so the programmed idleSlope value would be 880000 for a 1Gb/s connection, or 1760000 for a 100Mb/s or 10Mbs connection. See Figure 6.3 in the IEEE 1722 standard. In practice, the actual transmission rate will be vary slightly from that calculated. In this case, the idleSlope value should be recalibrated based on the variance between the measured and expected rate, and in this case very accurate transmission rates can be achieved.
ETH0_CBS_IDLESLOPE_Q_A	0x42C114C0	queue A is the highest priority queue. This would be queue 8 in an 8 queue configuration.
ETH0_CBS_IDLESLOPE_Q_B	0x42C114C4	queue B is the 2nd highest priority queue. This would be queue 7 in an 8 queue configuration.
ETH0_UPPER_TX_Q_BASE_ADDR	0x42C114C8	Upper 32 bits of transmit buffer descriptor queue base address.
ETH0_TX_BD_CONTROL	0x42C114CC	TX BD control register
ETH0_RX_BD_CONTROL	0x42C114D0	RX BD control register
ETH0_UPPER_RX_Q_BASE_ADDR	0x42C114D4	Upper 32 bits of receive buffer descriptor queue base address.
ETH0_HIDDEN_REG0	0x42C114E0	Hidden register
ETH0_HIDDEN_REG1	0x42C114E4	Hidden register
ETH0_HIDDEN_REG2	0x42C114E8	Hidden register
ETH0_HIDDEN_REG3	0x42C114EC	Hidden register

Ethernet registers

Register name	Address	Description
ETH0_SCREENING_TYPE_1_REGISTER_0	0x42C11500	Screening type 1 registers are used to allocate up to 16 priority queues to received frames based on certain IP or UDP fields of incoming frames. Firstly, when DS/TC match enable is set (bit 28), the DS (Differentiated Services) field of the received IPv4 header or TCfield (traffic class) of IPv6 headers are matched against bits 11 to 4. Secondly, when UDP port match enable is set (bit 29), the UDP Destination Port of the received UDP frame is matched against bits 27 to 12. Both UDP and DS/TC matching can be enabled simultaneously or individually. If a match is successful, then the queue value programmed in bits 2 to 0 is allocated to the frame. The required number of Type 1 screening registers is configured in the gem defines file. Up to 16 type 1 screening registers have been allocated APB address space between 0x500 and 0x53C.
ETH0_SCREENING_TYPE_1_REGISTER_1	0x42C11504	screening type 1 register 1, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_2	0x42C11508	screening type 1 register 2, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_3	0x42C1150C	screening type 1 register 3, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_4	0x42C11510	screening type 1 register 4, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_5	0x42C11514	screening type 1 register 5, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_6	0x42C11518	screening type 1 register 6, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_7	0x42C1151C	screening type 1 register 7, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_8	0x42C11520	screening type 1 register 8, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_9	0x42C11524	screening type 1 register 9, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_10	0x42C11528	screening type 1 register 10, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_11	0x42C1152C	screening type 1 register 11, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_12	0x42C11530	screening type 1 register 12, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_13	0x42C11534	screening type 1 register 13, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_1_REGISTER_14	0x42C11538	screening type 1 register 14, same as screening_type_1_register_0

Ethernet registers

Register name	Address	Description
ETH0_SCREENING_TYPE_1_REGISTER_15	0x42C1153C	screening type 1 register 15, same as screening_type_1_register_0
ETH0_SCREENING_TYPE_2_REGISTER_0	0x42C11540	Screener Type 2 match registers operate independently of screener type 1 registers and offer additional match capabilities, extending the capabilities into vendor specific protocols.
ETH0_SCREENING_TYPE_2_REGISTER_1	0x42C11544	screening type 2 register 1, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_2	0x42C11548	screening type 2 register 2, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_3	0x42C1154C	screening type 2 register 3, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_4	0x42C11550	screening type 2 register 4, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_5	0x42C11554	screening type 2 register 5, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_6	0x42C11558	screening type 2 register 6, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_7	0x42C1155C	screening type 2 register 7, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_8	0x42C11560	screening type 2 register 8, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_9	0x42C11564	screening type 2 register 9, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_10	0x42C11568	screening type 2 register 10, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_11	0x42C1156C	screening type 2 register 11, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_12	0x42C11570	screening type 2 register 12, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_13	0x42C11574	screening type 2 register 13, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_14	0x42C11578	screening type 2 register 14, same as screening_type_2_register_0
ETH0_SCREENING_TYPE_2_REGISTER_15	0x42C1157C	screening type 2 register 15, same as screening_type_2_register_0
ETH0_TX_SCHED_CTRL	0x42C11580	This register controls the transmit scheduling algorithm the user can select for each active transmit queue. By default all queues are initialized to fixed priority, with the top indexed queue having overall priority
ETH0_BW_RATE_LIMIT_Q0TO3	0x42C11590	This register holds the DWRR weighting value or the ETS bandwidth percentage value used by the transmit scheduler for queues 0 to 3.

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Register name	Address	Description
ETH0_BW_RATE_LIMIT_Q4TO7	0x42C11594	Not presents. EMAC has only 3 queues. Access to the register returns AHB error.
ETH0_BW_RATE_LIMIT_Q8TO11	0x42C11598	Not presents. EMAC has only 3 queues. Access to the register returns AHB error.
ETH0_BW_RATE_LIMIT_Q12TO15	0x42C1159C	Not presents. EMAC has only 3 queues. Access to the register returns AHB error. See ETH0_BW_RATE_LIMIT_Q8TO11 for the details of bit fields.
ETH0_TX_Q_SEG_ALLOC_Q0TO7	0x42C115A0	This register allows the user to distribute the Transmit SRAM used by the DMA across the priority queues, for queues 0 to 7. The SRAM itself is split into a number of evenly sized segments (this is defined in the verilog configuration defs file - for the configuration used to generate this register description, the total number of segments was set to '16'). Those segments can then be freely distributed across the active queues, in powers of 2. I.e. a value of 0 would mean 1 segment has been allocated to the queue. A value of 1 would mean 2 segments, a value of 2 means 4 segments and so on. The reset values of these registers are defined in the configuration defs file.
ETH0_TX_Q_SEG_ALLOC_Q8TO15	0x42C115A4	Not presents. Access to the register returns AHB error.
ETH0_RECEIVE_Q8_PTR	0x42C115C0	receive_q8_ptr to receive_q15_ptr doesn't present. Access to the register returns AHB error.
ETH0_RECEIVE_Q15_PTR	0x42C115DC	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.
ETH0_DMA_RXBUF_SIZE_Q8	0x42C115E0	dma_rxbuf_size_q8 to dma_rxbuf_size_q15 doesn't present. Access to the register returns AHB error.
ETH0_DMA_RXBUF_SIZE_Q15	0x42C115FC	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.
ETH0_INT_Q1_ENABLE	0x42C11600	At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero.
ETH0_INT_Q2_ENABLE	0x42C11604	At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero. See ETH0_INT_Q1_ENABLE for the details of bit fields.
ETH0_INT_Q3_ENABLE	0x42C11608	int_q3_enable to int_q7_enable doesn't present. Access to the register returns AHB error.
ETH0_INT_Q7_ENABLE	0x42C11618	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.

Ethernet registers

Register name	Address	Description
ETH0_INT_Q1_DISABLE	0x42C11620	Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero.
ETH0_INT_Q2_DISABLE	0x42C11624	Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero. See ETH0_INT_Q1_DISABLE for the details of bit fields.
ETH0_INT_Q3_DISABLE	0x42C11628	int_q3_disable to int_q7_disable doesn't present. Access to the register returns AHB error.
ETH0_INT_Q7_DISABLE	0x42C11638	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.
ETH0_INT_Q1_MASK	0x42C11640	The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register.
ETH0_INT_Q2_MASK	0x42C11644	The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register. See ETH0_INT_Q1_MASK for the details of bit fields.
ETH0_INT_Q3_MASK	0x42C11648	int_q3_mask to int_q7_mask doesn't present. Access to the register returns AHB error.
ETH0_INT_Q7_MASK	0x42C11658	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.
ETH0_INT_Q8_ENABLE	0x42C11660	int_q8_enable to int_q15_enable doesn't present. Access to the register returns AHB error.
ETH0_INT_Q15_ENABLE	0x42C1167C	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.
ETH0_INT_Q8_DISABLE	0x42C11680	int_q8_disable to int_q15_disable doesn't present. Access to the register returns AHB error.

Ethernet registers

Register name	Address	Description
ETH0_INT_Q15_DISABLE	0x42C1169C	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.
ETH0_INT_Q8_MASK	0x42C116A0	int_q8_mask to int_q15_mask doesn't present. Access to the register returns AHB error.
ETH0_INT_Q15_MASK	0x42C116BC	Not presents. See ETH0_EXTERNAL_FIFO_INTERFACE for the details of bit fields.
ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_0	0x42C116E0	Ethertype Register
ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_1	0x42C116E4	Ethertype Register. See ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_0 for the details of bit fields.
ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_2	0x42C116E8	Ethertype Register. See ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_0 for the details of bit fields.
ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_3	0x42C116EC	Ethertype Register. See ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_0 for the details of bit fields.
ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_4	0x42C116F0	Ethertype Register. See ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_0 for the details of bit fields.
ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_5	0x42C116F4	Ethertype Register. See ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_0 for the details of bit fields.
ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_6	0x42C116F8	Ethertype Register. See ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_0 for the details of bit fields.
ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_7	0x42C116FC	Ethertype Register. See ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_0 for the details of bit fields.

Ethernet registers

Register name	Address	Description
ETH0_TYPE2_COMPARE_0_WORD_0	0x42C11700	"Compare A, B and C fields of the screener type 2 match register are pointers to a pool of up to 32 compare registers. If enabled the compare is true if the data at the OFFSET into the frame, ANDed with the MASK Value if the mask is enabled, is equal to the COMPARE Value. Either a 16 bit comparison or a 32 bit comparison is done. This selection is made via the associated compare word1 register bit 9. If a 16 bit comparison is selected, then a 16 bit mask is also available to the user to select which bits should be compared. If the 32 bit compare option is selected, then no mask is available. The byte at the OFFSET number of bytes from the index start is compared thru bits 7 to 0 of the configured VALUE. The byte at the OFFSET number of bytes + 1 from the index start is compared thru bits 15 to 8 of the configured VALUE and so on. The OFFSET can be configured to be from 0 to 127 bytes from either the start of the frame, the byte following the therType field (last EtherType in the header if the frame is VLAN tagged), the byte following the IP header (IPv4 or IPv6) or from the byte following the start of the TCP/UDP header. The required number of Type 2 screening registers up to a maximum of 32 is configurable in the gem defines file and have been allocated APB address space between 0x700 and 0x7fc. Note. when using RX Partial Store and Forward mode and priority queues, the frame offset must be less than the Partial Store and Forward watermark. If the offset is higher than the watermark value it's not possible to identify the priority queue before the frame is sent to the AMBA interface, and an incorrect priority queue may be used. "
ETH0_TYPE2_COMPARE_0_WORD_1	0x42C11704	"Type2 Compare Word 1"
ETH0_TYPE2_COMPARE_1_WORD_0	0x42C11708	same as type2_compare_0_word_0
ETH0_TYPE2_COMPARE_1_WORD_1	0x42C1170C	same as type2_compare_0_word_1
ETH0_TYPE2_COMPARE_2_WORD_0	0x42C11710	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_2_WORD_1	0x42C11714	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_3_WORD_0	0x42C11718	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.

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Register name	Address	Description
ETH0_TYPE2_COMPARE_3_WORD_1	0x42C1171C	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_4_WORD_0	0x42C11720	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_4_WORD_1	0x42C11724	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_5_WORD_0	0x42C11728	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_5_WORD_1	0x42C1172C	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_6_WORD_0	0x42C11730	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_6_WORD_1	0x42C11734	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_7_WORD_0	0x42C11738	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_7_WORD_1	0x42C1173C	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_8_WORD_0	0x42C11740	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_8_WORD_1	0x42C11744	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_9_WORD_0	0x42C11748	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_9_WORD_1	0x42C1174C	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_10_WORD_0	0x42C11750	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_10_WORD_1	0x42C11754	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.

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Register name	Address	Description
ETH0_TYPE2_COMPARE_11_WORD_0	0x42C11758	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_11_WORD_1	0x42C1175C	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_12_WORD_0	0x42C11760	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_12_WORD_1	0x42C11764	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_13_WORD_0	0x42C11768	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_13_WORD_1	0x42C1176C	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_14_WORD_0	0x42C11770	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_14_WORD_1	0x42C11774	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_15_WORD_0	0x42C11778	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_15_WORD_1	0x42C1177C	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_16_WORD_0	0x42C11780	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_16_WORD_1	0x42C11784	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_17_WORD_0	0x42C11788	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_17_WORD_1	0x42C1178C	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_18_WORD_0	0x42C11790	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.

Ethernet registers

Register name	Address	Description
ETH0_TYPE2_COMPARE_18_WORD_1	0x42C11794	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_19_WORD_0	0x42C11798	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_19_WORD_1	0x42C1179C	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_20_WORD_0	0x42C117A0	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_20_WORD_1	0x42C117A4	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_21_WORD_0	0x42C117A8	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_21_WORD_1	0x42C117AC	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_22_WORD_0	0x42C117B0	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_22_WORD_1	0x42C117B4	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_23_WORD_0	0x42C117B8	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_23_WORD_1	0x42C117BC	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_24_WORD_0	0x42C117C0	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_24_WORD_1	0x42C117C4	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_25_WORD_0	0x42C117C8	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_25_WORD_1	0x42C117CC	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.

Ethernet registers

Register name	Address	Description
ETH0_TYPE2_COMPARE_26_WORD_0	0x42C117D0	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_26_WORD_1	0x42C117D4	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_27_WORD_0	0x42C117D8	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_27_WORD_1	0x42C117DC	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_28_WORD_0	0x42C117E0	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_28_WORD_1	0x42C117E4	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_29_WORD_0	0x42C117E8	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_29_WORD_1	0x42C117EC	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_30_WORD_0	0x42C117F0	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_30_WORD_1	0x42C117F4	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.
ETH0_TYPE2_COMPARE_31_WORD_0	0x42C117F8	same as type2_compare_0_word_0. See ETH0_TYPE2_COMPARE_1_WORD_0 for the details of bit fields.
ETH0_TYPE2_COMPARE_31_WORD_1	0x42C117FC	same as type2_compare_0_word_1. See ETH0_TYPE2_COMPARE_1_WORD_1 for the details of bit fields.

25.1.1 ETH0_CTL

Description: EMAC Control Register

Address: 0x42C10000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [7:3]					REFCLK_SRC_SEL	ETH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REFCLK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	EMAC enable: '0': Disabled. '1': Enabled. Default Value: 0
15 : 8	REFCLK_DIV	Specify the reference clock divider. Integer division by (1+REFCLK_DIV). Allows for integer divisions in the range [1, 256]. Default Value: 0
2	REFCLK_SRC_SEL	Select the source for reference clock. 0: Reference clock comes from ref_clk input port (HSIO). 1: Reference clock comes from an internal clock source (PLL). Default Value: 0
1 : 0	ETH_MODE	Set ethernet mode. The speed of 10M/100M/1G is selected by programming NETWORK_CONFIG after IP is enabled. The field also specifies the clock source of internal transmit clock and receive clock domain. Default Value: 0 **0x0: MII :** MII mode (10/100MHz speed is determined by NETWORK_CONFIG[0]). **0x1: GMII :** GMII mode (NETWORK_CONFIG[10] must be set to enable 1G operation).

25.1.1 ETH0_CTL (continued)

0x2: RGMII :

RGMII mode (10M/100M/1G speed is determined by NETWORK_CONFIG[10] and NETWORK_CONFIG[0]).

0x3: RMII :

RMII mode (10M/100M speed is determined by NETWORK_CONFIG[0]).

25.1.2 ETH0_STATUS

Description: EMAC Status Register

Address: 0x42C10004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							PFC_NE-GOTIATE

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RX_PFC_PAUSED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	RX_PFC_PAUSED	Each bit corresponds to a priority indicated within the PFC priority based pause frame. Each bit is set when a PFC priority based pause frame has been received, and the associated priority pause time quantum is non-zero. Each bit is cleared when the associated pause time identified by the received pause time quantum has elapsed. Default Value: 0
0	PFC_NEGOTIATE	Identifies that PFC priority based pause flow control has been negotiated. 0 - No PFC priority based pause frames have yet been received, flow control is being handled using classic 802.3 pause frames. 1 - At least one PFC priority based pause frames has been received. All subsequent 802.3 pause frames will be dropped. Default Value: 0

25.1.3 ETH0_NETWORK_CONTROL

Description: The network control register contains general MAC control functions for both receiver and transmitter.

Address: 0x42C11000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	W	W	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	STATS_WRITE_EN	INC_ALL_STATS_REGS	CLEAR_ALL_STATS_REGS	MAN_PORT_EN	ENABLE_TRANSMIT	ENABLE_RECEIVE	LOOPBACK_LOCAL	LOOPBACK

Bits	15	14	13	12	11	10	9	8
SW Access	RW	R	R	W	W	W	W	RW
HW Access	R	R	R	R	R	R	R	R
Name	STORE_RX_TS	REMOVED_14	REMOVED_13	TX_PAUSE_FRAME_ZERO	TX_PAUSE_FRAME_REQ	TX_HALT_PCLK	TX_START_PCLK	BACK_PRESSURE

Bits	23	22	21	20	19	18	17	16
SW Access	R	RW	RW	RW	RW	W	W	RW
HW Access	R	R	R	R	R	R	R	R
Name	EXT_TSU_PORT_ENABLE	STORE_UDP_OFFSET	ALT_SGMII_MODE	PTP_UNICAST_ENA	TX_LPI_EN	FLUSH_RX_PKT_PCLK	TRANSMIT_PFC_PRIORITY_BASED_PAUSE_FRAME	PFC_ENABLE

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EXT_RXQ_RESERVED_31	IFG_EATS_QAV_CREDIT	TWO_PT_FIVE_GIG	SEL_MII_ON_RGMII	OSS_CORRECTION_FIELD	EXT_RXQ_SEL_EN	PFC_CTRL	ONE_STEP_SYNC_MODE

Bits	Name	Description
31	EXT_RXQ_RESERVED_31	Reserved, read as 0, ignored on write. Default Value: 0
30	IFG_EATS_QAV_CREDIT	Setting this bit high modifies the CBS algorithm so the IFG/IPG associated with a transmit frame counts towards its 802.1Qav credit. Default Value: 0
29	TWO_PT_FIVE_GIG	2.5G operation selected - setting this bit high drives the SPEED_MODE[3] top level output pin high and also adjusts the link timer in the PCS auto-negotiation block to ensure it delivers 10ms for 2500BASE-X and 1.6ms in SGMII mode, and also ensures INT_MODERATION counts 800ns periods with the speeded up MAC clocks. Default Value: 0
28	SEL_MII_ON_RGMII	If the RGMII interface being used set this bit high to configure the interface for MII operation. Default Value: 0

25.1.3 ETH0_NETWORK_CONTROL (continued)

27	OSS_CORRECTION_-FIELD	1588 One Step Correction Field Update. Set this bit high to enable updating the correction field of PTP 1588 version 2 sync frames by adding current TSU timer value. Default Value: 0
26	EXT_RXQ_SEL_EN	Enable external selection of receive queue. When this bit is high the ext_match1, ext_match2, ext_match3 and ext_match4 inputs will determine which receive queue a frame is routed to. This will be the case regardless of the state of the external address match enable bit 9 of the network config register. Note that receive frames will be dropped unless they are matched by the internal frame filtering functionality. If the external address match enable bit 9 in the network config register is set frames may be matched by an external address match filter as long as one of the ext_match1, ext_match2, ext_match3 and ext_match4 inputs is asserted early enough. When set EXT_RXQ_SEL_EN takes precedence over the existing screener functionality. This bit is only relevant if priority queuing is configured. Note: ext_match1, ext_match2, ext_match_3 and ext_match4 inputs are fixed to 0 internally. Default Value: 0
25	PFC_CTRL	"Enable multiple PFC pause quantums, one per pause priority" Default Value: 0
24	ONE_STEP_SYNC_-MODE	1588 One Step Sync Mode. Write 1 to enable. Replace timestamp field in the 1588 header for TX Sync Frames with current TSU timer value. Default Value: 0
23	EXT_TSU_PORT_EN-ABLE	Write ignore, read 0 Default Value: 0
22	STORE_UDP_OFFSET	Store UDP / TCP offset to memory. Setting this bit to one will cause the upper 16-bits of the CRC of every received frame to be replaced with the offset from start of frame to the beginning of the UDP or TCP header. The lower 16-bits of the CRC are replaced with zero and reserved for future use. The offset is measured in units of 2 bytes. Set to zero for normal operation. Default Value: 0
21	ALT_SGMII_MODE	Alternative sgmii mode. If asserted with sgmii_mode in the network control register the ACK bit is driven before ability detect during transfer of status information from the PHY to the MAC. Default Value: 0
20	PTP_UNICAST_ENA	Enable detection of unicast PTP unicast frames. Default Value: 0
19	TX_LPI_EN	Enable LPI transmission when set LPI (low power idle) is immediately transmitted. LPI is transmitted even if bit 3 transmit enable is disabled. Setting this bit also sends a pause signal to the transmit datapath. Default Value: 0
18	FLUSH_RX_PKT_PCLK	Flush the next packet from the external RX DPRAM. Writing one to this bit will only have an effect if the DMA is not currently writing a packet already stored in the DPRAM to memory. Self clearing register. Default Value: 0
17	TRANSMIT_PFC_PRIOR-ITY_BASED_PAUSE_-FRAME	Write a one to transmit PFC priority based pause frame. Takes the values stored in the Transmit PFC Pause Register. Self clearing register. Default Value: 0
16	PFC_ENABLE	Enable PFC Priority Based Pause Reception capabilities. Setting this bit will enable PFC negotiation and recognition of priority based pause frames. Default Value: 0
15	STORE_RX_TS	Store receive time stamp to memory. Setting this bit to one will cause the CRC of every received frame to be replaced with the value of the nanoseconds field of the 1588 timer that was captured as the receive frame passed the message time stamp point. Set to zero for normal operation. Default Value: 0
14	REMOVED_14	Write ignore, read 0 Default Value: 0
13	REMOVED_13	Write ignore, read 0 Default Value: 0
12	TX_PAUSE_FRAME_ZE-RO	Transmit zero quantum pause frame - writing one to this bit causes a pause frame with zero quantum to be transmitted. Default Value: 0

25.1.3 ETH0_NETWORK_CONTROL (continued)

11	TX_PAUSE_-FRAME_REQ	Transmit pause frame - writing one to this bit causes a pause frame to be transmitted. Self clearing register. Default Value: 0
10	TX_HALT_PCLK	Transmit halt - writing one to this bit halts transmission as soon as any ongoing frame transmission ends. Default Value: 0
9	TX_START_PCLK	Start transmission - writing one to this bit starts transmission. Default Value: 0
8	BACK_PRESSURE	Back pressure if set in 10M or 100M half duplex mode will force collisions on all received frames. Ignored in gigabit half duplex mode. Default Value: 0
7	STATS_WRITE_EN	Write enable for statistics registers - setting this bit to one means the statistics registers can be written for functional test purposes. Default Value: 0
6	INC_ALL_STATS_REGS	Incremental statistics registers - this bit is write only. Writing a one increments all the statistics registers by one for test purposes. Self clearing register. Default Value: 0
5	CLEAR_ALL_STATS_REGS	Clear statistics registers - this bit is write only. Writing a one clears the statistics registers. Self clearing register. Default Value: 0
4	MAN_PORT_EN	Management port enable - set to one to enable the management port. When zero forces mdio to high impedance state and mdc low. Default Value: 0
3	ENABLE_TRANSMIT	Transmit enable - when set, it enables the GEM transmitter to send data. When reset transmission will stop immediately, the transmit pipeline and control registers will be cleared and the transmit queue pointer register will reset to point to the start of the transmit descriptor list. Default Value: 0
2	ENABLE_RECEIVE	Receive enable - when set, it enables the GEM to receive data. When reset frame reception will stop immediately and the receive pipeline will be cleared. The receive queue pointer register is unaffected. Default Value: 0
1	LOOPBACK_LOCAL	Not used. Default Value: 0
0	LOOPBACK	Not used. Default Value: 0

25.1.4 ETH0_NETWORK_CONFIG

Description: The network configuration register contains functions for setting the mode of operation for the Gigabit Ethernet MAC.

Address: 0x42C11004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	UNICAST-_HASH_ENABLE	MULTI-CAST_HASH_ENABLE	NO_BROADCAST	COPY_ALL_FRAMES	JUMBO_-FRAMES	DIS-CARD_NON_VLAN_-FRAMES	FULL_DU-PLEX	SPEED

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	RW	RW	RW	RW	RW
HW Access	R		R	R	R	R	R	R
Name	RECEIVE_BUFFER_OFF-SET [15:14]		PAUSE_ENABLE	RE-TRY_TEST	PCS_SE-LECT	GIGABIT_-MODE_EN-ABLE	EXTER-NAL_AD-DRESS_MATCH_EN-ABLE	RE-CEIVE_1536_BYTE_-FRAMES

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW		RW			RW	RW
HW Access	R	R		R			R	R
Name	DISABLE_-COPY_OF_PAUSE_-FRAMES	DATA_BUS_WIDTH [22:21]		MDC_CLOCK_DIVISION [20:18]			FCS_RE-MOVE	LENGTH_-FIELD_ER-ROR_FRAME_DIS-CARD

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RE-SERVED_31	IG-NORE_IP-G_RX_ER	NSP_CHANGE	IP-G_STRETCH_ENABLE	SGMII_-MODE_EN-ABLE	IG-NORE_RX-_FCS	EN_HALF_-DUPLEX-_RX	RECEIVE_-CHECK-SUM_OFFLOAD_EN-ABLE

Bits	Name	Description
31	RESERVED_31	Reserved. Writeable register. Ignore on read. Default Value: 0
30	IGNORE_IPG_RX_ER	Ignore IPG rx_er. When set rx_er has no effect on the GEMs operation when rx_ctl is low. Set this when using the RGMII wrapper in half-duplex mode. Default Value: 0
29	NSP_CHANGE	Receive bad preamble. When set frames with non-standard preamble are not rejected. Default Value: 0
28	IPG_STRETCH_ENABLE	IPG stretch enable - when set the transmit IPG can be increased above 96 bit times depending on the previous frame length using the IPG stretch register. Default Value: 0

25.1.4 ETH0_NETWORK_CONFIG (continued)

27	SGMII_MODE_ENABLE	SGMII mode enable - changes behaviour of the auto-negotiation advertisement and link partner ability registers to meet the requirements of SGMII and reduces the duration of the link timer from 10 ms to 1.6 ms. Default Value: 0
26	IGNORE_RX_FCS	Ignore RX FCS - when set frames with FCS/CRC errors will not be rejected. FCS error statistics will still be collected for frames with bad FCS and FCS status will be recorded in frame's DMA descriptor. For normal operation this bit must be set to zero. Default Value: 0
25	EN_HALF_DUPLEX_RX	Enable frames to be received in half-duplex mode while transmitting. Default Value: 0
24	RECEIVE_CHECK-SUM_OFFLOAD_EN-ABLE	Receive checksum offload enable - when set, the receive checksum engine is enabled. Frames with bad IP, TCP or UDP checksums are discarded. Default Value: 0
23	DISABLE_-COPY_OF_PAUSE_-FRAMES	Disable copy of pause frames - set to one to prevent pause frames being copied to memory. When set, neither control frames with type id 8808, nor pause frames with destination address 010000c28001 are copied to memory. Note that valid pause frames received will still increment pause statistics and pause the transmission of frames as required. Default Value: 0
22 : 21	DATA_BUS_WIDTH	Data bus width - set according to AMBA (AXI/AHB) or external FIFO data bus width. Only valid bus widths may be written if the system is configured to a maximum width less than 128-bits. 00: 32 bit data bus width 01: 64 bit AMBA (AXI/AHB) data bus width 10: 128 bit AMBA (AXI/AHB) data bus width 11: 128 bit AMBA (AXI/AHB) data bus width. Note: When AXI interface for DMA access is supported, EMAC only supports 64b DMA data bus width, so must set it 1. When AHB interface for DMA access is supported, EMAC only supports 32b DMA data bus width, so must set it 0. (See TRM feature list for AXI/AHB interface) Default Value: 0x1
20 : 18	MDC_CLOCK_DIVISION	MDC clock division - set according to clk_sys speed. These three bits determine the number clk_sys will be divided by to generate MDC. For conformance with the 802.3 specification, MDC must not exceed 2.5 MHz (MDC is only active during MDIO read and write operations). 000: divide clk_sys by 8 (clk_sys up to 20 MHz) 001: divide clk_sys by 16 (clk_sys up to 40 MHz) 010: divide clk_sys by 32 (clk_sys up to 80 MHz) 011: divide clk_sys by 48 (clk_sys up to 120MHz) 100: divide clk_sys by 64 (clk_sys up to 160 MHz) 101: divide clk_sys by 96 (clk_sys up to 240 MHz) 110: divide clk_sys by 128 (clk_sys up to 320 MHz) 111: divide clk_sys by 224 (clk_sys up to 540 MHz). Default Value: 0x3
17	FCS_REMOVE	FCS remove - setting this bit will cause received frames to be written to memory without their frame check sequence (last 4 bytes). The frame length indicated will be reduced by four bytes in this mode. Default Value: 0
16	LENGTH_FIELD_ER-ROR_FRAME_DISCARD	Length field error frame discard - setting this bit causes frames with a measured length shorter than the extracted length field (as indicated by bytes 13 and 14 in a non-VLAN tagged frame) to be discarded. This only applies to frames with a length field less than 0x0600. Default Value: 0
15 : 14	RECEIVE_BUFFER_OFF-SET	Receive buffer offset - indicates the number of bytes by which the received data is offset from the start of the receive buffer. Default Value: 0
13	PAUSE_ENABLE	Pause enable - when set, transmission will pause if a non zero 802.3 classic pause frame is received and PFC has not been negotiated. Default Value: 0

25.1.4 ETH0_NETWORK_CONFIG (continued)

12	RETRY_TEST	Retry test - must be set to zero for normal operation. If set to one the backoff between collisions will always be one slot time. Setting this bit to one helps test the too many retries condition. Also used in the pause frame tests to reduce the pause counter's decrement time from 512 bit times, to every receive clock cycle. Default Value: 0
11	PCS_SELECT	PCS select - selects between MII/GMII and TBI Default Value: 0
10	GIGABIT_MODE_ENABLE	Gigabit mode enable - setting this bit configures the GEM for 1000 Mbps operation. 0: 10/100 operation using MII interface 1: Gigabit operation using GMI interface Default Value: 0
9	EXTERNAL_ADDRESS_MATCH_ENABLE	External address match enable - when set the external address match interface can be used to copy frames to memory. Default Value: 0
8	RECEIVE_1536_BYTE_FRAMES	Receive 1536 byte frames - setting this bit means the GEM will accept frames up to 1536 bytes in length. Normally the GEM would reject any frame above 1518 bytes. Default Value: 0
7	UNICAST_HASH_ENABLE	Unicast hash enable - when set, unicast frames will be accepted when the 6 bit hash function of the destination address points to a bit that is set in the hash register. Default Value: 0
6	MULTICAST_HASH_ENABLE	Multicast hash enable - when set, multicast frames will be accepted when the 6 bit hash function of the destination address points to a bit that is set in the hash register. Default Value: 0
5	NO_BROADCAST	No broadcast - when set to logic one, frames addressed to the broadcast address of all ones will not be accepted. Default Value: 0
4	COPY_ALL_FRAMES	Copy all frames - when set to logic one, all valid frames will be accepted. Default Value: 0
3	JUMBO_FRAMES	Jumbo frames - set to one to enable jumbo frames up to 10,240 bytes to be accepted. The default length is 10,240 bytes. Default Value: 0
2	DISCARD_NON_VLAN_FRAMES	Discard non-VLAN frames - when set only VLAN tagged frames will be passed to the address matching logic. Default Value: 0
1	FULL_DUPLEX	Full duplex - if set to logic one, the transmit block ignores the state of collision and carrier sense and allows receive while transmitting. Default Value: 0
0	SPEED	Speed - set to logic one to indicate 100Mbps operation, logic zero for 10Mbps. Default Value: 0

25.1.5 ETH0_NETWORK_STATUS

Description: The network status register returns status information with respect to the PHY management interface.

Address: 0x42C11008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R		R	R	R	R
HW Access	W	W	W		W	W	W	W
Name	LPI_INDICATE_PCLK	PFC_NEGOTIATE_PCLK	REMOVED_5_4 [5:4]		MAC_FULL_DUPLEX	MAN_DONE	MDIO_IN	PCS_LINK_STATE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	LPI_INDICATE_PCLK	LPI Indication - Low power idle has been detected on receive. This bit is set when LPI is detected and reset when normal idle is detected. An interrupt is generated when the state of this bit changes. Default Value: 0
6	PFC_NEGOTIATE_PCLK	Set when PFC Priority Based Pause has been negotiated. Default Value: 0
5 : 4	REMOVED_5_4	Reserved, read as 0, ignored on write. Default Value: 0
3	MAC_FULL_DUPLEX	PCS auto-negotiation duplex resolution. Set to one if the resolution function determines that both devices are capable of full duplex operation. If zero half-duplex operation is possible as long as bit 0 (PCS link state) is also one. Default Value: 0
2	MAN_DONE	The PHY management logic is idle (i.e. has completed). Default Value: 1
1	MDIO_IN	Returns status of the mdio pin. Default Value: 1
0	PCS_LINK_STATE	Returns status of PCS link state. If auto-negotiation is disabled this returns the synchronisation status. If auto-negotiation is enabled it is set in the LINK_OK state as long as a compatible duplex mode is resolved. Default Value: 0

25.1.6 ETH0_USER_IO_REGISTER

Description: Not presents. Access to the register will return AHB error.

Address: 0x42C1100C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	RESERVED_31_0	Write ignore, read 0 Default Value: 0

25.1.7 ETH0_DMA_CONFIG

Description: DMA Configuration Register

Address: 0x42C11010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW				
HW Access	R	R	R	R				
Name	ENDIAN_SWAP_PACKET	ENDIAN_SWAP_MANAGEMENT	HDR_DATA_SPLITTING_EN	AMBA_BURST_LENGTH [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW	RW	RW	RW	RW	
HW Access	Reserved		R	R	R	R	R	
Name	Reserved [15:14]		CRC_ERROR_REPORT	INFINITE_LAST_DBUF_SIZE_EN	TX_PBUF_TCP_EN	TX_PBUF_SIZE	RX_PBUF_SIZE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RX_BUF_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW	RW	RW	Reserved	RW	RW	RW
HW Access	Reserved	R	R	R	Reserved	R	R	R
Name	Reserved	DMA_ADDR_BUS_WIDTH_1	TX_BD_EXTENDED_MODE_EN	RX_BD_EXTENDED_MODE_EN	Reserved	FORCE_MAX_AMBA_BURST_TX	FORCE_MAX_AMBA_BURST_RX	FORCE_DISCARD_ON_ERR

Bits	Name	Description
30	DMA_ADDR_BUS_WIDTH_1	DMA address bus width. 0 = 32b, 1 = 64b. Note: EMAC only supports 32b DMA address bus width, so must set it 0. Default Value: 0
29	TX_BD_EXTENDED_MODE_EN	Enable TX extended BD mode. See TX BD control register definition for description of feature. Default Value: 0
28	RX_BD_EXTENDED_MODE_EN	Enable RX extended BD mode. See RX BD control register definition for description of feature. Default Value: 0
26	FORCE_MAX_AMBA_BURST_TX	Force max length bursts on TX. Force the TX DMA to always issue max length bursts on EOP(end of packet) or EOB(end of buffer) transfers as defined by bits 4:0 of this register, even when there is less that max burst data bytes to read. Residual data read is ignored. Does not apply on bursts that break 1k boundary rule. Default Value: 0

25.1.7 ETH0_DMA_CONFIG (continued)

25	FORCE_MAX_AMBA_BURST_RX	Force max length bursts on RX. Force the RX DMA to always issue max length bursts on EOP(end of packet) or EOB(end of buffer)transfers, even if there is less than max burst real packet data required to write. Any extra bytes of pad data is set to 0x00. Does not apply on bursts that break 1k boundary rule. Default Value: 0
24	FORCE_DISCARD_ON_ERR	Auto Discard RX pkts during lack of resource. When set, the GEM DMA will automatically discard receive packets from the receiver packet buffer memory when no AMBA (AXI/AHB) resource is available. When low, then received packets will remain to be stored in the SRAM based packet buffer until AMBA (AXI/AHB) buffer resource next becomes available. A write to this bit is ignored if the DMA is not configured in the packet buffer full store and forward mode. Default Value: 0
23 : 16	RX_BUF_SIZE	DMA receive buffer size in external AMBA (AXI/AHB) system memory. The value defined by these bits determines the size of buffer to use in main system memory when writing received data. The value is defined in multiples of 64 bytes. 0x01 corresponds to buffers of 64 bytes 0x02 corresponds to 128 bytes etc. For example: 0x02: 128 byte. 0x18: 1536 byte (1*max length frame/buffer) 0xA0: 10240 byte (1*10K jumbo frame/buffer) Note that this value should never be written as zero. Default Value: 0x18
13	CRC_ERROR_REPORT	When the bit is set, bit 16 of the receive buffer descriptor will represent FCS/CRC error (only if frames with FCS are copied to memory as enabled by bit 26 in the network config register). When this bit is clear, bit 16 of the receive buffer descriptor will represent the Canonical format indicator (CFI) bit as extracted from the receive frame (if the receive buffer descriptor is pointing to the last data buffer of the receive frame and the received frame was VLAN tagged). Default Value: 0
12	INFINITE_LAST_DBUF_SIZE_EN	Forces the DMA to consider the data buffer pointed to by last descriptor in the descriptor list to be of infinite size. Default Value: 0
11	TX_PBUF_TCP_EN	Transmitter IP, TCP and UDP checksum generation offload enable (not supported when in TX Partial Store and Forward mode). When set, the transmitter checksum generation engine is enabled, to calculate and substitute checksums for transmit frames. When clear, frame data is unaffected. If the GEM is not configured to use the DMA packet buffer, this bit is not implemented and will be treated as reserved, read as 0, ignored on write. Default Value: 0
10	TX_PBUF_SIZE	Transmitter packet buffer memory size select. Having this bit at zero halves the amount of memory used for the transmit packet buffer. This reduces the amount of memory used by the GEM. It is important to set this bit to one if the full configured physical memory is available. The value in brackets below represents the size that would result for the default maximum configured memory size of 4 Kbytes. 1: Use full configured addressable space (4 Kb) 0: Do not use top address bit (2 Kb) If the GEM is not configured to use the DMA packet buffer, this bit is not implemented and will be treated as reserved, read as 0, ignored on write. Default Value: 1
9 : 8	RX_PBUF_SIZE	Receiver packet buffer memory size select. Having these bits at less than 11 reduces the amount of memory used for the receive packet buffer. This reduces the amount of memory used by the GEM. It is important to set these bits both to one if the full configured physical memory is available. The value in brackets below represents the size that would result for the default maximum configured memory size of 8 Kbytes. 11: Use full configured addressable space (8 Kb) 10: Do not use top address bit (4 Kb) 01: Do not use top two address bits (2 Kb) 00: Do not use top three address bits (1 Kb) If the GEM is not configured to use the DMA packet buffer, these bits are not implemented and will be treated as reserved, read as 0, ignored on write. Default Value: 0x3

25.1.7 ETH0_DMA_CONFIG (continued)

7	ENDIAN_SWAP_PACKET	endian swap mode enable for packet data accesses. When set, selects swapped endianism for AMBA (AXI/AHB) transfers. When clear, selects little endian mode. Default Value: 0
6	ENDIAN_SWAP_MAN-AGEMENT	endian swap mode enable for management descriptor accesses. When set, selects swapped endianism for AMBA (AXI/AHB) transfers. When clear, selects little endian mode. Default Value: 0
5	HDR_DATA_SPLIT-TING_EN	Enable header data Splitting. When set, receive frames will be forwarded to main memory using a minimum of two DMA data buffers. The first X data buffers will contain the frame header, consisting of the Ethernet,VLAN,(IPv4 or IPv6),(TCP or UDP). X= (frame header size divided by RX-_BUF_SIZE as defined in bits 23:16 of this register). The last Y data buffers will contain the frame payload. Y= (frame payload size divided by RX_BUF_SIZE). Note that for non VLAN/IP/TCP/UDP frames, the header will always be 14 bytes. When this feature is disabled, the frame is forwarded to main memory in blocks of RX_BUF_SIZE. Note: This feature can only be set when AXI interface for DMA access is used. (See TRM feature list for AXI/AHB interface) Default Value: 0
4 : 0	AMBA_BURST_LENGTH	Selects the burst length to use on the AMBA (AHB/AXI) when transferring frame data. Not used for DMA management operations and only used where space and data size allow and respecting AXI/AHB burst boundary rules. One-hot priority encoding enforced automatically on register writes as follows, where x represents don't care: 1xxxx: Attempt to use bursts of up to 16. 01xxx: Attempt to use bursts of up to 8. 001xx: Attempt to use bursts of up to 4. 0001x: Always use SINGLE bursts. 00001: Always use SINGLE bursts. 00000: Attempt to use bursts of up to 256. Note: EMAC only supports burst length up to 16. Default Value: 0x04

25.1.8 ETH0_TRANSMIT_STATUS

Description: This register, when read, provides details of the status of a transmit. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register.

Address: 0x42C11014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	R	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	W	RW1S	RW1S	RW1S
Name	LATE_COL-LI-SION_OCC URRED	TRANS-MIT_UNDE R_RUN123	TRANS-MIT_COM-PLETE123	AMBA_ER-ROR123	TRANS-MIT_GO	RE-TRY_LIM-IT_EXCEE DED	COLLI-SION_OC-CURRED	USED_BIT_ READ

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							RW1S
Name	Reserved [15:9]							RE-SP_NOT_O K123

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	RESP_NOT_OK123	bresp/hresp not OK - set when BRESP (AXI write response) or HRESP (AHB read/write response) is detected as not OK on AXI/AHB interface for DMA access. Cleared by writing a one to this bit. Default Value: 0
7	LATE_COLLISION_OC-CURRED	Late collision occurred - only set if the condition occurs in gigabit mode, as retry is not attempted. Cleared by writing a one to this bit. Default Value: 0
6	TRANS-MIT_UNDER_RUN123	Transmit under run - this bit is set if the transmitter was forced to terminate a frame that it had already began transmitting due to further data being unavailable. This bit is set if a transmitter status write back has not completed when another status write back is attempted. When using the DMA interface configured for packet buffer mode, this bit will never be set. Cleared by writing a 1. Default Value: 0
5	TRANSMIT_COM-PLETE123	Transmit complete - set when a frame has been transmitted. Cleared by writing a one to this bit. Default Value: 0

25.1.8 ETH0_TRANSMIT_STATUS (continued)

4	AMBA_ERROR123	Transmit frame corruption due to AMBA (AXI/AHB) errors. Set if an error occurs whilst midway through reading transmit frame from external memory including HRESP (read/write response on AHB interface for DMA access), RRESP or BRESP (read/write response on AXI interface for DMA access) errors and buffers exhausted mid frame (if the buffers run out during transmission of a frame then transmission stops, FCS shall be bad and tx_er asserted). Also set in DMA packet buffer mode if single frame is too large for configured packet buffer memory size. Cleared by writing a one to this bit. Default Value: 0
3	TRANSMIT_GO	Transmit go - if high transmit is active. When using the exposed FIFO interface, this bit represents bit 3 of the network control register. When using the DMA interface this bit represents the tx_go variable as specified in the transmit buffer description. Default Value: 0
2	RETRY_LIMIT_EXCEEDED	Retry limit exceeded - cleared by writing a one to this bit. Default Value: 0
1	COLLISION_OCCURRED	Collision occurred - set by the assertion of collision. Cleared by writing a one to this bit. When operating in 10/100 mode, this status indicates either a collision or a late collision. In gigabit mode, this status is not set for a late collision. Default Value: 0
0	USED_BIT_READ	Used bit read - set when a transmit buffer descriptor is read with its used bit set. Cleared by writing a one to this bit. Default Value: 0

25.1.9 ETH0_RECEIVE_Q_PTR

Description: This register holds the start address of the receive buffer queue (receive buffers descriptor list). The receive buffer queue base address must be initialized before receive is enabled through bit 2 of the network control register. Once reception is enabled, any write to the receive buffer queue base address register is ignored. Reading this register returns the location of the descriptor currently being accessed. This value increments as buffers are used. Software should not use this register for determining where to remove received frames from the queue as it constantly changes as new frames are received. Software should instead work its way through the buffer descriptor queue checking the used bits. In terms of AMBA (AXI) operation, the receive descriptors are read from memory using a single 32bit AXI access. When the datapath is configured at 64bit, the receive descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is written to using a single 64bit AXI access.

Address: 0x42C11018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	RW
HW Access	R						Reserved	R
Name	DMA_RX_Q_PTR [7:2]						Reserved	DMA_RX_DIS_Q

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DMA_RX_Q_PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DMA_RX_Q_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DMA_RX_Q_PTR [31:24]							

Bits	Name	Description
31 : 2	DMA_RX_Q_PTR	Receive buffer queue base address - written with the address of the start of the receive queue. Default Value: 0x00000000
0	DMA_RX_DIS_Q	Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while receive is not enabled. Default Value: 0

25.1.10 ETH0_TRANSMIT_Q_PTR

Description: This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit, the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.

Address: 0x42C1101C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	RW
HW Access	R						Reserved	R
Name	DMA_TX_Q_PTR [7:2]						Reserved	DMA_TX_DIS_Q

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DMA_TX_Q_PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DMA_TX_Q_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DMA_TX_Q_PTR [31:24]							

Bits	Name	Description
31 : 2	DMA_TX_Q_PTR	Transmit buffer queue base address - written with the address of the start of the transmit queue. Default Value: 0x00000000
0	DMA_TX_DIS_Q	Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while transmit is not enabled. Default Value: 0

25.1.11 ETH0_RECEIVE_STATUS

Description: This register, when read provides details of the status of a receive. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register.

Address: 0x42C11020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW1C	RW1C	RW1C	RW1C
HW Access	Reserved				RW1S	RW1S	RW1S	RW1S
Name	Reserved [7:4]				RE-SP_NOT_OK1234	RE-CEIVE_OVERRUN123	FRAME_RECEIVED	BUFFER_NOT_AVAIL-ABLE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	RESP_NOT_OK1234	bresp/hresp not OK - set when BRESP (AXI write response) or HRESP (AHB read/write response) is detected as not OK on AXI/AHB interface for DMA access. Cleared by writing a one to this bit. Default Value: 0
2	RECEIVE_OVERRUN123	Receive overrun - this bit is set if either the gem_dma RX FIFO or external RX FIFO were unable to store the receive frame due to a FIFO overflow, or if the receive status, reported by the gem_rx module to the gem_dma was not taken at end of frame. This bit is also set in DMA packet buffer mode if the packet buffer overflows. For DMA operation the buffer will be recovered if an overrun occurs. This bit is cleared by writing a one to it. Default Value: 0
1	FRAME_RECEIVED	Frame received - one or more frames have been received and placed in memory. Cleared by writing a one to this bit. Default Value: 0
0	BUFFER_NOT_AVAIL-ABLE	Buffer not available - an attempt was made to get a new buffer and the pointer indicated that it was owned by the processor. The DMA will reread the pointer each time an end of frame is received until a valid pointer is found. This bit is set following each descriptor read attempt that fails, even if consecutive pointers are unsuccessful and software has in the mean time cleared the status flag. Cleared by writing a one to this bit. Default Value: 0

25.1.12 ETH0_INT_STATUS

Description: If not configured for priority queueing, the GEM generates a single interrupt. This register indicates the source of this interrupt. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the ethernet_int signal will be asserted. For test purposes each bit can be set or reset by writing to the interrupt mask register. The default configuration is shown below whereby all bits are reset to zero on read. Changing the validity of the `gem_irq_read_clear define will instead require a one to be written to the appropriate bit in order to clear it. In this mode reading has no affect on the status of the bit.

Address: 0x42C11024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	TRANSMIT_COMPLETE	AMBA_ERROR	RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION	TRANSMIT_UNDER_RUN	TX_USED_BIT_READ	RX_USED_BIT_READ	RECEIVE_COMPLETE	MANAGEMENT_FRAME_SENT

Bits	15	14	13	12	11	10	9	8
SW Access	R	W1C	W1C	W1C	W1C	W1C	R	Reserved
HW Access	R	RW1S	RW1S	RW1S	RW1S	RW1S	R	Reserved
Name	REMOVED_15	PAUSE_FRAME_TRANSMITTED	PAUSE_TIME_ELAPSED	PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_RECEIVED	RESP_NOT_OK	RECEIVE_OVERRUN	REMOVED_9	Reserved

Bits	23	22	21	20	19	18	17	16
SW Access	W1C	W1C	W1C	W1C	W1C	W1C	R	R
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	R	R
Name	PTP_PDELAY_RESP_FRAME_RECEIVED	PTP_PDELAY_REQ_FRAME_RECEIVED	PTP_SYNC_FRAME_TRANSMITTED	PTP_DELAY_REQ_FRAME_TRANSMITTED	PTP_SYNC_FRAME_RECEIVED	PTP_DELAY_REQ_FRAME_RECEIVED	REMOVED_17	REMOVED_16

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		W1C	R	W1C	W1C	W1C	W1C
HW Access	Reserved		RW1S	R	RW1S	RW1S	RW1S	RW1S
Name	Reserved [31:30]		TSU_TIMER_COMPARISON_INTERRUPT	REMOVED_28	RECEIVE_LPI_INDICATION_STATUS_BIT_CHANGE	TSU_SECONDS_REGISTER_INCREMENT	PTP_PDELAY_RESP_FRAME_TRANSMITTED	PTP_PDELAY_REQ_FRAME_TRANSMITTED

Bits	Name	Description
29	TSU_TIMER_COMPARISON_INTERRUPT	TSU timer comparison interrupt. Indicates when TSU timer count value is equal to programmed value. Default Value: 0

25.1.12 ETH0_INT_STATUS (continued)

28	REMOVED_28	Write ignore, read 0 Default Value: 0
27	RECEIVE_LPI_INDICATION_STATUS_BIT_CHANGE	Receive LPI indication status bit change Default Value: 0
26	TSU_SECONDS_REGISTER_INCREMENT	TSU seconds register increment indicates the register has incremented. Cleared on read. Default Value: 0
25	PTP_PDELAY_RESP_FRAME_TRANSMITTED	PTP pdelay_resp frame transmitted indicates a PTP pdelay_resp frame has been transmitted. Cleared on read. Default Value: 0
24	PTP_PDELAY_REQ_FRAME_TRANSMITTED	PTP pdelay_req frame transmitted indicates a PTP pdelay_req frame has been transmitted. Cleared on read. Default Value: 0
23	PTP_PDELAY_RESP_FRAME_RECEIVED	PTP pdelay_resp frame received indicates a PTP pdelay_resp frame has been received. Cleared on read. Default Value: 0
22	PTP_PDELAY_REQ_FRAME_RECEIVED	PTP pdelay_req frame received indicates a PTP pdelay_req frame has been received. Cleared on read. Default Value: 0
21	PTP_SYNC_FRAME_TRANSMITTED	PTP sync frame transmitted indicates a PTP sync frame has been transmitted. Cleared on read. Default Value: 0
20	PTP_DELAY_REQ_FRAME_TRANSMITTED	PTP delay_req frame transmitted indicates a PTP delay_req frame has been transmitted. Cleared on read. Default Value: 0
19	PTP_SYNC_FRAME_RECEIVED	PTP sync frame received indicates a PTP sync frame has been received. Cleared on read. Default Value: 0
18	PTP_DELAY_REQ_FRAME_RECEIVED	PTP delay_req frame received indicates a PTP delay_req frame has been received. Cleared on read. Default Value: 0
17	REMOVED_17	Write ignore, read 0 Default Value: 0
16	REMOVED_16	Write ignore, read 0 Default Value: 0
15	REMOVED_15	Write ignore, read 0 Default Value: 0
14	PAUSE_FRAME_TRANSMITTED	Pause frame transmitted - indicates a pause frame has been successfully transmitted after being initiated from the network control register. Cleared on read. Default Value: 0
13	PAUSE_TIME_ELAPSED	Pause Time elapsed. set when either the pause time register at address 0x38 decrements to zero, or when a valid pause frame is received with a zero pause quantum field. Cleared on read. Default Value: 0
12	PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_RECEIVED	Pause frame with non-zero pause quantum received - indicates a valid pause has been received that has a non-zero pause quantum field. Cleared on read. Default Value: 0
11	RESP_NOT_OK	bresp/hresp not OK - set when BRESP (AXI write response) or HRESP (AHB read/write response) is detected as not OK on AXI/AHB interface for DMA access. Cleared on read. Default Value: 0
10	RECEIVE_OVERRUN	Receive overrun - set when the receive overrun status bit gets set. Cleared on read. Default Value: 0
9	REMOVED_9	Write ignore, read 0 Default Value: 0
7	TRANSMIT_COMPLETE	Transmit complete - set when a frame has been transmitted. Cleared on read. Default Value: 0

25.1.12 ETH0_INT_STATUS (continued)

6	AMBA_ERROR	Transmit frame corruption due to AMBA (AXI/AHB) error. Set if an error occurs whilst midway through reading transmit frame from external system memory, including HRESP (AHB), RRESP or BRESP(AXI) errors and buffers exhausted mid frame (if the buffers run out during transmission of a frame then transmission stops, FCS shall be bad and tx_er asserted). Also set in DMA packet buffer mode if single frame is too large for configured packet buffer memory size. Cleared on a read. Default Value: 0
5	RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION	Retry limit exceeded or late collision - transmit error. Late collision will only cause this status bit to be set in gigabit mode (as a retry is not attempted). Cleared on read. Default Value: 0
4	TRANSMIT_UNDER_RUN	Transmit under run - this interrupt is set if the transmitter was forced to terminate a frame that it has already began transmitting due to further data being unavailable. If an under run occurs, the transmitter will force bad crc and tx_er high. This interrupt is set if a transmitter status write back has not completed when another status write back is attempted. When using the DMA interface configured for internal FIFO mode, this interrupt is also set when the transmit DMA has written the SOP data into the FIFO and either the AHB bus was not granted in time for further data, or because an AHB/AXI error response was returned by the connected slave, or because a used bit was read. When using the DMA interface configured for packet buffer mode, this bit will never be set. Cleared on read. Default Value: 0
3	TX_USED_BIT_READ	TX used bit read - set when a transmit buffer descriptor is read with its used bit set. Cleared on read. Default Value: 0
2	RX_USED_BIT_READ	RX used bit read - set when a receive buffer descriptor is read with its used bit set. Cleared on read. Default Value: 0
1	RECEIVE_COMPLETE	Receive complete - a frame has been stored in memory. Cleared on read. Default Value: 0
0	MANAGEMENT_FRAME_SENT	Management frame sent - the PHY maintenance register has completed its operation. Cleared on read. Default Value: 0

25.1.13 ETH0_INT_ENABLE

Description: At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero.

Address: 0x42C11028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	W	W	W	W	W	W	W
HW Access	R	R	R	R	R	R	R	R
Name	ENABLE_TRANSMIT_COMPLETE_INTERRUPT	ENABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT	ENABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT	ENABLE_TRANSMIT_BUFFER_UNDERRUN_INTERRUPT	ENABLE_TRANSMIT_USED_BIT_READ_INTERRUPT	ENABLE_RECEIVE_USED_BIT_READ_INTERRUPT	ENABLE_RECEIVE_COMPLETE_INTERRUPT	ENABLE_MANAGEMENT_DONE_INTERRUPT

Bits	15	14	13	12	11	10	9	8
SW Access	W	W	W	W	W	W	W	W
HW Access	R	R	R	R	R	R	R	R
Name	UNUSED_15	ENABLE_PAUSE_FRAME_TRANSMITTED_INTERRUPT	ENABLE_PAUSE_TIME_ZERO_INTERRUPT	ENABLE_PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_INTERRUPT	ENABLE_RESP_NOT_OK_INTERRUPT	ENABLE_RECEIVE_OVERRUN_INTERRUPT	UNUSED_9	UNUSED_8

Bits	23	22	21	20	19	18	17	16
SW Access	W	W	W	W	W	W	W	W
HW Access	R	R	R	R	R	R	R	R
Name	ENABLE_PTP_PDELAY_RESP_FRAME_RECEIVED	ENABLE_PTP_PDELAY_REQ_FRAME_RECEIVED	ENABLE_PTP_SYNC_FRAME_TRANSMITTED	ENABLE_PTP_DELAY_REQ_FRAME_TRANSMITTED	ENABLE_PTP_SYNC_FRAME_RECEIVED	ENABLE_PTP_DELAY_REQ_FRAME_RECEIVED	UNUSED_17	UNUSED_16

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		W	W	W	W	W	W
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [31:30]		ENABLE_TSU_TIMER_COMPARISON_INTERRUPT	UNUSED_28	ENABLE_RX_LPI_INDICATION_INTERRUPT	ENABLE_TSU_SECONDS_REGISTER_INCREMENT	ENABLE_PTP_PDELAY_RESP_FRAME_TRANSMITTED	ENABLE_PTP_PDELAY_REQ_FRAME_TRANSMITTED

25.1.13 ETH0_INT_ENABLE (continued)

Bits	Name	Description
29	ENABLE_TSU_TIMER_-COMPARISON_INTER-RUPT	Enable TSU timer comparison interrupt. Default Value: 0
28	UNUSED_28	Not used Default Value: 0
27	ENABLE_RX_LPI_INDI-CATION_INTERRUPT	Enable RX LPI indication interrupt Default Value: 0
26	ENABLE_TSU_SEC-ONDS_REGISTER_IN-CREMENT	Enable TSU seconds register increment Default Value: 0
25	ENABLE_PTP_PDE-LAY_RESP_-FRAME_TRANSMITTED	Enable PTP pdelay_resp frame transmitted Default Value: 0
24	ENABLE_PTP_PDE-LAY_REQ_-FRAME_TRANSMITTED	Enable PTP pdelay_req frame transmitted Default Value: 0
23	ENABLE_PTP_PDE-LAY_RESP_FRAME_RE-CEIVED	Enable PTP pdelay_resp frame received Default Value: 0
22	ENABLE_PTP_PDE-LAY_REQ_FRAME_RE-CEIVED	Enable PTP pdelay_req frame received Default Value: 0
21	ENABLE_PTP_SYNC_-FRAME_TRANSMITTED	Enable PTP sync frame transmitted Default Value: 0
20	ENABLE_PTP_DE-LAY_REQ_-FRAME_TRANSMITTED	Enable PTP delay_req frame transmitted Default Value: 0
19	ENABLE_PTP_SYNC_-FRAME_RECEIVED	Enable PTP sync frame received Default Value: 0
18	ENABLE_PTP_DE-LAY_REQ_FRAME_RE-CEIVED	Enable PTP delay_req frame received Default Value: 0
17	UNUSED_17	Not used Default Value: 0
16	UNUSED_16	Not used Default Value: 0
15	UNUSED_15	Not used Default Value: 0
14	ENABLE_PAUSE_-FRAME_TRANSMIT-TED_INTERRUPT	Enable pause frame transmitted interrupt Default Value: 0
13	ENABLE_PAUSE_-TIME_ZERO_INTER-RUPT	Enable pause time zero interrupt Default Value: 0
12	ENABLE_PAUSE_-FRAME_WITH_NON_ZE-RO_PAUSE_QUANTUM_I NTERRUPT	Enable pause frame with non-zero pause quantum interrupt Default Value: 0
11	ENABLE_RE-SP_NOT_OK_INTER-RUPT	Enable bresp/hresp not OK interrupt Default Value: 0

25.1.13 ETH0_INT_ENABLE (continued)

10	ENABLE_RECEIVE_OVERRUN_INTERRUPT	Enable receive overrun interrupt Default Value: 0
9	UNUSED_9	Not used Default Value: 0
8	UNUSED_8	Not used Default Value: 0
7	ENABLE_TRANSMIT_COMPLETE_INTERRUPT	Enable transmit complete interrupt Default Value: 0
6	ENABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT	Enable transmit frame corruption due to AMBA (AXI/AHB) error interrupt Default Value: 0
5	ENABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT	Enable retry limit exceeded or late collision interrupt Default Value: 0
4	ENABLE_TRANSMIT_BUFFER_UNDER_RUN_INTERRUPT	Enable transmit buffer under run interrupt Default Value: 0
3	ENABLE_TRANSMIT_USED_BIT_READ_INTERRUPT	Enable transmit used bit read interrupt Default Value: 0
2	ENABLE_RECEIVE_USED_BIT_READ_INTERRUPT	Enable receive used bit read interrupt Default Value: 0
1	ENABLE_RECEIVE_COMPLETE_INTERRUPT	Enable receive complete interrupt Default Value: 0
0	ENABLE_MANAGEMENT_DONE_INTERRUPT	Enable management done interrupt Default Value: 0

25.1.14 ETH0_INT_DISABLE

Description: Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero.

Address: 0x42C1102C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	W	W	W	W	W	W	W
HW Access	R	R	R	R	R	R	R	R
Name	DISABLE_TRANSMIT_COMPLETE_INTERRUPT	DISABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT	DISABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT	DISABLE_TRANSMIT_BUFFER_UNDER_RUN_INTERRUPT	DISABLE_TRANSMIT_USED_BIT_READ_INTERRUPT	DISABLE_RECEIVE_USED_BIT_READ_INTERRUPT	DISABLE_RECEIVE_COMPLETE_INTERRUPT	DISABLE_MANAGEMENT_DONE_INTERRUPT

Bits	15	14	13	12	11	10	9	8
SW Access	W	W	W	W	W	W	W	W
HW Access	R	R	R	R	R	R	R	R
Name	UNUSED_15	DISABLE_PAUSE_FRAME_TRANSMITTED_INTERRUPT	DISABLE_PAUSE_TIME_ZERO_INTERRUPT	DISABLE_PAUSE_FRAME_WITH_NON_ZERO_PAUSE_QUANTUM_INTERRUPT	DISABLE_RESP_NOT_OK_INTERRUPT	DISABLE_RECEIVE_OVERRUN_INTERRUPT	UNUSED_9	UNUSED_8

Bits	23	22	21	20	19	18	17	16
SW Access	W	W	W	W	W	W	W	W
HW Access	R	R	R	R	R	R	R	R
Name	DISABLE_PTP_PDELAY_RESP_FRAME_RECEIVED	DISABLE_PTP_PDELAY_REQ_FRAME_RECEIVED	DISABLE_PTP_SYNC_FRAME_TRANSMITTED	DISABLE_PTP_DELAY_REQ_FRAME_TRANSMITTED	DISABLE_PTP_SYNC_FRAME_RECEIVED	DISABLE_PTP_DELAY_REQ_FRAME_RECEIVED	UNUSED_17	UNUSED_16

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	W	W	W	W	W	W
HW Access	R	R	R	R	R	R	R	R
Name	RESERVED_31_31	RESERVED_30_30	DISABLE_TSU_TIMER_COMPARISON_INTERRUPT	UNUSED_28	DISABLE_RX_LPI_INDICATION_INTERRUPT	DISABLE_TSU_SECONDS_REGISTER_INCREMENT	DISABLE_PTP_PDELAY_RESP_FRAME_TRANSMITTED	DISABLE_PTP_PDELAY_REQ_FRAME_TRANSMITTED

Bits	Name	Description

25.1.14 ETH0_INT_DISABLE (continued)

31	RESERVED_31_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	RESERVED_30_30	"Reserved, read as 0, ignored on write." Default Value: 0
29	DISABLE_TSU_TIMER_- COMPARISON_INTER- RUPT	"Disable TSU timer comparison interrupt." Default Value: 0
28	UNUSED_28	Not used Default Value: 0
27	DISABLE_RX_LPI_INDI- CATION_INTERRUPT	"Disable RX LPI indication interrupt" Default Value: 0
26	DISABLE_TSU_SEC- ONDS_REGISTER_IN- CREMENT	"Disable TSU seconds register increment" Default Value: 0
25	DISABLE_PTP_PDE- LAY_RESP_- FRAME_TRANSMITTED	"Disable PTP pdelay_resp frame transmitted" Default Value: 0
24	DISABLE_PTP_PDE- LAY_REQ_- FRAME_TRANSMITTED	"Disable PTP pdelay_req frame transmitted" Default Value: 0
23	DISABLE_PTP_PDE- LAY_RESP_FRAME_RE- CEIVED	"Disable PTP pdelay_resp frame received" Default Value: 0
22	DISABLE_PTP_PDE- LAY_REQ_FRAME_RE- CEIVED	"Disable PTP pdelay_req frame received" Default Value: 0
21	DISABLE_PTP_SYNC_- FRAME_TRANSMITTED	"Disable PTP sync frame transmitted " Default Value: 0
20	DISABLE_PTP_DE- LAY_REQ_- FRAME_TRANSMITTED	"Disable PTP delay_req frame transmitted " Default Value: 0
19	DISABLE_PTP_SYNC_- FRAME_RECEIVED	"Disable PTP sync frame received" Default Value: 0
18	DISABLE_PTP_DE- LAY_REQ_FRAME_RE- CEIVED	"Disable PTP delay_req frame received" Default Value: 0
17	UNUSED_17	Not used Default Value: 0
16	UNUSED_16	Not used Default Value: 0
15	UNUSED_15	Not used Default Value: 0
14	DISABLE_PAUSE_- FRAME_TRANSMIT- TED_INTERRUPT	"Disable pause frame transmitted interrupt" Default Value: 0
13	DISABLE_PAUSE_- TIME_ZERO_INTER- RUPT	"Disable pause time zero interrupt" Default Value: 0
12	DISABLE_PAUSE_- FRAME_WITH_NON_ZE- RO_PAUSE_QUANTUM_I NTERRUPT	"Disable pause frame with non-zero pause quantum interrupt" Default Value: 0

25.1.14 ETH0_INT_DISABLE (continued)

11	DISABLE_RESP_NOT_OK_INTERRUPT	"Disable bresp/hresp not OK interrupt" Default Value: 0
10	DISABLE_RECEIVE_OVERRUN_INTERRUPT	"Disable receive overrun interrupt" Default Value: 0
9	UNUSED_9	Not used Default Value: 0
8	UNUSED_8	Not used Default Value: 0
7	DISABLE_TRANSMIT_COMPLETE_INTERRUPT	"Disable transmit complete interrupt" Default Value: 0
6	DISABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT	"Disable transmit frame corruption due to AMBA (AHB/AXI) error interrupt" Default Value: 0
5	DISABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT	"Disable retry limit exceeded or late collision interrupt" Default Value: 0
4	DISABLE_TRANSMIT_BUFFER_UNDER_RUN_INTERRUPT	"Disable transmit buffer under run interrupt" Default Value: 0
3	DISABLE_TRANSMIT_USED_BIT_READ_INTERRUPT	"Disable transmit used bit read interrupt" Default Value: 0
2	DISABLE_RECEIVE_USED_BIT_READ_INTERRUPT	"Disable receive used bit read interrupt" Default Value: 0
1	DISABLE_RECEIVE_COMPLETE_INTERRUPT	"Disable receive complete interrupt" Default Value: 0
0	DISABLE_MANAGEMENT_DONE_INTERRUPT	"Disable management done interrupt" Default Value: 0

25.1.15 ETH0_INT_MASK

Description: The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register.

Address: 0x42C11030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	TRANS-MIT_COM-PLETE_INT ER-RUPT_MAS K	AMBA_ER-ROR_IN-TERRUPT_ MASK	RE-TRY_LIM-IT_EXCEE DED_OR_L ATE_COL-LI-SION_MAS K	TRANS-MIT_BUFF ER_UNDER _RUN_IN-TER-RUPT_MAS K	TRANS-MIT_USED _BIT_READ _INTER-RUPT_MAS K	RE-CEIVE_US ED_BIT_RE AD_INTER-RUPT_MAS K	RECEIVE_-COM-PLETE_INT ER-RUPT_MAS K	MANAGE-MENT_-DONE_INT ER-RUPT_MAS K

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	UN-USED_15	PAUSE_-FRAME_TR ANSMIT-TED_IN-TERRUPT_ MASK	PAUSE_-TIME_ZE-RO_INTER RUPT_MAS K	PAUSE_-FRAME_WI TH_NON_Z ERO_PAUS E_QUAN-TUM_IN-TERRUPT_ MASK	RE-SP_NOT_O K_INTER-RUPT_MAS K	RE-CEIVE_OV ERRUN_IN-TER-RUPT_MAS K	UNUSED_9	UNUSED_8

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PTP_PDE-LAY_RE-SP_FRAME _RE-CEIVED_M ASK	PTP_PDE-LAY_REQ_-FRAME_RE CEIVED_M ASK	PTP_SYN-C_-FRAME_TR ANSMIT-TED_MASK	PTP_DE-LAY_REQ_-FRAME_TR ANSMIT-TED_MASK	PTP_SYN-C_-FRAME_RE CEIVED_M ASK	PTP_DE-LAY_REQ_-FRAME_RE CEIVED_M ASK	UN-USED_17	UN-USED_16

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R	R	R	R	R	R
HW Access	Reserved		W	W	W	W	W	W
Name	Reserved [31:30]		TSU_TIM-ER_COM-PARISON_ MASK	UN-USED_28	RX-_LPI_INDI-CATION_M ASK	TSU_SEC-ONDS_RE GIS-TER_IN-CREMENT_ MASK	PTP_PDE-LAY_RE-SP_FRAME _TRANS-MIT-TED_MASK	PTP_PDE-LAY_REQ_-FRAME_TR ANSMIT-TED_MASK

Bits	Name	Description

25.1.15 ETH0_INT_MASK (continued)

29	TSU_TIMER_COMPARISON_MASK	Enable TSU timer comparison interrupt mask. Default Value: 1
28	UNUSED_28	unused Default Value: 1
27	RX_LPI_INDICATION_MASK	A read of this register returns the value of the RX LPI indication mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written Default Value: 1
26	TSU_SECONDS_REGISTER_INCREMENT_MASK	A read of this register returns the value of the TSU seconds register increment mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
25	PTP_PDELAY_RESP_FRAME_TRANSMITTED_MASK	A read of this register returns the value of the PTP pdelay_resp frame transmitted mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
24	PTP_PDELAY_REQ_FRAME_TRANSMITTED_MASK	A read of this register returns the value of the PTP pdelay_req frame transmitted mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
23	PTP_PDELAY_RESP_FRAME_RECEIVED_MASK	A read of this register returns the value of the PTP pdelay_resp frame received mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
22	PTP_PDELAY_REQ_FRAME_RECEIVED_MASK	A read of this register returns the value of the PTP pdelay_req frame received mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
21	PTP_SYNC_FRAME_TRANSMITTED_MASK	A read of this register returns the value of the PTP sync frame transmitted mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
20	PTP_DELAY_REQ_FRAME_TRANSMITTED_MASK	A read of this register returns the value of the PTP delay_req frame transmitted mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
19	PTP_SYNC_FRAME_RECEIVED_MASK	A read of this register returns the value of the PTP sync frame received mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1

25.1.15 ETH0_INT_MASK (continued)

18	PTP_DELAY_REQ_-FRAME_RE-CEIVED_MASK	A read of this register returns the value of the PTP delay_req frame received mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
17	UNUSED_17	Not used Default Value: 1
16	UNUSED_16	Not used Default Value: 1
15	UNUSED_15	Not used Default Value: 1
14	PAUSE_FRAME_TRANS-MITTED_INTER-RUPT_MASK	pause frame transmitted interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
13	PAUSE_TIME_ZERO_IN-TERRUPT_MASK	pause time zero interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
12	PAUSE_-FRAME_WITH_NON_ZE-RO_PAUSE_QUANTUM_I NTERRUPT_MASK	pause frame with non-zero pause quantum interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
11	RESP_NOT_OK_INTER-RUPT_MASK	bresp not OK interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
10	RECEIVE_OVERRUN_IN-TERRUPT_MASK	receive overrun interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
9	UNUSED_9	Not used Default Value: 1
8	UNUSED_8	Not used Default Value: 1
7	TRANSMIT_COM-PLETE_INTER-RUPT_MASK	transmit complete interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
6	AMBA_ERROR_INTER-RUPT_MASK	transmit frame corruption due to AMBA (AXI/AHB) error interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1

25.1.15 ETH0_INT_MASK (continued)

5	RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_MASK	A read of this register returns the value of the retry limit exceeded or late collision (gigabit mode only) interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
4	TRANSMIT_BUFFER_UNDER_RUN_INTERRUPT_MASK	transmit buffer under run interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
3	TRANSMIT_USED_BIT_READ_INTERRUPT_MASK	transmit used bit read interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
2	RECEIVE_USED_BIT_READ_INTERRUPT_MASK	receive used bit read interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
1	RECEIVE_COMPLETE_INTERRUPT_MASK	receive complete interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
0	MANAGEMENT_DONE_INTERRUPT_MASK	management done interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1

25.1.16 ETH0_PHY_MANAGEMENT

Description: The PHY maintenance register is implemented as a shift register. Writing to the register starts a shift operation which is signalled as complete when bit-2 is set in the network status register. It takes about 2000 pclk cycles to complete, when MDC is set for pclk divide by 32 in the network configuration register. An interrupt is generated upon completion. During this time, the MSB of the register is output on the MDIO pin and the LSB updated from the MDIO pin with each MDC cycle. This causes transmission of a PHY management frame on MDIO. See Section 22.2.4.5 of the IEEE 802.3 standard. Reading during the shift operation will return the current contents of the shift register. At the end of management operation, the bits will have shifted back to their original locations. For a read operation, the data bits will be updated with data read from the PHY. It is important to write the correct values to the register to ensure a valid PHY management frame is produced. The MDIO interface can read IEEE 802.3 clause 45 PHYs as well as clause 22 PHYs. To read clause 45 PHYs, bit 30 should be written with a 0 rather than a 1. For a description of MDC generation, see Network Configuration Register.

Address: 0x42C11034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PHY_WRITE_READ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PHY_WRITE_READ_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW					RW	
HW Access	R	R					R	
Name	PHY_ADDRESS	REGISTER_ADDRESS [22:18]					WRITE10 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		RW			
HW Access	R	R	R		R			
Name	WRITE0	WRITE1	OPERATION [29:28]		PHY_ADDRESS [27:24]			

Bits	Name	Description
31	WRITE0	Must be written with 0. Default Value: 0
30	WRITE1	Must be written to 1 for a valid Clause 22 frame and to 0 for a valid Clause 45 frame. Default Value: 0
29 : 28	OPERATION	Operation. For a Clause 45 frame: 00 is an addr, 01 is a write, 10 is a post read increment, 11 is a read frame. For a Clause 22 frame: 10 is a read, 01 is a write. Default Value: 0x0
27 : 23	PHY_ADDRESS	PHY address. Default Value: 0x00
22 : 18	REGISTER_ADDRESS	Register address - specifies the register in the PHY to access. Default Value: 0x00
17 : 16	WRITE10	Must be written with 10. Default Value: 0x0
15 : 0	PHY_WRITE_READ_DATA	For a write operation this is written with the data to be written to the PHY. After a read operation this contains the data read from the PHY. Default Value: 0x0000

25.1.17 ETH0_PAUSE_TIME

Description: Received Pause Quantum Register

Address: 0x42C11038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	QUANTUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	QUANTUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	QUANTUM	Received pause quantum - stores the current value of the received pause quantum register which is decremented every 512 bit times. Default Value: 0x0000

25.1.18 ETH0_TX_PAUSE_QUANTUM

Description: Transmit Pause Quantum Register

Address: 0x42C1103C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	QUANTUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	QUANTUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	QUANTUM_P1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	QUANTUM_P1 [31:24]							

Bits	Name	Description
31 : 16	QUANTUM_P1	Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 1. Default Value: 0xFFFF
15 : 0	QUANTUM	Transmit pause quantum - written with the pause quantum value for pause frame transmission. Default Value: 0xFFFF

25.1.19 ETH0_PBUF_TXCUTTHRU

Description: Partial store and forward is only applicable when using the DMA configured in SRAM based packet buffer mode. It is also not available when using multi buffer frames. TX Partial Store and Forward

Address: 0x42C11040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DMA_TX_CUTTHRU_THRESHOLD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							DMA_TX-_CUT-THRU_THRESHOLD

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	DMA_TX-_CUTTHRU	Reserved [30:24]						

Bits	Name	Description
31	DMA_TX_CUTTHRU	Enable TX partial store and forward operation Default Value: 0
8 : 0	DMA_TX_CUTTHRU_-THRESHOLD	Watermark value. This value must be >= 0x9. Default Value: 0x1FF

25.1.20 ETH0_PBUF_RXCUTTHRU

Description: RX Partial Store and Forward

Address: 0x42C11044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DMA_RX_CUTTHRU_THRESHOLD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	DMA_RX-_CUTTHRU	Reserved [30:24]						

Bits	Name	Description
31	DMA_RX_CUTTHRU	Enable RX partial store and forward operation Default Value: 0
7 : 0	DMA_RX_CUTTHRU_-THRESHOLD	Watermark value. Default Value: 0xFF

25.1.21 ETH0_JUMBO_MAX_LENGTH

Description: Maximum Jumbo Frame Size.

Address: 0x42C11048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	JUMBO_MAX_LENGTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		JUMBO_MAX_LENGTH [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
13 : 0	JUMBO_MAX_LENGTH	Maximum Jumbo Frame Size Default Value: 0x600

25.1.22 ETH0_EXTERNAL_FIFO_INTERFACE

Description: Not presents.

Address: 0x42C1104C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.23 ETH0_RSC_CONTROL

Description: Not presents. Access to the register will return AHB error.

Address: 0x42C11058

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.24 ETH0_INT_MODERATION

Description: Used to moderate the number of transmit and receive complete interrupts issued. With interrupt moderation enabled receive and transmit interrupts are not generated immediately a frame is transmitted or received. Instead when a receive or transmit event occurs a timer is started and the interrupt is asserted after it times out. This limits the frequency with which the CPU receives interrupts. When interrupt moderation is enabled interrupt status bit one is always used for receive and bit 7 is always used for transmit even when priority queuing is enabled. With interrupt moderation 800ns periods are counted. GEM determines what constitutes an 800ns period by looking at the tbi (bit 11), gigabit bit (10) and speed (bit 0) bits in the network configuration register and counting tx_clk cycles. Bit 0 needs to be set to 1 for 100M operation.

Address: 0x42C1105C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RX_INT_MODERATION [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TX_INT_MODERATION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	TX_INT_MODERATION	Count of 800ns periods before bit 7 is set in the interrupt status register after a frame is transmitted. A non-zero value indicates transmit interrupt moderation will be performed. Default Value: 0x00
7 : 0	RX_INT_MODERATION	Count of 800ns periods before bit 1 is set in the interrupt status register after a frame is received. A non-zero value indicates receive interrupt moderation will be performed. Default Value: 0x00

25.1.25 ETH0_SYS_WAKE_TIME

Description: Used to pause transmission after deassertion of tx_lpi_en. Each unit in this register corresponds to 64ns in gigabit mode, 320ns in 100M mode and 3200ns at 10M. After tx_lpi_en is deasserted transmission will pause for the set time.

Address: 0x42C11060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SYS_WAKE_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SYS_WAKE_TIME [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	SYS_WAKE_TIME	Count of 64ns, 320ns or 3200ns intervals before transmission starts after deassertion of TX-_LPI_EN bit field (each interval is equivalent to eight transmit clock periods and so varies with data rate) in the network control register. Default Value: 0x0000

25.1.26 ETH0_HASH_BOTTOM

Description: The unicast hash enable and the multicast hash enable bits in the network configuration register enable the reception of hash matched frames. Hash Register Bottom (31 to 0 bits)

Address: 0x42C11080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDRESS_HASH_B [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRESS_HASH_B [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDRESS_HASH_B [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDRESS_HASH_B [31:24]							

Bits	Name	Description
31 : 0	ADDRESS_HASH_B	The first 32 bits of the hash address register. Default Value: 0x00000000

25.1.27 ETH0_HASH_TOP

Description: Hash Register Top (63 to 32 bits)

Address: 0x42C11084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDRESS_HASH_T [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRESS_HASH_T [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDRESS_HASH_T [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDRESS_HASH_T [31:24]							

Bits	Name	Description
31 : 0	ADDRESS_HASH_T	The remaining 32 bits of the hash address register. Default Value: 0x00000000

25.1.28 ETH0_SPEC_ADD1_BOTTOM

Description: The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written.

Address: 0x42C11088

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDRESS_ADD1_B [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRESS_ADD1_B [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDRESS_ADD1_B [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDRESS_ADD1_B [31:24]							

Bits	Name	Description
31 : 0	ADDRESS_ADD1_B	"Least significant 32 bits of the destination address, that is bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received." Default Value: 0x00000000

25.1.29 ETH0_SPEC_ADD1_TOP

Description: Specific Address Top

Address: 0x42C1108C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDRESS_TOP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRESS_TOP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							FILTER_-TYPE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	FILTER_TYPE	This control bit selects whether this filter should be comparing the MAC source address or the MAC destination address of the received Ethernet frame. When set to zero, the filter is a destination address filter. When set to one, the filter is a source address filter. Specific address 1. The most significant bits of the destination address, that is bits 47:32. Default Value: 0
15 : 0	ADDRESS_TOP	Specific address 1. The most significant bits of the destination/source address that is to be compared, that is bits 47:32. Default Value: 0x0000

25.1.30 ETH0_SPEC_ADD2_BOTTOM

Description: The addresses stored in the specific address registers are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written.

Address: 0x42C11090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDRESS_BOTTOM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRESS_BOTTOM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDRESS_BOTTOM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDRESS_BOTTOM [31:24]							

Bits	Name	Description
31 : 0	ADDRESS_BOTTOM	Least significant 32 bits of the destination address, that is bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received. Default Value: 0x00000000

25.1.31 ETH0_SPEC_ADD2_TOP

Description: Specific Address Top

Address: 0x42C11094

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDRESS_TOP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRESS_TOP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							FILTER_-TYPE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		FILTER_BYTE_MASK [29:24]					

Bits	Name	Description
29 : 24	FILTER_BYTE_MASK	When high, the associated byte of the specific address will not be compared. Bit 24 controls whether the first byte received should be compared. Bit 29 controls whether the last byte received should be compared. Default Value: 0x00
16	FILTER_TYPE	This control bit selects whether this filter should be comparing the MAC source address or the MAC destination address of the received Ethernet frame. When set to zero, the filter is a destination address filter. When set to one, the filter is a source address filter. Specific address 1. The most significant bits of the destination address, that is bits 47:32. Default Value: 0
15 : 0	ADDRESS_TOP	Specific address 1. The most significant bits of the destination/source address that is to be compared, that is bits 47:32. Default Value: 0x0000

25.1.32 ETH0_SPEC_TYPE1

Description: Type ID Match 1

Address: 0x42C110A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLE_-COPY	Reserved [30:24]						

Bits	Name	Description
31	ENABLE_COPY	Enable copying of type ID match 1 matched frames. Default Value: 0
15 : 0	MATCH	Type ID match 1. For use in comparisons with received frames type ID/length field. Default Value: 0x0000

25.1.33 ETH0_SPEC_TYPE2

Description: Type ID Match 2

Address: 0x42C110AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLE_-COPY	Reserved [30:24]						

Bits	Name	Description
31	ENABLE_COPY	Enable copying of type ID match 2 matched frames. Default Value: 0
15 : 0	MATCH	Type ID match 2. For use in comparisons with received frames type ID/length field. Default Value: 0x0000

25.1.34 ETH0_SPEC_TYPE3

Description: Type ID Match 3

Address: 0x42C110B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLE_-COPY	Reserved [30:24]						

Bits	Name	Description
31	ENABLE_COPY	Enable copying of type ID match 3 matched frames. Default Value: 0
15 : 0	MATCH	Type ID match 3. For use in comparisons with received frames type ID/length field. Default Value: 0x0000

25.1.35 ETH0_SPEC_TYPE4

Description: Type ID Match 4

Address: 0x42C110B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLE_-COPY	Reserved [30:24]						

Bits	Name	Description
31	ENABLE_COPY	Enable copying of type ID match 4 matched frames. Default Value: 0
15 : 0	MATCH	Type ID match 4. For use in comparisons with received frames type ID/length field. Default Value: 0x0000

25.1.36 ETH0_WOL_REGISTER

Description: Wake on LAN Register. Presents in design, but feature is not supported.

Address: 0x42C110B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [23:20]				WOL_MASK_3	WOL_MASK_2	WOL_MASK_1	WOL_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19	WOL_MASK_3	Wake on LAN multicast hash event enable. Default Value: 0
18	WOL_MASK_2	Wake on LAN specific address register 1 event enable. Default Value: 0
17	WOL_MASK_1	Wake on LAN ARP request event enable. Default Value: 0
16	WOL_MASK_0	Wake on LAN magic packet event enable. Default Value: 0
15 : 0	ADDR	Wake on LAN ARP request IP address. Written to define the least significant 16 bits of the target IP address that is matched to generate a Wake on LAN event. A value of zero will not generate an event, even if this is matched by the received frame. Default Value: 0x0000

25.1.37 ETH0_STRETCH_RATIO

Description: IPG stretch register

Address: 0x42C110BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IPG_STRETCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IPG_STRETCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	IPG_STRETCH	IPG Stretch. Bits 7:0 are multiplied with the previously transmitted frame length (including preamble) bits 15:8 +1 divide the frame length. If the resulting number is greater than 96 and bit 28 is set in the network configuration register then the resulting number is used for the transmit inter-packet-gap. 1 is added to bits 15:8 to prevent a divide by zero. Default Value: 0x0000

25.1.38 ETH0_STACKED_VLAN

Description: Stacked VLAN Register

Address: 0x42C110C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLE_PROCESSING	Reserved [30:24]						

Bits	Name	Description
31	ENABLE_PROCESSING	Enable stacked VLAN processing mode Default Value: 0
15 : 0	MATCH	User defined VLAN_TYPE field. When Stacked VLAN is enabled, the first VLAN tag in a received frame will only be accepted if the VLAN type field is equal to this user defined VLAN_TYPE OR equal to the standard VLAN type (0x8100). Note that the second VLAN tag of a Stacked VLAN packet will only be matched correctly if its VLAN_TYPE field equals 0x8100. Default Value: 0x0000

25.1.39 ETH0_TX_PFC_PAUSE

Description: Transmit PFC Pause Register

Address: 0x42C110C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VECTOR_ENABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VECTOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	VECTOR	Priority Vector Pause Size. If bit 17 of the network control register is written with a one then for each entry equal to zero in the Transmit PFC Pause Register[15:8], the PFC pause frame's pause quantum field associated with that entry will be taken from the transmit pause quantum register. For each entry equal to one in the Transmit PFC Pause Register [15:8], the pause quantum associated with that entry will be zero. Default Value: 0x00
7 : 0	VECTOR_ENABLE	Priority Vector Enable. If bit 17 of the network control register is written with a one then the priority enable vector of the PFC priority based pause frame will be set equal to the value stored in this register [7:0]. Default Value: 0x00

25.1.40 ETH0_MASK_ADD1_BOTTOM

Description: Specific Address Mask 1 Bottom (31 to 0 bits)

Address: 0x42C110C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDRESS_MASK_BOTTOM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRESS_MASK_BOTTOM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDRESS_MASK_BOTTOM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDRESS_MASK_BOTTOM [31:24]							

Bits	Name	Description
31 : 0	ADDRESS_MASK_BOTTOM	Specific Address Mask. Setting a bit to one masks the corresponding bit in the specific address 1 register (31 to 0 bits) Default Value: 0x00000000

25.1.41 ETH0_MASK_ADD1_TOP

Description: Specific Address Mask 1 Top (47 to 32 bits)

Address: 0x42C110CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDRESS_MASK_TOP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRESS_MASK_TOP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	ADDRESS_MASK_TOP	Specific Address Mask. Setting a bit to one masks the corresponding bit in the specific address 1 register (47 to 32 bits). Default Value: 0x0000

25.1.42 ETH0_DMA_ADDR_OR_MASK

Description: Receive DMA Data Buffer Address Mask

Address: 0x42C110D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				MASK_ENABLE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				Reserved			
HW Access	R				Reserved			
Name	MASK_VALUE_DA [31:28]				Reserved [27:24]			

Bits	Name	Description
31 : 28	MASK_VALUE_DA	Data Buffer Address Mask Value. Values used to force bits 31:28 of the receive data buffer AHB address to a particular value when the associated enable bits stored in this register [3:0] are set. Any changes to this register will be ignored while the DMA is currently processing a receive packet. It will only affect the next full packet to be written to external system memory. Default Value: 0x0
3 : 0	MASK_ENABLE	Data Buffer Address Mask Enable. These bits are associated directly with bits[31:28].When bit 0 is set, the AXI/AHB address bit 28 used for accessing the receive data buffers will be forced to the value stored in bit 28 of this register. When bit 1 is set, the AXI/AHB address bit 29 used for accessing the receive data buffers will be forced to the value stored in bit 29 of this register. When bit 2 is set, the AXI/AHB address bit 30 used for accessing the receive data buffers will be forced to the value stored in bit 30 of this register. When bit 3 is set, the AXI/AHB address bit 31 used for accessing the receive data buffers will be forced to the value stored in bit 31 of this register. When these bits are clear, the associated value stored in bits 31:28 have no effect on the AXI/AHB address used for receive data buffer accesses. Any changes to this register will be ignored while the DMA is currently processing a receive packet. It will only affect the next full packet to be written to external memory. Default Value: 0x0

25.1.43 ETH0_RX_PTP_UNICAST

Description: PTP RX unicast IP destination address

Address: 0x42C110D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDRESS_UNICAST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRESS_UNICAST [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDRESS_UNICAST [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDRESS_UNICAST [31:24]							

Bits	Name	Description
31 : 0	ADDRESS_UNICAST	Unicast IP destination address. Used for detection of PTP frames on receive path. Default Value: 0x00000000

25.1.44 ETH0_TX_PTP_UNICAST

Description: PTP TX unicast IP destination address

Address: 0x42C110D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDRESS_UNICAST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDRESS_UNICAST [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDRESS_UNICAST [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDRESS_UNICAST [31:24]							

Bits	Name	Description
31 : 0	ADDRESS_UNICAST	Unicast IP destination address. Used for detection of PTP frames on transmit path. Default Value: 0x00000000

25.1.45 ETH0_TSU_NSEC_CMP

Description: TSU timer comparison value nanoseconds

Address: 0x42C110DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMPARISON_NSEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMPARISON_NSEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [23:22]		COMPARISON_NSEC [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 0	COMPARISON_NSEC	TSU timer comparison value (ns). Value is compared to the bits[45:24] of the TSU timer count value (upper 22 bits of nanosecond value). Default Value: 0x000000

25.1.46 ETH0_TSU_SEC_CMP

Description: TSU timer comparison value seconds (31 to 0 bits)

Address: 0x42C110E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMPARISON_SEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMPARISON_SEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMPARISON_SEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	COMPARISON_SEC [31:24]							

Bits	Name	Description
31 : 0	COMPARISON_SEC	TSU timer comparison value (s). Value is compared to seconds value bits [31:0] of the TSU timer count value. Default Value: 0x00000000

25.1.47 ETH0_TSU_MSB_SEC_CMP

Description: TSU timer comparison value seconds (47 to 32 bits)

Address: 0x42C110E4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMPARISON_MSB_SEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMPARISON_MSB_SEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COMPARISON_MS-B_SEC	TSU timer comparison value (s). Value is compared to the top 16 bits (most significant 16-bits {47:32] of seconds value) of the TSU timer count value. Default Value: 0x0000

25.1.48 ETH0_TSU_PTP_TX_MSB_SEC

Description: PTP Event Frame Transmitted Seconds Register (47 to 32 bits)

Address: 0x42C110E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_SECONDS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_SECONDS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	TIMER_SECONDS	PTP Event Frame TX Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. Default Value: 0x0000

25.1.49 ETH0_TSU_PTP_RX_MSB_SEC

Description: PTP Event Frame Received Seconds Register (47 to 32 bits)

Address: 0x42C110EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_SECONDS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_SECONDS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	TIMER_SECONDS	PTP Event Frame TX Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP receive primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. Default Value: 0x0000

25.1.50 ETH0_TSU_PEER_TX_MSB_SEC

Description: PTP Peer Event Frame Transmitted Seconds Register (47 to 32 bits)

Address: 0x42C110F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_SECONDS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_SECONDS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	TIMER_SECONDS	PTP Peer Event Frame TX Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. Default Value: 0x0000

25.1.51 ETH0_TSU_PEER_RX_MSB_SEC

Description: PTP Peer Event Frame Received Seconds Register (47 to 32 bits)

Address: 0x42C110F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_SECONDS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_SECONDS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	TIMER_SECONDS	PTP Peer Event Frame RX Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP receive peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. Default Value: 0x0000

25.1.52 ETH0_DPRAM_FILL_DBG

Description: The fill levels for the TX & RX packet buffers can be read using this register, including the fill level for each queue in the TX direction.

Address: 0x42C110F8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				Reserved			RW
HW Access	R				Reserved			R
Name	DMA_TX_Q_FILL_LEVEL_SELECT [7:4]				Reserved [3:1]			DMA_TX-_RX_-FILL_LEVEL_SELECT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DMA_TX_RX_FILL_LEVEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DMA_TX_RX_FILL_LEVEL [31:24]							

Bits	Name	Description
31 : 16	DMA_TX_RX_FILL_LEV-EL	Fill Level - TX or RX packet buffer fill level, selected by the DMA_TX_Q_FILL_LEVEL_SELECT and DMA_TX_RX_FILL_LEVEL_SELECT bit fields. Read this register to determine the fill level. Default Value: 0x0000
7 : 4	DMA_TX_Q_-FILL_LEVEL_SELECT	TX queue fill level select - select what TX queue to report fill levels for. Default Value: 0x0
0	DMA_TX_RX_-FILL_LEVEL_SELECT	TX/RX Fill Level select - report the fill level for the TX or RX packet buffer. Default Value: 0

25.1.53 ETH0_REVISION_REG

Description: This register indicates a Cadence module identification number and module revision. The value of this register is read only as defined by `gem_revision_reg_value

Address: 0x42C110FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	MODULE_REVISION [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	MODULE_REVISION [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	MODULE_IDENTIFICATION_NUMBER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	FIX_NUMBER [31:28]				MODULE_IDENTIFICATION_NUMBER [27:24]			

Bits	Name	Description
31 : 28	FIX_NUMBER	Fix number - incremented for fix releases. Default Value: 0x0
27 : 16	MODULE_IDENTIFICA-TION_NUMBER	Module identification number - for the GEM, this value is fixed. Default Value: 0x007
15 : 0	MODULE_REVISION	Module revision - fixed value specific to the revision of the design which is incremented for each non-fix release of the IP. Default Value: 0x0109

25.1.54 ETH0_OCTETS_TXED_BOTTOM

Description: Octets Transmitted lower bits (31 to 0 bits)

Address: 0x42C11100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_BOTTOM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_BOTTOM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_BOTTOM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_BOTTOM [31:24]							

Bits	Name	Description
31 : 0	COUNT_BOTTOM	Transmitted octets in frame without errors [31:0]. The number of octets transmitted in valid frames of any type. This counter is 48-bits, and is read through two registers. This count does not include octets from automatically generated pause frames. Default Value: 0x00000000

25.1.55 ETH0_OCTETS_TXED_TOP

Description: Octets Transmitted higher bits (47 to 32 bits)

Address: 0x42C11104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_TOP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_TOP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COUNT_TOP	Transmitted octets in frame without errors [47:32]. The number of octets transmitted in valid frames of any type. This counter is 48-bits, and is read through two registers. This count does not include octets from automatically generated pause frames. Default Value: 0x0000

25.1.56 ETH0_FRAMES_TXED_OK

Description: Frames Transmitted

Address: 0x42C11108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_OK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_OK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_OK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_OK [31:24]							

Bits	Name	Description
31 : 0	COUNT_OK	Frames transmitted without error. A 32 bit register counting the number of frames successfully transmitted, i.e. no under run and not too many retries. Excludes pause frames. Default Value: 0x00000000

25.1.57 ETH0_BROADCAST_TXED

Description: Broadcast Frames Transmitted

Address: 0x42C1110C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_BROADCAST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_BROADCAST [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_BROADCAST [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_BROADCAST [31:24]							

Bits	Name	Description
31 : 0	COUNT_BROADCAST	Broadcast frames transmitted without error. A 32 bit register counting the number of broadcast frames successfully transmitted without error, i.e. no under run and not too many retries. Excludes pause frames. Default Value: 0x00000000

25.1.58 ETH0_MULTICAST_TXED

Description: Multicast Frames Transmitted

Address: 0x42C11110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_MULTICAST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_MULTICAST [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_MULTICAST [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_MULTICAST [31:24]							

Bits	Name	Description
31 : 0	COUNT_MULTICAST	Multicast frames transmitted without error. A 32 bit register counting the number of multicast frames successfully transmitted without error, i.e. no under run and not too many retries. Excludes pause frames. Default Value: 0x00000000

25.1.59 ETH0_PAUSE_FRAMES_TXED

Description: Pause Frames Transmitted

Address: 0x42C11114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_PAUSE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_PAUSE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COUNT_PAUSE	Transmitted pause frames - a 16 bit register counting the number of pause frames transmitted. Only pause frames triggered by the register interface or through the external pause pins are counted as pause frames. Pause frames received through the external FIFO interface are counted in the frames transmitted counter. Default Value: 0x0000

25.1.60 ETH0_FRAMES_TXED_64

Description: 64 Byte Frames Transmitted

Address: 0x42C11118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_64 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_64 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_64 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_64 [31:24]							

Bits	Name	Description
31 : 0	COUNT_64	64 byte frames transmitted without error. A 32 bit register counting the number of 64 byte frames successfully transmitted without error, i.e. no under run and not too many retries. Excludes pause frames. Default Value: 0x00000000

25.1.61 ETH0_FRAMES_TXED_65

Description: 65 to 127 Byte Frames Transmitted

Address: 0x42C1111C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_65 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_65 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_65 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_65 [31:24]							

Bits	Name	Description
31 : 0	COUNT_65	65 to127 byte frames transmitted without error. A 32 bit register counting the number of 65 to127 byte frames successfully transmitted without error, i.e. no under run and not too many retries. Default Value: 0x00000000

25.1.62 ETH0_FRAMES_TXED_128

Description: 128 to 255 Byte Frames Transmitted

Address: 0x42C11120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_128 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_128 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_128 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_128 [31:24]							

Bits	Name	Description
31 : 0	COUNT_128	128 to 255 byte frames transmitted without error. A 32 bit register counting the number of 128 to 255 byte frames successfully transmitted without error, i.e. no under run and not too many retries. Default Value: 0x00000000

25.1.63 ETH0_FRAMES_TXED_256

Description: 256 to 511 Byte Frames Transmitted

Address: 0x42C11124

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_256 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_256 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_256 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_256 [31:24]							

Bits	Name	Description
31 : 0	COUNT_256	256 to 511 byte frames transmitted without error. A 32 bit register counting the number of 256 to 511 byte frames successfully transmitted without error, i.e. no under run and not too many retries. Default Value: 0x00000000

25.1.64 ETH0_FRAMES_TXED_512

Description: 512 to 1023 Byte Frames Transmitted

Address: 0x42C11128

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_512 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_512 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_512 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_512 [31:24]							

Bits	Name	Description
31 : 0	COUNT_512	512 to 1023 byte frames transmitted without error. A 32 bit register counting the number of 512 to 1023 byte frames successfully transmitted without error, i.e. no under run and not too many retries. Default Value: 0x00000000

25.1.65 ETH0_FRAMES_TXED_1024

Description: 1024 to 1518 Byte Frames Transmitted

Address: 0x42C1112C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_1024 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_1024 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_1024 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_1024 [31:24]							

Bits	Name	Description
31 : 0	COUNT_1024	1024 to 1518 byte frames transmitted without error. A 32 bit register counting the number of 1024 to 1518 byte frames successfully transmitted without error, i.e. no under run and not too many retries. Default Value: 0x00000000

25.1.66 ETH0_FRAMES_TXED_1519

Description: Greater Than 1518 Byte Frames Transmitted

Address: 0x42C11130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_1519 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_1519 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_1519 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_1519 [31:24]							

Bits	Name	Description
31 : 0	COUNT_1519	Greater than 1518 byte frames transmitted without error. A 32 bit register counting the number of 1518 or above byte frames successfully transmitted without error, i.e. no under run and not too many retries. Default Value: 0x00000000

25.1.67 ETH0_TX_UNDERRUNS

Description: Transmit Under Runs

Address: 0x42C11134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_UN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT_UN [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT_UN	Transmit under runs - a 10 bit register counting the number of frames not transmitted due to a transmit under run. If this register is incremented then no other statistics register is incremented. Default Value: 0x000

25.1.68 ETH0_SINGLE_COLLISIONS

Description: Single Collision Frames. Presents in design but not support.

Address: 0x42C11138

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT14 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT14 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [23:18]						COUNT14 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 0	COUNT14	Single collision frames - an 18 bit register counting the number of frames experiencing a single collision before being successfully transmitted, i.e. no under run. Default Value: 0x00000

25.1.69 ETH0_MULTIPLE_COLLISIONS

Description: Multiple Collision Frames. Presents in design but not support.

Address: 0x42C1113C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT15 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT15 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [23:18]						COUNT15 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 0	COUNT15	Multiple collision frames - an 18 bit register counting the number of frames experiencing between two and fifteen collisions prior to being successfully transmitted, i.e. no under run and not too many retries. Default Value: 0x00000

25.1.70 ETH0_EXCESSIVE_COLLISIONS

Description: Excessive Collisions. Presents in design but not support.

Address: 0x42C11140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT16 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT16	Excessive collisions - a 10 bit register counting the number of frames that failed to be transmitted because they experienced 16 collisions. Default Value: 0x000

25.1.71 ETH0_LATE_COLLISIONS

Description: Late Collisions. Presents in design but not support.

Address: 0x42C11144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT17 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT17 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT17	Late collisions - a 10 bit register counting the number of late collision occurring after the slot time (512 bits) has expired. In 10/100 mode, late collisions are counted twice i.e. both as a collision and a late collision. In gigabit mode, a late collision causes the transmission to be aborted, thus the single and multi collision registers are not updated. Default Value: 0x000

25.1.72 ETH0_DEFERRED_FRAMES

Description: Deferred Transmission Frames. Presents in design but not support.

Address: 0x42C11148

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT18 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT18 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [23:18]						COUNT18 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 0	COUNT18	Deferred transmission frames - an 18 bit register counting the number of frames experiencing deferral due to carrier sense being active on their first attempt at transmission. Frames involved in any collision are not counted nor are frames that experienced a transmit under run. Default Value: 0x00000

25.1.73 ETH0_CRS_ERRORS

Description: Carrier Sense Errors. Presents in design but not support.

Address: 0x42C1114C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT19 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT19 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT19	Carrier sense errors - a 10 bit register counting the number of frames transmitted where carrier sense was not seen during transmission or where carrier sense was deasserted after being asserted in a transmit frame without collision (no under run). Only incremented in half duplex mode. The only effect of a carrier sense error is to increment this register. The behaviour of the other statistics registers is unaffected by the detection of a carrier sense error. Default Value: 0x000

25.1.74 ETH0_OCTETS_RXED_BOTTOM

Description: Octets Received (31 to 0 bits)

Address: 0x42C11150

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_BOTTOM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_BOTTOM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_BOTTOM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_BOTTOM [31:24]							

Bits	Name	Description
31 : 0	COUNT_BOTTOM	Received octets in frame without errors [31:0]. The number of octets received in valid frames of any type. This counter is 48-bits and is read through two registers. This count does not include octets from pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.75 ETH0_OCTETS_RXED_TOP

Description: Octets Received (47 to 32 bits)

Address: 0x42C11154

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_TOP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_TOP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COUNT_TOP	Received octets in frame without errors [47:32]. The number of octets received in valid frames of any type. This counter is 48-bits and is read through two registers. This count does not include octets from pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x0000

25.1.76 ETH0_FRAMES_RXED_OK

Description: Frames Received

Address: 0x42C11158

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_OK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_OK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_OK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_OK [31:24]							

Bits	Name	Description
31 : 0	COUNT_OK	Frames received without error. A 32 bit register counting the number of frames successfully received. Excludes pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.77 ETH0_BROADCAST_RXED

Description: Broadcast Frames Received

Address: 0x42C1115C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_BROADCAST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_BROADCAST [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_BROADCAST [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_BROADCAST [31:24]							

Bits	Name	Description
31 : 0	COUNT_BROADCAST	Broadcast frames received without error. A 32 bit register counting the number of broadcast frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.78 ETH0_MULTICAST_RXED

Description: Multicast Frames Received

Address: 0x42C11160

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_MULTICAST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_MULTICAST [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_MULTICAST [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_MULTICAST [31:24]							

Bits	Name	Description
31 : 0	COUNT_MULTICAST	Multicast frames received without error. A 32 bit register counting the number of multicast frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.79 ETH0_PAUSE_FRAMES_RXED

Description: Pause Frames Received

Address: 0x42C11164

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_PAUSE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_PAUSE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COUNT_PAUSE	Received pause frames - a 16 bit register counting the number of pause frames received without error. Default Value: 0x0000

25.1.80 ETH0_FRAMES_RXED_64

Description: 64 Byte Frames Received

Address: 0x42C11168

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_64 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_64 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_64 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_64 [31:24]							

Bits	Name	Description
31 : 0	COUNT_64	64 byte frames received without error. A 32 bit register counting the number of 64 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.81 ETH0_FRAMES_RXED_65

Description: 65 to 127 Byte Frames Received

Address: 0x42C1116C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_65 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_65 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_65 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_65 [31:24]							

Bits	Name	Description
31 : 0	COUNT_65	65 to 127 byte frames received without error. A 32 bit register counting the number of 65 to 127 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.82 ETH0_FRAMES_RXED_128

Description: 128 to 255 Byte Frames Received

Address: 0x42C11170

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_128 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_128 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_128 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_128 [31:24]							

Bits	Name	Description
31 : 0	COUNT_128	128 to 255 byte frames received without error. A 32 bit register counting the number of 128 to 255 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.83 ETH0_FRAMES_RXED_256

Description: 256 to 511 Byte Frames Received

Address: 0x42C11174

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_256 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_256 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_256 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_256 [31:24]							

Bits	Name	Description
31 : 0	COUNT_256	256 to 511 byte frames received without error. A 32 bit register counting the number of 256 to 511 byte frames successfully transmitted without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.84 ETH0_FRAMES_RXED_512

Description: 512 to 1023 Byte Frames Received

Address: 0x42C11178

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_512 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_512 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_512 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_512 [31:24]							

Bits	Name	Description
31 : 0	COUNT_512	512 to 1023 byte frames received without error. A 32 bit register counting the number of 512 to 1023 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.85 ETH0_FRAMES_RXED_1024

Description: 1024 to 1518 Byte Frames Received

Address: 0x42C1117C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_1024 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_1024 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_1024 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_1024 [31:24]							

Bits	Name	Description
31 : 0	COUNT_1024	1024 to 1518 byte frames received without error. A 32 bit register counting the number of 1024 to 1518 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.86 ETH0_FRAMES_RXED_1519

Description: 1519 to maximum Byte Frames Received

Address: 0x42C11180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_1519 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_1519 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	W							
Name	COUNT_1519 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RC							
HW Access	W							
Name	COUNT_1519 [31:24]							

Bits	Name	Description
31 : 0	COUNT_1519	1519 to maximum byte frames received without error. A 32 bit register counting the number of 1519 byte or above frames successfully received without error. Maximum frame size is determined by the network configuration register bit 8 (1536 maximum frame size) or bit 3 (jumbo frame size). Excludes pause frames, and is only incremented if the frame is successfully filtered. Default Value: 0x00000000

25.1.87 ETH0_UNDERSIZE_FRAMES

Description: Undersized Frames Received

Address: 0x42C11184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_UNDERSIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT_UNDERSIZE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT_UNDERSIZE	Undersize frames received - a 10 bit register counting the number of frames received less than 64 bytes in length (10/100 mode or gigabit mode, full duplex) that do not have either a CRC error or an alignment error. In gigabit mode, half duplex, this register counts either frames not conforming to the minimum slot time of 512 bytes or frames not conforming to the minimum frame size once bursting is active. Default Value: 0x000

25.1.88 ETH0_EXCESSIVE_RX_LENGTH

Description: Oversize Frames Received

Address: 0x42C11188

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_OVERSIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT_OVERSIZE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT_OVERSIZE	Oversize frames received - a 10 bit register counting the number of frames received exceeding 1518 bytes (1536 bytes if bit 8 is set in network configuration register, 10,240 bytes if bit 3 is set in the network configuration register) in length but do not have either a CRC error, an alignment error nor a receive symbol error. Default Value: 0x000

25.1.89 ETH0_RX_JABBERS

Description: Jabbers Received

Address: 0x42C1118C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_JABBERS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT_JABBERS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT_JABBERS	Jabbers received - a 10 bit register counting the number of frames received exceeding 1518 bytes (1536 if bit 8 set in network configuration register, 10,240 bytes if bit 3 is set in the network configuration register) in length and have either a CRC error, an alignment error or a receive symbol error. Default Value: 0x000

25.1.90 ETH0_FCS_ERRORS

Description: Frame Check Sequence Errors

Address: 0x42C11190

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_FCS_ERR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT_FCS_ERR [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT_FCS_ERR	Frame check sequence errors - a 10 bit register counting frames that are an integral number of bytes, have bad CRC and are between 64 and 1518 bytes in length (1536 if bit 8 set in network configuration register, 10,240 bytes if bit 3 is set in the network configuration register). This register is also incremented if a symbol error is detected and the frame is of valid length and has an integral number of bytes. This register is incremented for a frame with bad FCS, regardless of whether it is copied to memory due to ignore FCS mode being enabled in bit 26 of the network configuration register. Default Value: 0x000

25.1.91 ETH0_RX_LENGTH_ERRORS

Description: Length Field Frame Errors

Address: 0x42C11194

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_LENGTH_ERR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT_LENGTH_ERR [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT_LENGTH_ERR	Length field frame errors - this 10-bit register counts the number of frames received that have a measured length shorter than that extracted from the length field (bytes 13 and 14). This condition is only counted if the value of the length field is less than 0x0600, the frame is not of excessive length and checking is enabled through bit 16 of the network configuration register. Default Value: 0x000

25.1.92 ETH0_RX_SYMBOL_ERRORS

Description: Receive Symbol Errors

Address: 0x42C11198

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_SYMBOL_ERR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT_SYMBOL_ERR [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT_SYMBOL_ERR	Receive symbol errors - a 10-bit register counting the number of frames that had rx_er asserted during reception. For 10/100 mode symbol errors are counted regardless of frame length checks. For gigabit mode the frame must satisfy slot time requirements in order to count a symbol error. Additionally, in gigabit half duplex mode, carrier extension errors are also recorded. Receive symbol errors will also be counted as an FCS or alignment error if the frame is between 64 and 1518 bytes (1536 bytes if bit 8 is set in the network configuration register, 10240 bytes if bit 3 is set in the network configuration register). If the frame is larger it will be recorded as a jabber error. Default Value: 0x000

25.1.93 ETH0_ALIGNMENT_ERRORS

Description: Alignment Errors

Address: 0x42C1119C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_ALIGNMENT_ERROR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT_ALIGN-MENT_ERROR [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT_ALIGN-MENT_ERROR	Alignment errors - a 10 bit register counting frames that are not an integral number of bytes long and have bad CRC when their length is truncated to an integral number of bytes and are between 64 and 1518 bytes in length (1536 if bit 8 set in network configuration register, 10,240 bytes if bit 3 is set in the network configuration register). This register is also incremented if a symbol error is detected and the frame is of valid length and does not have an integral number of bytes. Default Value: 0x000

25.1.94 ETH0_RX_RESOURCE_ERRORS

Description: Receive Resource Errors

Address: 0x42C111A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_RESOURCE_ERR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_RESOURCE_ERR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [23:18]						COUNT_RESOURCE_ERR [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 0	COUNT_RESOURCE_ERR	Receive resource errors - an 18 bit register counting the number of frames that were successfully received by the MAC (correct address matched frame and adequate slot time) but could not be copied to memory because no receive buffer was available. This occurs when the GEM reads a buffer descriptor with its ownership (or used) bit set. Default Value: 0x00000

25.1.95 ETH0_RX_OVERRUNS

Description: Receive Overruns

Address: 0x42C111A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_OVERRUN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RC	
HW Access	Reserved						W	
Name	Reserved [15:10]						COUNT_OVERRUN [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	COUNT_OVERRUN	Receive overruns - a 10 bit register counting the number of frames that are address recognized but were not copied to memory due to a receive overrun. Default Value: 0x000

25.1.96 ETH0_RX_IP_CK_ERRORS

Description: IP Header Checksum Errors

Address: 0x42C111A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_IPCK_ERR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	COUNT_IPCK_ERR	IP header checksum errors - an 8-bit register counting the number of frames discarded due to an incorrect IP header checksum, but are between 64 and 1518 bytes (1536 bytes if bit 8 is set in the network configuration register or 10240 bytes if bit 3 is in the network configuration register) and do not have a CRC error, an alignment error, nor a symbol error. Default Value: 0x00

25.1.97 ETH0_RX_TCP_CK_ERRORS

Description: TCP Checksum Errors

Address: 0x42C111AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_TCPCK_ERR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	COUNT_TCPCK_ERR	TCP checksum errors - an 8-bit register counting the number of frames discarded due to an incorrect TCP checksum, but are between 64 and 1518 bytes (1536 bytes if bit 8 is set in the network configuration register or 10240 bytes if bit 3 is in the network configuration register) and do not have a CRC error, an alignment error, nor a symbol error. Default Value: 0x00

25.1.98 ETH0_RX_UDP_CK_ERRORS

Description: UDP Checksum Errors

Address: 0x42C111B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_UDPCK_ERR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	COUNT_UDPCK_ERR	UDP checksum errors - an 8-bit register counting the number of frames discarded due to an incorrect UDP checksum, but are between 64 and 1518 bytes (1536 bytes if bit 8 is set in the network configuration register or 10240 bytes if bit 3 is in the network configuration register) and do not have a CRC error, an alignment error, nor a symbol error. Default Value: 0x00

25.1.99 ETH0_AUTO_FLUSHED_PKTS

Description: Receive DMA Flushed Packets

Address: 0x42C111B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	W							
Name	COUNT_FLUSHED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	W							
Name	COUNT_FLUSHED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COUNT_FLUSHED	Flushed RX packets counter. A 16 bit register counting the number of frames that have been flushed from the receive SRAM based packet buffer due to one of the following reasons .1. When partial store and forward mode is enabled or bit 24 of the DMA configuration register is enabled, a packet is received while there is no AMBA (AXI/AHB) resource. 2. When partial store and forward mode is enabled and an AMBA (AXI/AHB) error is encountered while writing the packet data to external memory. When bit 18 of the network control register(software action to flush a packet from the head of the PBUF queue) is pulsed and the GEM DMA is not currently busy. Default Value: 0x0000

25.1.100 ETH0_TSU_TIMER_INCR_SUB_NSEC

Description: 1588 Timer Increment Register sub nsec

Address: 0x42C111BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUB_NS_INCR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SUB_NS_INCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SUB_NS_INCR_LSB [31:24]							

Bits	Name	Description
31 : 24	SUB_NS_INCR_LSB	These are the least significant bits [7:0] of the sub-ns value by which the 1588 timer will be incremented each clock cycle. Default Value: 0x00
15 : 0	SUB_NS_INCR	These are the most significant bits [23:8] of the sub-ns value by which the 1588 timer will be incremented each clock cycle. 24 bits of sub nanosecond precision gives resolution of approximately 5.86E-17 seconds (16 bits gives 15.2 femtoseconds). Default Value: 0x0000

25.1.101 ETH0_TSU_TIMER_MSB_SEC

Description: 1588 Timer Seconds Register (47 to 32 bits)

Address: 0x42C111C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TIMER_MSB_SEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TIMER_MSB_SEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	TIMER_MSB_SEC	TSU timer value (s). Most significant 16 bits of seconds timer count. The register is writeable. The 48-bit counter increments by one when the 1588 nanoseconds counter counts to one second. It may also be incremented or decremented when the timer adjust register is written (if decremented from zero the 48-bit combined count would roll back to 0xFFFFFFFFFFFF). Note: The value of this register is used only when the lower 32 bit register is written to. This is to ensure a single update of the 48 bit seconds value Default Value: 0x0000

25.1.102 ETH0_TSU_STROBE_MSB_SEC

Description: 1588 Timer Sync Strobe Seconds Register (47 to 32 bits)

Address: 0x42C111C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	STROBE_MSB_SEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	STROBE_MSB_SEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	STROBE_MSB_SEC	Not used. Default Value: 0x0000

25.1.103 ETH0_TSU_STROBE_SEC

Description: 1588 Timer Sync Strobe Seconds Register (31 to 0 bits)

Address: 0x42C111C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	STROBE_SEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	STROBE_SEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	STROBE_SEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	STROBE_SEC [31:24]							

Bits	Name	Description
31 : 0	STROBE_SEC	Not used. Default Value: 0x00000000

25.1.104 ETH0_TSU_STROBE_NSEC

Description: 1588 Timer Sync Strobe Nanoseconds Register

Address: 0x42C111CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	STROBE_NSEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	STROBE_NSEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	STROBE_NSEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [31:30]		STROBE_NSEC [29:24]					

Bits	Name	Description
29 : 0	STROBE_NSEC	Not used. Default Value: 0x00000000

25.1.105 ETH0_TSU_TIMER_SEC

Description: 1588 Timer Seconds Register (31 to 0 bits)

Address: 0x42C111D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TIMER_SEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TIMER_SEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	TIMER_SEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	TIMER_SEC [31:24]							

Bits	Name	Description
31 : 0	TIMER_SEC	1588 Timer Seconds Register. TSU timer value (s). Least significant 32 bits of seconds timer count. This register is writeable. The 48-bit counter increments by one when the 1588 nanoseconds counter counts to one second. It may also be incremented or decremented when the timer adjust register is written (if decremented from zero the 48-bit combined count would roll back to 0xFFFFFFFFFFFF). Default Value: 0x00000000

25.1.106 ETH0_TSU_TIMER_NSEC

Description: 1588 Timer Nanoseconds Register

Address: 0x42C111D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TIMER_NSEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TIMER_NSEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	TIMER_NSEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		RW					
Name	Reserved [31:30]		TIMER_NSEC [29:24]					

Bits	Name	Description
29 : 0	TIMER_NSEC	Timer count in nanoseconds. This register is writeable. It can also be adjusted by writes to the 1588 timer adjust register. It increments by the value of the 1588 timer increment register each clock cycle (if this register is close to zero and a write to the timer adjust register causes a decrement the seconds register will be decremented if necessary and the nanoseconds register will roll back to 9999999xx(decimal)). Default Value: 0x00000000

25.1.107 ETH0_TSU_TIMER_ADJUST

Description: This register is used to adjust the value of the timer in the TSU. It allows an integral number of nanoseconds to be added or subtracted from the timer in a one-off operation. This register returns all zeroes when read.

Address: 0x42C111D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	INCREMENT_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	INCREMENT_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	INCREMENT_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W	Reserved	W					
HW Access	R	Reserved	R					
Name	ADD_SUB-TRACT	Reserved	INCREMENT_VALUE [29:24]					

Bits	Name	Description
31	ADD_SUBTRACT	Write as one to subtract from the 1588 timer. Write as zero to add to it. Default Value: 0
29 : 0	INCREMENT_VALUE	Timer increment value. The number of nanoseconds to increment or decrement the 1588 timer nanoseconds register. If necessary the 1588 seconds register will be incremented or decremented. Default Value: 0x0000

25.1.108 ETH0_TSU_TIMER_INCR

Description: 1588 Timer Increment Register

Address: 0x42C111DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	NS_INCREMENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ALT_NS_INCR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NUM_INCS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	NUM_INCS	Number of incs before alt inc. The number of increments after which the alternative increment is used. Default Value: 0x00
15 : 8	ALT_NS_INCR	Alternative nanoseconds count. Alternative count of nanoseconds by which the 1588 timer nanoseconds register will be incremented each clock cycle. Default Value: 0x00
7 : 0	NS_INCREMENT	A count of nanoseconds by which the 1588 timer nanoseconds register will be incremented each clock cycle. These are the most significant 8 bits of the 32 bit timer_increment counter. The TSU_TIMER_INCR_SUB_NSEC register holds the least significant 24 bits of the increment. Default Value: 0x00

25.1.109 ETH0_TSU_PTP_TX_SEC

Description: PTP Event Frame Transmitted Seconds Register (31 to 0 bits)

Address: 0x42C111E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_PTP_SEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_PTP_SEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TIMER_PTP_SEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TIMER_PTP_SEC [31:24]							

Bits	Name	Description
31 : 0	TIMER_PTP_SEC	PTP Event Frame Transmitted Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. Default Value: 0x00000000

25.1.110 ETH0_TSU_PTP_TX_NSEC

Description: PTP Event Frame Transmitted Nanoseconds Register

Address: 0x42C111E4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_PTP_NSEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_PTP_NSEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TIMER_PTP_NSEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [31:30]		TIMER_PTP_NSEC [29:24]					

Bits	Name	Description
29 : 0	TIMER_PTP_NSEC	PTP Event Frame Transmitted Nanoseconds. The register is updated with the value that the 1588 timer nanoseconds register held when the SFD of a PTP transmit primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. Default Value: 0x00000000

25.1.111 ETH0_TSU_PTP_RX_SEC

Description: PTP Event Frame Received Seconds Register (31 to 0 bits)

Address: 0x42C111E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_PTP_SEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_PTP_SEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TIMER_PTP_SEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TIMER_PTP_SEC [31:24]							

Bits	Name	Description
31 : 0	TIMER_PTP_SEC	PTP Event Frame Received Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP receive primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. Default Value: 0x00000000

25.1.112 ETH0_TSU_PTP_RX_NSEC

Description: PTP Event Frame Received Nanoseconds Register

Address: 0x42C111EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_PTP_NSEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_PTP_NSEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TIMER_PTP_NSEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [31:30]		TIMER_PTP_NSEC [29:24]					

Bits	Name	Description
29 : 0	TIMER_PTP_NSEC	PTP Event Frame Received Nanoseconds. The register is updated with the value that the 1588 timer nanoseconds register held when the SFD of a PTP receive primary event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP sync or delay_req frame. An interrupt is issued when the register is updated. Default Value: 0x00000000

25.1.113 ETH0_TSU_PEER_TX_SEC

Description: PTP Peer Event Frame Transmitted Seconds Register (31 to 0 bits)

Address: 0x42C111F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_PEER_SEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_PEER_SEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TIMER_PEER_SEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TIMER_PEER_SEC [31:24]							

Bits	Name	Description
31 : 0	TIMER_PEER_SEC	PTP Peer Event Frame Received Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. Default Value: 0x00000000

25.1.114 ETH0_TSU_PEER_TX_NSEC

Description: PTP Peer Event Frame Transmitted Nanoseconds Register

Address: 0x42C111F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_PEER_NSEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_PEER_NSEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TIMER_PEER_NSEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [31:30]		TIMER_PEER_NSEC [29:24]					

Bits	Name	Description
29 : 0	TIMER_PEER_NSEC	PTP Peer Event Frame Transmitted Nanoseconds. The register is updated with the value that the 1588 timer nanoseconds register held when the SFD of a PTP transmit peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. Default Value: 0x00000000

25.1.115 ETH0_TSU_PEER_RX_SEC

Description: PTP Peer Event Frame Received Seconds Register (31 to 0 bits)

Address: 0x42C111F8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_PEER_SEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_PEER_SEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TIMER_PEER_SEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TIMER_PEER_SEC [31:24]							

Bits	Name	Description
31 : 0	TIMER_PEER_SEC	PTP Peer Event Frame Received Seconds. The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP receive peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. Default Value: 0x00000000

25.1.116 ETH0_TSU_PEER_RX_NSEC

Description: PTP Peer Event Frame Received Nanoseconds Register

Address: 0x42C111FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TIMER_PEER_NSEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TIMER_PEER_NSEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TIMER_PEER_NSEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [31:30]		TIMER_PEER_NSEC [29:24]					

Bits	Name	Description
29 : 0	TIMER_PEER_NSEC	PTP Peer Event Frame Received Nanoseconds. The register is updated with the value that the 1588 timer nanoseconds register held when the SFD of a PTP receive peer event crosses the MII interface. The actual update occurs when the GEM recognizes the frame as a PTP pdelay_req or pdelay_resp frame. An interrupt is issued when the register is updated. Default Value: 0x00000000

25.1.117 ETH0_PCS_CONTROL

Description: Not presents. Access to the register returns AHB error.

Address: 0x42C11200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.118 ETH0_TX_PAUSE_QUANTUM1

Description: Transmit Pause Quantum Register 1

Address: 0x42C11260

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	QUANTUM_P2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	QUANTUM_P2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	QUANTUM_P3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	QUANTUM_P3 [31:24]							

Bits	Name	Description
31 : 16	QUANTUM_P3	Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 3. Default Value: 0xFFFF
15 : 0	QUANTUM_P2	Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 2. Default Value: 0xFFFF

25.1.119 ETH0_TX_PAUSE_QUANTUM2

Description: Transmit Pause Quantum Register 2

Address: 0x42C11264

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	QUANTUM_P4 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	QUANTUM_P4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	QUANTUM_P5 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	QUANTUM_P5 [31:24]							

Bits	Name	Description
31 : 16	QUANTUM_P5	Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 5. Default Value: 0xFFFF
15 : 0	QUANTUM_P4	Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 4. Default Value: 0xFFFF

25.1.120 ETH0_TX_PAUSE_QUANTUM3

Description: Transmit Pause Quantum Register 3

Address: 0x42C11268

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	QUANTUM_P6 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	QUANTUM_P6 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	QUANTUM_P7 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	QUANTUM_P7 [31:24]							

Bits	Name	Description
31 : 16	QUANTUM_P7	Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 7. Default Value: 0xFFFF
15 : 0	QUANTUM_P6	Transmit pause quantum - written with the pause quantum value for pause frame transmission of priority 6. Default Value: 0xFFFF

25.1.121 ETH0_RX_LPI

Description: Received LPI transitions

Address: 0x42C11270

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	R							
Name	COUNT_LPI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	R							
Name	COUNT_LPI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COUNT_LPI	Count of RX LPI transitions. A count of the number of times there is a transition from receiving normal idle to receiving low power idle. Cleared on read. Default Value: 0x0000

25.1.122 ETH0_RX_LPI_TIME

Description: Received LPI time

Address: 0x42C11274

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	R							
Name	LPI_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	R							
Name	LPI_TIME [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	R							
Name	LPI_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 0	LPI_TIME	Time in LPI. This register increments once every 16 clk_sys cycles when the LPI indication bit 20 is set in the receive configuration register. Cleared on read. Default Value: 0x000000

25.1.123 ETH0_TX_LPI

Description: Transmit LPI transitions

Address: 0x42C11278

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	R							
Name	COUNT_LPI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	R							
Name	COUNT_LPI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COUNT_LPI	Count of LPI transmissions. A count of the number of times the enable LPI transmission bit 20 goes from low to high in the transmit control register. Default Value: 0x0000

25.1.124 ETH0_TX_LPI_TIME

Description: Transmit LPI time

Address: 0x42C1127C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RC							
HW Access	R							
Name	LPI_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RC							
HW Access	R							
Name	LPI_TIME [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RC							
HW Access	R							
Name	LPI_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 0	LPI_TIME	Time in LPI. This register increments once every 16 clk_sys cycles when the enable LPI transmission bit 20 is set in the transmit control register. Cleared on read. Default Value: 0x000000

25.1.125 ETH0_DESIGNCFG_DEBUG1

Description: Design Configuration Register 1

Address: 0x42C11280

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R		R	R
HW Access	W	W	W	W	W		W	W
Name	RESERVED_7	EXT_FIFO_INTERFACE	RESERVED_5	INT_LOOPBACK	RESERVED_2 [3:2]		EXCLUDE_QBV	NO_PCS

Bits	15	14	13	12	11	10	9	8
SW Access	R	R					R	R
HW Access	W	W					W	W
Name	USER_IN_WIDTH	USER_OUT_WIDTH [14:10]					USER_IO	RESERVED_8

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R			
HW Access	W	W	W	W	W			
Name	IRQ_READ_CLEAR	NO_SNAPSHOT	NO_STATS	RESERVED_20	USER_IN_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			R
HW Access	W				W			W
Name	AXI_CACHE_VALUE [31:28]				DMA_BUS_WIDTH [27:25]			EXCLUDE_CBS

Bits	Name	Description
31 : 28	AXI_CACHE_VALUE	Write ignore, read the default value Default Value: 0x0
27 : 25	DMA_BUS_WIDTH	Write ignore, read the default value Default Value: 1
24	EXCLUDE_CBS	Write ignore, read the default value Default Value: 0
23	IRQ_READ_CLEAR	Write ignore, read the default value Default Value: 0
22	NO_SNAPSHOT	Write ignore, read the default value Default Value: 1
21	NO_STATS	Write ignore, read the default value Default Value: 0
20	RESERVED_20	Write ignore, read the default value Default Value: 1
19 : 15	USER_IN_WIDTH	Write ignore, read the default value Default Value: 0x01

25.1.125 ETH0_DESIGNCFG_DEBUG1 (continued)

14 : 10	USER_OUT_WIDTH	Write ignore, read the default value Default Value: 0x01
9	USER_IO	Write ignore, read the default value Default Value: 0
8	RESERVED_8	Write ignore, read the default value Default Value: 1
7	RESERVED_7	Write ignore, read the default value Default Value: 0
6	EXT_FIFO_INTERFACE	Write ignore, read the default value Default Value: 0
5	RESERVED_5	Write ignore, read the default value Default Value: 0
4	INT_LOOPBACK	Write ignore, read the default value Default Value: 0
3 : 2	RESERVED_2	Write ignore, read the default value Default Value: 0
1	EXCLUDE_QBV	Write ignore, read the default value Default Value: 1
0	NO_PCS	Write ignore, read the default value Default Value: 1

25.1.126 ETH0_DESIGNCFG_DEBUG2

Description: Design Configuration Register 2

Address: 0x42C11284

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	JUMBO_MAX_LENGTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [15:14]		JUMBO_MAX_LENGTH [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	R		R	R	R			
HW Access	W		W	W	W			
Name	RX_PBUF_ADDR [23:22]		TX_PK-T_BUFFER	RX_PK-T_BUFFER	HPROT_VALUE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R				R	
HW Access	W	W	W				W	
Name	SPRAM	AXI	TX_PBUF_ADDR [29:26]				RX_PBUF_ADDR [25:24]	

Bits	Name	Description
31	SPRAM	Write ignore, read the default value Default Value: 1
30	AXI	Write ignore, read the default value Default Value: 0
29 : 26	TX_PBUF_ADDR	Write ignore, read the default value Default Value: 0x9
25 : 22	RX_PBUF_ADDR	Write ignore, read the default value Default Value: 0x8
21	TX_PKT_BUFFER	Write ignore, read the default value Default Value: 1
20	RX_PKT_BUFFER	Write ignore, read the default value Default Value: 1
19 : 16	HPROT_VALUE	Write ignore, read the default value Default Value: 0x1
13 : 0	JUMBO_MAX_LENGTH	Write ignore, read the default value Default Value: 0x600

25.1.127 ETH0_DESIGNCFG_DEBUG3

Description: Design Configuration Register 3

Address: 0x42C11288

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [31:30]		NUM_SPEC_ADD_FILTERS [29:24]					

Bits	Name	Description
29 : 24	NUM_SPEC_ADD_FIL-TERS	Write ignore, read the default value Default Value: 0x04

25.1.128 ETH0_DESIGNCFG_DEBUG4

Description: Design Configuration Register 4

Address: 0x42C1128C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESERVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESERVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	RESERVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	RESERVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	RESERVED_31_0	Write ignore, read the default value Default Value: 0x00000000

25.1.129 ETH0_DESIGNCFG_DEBUG5

Description: Design Configuration Register 5

Address: 0x42C11290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	TX_FIFO_CNT_WIDTH [7:4]				RX_FIFO_CNT_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R			R		R	R
HW Access	W	W			W		W	W
Name	ENDI-AN_SWAP_DEF	MDC_CLOCK_DIV [14:12]			DMA_BUS_WIDTH_DEF [11:10]		PHY_I-DENT	TSU

Bits	23	22	21	20	19	18	17	16
SW Access	R				R	R		R
HW Access	W				W	W		W
Name	RX_BUFFER_LENGTH_DEF [23:20]				TX_PBUF_-SIZE_DEF	RX_PBUF_SIZE_DEF [18:17]		ENDI-AN_SWAP_DEF

Bits	31	30	29	28	27	26	25	24
SW Access	R			R	R			
HW Access	W			W	W			
Name	AXI_PROT_VALUE [31:29]			TSU_CLK	RX_BUFFER_LENGTH_DEF [27:24]			

Bits	Name	Description
31 : 29	AXI_PROT_VALUE	Write ignore, read the default value Default Value: 0x2
28	TSU_CLK	Write ignore, read the default value Default Value: 1
27 : 20	RX-_BUFFER_LENGTH_DEF	Write ignore, read the default value Default Value: 0x18
19	TX_PBUF_SIZE_DEF	Write ignore, read the default value Default Value: 1
18 : 17	RX_PBUF_SIZE_DEF	Write ignore, read the default value Default Value: 0x3
16 : 15	ENDIAN_SWAP_DEF	Write ignore, read the default value Default Value: 0x0
14 : 12	MDC_CLOCK_DIV	Write ignore, read the default value Default Value: 0x3
11 : 10	DMA_BUS_WIDTH_DEF	Write ignore, read the default value Default Value: 0x1
9	PHY_IDENT	Write ignore, read the default value Default Value: 1

25.1.129 ETH0_DESIGNCFG_DEBUG5 (continued)

8	TSU	Write ignore, read the default value Default Value: 1
7 : 4	TX_FIFO_CNT_WIDTH	Write ignore, read the default value Default Value: 0x4
3 : 0	RX_FIFO_CNT_WIDTH	Write ignore, read the default value Default Value: 0x4

25.1.130 ETH0_DESIGNCFG_DEBUG6

Description: Design Configuration Register 6

Address: 0x42C11294

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	Reserved
HW Access	W	W	W	W	W	W	W	Reserved
Name	DMA_PRIORITY_QUEUE7	DMA_PRIORITY_QUEUE6	DMA_PRIORITY_QUEUE5	DMA_PRIORITY_QUEUE4	DMA_PRIORITY_QUEUE3	DMA_PRIORITY_QUEUE2	DMA_PRIORITY_QUEUE1	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DMA_PRIORITY_QUEUE15	DMA_PRIORITY_QUEUE14	DMA_PRIORITY_QUEUE13	DMA_PRIORITY_QUEUE12	DMA_PRIORITY_QUEUE11	DMA_PRIORITY_QUEUE10	DMA_PRIORITY_QUEUE9	DMA_PRIORITY_QUEUE8

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R			
HW Access	W	W	W	W	W			
Name	DMA_ADDR_WIDTH_IS_64B	HOST_IF_SOFT_SELECT	TX_ADD_FIFO_IF	EXT_TSU_TIMER	TX_PBUF_QUEUE_SEGMENT_SIZE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [31:28]				PBUF_LSO	PBUF_RSC	PBUF_CUTTHRU	PFC_MULTI_QUANTUM

Bits	Name	Description
27	PBUF_LSO	Write ignore, read the default value Default Value: 0
26	PBUF_RSC	Write ignore, read the default value Default Value: 0
25	PBUF_CUTTHRU	Write ignore, read the default value Default Value: 1
24	PFC_MULTI_QUANTUM	Write ignore, read the default value Default Value: 1
23	DMA_ADDR_WIDTH_IS_64B	Write ignore, read the default value Default Value: 0
22	HOST_IF_SOFT_SELECT	Write ignore, read the default value Default Value: 0
21	TX_ADD_FIFO_IF	Write ignore, read the default value Default Value: 0
20	EXT_TSU_TIMER	Write ignore, read the default value Default Value: 0

25.1.130 ETH0_DESIGNCFG_DEBUG6 (continued)

19 : 16	TX_PBUF_QUEUE_SEG-MENT_SIZE	Write ignore, read the default value Default Value: 0x2
15	DMA_PRIORITY_-QUEUE15	Write ignore, read the default value Default Value: 0
14	DMA_PRIORITY_-QUEUE14	Write ignore, read the default value Default Value: 0
13	DMA_PRIORITY_-QUEUE13	Write ignore, read the default value Default Value: 0
12	DMA_PRIORITY_-QUEUE12	Write ignore, read the default value Default Value: 0
11	DMA_PRIORITY_-QUEUE11	Write ignore, read the default value Default Value: 0
10	DMA_PRIORITY_-QUEUE10	Write ignore, read the default value Default Value: 0
9	DMA_PRIORITY_-QUEUE9	Write ignore, read the default value Default Value: 0
8	DMA_PRIORITY_-QUEUE8	Write ignore, read the default value Default Value: 0
7	DMA_PRIORITY_-QUEUE7	Write ignore, read the default value Default Value: 0
6	DMA_PRIORITY_-QUEUE6	Write ignore, read the default value Default Value: 0
5	DMA_PRIORITY_-QUEUE5	Write ignore, read the default value Default Value: 0
4	DMA_PRIORITY_-QUEUE4	Write ignore, read the default value Default Value: 0
3	DMA_PRIORITY_-QUEUE3	Write ignore, read the default value Default Value: 0
2	DMA_PRIORITY_-QUEUE2	Write ignore, read the default value Default Value: 1
1	DMA_PRIORITY_-QUEUE1	Write ignore, read the default value Default Value: 1

25.1.131 ETH0_DESIGNCFG_DEBUG7

Description: Design Configuration Register 7

Address: 0x42C11298

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	X_PBUF_NUM_SEGMENTS_Q1 [7:4]				X_PBUF_NUM_SEGMENTS_Q0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	W				W			
Name	X_PBUF_NUM_SEGMENTS_Q3 [15:12]				X_PBUF_NUM_SEGMENTS_Q2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	W				W			
Name	X_PBUF_NUM_SEGMENTS_Q5 [23:20]				X_PBUF_NUM_SEGMENTS_Q4 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	X_PBUF_NUM_SEGMENTS_Q7 [31:28]				X_PBUF_NUM_SEGMENTS_Q6 [27:24]			

Bits	Name	Description
31 : 28	X_PBUF_NUM_SEGMENTS_Q7	Write ignore, read the default value Default Value: 0x0
27 : 24	X_PBUF_NUM_SEGMENTS_Q6	Write ignore, read the default value Default Value: 0x0
23 : 20	X_PBUF_NUM_SEGMENTS_Q5	Write ignore, read the default value Default Value: 0x0
19 : 16	X_PBUF_NUM_SEGMENTS_Q4	Write ignore, read the default value Default Value: 0x0
15 : 12	X_PBUF_NUM_SEGMENTS_Q3	Write ignore, read the default value Default Value: 0x0
11 : 8	X_PBUF_NUM_SEGMENTS_Q2	Write ignore, read the default value Default Value: 0x0
7 : 4	X_PBUF_NUM_SEGMENTS_Q1	Write ignore, read the default value Default Value: 0x0
3 : 0	X_PBUF_NUM_SEGMENTS_Q0	Write ignore, read the default value Default Value: 0x1

25.1.132 ETH0_DESIGNCFG_DEBUG8

Description: Design Configuration Register 8

Address: 0x42C1129C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	NUM_SCR2_COMPARE_REGS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	NUM_SCR2_ETHTYPE_REGS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	NUM_TYPE2_SCREENERS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	NUM_TYPE1_SCREENERS [31:24]							

Bits	Name	Description
31 : 24	NUM_TYPE1_SCREEN-ERS	Write ignore, read the default value Default Value: 0x10
23 : 16	NUM_TYPE2_SCREEN-ERS	Write ignore, read the default value Default Value: 0x10
15 : 8	NUM_SCR2_ETH-TYPE_REGS	Write ignore, read the default value Default Value: 0x08
7 : 0	NUM_SCR2_COM-PARE_REGS	Write ignore, read the default value Default Value: 0x20

25.1.133 ETH0_DESIGNCFG_DEBUG9

Description: Design Configuration Register 9

Address: 0x42C112A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	TX_PBUF_NUM_SEGMENTS_Q9 [7:4]				TX_PBUF_NUM_SEGMENTS_Q8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	W				W			
Name	TX_PBUF_NUM_SEGMENTS_Q11 [15:12]				TX_PBUF_NUM_SEGMENTS_Q10 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	W				W			
Name	TX_PBUF_NUM_SEGMENTS_Q13 [23:20]				TX_PBUF_NUM_SEGMENTS_Q12 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	TX_PBUF_NUM_SEGMENTS_Q15 [31:28]				TX_PBUF_NUM_SEGMENTS_Q14 [27:24]			

Bits	Name	Description
31 : 28	TX_PBUF_NUM_SEGMENTS_Q15	Write ignore, read the default value Default Value: 0x0
27 : 24	TX_PBUF_NUM_SEGMENTS_Q14	Write ignore, read the default value Default Value: 0x0
23 : 20	TX_PBUF_NUM_SEGMENTS_Q13	Write ignore, read the default value Default Value: 0x0
19 : 16	TX_PBUF_NUM_SEGMENTS_Q12	Write ignore, read the default value Default Value: 0x0
15 : 12	TX_PBUF_NUM_SEGMENTS_Q11	Write ignore, read the default value Default Value: 0x0
11 : 8	TX_PBUF_NUM_SEGMENTS_Q10	Write ignore, read the default value Default Value: 0x0
7 : 4	TX_PBUF_NUM_SEGMENTS_Q9	Write ignore, read the default value Default Value: 0x0
3 : 0	TX_PBUF_NUM_SEGMENTS_Q8	Write ignore, read the default value Default Value: 0x0

25.1.134 ETH0_DESIGNCFG_DEBUG10

Description: Design Configuration Register 10

Address: 0x42C112A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	AXI_TX_DESCR_WR_BUFF_BITS [7:4]				AXI_RX_DESCR_WR_BUFF_BITS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	W				W			
Name	AXI_TX_DESCR_RD_BUFF_BITS [15:12]				AXI_RX_DESCR_RD_BUFF_BITS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	W				W			
Name	RX_PBUF_DATA [23:20]				AXI_ACCESS_PIPELINE_BITS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	EMAC_BUS_WIDTH [31:28]				TX_PBUF_DATA [27:24]			

Bits	Name	Description
31 : 28	EMAC_BUS_WIDTH	Write ignore, read the default value Default Value: 1
27 : 24	TX_PBUF_DATA	Write ignore, read the default value Default Value: 0x4
23 : 20	RX_PBUF_DATA	Write ignore, read the default value Default Value: 0x4
19 : 16	AXI_ACCESS_PIPE-LINE_BITS	Write ignore, read the default value Default Value: 0x1
15 : 12	AXI_TX_DE-SCR_RD_BUFF_BITS	Write ignore, read the default value Default Value: 0x1
11 : 8	AXI_RX_DE-SCR_RD_BUFF_BITS	Write ignore, read the default value Default Value: 0x1
7 : 4	AXI_TX_DE-SCR_WR_BUFF_BITS	Write ignore, read the default value Default Value: 0x1
3 : 0	AXI_RX_DE-SCR_WR_BUFF_BITS	Write ignore, read the default value Default Value: 0x1

25.1.135 ETH0_SPEC_ADD5_BOTTOM

Description: Specific address registers 5 ~ 36 doesn't present. Access to the register returns AHB error.

Address: 0x42C11300

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	RESERVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.136 ETH0_SPEC_ADD36_BOTTOM

Description: Not presents.

Address: 0x42C113F8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RESERVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	RESERVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.137 ETH0_INT_Q1_STATUS

Description: Priority queue Interrupt Status Register

Address: 0x42C11400

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	Reserved		R	R	Reserved
HW Access	W	W	W	Reserved		W	W	Reserved
Name	TRANS-MIT_COM-PLETE	AMBA_ER-ROR	RE-TRY_LIM-IT_EXCEE DED_OR_L ATE_COL-LISION	Reserved [4:3]		RX-_USED_BIT _READ	RECEIVE_-COMPLETE	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R	Reserved		
HW Access	Reserved				W	Reserved		
Name	Reserved [15:12]				RE-SP_NOT_O K	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	RESP_NOT_OK	bresp not OK Default Value: 0
7	TRANSMIT_COMPLETE	Transmit complete Default Value: 0
6	AMBA_ERROR	Transmit frame corruption due to AMBA (AXI/AHB) error set if an error occurs whilst midway through reading transmit frame from the external memory, including HRESP (read/write response on AHB interface for DMA access), RRESP or BRESP (read/write response on AXI interface for DMA access) errors and buffers exhausted mid frame. Default Value: 0
5	RETRY_LIMIT_EXCEED-ED_OR_LATE_COLLI-SION	Retry limit exceeded or late collision Default Value: 0
2	RX_USED_BIT_READ	RX used bit read Default Value: 0
1	RECEIVE_COMPLETE	Receive complete Default Value: 0

25.1.138 ETH0_INT_Q3_STATUS

Description: int_q3_status to int_q15_status doesn't present. Access to the register returns AHB error.

Address: 0x42C11408

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0

25.1.139 ETH0_TRANSMIT_Q1_PTR

Description: This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.

Address: 0x42C11440

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	RW
HW Access	R						Reserved	R
Name	DMA_TX_Q_PTR [7:2]						Reserved	DMA_TX_DIS_Q

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DMA_TX_Q_PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DMA_TX_Q_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DMA_TX_Q_PTR [31:24]							

Bits	Name	Description
31 : 2	DMA_TX_Q_PTR	This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four clk_sys cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AHB/AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit or 128bit, the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AHB/AXI access. For 32bit datapaths, the descriptors should be aligned at 32-bit boundaries and the descriptors are read from memory using two individual 32-bit non sequential accesses. Default Value: 0x00000000
0	DMA_TX_DIS_Q	Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while transmit is not enabled. Default Value: 0

25.1.140 ETH0_TRANSMIT_Q2_PTR

Description: This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.

Address: 0x42C11444

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	RW
HW Access	R						Reserved	R
Name	DMA_TX_Q_PTR [7:2]						Reserved	DMA_TX_DIS_Q

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DMA_TX_Q_PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DMA_TX_Q_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DMA_TX_Q_PTR [31:24]							

Bits	Name	Description
31 : 2	DMA_TX_Q_PTR	This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four clk_sys cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AHB/AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit or 128bit, the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AHB/AXI access. For 32bit datapaths, the descriptors should be aligned at 32-bit boundaries and the descriptors are read from memory using two individual 32-bit non sequential accesses Default Value: 0x00000000
0	DMA_TX_DIS_Q	Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while transmit is not enabled. Default Value: 0

25.1.141 ETH0_TRANSMIT_Q3_PTR

Description: transmit_q3_ptr to transmit_q15_ptr doesn't present. Access to the register returns AHB error.

Address: 0x42C11448

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.142 ETH0_RECEIVE_Q1_PTR

Description: This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The transmit buffer queue base address register must be initialized before transmit is started through bit 9 of the network control register. Once transmission has started, any write to the transmit buffer queue base address register is illegal and therefore ignored. Note that due to clock boundary synchronization, it takes a maximum of four pclk cycles from the writing of the transmit start bit before the transmitter is active. Writing to the transmit buffer queue base address register during this time may produce unpredictable results. Reading this register returns the location of the descriptor currently being accessed. Because the DMA can store data for multiple frames at once, this may not necessarily be pointing to the current frame being transmitted. In terms of AMBA AXI operation, the transmit descriptors are written to memory using a single 32bit AHB access. When the datapath is configured as 64bit , the transmit descriptors should be aligned at 64-bit boundaries and each pair of 32-bit descriptors is read from memory using a single AXI access.

Address: 0x42C11480

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	RW
HW Access	R						Reserved	R
Name	DMA_RX_Q_PTR [7:2]						Reserved	DMA_RX_DIS_Q

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DMA_RX_Q_PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DMA_RX_Q_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DMA_RX_Q_PTR [31:24]							

Bits	Name	Description
31 : 2	DMA_RX_Q_PTR	Receive buffer queue base address - written with the address of the start of the receive queue. Default Value: 0x00000000
0	DMA_RX_DIS_Q	Disable queue if set to 1. This can be used to reduce the number of active queues and should only be changed while receive is not enabled. Default Value: 0

25.1.143 ETH0_RECEIVE_Q3_PTR

Description: Not presents. Start address register doesn't present for queue3 ~ queue7.

Address: 0x42C11488

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.144 ETH0_DMA_RXBUF_SIZE_Q1

Description: Receive Buffer queue 1 Size

Address: 0x42C114A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DMA_RX_Q_BUF_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DMA_RX_Q_BUF_SIZE	DMA receive buffer size in system memory. The value defined by these bits determines the size of buffer to use in main system memory when writing received data. The value is defined in multiples of 64 bytes. 0x01 corresponds to buffers of 64 bytes. 0x02 corresponds to 128 bytes etc. For example: 0x02: 128 byte 0x18: 1536 byte (1*max length frame/buffer) 0xA0: 10240 byte (1*10K jumbo frame/buffer) Note that this value should never be written as zero. Default Value: 0x18

25.1.145 ETH0_DMA_RXBUF_SIZE_Q2

Description: Receive Buffer queue 2 Size

Address: 0x42C114A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DMA_RX_Q_BUF_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DMA_RX_Q_BUF_SIZE	DMA receive buffer size in system memory. The value defined by these bits determines the size of buffer to use in main system memory when writing received data. The value is defined in multiples of 64 bytes. 0x01 corresponds to buffers of 64 bytes. 0x02 corresponds to 128 bytes etc. For example: 0x02: 128 byte 0x18: 1536 byte (1*max length frame/buffer) 0xA0: 10240 byte (1*10K jumbo frame/buffer) Note that this value should never be written as zero. Default Value: 0x18

25.1.146 ETH0_DMA_RXBUF_SIZE_Q3

Description: dma_rxbuf_size_q3 to dma_rxbuf_size_q7 doesn't present.

Address: 0x42C114A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.147 ETH0_CBS_CONTROL

Description: The IdleSlope value is defined as the rate of change of credit when a packet is waiting to be sent. This must not exceed the portTransmitRate which is dependent on the speed of operation, eg, portTranmsitRate. 1Gb/s = 32'h07735940 (125 Mbytes/s), 100Mb/sec = 32'h017D7840 (25 Mnibbles/s), 10Mb/sec = 32'h002625A0 (2.5 Mnibbles/s). If 50% of bandwidth was to be allocated to a particular queue in 1Gb/sec mode then the IdleSlope value for that queue would be calculated as 32'h07735940/2. Note that Credit-Based Shaping should be disabled prior to updating the IdleSlope values. As another example, for a 1722 audio packet with a payload of 6 samples per channel, the packet size would be 7 (preamble) + 1 (SFD) + 50 (packet header) + 6x4x2(payload) + 4 (CRC) = 110 bytes. For a rate of 8000 packets per second, the desired rate would 110 x 8000 bytes per second, so the programmed idleSlope value would be 880000 for a 1Gb/s connection, or 1760000 for a 100Mb/s or 10Mbs connection. See Figure 6.3 in the IEEE 1722 standard. In practice, the actual transmission rate will be vary slightly from that calculated. In this case, the idleSlope value should be recalibrated based on the variance between the measured and expected rate, and in this case very accurate transmission rates can be achieved.

Address: 0x42C114BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						CBS_ENABLE_QUEUE_B	CBS_ENABLE_QUEUE_A

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	CBS_ENABLE_QUEUE_B	Enable Credit-Based shaping on the 2nd highest priority queue (queue B). Write 1 to enable Default Value: 0
0	CBS_ENABLE_QUEUE_A	Enable Credit-Based Shaping on the highest priority queue (queue A). Write 1 to enable Default Value: 0

25.1.148 ETH0_CBS_IDLESLOPE_Q_A

Description: queue A is the highest priority queue. This would be queue 8 in an 8 queue configuration.

Address: 0x42C114C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IDLESLOPE_A [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IDLESLOPE_A [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	IDLESLOPE_A [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	IDLESLOPE_A [31:24]							

Bits	Name	Description
31 : 0	IDLESLOPE_A	IdleSlope value for queue A in bytes/sec for gigabit operation and nibbles/sec for 10/100 operation Default Value: 0x00000000

25.1.149 ETH0_CBS_IDLESLOPE_Q_B

Description: queue B is the 2nd highest priority queue. This would be queue 7 in an 8 queue configuration.

Address: 0x42C114C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IDLESLOPE_B [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IDLESLOPE_B [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	IDLESLOPE_B [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	IDLESLOPE_B [31:24]							

Bits	Name	Description
31 : 0	IDLESLOPE_B	IdleSlope value for queue B in bytes/sec for gigabit operation and nibbles/sec for 10/100 operation Default Value: 0x00000000

25.1.150 ETH0_UPPER_TX_Q_BASE_ADDR

Description: Upper 32 bits of transmit buffer descriptor queue base address.

Address: 0x42C114C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UPPER_TX_Q_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	UPPER_TX_Q_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UPPER_TX_Q_BASE_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	UPPER_TX_Q_BASE_ADDR [31:24]							

Bits	Name	Description
31 : 0	UPPER_TX- _Q_BASE_ADDR	Upper 32 bits of transmit buffer descriptor queue base address. Used when 64 bit addressing is enabled. Default Value: 0x00000000

25.1.151 ETH0_TX_BD_CONTROL

Description: TX BD control register

Address: 0x42C114CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW		Reserved			
HW Access	Reserved		R		Reserved			
Name	Reserved [7:6]		TX_BD_TS_MODE [5:4]		Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 4	TX_BD_TS_MODE	TX Descriptor Timestamp Insertion mode, 00: TS insertion disable, 01: TS inserted for PTP Event Frames only, 10: TS inserted for All PTP Frames only, 11: TS insertion for All Frames Default Value: 0x0

25.1.152 ETH0_RX_BD_CONTROL

Description: RX BD control register

Address: 0x42C114D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW		Reserved			
HW Access	Reserved		R		Reserved			
Name	Reserved [7:6]		RX_BD_TS_MODE [5:4]		Reserved [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 4	RX_BD_TS_MODE	RX Descriptor Timestamp Insertion mode, 00: TS insertion disable, 01: TS inserted for PTP Event Frames only, 10: TS inserted for All PTP Frames only, 11: TS insertion for All Frames Default Value: 0x0

25.1.153 ETH0_UPPER_RX_Q_BASE_ADDR

Description: Upper 32 bits of receive buffer descriptor queue base address.

Address: 0x42C114D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UPPER_RX_Q_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	UPPER_RX_Q_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UPPER_RX_Q_BASE_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	UPPER_RX_Q_BASE_ADDR [31:24]							

Bits	Name	Description
31 : 0	UPPER_RX- _Q_BASE_ADDR	Upper 32 bits of receive buffer descriptor queue base address. Used when 64 bit addressing is enabled. Default Value: 0x00000000

25.1.154 ETH0_HIDDEN_REG0

Description: Hidden register

Address: 0x42C114E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HIDDEN0_FIELD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	HIDDEN0_FIELD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	HIDDEN0_FIELD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	HIDDEN0_FIELD [31:24]							

Bits	Name	Description
31 : 0	HIDDEN0_FIELD	Writing is prohibited. Default Value: 0x002625A0

25.1.155 ETH0_HIDDEN_REG1

Description: Hidden register

Address: 0x42C114E4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HIDDEN1_FIELD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	HIDDEN1_FIELD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	HIDDEN1_FIELD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	HIDDEN1_FIELD [31:24]							

Bits	Name	Description
31 : 0	HIDDEN1_FIELD	Writing is prohibited. Default Value: 0x017D7840

25.1.156 ETH0_HIDDEN_REG2

Description: Hidden register

Address: 0x42C114E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HIDDEN2_FIELD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	HIDDEN2_FIELD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	HIDDEN2_FIELD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	HIDDEN2_FIELD [31:24]							

Bits	Name	Description
31 : 0	HIDDEN2_FIELD	Writing is prohibited. Default Value: 0x07735940

25.1.157 ETH0_HIDDEN_REG3

Description: Hidden register

Address: 0x42C114EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				HIDDEN3_FIELD [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	HIDDEN3_FIELD	Writing is prohibited. Default Value: 0x00000007

25.1.158 ETH0_SCREENING_TYPE_1_REGISTER_0

Description: Screening type 1 registers are used to allocate up to 16 priority queues to received frames based on certain IP or UDP fields of incoming frames. Firstly, when DS/TC match enable is set (bit 28), the DS (Differentiated Services) field of the received IPv4 header or TCfield (traffic class) of IPv6 headers are matched against bits 11 to 4. Secondly, when UDP port match enable is set (bit 29), the UDP Destination Port of the received UDP frame is matched against bits 27 to 12. Both UDP and DS/TC matching can be enabled simultaneously or individually. If a match is successful, then the queue value programmed in bits 2 to 0 is allocated to the frame. The required number of Type 1 screening registers is configured in the gem defines file. Up to 16 type 1 screening registers have been allocated APB address space between 0x500 and 0x53C.

Address: 0x42C11500

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.159 ETH0_SCREENING_TYPE_1_REGISTER_1

Description: screening type 1 register 1, same as screening_type_1_register_0

Address: 0x42C11504

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.160 ETH0_SCREENING_TYPE_1_REGISTER_2

Description: screening type 1 register 2, same as screening_type_1_register_0

Address: 0x42C11508

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.161 ETH0_SCREENING_TYPE_1_REGISTER_3

Description: screening type 1 register 3, same as screening_type_1_register_0

Address: 0x42C1150C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.162 ETH0_SCREENING_TYPE_1_REGISTER_4

Description: screening type 1 register 4, same as screening_type_1_register_0

Address: 0x42C11510

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.163 ETH0_SCREENING_TYPE_1_REGISTER_5

Description: screening type 1 register 5, same as screening_type_1_register_0

Address: 0x42C11514

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.164 ETH0_SCREENING_TYPE_1_REGISTER_6

Description: screening type 1 register 6, same as screening_type_1_register_0

Address: 0x42C11518

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.165 ETH0_SCREENING_TYPE_1_REGISTER_7

Description: screening type 1 register 7, same as screening_type_1_register_0

Address: 0x42C1151C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.166 ETH0_SCREENING_TYPE_1_REGISTER_8

Description: screening type 1 register 8, same as screening_type_1_register_0

Address: 0x42C11520

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.167 ETH0_SCREENING_TYPE_1_REGISTER_9

Description: screening type 1 register 9, same as screening_type_1_register_0

Address: 0x42C11524

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.168 ETH0_SCREENING_TYPE_1_REGISTER_10

Description: screening type 1 register 10, same as screening_type_1_register_0

Address: 0x42C11528

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.169 ETH0_SCREENING_TYPE_1_REGISTER_11

Description: screening type 1 register 11, same as screening_type_1_register_0

Address: 0x42C1152C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.170 ETH0_SCREENING_TYPE_1_REGISTER_12

Description: screening type 1 register 12, same as screening_type_1_register_0

Address: 0x42C11530

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.171 ETH0_SCREENING_TYPE_1_REGISTER_13

Description: screening type 1 register 13, same as screening_type_1_register_0

Address: 0x42C11534

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.172 ETH0_SCREENING_TYPE_1_REGISTER_14

Description: screening type 1 register 14, same as screening_type_1_register_0

Address: 0x42C11538

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.173 ETH0_SCREENING_TYPE_1_REGISTER_15

Description: screening type 1 register 15, same as screening_type_1_register_0

Address: 0x42C1153C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSTC_MATCH [7:4]				QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	UDP_PORT_MATCH [15:12]				DSTC_MATCH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDP_PORT_MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [31:30]		UDP_PORT_MATCH_ENABLE	DSTC_ENABLE	UDP_PORT_MATCH [27:24]			

Bits	Name	Description
29	UDP_PORT_MATCH_ENABLE	UDP port match enable Default Value: 0
28	DSTC_ENABLE	DS/TC Enable Default Value: 0
27 : 12	UDP_PORT_MATCH	UDP Port Match Default Value: 0x0000
11 : 4	DSTC_MATCH	DS/TC Match Default Value: 0x00
3 : 0	QUEUE_NUMBER	Queue Number (0 to 15) Default Value: 0x0

25.1.174 ETH0_SCREENING_TYPE_2_REGISTER_0

Description: Screener Type 2 match registers operate independently of screener type 1 registers and offer additional match capabilities, extending the capabilities into vendor specific protocols.

Address: 0x42C11540

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.174 ETH0_SCREENING_TYPE_2_REGISTER_0 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.175 ETH0_SCREENING_TYPE_2_REGISTER_1

Description: screening type 2 register 1, same as screening_type_2_register_0

Address: 0x42C11544

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.175 ETH0_SCREENING_TYPE_2_REGISTER_1 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.176 ETH0_SCREENING_TYPE_2_REGISTER_2

Description: screening type 2 register 2, same as screening_type_2_register_0

Address: 0x42C11548

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.176 ETH0_SCREENING_TYPE_2_REGISTER_2 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.177 ETH0_SCREENING_TYPE_2_REGISTER_3

Description: screening type 2 register 3, same as screening_type_2_register_0

Address: 0x42C1154C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.177 ETH0_SCREENING_TYPE_2_REGISTER_3 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.178 ETH0_SCREENING_TYPE_2_REGISTER_4

Description: screening type 2 register 4, same as screening_type_2_register_0

Address: 0x42C11550

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.178 ETH0_SCREENING_TYPE_2_REGISTER_4 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.179 ETH0_SCREENING_TYPE_2_REGISTER_5

Description: screening type 2 register 5, same as screening_type_2_register_0

Address: 0x42C11554

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.179 ETH0_SCREENING_TYPE_2_REGISTER_5 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.180 ETH0_SCREENING_TYPE_2_REGISTER_6

Description: screening type 2 register 6, same as screening_type_2_register_0

Address: 0x42C11558

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.180 ETH0_SCREENING_TYPE_2_REGISTER_6 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.181 ETH0_SCREENING_TYPE_2_REGISTER_7

Description: screening type 2 register 7, same as screening_type_2_register_0

Address: 0x42C1155C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.181 ETH0_SCREENING_TYPE_2_REGISTER_7 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.182 ETH0_SCREENING_TYPE_2_REGISTER_8

Description: screening type 2 register 8, same as screening_type_2_register_0

Address: 0x42C11560

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.182 ETH0_SCREENING_TYPE_2_REGISTER_8 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.183 ETH0_SCREENING_TYPE_2_REGISTER_9

Description: screening type 2 register 9, same as screening_type_2_register_0

Address: 0x42C11564

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.183 ETH0_SCREENING_TYPE_2_REGISTER_9 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.184 ETH0_SCREENING_TYPE_2_REGISTER_10

Description: screening type 2 register 10, same as screening_type_2_register_0

Address: 0x42C11568

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.184 ETH0_SCREENING_TYPE_2_REGISTER_10 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.185 ETH0_SCREENING_TYPE_2_REGISTER_11

Description: screening type 2 register 11, same as screening_type_2_register_0

Address: 0x42C1156C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.185 ETH0_SCREENING_TYPE_2_REGISTER_11 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.186 ETH0_SCREENING_TYPE_2_REGISTER_12

Description: screening type 2 register 12, same as screening_type_2_register_0

Address: 0x42C11570

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.186 ETH0_SCREENING_TYPE_2_REGISTER_12 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.187 ETH0_SCREENING_TYPE_2_REGISTER_13

Description: screening type 2 register 13, same as screening_type_2_register_0

Address: 0x42C11574

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.187 ETH0_SCREENING_TYPE_2_REGISTER_13 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.188 ETH0_SCREENING_TYPE_2_REGISTER_14

Description: screening type 2 register 14, same as screening_type_2_register_0

Address: 0x42C11578

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW					RW	RW	
HW Access	R					R	R	
Name	COMPARE_B [23:19]					COMPARE_A_ENABLE	COMPARE_A [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.188 ETH0_SCREENING_TYPE_2_REGISTER_14 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.189 ETH0_SCREENING_TYPE_2_REGISTER_15

Description: screening type 2 register 15, same as screening_type_2_register_0

Address: 0x42C1157C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	RESERVED_7	VLAN_PRIORITY [6:4]			QUEUE_NUMBER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW			RW
HW Access	R			R	R			R
Name	COMPARE_A [15:13]			ETHERTYPE_ENABLE	INDEX [11:9]			VLAN_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	RW		
HW Access	R				R	R		
Name	COMPARE_B [23:19]				COMPARE_A_ENABLE	COMPARE_A [17:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW					RW
HW Access	R	R	R					R
Name	RESERVED_31	COMPARE_C_ENABLE	COMPARE_C [29:25]					COMPARE_B_ENABLE

Bits	Name	Description
31	RESERVED_31	"Reserved, read as 0, ignored on write." Default Value: 0
30	COMPARE_C_ENABLE	"Compare C Enable" Default Value: 0
29 : 25	COMPARE_C	"Compare C - Index to screener type 2 Compare register" Default Value: 0x00
24	COMPARE_B_ENABLE	"Compare B Enable" Default Value: 0
23 : 19	COMPARE_B	"Compare B - Index to screener type 2 Compare register" Default Value: 0x00
18	COMPARE_A_ENABLE	"Compare A Enable" Default Value: 0
17 : 13	COMPARE_A	"Compare A - Index to screener type 2 Compare register " Default Value: 0x00
12	ETHERTYPE_ENABLE	"EtherType Enable" Default Value: 0

25.1.189 ETH0_SCREENING_TYPE_2_REGISTER_15 (continued)

11 : 9	INDEX	"Index to screener type 2 EtherType register" Default Value: 0x0
8	VLAN_ENABLE	"VLAN Enable" Default Value: 0
7	RESERVED_7	"Reserved and implemented as RW" Default Value: 0
6 : 4	VLAN_PRIORITY	"VLAN Priority" Default Value: 0x0
3 : 0	QUEUE_NUMBER	"Queue Number (0 to 15)" Default Value: 0x0

25.1.190 ETH0_TX_SCHED_CTRL

Description: This register controls the transmit scheduling algorithm the user can select for each active transmit queue. By default all queues are initialized to fixed priority, with the top indexed queue having overall priority

Address: 0x42C11580

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		RW		RW		RW	
HW Access								
Name	TX_SCHED_Q3 [7:6]		TX_SCHED_Q2 [5:4]		TX_SCHED_Q1 [3:2]		TX_SCHED_Q0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	REMOVED_31_8 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	REMOVED_31_8 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	REMOVED_31_8 [31:24]							

Bits	Name	Description
31 : 8	REMOVED_31_8	Write ignore, read 0 Default Value: 0x000000
7 : 6	TX_SCHED_Q3	Write ignore, read 0 Default Value: 0x0
5 : 4	TX_SCHED_Q2	"Queue 2 selection. 00 : Fixed Priority 01 : CBS Enabled only valid for top two enabled queues and if CBS capability selected. 10 : DWRR Enabled 11 : ETS Enabled Default Value: 0x0
3 : 2	TX_SCHED_Q1	"Queue 1 selection. 00 : Fixed Priority 01 : CBS Enabled only valid for top two enabled queues and if CBS capability selected. 10 : DWRR Enabled 11 : ETS Enabled" Default Value: 0x0
1 : 0	TX_SCHED_Q0	"Queue 0 selection. 00 : Fixed Priority 01 : CBS Enabled only valid for top two enabled queues and if CBS capability selected. 10 : DWRR Enabled 11 : ETS Enabled" Default Value: 0x0

25.1.191 ETH0_BW_RATE_LIMIT_Q0TO3

Description: This register holds the DWRR weighting value or the ETS bandwidth percentage value used by the transmit scheduler for queues 0 to 3.

Address: 0x42C11590

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DWRR_ETS_WEIGHT_Q0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DWRR_ETS_WEIGHT_Q1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DWRR_ETS_WEIGHT_Q2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	DWRR_ETS_WEIGHT_Q3 [31:24]							

Bits	Name	Description
31 : 24	DWRR_ETS_- WEIGHT_Q3	Write ignore, read 0 Default Value: 0x00
23 : 16	DWRR_ETS_- WEIGHT_Q2	"DWRR Weighting / ETS Bandwidth Allocation for queue 2" Default Value: 0x00
15 : 8	DWRR_ETS_- WEIGHT_Q1	"DWRR Weighting / ETS Bandwidth Allocation for queue 1" Default Value: 0x00
7 : 0	DWRR_ETS_- WEIGHT_Q0	"DWRR Weighting / ETS Bandwidth Allocation for queue 0" Default Value: 0x00

25.1.192 ETH0_BW_RATE_LIMIT_Q4TO7

Description: Not presents. EMAC has only 3 queues. Access to the register returns AHB error.

Address: 0x42C11594

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	"DWRR Weighting / ETS Bandwidth Allocation for queue 0" Default Value: 0x00

25.1.193 ETH0_BW_RATE_LIMIT_Q8TO11

Description: Not presents. EMAC has only 3 queues. Access to the register returns AHB error.

Address: 0x42C11598

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.194 ETH0_TX_Q_SEG_ALLOC_Q0TO7

Description: This register allows the user to distribute the Transmit SRAM used by the DMA across the priority queues, for queues 0 to 7. The SRAM itself is split into a number of evenly sized segments (this is defined in the verilog configuration defs file - for the configuration used to generate this register description, the total number of segments was set to '16'). Those segments can then be freely distributed across the active queues, in powers of 2. I.e. a value of 0 would mean 1 segment has been allocated to the queue. A value of 1 would mean 2 segments, a value of 2 means 4 segments and so on. The reset values of these registers are defined in the configuration defs file.

Address: 0x42C115A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW			R	RW		
HW Access	R	R			R	R		
Name	RE-SERVED_7_7	SEGMENT_ALLOC_Q1 [6:4]			RE-SERVED_3_3	SEGMENT_ALLOC_Q0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	R	R			R	RW		
HW Access	R	R			R	R		
Name	RE-SERVED_15_15	REMOVED_14_12 [14:12]			RE-SERVED_11_11	SEGMENT_ALLOC_Q2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	R	R			R	R		
HW Access	R	R			R	R		
Name	RE-SERVED_23	REMOVED_22_20 [22:20]			RE-SERVED_19_19	REMOVED_18_16 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	R	R			R	R		
HW Access	R	R			R	R		
Name	RE-SERVED_31_31	REMOVED_30_28 [30:28]			RE-SERVED_27_27	REMOVED_26_24 [26:24]		

Bits	Name	Description
31	RESERVED_31_31	Write ignore, read 0 Default Value: 0x0
30 : 28	REMOVED_30_28	Write ignore, read 0 Default Value: 0x0
27	RESERVED_27_27	Write ignore, read 0 Default Value: 0x0
26 : 24	REMOVED_26_24	Write ignore, read 0 Default Value: 0x0
23	RESERVED_23	Write ignore, read 0 Default Value: 0x0
22 : 20	REMOVED_22_20	Write ignore, read 0 Default Value: 0x0

25.1.194 ETH0_TX_Q_SEG_ALLOC_Q0TO7 (continued)

19	RESERVED_19_19	Write ignore, read 0 Default Value: 0x0
18 : 16	REMOVED_18_16	Write ignore, read 0 Default Value: 0x0
15	RESERVED_15_15	Write ignore, read 0 Default Value: 0x0
14 : 12	REMOVED_14_12	Write ignore, read 0 Default Value: 0x0
11	RESERVED_11_11	Write ignore, read 0 Default Value: 0x0
10 : 8	SEGMENT_ALLOC_Q2	Number of segments allocated to q2. This should be entered as a log 2, for example entering a value of 2 would grant 4 segments. A maximum of 32 segments can be granted Default Value: 0x0
7	RESERVED_7_7	Reserved, read as 0, ignored on write. Default Value: 0x0
6 : 4	SEGMENT_ALLOC_Q1	Number of segments allocated to q1. This should be entered as a log 2, for example entering a value of 2 would grant 4 segments. A maximum of 32 segments can be granted Default Value: 0x0
3	RESERVED_3_3	Reserved, read as 0, ignored on write. Default Value: 0x0
2 : 0	SEGMENT_ALLOC_Q0	Number of segments allocated to q0. This should be entered as a log 2, for example entering a value of 2 would grant 4 segments. A maximum of 32 segments can be granted. Default Value: 0x1

25.1.195 ETH0_TX_Q_SEG_ALLOC_Q8TO15

Description: Not presents. Access to the register returns AHB error.

Address: 0x42C115A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.196 ETH0_RECEIVE_Q8_PTR

Description: receive_q8_ptr to receive_q15_ptr doesn't present. Access to the register returns AHB error.

Address: 0x42C115C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.197 ETH0_DMA_RXBUF_SIZE_Q8

Description: dma_rxbuf_size_q8 to dma_rxbuf_size_q15 doesn't present. Access to the register returns AHB error.

Address: 0x42C115E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.198 ETH0_INT_Q1_ENABLE

Description: At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero.

Address: 0x42C11600

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	W	W	Reserved		W	W	Reserved
HW Access	R	R	R	Reserved		R	R	Reserved
Name	ENABLE_TRANSMIT_COMPLETE_INTERRUPT	ENABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT	ENABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT	Reserved [4:3]		ENABLE_RX_USED_BIT_READ_INTERRUPT	ENABLE_RECEIVE_COMPLETE_INTERRUPT	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				W	Reserved		
HW Access	Reserved				R	Reserved		
Name	Reserved [15:12]				ENABLE_RESP_NOT_OK_INTERRUPT	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	ENABLE_RESP_NOT_OK_INTERRUPT	Enable bresp not OK interrupt Default Value: 0
7	ENABLE_TRANSMIT_COMPLETE_INTERRUPT	Enable Transmit complete interrupt Default Value: 0
6	ENABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT	Enable Transmit frame corruption due to AMBA (AXI/AHB) error interrupt Default Value: 0

25.1.198 ETH0_INT_Q1_ENABLE (continued)

5	ENABLE_RETRY_LIMIT_-EXCEED-ED_OR_LATE_COLLISIO N_INTERRUPT	Enable Retry limit exceeded or late collision interrupt Default Value: 0
2	ENABLE_RX-_USED_BIT_READ_IN-TERRUPT	Enable RX used bit read interrupt Default Value: 0
1	ENABLE_RECEIVE_-COMPLETE_INTERRUPT	Enable Receive complete interrupt Default Value: 0

25.1.199 ETH0_INT_Q3_ENABLE

Description: int_q3_enable to int_q7_enable doesn't present. Access to the register returns AHB error.

Address: 0x42C11608

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.200 ETH0_INT_Q1_DISABLE

Description: Writing a 1 to the relevant bit location disables that particular interrupt. This register is write only and when read will return zero.

Address: 0x42C11620

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	W	W	Reserved		W	W	Reserved
HW Access	R	R	R	Reserved		R	R	Reserved
Name	DISABLE_TRANSMIT_COMPLETE_INTERRUPT	DISABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT	DISABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT	Reserved [4:3]		DISABLE_RX_USED_BIT_READ_INTERRUPT	DISABLE_RECEIVE_COMPLETE_INTERRUPT	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				W	Reserved		
HW Access	Reserved				R	Reserved		
Name	Reserved [15:12]				DISABLE_RESP_NOT_OK_INTERRUPT	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	DISABLE_RESP_NOT_OK_INTERRUPT	Disable bresp not OK interrupt Default Value: 0
7	DISABLE_TRANSMIT_COMPLETE_INTERRUPT	Disable Transmit complete interrupt Default Value: 0
6	DISABLE_TRANSMIT_FRAME_CORRUPTION_DUE_TO_AMBA_ERROR_INTERRUPT	Disable Transmit frame corruption due to AMBA (AXI/AHB) error interrupt Default Value: 0
5	DISABLE_RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT	Disable Retry limit exceeded or late collision interrupt Default Value: 0

25.1.200 ETH0_INT_Q1_DISABLE (continued)

2	DISABLE_RX- _USED_BIT_READ_IN- TERRUPT	Disable RX used bit read interrupt Default Value: 0
1	DISABLE_RECEIVE_- COMPLETE_INTERRUPT	Disable Receive complete interrupt Default Value: 0

25.1.201 ETH0_INT_Q3_DISABLE

Description: int_q3_disable to int_q7_disable doesn't present. Access to the register returns AHB error.

Address: 0x42C11628

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.202 ETH0_INT_Q1_MASK

Description: The interrupt mask register is a read only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the interrupt enable register or set individually by writing to the interrupt disable register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the interrupt mask register. For test purposes there is a write-only function to this register that allows the bits in the interrupt status register to be set or cleared, regardless of the state of the mask register.

Address: 0x42C11640

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	Reserved		R	R	Reserved
HW Access	W	W	W	Reserved		W	W	Reserved
Name	TRANS-MIT_COM-PLETE_INT ER-RUPT_MAS K	AMBA_ER-ROR_IN-TERRUPT_ MASK	RE-TRY_LIM-IT_EXCEE DED_OR_L ATE_COL-LISION_IN-TERRUPT_ MASK	Reserved [4:3]		RX-_USED_IN-TERRUPT_ MASK	RECEIVE_-COM-PLETE_INT ER-RUPT_MAS K	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R	Reserved		
HW Access	Reserved				W	Reserved		
Name	Reserved [15:12]				RE-SP_NOT_O K_INTER-RUPT_MAS K	Reserved [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	RESP_NOT_OK_INTER-RUPT_MASK	bresp not OK interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
7	TRANSMIT_COM-PLETE_INTER-RUPT_MASK	transmit complete interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1

25.1.202 ETH0_INT_Q1_MASK (continued)

6	AMBA_ERROR_INTERRUPT_MASK	A read of this register returns the value of the AMBA (AXI/AHB) error interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
5	RETRY_LIMIT_EXCEEDED_OR_LATE_COLLISION_INTERRUPT_MASK	retry limit exceeded or late collision interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
2	RX_USED_INTERRUPT_MASK	A read of this register returns the value of the RX Used interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1
1	RECEIVE_COMPLETE_INTERRUPT_MASK	receive complete interrupt mask. 0: Interrupt is enabled. 1: Interrupt is disabled. A write to this register directly affects the state of the corresponding bit in the interrupt status register, causing an interrupt to be generated if a 1 is written. Default Value: 1

25.1.203 ETH0_INT_Q3_MASK

Description: int_q3_mask to int_q7_mask doesn't present. Access to the register returns AHB error.

Address: 0x42C11648

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.204 ETH0_INT_Q8_ENABLE

Description: int_q8_enable to int_q15_enable doesn't present. Access to the register returns AHB error.

Address: 0x42C11660

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.205 ETH0_INT_Q8_DISABLE

Description: int_q8_disable to int_q15_disable doesn't present. Access to the register returns AHB error.

Address: 0x42C11680

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.206 ETH0_INT_Q8_MASK

Description: int_q8_mask to int_q15_mask doesn't present. Access to the register returns AHB error.

Address: 0x42C116A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	REMOVED_31_0 [31:24]							

Bits	Name	Description
31 : 0	REMOVED_31_0	Write ignore, read 0 Default Value: 0x0

25.1.207 ETH0_SCREENING_TYPE_2_ETHERTYPE_REG_0

Description: Ethertype Register

Address: 0x42C116E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMPARE_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMPARE_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RESERVED_31_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RESERVED_31_16 [31:24]							

Bits	Name	Description
31 : 16	RESERVED_31_16	"Reserved, read as 0, ignored on write " Default Value: 0x0000
15 : 0	COMPARE_VALUE	"EtherType compare value" Default Value: 0x0000

25.1.208 ETH0_TYPE2_COMPARE_0_WORD_0

Description: "Compare A, B and C fields of the screener type 2 match register are pointers to a pool of up to 32 compare registers. If enabled the compare is true if the data at the OFFSET into the frame, ANDed with the MASK Value if the mask is enabled, is equal to the COMPARE Value. Either a 16 bit comparison or a 32 bit comparison is done. This selection is made via the associated compare word1 register bit 9. If a 16 bit comparison is selected, then a 16 bit mask is also available to the user to select which bits should be compared. If the 32 bit compare option is selected, then no mask is available. The byte at the OFFSET number of bytes from the index start is compared thru bits 7 to 0 of the configured VALUE. The byte at the OFFSET number of bytes + 1 from the index start is compared thru bits 15 to 8 of the configured VALUE and so on. The OFFSET can be configured to be from 0 to 127 bytes from either the start of the frame, the byte following the therType field (last EtherType in the header if the frame is VLAN tagged), the byte following the IP header (IPv4 or IPv6) or from the byte following the start of the TCP/UDP header. The required number of Type 2 screening registers up to a maximum of 32 is configurable in the gem defines file and have been allocated APB address space between 0x700 and 0x7fc. Note. when using RX Partial Store and Forward mode and priority queues, the frame offset must be less than the Partial Store and Forward watermark. If the offset is higher than the watermark value it's not possible to identify the priority queue before the frame is sent to the AMBA interface, and an incorrect priority queue may be used. "

Address: 0x42C11700

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MASK_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MASK_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMPARE_VALUE_TYPE2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	COMPARE_VALUE_TYPE2 [31:24]							

Bits	Name	Description
31 : 16	COMPARE_VALUE_-TYPE2	2 byte Compare Value. If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3. If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. Default Value: 0x0000
15 : 0	MASK_VALUE	These bits can be either a 2 byte mask field or an additional 2 byte Compare Value. If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1. If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. Default Value: 0x0000

25.1.209 ETH0_TYPE2_COMPARE_0_WORD_1

Description: "Type2 Compare Word 1"

Address: 0x42C11704

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	COMPARE_OFFSET	OFFSET_VALUE [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	R						RW	RW
HW Access	R						R	R
Name	RESERVED_31_10 [15:10]						DISABLE_MASK	COMPARE_OFFSET

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RESERVED_31_10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RESERVED_31_10 [31:24]							

Bits	Name	Description
31 : 10	RESERVED_31_10	"Reserved, read as 0, ignored on write." Default Value: 0x000000
9	DISABLE_MASK	"This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value. 1 - 4-byte compare value 0 - 2-byte compare, 2-byte mask " Default Value: 0
8 : 7	COMPARE_OFFSET	"Compare byte offset. 00 : Offset from beginning of the frame. 01 : Offset from byte after Ether Type. 10 : Offset from byte following end of IP header. 11 : Offset from byte following end of TCP/UDP header" If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3. If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. Default Value: 0x0
6 : 0	OFFSET_VALUE	"Offset value in bytes" Default Value: 0x00

25.1.210 ETH0_TYPE2_COMPARE_1_WORD_0

Description: same as type2_compare_0_word_0

Address: 0x42C11708

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MASK_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MASK_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMPARE_VALUE_TYPE2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	COMPARE_VALUE_TYPE2 [31:24]							

Bits	Name	Description
31 : 16	COMPARE_VALUE_-TYPE2	2 byte Compare Value. If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3. If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. Default Value: 0x0000
15 : 0	MASK_VALUE	These bits can be either a 2 byte mask field or an additional 2 byte Compare Value. If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [7:0] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [15:8] is compared against the byte in the received frame from the selected offset+1. If bit 9 of the associated compare_word1 register is clear, these bits become a direct 2-byte mask for the 2-byte compare register in bits [31:16]. Default Value: 0x0000

25.1.211 ETH0_TYPE2_COMPARE_1_WORD_1

Description: same as type2_compare_0_word_1

Address: 0x42C1170C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	COMPARE_OFFSET	OFFSET_VALUE [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	R						RW	RW
HW Access	R						R	R
Name	RESERVED_31_10 [15:10]						DISABLE_MASK	COMPARE_OFFSET

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RESERVED_31_10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RESERVED_31_10 [31:24]							

Bits	Name	Description
31 : 10	RESERVED_31_10	"Reserved, read as 0, ignored on write." Default Value: 0x000000
9	DISABLE_MASK	"This bit is used to control whether the compare register word_0 contains a 4-byte compare value, or a 2-byte compare value with a 2-byte mask value. 1 - 4-byte compare value 0 - 2-byte compare, 2-byte mask " Default Value: 0
8 : 7	COMPARE_OFFSET	"Compare byte offset. 00 : Offset from beginning of the frame. 01 : Offset from byte after Ether Type. 10 : Offset from byte following end of IP header. 11 : Offset from byte following end of TCP/UDP header" If bit 9 of the associated compare_word1 register is set, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+2 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+3. If bit 9 of the associated compare_word1 register is clear, then the byte stored in bits [23:16] is compared against the byte in the received frame from the selected offset+0 and the byte stored in bits [31:24] is compared against the byte in the received frame from the selected offset+1. Default Value: 0x0
6 : 0	OFFSET_VALUE	"Offset value in bytes" Default Value: 0x00

26 Controller Area Network Flexible Data- Rate (CAN-FD) registers

This section discusses the CAN-FD registers. It lists all the registers in mapping tables, in address order.

26.1 Register details

Register name	Address	Description
CANFD0_CH0_CREL	0x42840000	Core Release Register
CANFD0_CH0_ENDN	0x42840004	Endian Register
CANFD0_CH0_DBTP	0x4284000C	Data Bit Timing & Prescaler Register
CANFD0_CH0_TEST	0x42840010	Test Register
CANFD0_CH0_RWD	0x42840014	RAM Watchdog
CANFD0_CH0_CCCR	0x42840018	CC Control Register
CANFD0_CH0_NBTP	0x4284001C	Nominal Bit Timing & Prescaler Register
CANFD0_CH0_TSCC	0x42840020	Timestamp Counter Configuration
CANFD0_CH0_TSCV	0x42840024	Timestamp Counter Value
CANFD0_CH0_TOCC	0x42840028	Timeout Counter Configuration
CANFD0_CH0_TOCV	0x4284002C	Timeout Counter Value
CANFD0_CH0_ECR	0x42840040	Error Counter Register
CANFD0_CH0_PSR	0x42840044	Protocol Status Register
CANFD0_CH0_TDCR	0x42840048	Transmitter Delay Compensation Register
CANFD0_CH0_IR	0x42840050	Interrupt Register
CANFD0_CH0_IE	0x42840054	Interrupt Enable
CANFD0_CH0_ILS	0x42840058	Interrupt Line Select
CANFD0_CH0_ILE	0x4284005C	Interrupt Line Enable
CANFD0_CH0_GFC	0x42840080	Global Filter Configuration
CANFD0_CH0_SIDFC	0x42840084	Standard ID Filter Configuration
CANFD0_CH0_XIDFC	0x42840088	Extended ID Filter Configuration
CANFD0_CH0_XIDAM	0x42840090	Extended ID AND Mask
CANFD0_CH0_HPMS	0x42840094	High Priority Message Status
CANFD0_CH0_NDAT1	0x42840098	New Data 1
CANFD0_CH0_NDAT2	0x4284009C	New Data 2
CANFD0_CH0_RXF0C	0x428400A0	Rx FIFO 0 Configuration
CANFD0_CH0_RXF0S	0x428400A4	Rx FIFO 0 Status
CANFD0_CH0_RXF0A	0x428400A8	Rx FIFO 0 Acknowledge
CANFD0_CH0_RXBC	0x428400AC	Rx Buffer Configuration
CANFD0_CH0_RXF1C	0x428400B0	Rx FIFO 1 Configuration
CANFD0_CH0_RXF1S	0x428400B4	Rx FIFO 1 Status
CANFD0_CH0_RXF1A	0x428400B8	Rx FIFO 1 Acknowledge
CANFD0_CH0_RXESC	0x428400BC	Rx Buffer / FIFO Element Size Configuration

Controller Area Network Flexible Data- Rate (CAN-FD) registers

Register name	Address	Description
CANFD0_CH0_TXBC	0x428400C0	Tx Buffer Configuration
CANFD0_CH0_TXFQS	0x428400C4	Tx FIFO/Queue Status
CANFD0_CH0_TXESC	0x428400C8	Tx Buffer Element Size Configuration
CANFD0_CH0_TXBRP	0x428400CC	Tx Buffer Request Pending
CANFD0_CH0_TXBAR	0x428400D0	Tx Buffer Add Request
CANFD0_CH0_TXBCR	0x428400D4	Tx Buffer Cancellation Request
CANFD0_CH0_TXBTO	0x428400D8	Tx Buffer Transmission Occurred
CANFD0_CH0_TXBCF	0x428400DC	Tx Buffer Cancellation Finished
CANFD0_CH0_TXBTIE	0x428400E0	Tx Buffer Transmission Interrupt Enable
CANFD0_CH0_TXBCIE	0x428400E4	Tx Buffer Cancellation Finished Interrupt Enable
CANFD0_CH0_TXEFC	0x428400F0	Tx Event FIFO Configuration
CANFD0_CH0_TXEFS	0x428400F4	Tx Event FIFO Status
CANFD0_CH0_TXEFA	0x428400F8	Tx Event FIFO Acknowledge
CANFD0_CH0_TTTMC	0x42840100	TT Trigger Memory Configuration
CANFD0_CH0_TTRMC	0x42840104	TT Reference Message Configuration
CANFD0_CH0_TTOCF	0x42840108	TT Operation Configuration
CANFD0_CH0_TTMLM	0x4284010C	TT Matrix Limits
CANFD0_CH0_TURCF	0x42840110	TUR Configuration
CANFD0_CH0_TTOCN	0x42840114	TT Operation Control
CANFD0_CH0_TTGTP	0x42840118	TT Global Time Preset
CANFD0_CH0_TTTMK	0x4284011C	TT Time Mark
CANFD0_CH0_TTIR	0x42840120	TT Interrupt Register
CANFD0_CH0_TTIE	0x42840124	TT Interrupt Enable
CANFD0_CH0_TTILS	0x42840128	TT Interrupt Line Select
CANFD0_CH0_TTOST	0x4284012C	TT Operation Status
CANFD0_CH0_TURNA	0x42840130	TUR Numerator Actual
CANFD0_CH0_TTLGT	0x42840134	TT Local & Global Time
CANFD0_CH0_TTCTC	0x42840138	TT Cycle Time & Count
CANFD0_CH0_TTCPT	0x4284013C	TT Capture Time
CANFD0_CH0_TTCSM	0x42840140	TT Cycle Sync Mark
CANFD0_CH0_RXFTOP_CTL	0x42840180	Receive FIFO Top control
CANFD0_CH0_RXFTOP0_STAT	0x428401A0	Receive FIFO 0 Top Status
CANFD0_CH0_RXFTOP0_DATA	0x428401A8	Receive FIFO 0 Top Data
CANFD0_CH0_RXFTOP1_STAT	0x428401B0	Receive FIFO 1 Top Status
CANFD0_CH0_RXFTOP1_DATA	0x428401B8	Receive FIFO 1 Top Data
CANFD0_CH1_CREL	0x42840200	Core Release Register. See CANFD0_CH0_CREL for the details of bit fields.
CANFD0_CH1_ENDN	0x42840204	Endian Register. See CANFD0_CH0_ENDN for the details of bit fields.

Controller Area Network Flexible Data- Rate (CAN-FD) registers

Register name	Address	Description
CANFD0_CH1_DBTP	0x4284020C	Data Bit Timing & Prescaler Register. See CANFD0_CH0_DBTP for the details of bit fields.
CANFD0_CH1_TEST	0x42840210	Test Register. See CANFD0_CH0_TEST for the details of bit fields.
CANFD0_CH1_RWD	0x42840214	RAM Watchdog. See CANFD0_CH0_RWD for the details of bit fields.
CANFD0_CH1_CCCR	0x42840218	CC Control Register. See CANFD0_CH0_CCCR for the details of bit fields.
CANFD0_CH1_NBTP	0x4284021C	Nominal Bit Timing & Prescaler Register. See CANFD0_CH0_NBTP for the details of bit fields.
CANFD0_CH1_TSCC	0x42840220	Timestamp Counter Configuration. See CANFD0_CH0_TSCC for the details of bit fields.
CANFD0_CH1_TSCV	0x42840224	Timestamp Counter Value. See CANFD0_CH0_TSCV for the details of bit fields.
CANFD0_CH1_TOCC	0x42840228	Timeout Counter Configuration. See CANFD0_CH0_TOCC for the details of bit fields.
CANFD0_CH1_TOCV	0x4284022C	Timeout Counter Value. See CANFD0_CH0_TOCV for the details of bit fields.
CANFD0_CH1_ECR	0x42840240	Error Counter Register. See CANFD0_CH0_ECR for the details of bit fields.
CANFD0_CH1_PSR	0x42840244	Protocol Status Register. See CANFD0_CH0_PSR for the details of bit fields.
CANFD0_CH1_TDCR	0x42840248	Transmitter Delay Compensation Register. See CANFD0_CH0_TDCR for the details of bit fields.
CANFD0_CH1_IR	0x42840250	Interrupt Register. See CANFD0_CH0_IR for the details of bit fields.
CANFD0_CH1_IE	0x42840254	Interrupt Enable. See CANFD0_CH0_IE for the details of bit fields.
CANFD0_CH1_ILS	0x42840258	Interrupt Line Select. See CANFD0_CH0_ILS for the details of bit fields.
CANFD0_CH1_ILE	0x4284025C	Interrupt Line Enable. See CANFD0_CH0_ILE for the details of bit fields.
CANFD0_CH1_GFC	0x42840280	Global Filter Configuration. See CANFD0_CH0_GFC for the details of bit fields.
CANFD0_CH1_SIDFC	0x42840284	Standard ID Filter Configuration. See CANFD0_CH0_SIDFC for the details of bit fields.
CANFD0_CH1_XIDFC	0x42840288	Extended ID Filter Configuration. See CANFD0_CH0_XIDFC for the details of bit fields.
CANFD0_CH1_XIDAM	0x42840290	Extended ID AND Mask. See CANFD0_CH0_XIDAM for the details of bit fields.
CANFD0_CH1_HPMS	0x42840294	High Priority Message Status. See CANFD0_CH0_HPMS for the details of bit fields.

Controller Area Network Flexible Data- Rate (CAN-FD) registers

Register name	Address	Description
CANFD0_CH1_NDAT1	0x42840298	New Data 1. See CANFD0_CH0_NDAT1 for the details of bit fields.
CANFD0_CH1_NDAT2	0x4284029C	New Data 2. See CANFD0_CH0_NDAT2 for the details of bit fields.
CANFD0_CH1_RXF0C	0x428402A0	Rx FIFO 0 Configuration. See CANFD0_CH0_RXF0C for the details of bit fields.
CANFD0_CH1_RXF0S	0x428402A4	Rx FIFO 0 Status. See CANFD0_CH0_RXF0S for the details of bit fields.
CANFD0_CH1_RXF0A	0x428402A8	Rx FIFO 0 Acknowledge. See CANFD0_CH0_RXF0A for the details of bit fields.
CANFD0_CH1_RXBC	0x428402AC	Rx Buffer Configuration. See CANFD0_CH0_RXBC for the details of bit fields.
CANFD0_CH1_RXF1C	0x428402B0	Rx FIFO 1 Configuration. See CANFD0_CH0_RXF1C for the details of bit fields.
CANFD0_CH1_RXF1S	0x428402B4	Rx FIFO 1 Status. See CANFD0_CH0_RXF1S for the details of bit fields.
CANFD0_CH1_RXF1A	0x428402B8	Rx FIFO 1 Acknowledge. See CANFD0_CH0_RXF1A for the details of bit fields.
CANFD0_CH1_RXESC	0x428402BC	Rx Buffer / FIFO Element Size Configuration. See CANFD0_CH0_RXESC for the details of bit fields.
CANFD0_CH1_TXBC	0x428402C0	Tx Buffer Configuration. See CANFD0_CH0_TXBC for the details of bit fields.
CANFD0_CH1_TXFQS	0x428402C4	Tx FIFO/Queue Status. See CANFD0_CH0_TXFQS for the details of bit fields.
CANFD0_CH1_TXESC	0x428402C8	Tx Buffer Element Size Configuration. See CANFD0_CH0_TXESC for the details of bit fields.
CANFD0_CH1_TXBRP	0x428402CC	Tx Buffer Request Pending. See CANFD0_CH0_TXBRP for the details of bit fields.
CANFD0_CH1_TXBAR	0x428402D0	Tx Buffer Add Request. See CANFD0_CH0_TXBAR for the details of bit fields.
CANFD0_CH1_TXBCR	0x428402D4	Tx Buffer Cancellation Request. See CANFD0_CH0_TXBCR for the details of bit fields.
CANFD0_CH1_TXBTO	0x428402D8	Tx Buffer Transmission Occurred. See CANFD0_CH0_TXBTO for the details of bit fields.
CANFD0_CH1_TXBCF	0x428402DC	Tx Buffer Cancellation Finished. See CANFD0_CH0_TXBCF for the details of bit fields.
CANFD0_CH1_TXBTIE	0x428402E0	Tx Buffer Transmission Interrupt Enable. See CANFD0_CH0_TXBTIE for the details of bit fields.
CANFD0_CH1_TXBCIE	0x428402E4	Tx Buffer Cancellation Finished Interrupt Enable. See CANFD0_CH0_TXBCIE for the details of bit fields.
CANFD0_CH1_TXEFC	0x428402F0	Tx Event FIFO Configuration. See CANFD0_CH0_TXEFC for the details of bit fields.

Controller Area Network Flexible Data- Rate (CAN-FD) registers

Register name	Address	Description
CANFD0_CH1_TXEFS	0x428402F4	Tx Event FIFO Status. See CANFD0_CH0_TXEFS for the details of bit fields.
CANFD0_CH1_TXEFA	0x428402F8	Tx Event FIFO Acknowledge. See CANFD0_CH0_TXEFA for the details of bit fields.
CANFD0_CH1_TTTMC	0x42840300	TT Trigger Memory Configuration. See CANFD0_CH0_TTTMC for the details of bit fields.
CANFD0_CH1_TTRMC	0x42840304	TT Reference Message Configuration. See CANFD0_CH0_TTRMC for the details of bit fields.
CANFD0_CH1_TTOCF	0x42840308	TT Operation Configuration. See CANFD0_CH0_TTOCF for the details of bit fields.
CANFD0_CH1_TTMLM	0x4284030C	TT Matrix Limits. See CANFD0_CH0_TTMLM for the details of bit fields.
CANFD0_CH1_TURCF	0x42840310	TUR Configuration. See CANFD0_CH0_TURCF for the details of bit fields.
CANFD0_CH1_TTOCN	0x42840314	TT Operation Control. See CANFD0_CH0_TTOCN for the details of bit fields.
CANFD0_CH1_TTGTP	0x42840318	TT Global Time Preset. See CANFD0_CH0_TTGTP for the details of bit fields.
CANFD0_CH1_TTTMK	0x4284031C	TT Time Mark. See CANFD0_CH0_TTTMK for the details of bit fields.
CANFD0_CH1_TTIR	0x42840320	TT Interrupt Register. See CANFD0_CH0_TTIR for the details of bit fields.
CANFD0_CH1_TTIE	0x42840324	TT Interrupt Enable. See CANFD0_CH0_TTIE for the details of bit fields.
CANFD0_CH1_TTILS	0x42840328	TT Interrupt Line Select. See CANFD0_CH0_TTILS for the details of bit fields.
CANFD0_CH1_TTOST	0x4284032C	TT Operation Status. See CANFD0_CH0_TTOST for the details of bit fields.
CANFD0_CH1_TURNA	0x42840330	TUR Numerator Actual. See CANFD0_CH0_TURNA for the details of bit fields.
CANFD0_CH1_TTLGT	0x42840334	TT Local & Global Time. See CANFD0_CH0_TTLGT for the details of bit fields.
CANFD0_CH1_TTCTC	0x42840338	TT Cycle Time & Count. See CANFD0_CH0_TTCTC for the details of bit fields.
CANFD0_CH1_TTCPT	0x4284033C	TT Capture Time. See CANFD0_CH0_TTCPT for the details of bit fields.
CANFD0_CH1_TTCSM	0x42840340	TT Cycle Sync Mark. See CANFD0_CH0_TTCSM for the details of bit fields.
CANFD0_CH1_RXFTOP_CTL	0x42840380	Receive FIFO Top control. See CANFD0_CH0_RXFTOP_CTL for the details of bit fields.
CANFD0_CH1_RXFTOP0_STAT	0x428403A0	Receive FIFO 0 Top Status. See CANFD0_CH0_RXFTOP0_STAT for the details of bit fields.

Controller Area Network Flexible Data- Rate (CAN-FD) registers

Register name	Address	Description
CANFD0_CH1_RXFTOP0_DATA	0x428403A8	Receive FIFO 0 Top Data. See CANFD0_CH0_RXFTOP0_DATA for the details of bit fields.
CANFD0_CH1_RXFTOP1_STAT	0x428403B0	Receive FIFO 1 Top Status. See CANFD0_CH0_RXFTOP1_STAT for the details of bit fields.
CANFD0_CH1_RXFTOP1_DATA	0x428403B8	Receive FIFO 1 Top Data. See CANFD0_CH0_RXFTOP1_DATA for the details of bit fields.
CANFD0_CTL	0x42841000	Global CAN control register
CANFD0_STATUS	0x42841004	Global CAN status register
CANFD0_INTR0_CAUSE	0x42841010	Consolidated interrupt0 cause register
CANFD0_INTR1_CAUSE	0x42841014	Consolidated interrupt1 cause register
CANFD0_TS_CTL	0x42841020	Time Stamp control register
CANFD0_TS_CNT	0x42841024	Time Stamp counter value

26.1.1 CANFD0_CH0_CREL

Description: Core Release Register

Address: 0x42840000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	DAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	R				R			
Name	SUBSTEP [23:20]				YEAR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	R				R			
Name	REL [31:28]				STEP [27:24]			

Bits	Name	Description
31 : 28	REL	Core Release One digit, BCD-coded. Default Value: 0x3
27 : 24	STEP	Step of Core Release One digit, BCD-coded. Default Value: 0x2
23 : 20	SUBSTEP	Sub-step of Core Release One digit, BCD-coded. Default Value: 0x3
19 : 16	YEAR	Time Stamp Year One digit, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0x8
15 : 8	MON	Time Stamp Month Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0x06
7 : 0	DAY	Time Stamp Day Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0x09

26.1.2 CANFD0_CH0_ENDN

Description: Endian Register

Address: 0x42840004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	ETV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ETV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ETV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ETV [31:24]							

Bits	Name	Description
31 : 0	ETV	Endianness Test Value The endianness test value is 0x87654321. Default Value: 0x87654321

26.1.3 CANFD0_CH0_DBTP

Description: Data Bit Timing & Prescaler Register

Address: 0x4284000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DTSEG2 [7:4]				DSJW [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			DTSEG1 [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW	Reserved		RW				
HW Access	R	Reserved		R				
Name	TDC	Reserved [22:21]		DBRP [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23	TDC	Transmitter Delay Compensation 0= Transmitter Delay Compensation disabled 1= Transmitter Delay Compensation enabled Default Value: 0
20 : 16	DBRP	Data Bit Rate Prescaler 0x00-0x1F The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
12 : 8	DTSEG1	Data time segment before sample point 0x00-0x1F Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 0xA
7 : 4	DTSEG2	Data time segment after sample point 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 3
3 : 0	DSJW	Data (Re)Synchronization Jump Width 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 3

26.1.4 CANFD0_CH0_TEST

Description: Test Register

Address: 0x42840010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	RX	TX [6:5]		LBCK	CAT	CAM	TAT	TAM

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	RX	Receive Pin Monitors the actual value of pin m_ttcan_rx 0= The CAN bus is dominant (m_ttcan_rx = '0') 1= The CAN bus is recessive (m_ttcan_rx = '1') Default Value: Undefined
6 : 5	TX	Control of Transmit Pin 00 Reset value, m_ttcan_tx controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at pin m_ttcan_tx 10 Dominant ('0') level at pin m_ttcan_tx 11 Recessive ('1') at pin m_ttcan_tx Default Value: 0
4	LBCK	Loop Back Mode 0= Reset value, Loop Back Mode is disabled 1= Loop Back Mode is enabled (see Section 3.1.9, Test Modes) Default Value: 0
3	CAT	ASC is not supported by M_TTCAN Check ASC Transmit Control Monitors level at output pin m_ttcan_asct. 0= Output pin m_ttcan_asct = '0' Default Value: 0
2	CAM	ASC is not supported by M_TTCAN Check ASC Multiplexer Control Monitors level at output pin m_ttcan_ascm. 0= Output pin m_ttcan_ascm = '0' 1= Output pin m_ttcan_ascm = '1' Default Value: 0

26.1.4 CANFD0_CH0_TEST (continued)

1	TAT	ASC is not supported by M_TTCAN Test ASC Transmit Control Controls output pin m_ttcan_asct in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcan_asct controlled by FSE 1= Level at pin m_ttcan_asct = '1' Default Value: 0
0	TAM	ASC is not supported by M_TTCAN Test ASC Multiplexer Control Controls output pin m_ttcan_ascm in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcan_ascm controlled by FSE 1= Level at pin m_ttcan_ascm = '1' Default Value: 0

26.1.5 CANFD0_CH0_RWD

Description: RAM Watchdog

Address: 0x42840014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	WDV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	WDV	Watchdog Value Actual Message RAM Watchdog Counter Value. Default Value: 0
7 : 0	WDC	Watchdog Configuration Start value of the Message RAM Watchdog Counter. With the reset value of '00' the counter is disabled. Default Value: 0

26.1.6 CANFD0_CH0_CCCR

Description: CC Control Register

Address: 0x42840018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST	DAR	MON_	CSR	CSA	ASM	CCE	INIT

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	Reserved		RW	RW
HW Access	R	R	R	R	Reserved		R	R
Name	NISO	TXP	EFBI	PXHD	Reserved [11:10]		BRSE	FDOE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	NISO	Non ISO Operation If this bit is set, the M_TTCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0= CAN FD frame format according to ISO 11898-1:2015 1= CAN FD frame format according to Bosch CAN FD Specification V1.0 addressing the non-ISO CAN FD Default Value: 0
14	TXP	Transmit Pause If this bit is set, the M_TTCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame (see Section 3.5). 0= Transmit pause disabled 1= Transmit pause enabled Default Value: 0
13	EFBI	Edge Filtering during Bus Integration 0= Edge filtering disabled 1= Two consecutive dominant tq required to detect an edge for hard synchronization Default Value: 0
12	PXHD	Protocol Exception Handling Disable 0= Protocol exception handling enabled 1= Protocol exception handling disabled Default Value: 0
9	BRSE	Bit Rate Switch Enable 0= Bit rate switching for transmissions disabled 1= Bit rate switching for transmissions enabled Default Value: 0

26.1.6 CANFD0_CH0_CCCR (continued)

8	FDOE	FD Operation Enable 0= FD operation disabled 1= FD operation enabled Default Value: 0
7	TEST	Test Mode Enable 0= Normal operation, register TEST holds reset values 1= Test Mode, write access to register TEST enabled Default Value: 0
6	DAR	Disable Automatic Retransmission 0= Automatic retransmission of messages not transmitted successfully enabled 1= Automatic retransmission disabled Default Value: 0
5	MON_	Bus Monitoring Mode Bit MON can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. 0= Bus Monitoring Mode is disabled 1= Bus Monitoring Mode is enabled Default Value: 0
4	CSR	Clock Stop Request, not supported by M_TTCAN use CTL.STOP_REQ at the group level instead. 0= No clock stop is requested 1= Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle. Default Value: 0
3	CSA	Clock Stop Acknowledge 0= No clock stop acknowledged 1= M_TTCAN may be set in power down by stopping m_ttcan_hclk and m_ttcan_cclk Default Value: 0
2	ASM	Restricted Operation Mode Bit ASM can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. For a description of the Restricted Operation Mode see Section 3.1.5. 0= Normal CAN operation 1= Restricted Operation Mode active Default Value: 0
1	CCE	Configuration Change Enable 0= The CPU has no write access to the protected configuration registers 1= The CPU has write access to the protected configuration registers (while CCCR.INIT = '1') Default Value: 0
0	INIT	Initialization 0= Normal Operation 1= Initialization is started Default Value: 1

26.1.7 CANFD0_CH0_NBTP

Description: Nominal Bit Timing & Prescaler Register

Address: 0x4284001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	NTSEG2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NTSEG1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NBRP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							RW
HW Access	R							R
Name	NSJW [31:25]							NBRP

Bits	Name	Description
31 : 25	NSJW	Nominal (Re)Synchronization Jump Width 0x00-0x7F Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 3
24 : 16	NBRP	Nominal Bit Rate Prescaler 0x000-0x1FFThe value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
15 : 8	NTSEG1	Nominal Time segment before sample point 0x01-0xFF Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 0xA
6 : 0	NTSEG2	Nominal Time segment after sample point 0x01-0x7F Valid values are 1 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 3

26.1.8 CANFD0_CH0_TSCC

Description: Timestamp Counter Configuration

Address: 0x42840020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						TSS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				TCP [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 16	TCP	Timestamp Counter Prescaler (still used for TOCC) 0x0-0xF Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
1 : 0	TSS	Timestamp Select, should always be set to external timestamp counter 00= Timestamp counter value always 0x0000 01= Timestamp counter value incremented according to TCP 10= External timestamp counter value used 11= Same as '00' Default Value: 0

26.1.9 CANFD0_CH0_TSCV

Description: Timestamp Counter Value

Address: 0x42840024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TSC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TSC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	TSC	Timestamp Counter, not used for M_TTCAN The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = '01', the Timestamp Counter is incremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = '10', TSC reflects the external Timestamp Counter value. A write access has no impact. Default Value: 0

26.1.10 CANFD0_CH0_TOCC

Description: Timeout Counter Configuration

Address: 0x42840028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		RW
HW Access	Reserved					R		R
Name	Reserved [7:3]					TOS [2:1]		ETOC

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TOP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TOP [31:24]							

Bits	Name	Description
31 : 16	TOP	Timeout Period Start value of the Timeout Counter (down-counter). Configures the Timeout Period. Default Value: 0xFFFF
2 : 1	TOS	Timeout Select When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00= Continuous operation 01= Timeout controlled by Tx Event FIFO 10= Timeout controlled by Rx FIFO 0 11= Timeout controlled by Rx FIFO 1 Default Value: 0
0	ETOC	Enable Timeout Counter 0= Timeout Counter disabled 1= Timeout Counter enabled Default Value: 0

26.1.11 CANFD0_CH0_TOCV

Description: Timeout Counter Value

Address: 0x4284002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TOC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TOC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	TOC	Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS. Default Value: 0xFFFF

26.1.12 CANFD0_CH0_ECR

Description: Error Counter Register

Address: 0x42840040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	RW	RW						
Name	RP	REC [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW1C							
Name	CEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	CEL	CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO. Default Value: 0
15	RP	Receive Error Passive 0= The Receive Error Counter is below the error passive level of 128 1= The Receive Error Counter has reached the error passive level of 128 Default Value: 0
14 : 8	REC	Receive Error Counter Actual state of the Receive Error Counter, values between 0 and 127 Default Value: 0
7 : 0	TEC	Transmit Error Counter Actual state of the Transmit Error Counter, values between 0 and 255 Default Value: 0

26.1.13 CANFD0_CH0_PSR

Description: Protocol Status Register

Address: 0x42840044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R		R		
HW Access	RW	RW	RW	RW		RW1S		
Name	BO	EW	EP	ACT [4:3]		LEC [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	R	R	R	R	R		
HW Access	Reserved	RW1C	RW1C	RW1C	RW1C	RW1S		
Name	Reserved	PXE	RFDF	RBRS	RESI	DLEC [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	R						
HW Access	Reserved	RW						
Name	Reserved	TDCV [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
22 : 16	TDCV	Transmitter Delay Compensation Value 0x00-0x7F Position of the secondary sample point, defined by the sum of the measured delay from m_can_tx to m_can_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq. Default Value: 0
14	PXE	Protocol Exception Event , Reset on Read 0= No protocol exception event occurred since last read access 1= Protocol exception event occurred Default Value: 0
13	RFDF	Received a CAN FD Message , Reset on Read This bit is set independent of acceptance filtering. 0= Since this bit was reset by the CPU, no CAN FD message has been received 1= Message in CAN FD format with FDF flag set has been received Default Value: 0
12	RBRS	BRS flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its BRS flag set 1= Last received CAN FD message had its BRS flag set Default Value: 0

26.1.13 CANFD0_CH0_PSR (continued)

11	RESI	ESI flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its ESI flag set 1= Last received CAN FD message had its ESI flag set Default Value: 0
10 : 8	DLEC	Data Phase Last Error Code , Set on Read Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error. Default Value: 7
7	BO	Bus_Off Status 0= The M_CAN is not Bus_Off 1= The M_CAN is in Bus_Off state Default Value: 0
6	EW	Warning Status 0= Both error counters are below the Error_Warning limit of 96 1= At least one of error counter has reached the Error_Warning limit of 96 Default Value: 0
5	EP	Error Passive 0= The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1= The M_CAN is in the Error_Passive state Default Value: 0
4 : 3	ACT	Activity Monitors the module's CAN communication state. 00= Synchronizing - node is synchronizing on CAN communication 01= Idle - node is neither receiver nor transmitter 10= Receiver - node is operating as receiver 11= Transmitter - node is operating as transmitter Default Value: 0
2 : 0	LEC	Last Error Code, Set on Read0 The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error. 0= No Error: No error occurred since LEC has been reset by successful reception or transmission. 1= Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2= Form Error: A fixed format part of a received frame has the wrong format. 3= AckError: The message transmitted by the M_TTCAN was not acknowledged by another node. 4= Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant. 5= Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6= CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7= NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register. Default Value: 7

26.1.14 CANFD0_CH0_TDCR

Description: Transmitter Delay Compensation Register

Address: 0x42840048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	TDCF [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	TDCO [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14 : 8	TDCO	Transmitter Delay Compensation Offset 0x00-0x7F Offset value defining the distance between the measured delay from m_ttcan_tx to m_ttcan_rx and the secondary sample point. Valid values are 0 to 127 mtq. Default Value: 0
6 : 0	TDCF	Transmitter Delay Compensation Filter Window Length 0x00-0x7F Defines the minimum value for the SSP position, dominant edges on m_ttcan_rx that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq Default Value: 0

26.1.15 CANFD0_CH0_IR

Description: Interrupt Register

Address: 0x42840050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RF1L_	RF1F	RF1W	RF1N	RF0L_	RF0F	RF0W	RF0N

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TEFL_	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP_	ELO	BEU	BEC	DRX	TOO	MRAF	TSW

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	Reserved		RW	RW	RW	RW	RW	RW
Name	Reserved [31:30]		ARA	PED	PEA	WDI	BO_	EW_

Bits	Name	Description
29	ARA	Access to Reserved Address 0= No access to reserved address occurred 1= Access to reserved address occurred Default Value: 0
28	PED	Protocol Error in Data Phase (Data Bit Time is used) 0= No protocol error in data phase 1= Protocol error in data phase detected (PSR.DLEC != 0,7) Default Value: 0
27	PEA	Protocol Error in Arbitration Phase (Nominal Bit Time is used) 0= No protocol error in arbitration phase 1= Protocol error in arbitration phase detected (PSR.LEC != 0,7) Default Value: 0
26	WDI	Watchdog Interrupt 0= No Message RAM Watchdog event occurred 1= Message RAM Watchdog event due to missing READY Default Value: 0
25	BO_	Bus_Off Status 0= Bus_Off status unchanged 1= Bus_Off status changed Default Value: 0
24	EW_	Warning Status 0= Error_Warning status unchanged 1= Error_Warning status changed Default Value: 0

26.1.15 CANFD0_CH0_IR (continued)

23	EP_	Error Passive 0= Error_Passive status unchanged 1= Error_Passive status changed Default Value: 0
22	ELO	Error Logging Overflow 0= CAN Error Logging Counter did not overflow 1= Overflow of CAN Error Logging Counter occurred Default Value: 0
21	BEU	Bit Error Uncorrected Message RAM bit error detected, uncorrected. The flag is set in the folloiwng cases. - M_TTCAN detects uncorrectable ECC error from Message RAM when ECC is enabled and ECC error injection is disabled. - M_TTCAN reads from an out of range Message RAM address. Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data. 0= No bit error detected when reading from Message RAM 1= Bit error detected, uncorrected Default Value: 0
20	BEC	Bit Error Corrected This bit always reads as 0. Default Value: 0
19	DRX	Message stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0= No Rx Buffer updated 1= At least one received message stored into a Rx Buffer Default Value: 0
18	TOO	Timeout Occurred 0= No timeout 1= Timeout reached Default Value: 0
17	MRAF	Message RAM Access Failure The flag is set, when the Rx Handler - has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. - was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_TTCAN is switched into Restricted Operation Mode (see Section 3.1.5). To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0= No Message RAM access failure occurred 1= Message RAM access failure occurred Default Value: 0
16	TSW	Timestamp Wraparound 0= No timestamp counter wrap-around 1= Timestamp counter wrapped around Default Value: 0
15	TEFL_	Tx Event FIFO Element Lost 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero Default Value: 0
14	TEFF	Tx Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full Default Value: 0

26.1.15 CANFD0_CH0_IR (continued)

13	TEFW	Tx Event FIFO Watermark Reached 0= Tx Event FIFO fill level below watermark 1= Tx Event FIFO fill level reached watermark Default Value: 0
12	TEFN	Tx Event FIFO New Entry 0= Tx Event FIFO unchanged 1= Tx Handler wrote Tx Event FIFO element Default Value: 0
11	TFE	Tx FIFO Empty 0= Tx FIFO non-empty 1= Tx FIFO empty Default Value: 0
10	TCF	Transmission Cancellation Finished 0= No transmission cancellation finished 1= Transmission cancellation finished Default Value: 0
9	TC	Transmission Completed 0= No transmission completed 1= Transmission completed Default Value: 0
8	HPM	High Priority Message 0= No high priority message received 1= High priority message received Default Value: 0
7	RF1L_	Rx FIFO 1 Message Lost 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Default Value: 0
6	RF1F	Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full Default Value: 0
5	RF1W	Rx FIFO 1 Watermark Reached 0= Rx FIFO 1 fill level below watermark 1= Rx FIFO 1 fill level reached watermark Default Value: 0
4	RF1N	Rx FIFO 1 New Message 0= No new message written to Rx FIFO 1 1= New message written to Rx FIFO 1 Default Value: 0
3	RF0L_	Rx FIFO 0 Message Lost 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Default Value: 0
2	RF0F	Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full Default Value: 0
1	RF0W	Rx FIFO 0 Watermark Reached 0= Rx FIFO 0 fill level below watermark 1= Rx FIFO 0 fill level reached watermark Default Value: 0
0	RF0N	Rx FIFO 0 New Message 0= No new message written to Rx FIFO 0 1= New message written to Rx FIFO 0 Default Value: 0

26.1.16 CANFD0_CH0_IE

Description: Interrupt Enable

Address: 0x42840054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [31:30]		ARAE	PEDE	PEAE	WDIE	BOE	EWE

Bits	Name	Description
29	ARAE	Access to Reserved Address Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
28	PEDE	Protocol Error in Data Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
27	PEAE	Protocol Error in Arbitration Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
26	WDIE	Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
25	BOE	Bus_Off Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
24	EWE	Warning Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

26.1.16 CANFD0_CH0_IE (continued)

23	EPE	Error Passive Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
22	ELOE	Error Logging Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
21	BEUE	Bit Error Uncorrected Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
20	BECE	Bit Error Corrected Interrupt Enable (not used in M_TTCAN) 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
19	DRXE	Message stored to Dedicated Rx Buffer Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
18	TOOE	Timeout Occurred Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
17	MRAFE	Message RAM Access Failure Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
16	TSWE	Timestamp Wraparound Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
15	TEFLE	Tx Event FIFO Event Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
14	TEFFE	Tx Event FIFO Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
13	TEFWE	Tx Event FIFO Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
12	TEFNE	Tx Event FIDO New Entry Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
11	TFEE	Tx FIFO Empty Interrupt Enable 0= Interrupt Disabled 1= Interrupt EnabledTx FIFO Empty Interrupt Enable Default Value: 0
10	TCFE	Transmission Cancellation Finished Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

26.1.16 CANFD0_CH0_IE (continued)

9	TCE	Transmission Completed Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
8	HPME	High Priority Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
7	RF1LE	Rx FIFO 1 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
6	RF1FE	Rx FIFO 1 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
5	RF1WE	Rx FIFO 1 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
4	RF1NE	Rx FIFO 1 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
3	RF0LE	Rx FIFO 0 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
2	RF0FE	Rx FIFO 0 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
1	RF0WE	Rx FIFO 0 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
0	RF0NE	Rx FIFO 0 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

26.1.17 CANFD0_CH0_ILS

Description: Interrupt Line Select

Address: 0x42840058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW	RW	RW	RW	RW	RW
HW Access	Reserved		R	R	R	R	R	R
Name	Reserved [31:30]		ARAL	PEDL	PEAL	WDIL	BOL	EWL

Bits	Name	Description
29	ARAL	Access to Reserved Address Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
28	PEDL	Protocol Error in Data Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
27	PEAL	Protocol Error in Arbitration Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
26	WDIL	Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
25	BOL	Bus_Off Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
24	EWL	Warning Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

26.1.17 CANFD0_CH0_ILS (continued)

23	EPL	Error Passive Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
22	ELOL	Error Logging Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
21	BEUL	Bit Error Uncorrected Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
20	BECL	Bit Error Corrected Interrupt Select (not used in M_TTCAN) 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
19	DRXL	Message stored to Dedicated Rx Buffer Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
18	TOOL	Timeout Occurred Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
17	MRAFL	Message RAM Access Failure Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
16	TSWL	Timestamp Wraparound Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
15	TEFLL	Tx Event FIFO Event Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
14	TEFFL	Tx Event FIFO Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
13	TEFWL	Tx Event FIFO Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
12	TEFNL	Tx Event FIFO New Entry Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
11	TFEL	Tx FIFO Empty Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
10	TCFL	Transmission Cancellation Finished Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

26.1.17 CANFD0_CH0_ILS (continued)

9	TCL	Transmission Completed Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
8	HPML	High Priority Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
7	RF1LL	Rx FIFO 1 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
6	RF1FL	Rx FIFO 1 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
5	RF1WL	Rx FIFO 1 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
4	RF1NL	Rx FIFO 1 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
3	RF0LL	Rx FIFO 0 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
2	RF0FL	Rx FIFO 0 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
1	RF0WL	Rx FIFO 0 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
0	RF0NL	Rx FIFO 0 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

26.1.18 CANFD0_CH0_ILE

Description: Interrupt Line Enable

Address: 0x4284005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						EINT1	EINT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	EINT1	Enable Interrupt Line 1 0= Interrupt line m_ttcan_int1 disabled 1= Interrupt line m_ttcan_int1 enabled Default Value: 0
0	EINT0	Enable Interrupt Line 0 0= Interrupt line m_ttcan_int0 disabled 1= Interrupt line m_ttcan_int0 enabled Default Value: 0

26.1.19 CANFD0_CH0_GFC

Description: Global Filter Configuration

Address: 0x42840080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW		RW		RW	RW
HW Access	Reserved		R		R		R	R
Name	Reserved [7:6]		ANFS [5:4]		ANFE [3:2]		RRFS	RRFE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 4	ANFS	Accept Non-matching Frames Standard Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject Default Value: 0
3 : 2	ANFE	Accept Non-matching Frames Extended Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject Default Value: 0
1	RRFS	Reject Remote Frames Standard 0= Filter remote frames with 11-bit standard IDs 1= Reject all remote frames with 11-bit standard IDs Default Value: 0
0	RRFE	Reject Remote Frames Extended 0= Filter remote frames with 29-bit extended IDs 1= Reject all remote frames with 29-bit extended IDs Default Value: 0

26.1.20 CANFD0_CH0_SIDFC

Description: Standard ID Filter Configuration

Address: 0x42840084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	
HW Access	R						Reserved	
Name	FLSSA [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLSSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LSS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	LSS	List Size Standard 0= No standard Message ID filter 1-128= Number of standard Message ID filter elements 128= Values greater than 128 are interpreted as 128 Default Value: 0
15 : 2	FLSSA	Filter List Standard Start Address Start address of standard Message ID filter list (32-bit word address, see Figure 2). Default Value: 0

26.1.21 CANFD0_CH0_XIDFC

Description: Extended ID Filter Configuration

Address: 0x42840088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	
HW Access	R						Reserved	
Name	FLESA [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLESA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	LSE [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
22 : 16	LSE	List Size Extended 0= No extended Message ID filter 1-64= Number of extended Message ID filter elements 64= Values greater than 64 are interpreted as 64 Default Value: 0
15 : 2	FLESA	Filter List Extended Start Address Start address of extended Message ID filter list (32-bit word address, see Figure 2). Default Value: 0

26.1.22 CANFD0_CH0_XIDAM

Description: Extended ID AND Mask

Address: 0x42840090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	EIDM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	EIDM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	EIDM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [31:29]			EIDM [28:24]				

Bits	Name	Description
28 : 0	EIDM	Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. Default Value: 0x1FFFFFFF

26.1.23 CANFD0_CH0_HPMS

Description: High Priority Message Status

Address: 0x42840094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R					
HW Access	RW		RW					
Name	MSI [7:6]		BIDX [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	RW	RW						
Name	FLST	FIDX [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	FLST	Filter List Indicates the filter list of the matching filter element. 0= Standard Filter List 1= Extended Filter List Default Value: 0
14 : 8	FIDX	Filter Index Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1. Default Value: 0
7 : 6	MSI	Message Storage Indicator 00= No FIFO selected 01= FIFO message lost 10= Message stored in FIFO 0 11= Message stored in FIFO 1 Default Value: 0
5 : 0	BIDX	Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = '1'. Default Value: 0

26.1.24 CANFD0_CH0_NDAT1

Description: New Data 1

Address: 0x42840098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	ND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	ND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	ND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	ND [31:24]							

Bits	Name	Description
31 : 0	ND	New Data The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message Default Value: 0

26.1.25 CANFD0_CH0_NDAT2

Description: New Data 2

Address: 0x4284009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	ND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	ND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	ND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	ND [31:24]							

Bits	Name	Description
31 : 0	ND	New Data The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message Default Value: 0

26.1.26 CANFD0_CH0_RXF0C

Description: Rx FIFO 0 Configuration

Address: 0x428400A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	
HW Access	R						Reserved	
Name	F0SA [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	F0SA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	F0S [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						
HW Access	R	R						
Name	F0OM	F0WM [30:24]						

Bits	Name	Description
31	F0OM	FIFO 0 Operation Mode FIFO 0 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 0 blocking mode 1= FIFO 0 overwrite mode Default Value: 0
30 : 24	F0WM	Rx FIFO 0 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 0 watermark interrupt (IR.RF0W) 64= Watermark interrupt disabled Default Value: 0
22 : 16	F0S	Rx FIFO 0 Size 0= No Rx FIFO 0 1-64= Number of Rx FIFO 0 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to F0S-1 Default Value: 0
15 : 2	F0SA	Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM (32-bit word address, see Figure 2). Default Value: 0

26.1.27 CANFD0_CH0_RXF0S

Description: Rx FIFO 0 Status

Address: 0x428400A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R						
HW Access	Reserved	RW						
Name	Reserved	F0FL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [15:14]		F0GI [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [23:22]		F0PI [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						R	R
HW Access	Reserved						RW	RW
Name	Reserved [31:26]						RF0L	F0F

Bits	Name	Description
25	RF0L	Rx FIFO 0 Message Lost This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Default Value: 0
24	F0F	Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full Default Value: 0
21 : 16	F0PI	Rx FIFO 0 Put Index Rx FIFO 0 write index pointer, range 0 to 63. Default Value: 0
13 : 8	F0GI	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RXF0A.F0AI. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected. Default Value: 0
6 : 0	F0FL	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected. Default Value: 0

26.1.28 CANFD0_CH0_RXF0A

Description: Rx FIFO 0 Acknowledge

Address: 0x428400A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		A					
Name	Reserved [7:6]		F0AI [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	F0AI	Rx FIFO 0 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL. Default Value: 0

26.1.29 CANFD0_CH0_RXBC

Description: Rx Buffer Configuration

Address: 0x428400AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	
HW Access	R						Reserved	
Name	RBSA [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RBSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 2	RBSA	Rx Buffer Start Address Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address). Also used to reference debug messages A,B,C. Default Value: 0

26.1.30 CANFD0_CH0_RXF1C

Description: Rx FIFO 1 Configuration

Address: 0x428400B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	
HW Access	R						Reserved	
Name	F1SA [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	F1SA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	F1S [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						
HW Access	R	R						
Name	F1OM	F1WM [30:24]						

Bits	Name	Description
31	F1OM	FIFO 1 Operation Mode FIFO 1 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 1 blocking mode 1= FIFO 1 overwrite mode Default Value: 0
30 : 24	F1WM	Rx FIFO 1 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 1 watermark interrupt (IR.RF1W) 64= Watermark interrupt disabled Default Value: 0
22 : 16	F1S	Rx FIFO 1 Size 0= No Rx FIFO 1 1-64= Number of Rx FIFO 1 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to F1S - 1 Default Value: 0
15 : 2	F1SA	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see Figure 2). Default Value: 0

26.1.31 CANFD0_CH0_RXF1S

Description: Rx FIFO 1 Status

Address: 0x428400B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	R						
HW Access	Reserved	RW						
Name	Reserved	F1FL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [15:14]		F1GI [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [23:22]		F1PI [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R		Reserved				R	R
HW Access	RW		Reserved				RW	RW
Name	DMS [31:30]		Reserved [29:26]				RF1L	F1F

Bits	Name	Description
31 : 30	DMS	Debug Message Status 00= Idle state, wait for reception of debug messages, DMA request is cleared 01= Debug message A received 10= Debug messages A, B received 11= Debug messages A, B, C received, DMA request is set Default Value: 0
25	RF1L	Rx FIFO 1 Message Lost This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Default Value: 0
24	F1F	Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full Default Value: 0
21 : 16	F1PI	Rx FIFO 1 Put Index Rx FIFO 1 write index pointer, range 0 to 63. Default Value: 0
13 : 8	F1GI	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RXF1A.F1AI. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected. Default Value: 0

26.1.31 CANFD0_CH0_RXF1S (continued)

6 : 0	F1FL	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected. Default Value: 0

26.1.32 CANFD0_CH0_RXF1A

Description: Rx FIFO 1 Acknowledge

Address: 0x428400B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		A					
Name	Reserved [7:6]		F1AI [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	F1AI	Rx FIFO 1 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL. Default Value: 0

26.1.33 CANFD0_CH0_RXESC

Description: Rx Buffer / FIFO Element Size Configuration

Address: 0x428400BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW			Reserved	RW		
HW Access	Reserved	R			Reserved	R		
Name	Reserved	F1DS [6:4]			Reserved	F0DS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [15:11]					RBDS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10 : 8	RBDS	Rx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0
6 : 4	F1DS	Rx FIFO 1 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

26.1.33 CANFD0_CH0_RXESC (continued)

2 : 0	F0DS	Rx FIFO 0 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

26.1.34 CANFD0_CH0_TXBC

Description: Tx Buffer Configuration

Address: 0x428400C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	
HW Access	R						Reserved	
Name	TBSA [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TBSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [23:22]		NDTB [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW	RW					
HW Access	Reserved	R	R					
Name	Reserved	TFQM	TFQS [29:24]					

Bits	Name	Description
30	TFQM	Tx FIFO/Queue Mode 0= Tx FIFO operation 1= Tx Queue operation Default Value: 0
29 : 24	TFQS	Transmit FIFO/Queue Size 0= No Tx FIFO/Queue 1-32= Number of Tx Buffers used for Tx FIFO/Queue 32= Values greater than 32 are interpreted as 32 Default Value: 0
21 : 16	NDTB	Number of Dedicated Transmit Buffers 0= No Dedicated Tx Buffers 1-32= Number of Dedicated Tx Buffers 32= Values greater than 32 are interpreted as 32 Default Value: 0
15 : 2	TBSA	Tx Buffers Start Address Start address of Tx Buffers section in Message RAM (32-bit word address, see Figure 2). Default Value: 0

26.1.35 CANFD0_CH0_TXFQS

Description: Tx FIFO/Queue Status

Address: 0x428400C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [7:6]		TFFL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R				
HW Access	Reserved			RW				
Name	Reserved [15:13]			TFGI [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R	R				
HW Access	Reserved		RW	RW				
Name	Reserved [23:22]		TFQF	TFQPI [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21	TFQF	Tx FIFO/Queue Full 0= Tx FIFO/Queue not full 1= Tx FIFO/Queue full Default Value: 0
20 : 16	TFQPI	Tx FIFO/Queue Put Index Tx FIFO/Queue write index pointer, range 0 to 31. Default Value: 0
12 : 8	TFGI	Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured TXBC.TFQM = '1'). Default Value: 0
5 : 0	TFFL	Tx FIFO Free Level Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1') Default Value: 0

26.1.36 CANFD0_CH0_TXESC

Description: Tx Buffer Element Size Configuration

Address: 0x428400C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:3]						TBDS [2:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	TBDS	Tx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

26.1.37 CANFD0_CH0_TXBRP

Description: Tx Buffer Request Pending

Address: 0x428400CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TRP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TRP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TRP [31:24]							

Bits	Name	Description
31 : 0	TRP	Transmission Request Pending Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TX-BAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan (see Section 3.5, Tx Handling) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signaled via TXBCF after successful transmission together with the corresponding TXBTO bit when the transmission has not yet been started at the point of cancellation when the transmission has been aborted due to lost arbitration when an error occurred during frame transmission In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0= No transmission request pending 1= Transmission request pending Default Value: 0

26.1.38 CANFD0_CH0_TXBAR

Description: Tx Buffer Add Request

Address: 0x428400D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	AR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	AR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	AR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	AR [31:24]							

Bits	Name	Description
31 : 0	AR	Add Request Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0= No transmission request added 1= Transmission requested added Default Value: 0

26.1.39 CANFD0_CH0_TXBCR

Description: Tx Buffer Cancellation Request

Address: 0x428400D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CR [31:24]							

Bits	Name	Description
31 : 0	CR	Cancellation Request Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0= No cancellation pending 1= Cancellation pending Default Value: 0

26.1.40 CANFD0_CH0_TXBTO

Description: Tx Buffer Transmission Occurred

Address: 0x428400D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TO [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TO [31:24]							

Bits	Name	Description
31 : 0	TO	Transmission Occurred Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmission occurred 1= Transmission occurred Default Value: 0

26.1.41 CANFD0_CH0_TXBCF

Description: Tx Buffer Cancellation Finished

Address: 0x428400DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CF [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	CF [31:24]							

Bits	Name	Description
31 : 0	CF	Cancellation Finished Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmit buffer cancellation 1= Transmit buffer cancellation finished Default Value: 0

26.1.42 CANFD0_CH0_TXBTIE

Description: Tx Buffer Transmission Interrupt Enable

Address: 0x428400E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TIE [31:24]							

Bits	Name	Description
31 : 0	TIE	Transmission Interrupt Enable Each Tx Buffer has its own Transmission Interrupt Enable bit. 0= Transmission interrupt disabled 1= Transmission interrupt enable Default Value: 0

26.1.43 CANFD0_CH0_TXBCIE

Description: Tx Buffer Cancellation Finished Interrupt Enable

Address: 0x428400E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CFIE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CFIE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFIE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CFIE [31:24]							

Bits	Name	Description
31 : 0	CFIE	Cancellation Finished Interrupt Enable Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0= Cancellation finished interrupt disabled 1= Cancellation finished interrupt enabled Default Value: 0

26.1.44 CANFD0_CH0_TXEFC

Description: Tx Event FIFO Configuration

Address: 0x428400F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	
HW Access	R						Reserved	
Name	EFSA [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	EFSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [23:22]		EFS [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [31:30]		EFWM [29:24]					

Bits	Name	Description
29 : 24	EFWM	Event FIFO Watermark 0= Watermark interrupt disabled 1-32= Level for Tx Event FIFO watermark interrupt (IR.TEFW) 32= Watermark interrupt disabled Default Value: 0
21 : 16	EFS	Event FIFO Size 0= Tx Event FIFO disabled 1-32= Number of Tx Event FIFO elements 32= Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to EFS-1 Default Value: 0
15 : 2	EFSA	Event FIFO Start Address Start address of Tx Event FIFO in Message RAM (32-bit word address, see Figure 2). Default Value: 0

26.1.45 CANFD0_CH0_TXEFS

Description: Tx Event FIFO Status

Address: 0x428400F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [7:6]		EFFL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R				
HW Access	Reserved			RW				
Name	Reserved [15:13]			EFGI [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			R				
HW Access	Reserved			RW				
Name	Reserved [23:21]			EFPI [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						R	R
HW Access	Reserved						RW	RW
Name	Reserved [31:26]						TEFL	EFF

Bits	Name	Description
25	TEFL	Tx Event FIFO Element Lost This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero. Default Value: 0
24	EFF	Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full Default Value: 0
20 : 16	EFPI	Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31. Default Value: 0
12 : 8	EFGI	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. This field is updated by the software writing to TXEFA.EFAI. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected. Default Value: 0
5 : 0	EFFL	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected. Default Value: 0

26.1.46 CANFD0_CH0_TXEFA

Description: Tx Event FIFO Acknowledge

Address: 0x428400F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			EFAI [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	EFAI	Event FIFO Acknowledge Index After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL. Default Value: 0

26.1.47 CANFD0_CH0_TTTMC

Description: TT Trigger Memory Configuration

Address: 0x42840100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						Reserved	
HW Access	R						Reserved	
Name	TMSA [7:2]						Reserved [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TMSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	TME [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
22 : 16	TME	Trigger Memory Elements 0= No Trigger Memory 1-64= Number of Trigger Memory elements 64= Values greater than 64 are interpreted as 64 Default Value: 0
15 : 2	TMSA	Trigger Memory Start Address Start address of Trigger Memory in Message RAM (32-bit word address, see Figure 2). Default Value: 0

26.1.48 CANFD0_CH0_TTRMC

Description: TT Reference Message Configuration

Address: 0x42840104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved	RW				
HW Access	R	R	Reserved	R				
Name	RMPS	XTD	Reserved	RID [28:24]				

Bits	Name	Description
31	RMPS	Reference Message Payload Select Ignored in case of time slaves. 0= Reference message has no additional payload 1= The following elements are taken from Tx Buffer 0: Message Marker MM, Event FIFO Control EFC, Data Length Code DLC, Data Bytes DB Level 1: bytes 2-8, Level 0,2: bytes 5-8) Default Value: 0
30	XTD	Extended Identifier 0= 11-bit standard identifier 1= 29-bit extended identifier Default Value: 0
28 : 0	RID	Reference Identifier Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference identifier depending on bit XTD. A standard identifier has to be written to ID[28:18]. Default Value: 0

26.1.49 CANFD0_CH0_TTOCF

Description: TT Operation Configuration

Address: 0x42840108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW	RW	Reserved	RW	
HW Access	R			R	R	Reserved	R	
Name	LDSDL [7:5]			TM	GEN	Reserved	OM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	R	R						
Name	EECS	IRTO [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	AWL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [31:27]					EVTP	ECC	EGTF

Bits	Name	Description
26	EVTP	Event Trigger Polarity 0= Rising edge trigger 1= Falling edge trigger Default Value: 0
25	ECC	Enable Clock Calibration 0= Automatic clock calibration in TTCAN Level 0,2 is disabled 1= Automatic clock calibration in TTCAN Level 0,2 is enabled Default Value: 0
24	EGTF	Enable Global Time Filtering 0= Global time filtering in TTCAN Level 0,2 is disabled 1= Global time filtering in TTCAN Level 0,2 is enabled Default Value: 0
23 : 16	AWL	Application Watchdog Limit The application watchdog can be disabled by programming AWL to 0x00. 0x00-FF Maximum time after which the application has to serve the application watchdog. The application watchdog is incremented once each 256 NTUs. Default Value: 1
15	EECS	Enable External Clock Synchronization If enabled, TUR configuration (TURCF.NCL only) may be updated during TTCAN operation. 0= External clock synchronization in TTCAN Level 0,2 disabled 1= External clock synchronization in TTCAN Level 0,2 enabled Default Value: 0
14 : 8	IRTO	Initial Reference Trigger Offset 0x00-7F Positive offset, range from 0 to 127 Default Value: 0

26.1.49 CANFD0_CH0_TTOCF (continued)

7 : 5	LDSDL	LD of Synchronization Deviation Limit The Synchronization Deviation Limit SDL is configured by its dual logarithm LDSDL with SDL = 2(LDSDL + 5). It should not exceed the clock tolerance given by the CAN bit timing configuration. 0x0-7 LD of Synchronization Deviation Limit (SDL <= 32...4096) Default Value: 0
4	TM	Time Master 0= Time Master function disabled 1= Potential Time Master Default Value: 0
3	GEN	Gap Enable 0= Strictly time-triggered operation 1= External event-synchronized time-triggered operation Default Value: 0
1 : 0	OM	Operation Mode 00= Event-driven CAN communication, default 01= TTCAN level 1 10= TTCAN level 2 11= TTCAN level 0 Default Value: 0

26.1.50 CANFD0_CH0_TTMLM

Description: TT Matrix Limits

Address: 0x4284010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	CSS [7:6]		CCM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				TXEW [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENTT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				ENTT [27:24]			

Bits	Name	Description
27 : 16	ENTT	Expected Number of Tx Triggers 0x000-FFF Expected number of Tx Triggers in one Matrix Cycle Default Value: 0
11 : 8	TXEW	Tx Enable Window 0x0-F Length of Tx enable window, 1-16 NTU cycles Default Value: 0
7 : 6	CSS	Cycle Start Synchronization Enables sync pulse output at pin m_ttcan_soc. 00= No sync pulse 01= Sync pulse at start of basic cycle 10= Sync pulse at start of matrix cycle 11= Reserved Default Value: 0
5 : 0	CCM	Cycle Count Max 0x00 1 Basic Cycle per Matrix Cycle 0x01 2 Basic Cycles per Matrix Cycle 0x03 4 Basic Cycles per Matrix Cycle 0x07 8 Basic Cycles per Matrix Cycle 0x0F 16 Basic Cycles per Matrix Cycle 0x1F 32 Basic Cycles per Matrix Cycle 0x3F 64 Basic Cycles per Matrix Cycle others Reserved Default Value: 0

26.1.51 CANFD0_CH0_TURCF

Description: TUR Configuration

Address: 0x42840110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	NCL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NCL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved	RW					
HW Access	R	Reserved	R					
Name	ELT	Reserved	DC [29:24]					

Bits	Name	Description
31	ELT	Enable Local Time 0= Local time is stopped, default 1= Local time is enabled Default Value: 0
29 : 16	DC	Denominator Configuration 0x0000 Illegal value 0x0001-3FFF Denominator Configuration Default Value: 0x1000
15 : 0	NCL	Numerator Configuration Low Write access to the TUR Numerator Configuration Low is only possible during configuration with TURCF.ELT = '0' or if TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT Configuration Mode, the new value takes effect when TTOST.WECS is cleared to '0'. NCL is locked TTOST.WECS is '1'. 0x0000-FFFF Numerator Configuration Low Default Value: 0

26.1.52 CANFD0_CH0_TTOCN

Description: TT Operation Control

Address: 0x42840114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW		RW	RW	RW
HW Access	R		R	R		R	R	R
Name	TMC [7:6]		RTIE	SWS [4:3]		SWP	ECS	SGT

Bits	15	14	13	12	11	10	9	8
SW Access	R	Reserved	RW	RW	RW	RW	RW	RW
HW Access	RW	Reserved	R	R	R	R	R	R
Name	LCKC	Reserved	ESCN	NIG	TMG	FGP	GCS	TTIE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	LCKC	TT Operation Control Register Locked Set by a write access to register TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain. 0= Write access to TTOCN enabled 1= Write access to TTOCN locked Default Value: 0
13	ESCN	External Synchronization Control If enabled the M_TTCAN synchronizes its cycle time phase to an external event signaled by a rising edge at pin m_ttcan_evt (see Section 4.11). 0= External synchronization disabled 1= External synchronization enabled Default Value: 0
12	NIG	Next is Gap This bit can only be set when the M_TTCAN is the actual Time Master and when it is configured for external event-synchronized time-triggered operation (TTOCF.GEN = '1') 0= No action, reset by reception of any reference message 1= Transmit next reference message with Next_is_Gap = '1' Default Value: 0
11	TMG	Time Mark Gap 0= Reset by each reference message 1= Next reference message started when Register Time Mark interrupt TTIR.RTMI is activated Default Value: 0

26.1.52 CANFD0_CH0_TTOCN (continued)

10	FGP	Finish Gap Set by the CPU, reset by each reference message 0= No reference message requested 1= Application requested start of reference message Default Value: 0
9	GCS	Gap Control Select 0= Gap control independent from m_ttcan_evt 1= Gap control by input pin m_ttcan_evt Default Value: 0
8	TTIE	Trigger Time Mark Interrupt Pulse Enable External time mark events are configured by trigger memory element TMEX (see Section 2.4.7). A trigger time mark interrupt pulse is generated when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Schedule or In_Gap. 0= Trigger Time Mark Interrupt output m_ttcan_tmp disabled 1= Trigger Time Mark Interrupt output m_ttcan_tmp enabled Default Value: 0
7 : 6	TMC	Register Time Mark Compare 00= No Register Time Mark Interrupt generated 01= Register Time Mark Interrupt if Time Mark = cycle time 10= Register Time Mark Interrupt if Time Mark = local time 11= Register Time Mark Interrupt if Time Mark = global time Default Value: 0
5	RTIE	Register Time Mark Interrupt Pulse Enable Register time mark interrupts are configured by register TTTMK. A register time mark interrupt pulse with the length of one NTU is generated when the time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Register Time Mark Interrupt output m_ttcan_rtp disabled 1= Register Time Mark Interrupt output m_ttcan_rtp enabled Default Value: 0
4 : 3	SWS	Stop Watch Source 00= Stop Watch disabled 01= Actual value of cycle time is copied to TTCPT.SWV 10= Actual value of local time is copied to TTCPT.SWV 11= Actual value of global time is copied to TTCPT.SWV Default Value: 0
2	SWP	Stop Watch Polarity 0= Rising edge trigger 1= Falling edge trigger Default Value: 0
1	ECS	External Clock Synchronization Writing a '1' to ECS sets TTOST.WECS if the node is the actual Time Master. ECS is reset after one Host clock period. The external clock synchronization takes effect at the start of the next basic cycle. Default Value: 0
0	SGT	Set Global time Writing a '1' to SGT sets TTOST.WGDT if the node is the actual Time Master. SGT is reset after one Host clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to TTGTP. Default Value: 0

26.1.53 CANFD0_CH0_TTGTP

Description: TT Global Time Preset

Address: 0x42840118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CTP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CTP [31:24]							

Bits	Name	Description
31 : 16	CTP	Cycle Time Target Phase CTP is write-protected while TTOCN.ESCN or TTOST.SPL are set (see Section 4.11). 0x0000-FFFF Defines target value of cycle time when a rising edge of m_ttcan_evt is expected Default Value: 0
15 : 0	TP	Time Preset TP is write-protected while TTOST.WGTD is set. 0x0000-7FFF Next Master Reference Mark = Master Reference Mark + TP 0x8000 reserved 0x8001-FFFF Next Master Reference Mark = Master Reference Mark - (0x10000 - TP) Default Value: 0

26.1.54 CANFD0_CH0_TTTMK

Description: TT Time Mark

Address: 0x4284011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TM_ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TM_ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	TICC [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	RW	Reserved						
Name	LCKM	Reserved [30:24]						

Bits	Name	Description
31	LCKM	TT Time Mark Register Locked Always set by a write access to registers TTOCN. Set by write access to register TTTMK when TTOCN.TMC != '00'. Reset when the registers have been synchronized into the CAN clock domain. 0= Write access to TTTMK enabled 1= Write access to TTTMK locked Default Value: 0
22 : 16	TICC	Time Mark Cycle Code Cycle count for which the time mark is valid. 0b000000x valid for all cycles 0b000001c valid every second cycle at cycle count mod2 = c 0b00001cc valid every fourth cycle at cycle count mod4 = cc 0b0001ccc valid every eighth cycle at cycle count mod8 = ccc 0b001cccc valid every sixteenth cycle at cycle count mod16 = cccc 0b01ccccc valid every thirty-second cycle at cycle count mod32 = ccccc 0b1cccccc valid every sixty-fourth cycle at cycle count mod64 = cccccc Default Value: 0
15 : 0	TM_	Time Mark 0x0000-FFFF Time Mark Default Value: 0

26.1.55 CANFD0_CH0_TTIR

Description: TT Interrupt Register

Address: 0x42840120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	GTW	SWE	TTMI	RTMI	SOG	CSM_	SMC	SBC

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	IWT	ELC	SE2	SE1	TXO	TXU	GTE	GTD

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW1C	RW1C	RW1C
HW Access	Reserved					RW	RW	RW
Name	Reserved [23:19]					CER	AW	WT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	CER	Configuration Error Trigger out of order. 0= No error found in trigger list 1= Error found in trigger list Default Value: 0
17	AW	Application Watchdog 0= Application watchdog served in time 1= Application watchdog not served in time Default Value: 0
16	WT	Watch Trigger 0= No missing reference message 1= Missing reference message (Level 0: cycle time 0xFF00) Default Value: 0
15	IWT	Initialization Watch Trigger The initialization is restarted by resetting IWT. 0= No missing reference message during system startup 1= No system startup due to missing reference message Default Value: 0
14	ELC	Error Level Changed Not set when error level changed during initialization. 0= No change in error level 1= Error level changed Default Value: 0

26.1.55 CANFD0_CH0_TTIR (continued)

13	SE2	Scheduling Error 2 0= No scheduling error 2 1= Scheduling error 2 occurred Default Value: 0
12	SE1	Scheduling Error 1 0= No scheduling error 1 1= Scheduling error 1 occurred Default Value: 0
11	TXO	Tx Count Overflow 0= Number of Tx Trigger as expected 1= More Tx trigger than expected in one matrix cycle Default Value: 0
10	TXU	Tx Count Underflow 0= Number of Tx Trigger as expected 1= Less Tx trigger than expected in one matrix cycle Default Value: 0
9	GTE	Global Time Error Synchronization deviation SD exceeds limit specified by TTOCF.LDSDL, TTCAN Level 0,2 only. 0= Synchronization deviation within limit 1= Synchronization deviation exceeded limit Default Value: 0
8	GTD	Global Time Discontinuity 0= No discontinuity of global time 1= Discontinuity of global time Default Value: 0
7	GTW	Global Time Wrap 0= No global time wrap occurred 1= Global time wrap from 0xFFFF to 0x0000 occurred Default Value: 0
6	SWE	Stop Watch Event 0= No rising/falling edge at stop watch trigger pin m_ttcan_swt detected 1= Rising/falling edge at stop watch trigger pin m_ttcan_swt detected Default Value: 0
5	TTMI	Trigger Time Mark Event Internal Internal time mark events are configured by trigger memory element TMIN (see Section 2.4.7). Set when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Gap or In_Schedule. 0= Time mark not reached 1= Time mark reached (Level 0: cycle time TTOCF.IRTO * 0x200) Default Value: 0
4	RTMI	Register Time Mark Interrupt Set when time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Time mark not reached 1= Time mark reached Default Value: 0
3	SOG	Start of Gap 0= No reference message seen with Next_is_Gap bit set 1= Reference message with Next_is_Gap bit set becomes valid Default Value: 0
2	CSM_	Change of Synchronization Mode 0= No change in master to slave relation or schedule synchronization 1= Master to slave relation or schedule synchronization changed, also set when TTOST.SPL is reset Default Value: 0

26.1.55 CANFD0_CH0_TTIR (continued)

1	SMC	Start of Matrix Cycle 0= No Matrix Cycle started since bit has been reset 1= Matrix Cycle started Default Value: 0
0	SBC	Start of Basic Cycle 0= No Basic Cycle started since bit has been reset 1= Basic Cycle started Default Value: 0

26.1.56 CANFD0_CH0_TTIE

Description: TT Interrupt Enable

Address: 0x42840124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	GTWE	SWEE	TTMIE	RTMIE	SOGE	CSME	SMCE	SBCE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	IWTE	ELCE	SE2E	SE1E	TXOE	TXUE	GTEE	GTDE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [23:19]					CERE	AWE_	WTE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	CERE	Configuration Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
17	AWE_	Application Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
16	WTE	Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
15	IWTE	Initialization Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
14	ELCE	Change Error Level Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
13	SE2E	Scheduling Error 2 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

26.1.56 CANFD0_CH0_TTIE (continued)

12	SE1E	Scheduling Error 1 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
11	TXOE	Tx Count Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
10	TXUE	Tx Count Underflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
9	GTEE	Global Time Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
8	GTDE	Global Time Discontinuity Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
7	GTWE	Global Time Wrap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
6	SWEE	Stop Watch Event Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
5	TTMIE	Trigger Time Mark Event Internal Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
4	RTMIE	Register Time Mark Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
3	SOGE	Start of Gap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
2	CSME	Change of Synchronization Mode Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
1	SMCE	Start of Matrix Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
0	SBCE	Start of Basic Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

26.1.57 CANFD0_CH0_TTILS

Description: TT Interrupt Line Select

Address: 0x42840128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	GTWL	SWEL	TTMIL	RTMIL	SOGL	CSML	SMCL	SBCL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	IWTL	ELCL	SE2L	SE1L	TXOL	TXUL	GTEL	GTDL

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [23:19]					CERL	AWL_	WTL

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
18	CERL	Configuration Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
17	AWL_	Application Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
16	WTL	Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
15	IWTL	Initialization Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
14	ELCL	Change Error Level Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
13	SE2L	Scheduling Error 2 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

26.1.57 CANFD0_CH0_TTILS (continued)

12	SE1L	Scheduling Error 1 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
11	TXOL	Tx Count Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
10	TXUL	Tx Count Underflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
9	GTEL	Global Time Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
8	GTDL	Global Time Discontinuity Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
7	GTWL	Global Time Wrap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
6	SWEL	Stop Watch Event Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
5	TTMIL	Trigger Time Mark Event Internal Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
4	RTMIL	Register Time Mark Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
3	SOGL	Start of Gap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
2	CSML	Change of Synchronization Mode Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
1	SMCL	Start of Matrix Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
0	SBCL	Start of Basic Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

26.1.58 CANFD0_CH0_TTOST

Description: TT Operation Status

Address: 0x4284012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R		R		R	
HW Access	RW	RW	RW		RW		RW	
Name	QCS	QGTP	SYS [5:4]		MS [3:2]		EL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RTO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	Reserved					
HW Access	RW	RW	Reserved					
Name	GFI	WGTD	Reserved [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	R	R		
HW Access	RW	RW	RW	RW	RW	RW		
Name	SPL	WECS	AWE	WFE	GSI	TMP [26:24]		

Bits	Name	Description
31	SPL	Schedule Phase Lock The bit is valid only when external synchronization is enabled (TTOCN.ESCN = '1'). In this case it signals that the difference between cycle time configured by TTGTP.CTP and the cycle time at the rising edge at pin m_ttcan_evt is less or equal 9 NTU (see Section 4.11). 0= Phase outside range 1= Phase inside range Default Value: 0
30	WECS	Wait for External Clock Synchronization 0= No external clock synchronization pending 1= Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle. Default Value: 0
29	AWE	Application Watchdog Event The application watchdog is served by reading TTOST. When the watchdog is not served in time, bit AWE is set, all TTCAN communication is stopped, and the M_TTCAN is set into Bus Monitor-ing Mode. 0= Application Watchdog served in time 1= Failed to serve Application Watchdog in time Default Value: 0
28	WFE	Wait for Event 0= No Gap announced, reset by a reference message with Next_is_Gap = '0' 1= Reference message with Next_is_Gap = '1' received Default Value: 0

26.1.58 CANFD0_CH0_TTOST (continued)

27	GSI	Gap Started Indicator 0= No Gap in schedule, reset by each reference message and for all time slaves 1= Gap time after Basic Cycle has started Default Value: 0
26 : 24	TMP	Time Master Priority 0x0-7 Priority of actual Time Master Default Value: 0
23	GFI	Gap Finished Indicator Set when the CPU writes TTOCN.FGP, or by a time mark interrupt if TMG = '1', or via input pin m_ttcan_evt if TTOCN.GCS = '1'. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message. 0= Reset at the end of each reference message 1= Gap finished by M_TTCAN Default Value: 0
22	WGTD	Wait for Global Time Discontinuity 0= No global time preset pending 1= Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = '1' or after it received a reference message. Default Value: 0
15 : 8	RTO	Reference Trigger Offset The Reference Trigger Offset value is a signed integer with a range from -127 (0x81) to 127 (0x7F). There is no notification when the lower limit of -127 is reached. In case the M_TTCAN becomes Time Master (MS[1:0] = '11'), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by TTOCF.IRTO is read. 0x00-FF Actual Reference Trigger offset value Default Value: 0
7	QCS	Quality of Clock Speed Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '1'. 0= Local clock speed not synchronized to Time Master clock speed 1= Synchronization Deviation <= SDL Default Value: 1
6	QGTP	Quality of Global Time Phase Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '0'. 0= Global time not valid 1= Global time in phase with Time Master Default Value: 0
5 : 4	SYS	Synchronization State 00= Out of Synchronization 01= Synchronizing to TTCAN communication 10= Schedule suspended by Gap (In_Gap) 11= Synchronized to schedule (In_Schedule) Default Value: 0
3 : 2	MS	Master State 00= Master_Off, no master properties relevant 01= Operating as Time Slave 10= Operating as Backup Time Master 11= Operating as current Time Master Default Value: 0
1 : 0	EL	Error Level 00= Severity 0 - No Error 01= Severity 1 - Warning 10= Severity 2 - Error 11= Severity 3 - Severe Error Default Value: 0

26.1.59 CANFD0_CH0_TURNA

Description: TUR Numerator Actual

Address: 0x42840130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NAV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NAV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						R	
HW Access	Reserved						RW	
Name	Reserved [23:18]						NAV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17 : 0	NAV	Numerator Actual Value 0x0EFFF reserved 0x0F000-20FFF Actual numerator value 0x21000 reserved Default Value: 0x10000

26.1.60 CANFD0_CH0_TTLGT

Description: TT Local & Global Time

Address: 0x42840134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	GT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	GT [31:24]							

Bits	Name	Description
31 : 16	GT	Global Time Non-fractional part of the sum of the node's local time and its local offset (see Section 4.5). 0x0000-FFFF Global time value of TTCAN network Default Value: 0
15 : 0	LT	Local Time Non-fractional part of local time, incremented once each local NTU (see Section 4.5). 0x0000-FFFF Local time value of TTCAN node Default Value: 0

26.1.61 CANFD0_CH0_TTCTC

Description: TT Cycle Time & Count

Address: 0x42840138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [23:22]		CC [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
21 : 16	CC	Cycle Count 0x00-3F Number of actual Basic Cycle in the System Matrix Default Value: 0x3F
15 : 0	CT	Cycle Time Non-fractional part of the difference of the node's local time and Ref_Mark (see Section 4.5). 0x0000-FFFF Cycle time value of TTCAN Basic Cycle Default Value: 0

26.1.62 CANFD0_CH0_TTCPT

Description: TT Capture Time

Address: 0x4284013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R					
HW Access	Reserved		RW					
Name	Reserved [7:6]		CCV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	SWV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	SWV [31:24]							

Bits	Name	Description
31 : 16	SWV	Stop Watch Value On a rising/falling edge (as configured via TTOCN.SWP) at the Stop Watch Trigger pin m_ttcan_swt, when TTOCN.SWS is != '00' and TTIR.SWE is '0', the actual time value as selected by TTOCN.SWS (cycle, local, global) is copied to SWV and TTIR.SWE will be set to '1'. Capturing of the next stop watch value is enabled by resetting TTIR.SWE. 0x0000-FFFF Captured Stop Watch value Default Value: 0
5 : 0	CCV	Cycle Count Value Cycle count value captured together with SWV. 0x00-3F Captured cycle count value Default Value: 0

26.1.63 CANFD0_CH0_TTCSM

Description: TT Cycle Sync Mark

Address: 0x42840140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CSM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CSM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	CSM	Cycle Sync Mark The Cycle Sync Mark is measured Default Value: 0

26.1.64 CANFD0_CH0_RXFTOP_CTL

Description: Receive FIFO Top control

Address: 0x42840180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						F1TPE	F0TPE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	F1TPE	FIFO 1 Top Pointer Enable. Default Value: 0
0	F0TPE	FIFO 0 Top Pointer Enable. This enables the FIFO top pointer logic to set the FIFO Top Address (FnTA) and message word counter. This logic is also disabled when the IP is being reconfigured (CCCR.CCE=1). When this logic is disabled a Read from RXFTOP0_DATA is undefined. Default Value: 0

26.1.65 CANFD0_CH0_RXFTOP0_STAT

Description: Receive FIFO 0 Top Status

Address: 0x428401A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	F0TA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	F0TA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	F0TA	Current FIFO 0 Top Address. This is a pointer to the next word in the message buffer defined by the FIFO Start Address (FnSA), Get Index (FnGI), the FIFO message size (FnDS) and the message word counter (FnMWC) FnTA = FnSA + FnGI * msg_size[FnDS] + FnMWC Default Value: 0

26.1.66 CANFD0_CH0_RXFTOP0_DATA

Description: Receive FIFO 0 Top Data

Address: 0x428401A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	F0TD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	F0TD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	F0TD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	F0TD [31:24]							

Bits	Name	Description
31 : 0	F0TD	When enabled (F0TPE=1) read data from MRAM at location FnTA. This register can have a read side effect if the following conditions are met: - M_TTCAN not being reconfigured (CCCR.CCE=0) - FIFO Top Pointer logic is enabled (FnTPE=1) - FIFO is not empty (FnFL!=0) The read side effect is as follows: - if FnMWC pointed to the last word of the message (as indicated by FnDS) then the corresponding message index (FnGI) is automatically acknowledge by a write to FnAI - FnMWC is incremented (or restarted if FnMWC pointed to the last word of the message) - the FIFO top address FnTA is incremented (with FIFO wrap around) When this logic is disabled (F0TPE=0) a Read from this register returns undefined data. Default Value: Undefined

26.1.67 CANFD0_CH0_RXFTOP1_STAT

Description: Receive FIFO 1 Top Status

Address: 0x428401B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	F1TA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	F1TA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	F1TA	See F0TA description Default Value: 0

26.1.68 CANFD0_CH0_RXFTOP1_DATA

Description: Receive FIFO 1 Top Data

Address: 0x428401B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	F1TD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	F1TD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	F1TD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	F1TD [31:24]							

Bits	Name	Description
31 : 0	F1TD	See F0TD description Default Value: Undefined

26.1.69 CANFD0_CTL

Description: Global CAN control register

Address: 0x42841000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						STOP_REQ [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	STOP_REQ	Clock Stop Request for each TTCAN IP . The m_ttcan_clkstop_req of each TTCAN IP is directly driven by these bits. Default Value: 0

26.1.70 CANFD0_STATUS

Description: Global CAN status register

Address: 0x42841004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	
HW Access	Reserved						RW	
Name	Reserved [7:2]						STOP_ACK [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	STOP_ACK	Clock Stop Acknowledge for each TTCAN IP. These bits are directly driven by m_ttcan_clkstop_ack of each TTCAN IP. When this bit is set the corresponding TTCAN IP clocks will be gated off, except HCLK will enabled for each AHB write Default Value: 0

26.1.71 CANFD0_INTR0_CAUSE

Description: Consolidated interrupt0 cause register

Address: 0x42841010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	
HW Access	Reserved						RW	
Name	Reserved [7:2]						INT0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	INT0	Show pending m_ttcan_int0 of each channel Default Value: 0

26.1.72 CANFD0_INTR1_CAUSE

Description: Consolidated interrupt1 cause register

Address: 0x42841014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	
HW Access	Reserved						RW	
Name	Reserved [7:2]						INT1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	INT1	Show pending m_ttcan_int1 of each channel Default Value: 0

26.1.73 CANFD0_TS_CTL

Description: Time Stamp control register

Address: 0x42841020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRESCALE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PRESCALE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	Counter enable bit 0 = Count disabled. Stop counting up and keep the counter value 1 = Count enabled. Start counting up from the current value Default Value: 0
15 : 0	PRESCALE	Time Stamp counter prescale value. When enabled divide the Host clock (HCLK) by PRESCALE+1 to create Time Stamp clock ticks. Default Value: 0

26.1.74 CANFD0_TS_CNT

Description: Time Stamp counter value

Address: 0x42841024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	VALUE	The counter value of the Time Stamp Counter. When enabled this counter will count Time Stamp clock ticks from the pre-scaler. When written this counter and the pre-scaler will reset to 0 (write data is ignored). Default Value: 0

27 Graphics Subsystem (GFXSS) registers

This section discusses the GFXSS registers. It lists all the registers in mapping tables, in address order.

27.1 Register details

Register name	Address	Description
GFXSS_GPU_MXGPU_CTL	0x44800000	IP control.
GFXSS_GPU_MXGPU_STATUS	0x4480000C	IP status.
GFXSS_GPU_MXGPU_INTR	0x44800010	Interrupt status bits.
GFXSS_GPU_MXGPU_INTR_SET	0x44800014	Interrupt set bits.
GFXSS_GPU_MXGPU_INTR_MASK	0x44800018	Interrupt mask bits.
GFXSS_GPU_MXGPU_INTR_MASKED	0x4480001C	Interrupt masked bits.
GFXSS_GPU_GCNANO_AQHICLOCKCONTROL	0x44800800	Clock Control Register.
GFXSS_GPU_GCNANO_AQHIIDLE	0x44800804	Idle Status Register.
GFXSS_GPU_GCNANO_AQAXICONFIG	0x44800808	AXI Configuration Register.
GFXSS_GPU_GCNANO_AQAXISTATUS	0x4480080C	AXI Status Register. READ ONLY. Back-to-back read is forbidden to this register and can cause system hang. Please insert delay (nop operation) between two consecutive reads while accessing this register outside of VSI drivers.
GFXSS_GPU_GCNANO_AQINTRACKNOWLEDGE	0x44800810	Interrupt Acknowledge Register. Each bit represents a corresponding event being triggered. Reading from this register clears the outstanding interrupt. READ ONLY. When the access comes from a debugger (HMASTER[0] == 1), the clear by read function is disabled. Back-to-back read is forbidden to this register and can cause system hang. Please insert delay (nop operation) between two consecutive reads while accessing this register outside of VSI drivers.
GFXSS_GPU_GCNANO_AQINTRENBL	0x44800814	Interrupt Enable Register. Each bit enables a corresponding event.
GFXSS_GPU_GCNANO_GCCHIPREV	0x44800824	Chip Revsion Register. Shows the revision for the chip in BCD. This register has no set reset value. It varies with the implementation. READ ONLY.
GFXSS_GPU_GCNANO_GCCHIPDATE	0x44800828	Chip Date Register. Shows the release date for the IP in YYYYMMDD (year/month/day) format. This register has no set reset value. It varies with the implementation. READ ONLY.
GFXSS_GPU_GCNANO_GCREGHICHIPPATCHREV	0x44800898	Chip Patch Revision Register. Patch revision level for the chip. It varies per release. READ ONLY
GFXSS_GPU_GCNANO_GCPRODUCTID	0x448008A8	Product Identification Register. Shows Product ID. READ ONLY.

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_GPU_GCNANO_GCMODULEPOWERCONTROLS	0x44800900	Module Power Control Register. Control register for module level power controls.
GFXSS_GPU_GCNANO_GCMODULEPOWERMODULECONTROL	0x44800904	Module Power Module Control Register. Module level control register.
GFXSS_GPU_GCNANO_GCMODULEPOWERMODULESTATUS	0x44800908	Module Power Module Status Register. Module level control status.
GFXSS_GPU_GCNANO_AQMEMORYDEBUG	0x44800C14	Memory Debug Register.
GFXSS_GPU_GCNANO_AQREGISTERTIMINGCONTROL	0x44800C2C	Timing Control Register.
GFXSS_GPU_GCNANO_GCREGFETCHADDRESS	0x44800D00	Fetch Command Buffer Base Address Register. Address of the command buffer. The address must be 64-byte aligned.
GFXSS_GPU_GCNANO_GCREGFETCHCONTROL	0x44800D04	Fetch Control Register. Writing a non-zero value to this register starts the fetch engine. The FE will start fetching 64-bit commands and data starting at the address specified by the gcregFetchAddress register. Make sure this count is large enough to fetch the END command, otherwise the FE will wait until more data is coming.
GFXSS_GPU_GCNANO_GCREGCURRENTFETCHADDRESS	0x44800D08	Current Fetch Command Address Register. Debugging register that defines the current address the FE is fetching data from. READ ONLY.
GFXSS_DC_MXDC_CTL	0x44801000	IP control.
GFXSS_DC_MXDC_CLK_CTL	0x44801004	Clock control.
GFXSS_DC_MXDC_IO_CTL	0x44801008	IO enable control.
GFXSS_DC_MXDC_STATUS	0x4480100C	IP status.
GFXSS_DC_MXDC_INTR	0x44801010	Interrupt status.
GFXSS_DC_MXDC_INTR_SET	0x44801014	Interrupt set bits.
GFXSS_DC_MXDC_INTR_MASK	0x44801018	Interrupt mask bits.
GFXSS_DC_MXDC_INTR_MASKED	0x4480101C	Interrupt masked bits.
GFXSS_DC_MXDC_ADDR0_INT	0x44801020	Address 0 for interrupt generation.
GFXSS_DC_MXDC_ADDR1_INT	0x44801024	Address 1 for interrupt generation.
GFXSS_DC_MXDC_ADDR2_INT	0x44801028	Address 2 for interrupt generation.
GFXSS_DC_MXDC_ADDR3_INT	0x4480102C	Address 3 for interrupt generation.
GFXSS_DC_MXDC_RLAD_CTL	0x44801040	Control options for the RLAD decoder.
GFXSS_DC_MXDC_RLAD_IMG	0x44801044	Properties of the uncompressed image.
GFXSS_DC_MXDC_RLAD_ENC	0x44801048	Configuration of the encoder that compressed the image.
GFXSS_DC_MXDC_RLAD_BUF0	0x4480104C	Properties of the compressed image data buffer.
GFXSS_DC_MXDC_RLAD_BUF1	0x44801050	Properties of the compressed image data buffer.
GFXSS_DC_MXDC_RLAD_STATUS	0x44801054	RLAD decoder status.

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_DC_MXDC_IPIDENTIFIER	0x44801070	GFXSS IP and desig release identification (with DC, GPU and MIPIDSI).
GFXSS_DC_DCNANO_GCREGDCCHIPREV	0x44801800	Chip Revision Register. Shows the revision for the chip in BCD. This register has no set reset value. It varies with the implementation. READ ONLY.
GFXSS_DC_DCNANO_GCREGDCCHIPDATE	0x44801804	Chip Date Register. Shows the release date for the IP in YYYYMMDD (year, month. day) format. This register has no set reset value. It varies with the implementation. READ ONLY.
GFXSS_DC_DCNANO_GCREGDCCHIPPATCHREV	0x44801808	Patch Revision Register. Patch revision level for the chip. READ ONLY.
GFXSS_DC_DCNANO_GCREGDCPRODUCTID	0x4480180C	Product Identification Register. READ ONLY.
GFXSS_DC_DCNANO_GCREGFRAMEBUFFERCONFIG	0x44801824	Frame Buffer Configuration Register. Frame Buffer and Timing control. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGFRAMEBUFFERADDRESS	0x44801828	Frame Buffer Base Address Register. Starting address of the frame buffer. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGFRAMEBUFFERSTRIDE	0x4480182C	Frame Buffer Stride Register. Stride of the frame buffer in bytes. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDCTILEINCFG	0x44801834	Tile Input Configuration Register. Tile input configuration. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDCTILEUVFRAMEBUFFERADR	0x44801838	Frame Buffer Tiled UV Base Address Register. UV frame buffer address when tile input. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDCTILEUVFRAMEBUFFERSTR	0x4480183C	Frame Buffer Tiled UV Stride Register. UV frame buffer stride when tile input NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGFRAMEBUFFERBACKGROUND	0x44801858	Framebuffer background color. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGFRAMEBUFFERCOLORKEY	0x4480185C	Framebuffer Color Key Start Address Register. Start of color key range of framebuffer. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGFRAMEBUFFERCOLORKEYHIGH	0x44801860	Framebuffer Color Key End Address Register. End of color key range of framebuffer. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGFRAMEBUFFERCLEARVALUE	0x44801864	Framebuffer Clear Value Register. Clear value used when dcregFrameBufferConfig.Clear is enabled, format is A8R8G8B8. NOTE.. This register is double buffered.

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_DC_DCNANO_GCREGVIDEOTL	0x44801868	Top left coordinate of panel pixel where the video should start. Be aware there is no panning inside the video. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGFRAMEBUFFERSIZE	0x4480186C	video size information. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGVIDEOGLOBALALPHA	0x44801870	Global alpha for the video. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGBLENDSTACKORDER	0x44801874	Set the video, overlay0, overlay1 order for blend. The 1st is the lowest layer, the 2nd is the middle layer, the 3rd is the highest layer. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGVIDEOALPHABLENDCONFIG	0x44801878	Alpha Blending Configuration Register. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYCONFIG	0x4480187C	Overlay Configuration Register. Overlay control. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYADDRESS	0x44801880	Starting address of the overlay. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYSTRIDE	0x44801884	Stride of the overlay in bytes. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDCOVERLAYTILEINCFG	0x44801888	Tile Input Configuration Register. Tile input configuration. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDCTILEUVOVERLAYADR	0x4480188C	Starting address of the overlay UV. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDCTILEUVOVERLAYSTR	0x44801890	Stride of the overlay UV in bytes. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYTL	0x44801894	Top left coordinate of panel pixel where the overlay should start. Be aware there is no panning inside the overlay. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYSIZE	0x44801898	overlay size information. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYCOLORKEY	0x4480189C	Overlay Color Key Start Address Register. Start of color key range for overlay. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYCOLORKEYHIGH	0x448018A0	Overlay Color Key End Address Register. End of color key range for overlay. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYALPHABLENDCONFIG	0x448018A4	Alpha Blending Configuration Register. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYGLOBALALPHA	0x448018A8	Overlay global alpha value. NOTE.. This register is double buffered.

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_DC_DCNANO_GCREGOVERLAYCLEARVALUE	0x448018AC	Overlay Clear Value Register. Clear value used when dcregOverlayConfig.Clear is enabled, Format is A8R8G8B8. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYCONFIG1	0x448018B0	Overlay Configuration Register. Overlay control. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYADDRESS1	0x448018B4	Starting address of the overlay. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYSTRIDE1	0x448018B8	Stride of the overlay in bytes. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYTL1	0x448018BC	Top left coordinate of panel pixel where the overlay should start. Be aware there is no panning inside the overlay. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYSIZE1	0x448018C0	overlay1 size information. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYCOLORKEY1	0x448018C4	Overlay Color Key Start Address Register. Start of color key range for overlay. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYCOLORKEYHIGH1	0x448018C8	Overlay Color Key End Address Register. End of color key range for overlay. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYALPHABLENDCONFIG1	0x448018CC	Alpha Blending Configuration Register. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYGLOBALALPHA1	0x448018D0	Overlay global alpha value. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGOVERLAYGLOBALALPHA1	0x448018D4	Overlay Clear Value Register. Clear value used when dcregOverlayConfig.Clear is enabled, Format is A8R8G8B8. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDISPLAYDITHERTABLELOW	0x448018E0	Dither Threshold Table Register.
GFXSS_DC_DCNANO_GCREGDISPLAYDITHERTABLEHIGH	0x448018E4	Dither Threshold Table Register.
GFXSS_DC_DCNANO_GCREGPANELCONFIG	0x448018E8	Panel Configuration Register.
GFXSS_DC_DCNANO_GCREGPANELCONTROL	0x448018EC	Panel control Register.
GFXSS_DC_DCNANO_GCREGPANELFUNCTION	0x448018F0	Panel function Register. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGPANELWORKING	0x448018F4	Register to trigger Display Controller.
GFXSS_DC_DCNANO_GCREGPANELSTATE	0x448018F8	Register representing the Display Controller status. READ ONLY.

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_DC_DCNANO_GCREGHDISPLAY	0x44801900	Horizontal Display Total and Visible Pixel Count Register. Horizontal Total and Display End counters. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGHSYNC	0x44801904	Horizontal Sync Counter Register. Horizontal Sync counters. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGVDISPLAY	0x44801910	Vertical Total and Visible Pixel Count Register. Vertical Total and Display End counters. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGVSYNC	0x44801914	Vertical Sync Counter Register. Vertical Sync counters. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDISPLAYCURRENTLOCATION	0x44801918	Display Current Location Register. Current x,y location of display controller. READ ONLY.
GFXSS_DC_DCNANO_GCREGGAMMAINDEX	0x4480191C	Gamma Index Register. Index into gamma table. See gcregGammaData for more information.
GFXSS_DC_DCNANO_GCREGGAMMADATA	0x44801920	Gamma Data Register. Translation values for the gamma table. When this register gets written, the data gets stored in the gamma table at the index specified by the gcregGammaIndex register. After the register is written, the index gets incremented.
GFXSS_DC_DCNANO_GCREGCURSORCONFIG	0x44801924	Cursor Configuration Register. Configuration register for the cursor. Double-buffered values in this register cannot be read while a flip is in progress. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGCURSORADDRESS	0x44801928	Cursor Base Address Register. Address of the cursor shape. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGCURSORLOCATION	0x4480192C	Cursor Location Register. Location of the cursor on the owning display. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGCURSORBACKGROUND	0x44801930	Cursor Background Color Register. The background color for Masked cursors. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGCURSORFOREGROUND	0x44801934	Cursor Foreground Color Register. The foreground color for Masked cursors. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDISPLAYINTR	0x44801938	Display Interrupt Register. This is the interrupt register for the Display. This register will automatically clear after a read. The interrupt bit is set when the current frame buffer is used up. The interrupt signal will be pulled up only when the interrupt enable bit in register gcregDisplayIntrEnable is enabled. READ ONLY. When the access comes from a debugger (HMASTER[0] == 1), the clear by read function is disabled.

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_DC_DCNANO_GCREGDISPLAYINTRENABLE	0x4480193C	Display Interrupt Enable Register. The interrupt enable register for display_0 (and display_1 if present). NOTE.. Interrupt enable for register gcregDisplayIntr. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDBICONFIG	0x44801940	DBI Configuration Register. Configuration register for DBI output.
GFXSS_DC_DCNANO_GCREGDBIIFRESET	0x44801944	DBI Reset Register. Reset DBI interface to idle state. WRITE ONLY.
GFXSS_DC_DCNANO_GCREGDBIWRCHAR1	0x44801948	DBI Write AC Characteristics 1 Register. DBI write AC characteristics definition register 1
GFXSS_DC_DCNANO_GCREGDBIWRCHAR2	0x4480194C	DBI Write AC Characteristics 2 Register. DBI write AC characteristics definition register 2
GFXSS_DC_DCNANO_GCREGDBICMD	0x44801950	DBI Command Control Register. DBI Command in/out port. Writes to this register will send command/data to the DBI port. WRITE ONLY.
GFXSS_DC_DCNANO_GCREGDPICONFIG	0x44801954	DPI Configuration Register. The configuration register for DPI output. NOTE.. This register is double buffered.
GFXSS_DC_DCNANO_GCREGDBITYPECCFG	0x44801958	DBI Type C Timing Control Register. DBI Type C write timing definition.
GFXSS_DC_DCNANO_GCREGDCSTATUS	0x4480195C	Display Controller Status Register. READ ONLY.
GFXSS_DC_DCNANO_GCREGSRCCONFIGENDIAN	0x44801960	Endian control.
GFXSS_DC_DCNANO_GCREGSOFTRESET	0x44801964	Soft reset. WRITE ONLY.
GFXSS_DC_DCNANO_GCREGDCCONTROL	0x44801968	Control register.
GFXSS_DC_DCNANO_GCREGREGISTERTIMINGCONTROL	0x4480196C	Timing control register.
GFXSS_DC_DCNANO_GCREGDEBUGCOUNTERSELECT	0x44801970	Debug Counter Select Register.
GFXSS_DC_DCNANO_GCREGDEBUGCOUNTERVALUE	0x44801974	Debug Counter Value Register. Debug Counter Value as specified in gcregDebugCounterSelect. READ ONLY
GFXSS_DC_DCNANO_GCREGLAYERCLOCKGATE	0x448019A0	Layer clock gater Register. disable video/overlay0/overlay1 clock gater
GFXSS_DC_DCNANO_GCREGDEBUGTOTVIDEOREQ	0x448019A4	debug registers.. count video current frame number of requested burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGLSTVIDEOREQ	0x448019A8	debug registers.. count video last frame number of requested burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGTOTVIDEORRB	0x448019AC	debug registers.. count video current frame number of returned burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGLSTVIDEORRB	0x448019B0	debug registers.. count video last frame number of returned burst. READ ONLY

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_DC_DCNANO_GCREGDEBUGTOTOVERLAY0REQ	0x448019B4	debug registers.. count overlay0 current frame number of requested burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGLSTOVERLAY0REQ	0x448019B8	debug registers.. count overlay0 last frame number of requested burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGTOTOVERLAY0RRB	0x448019BC	debug registers.. count overlay0 current frame number of returned burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGLSTOVERLAY0RRB	0x448019C0	debug registers.. count overlay0 last frame number of returned burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGTOTOVERLAY1REQ	0x448019C4	debug registers.. count overlay1 current frame number of requested burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGLSTOVERLAY1REQ	0x448019C8	debug registers.. count overlay1 last frame number of requested burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGTOTOVERLAY1RRB	0x448019CC	debug registers.. count overlay1 current frame number of returned burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGLSTOVERLAY1RRB	0x448019D0	debug registers.. count overlay1 last frame number of returned burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGTOTCURSORREQ	0x448019D4	debug registers.. count cursor current frame number of requested burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGLSTCURSORREQ	0x448019D8	debug registers.. count cursor last frame number of requested burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGTOTCURSORRRB	0x448019DC	debug registers.. count cursor current frame number of returned burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGLSTCURSORRRB	0x448019E0	debug registers.. count cursor last frame number of returned burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGTOTDCREQ	0x448019E4	debug registers.. count DC current frame number of requested burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGLSTDCREQ	0x448019E8	debug registers.. count DC last frame number of requested burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGTOTDCRRB	0x448019EC	debug registers.. count DC current frame number of returned burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGLSTDCRRB	0x448019F0	debug registers.. count DC last frame number of returned burst. READ ONLY
GFXSS_DC_DCNANO_GCREGDEBUGFRAMEANDMISFLAG	0x448019F4	debug registers. READ ONLY
GFXSS_MIPIDSI_MXMIPIDSI_CTL	0x44802000	IP control.
GFXSS_MIPIDSI_MXMIPIDSI_CLK_CTL	0x44802004	Clock control.
GFXSS_MIPIDSI_MXMIPIDSI_INTR	0x44802010	Interrupt status bits.
GFXSS_MIPIDSI_MXMIPIDSI_INTR_SET	0x44802014	Interrupt set bits.
GFXSS_MIPIDSI_MXMIPIDSI_INTR_MASK	0x44802018	Interrupt mask bits.
GFXSS_MIPIDSI_MXMIPIDSI_INTR_MASKED	0x4480201C	Interrupt masked bits.
GFXSS_MIPIDSI_MXMIPIDSI_DPI_CMD	0x44802020	DPI command control.

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_MIPIDSI_MXMIPIDSI_DBI_CMD	0x44802024	DBI command control.
GFXSS_MIPIDSI_MXMIPIDSI_PHY_FREQ_RANGE	0x44802030	PHY frequency range selection.
GFXSS_MIPIDSI_MXMIPIDSI_BIST	0x44802034	BIST control.
GFXSS_MIPIDSI_MXMIPIDSI_IO_CONTINUITY_TEST	0x44802038	IO continuity test control.
GFXSS_MIPIDSI_MXMIPIDSI_PLL_TEST_CONFIG1	0x4480203C	PLL-SoC interface configuration for Test.
GFXSS_MIPIDSI_MXMIPIDSI_PLL_TEST_CONFIG2	0x44802040	PLL-SoC interface configuration for Test.
GFXSS_MIPIDSI_MXMIPIDSI_PLL_TEST_OBS1	0x44802044	PLL Test Observation bits.
GFXSS_MIPIDSI_MXMIPIDSI_PLL_TEST_OBS2	0x44802048	PLL Test Observation bits.
GFXSS_MIPIDSI_MXMIPIDSI_LP_INTERNAL_LOOPBACK_TEST	0x4480204C	Low Power internal Loopback Test
GFXSS_MIPIDSI_DWCMIPIDSI_VERSION	0x44803000	Contains the version of the DSI host controller.
GFXSS_MIPIDSI_DWCMIPIDSI_PWR_UP	0x44803004	Controls the power up of the controller.
GFXSS_MIPIDSI_DWCMIPIDSI_CLKMGR_CFG	0x44803008	Configures the factor for internal dividers to divide lanebyteclk for timeout purposes.
GFXSS_MIPIDSI_DWCMIPIDSI_DPI_VCID	0x4480300C	Configures the Virtual Channel ID for DPI traffic.
GFXSS_MIPIDSI_DWCMIPIDSI_DPI_COLOR_CODING	0x44803010	Configures DPI color coding.
GFXSS_MIPIDSI_DWCMIPIDSI_DPI_CFG_POL	0x44803014	Configures the polarity of DPI signals.
GFXSS_MIPIDSI_DWCMIPIDSI_DPI_LP_CMD_TIM	0x44803018	Configures the timing for low-power commands sent while in video mode.
GFXSS_MIPIDSI_DWCMIPIDSI_DBI_VCID	0x4480301C	Configures Virtual Channel ID for DBI traffic.
GFXSS_MIPIDSI_DWCMIPIDSI_DBI_CFG	0x44803020	Configures the bit width of pixels for DBI.
GFXSS_MIPIDSI_DWCMIPIDSI_DBI_PARTITIONING_EN	0x44803024	Configures whether DWC_mipi_dsi_host is to partition DBI traffic automatically.
GFXSS_MIPIDSI_DWCMIPIDSI_DBI_CMDSIZE	0x44803028	Configures the command size and the size for automatic partitioning of DBI packets.
GFXSS_MIPIDSI_DWCMIPIDSI_PCKHDL_CFG	0x4480302C	Configures how EoTp, BTA, CRC and ECC are to be used, to meet peripherals characteristics
GFXSS_MIPIDSI_DWCMIPIDSI_GEN_VCID	0x44803030	Configures the Virtual Channel ID of READ responses to store and return to Generic interface.
GFXSS_MIPIDSI_DWCMIPIDSI_MODE_CFG	0x44803034	Configures the mode of operation between Video or Command Mode. (Commands can still be sent while in video mode.)

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_MIPIDSI_DWCMIPIDSI_VID_MODE_CFG	0x44803038	Configures several aspects of Video mode operation, the transmission mode, switching to low-power in the middle of a frame, enabling acknowledge and whether to send commands in low-power.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_PKT_SIZE	0x4480303C	Configures the video packet size.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_NUM_CHUNKS	0x44803040	Configures the number of chunks to use. The data in each chunk has the size provided by VID_PKT_SIZE.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_NULL_SIZE	0x44803044	Configures the size of null packets.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_HSA_TIME	0x44803048	Configures the video HSA time.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_HBP_TIME	0x4480304C	Configures the video HBP time.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_HLINE_TIME	0x44803050	Configures the overall time for each video line.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_VSA_LINES	0x44803054	Configures the VSA period.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_VBP_LINES	0x44803058	Configures the VBP period.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_VFP_LINES	0x4480305C	Configures the VFP period.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_VACTIVE_LINES	0x44803060	Configures the vertical resolution of video.
GFXSS_MIPIDSI_DWCMIPIDSI_CMD_MODE_CFG	0x44803068	Configures several aspect of command mode operation, tearing effect, acknowledge for each packet and the speed mode to transmit each Data Type related to commands.
GFXSS_MIPIDSI_DWCMIPIDSI_GEN_HDR	0x4480306C	Sets the header for new packets sent using the Generic interface.
GFXSS_MIPIDSI_DWCMIPIDSI_GEN_PLD_DATA	0x44803070	Sets the payload for packets sent using the Generic interface and, when read returns the contents of READ responses from the peripheral.
GFXSS_MIPIDSI_DWCMIPIDSI_CMD_PKT_STATUS	0x44803074	Contains information about the status of FIFOs related to DBI and Generic interface.
GFXSS_MIPIDSI_DWCMIPIDSI_TO_CNT_CFG	0x44803078	Configures counters that trigger timeout errors. These are used to warn the system of a failure, through an interrupt, and restart the controller in case of unexpected situations that cause deadlock conditions.
GFXSS_MIPIDSI_DWCMIPIDSI_HS_RD_TO_CNT	0x4480307C	Configures the Peripheral Response timeout after high-speed Read operations.

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_MIPIDSI_DWCMIPIDSI_LP_RD_TO_CNT	0x44803080	Configures the Peripheral Response timeout after low-power Read operations.
GFXSS_MIPIDSI_DWCMIPIDSI_HS_WR_TO_CNT	0x44803084	Configures the Peripheral Response timeout after high-speed Write operations.
GFXSS_MIPIDSI_DWCMIPIDSI_LP_WR_TO_CNT	0x44803088	Configures the Peripheral Response timeout after low-power Write operations.
GFXSS_MIPIDSI_DWCMIPIDSI_BTA_TO_CNT	0x4480308C	Configures the Peripheral Response timeout after Bus Turnaround completion.
GFXSS_MIPIDSI_DWCMIPIDSI_SDF_3D	0x44803090	Stores 3D control information for VSS packets in video mode.
GFXSS_MIPIDSI_DWCMIPIDSI_LPCLK_CTRL	0x44803094	Configures the possibility for using non continuous clock in the clock lane.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TMR_LPCLK_CFG	0x44803098	Sets the time that DWC_mipi_dsi_host assumes in calculations for the clock lane to switch between high-speed and low-power.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TMR_CFG	0x4480309C	Sets the time that DWC_mipi_dsi_host assumes in calculations for the data lanes to switch between high-speed and low-power.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_RSTZ	0x448030A0	Controls resets and the PLL of the D-PHY.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_IF_CFG	0x448030A4	Configures the number of active lanes and the minimum time to remain in stop state.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_ULPS_CTRL	0x448030A8	Configures entering and leaving ULPS in the D-PHY.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TX_TRIGGERS	0x448030AC	Configures the pins that activate triggers in the D-PHY.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_STATUS	0x448030B0	Contains information about the status of the D-PHY.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TST_CTRL0	0x448030B4	Controls clock and clear pins of the D-PHY vendor specific interface.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TST_CTRL1	0x448030B8	Controls data and enable pins of the D-PHY vendor specific interface.
GFXSS_MIPIDSI_DWCMIPIDSI_INT_ST0	0x448030BC	Contains the status of interrupt sources from acknowledge reports and the D-PHY.
GFXSS_MIPIDSI_DWCMIPIDSI_INT_ST1	0x448030C0	Contains the status of interrupt sources related to timeouts, ECC, CRC, packet size, EoTp, Generic and DBI interfaces.
GFXSS_MIPIDSI_DWCMIPIDSI_INT_MSK0	0x448030C4	Configures masks for the sources of interrupts that affect the INT_ST0 register. Write 1 to un-mask each error report.
GFXSS_MIPIDSI_DWCMIPIDSI_INT_MSK1	0x448030C8	Configures masks for the sources of interrupts that affect the INT_ST1 register.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_CAL	0x448030CC	Controls the skew calibration of D-PHY.

Graphics Subsystem (GFXSS) registers

Register name	Address	Description
GFXSS_MIPIDSI_DWCMIPIDSI_INT_FORCE0	0x448030D8	Forces interrupt that affect the INT_ST0 register.
GFXSS_MIPIDSI_DWCMIPIDSI_INT_FORCE1	0x448030DC	Forces interrupts that affect the INT_ST1 register.
GFXSS_MIPIDSI_DWCMIPIDSI_DSC_PARAMETER	0x448030F0	Configures Display Stream Compression.
GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TMR_RD_CFG	0x448030F4	Configures times related to PHY to perform some operations in lane byte clock cycles.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_SHADOW_CTRL	0x44803100	Controls dpi shadow feature
GFXSS_MIPIDSI_DWCMIPIDSI_DPI_VCID_ACT	0x4480310C	Holds the value that controller is using for DPI_VCID.
GFXSS_MIPIDSI_DWCMIPIDSI_DPI_COLOR_CODING_ACT	0x44803110	Holds the value that controller is using for DPI_COLOR_CODING.
GFXSS_MIPIDSI_DWCMIPIDSI_DPI_LP_CMD_TIM_ACT	0x44803118	Holds the value that controller is using for DPI_LP_CMD_TIM.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_MODE_CFG_ACT	0x44803138	Holds the value that controller is using for VID_MODE_CFG.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_PKT_SIZE_ACT	0x4480313C	Holds the value that controller is using for VID_PKT_SIZE.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_NUM_CHUNKS_ACT	0x44803140	This register holds the value that controller is using for VID_NUM_CHUNKS.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_NULL_SIZE_ACT	0x44803144	Holds the value that controller is using for VID_NULL_SIZE.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_HSA_TIME_ACT	0x44803148	Holds the value that controller is using for VID_HSA_TIME.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_HBP_TIME_ACT	0x4480314C	Holds the value that controller is using for VID_HBP_TIME.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_HLINE_TIME_ACT	0x44803150	Holds the value that controller is using for VID_HLINE_TIME.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_VSA_LINES_ACT	0x44803154	Holds the value that controller is using for VID_VSA_LINES.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_VBP_LINES_ACT	0x44803158	Holds the value that controller is using for VID_VBP_LINES.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_VFP_LINES_ACT	0x4480315C	Holds the value that controller is using for VID_VFP_LINES.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_VACTIVE_LINES_ACT	0x44803160	Holds the value that controller is using for VID_VACTIVE_LINES.
GFXSS_MIPIDSI_DWCMIPIDSI_VID_PKT_STATUS	0x44803168	Contains information about the status of FIFOs related to DPI and eDPI interfaces.
GFXSS_MIPIDSI_DWCMIPIDSI_SDF_3D_ACT	0x44803190	Holds the value that controller is using for SDF_3D.

27.1.1 GFXSS_GPU_MXGPU_CTL

Description: IP control.

Address: 0x44800000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	IP enable bit. When disabled (value 0), the functional state of the GCNano core is reset and its clock input gated. Access to MMIO of the core results in an AHB error response. Note, that the effect of this bit is delayed (see STATUS.CORE_RST). The core must be idle (no outstanding or pending AXI transactions) before clearing this bit. Default Value: 0

27.1.2 GFXSS_GPU_MXGPU_STATUS

Description: IP status.

Address: 0x4480000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							CORE_RST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CORE_RST	Reset state of the GCNano core (1 = in reset). This state is delayed to GFXSS_GPU reset. After reset de-activation it has to be checked for value 0 before the core can be used. After activation it has to be checked for value 1 before turning off the external clk_hf source. Default Value: 1

27.1.3 GFXSS_GPU_MXGPU_INTR

Description: Interrupt status bits.

Address: 0x44800010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1C
HW Access	Reserved							RW1SC
Name	Reserved [7:1]							CORE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CORE	GCNanoLiteV core has signalled an interrupt. Writing a '1' to this field will reset the bit. Interrupt stats inside the core is not affected by this. Default Value: 0

27.1.4 GFXSS_GPU_MXGPU_INTR_SET

Description: Interrupt set bits.

Address: 0x44800014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							CORE_SET

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CORE_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

27.1.5 GFXSS_GPU_MXGPU_INTR_MASK

Description: Interrupt mask bits.

Address: 0x44800018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							CORE_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CORE_MASK	Mask for corresponding field in INTR register. Default Value: 0

27.1.6 GFXSS_GPU_MXGPU_INTR_MASKED

Description: Interrupt masked bits.

Address: 0x4480001C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							CORE_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CORE_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0

27.1.7 GFXSS_GPU_GCNANO_AQHICLOCKCONTROL

Description: Clock Control Register.

Address: 0x44800800

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						RW	RW
HW Access	R						R	R
Name	AQHICLOCKCONTROL_FSCALE_VAL [7:2]						AQHI-CLOCK-CONTROL_CLK2D_DIS	AQHI-CLOCK-CONTROL_RE-SERVED_1

Bits	15	14	13	12	11	10	9	8
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access	W	R	R	R	R	R	R	R
Name	AQHI-CLOCK-CONTROL_RE-SERVED_3	AQHI-CLOCK-CONTROL_RE-SERVED_2	AQHI-CLOCK-CONTROL_DIS-ABLE_RAM_POW-ER_OPTI-MIZATION	AQHI-CLOCK-CONTROL_SOFT_RE-SET	AQHI-CLOCK-CONTROL_DIS-ABLE_DE-BUG_REGI STERS	AQHI-CLOCK-CONTROL_DIS-ABLE_RAM_CLOCK_-GATING	AQHI-CLOCK-CONTROL_FSCALE_C-MD_LOAD	AQHI-CLOCK-CONTROL_FS-CALE_VAL

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	R	R	R
HW Access	R				R	W	W	W
Name	AQHICLOCKCONTROL_RESERVED_4 [23:20]				AQHI-CLOCK-CONTROL_ISO-LATE_GPU	AQHI-CLOCK-CONTROL_IDLE_VG	AQHI-CLOCK-CONTROL_IDLE2_D	AQHI-CLOCK-CONTROL_IDLE3_D

Bits	31	30	29	28	27	26	25	24
SW Access	R			RW				
HW Access	W			R				
Name	AQHICLOCKCONTROL_RESERVED_5 [31:29]			AQHICLOCKCONTROL_RESERVED_4 [28:24]				

Bits	Name	Description
31 : 29	AQHICLOCKCON-TROL_RESERVED_5	Reserved Default Value: 0x0
28 : 20	AQHICLOCKCON-TROL_RESERVED_4	Reserved Default Value: 0x000
19	AQHICLOCKCON-TROL_ISOLATE_GPU	Reserved Default Value: 0x0
18	AQHICLOCKCON-TROL_IDLE_VG	VG pipe is idle: 0=Busy: 1=Idle or not present Default Value: 0x1
17	AQHICLOCKCON-TROL_IDLE2_D	2D pipe is idle or not present: 0=Busy: 1=Idle or not present Default Value: 0x1

27.1.7 GFXSS_GPU_GCNANO_AQHICLOCKCONTROL (continued)

16	AQHICLOCKCON-TROL_IDLE3_D	3D pipe is idle or not present: 0=Busy: 1=Idle or not present Default Value: 0x1
15	AQHICLOCKCON-TROL_RESERVED_3	Reserved Default Value: 0x0
14	AQHICLOCKCON-TROL_RESERVED_2	Reserved Default Value: 0x0
13	AQHICLOCKCONTROL_-DISABLE_RAM_POW-ER_OPTIMIZATION	Reserved Default Value: 0x0
12	AQHICLOCKCONTROL_-SOFT_RESET	Soft resets the IP. Write 1 to reset, defaults to 0 after reset. Default Value: 0x0
11	AQHICLOCKCONTROL_-DISABLE_DEBUG_REG-ISTERS	0=Enable debug registers 1=Disable debug registers Default Value: 0x1
10	AQHICLOCKCONTROL_-DISABLE_RAM_CLOCK_-GATING	RAM clock gating: 0=automatic turn off RAM clock when RAM not accessed; 1=ram clock always on Default Value: 0x0
9	AQHICLOCKCON-TROL_FSCALE_CMD_-LOAD	Core clock frequency scale value enable. When writing a 1 to this bit, it updates the frequency scale factor with the value FSCALE_VAL[6:0]. The bit must be set back to 0 after that. If this bit is set and FSCALE_VAL=0 (an invalid combination), the HREADYOUT output signal will get stuck to 0. Default Value: 0x0
8 : 2	AQHICLOCKCON-TROL_FSCALE_VAL	Core clock frequency scale value. Default Value: 0x40
1	AQHICLOCKCONTROL_-CLK2D_DIS	Disable 2D/VG clock when set to 1. CLK2D_DIS should be controlled by software. The AXI interface clock is the only block not stalled at that point. 0: VG clock on 1:VG clock off Default Value: 0x0
0	AQHICLOCKCON-TROL_RESERVED_1	Reserved Default Value: 0x0

27.1.8 GFXSS_GPU_GCNANO_AQHIIDLE

Description: Idle Status Register.

Address: 0x44800804

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	AQHI-IDLE_IDLE_TX	AQHI-IDLE_IDLE_RA	AQHI-IDLE_IDLE_SE	AQHI-IDLE_IDLE_PA	AQHI-IDLE_IDLE_SH	AQHI-IDLE_IDLE_PE	AQHI-IDLE_IDLE_DE	AQHI-IDLE_IDLE_FE

Bits	15	14	13	12	11	10	9	8
SW Access	R			R	R	R	R	R
HW Access	W			W	W	W	W	W
Name	AQHIIDLE_UNUSED [15:13]			AQHI-IDLE_IDLE_BLT	AQHI-IDLE_IDLE_TS	AQHI-IDLE_IDLE_FP	AQHI-IDLE_IDLE_IM	AQHI-IDLE_IDLE_VG

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	AQHIIDLE_UNUSED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R						
HW Access	W	W						
Name	AQHI-IDLE_AXI_LP	AQHIIDLE_UNUSED [30:24]						

Bits	Name	Description
31	AQHIIDLE_AXI_LP	AXI low power mode: 0=not in low power mode; 1=in low power mode. Using the AXI low power interface to make the GPU enter a low power mode will set this bit to 1. Default Value: 0x0
30 : 13	AQHIIDLE_UNUSED	Reserved Default Value: 0x3FFFF
12	AQHIIDLE_IDLE_BLT	Reserved Default Value: 0x1
11	AQHIIDLE_IDLE_TS	TS (Tessellation Engine): 0=Busy: 1=Idle or not present Default Value: 0x1
10	AQHIIDLE_IDLE_FP	Reserved Default Value: 0x1
9	AQHIIDLE_IDLE_IM	IM (Image Engine): 1= IM is idle: 0=Busy: 1=Idle or not present Default Value: 0x1
8	AQHIIDLE_IDLE_VG	VG (Vector Graphics Engine): 1= VG is idle: 0=Busy: 1=Idle or not present Default Value: 0x1
7	AQHIIDLE_IDLE_TX	Reserved Default Value: 0x1

27.1.8 GFXSS_GPU_GCNANO_AQHIIDLE (continued)

6	AQHIIDLE_IDLE_RA	Reserved Default Value: 0x1
5	AQHIIDLE_IDLE_SE	Reserved Default Value: 0x1
4	AQHIIDLE_IDLE_PA	Reserved Default Value: 0x1
3	AQHIIDLE_IDLE_SH	Reserved Default Value: 0x1
2	AQHIIDLE_IDLE_PE	PE (Pixel Engine): 0=Busy: 1=Idle or not present Default Value: 0x1
1	AQHIIDLE_IDLE_DE	Reserved Default Value: 0x1
0	AQHIIDLE_IDLE_FE	FE (Fetch Engine): 0=FE is busy; 1=FE is idle. Default Value: 0x1

27.1.9 GFXSS_GPU_GCNANO_AQAXICONFIG

Description: AXI Configuration Register.

Address: 0x44800808

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AQAXICONFIG_RESERVED_1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	AQAXICONFIG_ARCACHE [15:12]				AQAXICONFIG_AWCACHE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW		RW	
HW Access	R				R		R	
Name	AQAXICONFIG_AXCACHE_OVERRIDE_SHARED [23:20]				AQAXICONFIG_AXDOMAIN_NON_SHARED [19:18]		AQAXICONFIG_AXDOMAIN_SHARED [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	AQAXICONFIG_RESERVED_2 [31:24]							

Bits	Name	Description
31 : 24	AQAXICONFIG_RESERVED_2	Reserved Default Value: 0x00
23 : 20	AQAXICONFIG_AXCACHE_OVERRIDE_SHARED	Configure AxCACHE value for shareable request. Not used for VG cores Default Value: 0x2
19 : 18	AQAXICONFIG_AXDOMAIN_NON_SHARED	Configure AxDOMAIN value for non-shareable request. Not used for VG cores Default Value: 0x0
17 : 16	AQAXICONFIG_AXDOMAIN_SHARED	Configure AxDOMAIN value for shareable request. Not used for VG cores Default Value: 0x2
15 : 12	AQAXICONFIG_ARCACHE	Set ARCACHE[3:0] value. Default Value: 0x2
11 : 8	AQAXICONFIG_AWCACHE	Set AWCACHE[3:0] value. Default Value: 0x2
7 : 0	AQAXICONFIG_RESERVED_1	Reserved Default Value: 0x00

27.1.10 GFXSS_GPU_GCNANO_AQAXISTATUS

Description: AXI Status Register. READ ONLY. Back-to-back read is forbidden to this register and can cause system hang. Please insert delay (nop operation) between two consecutive reads while accessing this register outside of VSI drivers.

Address: 0x4480080C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	AQAXISTATUS_RD_ERR_ID [7:4]				AQAXISTATUS_WR_ERR_ID [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R						R	R
HW Access	W						W	W
Name	AQAXISTATUS_RESERVED [15:10]						AQAXISTA-TUS_DE-T_RD_ERR	AQAXISTA-TUS_DE-T_WR_ERR

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	AQAXISTATUS_RESERVED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	AQAXISTATUS_RESERVED [31:24]							

Bits	Name	Description
31 : 10	AQAXISTATUS_RE-SERVED	Reserved Default Value: 0x000000
9	AQAXISTATUS_DE-T_RD_ERR	1=A read error is detected. Default Value: 0x0
8	AQAXISTATUS_DE-T_WR_ERR	1=A write error is detected. Default Value: 0x0
7 : 4	AQAXISTATUS_RD_ER-R_ID	The ID which caused illegal read access error. Default Value: 0x0
3 : 0	AQAXISTATUS_WR_ER-R_ID	The ID which caused illegal write access error. Default Value: 0x0

27.1.11 GFXSS_GPU_GCNANO_AQINTRACKNOWLEDGE

Description: Interrupt Acknowledge Register. Each bit represents a corresponding event being triggered. Reading from this register clears the outstanding interrupt. READ ONLY. When the access comes from a debugger (HMASTER[0] == 1), the clear by read function is disabled. Back-to-back read is forbidden to this register and can cause system hang. Please insert delay (nop operation) between two consecutive reads while accessing this register outside of VSI drivers.

Address: 0x44800810

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	AQINTRACKNOWLEDGE_INTR_VEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	AQINTRACKNOWLEDGE_INTR_VEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	AQINTRACKNOWLEDGE_INTR_VEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	AQINTRACKNOWLEDGE_INTR_VEC [31:24]							

Bits	Name	Description
31 : 0	AQINTRACKNOWL-EDGE_INTR_VEC	For each interrupt event, 0=Clear, 1=Interrupt Active. For all cores: Bit 31 is AXI_BUS_ERROR. 0=No error, 1=Interrupt Active. Default Value: 0x00000000

27.1.12 GFXSS_GPU_GCNANO_AQINTRENBL

Description: Interrupt Enable Register. Each bit enables a corresponding event.

Address: 0x44800814

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AQINTRENBL_INTR_ENBL_VEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	AQINTRENBL_INTR_ENBL_VEC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	AQINTRENBL_INTR_ENBL_VEC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	AQINTRENBL_INTR_ENBL_VEC [31:24]							

Bits	Name	Description
31 : 0	AQINTRENBL_INTR_ENBL_VEC	0=Disable Interrupt; 1=Enable interrupt. Default Value: 0x00000000

27.1.13 GFXSS_GPU_GCNANO_GCCHIPREV

Description: Chip Revsion Register. Shows the revision for the chip in BCD. This register has no set reset value. It varies with the implementation. READ ONLY.

Address: 0x44800824

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCCHIPREV_REV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCCHIPREV_REV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCCHIPREV_REV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCCHIPREV_REV [31:24]							

Bits	Name	Description
31 : 0	GCCHIPREV_REV	Revision. This value may vary between releases and can be ignored during test. Default Value: Undefined

27.1.14 GFXSS_GPU_GCNANO_GCCHIPDATE

Description: Chip Date Register. Shows the release date for the IP in YYYYMMDD (year/month/day) format. This register has no set reset value. It varies with the implementation. READ ONLY.

Address: 0x44800828

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCCHIPDATE_DATE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCCHIPDATE_DATE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCCHIPDATE_DATE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCCHIPDATE_DATE [31:24]							

Bits	Name	Description
31 : 0	GCCHIPDATE_DATE	Date. This value will vary each release and can be ignored during test. Default Value: Undefined

27.1.15 GFXSS_GPU_GCNANO_GCREGHICHIPPATCHREV

Description: Chip Patch Revision Register. Patch revision level for the chip. It varies per release. READ ONLY

Address: 0x44800898

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGHICHIPPATCHREV_PATCH_REV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGHICHIPPATCHREV_RESERVED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGHICHIPPATCHREV_RESERVED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGHICHIPPATCHREV_RESERVED [31:24]							

Bits	Name	Description
31 : 8	GCREGHICHIP-PATCHREV_RESERVED	Reserved Default Value: 0x000000
7 : 0	GCREGHICHIP-PATCHREV_-PATCH_REV	Patch Revision. This value will vary each release and can be ignored during test. Default Value: Undefined

27.1.16 GFXSS_GPU_GCNANO_GCPRODUCTID

Description: Product Identification Register. Shows Product ID. READ ONLY.

Address: 0x448008A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	GCPRODUCTID_NUM [7:4]				GCPRODUCTID_GRADE_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCPRODUCTID_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCPRODUCTID_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	GCPRODUCTID_RESERVED [31:28]				GCPRODUCTID_TYPE [27:24]			

Bits	Name	Description
31 : 28	GCPRODUCTID_RESERVED	Reserved Default Value: 0x0
27 : 24	GCPRODUCTID_TYPE	Product Type is 3: VG (Vector Graphics). Default Value: 0x3
23 : 4	GCPRODUCTID_NUM	Product number is 265. Default Value: 0x00265
3 : 0	GCPRODUCTID_GRADE_LEVEL	0:None-no extra letter on the product name for this core; 1:Nano; 5:NanoUltra. Default Value: 0x5

27.1.17 GFXSS_GPU_GCNANO_GCMODULEPOWERCONTROLS

Description: Module Power Control Register. Control register for module level power controls.

Address: 0x44800900

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				R	RW	RW	RW
HW Access	R				W	R	R	R
Name	GCMODULEPOWERCONTROLS_TURN_ON_COUNTER [7:4]				GCMODULEPOWERCONTROLS_RESERVED_1	GCMODULEPOWERCONTROLS_DISABLE_STARVE_MODULE_CLOCK_GATING	GCMODULEPOWERCONTROLS_DISABLE_STALL_MODULE_CLOCK_GATING	GCMODULEPOWERCONTROLS_ENABLE_MODULE_CLOCK_GATING

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCMODULEPOWERCONTROLS_RESERVED_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCMODULEPOWERCONTROLS_TURN_OFF_COUNTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCMODULEPOWERCONTROLS_TURN_OFF_COUNTER [31:24]							

Bits	Name	Description
31 : 16	GCMODULEPOWERCONTROLS_TURN_OFF_COUNTER	Counter value for clock gating the module if the module is idle for this amount of clock cycles. Default Value: 0x0014
15 : 8	GCMODULEPOWERCONTROLS_RESERVED_2	Reserved Default Value: 0x00
7 : 4	GCMODULEPOWERCONTROLS_TURN_ON_COUNTER	Number of clock cycles to wait after turning on the clock: 0-15 cycles Default Value: 0x2
3	GCMODULEPOWERCONTROLS_RESERVED_1	Reserved Default Value: 0x0
2	GCMODULEPOWERCONTROLS_DISABLE_STARVE_MODULE_CLOCK_GATING	Disables module level clock gating for starve/idle condition:0=module clock can be turned off for starve/idle condition 1=module clock can not be turned off for starve/idle condition Default Value: 0x0

27.1.17 GFXSS_GPU_GCNANO_GCMODULEPOWERCONTROLS (continued)

1	GCMODULEPOWER-CONTROLS_DIS-ABLE_STALL_MODULE_CLOCK_GATING	Disables module level clock gating for stall condition: 0=module clock can be turned off for stall condition 1=module clock can not be turned off for stall condition Default Value: 0x0
0	GCMODULEPOWER-CONTROLS_ENABLE_-MODULE_CLOCK_GATING	0=module clock always on 1=If the corresponding bit in GCMODULEPOWERMODULECONTROL is configured as 0, the clock will be turned off when the module is not working. Default Value: 0x0

27.1.18 GFXSS_GPU_GCNANO_GCMODULEPOWERMODULECONTROL

Description: Module Power Module Control Register. Module level control register.

Address: 0x44800904

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	GCMODULEPOWERMODULECONTROL_RESERVED_2 [7:3]					GCMODULEPOWERMODULECONTROL_DISABLE_MODULE_CLOCK_GATING_PE	GCMODULEPOWERMODULECONTROL_RESERVED_1	GCMODULEPOWERMODULECONTROL_DISABLE_MODULE_CLOCK_GATING_FE

Bits	15	14	13	12	11	10	9	8
SW Access	R			R	RW	RW	RW	RW
HW Access	W			W	R	R	R	R
Name	GCMODULEPOWERMODULECONTROL_RESERVED_4 [15:13]			GCMODULEPOWERMODULECONTROL_DISABLE_MODULE_CLOCK_GATING_FLEXA	GCMODULEPOWERMODULECONTROL_DISABLE_MODULE_CLOCK_GATING_TS	GCMODULEPOWERMODULECONTROL_RESERVED_3	GCMODULEPOWERMODULECONTROL_DISABLE_MODULE_CLOCK_GATING_IM	GCMODULEPOWERMODULECONTROL_DISABLE_MODULE_CLOCK_GATING_VG

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCMODULEPOWERMODULECONTROL_RESERVED_4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCMODULEPOWERMODULECONTROL_RESERVED_4 [31:24]							

Bits	Name	Description
31 : 13	GCMODULEPOWERMODULECONTROL_RESERVED_4	Reserved Default Value: 0x00000
12	GCMODULEPOWERMODULECONTROL_DISABLE_MODULE_CLOCK_GATING_FLEXA	Reserved Default Value: 0x0

27.1.18 GFXSS_GPU_GCNANO_GCMODULEPOWERMODULECONTROL (continued)

11	GCMODULEPOWER-MODULECONTROL_DIS-ABLE_MODULE_CLOCK _GATING_TS	Disables module level clock gating for TS(Tessellation Engine): 0=the module clock can be turned off when the module not working 1=the module clock always on Default Value: 0x0
10	GCMODULEPOWER-MODULECONTROL_RE-SERVED_3	Reserved Default Value: 0x0
9	GCMODULEPOWER-MODULECONTROL_DIS-ABLE_MODULE_CLOCK _GATING_IM	Disables module level clock gating for IM(Image Engine): 0=the module clock can be turned off when the module not working 1=the module clock always on Default Value: 0x0
8	GCMODULEPOWER-MODULECONTROL_DIS-ABLE_MODULE_CLOCK _GATING_VG	Disables module level clock gating for VG(Vector Graphics Engine): 0=the module clock can be turned off when the module not working 1=the module clock always on Default Value: 0x0
7 : 3	GCMODULEPOWER-MODULECONTROL_RE-SERVED_2	Reserved Default Value: 0x00
2	GCMODULEPOWER-MODULECONTROL_DIS-ABLE_MODULE_CLOCK _GATING_PE	Disables module level clock gating for PE(Pixel Engine) : 0=the module clock can be turned off when the module not working 1=the module clock always on Default Value: 0x0
1	GCMODULEPOWER-MODULECONTROL_RE-SERVED_1	Reserved Default Value: 0x0
0	GCMODULEPOWER-MODULECONTROL_DIS-ABLE_MODULE_CLOCK _GATING_FE	Disables module level clock gating for FE(Fetch Engine): 0=the module clock can be turned off when the module not working 1=the module clock always on Default Value: 0x0

27.1.19 GFXSS_GPU_GCNANO_GCMODULEPOWERMODULESTATUS

Description: Module Power Module Status Register. Module level control status.

Address: 0x44800908

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R					R	R	R
HW Access	W					W	W	W
Name	GCMODULEPOWERMODULESTATUS_RESERVED_2 [7:3]					GCMODULEPOWERMODULESTATUS_MODULE_CLOCK_GATED_PE	GCMODULEPOWERMODULESTATUS_RESERVED_1	GCMODULEPOWERMODULESTATUS_MODULE_CLOCK_GATED_FE

Bits	15	14	13	12	11	10	9	8
SW Access	R			R	R	Reserved	R	R
HW Access	W			W	W	Reserved	W	W
Name	GCMODULEPOWERMODULESTATUS_RESERVED_3 [15:13]			GCMODULEPOWERMODULESTATUS_MODULE_CLOCK_GATED_FLEXA	GCMODULEPOWERMODULESTATUS_MODULE_CLOCK_GATED_TS	Reserved	GCMODULEPOWERMODULESTATUS_MODULE_CLOCK_GATED_IM	GCMODULEPOWERMODULESTATUS_MODULE_CLOCK_GATED_VG

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCMODULEPOWERMODULESTATUS_RESERVED_3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCMODULEPOWERMODULESTATUS_RESERVED_3 [31:24]							

Bits	Name	Description
31 : 13	GCMODULEPOWERMODULESTATUS_RESERVED_3	Reserved Default Value: 0x00000
12	GCMODULEPOWERMODULESTATUS_MODULE_CLOCK_GATED_FLEXA	Reserved Default Value: 0x0
11	GCMODULEPOWERMODULESTATUS_MODULE_CLOCK_GATED_TS	Module level clock gating is ON for TS: 0=TS module clock is turned on. 1=TS module clock is turned off. Default Value: 0x0
9	GCMODULEPOWERMODULESTATUS_MODULE_CLOCK_GATED_IM	Module level clock gating is ON for IM: 0=IM module clock is turned on. 1=IM module clock is turned off. Default Value: 0x0

27.1.19 GFXSS_GPU_GCNANO_GCMODULEPOWERMODULESTATUS (continued)

8	GCMODULEPOWER-MODULESTATUS_MOD-ULE_CLOCK_GATED_VG	Module level clock gating is ON for VG: 0=VG module clock is turned on. 1=VG module clock is turned off. Default Value: 0x0
7 : 3	GCMODULEPOWER-MODULESTATUS_RE-SERVED_2	Reserved Default Value: 0x00
2	GCMODULEPOWER-MODULESTATUS_MOD-ULE_CLOCK_GATED_PE	Module level clock gating is ON for PE: 0=PE module clock is turned on. 1=PE module clock is turned off. Default Value: 0x0
1	GCMODULEPOWER-MODULESTATUS_RE-SERVED_1	Reserved Default Value: 0x0
0	GCMODULEPOWER-MODULESTATUS_MOD-ULE_CLOCK_GATED_FE	Module level clock gating is ON for FE: 0=FE module clock is turned on. 1=FE module clock is turned off. Default Value: 0x0

27.1.20 GFXSS_GPU_GCNANO_AQMEMORYDEBUG

Description: Memory Debug Register.

Address: 0x44800C14

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AQMEMORYDEBUG_MAX_OUTSTANDING_READS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	AQMEMORYDEBUG_RESERVED_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW					R		RW
HW Access	R					W		R
Name	AQMEMORYDEBUG_RESERVED_4 [23:19]					AQMEMORYDEBUG_RESERVED_3 [18:17]		AQMEMORYDEBUG_RESERVED_2

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	AQMEMORYDEBUG_RESERVED_5 [31:24]							

Bits	Name	Description
31 : 24	AQMEMORYDEBUG_RESERVED_5	Reserved Default Value: 0x00
23 : 19	AQMEMORYDEBUG_RESERVED_4	Reserved Default Value: 0x00
18 : 17	AQMEMORYDEBUG_RESERVED_3	Reserved Default Value: 0x0
16	AQMEMORYDEBUG_RESERVED_2	Reserved Default Value: 0x0
15 : 8	AQMEMORYDEBUG_RESERVED_1	Reserved Default Value: 0x00
7 : 0	AQMEMORYDEBUG_MAX_OUTSTANDING_READS	Limits the total number of outstanding read requests. Default Value: 0x00

27.1.21 GFXSS_GPU_GCNANO_AQREGISTERTIMINGCONTROL

Description: Timing Control Register.

Address: 0x44800C2C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AQREGISTERTIMINGCONTROL_FOR_RF1P [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	AQREGISTERTIMINGCONTROL_FOR_RF2P [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	AQREGISTERTIMINGCONTROL_RESERVED [23:21]			AQREGISTERTIMINGCONTROL_POWER_DOWN	AQREGISTERTIMINGCONTROL_FAST_WTC [19:18]		AQREGISTERTIMINGCONTROL_FAST_RTC [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	AQREGISTERTIMINGCONTROL_RESERVED [31:24]							

Bits	Name	Description
31 : 21	AQREGISTERTIMINGCONTROL_RESERVED	Reserved Default Value: 0x000
20	AQREGISTERTIMINGCONTROL_POWER_DOWN	Reserved Default Value: 0x0
19 : 18	AQREGISTERTIMINGCONTROL_FAST_WTC	Reserved Default Value: 0x0
17 : 16	AQREGISTERTIMINGCONTROL_FAST_RTC	Reserved Default Value: 0x3
15 : 8	AQREGISTERTIMINGCONTROL_FOR_RF2P	Reserved Default Value: 0x00
7 : 0	AQREGISTERTIMINGCONTROL_FOR_RF1P	Reserved Default Value: 0x00

27.1.22 GFXSS_GPU_GCNANO_GCREGFETCHADDRESS

Description: Fetch Command Buffer Base Address Register. Address of the command buffer. The address must be 64-byte aligned.

Address: 0x44800D00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						RW	
HW Access	R						R	
Name	GCREGFETCHADDRESS_ADDRESS [7:2]						GCREGFETCHAD-DRESS_TYPE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGFETCHADDRESS_ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGFETCHADDRESS_ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGFETCHADDRESS_ADDRESS [31:24]							

Bits	Name	Description
31 : 2	GCREGFETCHAD-DRESS_ADDRESS	fetch address Default Value: 0x00000000
1 : 0	GCREGFETCHAD-DRESS_TYPE	Type of address. Local is reserved for now. Default Value: 0x0 **0x0: SYSTEM :** (none) **0x2: VIRTUAL :** (none) **0x1: LOCAL :** (none)

27.1.23 GFXSS_GPU_GCNANO_GCREGFETCHCONTROL

Description: Fetch Control Register. Writing a non-zero value to this register starts the fetch engine. The FE will start fetching 64-bit commands and data starting at the address specified by the gcregFetchAddress register. Make sure this count is large enough to fetch the END command, otherwise the FE will wait until more data is coming.

Address: 0x44800D04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGFETCHCONTROL_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGFETCHCONTROL_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R			RW				
HW Access	W			R				
Name	GCREGFETCHCONTROL_RESERVED [23:21]			GCREGFETCHCONTROL_COUNT [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGFETCHCONTROL_RESERVED [31:24]							

Bits	Name	Description
31 : 21	GCREGFETCHCON-TROL_RESERVED	Reserved Default Value: 0x000
20 : 0	GCREGFETCHCON-TROL_COUNT	Number of 64-bit words to fetch. 21 bits is enough for 16 MB. Default Value: 0x000000

27.1.24 GFXSS_GPU_GCNANO_GCREGCURRENTFETCHADDRESS

Description: Current Fetch Command Address Register. Debugging register that defines the current address the FE is fetching data from. READ ONLY.

Address: 0x44800D08

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGCURRENTFETCHADDRESS_ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGCURRENTFETCHADDRESS_ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGCURRENTFETCHADDRESS_ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGCURRENTFETCHADDRESS_ADDRESS [31:24]							

Bits	Name	Description
31 : 0	GCREGCURRENT-FETCHADDRESS_AD-DRESS	(none) Default Value: 0x00000000

27.1.25 GFXSS_DC_MXDC_CTL

Description: IP control.

Address: 0x44801000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	IP enable bit. When disabled (value 0), the functional state of the DCNano core is reset and its clock input gated. Access to MMIO of the core results in an AHB error response. Note, that the effect of this bit is delayed (see STATUS.CORE_RST). The core must be idle (no outstanding or pending AXI transactions) before clearing this bit. Default Value: 0

27.1.26 GFXSS_DC_MXDC_CLK_CTL

Description: Clock control.

Address: 0x44801004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		Reserved					RW
HW Access	R		Reserved					R
Name	CLK_DIV [7:6]		Reserved [5:1]					CLK_CORE

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CLK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CLK_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CLK_DIV [31:24]							

Bits	Name	Description
31 : 6	CLK_DIV	Setup of the fractional divider to generate clk_hf_div. In DPI mode the output is the pixel clock. In DBI Type C mode it's two times the serial clock. Format of programmed value is unsigned fix-point 10.16. It must not be set to a value smaller than 2.0 (= 0x020000). It can be set to 0, which results in no clock being generated. Change only while CTL.ENABLED is off. Default Value: 0x80000
0	CLK_CORE	Setup for DC core and AXI clock. Must only be set to 0 if clk_hf is not faster than 200 MHz. Change only while CTL.ENABLED is off. Default Value: 1 **0x0: HF_DIV1 :** Core clock is clk_hf. **0x1: HF_DIV2 :** Core clock is clk_hf divided by 2.

27.1.27 GFXSS_DC_MXDC_IO_CTL

Description: IO enable control.

Address: 0x44801008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						SPI_S-DOEN	SPI_EN-ABLED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							DPI_EN-ABLED

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							DBI_EN-ABLED

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	DBI_ENABLED	Enable control for IO cells in DBI Type A/B mode (1 = enabled). CTL.ENABLED must also be 1. Default Value: 1
8	DPI_ENABLED	Enable control for IO cells in DPI mode (1 = enabled). CTL.ENABLED must also be 1. Default Value: 1
1	SPI_SDOEN	Controls if the enable for spi_dout is separately controlled by the DCNano core with dbiTypecS-doEn signal (0 = yes, 1 = no). Field has no effect if SPI_ENABLED is 0. Default Value: 1
0	SPI_ENABLED	Enable control for IO cells in DBI Type C mode (1 = enabled). CTL.ENABLED must also be 1. Default Value: 1

27.1.28 GFXSS_DC_MXDC_STATUS

Description: IP status.

Address: 0x4480100C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							CORE_RST

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CORE_RST	Reset state of the DCNano core (1 = in reset). This state is delayed to GFXSS_DC reset. After reset de-activation it has to be checked for value 0 before the core can be used. After activation it has to be checked for value 1 before turning off the external clk_hf source. Default Value: 1

27.1.29 GFXSS_DC_MXDC_INTR

Description: Interrupt status.

Address: 0x44801010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1C
HW Access	Reserved							RW1SC
Name	Reserved [7:1]							CORE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW1C	RW1C	RW1C	RW1C
HW Access	Reserved				RW1SC	RW1SC	RW1SC	RW1SC
Name	Reserved [15:12]				ADDR3	ADDR2	ADDR1	ADDR0

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW1C
HW Access	Reserved							RW1SC
Name	Reserved [23:17]							RLAD_ER-ROR

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	RLAD_ERROR	The RLAD decoder has entered fail state (see RLAD_STATUS register). Writing a '1' to this field will reset the bit. Default Value: 0
11	ADDR3	Read access to INT_ADDR3 completed. Writing a '1' to this field will reset the bit. Default Value: 0
10	ADDR2	Read access to INT_ADDR2 completed. Writing a '1' to this field will reset the bit. Default Value: 0
9	ADDR1	Read access to INT_ADDR1 completed. Writing a '1' to this field will reset the bit. Default Value: 0
8	ADDR0	Read access to INT_ADDR0 completed. Writing a '1' to this field will reset the bit. Default Value: 0
0	CORE	DCNano core has signalled an interrupt. Writing a '1' to this field will reset the bit. Interrupt status inside the core is not affected by this. Default Value: 0

27.1.30 GFXSS_DC_MXDC_INTR_SET

Description: Interrupt set bits.

Address: 0x44801014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							CORE_SET

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW1S	RW1S	RW1S	RW1S
HW Access	Reserved				A	A	A	A
Name	Reserved [15:12]				ADDR3_SET	ADDR2_SET	ADDR1_SET	ADDR0_SET

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [23:17]							RLAD_ERROR_SET

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	RLAD_ERROR_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
11	ADDR3_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
10	ADDR2_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
9	ADDR1_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
8	ADDR0_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
0	CORE_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

27.1.31 GFXSS_DC_MXDC_INTR_MASK

Description: Interrupt mask bits.

Address: 0x44801018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							CORE_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW	RW	RW	RW
HW Access	Reserved				R	R	R	R
Name	Reserved [15:12]				ADDR3_MASK	ADDR2_MASK	ADDR1_MASK	ADDR0_MASK

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							RLAD_ERROR_MASK

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	RLAD_ERROR_MASK	Mask for corresponding field in INTR register. Default Value: 0
11	ADDR3_MASK	Mask for corresponding field in INTR register. Default Value: 0
10	ADDR2_MASK	Mask for corresponding field in INTR register. Default Value: 0
9	ADDR1_MASK	Mask for corresponding field in INTR register. Default Value: 0
8	ADDR0_MASK	Mask for corresponding field in INTR register. Default Value: 0
0	CORE_MASK	Mask for corresponding field in INTR register. Default Value: 0

27.1.32 GFXSS_DC_MXDC_INTR_MASKED

Description: Interrupt masked bits.

Address: 0x4480101C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							CORE_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				R	R	R	R
HW Access	Reserved				W	W	W	W
Name	Reserved [15:12]				ADDR3_MASKED	ADDR2_MASKED	ADDR1_MASKED	ADDR0_MASKED

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [23:17]							RLAD_ERROR_MASKED

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	RLAD_ERROR_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
11	ADDR3_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
10	ADDR2_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
9	ADDR1_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
8	ADDR0_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
0	CORE_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0

27.1.33 GFXSS_DC_MXDC_ADDR0_INT

Description: Address 0 for interrupt generation.

Address: 0x44801020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR0_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR0_INT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR0_INT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR0_INT [31:24]							

Bits	Name	Description
31 : 0	ADDR0_INT	A completed read access to this memory address will set INTR.ADDR0. The shadow values of all address fields are copied into the active configuration when a display frame has completed and GCREGPANELCONTROL_VALID was set before in DCNANO. Default Value: 0

27.1.34 GFXSS_DC_MXDC_ADDR1_INT

Description: Address 1 for interrupt generation.

Address: 0x44801024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR1_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR1_INT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR1_INT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR1_INT [31:24]							

Bits	Name	Description
31 : 0	ADDR1_INT	A completed read access to this memory address will set INTR.ADDR1. Default Value: 0

27.1.35 GFXSS_DC_MXDC_ADDR2_INT

Description: Address 2 for interrupt generation.

Address: 0x44801028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR2_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR2_INT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR2_INT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR2_INT [31:24]							

Bits	Name	Description
31 : 0	ADDR2_INT	A completed read access to this memory address will set INTR.ADDR2. Default Value: 0

27.1.36 GFXSS_DC_MXDC_ADDR3_INT

Description: Address 3 for interrupt generation.

Address: 0x4480102C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR3_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR3_INT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR3_INT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR3_INT [31:24]							

Bits	Name	Description
31 : 0	ADDR3_INT	A completed read access to this memory address will set INTR.ADDR3. Default Value: 0

27.1.37 GFXSS_DC_MXDC_RLAD_CTL

Description: Control options for the RLAD decoder.

Address: 0x44801040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							RLAD_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						RLAD_LAYER [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 8	RLAD_LAYER	ID of the display layer to decode (0 = reserved, 1 = video, 2 = overlay 0, 3 = overlay 1). Default Value: 0
0	RLAD_ENABLE	When set to 0, the RLAD decoder is disabled. It's clock tree is gated and the functional logic reset. All RLAD configuration fields, including this enable field, are shadowed. The shadow values are copied into the active configuration when a display frame has completed and GCREGPANELCONTROL_VALID was set before in DCNANO. Once the load of shadows has been initiated by setting the VALID flag, the RLAD configuration fields must not be changed again before the frame complete interrupt. Beside inconsistent setup for a display frame, this can lead to data corruption of the active configuration. Default Value: 0

27.1.38 GFXSS_DC_MXDC_RLAD_IMG

Description: Properties of the uncompressed image.

Address: 0x44801044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RLAD_WIDTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW		Reserved		RW			
HW Access	R		Reserved		R			
Name	RLAD_HEIGHT [15:14]		Reserved [13:12]		RLAD_WIDTH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RLAD_HEIGHT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				Reserved		RW	
HW Access	R				Reserved		R	
Name	RLAD_FORMAT [31:28]				Reserved [27:26]		RLAD_HEIGHT [25:24]	

Bits	Name	Description
31 : 28	RLAD_FORMAT	Color format of the uncompressed image. The RLAD block converts the configured format after decompression to ARGB8888, which is the format the DC layer has to be configured for (in linear order and with component swizzle ARGB). Alpha value is set to 255 for RGB and GRAY formats. Default Value: 4 **0x1: ARGB4444 :** **0x2: ARGB1555 :** **0x3: RGB565 :** **0x4: ARGB8888 :** **0x5: RGB888 :** **0x6: RGB666 :** **0x7: RGB444 :** **0x8: GRAY8 :** **0x9: GRAY6 :**

27.1.38 GFXSS_DC_MXDC_RLAD_IMG (continued)

0xa: GRAY4 :

25 : 14	RLAD_HEIGHT	Height of the image in number of lines minus one. The DC layer must be setup for the same height. Default Value: 0
11 : 0	RLAD_WIDTH	Width of the image in number of pixels minus one. The DC layer must be setup for the same width. Default Value: 0

27.1.39 GFXSS_DC_MXDC_RLAD_ENC

Description: Configuration of the encoder that compressed the image.

Address: 0x44801048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						RLAD_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	RLAD_BITS_G [23:20]				RLAD_BITS_R [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	RLAD_BITS_A [31:28]				RLAD_BITS_B [27:24]			

Bits	Name	Description
31 : 28	RLAD_BITS_A	Max number of alpha channel bits (used for RLAD modes only). Default Value: 8
27 : 24	RLAD_BITS_B	Max number of blue channel bits (used for RLAD modes only). Default Value: 8
23 : 20	RLAD_BITS_G	Max number of green channel bits (used for RLAD modes only). Default Value: 8
19 : 16	RLAD_BITS_R	Max number of red channel bits (used for RLAD modes only). Default Value: 8
1 : 0	RLAD_MODE	Encoding mode. Default Value: 0 **0x0: RLAD :** Run-Length Adaptive Dithering (lossy). **0x1: RLAD_UNIFORM :** RLAD with uniform package size (less efficient, but can force a consistent read bandwidth if needed). **0x2: RLA :** Run-Length Adaptive (lossless).

27.1.39 GFXSS_DC_MXDC_RLAD_ENC (continued)

0x3: RL :

Standard Run-Length (lossless).

27.1.40 GFXSS_DC_MXDC_RLAD_BUF0

Description: Properties of the compressed image data buffer.

Address: 0x4480104C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	RLAD_ADDRESS	Reserved [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RLAD_ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RLAD_ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RLAD_ADDRESS [31:24]							

Bits	Name	Description
31 : 7	RLAD_ADDRESS	Base address of the encoded image buffer in multiple of 128 bytes. The DC layer must be configured to the same base address and with the smallest possible stride value (aligned to 128 bytes). Default Value: 0

27.1.41 GFXSS_DC_MXDC_RLAD_BUF1

Description: Properties of the compressed image data buffer.

Address: 0x44801050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RLAD_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RLAD_SIZE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RLAD_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [31:29]			RLAD_SIZE [28:24]				

Bits	Name	Description
28 : 0	RLAD_SIZE	Size of the the encoded image in number of 32-bit words minus one. The buffer must be readable to the subsequent 128 bytes boundary. Default Value: 0

27.1.42 GFXSS_DC_MXDC_RLAD_STATUS

Description: RLAD decoder status.

Address: 0x44801054

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R		
HW Access	Reserved					W		
Name	Reserved [7:3]					RLAD_FAILED [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	RLAD_FAILED	The fail state is activated in case an error condition has been detected. This will also trigger the RLAD_ERROR interrupt. In that state the RLAD decoding process is stopped and the DC will only read null data. No more read accesses to the memory buffer are generated. The fail state is quit by disabling the DC via CTL.ENABLED. Default Value: 0 **0x0: OFF :** No fail state (= normal operation). **0x1: AXI_ERROR :** An AXI error response was received when reading compressed image data. **0x2: BUF_TOO_SMALL :** The RLAD_SIZE setting is inconsistent with the compressed image data (image decompression not complete when end of buffer was reached). **0x3: BUF_TOO_LARGE :** The RLAD_SIZE setting is inconsistent with the compressed image data (image decompression completed before end of buffer was reached).

27.1.42 GFXSS_DC_MXDC_RLAD_STATUS (continued)

0x4: DC_INVALID_SIZE :

The DC was reading the first pixel of a frame when it was not expected. This means an inconsistent setup of RLAD and DC configuration.

0x5: DC_INVALID_FORMAT :

The DC was reading data with an unexpected burst length. This means an invalid buffer format was configured.

27.1.43 GFXSS_DC_MXDC_IPIDENTIFIER

Description: GFXSS IP and desig release identification (with DC, GPU and MIPIDSI).

Address: 0x44801070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R		Reserved			R
HW Access	Reserved		W		Reserved			W
Name	Reserved [7:6]		IPNAME [5:4]		Reserved [3:1]			IPPLAT-FORM

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	W				W			
Name	IPVERMINOR [15:12]				IPVERMAJOR [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				Reserved		R	
HW Access	W				Reserved		W	
Name	IPRELEASE [23:20]				Reserved [19:18]		IPMATURITY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			R	R			
HW Access	Reserved			W	W			
Name	Reserved [31:29]			IPIMPLE-MENTA-TION	IPRELEASE [27:24]			

Bits	Name	Description
28	IPIMPLEMENTATION	Implementation type. Default Value: Undefined **0x0: RTL :** Logic design for FPGA and ASIC synthesis.
27 : 20	IPRELEASE	Release ID. This is independently set for each implementation type. The value starts with 0 and is increased for every new release of a an IP project, which is defined by IPName, IPVERMAJOR and IPVERMINOR. Default Value: Undefined
17 : 16	IPMATURITY	IP Maturity Status with Chip Integration Cycle targets (CIC). This is independently set for each implementation type. Default Value: Undefined **0x0: NONE :** Undefined. **0x1: CPR :** Implementation incomplete (for CIC Physical Readiness Review).

27.1.43 GFXSS_DC_MXDC_IPIDENTIFIER (continued)

		0x2: CMR : Implementation complete (for CIC Mock Review). **0x3: CFR :** Verification complete (for CIC Final Handoff Review).
15 : 12	IPVERMINOR	Minor IP Version Number. Default Value: Undefined
11 : 8	IPVERMAJOR	Major IP Version Number. Default Value: Undefined
5 : 4	IPNAME	Name of IP family. Default Value: Undefined **0x0: GFXSS :** Graphics Subsystem with Display Controller for Low Power applications.
0	IPPLATFORM	Name of SOC Platform. Default Value: Undefined **0x0: MXS22_S22 :** MXS22 Base Variant.

27.1.44 GFXSS_DC_DCNANO_GCREGDCCHIPREV

Description: Chip Revision Register. Shows the revision for the chip in BCD. This register has no set reset value. It varies with the implementation. READ ONLY.

Address: 0x44801800

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPREV_REV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPREV_REV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPREV_REV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPREV_REV [31:24]							

Bits	Name	Description
31 : 0	GCREGDC-CHIPREV_REV	Revision. The reset value for this field is subject to change and may be ignored during test. Default Value: Undefined

27.1.45 GFXSS_DC_DCNANO_GCREGDCCHIPDATE

Description: Chip Date Register. Shows the release date for the IP in YYYYMMDD (year, month. day) format. This register has no set reset value. It varies with the implementation. READ ONLY.

Address: 0x44801804

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPDATE_DATE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPDATE_DATE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPDATE_DATE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPDATE_DATE [31:24]							

Bits	Name	Description
31 : 0	GCREGDCCHIPDATE_-DATE	Date. The reset value for this field changes per release and may be ignored during test. You can read the accurate value from the RTL file because the actual value may be later than the document release time. Default Value: Undefined

27.1.46 GFXSS_DC_DCNANO_GCREGDCCHIPPATCHREV

Description: Patch Revision Register. Patch revision level for the chip. READ ONLY.

Address: 0x44801808

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPPATCHREV_PATCH_REV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPPATCHREV_PATCH_REV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPPATCHREV_PATCH_REV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDCCHIPPATCHREV_PATCH_REV [31:24]							

Bits	Name	Description
31 : 0	GCREGDCCHIP-PATCHREV_-PATCH_REV	Patch revision. The reset value for this field changes per release and may be ignored during test. You can read the accurate value from the RTL file because the actual value may be later than the document release time. Default Value: Undefined

27.1.47 GFXSS_DC_DCNANO_GCREGDCPRODUCTID

Description: Product Identification Register. READ ONLY.

Address: 0x4480180C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDCPRODUCTID_PRODUCT_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDCPRODUCTID_PRODUCT_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDCPRODUCTID_PRODUCT_ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDCPRODUCTID_PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 0	GCREGDCPRODUC-TID_PRODUCT_ID	Product ID. Bits 3:0 contain Product GRADE_LEVEL. 1 indicates level is Nano. Bits 23:4 contain Product NUM, product number. None for DCNano; 8000 for DC8000 Series. Bits 27:24 contain Product TYPE. 2 indicates Display Controller. Default Value: 0x02080001

27.1.48 GFXSS_DC_DCNANO_GCREGFRAMEBUFFERCONFIG

Description: Frame Buffer Configuration Register. Frame Buffer and Timing control. NOTE.. This register is double buffered.

Address: 0x44801824

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	Reserved	RW	RW		
HW Access	Reserved		R	Reserved	R	R		
Name	Reserved [7:6]		GCREG-FRAME-BUFFERCONFIG_-CLEAR_EN	Reserved	GCREG-FRAME-BUFFERCONFIG_EN-ABLE	GCREGFRAMEBUFFERCONFIG_FOR-MAT [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					RW	Reserved	
HW Access	Reserved					R	Reserved	
Name	Reserved [15:11]					GCREG-FRAME-BUFFERCONFIG_COL-OR_KEY_EN	Reserved [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW	RW		Reserved
HW Access	Reserved				R	R		Reserved
Name	Reserved [23:20]				GCREG-FRAME-BUFFERCONFIG_U-V_SWIZ-ZLE	GCREGFRAMEBUFFER-CONFIG_SWIZZLE [18:17]		Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19	GCREGFRAMEBUFFER-CONFIG_UV_SWIZZLE	NOTE: This field is double buffered. Default Value: 0x0
18 : 17	GCREGFRAMEBUFFER-CONFIG_SWIZZLE	NOTE: This field is double buffered. Default Value: 0x0 **0x0: ARGB :** (none) **0x1: RGBA :** (none)

27.1.48 GFXSS_DC_DCNANO_GCREGFRAMEBUFFERCONFIG (continued)

		0x2: ABGR : (none) **0x3: BGRA :** (none)
10	GCREGFRAMEBUFFER-CONFIG_COL-OR_KEY_EN	Enable or disable color key. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
5	GCREGFRAMEBUFFER-CONFIG_CLEAR_EN	Enable or disable clear. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
3	GCREGFRAMEBUFFER-CONFIG_ENABLE	Enable this layer or disable this layer. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
2 : 0	GCREGFRAMEBUFFER-CONFIG_FORMAT	The format of the frame buffer. None means there is no frame buffer and the display controller will not produce any output. NOTE: This field is double buffered. Default Value: 0x0 **0x0: NONE :** (none) **0x1: A4R4G4B4 :** (none) **0x2: A1R5G5B5 :** (none)

27.1.48 GFXSS_DC_DCNANO_GCREGFRAMEBUFFERCONFIG (continued)

0x3: R5G6B5 :

(none)

0x4: A8R8G8B8 :

(none)

27.1.49 GFXSS_DC_DCNANO_GCREGFRAMEBUFFERADDRESS

Description: Frame Buffer Base Address Register. Starting address of the frame buffer. NOTE.. This register is double buffered.

Address: 0x44801828

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERADDRESS_ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERADDRESS_ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERADDRESS_ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERADDRESS_ADDRESS [31:24]							

Bits	Name	Description
31 : 0	GCREGFRAME-BUFFERADDRESS_AD-DRESS	32 bit address. Default Value: 0x00000000

27.1.50 GFXSS_DC_DCNANO_GCREGFRAMEBUFFERSTRIDE

Description: Frame Buffer Stride Register. Stride of the frame buffer in bytes. NOTE.. This register is double buffered.

Address: 0x4480182C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERSTRIDE_STRIDE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERSTRIDE_STRIDE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							GCREG-FRAME-BUFFERSTRIDE_STRIDE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16 : 0	GCREGFRAMEBUFFER-STRIDE_STRIDE	Number of bytes from start of one line to next line. NOTE: This field is double buffered. Default Value: 0x00000

27.1.51 GFXSS_DC_DCNANO_GCREGDCTILEINCFG

Description: Tile Input Configuration Register. Tile input configuration. NOTE.. This register is double buffered.

Address: 0x44801834

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [7:3]					GCREGDC-TILEINCF-G_YUV_STANDARD	GCREGDCTILEINCF-G_TILE_FORMAT [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	GCREGDCTILEINCF-G_YUV_STANDARD	YUV standard select. NOTE: This field is double buffered. Default Value: 0x0 **0x0: BT601 :** (none) **0x1: BT709 :** (none)
1 : 0	GCREGDCTILEINCF-G_TILE_FORMAT	Tile input data format 0 means non-tile input. NOTE: This field is double buffered. Default Value: 0x0 **0x0: NONE :** (none) **0x1: ARGB8888 :** (none)

27.1.51 GFXSS_DC_DCNANO_GCREGDCTILEINCFG (continued)

0x2: YUY2 :

(none)

0x3: NV12 :

(none)

27.1.52 GFXSS_DC_DCNANO_GCREGDCTILEUVFRAMEBUFFERADR

Description: Frame Buffer Tiled UV Base Address Register. UV frame buffer address when tile input. NOTE.. This register is double buffered.

Address: 0x44801838

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVFRAMEBUFFERADR_ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVFRAMEBUFFERADR_ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVFRAMEBUFFERADR_ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVFRAMEBUFFERADR_ADDRESS [31:24]							

Bits	Name	Description
31 : 0	GCREGDCTILEUV-FRAMEBUFFERADR_AD-DRESS	UV frame buffer address when tile input NOTE: This field is double buffered. Default Value: 0x00000000

27.1.53 GFXSS_DC_DCNANO_GCREGDCTILEUVFRAMEBUFFERSTR

Description: Frame Buffer Tiled UV Stride Register. UV frame buffer stride when tile input NOTE.. This register is double buffered.

Address: 0x4480183C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVFRAMEBUFFERSTR_STRIDE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVFRAMEBUFFERSTR_STRIDE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	GCREGDCTILEUV-FRAMEBUFFER-STR_STRIDE	UV frame buffer stride when tile input NOTE: This field is double buffered. Default Value: 0x0000

27.1.54 GFXSS_DC_DCNANO_GCREGFRAMEBUFFERBACKGROUND

Description: Framebuffer background color. NOTE.. This register is double buffered.

Address: 0x44801858

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERBACKGROUND_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERBACKGROUND_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERBACKGROUND_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERBACKGROUND_ALPHA [31:24]							

Bits	Name	Description
31 : 24	GCREGFRAMEBUFFER-BACKGROUND_ALPHA	NOTE: This field is double buffered. Default Value: 0x00
23 : 16	GCREGFRAMEBUFFER-BACKGROUND_RED	NOTE: This field is double buffered. Default Value: 0x00
15 : 8	GCREGFRAMEBUFFER-BACKGROUND_GREEN	NOTE: This field is double buffered. Default Value: 0x00
7 : 0	GCREGFRAMEBUFFER-BACKGROUND_BLUE	NOTE: This field is double buffered. Default Value: 0x00

27.1.55 GFXSS_DC_DCNANO_GCREGFRAMEBUFFERCOLORKEY

Description: Framebuffer Color Key Start Address Register. Start of color key range of framebuffer. NOTE.. This register is double buffered.

Address: 0x4480185C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCOLORKEY_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCOLORKEY_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCOLORKEY_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCOLORKEY_ALPHA [31:24]							

Bits	Name	Description
31 : 24	GCREGFRAMEBUFFER-COLORKEY_ALPHA	8 bit alpha value. Default Value: 0x00
23 : 16	GCREGFRAMEBUFFER-COLORKEY_RED	8 bit red color. Default Value: 0x00
15 : 8	GCREGFRAMEBUFFER-COLORKEY_GREEN	8 bit green color. Default Value: 0x00
7 : 0	GCREGFRAMEBUFFER-COLORKEY_BLUE	8 bit blue color. Default Value: 0x00

27.1.56 GFXSS_DC_DCNANO_GCREGFRAMEBUFFERCOLORKEYHIGH

Description: Framebuffer Color Key End Address Register. End of color key range of framebuffer. NOTE.. This register is double buffered.

Address: 0x44801860

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCOLORKEYHIGH_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCOLORKEYHIGH_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCOLORKEYHIGH_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCOLORKEYHIGH_ALPHA [31:24]							

Bits	Name	Description
31 : 24	GCREGFRAMEBUFFER-COLORKEYHIGH_ALPHA	8 bit alpha value. Default Value: 0x00
23 : 16	GCREGFRAMEBUFFER-COLORKEYHIGH_RED	8 bit red color. Default Value: 0x00
15 : 8	GCREGFRAMEBUFFER-COLORKEY-HIGH_GREEN	8 bit green color. Default Value: 0x00
7 : 0	GCREGFRAMEBUFFER-COLORKEYHIGH_BLUE	8 bit blue color. Default Value: 0x00

27.1.57 GFXSS_DC_DCNANO_GCREGFRAMEBUFFERCLEARVALUE

Description: Framebuffer Clear Value Register. Clear value used when dcregFrameBufferConfig.Clear is enabled, format is A8R8G8B8. NOTE.. This register is double buffered.

Address: 0x44801864

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCLEARVALUE_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCLEARVALUE_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCLEARVALUE_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERCLEARVALUE_ALPHA [31:24]							

Bits	Name	Description
31 : 24	GCREGFRAMEBUFFER-CLEARVALUE_ALPHA	8 bit alpha value. Default Value: 0x00
23 : 16	GCREGFRAMEBUFFER-CLEARVALUE_RED	8 bit red color. Default Value: 0x00
15 : 8	GCREGFRAMEBUFFER-CLEARVALUE_GREEN	8 bit green color. Default Value: 0x00
7 : 0	GCREGFRAMEBUFFER-CLEARVALUE_BLUE	8 bit blue color. Default Value: 0x00

27.1.58 GFXSS_DC_DCNANO_GCREGVIDEOTL

Description: Top left coordinate of panel pixel where the video should start. Be aware there is no panning inside the video. NOTE.. This register is double buffered.

Address: 0x44801868

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGVIDEOTL_X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				GCREGVIDEOTL_X [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGVIDEOTL_Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				GCREGVIDEOTL_Y [27:24]			

Bits	Name	Description
27 : 16	GCREGVIDEOTL_Y	Top boundary of video window. NOTE: This field is double buffered. Default Value: 0x000
11 : 0	GCREGVIDEOTL_X	Left boundary of video window. NOTE: This field is double buffered. Default Value: 0x000

27.1.59 GFXSS_DC_DCNANO_GCREGFRAMEBUFFERSIZE

Description: video size information. NOTE.. This register is double buffered.

Address: 0x4480186C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERSIZE_WIDTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				GCREGFRAMEBUFFERSIZE_WIDTH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGFRAMEBUFFERSIZE_HEIGHT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				GCREGFRAMEBUFFERSIZE_HEIGHT [27:24]			

Bits	Name	Description
27 : 16	GCREGFRAMEBUFFER-SIZE_HEIGHT	video height. NOTE: This field is double buffered. Default Value: 0x000
11 : 0	GCREGFRAMEBUFFER-SIZE_WIDTH	video width. NOTE: This field is double buffered. Default Value: 0x000

27.1.60 GFXSS_DC_DCNANO_GCREGVIDEOGLOBALALPHA

Description: Global alpha for the video. NOTE.. This register is double buffered.

Address: 0x44801870

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGVIDEOGLOBALALPHA_SRC_ALPHA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGVIDEOGLOBALALPHA_DST_ALPHA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	GCREGVIDEOGLOBAL-ALPHA_DST_ALPHA	Destination alpha for video. NOTE: This field is double buffered. Default Value: 0x00
7 : 0	GCREGVIDEOGLOBAL-ALPHA_SRC_ALPHA	Source alpha for video. NOTE: This field is double buffered. Default Value: 0x00

27.1.61 GFXSS_DC_DCNANO_GCREGBLENDSTACKORDER

Description: Set the video, overlay0, overlay1 order for blend. The 1st is the lowest layer, the 2nd is the middle layer, the 3rd is the highest layer. NOTE.. This register is double buffered.

Address: 0x44801874

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					GCREGBLENDSTACKORDER_ORDER [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	GCREGBLENDSTACK-ORDER_ORDER	NOTE: This field is double buffered. Default Value: 0x0 **0x0: VIDEO_OVERLAY0_OVERLAY1 :** (none) **0x1: VIDEO_OVERLAY1_OVERLAY0 :** (none) **0x2: OVERLAY0_VIDEO_OVERLAY1 :** (none) **0x3: OVERLAY0_OVERLAY1_VIDEO :** (none) **0x4: OVERLAY1_VIDEO_OVERLAY0 :** (none)

27.1.61 GFXSS_DC_DCNANO_GCREGBLENDSTACKORDER (continued)

0x5: OVERLAY1_OVERLAY0_VIDEO :

(none)

27.1.62 GFXSS_DC_DCNANO_GCREGVIDEOALPHABLENDCONFIG

Description: Alpha Blending Configuration Register. NOTE.. This register is double buffered.

Address: 0x44801878

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		Reserved	RW		Reserved	RW	RW
HW Access	R		Reserved	R		Reserved	R	R
Name	GCREGVIDEOALPHA-BLENDCONFIG_S-RC_BLENDING_MODE [7:6]		Reserved	GCREGVIDEOALPHA-BLENDCONFIG_SRC_-GLOBAL_ALPHA_MODE [4:3]		Reserved	GCREGVIDEOALPHA-BLEND-CONFIG_SRC_AL-PHA_-MODE	GCREGVIDEOALPHA-BLEND-CONFIG_ALPHA_BLEND

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		Reserved	RW		RW	RW
HW Access	R	R		Reserved	R		R	R
Name	GCREGVIDEOALPHA-BLEND-CONFIG_DST_AL-PHA_FAC-TOR	GCREGVIDEOALPHA-BLENDCONFIG_D-ST_BLENDING_MODE [14:13]		Reserved	GCREGVIDEOALPHA-BLENDCONFIG_DST_-GLOBAL_ALPHA_MODE [11:10]		GCREGVIDEOALPHA-BLEND-CONFIG_DST_AL-PHA_-MODE	GCREGVIDEOALPHA-BLEND-CONFIG_SRC_AL-PHA_FAC-TOR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	GCREGVIDEOALPHA-BLENDCONFIG_DST_AL-PHA_FACTOR	Destination blending factor is calculated from Dst alpha. Default Value: 0x0 **0x0: DISABLED :** Select src alpha after global value substitution to calculate dst blending factor. **0x1: ENABLED :** Select dst alpha after global value substitution to calculate dst blending factor.
14 : 13	GCREGVIDEOALPHA-BLENDCONFIG_D-ST_BLENDING_MODE	Control the destination blending factor generation. Default Value: 0x0

27.1.62 GFXSS_DC_DCNANO_GCREGVIDEOALPHABLENDCONFIG (continued)

		0x0: ZERO : Use 0 as factor. **0x1: ONE :** Use 1 as factor. **0x2: NORMAL :** Use the selected alpha as factor (use GCREGVIDEOALPHABLENDCONFIG_DST_ALPHA_-FACTOR to select alpha). **0x3: INVERSED :** Use 1 minus the selected alpha as factor (use GCREGVIDEOALPHABLENDCONFIG_DST_ALPHA_FACTOR to select alpha).
11 : 10	GCREGVIDEOALPHA-BLENDCONFIG_DST_-GLOBAL_ALPHA_MODE	Set destination global alpha mode. Default Value: 0x0 **0x0: NORMAL :** No operation. **0x1: GLOBAL :** Use the destination global alpha value (GCREGVIDEOGLOBALALPHA_DST_ALPHA) to replace. **0x2: SCALED :** Multiply by the destination global alpha value.
9	GCREGVIDEOALPHA-BLENDCONFIG_DST_ALPHA_MODE	Set destination alpha mode. Default Value: 0x0 **0x0: NORMAL :** No operation. **0x1: INVERSED :** Use 1 to subtract destination alpha before global alpha.
8	GCREGVIDEOALPHA-BLENDCONFIG_S-RC_ALPHA_FACTOR	Src Blending factor is calculated from Src alpha. Default Value: 0x0 **0x0: DISABLED :** Select dst alpha after global value substitution to calculate src blending factor. **0x1: ENABLED :** Select src alpha after global value substitution to calculate src blending factor.

27.1.62 GFXSS_DC_DCNANO_GCREGVIDEOALPHABLENDCONFIG (continued)

7 : 6	GCREGVIDEOALPHA-BLENDCONFIG_S-RC_BLENDING_MODE	Control the source blending factor generation. Default Value: 0x0 **0x0: ZERO :** Use 0 as factor. **0x1: ONE :** Use 1 as factor. **0x2: NORMAL :** Use the selected alpha as factor (use GCREGVIDEOALPHABLENDCONFIG_SRC_ALPHA_-FACTOR to select alpha). **0x3: INVERSED :** Use 1 minus the selected alpha as factor (use GCREGVIDEOALPHABLENDCONFIG_S-RC_ALPHA_FACTOR to select alpha).
4 : 3	GCREGVIDEOALPHA-BLENDCONFIG_SRC_-GLOBAL_ALPHA_MODE	Set source global alpha mode. Default Value: 0x0 **0x0: NORMAL :** No operation. **0x1: GLOBAL :** Use the source global alpha value (GCREGVIDEOGLOBALALPHA_SRC_ALPHA) to replace. **0x2: SCALED :** Multiply by source global alpha value.
1	GCREGVIDEOALPHA-BLENDCONFIG_S-RC_ALPHA_MODE	Set alpha source mode. Default Value: 0x0 **0x0: NORMAL :** No operation. **0x1: INVERSED :** Use 1 to subtract source alpha before global alpha.
0	GCREGVIDEOALPHA-BLENDCONFIG_AL-PHA_BLEND	Enable or disable alpha blending. Default Value: 0x0 **0x0: DISABLED :** Use source color as blend result.

27.1.62 GFXSS_DC_DCNANO_GCREGVIDEOALPHABLENDCONFIG (continued)

0x1: ENABLED :

Enable blending.

27.1.63 GFXSS_DC_DCNANO_GCREGOVERLAYCONFIG

Description: Overlay Configuration Register. Overlay control. NOTE.. This register is double buffered.

Address: 0x4480187C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	Reserved	RW	RW		
HW Access	Reserved		R	Reserved	R	R		
Name	Reserved [7:6]		GCREGOVERLAY-CONFIG_CLEAR_EN	Reserved	GCREGOVERLAY-CONFIG_ENABLE	GCREGOVERLAYCONFIG_FORMAT [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW	RW	RW		Reserved
HW Access	Reserved			R	R	R		Reserved
Name	Reserved [23:21]			GCREGOVERLAY-CONFIG_COL-OR_KEY_EN	GCREGOVERLAY-CONFIG_UV_SWIZ-ZLE	GCREGOVERLAYCON-FIG_SWIZZLE [18:17]		Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20	GCREGOVERLAYCON-FIG_COLOR_KEY_EN	Enable or disable color key. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
19	GCREGOVERLAYCON-FIG_UV_SWIZZLE	NOTE: This field is double buffered. Default Value: 0x0
18 : 17	GCREGOVERLAYCON-FIG_SWIZZLE	NOTE: This field is double buffered. Default Value: 0x0

27.1.63 GFXSS_DC_DCNANO_GCREGOVERLAYCONFIG (continued)

		0x0: ARGB : (none) **0x1: RGBA :** (none) **0x2: ABGR :** (none) **0x3: BGRA :** (none)
5	GCREGOVERLAYCONFIG_CLEAR_EN	Enable or disable clear. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
3	GCREGOVERLAYCONFIG_ENABLE	Enable this overlay layer. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLE :** (none) **0x1: ENABLE :** (none)
2 : 0	GCREGOVERLAYCONFIG_FORMAT	The format of the overlay. None means there is no overlay. NOTE: This field is double buffered. Default Value: 0x0 **0x0: NONE :** (none) **0x1: A4R4G4B4 :** (none) **0x2: A1R5G5B5 :** (none) **0x3: R5G6B5 :** (none)

27.1.63 GFXSS_DC_DCNANO_GCREGOVERLAYCONFIG (continued)

0x4: A8R8G8B8 :

(none)

27.1.64 GFXSS_DC_DCNANO_GCREGOVERLAYADDRESS

Description: Starting address of the overlay. NOTE.. This register is double buffered.

Address: 0x44801880

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYADDRESS_ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYADDRESS_ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYADDRESS_ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYADDRESS_ADDRESS [31:24]							

Bits	Name	Description
31 : 0	GCREGOVERLAYAD-DRESS_ADDRESS	32 bit address. Default Value: 0x00000000

27.1.65 GFXSS_DC_DCNANO_GCREGOVERLAYSTRIDE

Description: Stride of the overlay in bytes. NOTE.. This register is double buffered.

Address: 0x44801884

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYSTRIDE_STRIDE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYSTRIDE_STRIDE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							GCREGOV-ERLAY-STRIDE_STRIDE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16 : 0	GCREGOVERLAY-STRIDE_STRIDE	Number of bytes from start of one line to next line. Default Value: 0x00000

27.1.66 GFXSS_DC_DCNANO_GCREGDCOVERLAYTILEINCFG

Description: Tile Input Configuration Register. Tile input configuration. NOTE.. This register is double buffered.

Address: 0x44801888

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	
HW Access	Reserved					R	R	
Name	Reserved [7:3]					GCREGD-COVER-LAYTILEIN CFG_YU-V_STAN-DARD	GCREGDCOVERLAYTIL-EINCFG_TILE_FORMAT [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	GCREGDCOVERLAYTIL-EINCFG_YUV_STAN-DARD	YUV standard select. NOTE: This field is double buffered. Default Value: 0x0 **0x0: BT601 :** (none) **0x1: BT709 :** (none)
1 : 0	GCREGDCOVERLAYTIL-EINCFG_TILE_FORMAT	Tile input data format 0 means non-tile input NOTE: This field is double buffered. Default Value: 0x0 **0x0: NONE :** (none)

27.1.66 GFXSS_DC_DCNANO_GCREGDCOVERLAYTILEINCFG (continued)

0x1: ARGB8888 :

(none)

0x2: YUY2 :

(none)

0x3: NV12 :

(none)

27.1.67 GFXSS_DC_DCNANO_GCREGDCTILEUVOVERLAYADR

Description: Starting address of the overlay UV. NOTE.. This register is double buffered.

Address: 0x4480188C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVOVERLAYADR_ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVOVERLAYADR_ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVOVERLAYADR_ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVOVERLAYADR_ADDRESS [31:24]							

Bits	Name	Description
31 : 0	GCREGDCTILEUVOVER-LAYADR_ADDRESS	32 bit address. Default Value: 0x00000000

27.1.68 GFXSS_DC_DCNANO_GCREGDCTILEUVOVERLAYSTR

Description: Stride of the overlay UV in bytes. NOTE.. This register is double buffered.

Address: 0x44801890

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVOVERLAYSTR_STRIDE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGDCTILEUVOVERLAYSTR_STRIDE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	GCREGDCTILEUVOVER-LAYSTR_STRIDE	Number of bytes from start of one line to next line. NOTE: This field is double buffered. Default Value: 0x0000

27.1.69 GFXSS_DC_DCNANO_GCREGOVERLAYTL

Description: Top left coordinate of panel pixel where the overlay should start. Be aware there is no panning inside the overlay. NOTE.. This register is double buffered.

Address: 0x44801894

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYTL_X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				GCREGOVERLAYTL_X [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYTL_Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				GCREGOVERLAYTL_Y [27:24]			

Bits	Name	Description
27 : 16	GCREGOVERLAYTL_Y	Top boundary of overlay window. Default Value: 0x000
11 : 0	GCREGOVERLAYTL_X	Left boundary of overlay window. Default Value: 0x000

27.1.70 GFXSS_DC_DCNANO_GCREGOVERLAYSIZE

Description: overlay size information. NOTE.. This register is double buffered.

Address: 0x44801898

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYSIZE_WIDTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				GCREGOVERLAYSIZE_WIDTH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYSIZE_HEIGHT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				GCREGOVERLAYSIZE_HEIGHT [27:24]			

Bits	Name	Description
27 : 16	GCREGOVERLAY-SIZE_HEIGHT	overlay height. Default Value: 0x000
11 : 0	GCREGOVERLAY-SIZE_WIDTH	overlay width. Default Value: 0x000

27.1.71 GFXSS_DC_DCNANO_GCREGOVERLAYCOLORKEY

Description: Overlay Color Key Start Address Register. Start of color key range for overlay. NOTE.. This register is double buffered.

Address: 0x4480189C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEY_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEY_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEY_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEY_ALPHA [31:24]							

Bits	Name	Description
31 : 24	GCREGOVERLAYCOL-ORKEY_ALPHA	8 bit alpha value. Default Value: 0x00
23 : 16	GCREGOVERLAYCOL-ORKEY_RED	8 bit red color. Default Value: 0x00
15 : 8	GCREGOVERLAYCOL-ORKEY_GREEN	8 bit green color. Default Value: 0x00
7 : 0	GCREGOVERLAYCOL-ORKEY_BLUE	8 bit blue color. Default Value: 0x00

27.1.72 GFXSS_DC_DCNANO_GCREGOVERLAYCOLORKEYHIGH

Description: Overlay Color Key End Address Register. End of color key range for overlay. NOTE.. This register is double buffered.

Address: 0x448018A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEYHIGH_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEYHIGH_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEYHIGH_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEYHIGH_ALPHA [31:24]							

Bits	Name	Description
31 : 24	GCREGOVERLAYCOL-ORKEYHIGH_ALPHA	8 bit alpha value. Default Value: 0x00
23 : 16	GCREGOVERLAYCOL-ORKEYHIGH_RED	8 bit red color. Default Value: 0x00
15 : 8	GCREGOVERLAYCOL-ORKEYHIGH_GREEN	8 bit green color. Default Value: 0x00
7 : 0	GCREGOVERLAYCOL-ORKEYHIGH_BLUE	8 bit blue color. Default Value: 0x00

27.1.73 GFXSS_DC_DCNANO_GCREGOVERLAYALPHABLENDCONFIG

Description: Alpha Blending Configuration Register. NOTE.. This register is double buffered.

Address: 0x448018A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		Reserved	RW		Reserved	RW	RW
HW Access	R		Reserved	R		Reserved	R	R
Name	GCREGOVERLAYALPHA-BLENDCONFIG_S-RC_BLENDING_MODE [7:6]		Reserved	GCREGOVERLAYALPHA-BLENDCONFIG_SRC_-GLOBAL_ALPHA_MODE [4:3]		Reserved	GCREGOV-ERLAYAL-PHABLEND CONFIG_S-RC_AL-PHA_MOD E	GCREGOV-ERLAYAL-PHABLEND CON-FIG_AL-PHA_BLEN D

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		Reserved	RW		RW	RW
HW Access	R	R		Reserved	R		R	R
Name	GCREGOV-ERLAYAL-PHABLEND CONFIG_D-ST_AL-PHA_FACT OR	GCREGOVERLAYALPHA-BLENDCONFIG_D-ST_BLENDING_MODE [14:13]		Reserved	GCREGOVERLAYALPHA-BLENDCONFIG_DST_-GLOBAL_ALPHA_MODE [11:10]		GCREGOV-ERLAYAL-PHABLEND CONFIG_D-ST_AL-PHA_MOD E	GCREGOV-ERLAYAL-PHABLEND CONFIG_S-RC_AL-PHA_FACT OR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	GCREGOVERLAYALPH-ABLENDCONFIG_D-ST_ALPHA_FACTOR	Destination blending factor is calculated from Dst alpha. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
14 : 13	GCREGOVERLAYALPH-ABLENDCONFIG_D-ST_BLENDING_MODE	(none) Default Value: 0x0

27.1.73 GFXSS_DC_DCNANO_GCREGOVERLAYALPHABLENDCONFIG (continued)

		0x0: ZERO : (none) **0x1: ONE :** (none) **0x2: NORMAL :** (none) **0x3: INVERSED :** (none)
11 : 10	GCREGOVERLAYALPH-ABLENDCONFIG_DST_-GLOBAL_ALPHA_MODE	(none) Default Value: 0x0 **0x0: NORMAL :** (none) **0x1: GLOBAL :** (none) **0x2: SCALED :** (none)
9	GCREGOVERLAYALPH-ABLENDCONFIG_D-ST_ALPHA_MODE	(none) Default Value: 0x0 **0x0: NORMAL :** (none) **0x1: INVERSED :** (none)
8	GCREGOVERLAYALPH-ABLENDCONFIG_S-RC_ALPHA_FACTOR	Src Blending factor is calculated from Src alpha. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
7 : 6	GCREGOVERLAYALPH-ABLENDCONFIG_S-RC_BLENDING_MODE	(none) Default Value: 0x0

27.1.73 GFXSS_DC_DCNANO_GCREGOVERLAYALPHABLENDCONFIG (continued)

		0x0: ZERO : (none) **0x1: ONE :** (none) **0x2: NORMAL :** (none) **0x3: INVERSED :** (none)
4 : 3	GCREGOVERLAYALPH-ABLENDCONFIG_SRC_-GLOBAL_ALPHA_MODE	(none) Default Value: 0x0 **0x0: NORMAL :** (none) **0x1: GLOBAL :** (none) **0x2: SCALED :** (none)
1	GCREGOVERLAYALPH-ABLENDCONFIG_S-RC_ALPHA_MODE	(none) Default Value: 0x0 **0x0: NORMAL :** (none) **0x1: INVERSED :** (none)
0	GCREGOVERLAYALPH-ABLENDCONFIG_AL-PHA_BLEND	(none) Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)

27.1.74 GFXSS_DC_DCNANO_GCREGOVERLAYGLOBALALPHA

Description: Overlay global alpha value. NOTE.. This register is double buffered.

Address: 0x448018A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYGLOBALALPHA_SRC_ALPHA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYGLOBALALPHA_DST_ALPHA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	GCREGOVERLAYGLO-BALALPHA_DST_ALPHA	(none) Default Value: 0x00
7 : 0	GCREGOVERLAYGLO-BALALPHA_SRC_ALPHA	(none) Default Value: 0x00

27.1.75 GFXSS_DC_DCNANO_GCREGOVERLAYCLEARVALUE

Description: Overlay Clear Value Register. Clear value used when dcregOverlayConfig.Clear is enabled, Format is A8R8G8B8. NOTE.. This register is double buffered.

Address: 0x448018AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCLEARVALUE_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCLEARVALUE_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCLEARVALUE_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCLEARVALUE_ALPHA [31:24]							

Bits	Name	Description
31 : 24	GCREGOVERLAY-CLEARVALUE_ALPHA	8 bit alpha value. Default Value: 0x00
23 : 16	GCREGOVERLAY-CLEARVALUE_RED	8 bit red color. Default Value: 0x00
15 : 8	GCREGOVERLAY-CLEARVALUE_GREEN	8 bit green color. Default Value: 0x00
7 : 0	GCREGOVERLAY-CLEARVALUE_BLUE	8 bit blue color. Default Value: 0x00

27.1.76 GFXSS_DC_DCNANO_GCREGOVERLAYCONFIG1

Description: Overlay Configuration Register. Overlay control. NOTE.. This register is double buffered.

Address: 0x448018B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	Reserved	RW	RW		
HW Access	Reserved		R	Reserved	R	R		
Name	Reserved [7:6]		GCREGOVERLAY-CONFIG1_CLEAR_EN	Reserved	GCREGOVERLAY-CONFIG1_ENABLE	GCREGOVERLAYCONFIG1_FORMAT [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW	Reserved	RW		Reserved
HW Access	Reserved			R	Reserved	R		Reserved
Name	Reserved [23:21]			GCREGOVERLAY-CONFIG1_COL-OR_KEY_EN	Reserved	GCREGOVERLAYCON-FIG1_SWIZZLE [18:17]		Reserved

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20	GCREGOVERLAYCON-FIG1_COLOR_KEY_EN	Enable or disable color key. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
18 : 17	GCREGOVERLAYCON-FIG1_SWIZZLE	NOTE: This field is double buffered. Default Value: 0x0 **0x0: ARGB :** (none)

27.1.76 GFXSS_DC_DCNANO_GCREGOVERLAYCONFIG1 (continued)

		0x1: RGBA : (none) **0x2: ABGR :** (none) **0x3: BGRA :** (none)
5	GCREGOVERLAYCONFIG1_CLEAR_EN	Enable or disable clear. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
3	GCREGOVERLAYCONFIG1_ENABLE	Enable this overlay layer. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLE :** (none) **0x1: ENABLE :** (none)
2 : 0	GCREGOVERLAYCONFIG1_FORMAT	The format of the overlay. None means there is no overlay. NOTE: This field is double buffered. Default Value: 0x0 **0x0: NONE :** (none) **0x1: A4R4G4B4 :** (none) **0x2: A1R5G5B5 :** (none) **0x3: R5G6B5 :** (none) **0x4: A8R8G8B8 :** (none)

27.1.77 GFXSS_DC_DCNANO_GCREGOVERLAYADDRESS1

Description: Starting address of the overlay. NOTE.. This register is double buffered.

Address: 0x448018B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYADDRESS1_ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYADDRESS1_ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYADDRESS1_ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYADDRESS1_ADDRESS [31:24]							

Bits	Name	Description
31 : 0	GCREGOVERLAYAD-DRESS1_ADDRESS	32 bit address. Default Value: 0x00000000

27.1.78 GFXSS_DC_DCNANO_GCREGOVERLAYSTRIDE1

Description: Stride of the overlay in bytes. NOTE.. This register is double buffered.

Address: 0x448018B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYSTRIDE1_STRIDE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYSTRIDE1_STRIDE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							GCREGOV-ERLAY-STRIDE1_STRIDE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16 : 0	GCREGOVERLAY-STRIDE1_STRIDE	Number of bytes from start of one line to next line. Default Value: 0x00000

27.1.79 GFXSS_DC_DCNANO_GCREGOVERLAYTL1

Description: Top left coordinate of panel pixel where the overlay should start. Be aware there is no panning inside the overlay. NOTE.. This register is double buffered.

Address: 0x448018BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYTL1_X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				GCREGOVERLAYTL1_X [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYTL1_Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				GCREGOVERLAYTL1_Y [27:24]			

Bits	Name	Description
27 : 16	GCREGOVERLAYTL1_Y	Top boundary of overlay window. Default Value: 0x000
11 : 0	GCREGOVERLAYTL1_X	Left boundary of overlay window. Default Value: 0x000

27.1.80 GFXSS_DC_DCNANO_GCREGOVERLAYSIZE1

Description: overlay1 size information. NOTE.. This register is double buffered.

Address: 0x448018C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYSIZE1_WIDTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				GCREGOVERLAYSIZE1_WIDTH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYSIZE1_HEIGHT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				GCREGOVERLAYSIZE1_HEIGHT [27:24]			

Bits	Name	Description
27 : 16	GCREGOVERLAY-SIZE1_HEIGHT	overlay1 height. Default Value: 0x000
11 : 0	GCREGOVERLAY-SIZE1_WIDTH	overlay1 width. Default Value: 0x000

27.1.81 GFXSS_DC_DCNANO_GCREGOVERLAYCOLORKEY1

Description: Overlay Color Key Start Address Register. Start of color key range for overlay. NOTE.. This register is double buffered.

Address: 0x448018C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEY1_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEY1_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEY1_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEY1_ALPHA [31:24]							

Bits	Name	Description
31 : 24	GCREGOVERLAYCOL-ORKEY1_ALPHA	8 bit alpha value. Default Value: 0x00
23 : 16	GCREGOVERLAYCOL-ORKEY1_RED	8 bit red color. Default Value: 0x00
15 : 8	GCREGOVERLAYCOL-ORKEY1_GREEN	8 bit green color. Default Value: 0x00
7 : 0	GCREGOVERLAYCOL-ORKEY1_BLUE	8 bit blue color. Default Value: 0x00

27.1.82 GFXSS_DC_DCNANO_GCREGOVERLAYCOLORKEYHIGH1

Description: Overlay Color Key End Address Register. End of color key range for overlay. NOTE.. This register is double buffered.

Address: 0x448018C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEYHIGH1_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEYHIGH1_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEYHIGH1_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCOLORKEYHIGH1_ALPHA [31:24]							

Bits	Name	Description
31 : 24	GCREGOVERLAYCOL-ORKEYHIGH1_ALPHA	8 bit alpha value. Default Value: 0x00
23 : 16	GCREGOVERLAYCOL-ORKEYHIGH1_RED	8 bit red color. Default Value: 0x00
15 : 8	GCREGOVERLAYCOL-ORKEYHIGH1_GREEN	8 bit green color. Default Value: 0x00
7 : 0	GCREGOVERLAYCOL-ORKEYHIGH1_BLUE	8 bit blue color. Default Value: 0x00

27.1.83 GFXSS_DC_DCNANO_GCREGOVERLAYALPHABLENDCONFIG1

Description: Alpha Blending Configuration Register. NOTE.. This register is double buffered.

Address: 0x448018CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		Reserved	RW		Reserved	RW	RW
HW Access	R		Reserved	R		Reserved	R	R
Name	GCREGOVERLAYALPHA-BLENDCONFIG1_S-RC_BLENDING_MODE [7:6]		Reserved	GCREGOVERLAYALPHA-BLENDCONFIG1_SRC_-GLOBAL_ALPHA_MODE [4:3]		Reserved	GCREGOV-ERLAYAL-PHABLEND CON-FIG1_S-RC_ALPHA _MODE	GCREGOV-ERLAYAL-PHABLEND CON-FIG1_AL-PHA_BLEN D

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		Reserved	RW		RW	RW
HW Access	R	R		Reserved	R		R	R
Name	GCREGOV-ERLAYAL-PHABLEND CON-FIG1_D-ST_ALPHA _FACTOR	GCREGOVERLAYALPHA-BLENDCONFIG1_D-ST_BLENDING_MODE [14:13]		Reserved	GCREGOVERLAYALPHA-BLENDCONFIG1_DST_-GLOBAL_ALPHA_MODE [11:10]		GCREGOV-ERLAYAL-PHABLEND CON-FIG1_D-ST_ALPHA _MODE	GCREGOV-ERLAYAL-PHABLEND CON-FIG1_S-RC_ALPHA _FACTOR

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15	GCREGOVERLAYALPH-ABLENDCONFIG1_D-ST_ALPHA_FACTOR	Destination blending factor is calculated from Dst alpha. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
14 : 13	GCREGOVERLAYALPH-ABLENDCONFIG1_D-ST_BLENDING_MODE	(none) Default Value: 0x0

27.1.83 GFXSS_DC_DCNANO_GCREGOVERLAYALPHABLENDCONFIG1 (continued)

		0x0: ZERO : (none) **0x1: ONE :** (none) **0x2: NORMAL :** (none) **0x3: INVERSED :** (none)
11 : 10	GCREGOVERLAYALPH-ABLENDCONFIG1_DST_-GLOBAL_ALPHA_MODE	(none) Default Value: 0x0 **0x0: NORMAL :** (none) **0x1: GLOBAL :** (none) **0x2: SCALED :** (none)
9	GCREGOVERLAYALPH-ABLENDCONFIG1_D-ST_ALPHA_MODE	(none) Default Value: 0x0 **0x0: NORMAL :** (none) **0x1: INVERSED :** (none)
8	GCREGOVERLAYALPH-ABLENDCONFIG1_S-RC_ALPHA_FACTOR	Src Blending factor is calculated from Src alpha. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
7 : 6	GCREGOVERLAYALPH-ABLENDCONFIG1_S-RC_BLENDING_MODE	(none) Default Value: 0x0

27.1.83 GFXSS_DC_DCNANO_GCREGOVERLAYALPHABLENDCONFIG1 (continued)

		0x0: ZERO : (none) **0x1: ONE :** (none) **0x2: NORMAL :** (none) **0x3: INVERSED :** (none)
4 : 3	GCREGOVERLAYALPH-ABLENDCONFIG1_S-RC_GLOBAL_ALPHA_MODE	(none) Default Value: 0x0 **0x0: NORMAL :** (none) **0x1: GLOBAL :** (none) **0x2: SCALED :** (none)
1	GCREGOVERLAYALPH-ABLENDCONFIG1_S-RC_ALPHA_MODE	(none) Default Value: 0x0 **0x0: NORMAL :** (none) **0x1: INVERSED :** (none)
0	GCREGOVERLAYALPH-ABLENDCONFIG1_AL-PHA_BLEND	(none) Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)

27.1.84 GFXSS_DC_DCNANO_GCREGOVERLAYGLOBALALPHA1

Description: Overlay global alpha value. NOTE.. This register is double buffered.

Address: 0x448018D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYGLOBALALPHA1_SRC_ALPHA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYGLOBALALPHA1_DST_ALPHA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	GCREGOVERLAYGLOBALALPHA1_DST_ALPHA	(none) Default Value: 0x00
7 : 0	GCREGOVERLAYGLOBALALPHA1_SRC_ALPHA	(none) Default Value: 0x00

27.1.85 GFXSS_DC_DCNANO_GCREGOVERLAYCLEARVALUE1

Description: Overlay Clear Value Register. Clear value used when dcregOverlayConfig.Clear is enabled, Format is A8R8G8B8. NOTE.. This register is double buffered.

Address: 0x448018D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCLEARVALUE1_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCLEARVALUE1_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCLEARVALUE1_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGOVERLAYCLEARVALUE1_ALPHA [31:24]							

Bits	Name	Description
31 : 24	GCREGOVERLAY-CLEARVALUE1_ALPHA	8 bit alpha value. Default Value: 0x00
23 : 16	GCREGOVERLAY-CLEARVALUE1_RED	8 bit red color. Default Value: 0x00
15 : 8	GCREGOVERLAY-CLEARVALUE1_GREEN	8 bit green color. Default Value: 0x00
7 : 0	GCREGOVERLAY-CLEARVALUE1_BLUE	8 bit blue color. Default Value: 0x00

27.1.86 GFXSS_DC_DCNANO_GCREGDISPLAYDITHERTABLELOW

Description: Dither Threshold Table Register.

Address: 0x448018E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDISPLAYDITHERTABLELOW_Y0_X1 [7:4]				GCREGDISPLAYDITHERTABLELOW_Y0_X0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDISPLAYDITHERTABLELOW_Y0_X3 [15:12]				GCREGDISPLAYDITHERTABLELOW_Y0_X2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDISPLAYDITHERTABLELOW_Y1_X1 [23:20]				GCREGDISPLAYDITHERTABLELOW_Y1_X0 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDISPLAYDITHERTABLELOW_Y1_X3 [31:28]				GCREGDISPLAYDITHERTABLELOW_Y1_X2 [27:24]			

Bits	Name	Description
31 : 28	GCREGDISPLAYDITH-ERTABLELOW_Y1_X3	Dither threshold value for x,y=3,1. Default Value: 0x0
27 : 24	GCREGDISPLAYDITH-ERTABLELOW_Y1_X2	Dither threshold value for x,y=2,1. Default Value: 0x0
23 : 20	GCREGDISPLAYDITH-ERTABLELOW_Y1_X1	Dither threshold value for x,y=1,1. Default Value: 0x0
19 : 16	GCREGDISPLAYDITH-ERTABLELOW_Y1_X0	Dither threshold value for x,y=0,1. Default Value: 0x0
15 : 12	GCREGDISPLAYDITH-ERTABLELOW_Y0_X3	Dither threshold value for x,y=3,0. Default Value: 0x0
11 : 8	GCREGDISPLAYDITH-ERTABLELOW_Y0_X2	Dither threshold value for x,y=2,0. Default Value: 0x0
7 : 4	GCREGDISPLAYDITH-ERTABLELOW_Y0_X1	Dither threshold value for x,y=1,0. Default Value: 0x0
3 : 0	GCREGDISPLAYDITH-ERTABLELOW_Y0_X0	Dither threshold value for x,y=0,0. Default Value: 0x0

27.1.87 GFXSS_DC_DCNANO_GCREGDISPLAYDITHERTABLEHIGH

Description: Dither Threshold Table Register.

Address: 0x448018E4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDISPLAYDITHERTABLEHIGH_Y2_X1 [7:4]				GCREGDISPLAYDITHERTABLEHIGH_Y2_X0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDISPLAYDITHERTABLEHIGH_Y2_X3 [15:12]				GCREGDISPLAYDITHERTABLEHIGH_Y2_X2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDISPLAYDITHERTABLEHIGH_Y3_X1 [23:20]				GCREGDISPLAYDITHERTABLEHIGH_Y3_X0 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDISPLAYDITHERTABLEHIGH_Y3_X3 [31:28]				GCREGDISPLAYDITHERTABLEHIGH_Y3_X2 [27:24]			

Bits	Name	Description
31 : 28	GCREGDISPLAYDITH-ERTABLEHIGH_Y3_X3	Dither threshold value for x,y=3,3. Default Value: 0x0
27 : 24	GCREGDISPLAYDITH-ERTABLEHIGH_Y3_X2	Dither threshold value for x,y=2,3. Default Value: 0x0
23 : 20	GCREGDISPLAYDITH-ERTABLEHIGH_Y3_X1	Dither threshold value for x,y=1,3. Default Value: 0x0
19 : 16	GCREGDISPLAYDITH-ERTABLEHIGH_Y3_X0	Dither threshold value for x,y=0,3. Default Value: 0x0
15 : 12	GCREGDISPLAYDITH-ERTABLEHIGH_Y2_X3	Dither threshold value for x,y=3,2. Default Value: 0x0
11 : 8	GCREGDISPLAYDITH-ERTABLEHIGH_Y2_X2	Dither threshold value for x,y=2,2. Default Value: 0x0
7 : 4	GCREGDISPLAYDITH-ERTABLEHIGH_Y2_X1	Dither threshold value for x,y=1,2. Default Value: 0x0
3 : 0	GCREGDISPLAYDITH-ERTABLEHIGH_Y2_X0	Dither threshold value for x,y=0,2. Default Value: 0x0

27.1.88 GFXSS_DC_DCNANO_GCREGPANELCONFIG

Description: Panel Configuration Register.

Address: 0x448018E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	Reserved			RW	RW
HW Access	Reserved		R	Reserved			R	R
Name	Reserved [7:6]		GCREGPA-NELCON-FIG_DATA_POLARITY	Reserved [4:2]			GCREGPA-NELCON-FIG_DE_POLARITY	GCREGPA-NELCON-FIG_DE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [15:10]						GCREGPA-NELCON-FIG_CLOCK_POLARI-TY	GCREGPA-NELCON-FIG_CLOCK

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9	GCREGPANELCONFIG_-CLOCK_POLARITY	Clock polarity. Default Value: 0x0 **0x0: POSITIVE :** (none) **0x1: NEGATIVE :** (none)
8	GCREGPANELCONFIG_-CLOCK	Clock enable/disable. Default Value: 0x0 **0x0: DISABLED :** (none)

27.1.88 GFXSS_DC_DCNANO_GCREGPANELCONFIG (continued)

		0x1: ENABLED : (none)
5	GCREGPANELCONFIG_-DATA_POLARITY	Data polarity. Default Value: 0x0 **0x0: POSITIVE :** (none) **0x1: NEGATIVE :** (none)
1	GCREGPANELCON-FIG_DE_POLARITY	Data Enable polarity. Default Value: 0x0 **0x0: POSITIVE :** (none) **0x1: NEGATIVE :** (none)
0	GCREGPANELCON-FIG_DE	Data Enable enabled/disabled. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)

27.1.89 GFXSS_DC_DCNANO_GCREGPANELCONTROL

Description: Panel control Register.

Address: 0x448018EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						GCREGPANELCONTROL_BACK_PRESSURE_DISABLE	GCREGPANELCONTROL_VALID

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	GCREGPANELCONTROL_BACK_PRESSURE_DISABLE	Interface of DPI Default Value: 0x0 **0x0: NO :** (none) **0x1: YES :** (none)
0	GCREGPANELCONTROL_VALID	The valid field defines whether we can copy a new set of registers at the next VBLANK or not. This ensures a frame will always start with a valid working set if this register is programmed last, which reduces the need for SW to wait for the start of a VBLANK signal in order to ensure all states are loaded before the next VBLANK. Default Value: 0x0 **0x0: PENDING :** (none)

27.1.89 GFXSS_DC_DCNANO_GCREGPANELCONTROL (continued)

0x1: WORKING :

(none)

27.1.90 GFXSS_DC_DCNANO_GCREGPANELFUNCTION

Description: Panel function Register. NOTE.. This register is double buffered.

Address: 0x448018F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [7:3]					GCREG-PANEL-FUNCTION_DITHER	GCREG-PANEL-FUNCTION_GAMMA	GCREG-PANEL-FUNCTION_OUTPUT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	GCREGPANELFUNC-TION_DITHER	Enabling dithering allows R8G8B8 modes to show better on panels with less bits-per-pixel. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
1	GCREGPANELFUNC-TION_GAMMA	When Gamma is enabled, the R, G, and B channels will be routed through the Gamma LUT to perform gamma correction. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)

27.1.90 GFXSS_DC_DCNANO_GCREGPANELFUNCTION (continued)

0	GCREGPANELFUNC-TION_OUTPUT	When Output is enabled, pixels will be displayed. When Output is disabled, all pixels will be black. This allows a panel to have correct timing but without any pixels. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)

27.1.91 GFXSS_DC_DCNANO_GCREGPANELWORKING

Description: Register to trigger Display Controller.

Address: 0x448018F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							W
HW Access	Reserved							R
Name	Reserved [7:1]							GCREG-PANEL-WORKING_WORKING

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	GCREGPANELWORK-ING_WORKING	Writing a one in this register will force a reset of the display controller. All registers will be copied to the working set and counters will be reset to the end of HSYNC and VSYNC. Default Value: 0x0 **0x1: WORKING :** (none)

27.1.92 GFXSS_DC_DCNANO_GCREGPANELSTATE

Description: Register representing the Display Controller status. READ ONLY.

Address: 0x448018F8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				R	R	R	Reserved
HW Access	Reserved				W	W	W	Reserved
Name	Reserved [7:4]				GCREG-PANEL-STATE_OVER-LAY_UNDER_FLOW1	GCREG-PANEL-STATE_OVER-LAY_UNDER_FLOW	GCREG-PANEL-STATE_VIDEO-_UNDER_-FLOW	Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3	GCREGPANEL-STATE_OVER-LAY_UNDER_FLOW1	When the overlay FIFO underflows, this bit gets set to one. Reading this register will reset it back to zero. Default Value: 0x0 **0x0: NO :** (none) **0x1: YES :** (none)
2	GCREGPANEL-STATE_OVER-LAY_UNDER_FLOW	When the overlay FIFO underflows, this bit gets set to one. Reading this register will reset it back to zero. Default Value: 0x0 **0x0: NO :** (none)

27.1.92 GFXSS_DC_DCNANO_GCREGPANELSTATE (continued)

		0x1: YES : (none)
1	GCREGPANEL-STATE_VIDEO_UNDER_-FLOW	When the display FIFO underflows, this bit gets set to one. Reading this register will reset it back to zero. Default Value: 0x0 **0x0: NO :** (none) **0x1: YES :** (none)

27.1.93 GFXSS_DC_DCNANO_GCREGHDISPLAY

Description: Horizontal Display Total and Visible Pixel Count Register. Horizontal Total and Display End counters. NOTE.. This register is double buffered.

Address: 0x44801900

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGHDISPLAY_DISPLAY_END [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			GCREGHDISPLAY_DISPLAY_END [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGHDISPLAY_TOTAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [31:29]			GCREGHDISPLAY_TOTAL [28:24]				

Bits	Name	Description
28 : 16	GCREGHDISPLAY_TOTAL	Total number of horizontal pixels. NOTE: This field is double buffered. Default Value: 0x0000
12 : 0	GCREGHDISPLAY_DISPLAY_END	Number of visible horizontal pixels. NOTE: This field is double buffered. Default Value: 0x0000

27.1.94 GFXSS_DC_DCNANO_GCREGHSYNC

Description: Horizontal Sync Counter Register. Horizontal Sync counters. NOTE.. This register is double buffered.

Address: 0x44801904

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGHSYNC_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			GCREGHSYNC_START [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGHSYNC_END [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved	RW				
HW Access	R	R	Reserved	R				
Name	GCREGHSYNC_POLARITY	GCREGHSYNC_PULSE	Reserved	GCREGHSYNC_END [28:24]				

Bits	Name	Description
31	GCREGHSYNC_POLARITY	Polarity of the horizontal sync pulse. NOTE: This field is double buffered. Default Value: 0x0 **0x0: POSITIVE :** (none) **0x1: NEGATIVE :** (none)
30	GCREGHSYNC_PULSE	Horizontal sync pulse control. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
28 : 16	GCREGHSYNC_END	End of horizontal sync pulse. NOTE: This field is double buffered. Default Value: 0x0000

27.1.94 GFXSS_DC_DCNANO_GCREGHSYNC (continued)

12 : 0	GCREGHSYNC_START	Start of horizontal sync pulse. NOTE: This field is double buffered. Default Value: 0x0000

27.1.95 GFXSS_DC_DCNANO_GCREGVDISPLAY

Description: Vertical Total and Visible Pixel Count Register. Vertical Total and Display End counters. NOTE.. This register is double buffered.

Address: 0x44801910

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGVDISPLAY_DISPLAY_END [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				GCREGVDISPLAY_DISPLAY_END [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGVDISPLAY_TOTAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				GCREGVDISPLAY_TOTAL [27:24]			

Bits	Name	Description
27 : 16	GCREGVDISPLAY_TOTAL	Total number of vertical lines. NOTE: This field is double buffered. Default Value: 0x000
11 : 0	GCREGVDISPLAY_DISPLAY_END	Number of visible vertical lines. NOTE: This field is double buffered. Default Value: 0x000

27.1.96 GFXSS_DC_DCNANO_GCREGVSYNC

Description: Vertical Sync Counter Register. Vertical Sync counters. NOTE.. This register is double buffered.

Address: 0x44801914

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGVSYNC_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				GCREGVSYNC_START [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGVSYNC_END [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved		RW			
HW Access	R	R	Reserved		R			
Name	GCREGVSYNC_POLARITY	GCREGVSYNC_PULSE	Reserved [29:28]		GCREGVSYNC_END [27:24]			

Bits	Name	Description
31	GCREGVSYNC_POLARITY	Polarity of the vertical sync pulse. NOTE: This field is double buffered. Default Value: 0x0 **0x0: POSITIVE :** (none) **0x1: NEGATIVE :** (none)
30	GCREGVSYNC_PULSE	Vertical sync pulse control. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
27 : 16	GCREGVSYNC_END	End of the vertical sync pulse. NOTE: This field is double buffered. Default Value: 0x000

27.1.96 GFXSS_DC_DCNANO_GCREGVSYNC (continued)

11 : 0	GCREGVSYNC_START	Start of the vertical sync pulse. NOTE: This field is double buffered. Default Value: 0x000

27.1.97 GFXSS_DC_DCNANO_GCREGDISPLAYCURRENTLOCATION

Description: Display Current Location Register. Current x,y location of display controller. READ ONLY.

Address: 0x44801918

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDISPLAYCURRENTLOCATION_X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDISPLAYCURRENTLOCATION_X [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDISPLAYCURRENTLOCATION_Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDISPLAYCURRENTLOCATION_Y [31:24]							

Bits	Name	Description
31 : 16	GCREGDISPLAYCUR-RENTLOCATION_Y	Current Y location. Default Value: 0x0000
15 : 0	GCREGDISPLAYCUR-RENTLOCATION_X	Current X location. Default Value: 0x0000

27.1.98 GFXSS_DC_DCNANO_GCREGGAMMAINDEX

Description: Gamma Index Register. Index into gamma table. See gcregGammaData for more information.

Address: 0x4480191C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	GCREGGAMMAINDEX_INDEX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	GCREGGAMMAINDEX-_INDEX	Index into gamma table. Default Value: 0x00

27.1.99 GFXSS_DC_DCNANO_GCREGGAMMADATA

Description: Gamma Data Register. Translation values for the gamma table. When this register gets written, the data gets stored in the gamma table at the index specified by the gcregGammaIndex register. After the register is written, the index gets incremented.

Address: 0x44801920

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	GCREGGAMMADATA_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	GCREGGAMMADATA_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	GCREGGAMMADATA_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	GCREGGAMMADATA_RED	Red translation value. Default Value: 0x00
15 : 8	GCREGGAMMADATA_GREEN	Green translation value. Default Value: 0x00
7 : 0	GCREGGAMMADATA_BLUE	Blue translation value. Default Value: 0x00

27.1.100 GFXSS_DC_DCNANO_GCREGCURSORCONFIG

Description: Cursor Configuration Register. Configuration register for the cursor. Double-buffered values in this register cannot be read while a flip is in progress. NOTE.. This register is double buffered.

Address: 0x44801924

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						GCREGCURSORCON-FIG_FORMAT [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			GCREGCURSORCONFIG_HOT_SPOT_Y [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [23:21]			GCREGCURSORCONFIG_HOT_SPOT_X [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
20 : 16	GCREGCURSORCON-FIG_HOT_SPOT_X	Horizontal offset to cursor hotspot. NOTE: This field is double buffered. Default Value: 0x00
12 : 8	GCREGCURSORCON-FIG_HOT_SPOT_Y	Vertical offset to cursor hotspot. NOTE: This field is double buffered. Default Value: 0x00
1 : 0	GCREGCURSORCON-FIG_FORMAT	Format of the cursor. NOTE: This field is double buffered. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: MASKED :** (none) **0x2: A8R8G8B8 :** (none)

27.1.101 GFXSS_DC_DCNANO_GCREGCURSORADDRESS

Description: Cursor Base Address Register. Address of the cursor shape. NOTE.. This register is double buffered.

Address: 0x44801928

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGCURSORADDRESS_ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGCURSORADDRESS_ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGCURSORADDRESS_ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GCREGCURSORADDRESS_ADDRESS [31:24]							

Bits	Name	Description
31 : 0	GCREGCURSORAD-DRESS_ADDRESS	32 bit address. Default Value: 0x00000000

27.1.102 GFXSS_DC_DCNANO_GCREGCURSORLOCATION

Description: Cursor Location Register. Location of the cursor on the owning display. NOTE.. This register is double buffered.

Address: 0x4480192C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGCURSORLOCATION_X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			GCREGCURSORLOCATION_X [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGCURSORLOCATION_Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [31:28]				GCREGCURSORLOCATION_Y [27:24]			

Bits	Name	Description
27 : 16	GCREGCURSORLOCATION_Y	Y location of cursor's hotspot. NOTE: This field is double buffered. Default Value: 0x000
12 : 0	GCREGCURSORLOCATION_X	X location of cursor's hotspot. NOTE: This field is double buffered. Default Value: 0x0000

27.1.103 GFXSS_DC_DCNANO_GCREGCURSORBACKGROUND

Description: Cursor Background Color Register. The background color for Masked cursors. NOTE.. This register is double buffered.

Address: 0x44801930

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGCURSORBACKGROUND_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGCURSORBACKGROUND_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGCURSORBACKGROUND_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	GCREGCURSORBACK-GROUND_RED	Red value. NOTE: This field is double buffered. Default Value: 0x00
15 : 8	GCREGCURSORBACK-GROUND_GREEN	Green value. NOTE: This field is double buffered. Default Value: 0x00
7 : 0	GCREGCURSORBACK-GROUND_BLUE	Blue value. NOTE: This field is double buffered. Default Value: 0x00

27.1.104 GFXSS_DC_DCNANO_GCREGCURSORFOREGROUND

Description: Cursor Foreground Color Register. The foreground color for Masked cursors. NOTE.. This register is double buffered.

Address: 0x44801934

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGCURSORFOREGROUND_BLUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGCURSORFOREGROUND_GREEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GCREGCURSORFOREGROUND_RED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 16	GCREGCURSORFORE-GROUND_RED	Red value. NOTE: This field is double buffered. Default Value: 0x00
15 : 8	GCREGCURSORFORE-GROUND_GREEN	Green value. NOTE: This field is double buffered. Default Value: 0x00
7 : 0	GCREGCURSORFORE-GROUND_BLUE	Blue value. NOTE: This field is double buffered. Default Value: 0x00

27.1.105 GFXSS_DC_DCNANO_GCREGDISPLAYINTR

Description: Display Interrupt Register. This is the interrupt register for the Display. This register will automatically clear after a read. The interrupt bit is set when the current frame buffer is used up. The interrupt signal will be pulled up only when the interrupt enable bit in register gcregDisplayIntrEnable is enabled. READ ONLY. When the access comes from a debugger (HMASTER[0] == 1), the clear by read function is disabled.

Address: 0x44801938

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							GCREG-DISPLAYIN-TR_DISP0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R	Reserved			
HW Access	Reserved			W	Reserved			
Name	Reserved [15:13]			GCREG-DISPLAYIN-TR_DISP0_DBI_CF-G_ERROR	Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	Reserved				
HW Access	W	W	W	Reserved				
Name	GCREG-DISPLAYIN-TR_BUS_ERROR	GCREG-DISPLAYIN-TR_SOFT_RESET_-DONE	GCREG-DISPLAYIN-TR_PANEL_UNDER-FLOW	Reserved [28:24]				

Bits	Name	Description
31	GCREGDISPLAYIN-TR_BUS_ERROR	Bus error Default Value: 0x0
30	GCREGDISPLAYINTR_-SOFT_RESET_DONE	Soft reset done Default Value: 0x0
29	GCREGDISPLAYIN-TR_PANEL_UNDER-FLOW	Panel underflow intr. Default Value: 0x0
12	GCREGDISPLAYIN-TR_DISP0_DBI_CF-G_ERROR	Display0 DBI configure error Default Value: 0x0
0	GCREGDISPLAYIN-TR_DISP0	Display0 interrupt Default Value: 0x0

27.1.106 GFXSS_DC_DCNANO_GCREGDISPLAYINTRENABLE

Description: Display Interrupt Enable Register. The interrupt enable register for display_0 (and display_1 if present). NOTE.. Interrupt enable for register gcregDisplayIntr. NOTE.. This register is double buffered.

Address: 0x4480193C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							GCREG-DISPLAYIN-TRENABLE_DISP0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW	Reserved			
HW Access	Reserved			R	Reserved			
Name	Reserved [15:13]			GCREG-DISPLAYIN-TRENABLE_DISP0_D-BI_CF-G_ERROR	Reserved [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	Reserved				
HW Access	R	R	R	Reserved				
Name	GCREG-DISPLAYIN-TRENABLE_BUS_ER-ROR	GCREG-DISPLAYIN-TRENABLE_SOFT_RE-SET_DONE	GCREG-DISPLAYIN-TRENABLE_PAN-EL_UN-DERFLOW	Reserved [28:24]				

Bits	Name	Description
31	GCREGDISPLAYIN-TRENABLE_BUS_ER-ROR	Bus error enable NOTE: This field is double buffered. Default Value: 0x0
30	GCREGDISPLAYIN-TRENABLE_SOFT_RE-SET_DONE	Soft reset done enable NOTE: This field is double buffered. Default Value: 0x1
29	GCREGDISPLAYIN-TRENABLE_PANEL_UN-DERFLOW	Panel underflow intr enable. NOTE: This field is double buffered. Default Value: 0x0
12	GCREGDISPLAYIN-TRENABLE_DISP0_D-BI_CFG_ERROR	Display0 DBI configure error enable NOTE: This field is double buffered. Default Value: 0x0

27.1.106 GFXSS_DC_DCNANO_GCREGDISPLAYINTRENABLE (continued)

0	GCREGDISPLAYIN-TRENABLE_DISP0	Display0 interrupt enable NOTE: This field is double buffered. Default Value: 0x0

27.1.107 GFXSS_DC_DCNANO_GCREGDBICONFIG

Description: DBI Configuration Register. Configuration register for DBI output.

Address: 0x44801940

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW				RW	
HW Access	Reserved	R	R				R	
Name	Reserved	GCREGD-BICON-FIG_BUS_OUTPUT_-SEL	GCREGDBICONFIG_DBI_DATA_FORMAT [5:2]				GCREGDBICONFIG_D-BI_TYPE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW		RW			
HW Access	Reserved		R		R			
Name	Reserved [15:14]		GCREGDBICONFIG_D-BI_TYPEC_OPT [13:12]		GCREGDBICONFIG_DBI_AC_TIME_UNIT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
13 : 12	GCREGDBICONFIG_D-BI_TYPEC_OPT	Options for DBI Type C Interface Read/Write Sequence; 0: Option 1; 1: Option 2; 2: Option 3. Default Value: 0x0
11 : 8	GCREGDBICONFIG_D-BI_AC_TIME_UNIT	Time unit for AC characteristics Default Value: 0x0
6	GCREGDBICON-FIG_BUS_OUTPUT_SEL	Output bus select Default Value: 0x1 **0x0: DPI :** (none) **0x1: DBI :** (none)
5 : 2	GCREGDBICONFIG_D-BI_DATA_FORMAT	DBI interface data format. Refer to DBI specification section on Interface Color Coding for detail. Default Value: 0x0 **0x0: D8R3G3B2 :** (none)

27.1.107 GFXSS_DC_DCNANO_GCREGDBICONFIG (continued)

0x1: D8R4G4B4 :

(none)

0x2: D8R5G6B5 :

(none)

0x3: D8R6G6B6 :

(none)

0x4: D8R8G8B8 :

(none)

0x5: D9R6G6B6 :

(none)

0x6: D16R3G3B2 :

(none)

0x7: D16R4G4B4 :

(none)

0x8: D16R5G6B5 :

(none)

0x9: D16_R6_G6_B6_OP1 :

(none)

0xa: D16_R6_G6_B6_OP2 :

(none)

0xb: D16_R8_G8_B8_OP1 :

(none)

0xc: D16_R8_G8_B8_OP2 :

(none)

0xd: D1R5G6B5 :

(none)

0xe: D1R8G8B8 :

(none)

27.1.107 GFXSS_DC_DCNANO_GCREGDBICONFIG (continued)

1 : 0	GCREGDBICONFIG_DBI_TYPE	DBI Type select Default Value: 0x0 **0x0: TYPE_AFIXED_E :** (none) **0x1: TYPE_ACLOCK_E :** (none) **0x2: TYPE_B :** (none) **0x3: TYPE_C :** (none)

27.1.108 GFXSS_DC_DCNANO_GCREGDBIIFRESET

Description: DBI Reset Register. Reset DBI interface to idle state. WRITE ONLY.

Address: 0x44801944

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							W
HW Access	Reserved							R
Name	Reserved [7:1]							GCREGD-BIIFRE-SET_DBI_I F_LEVEL_ RESET

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	GCREGDBIIFRESET_D-BI_IF_LEVEL_RESET	Reset DBI interface to idle state Default Value: 0x0 **0x1: RESET :** (none)

27.1.109 GFXSS_DC_DCNANO_GCREGDBIWRCHAR1

Description: DBI Write AC Characteristics 1 Register. DBI write AC characteristics definition register 1

Address: 0x44801948

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGDBIWRCHAR1_DBI_WR_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDBIWRCHAR1_DBI_WR_CS_ASSERT [15:12]				GCREGDBIWRCHAR1_DBI_WR_EOR_WR_ASSERT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 12	GCREGDBI-WRCHAR1_D-BI_WR_CS_ASSERT	Cycle number=Setting*(DbiAcTimeUnit+1). 0: When Type A Fixed E mode: Time to assert CSX. 1: When Type A Clock E mode: Not used. 2: When Type B mode: Time to assert CSX. Default Value: 0x0
11 : 8	GCREGDBI-WRCHAR1_D-BI_WR_EOR_WR_ASSERT	Cycle number=Setting*(DbiAcTimeUnit+1). 0: When Type A Fixed E mode: Not used. 1: When Type A Clock E mode: Time to assert E. 2: When Type B mode: Time to assert WRX. Default Value: 0x0
7 : 0	GCREGDBI-WRCHAR1_DBI_WR_PE-RIOD	Single write period duration. Cycle number=Setting*(DbiAcTimeUnit+1). This field must be no less than 3. Default Value: 0x00

27.1.110 GFXSS_DC_DCNANO_GCREGDBIWRCHAR2

Description: DBI Write AC Characteristics 2 Register. DBI write AC characteristics definition register 2

Address: 0x4480194C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGDBIWRCHAR2_DBI_WR_EOR_WR_DE_ASRT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGDBIWRCHAR2_DBI_WR_CS_DE_ASRT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 8	GCREGDBI-WRCHAR2_D-BI_WR_CS_DE_ASRT	Cycle number=Setting*(DbiAcTimeUnit+1). 0: When type A fixed E mode: Time to de-assert CSX. 1: When type A clock E mode: Not used. 2: When type B mode: Time to de-assert CSX. Default Value: 0x00
7 : 0	GCREGDBI-WRCHAR2_D-BI_WR_EOR_WR_DE_ASRT	Cycle number=Setting*(DbiAcTimeUnit+1). 0: When Type A Fixed E mode: Not used. 1: When type A Clock E mode: Time to de-assert E. 2: When Type B mode: Time to de-assert WRX. Default Value: 0x00

27.1.111 GFXSS_DC_DCNANO_GCREGDBICMD

Description: DBI Command Control Register. DBI Command in/out port. Writes to this register will send command/data to the DBI port. WRITE ONLY.

Address: 0x44801950

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	GCREGDBICMD_DBI_COMMAND_WORD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	GCREGDBICMD_DBI_COMMAND_WORD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W		Reserved					
HW Access	R		Reserved					
Name	GCREGDBICMD_DBI_COMMANDFLAG [31:30]		Reserved [29:24]					

Bits	Name	Description

31 : 30	GCREGDBICMD_DBI_COMMANDFLAG	DBI command flag.
		Default Value: 0x0
		0x0: ADDRESS :
		//DBI_COMMAND_WORD will contain an address.
		0x1: WRITE_MEM_START :
		//Starts a write. Contents of DBI_COMMAND_WORD are ignored.
		0x2: PARAMETER_OR_DATA :
		//DBI_COMMAND_WORD will contain a parameter or data.

15 : 0	GCREGDBICMD_DBI_COMMAND_WORD	The type of data contained in this word is specified using DBI_COMMANDFLAG[bits 31:30]. For Type C Options 1 and 2: DBI_COMMAND_WORD[8] is used to indicate the polarity of D/CX. DBI_COMMAND_WORD[8] = 0 indicates DBI_COMMAND_WORD[7:0] is COMMAND WORD. DBI_COMMAND_WORD[8] = 1 indicates DBI_COMMAND_WORD[7:0] is DATA WORD. Default Value: 0x0000

27.1.112 GFXSS_DC_DCNANO_GCREGDPICONFIG

Description: DPI Configuration Register. The configuration register for DPI output. NOTE.. This register is double buffered.

Address: 0x44801954

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					GCREGDPICONFIG_DPI_DATA_FORMAT [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	GCREGDPICONFIG_DPI_DATA_FORMAT	DPI interface data format. Refer to DPI specification section for Interface Color Coding' for detail. NOTE: This field is double buffered. Default Value: 0x5 **0x0: D16CFG1 :** (none) **0x1: D16CFG2 :** (none) **0x2: D16CFG3 :** (none) **0x3: D18CFG1 :** (none) **0x4: D18CFG2 :** (none)

27.1.112 GFXSS_DC_DCNANO_GCREGDPICONFIG (continued)

0x5: D24 :

(none)

27.1.113 GFXSS_DC_DCNANO_GCREGDBITYPECCFG

Description: DBI Type C Timing Control Register. DBI Type C write timing definition.

Address: 0x44801958

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDBITYPECCFG_SCL_TWRL [7:4]				GCREGDBITYPECCFG_TAS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	GCREGDBITYPECCFG_SCL_TWRH [15:12]				GCREGDBITYPECCFG_SCL_TWRL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [23:20]				GCREGDBITYPECCFG_SCL_TWRH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
19 : 12	GCREGDBITYPECCF-G_SCL_TWRH	Divide counter for Twrh (SCL H duration (write)). Specifies how many sdaClk cycles in Twrh phase. SCL Twrh means number of DBI_AC_TIME_UNIT of sdaClk for scl staying high. This field need to be at least 1. Default Value: 0x00
11 : 4	GCREGDBITYPECCF-G_SCL_TWRL	Divide counter for Twrl (SCL L duration (write)). Specifies how many sdaClk cycles in Twrl phase. SCL Twrl means number of DBI_AC_TIME_UNIT of sdaClk for scl staying low This field needs to be at least 1. Default Value: 0x00
3 : 0	GCREGDBITYPECCFG_-TAS	Divide counter for Tas (address setup time). Specifies how many sdaClk cycles in Tas phase. DCX Tas means number of DBI_AC_TIME_UNIT of sdaClk to be ahead of scl. Only works for DBI TYPE C Option3. Option1/2 will ignore this setting. This field needs to be at least 1. Default Value: 0x0

27.1.114 GFXSS_DC_DCNANO_GCREGDCSTATUS

Description: Display Controller Status Register. READ ONLY.

Address: 0x4480195C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							GCREGDC-STATUS_D-BI_TYPEC_FIFO_FULL

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	GCREGDCSTATUS_D-BI_TYPEC_FIFO_FULL	DBI Type C afifo full. Default Value: 0x0

27.1.115 GFXSS_DC_DCNANO_GCREGSRCCONFIGENDIAN

Description: Endian control.

Address: 0x44801960

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						GCREGSRCCONFIGEN-DIAN_CONTROL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	GCREGSRCCONFIGEN-DIAN_CONTROL	Control source endian. Default Value: 0x0 **0x0: NO_SWAP :** No swapping. **0x1: SWAP_WORD :** Swap at 16-bit boundary: 0123 to 1032. **0x2: SWAP_DWORD :** Swap at 32-bit boundary: 0123 to 3210.

27.1.116 GFXSS_DC_DCNANO_GCREGSOFTRESET

Description: Soft reset. WRITE ONLY.

Address: 0x44801964

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							W
HW Access	Reserved							R
Name	Reserved [7:1]							GCREG-SOFT-RESET_RESET

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	GCREGSOFT-RESET_RESET	Writing a one in this register will force a soft reset of the display controller. Default Value: 0x0 **0x1: RESET :** (none)

27.1.117 GFXSS_DC_DCNANO_GCREGDCCONTROL

Description: Control register.

Address: 0x44801968

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW	Reserved		
HW Access	Reserved			R	R	Reserved		
Name	Reserved [7:5]			GCREGDC-CON-TROL_RAM_CLOCK_-GATING	GCREGDC-CON-TROL_DEBUG_REGIS-TER	Reserved [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	GCREGDCCON-TROL_RAM_CLOCK_-GATING	Enable or disable ram clock gating. Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
3	GCREGDCCON-TROL_DEBUG_REGIS-TER	Enable or disable the debug register. Default Value: 0x0 **0x0: DISABLED :** (none)

27.1.117 GFXSS_DC_DCNANO_GCREGDCCONTROL (continued)

0x1: ENABLED :

(none)

27.1.118 GFXSS_DC_DCNANO_GCREGREGISTERTIMINGCONTROL

Description: Timing control register.

Address: 0x4480196C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGREGISTERTIMINGCONTROL_FOR_PF1P [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GCREGREGISTERTIMINGCONTROL_FOR_RF2P [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW	RW	RW	RW		RW	
HW Access	Reserved	R	R	R	R		R	
Name	Reserved	GCRE-GREGIS-TERTIMING CON-TROL_LIG HT_SLEEP	GCRE-GREGIS-TERTIMING CON-TROL_DEE P_SLEEP	GCRE-GREGIS-TERTIMING CON-TROL_PO WER_DOW N	GCREGREGISTERTIM-INGCONTROL_-FAST_WTC [19:18]		GCREGREGISTERTIM-INGCONTROL_-FAST_RTC [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
22	GCREGREGISTERTIM-INGCON-TROL_LIGHT_SLEEP	(none) Default Value: 0x0
21	GCREGREGISTERTIM-INGCONTROL_DEEP-_SLEEP	(none) Default Value: 0x0
20	GCREGREGISTERTIM-INGCONTROL_POW-ER_DOWN	(none) Default Value: 0x0
19 : 18	GCREGREGISTERTIM-INGCONTROL_-FAST_WTC	(none) Default Value: 0x0
17 : 16	GCREGREGISTERTIM-INGCONTROL_-FAST_RTC	(none) Default Value: 0x0
15 : 8	GCREGREGISTERTIM-INGCONTROL_-FOR_RF2P	(none) Default Value: 0x00

27.1.118 GFXSS_DC_DCNANO_GCREGREGISTERTIMINGCONTROL (continued)

7 : 0	GCREGREGISTERTIM-INGCONTROL_-FOR_PF1P	(none) Default Value: 0x00

27.1.119 GFXSS_DC_DCNANO_GCREGDEBUGCOUNTERSELECT

Description: Debug Counter Select Register.

Address: 0x44801970

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GCREGDEBUGCOUNTERSELECT_SELECT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description

7 : 0	GCREGDEBUG-COUNTERSELECT_SE-LECT	Write a value to this field to pick up from 0~255 counters. Then the counter will be in gcregDe-bugCounterValue.
		Default Value: 0x00
		0x0: TOTAL_AXI_RD_REQ_CNT :
		//request number
		0x1: TOTAL_AXI_RD_LAST_CNT :
		//read return data last number
		0x2: TOTAL_AXI_REQ_BURST_CNT :
		//number of 8bytes of request bytes
		0x3: TOTAL_AXI_RD_BURST_CUNT :
		//number of 8bytes of read return data
		0x4: TOTAL_PIXEL_CNT :
		//total pixels sent

27.1.119 GFXSS_DC_DCNANO_GCREGDEBUGCOUNTERSELECT (continued)

0x5: TOTAL_FRAME_CNT :

//total frame sent

0x6: TOTAL_INPUT_DBI_CMD_CNT :

//total dbi input cmd

0x7: TOTAL_OUTPUT_DBI_CMD_CNT :

//total dbi output cmd

0x8: DEBUG_SIGNALS0 :

//debug signals

0xff: RESET_ALL_DEBUG_COUNTERS :

//reset all debug counters

27.1.120 GFXSS_DC_DCNANO_GCREGDEBUGCOUNTERVALUE

Description: Debug Counter Value Register. Debug Counter Value as specified in gcregDebugCounterSelect. READ ONLY

Address: 0x44801974

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGCOUNTERVALUE_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGCOUNTERVALUE_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGCOUNTERVALUE_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGCOUNTERVALUE_VALUE [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGCOUN-TERVALUE_VALUE	Selected debug counter value Default Value: 0x00000000

27.1.121 GFXSS_DC_DCNANO_GCREGLAYERCLOCKGATE

Description: Layer clock gater Register. disable video/overlay0/overlay1 clock gater

Address: 0x448019A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW	RW	RW
HW Access	Reserved					R	R	R
Name	Reserved [7:3]					GCREGLAYERCLOCK-GATE_DIS-ABLE_OVERLAY1_-CLK	GCREGLAYERCLOCK-GATE_DIS-ABLE_OVERLAY0_-CLK	GCREGLAYERCLOCK-GATE_DIS-ABLE_VIDEO_CLK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	GCREGLAYERCLOCK-GATE_DISABLE_OVER-LAY1_CLK	(none) Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)
1	GCREGLAYERCLOCK-GATE_DISABLE_OVER-LAY0_CLK	(none) Default Value: 0x0 **0x0: DISABLED :** (none)

27.1.121 GFXSS_DC_DCNANO_GCREGLAYERCLOCKGATE (continued)

		0x1: ENABLED : (none)
0	GCREGLAYERCLOCK-GATE_DIS-ABLE_VIDEO_CLK	(none) Default Value: 0x0 **0x0: DISABLED :** (none) **0x1: ENABLED :** (none)

27.1.122 GFXSS_DC_DCNANO_GCREGDEBUGTOTVIDEOREQ

Description: debug registers.. count video current frame number of requested burst. READ ONLY

Address: 0x448019A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTVIDEOREQ_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTVIDEOREQ_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTVIDEOREQ_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTVIDEOREQ_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGTOT-VIDEOREQ_NUM	(none) Default Value: 0x00000000

27.1.123 GFXSS_DC_DCNANO_GCREGDEBUGLSTVIDEOREQ

Description: debug registers.. count video last frame number of requested burst. READ ONLY

Address: 0x448019A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTVIDEOREQ_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTVIDEOREQ_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTVIDEOREQ_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTVIDEOREQ_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGLST-VIDEOREQ_NUM	(none) Default Value: 0x00000000

27.1.124 GFXSS_DC_DCNANO_GCREGDEBUGTOTVIDEORRB

Description: debug registers.. count video current frame number of returned burst. READ ONLY

Address: 0x448019AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTVIDEORRB_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTVIDEORRB_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTVIDEORRB_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTVIDEORRB_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGTOT-VIDEORRB_NUM	(none) Default Value: 0x00000000

27.1.125 GFXSS_DC_DCNANO_GCREGDEBUGLSTVIDEORRB

Description: debug registers.. count video last frame number of returned burst. READ ONLY

Address: 0x448019B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTVIDEORRB_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTVIDEORRB_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTVIDEORRB_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTVIDEORRB_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGLST-VIDEORRB_NUM	(none) Default Value: 0x00000000

27.1.126 GFXSS_DC_DCNANO_GCREGDEBUGTOTOVERLAY0REQ

Description: debug registers.. count overlay0 current frame number of requested burst. READ ONLY

Address: 0x448019B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY0REQ_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY0REQ_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY0REQ_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY0REQ_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUG-TOTOVERLAY0REQ_-NUM	(none) Default Value: 0x00000000

27.1.127 GFXSS_DC_DCNANO_GCREGDEBUGLSTOVERLAY0REQ

Description: debug registers.. count overlay0 last frame number of requested burst. READ ONLY

Address: 0x448019B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY0REQ_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY0REQ_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY0REQ_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY0REQ_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGLSTO-VERLAY0REQ_NUM	(none) Default Value: 0x00000000

27.1.128 GFXSS_DC_DCNANO_GCREGDEBUGTOTOVERLAY0RRB

Description: debug registers.. count overlay0 current frame number of returned burst. READ ONLY

Address: 0x448019BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY0RRB_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY0RRB_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY0RRB_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY0RRB_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUG-TOTOVERLAY0RRB_-NUM	(none) Default Value: 0x00000000

27.1.129 GFXSS_DC_DCNANO_GCREGDEBUGLSTOVERLAY0RRB

Description: debug registers.. count overlay0 last frame number of returned burst. READ ONLY

Address: 0x448019C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY0RRB_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY0RRB_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY0RRB_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY0RRB_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGLSTO-VERLAY0RRB_NUM	(none) Default Value: 0x00000000

27.1.130 GFXSS_DC_DCNANO_GCREGDEBUGTOTOVERLAY1REQ

Description: debug registers.. count overlay1 current frame number of requested burst. READ ONLY

Address: 0x448019C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY1REQ_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY1REQ_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY1REQ_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY1REQ_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUG-TOTOVERLAY1REQ_-NUM	(none) Default Value: 0x00000000

27.1.131 GFXSS_DC_DCNANO_GCREGDEBUGLSTOVERLAY1REQ

Description: debug registers.. count overlay1 last frame number of requested burst. READ ONLY

Address: 0x448019C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY1REQ_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY1REQ_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY1REQ_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY1REQ_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGLSTO-VERLAY1REQ_NUM	(none) Default Value: 0x00000000

27.1.132 GFXSS_DC_DCNANO_GCREGDEBUGTOTOVERLAY1RRB

Description: debug registers.. count overlay1 current frame number of returned burst. READ ONLY

Address: 0x448019CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY1RRB_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY1RRB_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY1RRB_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTOVERLAY1RRB_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUG-TOTOVERLAY1RRB_-NUM	(none) Default Value: 0x00000000

27.1.133 GFXSS_DC_DCNANO_GCREGDEBUGLSTOVERLAY1RRB

Description: debug registers.. count overlay1 last frame number of returned burst. READ ONLY

Address: 0x448019D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY1RRB_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY1RRB_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY1RRB_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTOVERLAY1RRB_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGLSTO-VERLAY1RRB_NUM	(none) Default Value: 0x00000000

27.1.134 GFXSS_DC_DCNANO_GCREGDEBUGTOTCURSORREQ

Description: debug registers.. count cursor current frame number of requested burst. READ ONLY

Address: 0x448019D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTCURSORREQ_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTCURSORREQ_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTCURSORREQ_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTCURSORREQ_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGTOTCUR-SORREQ_NUM	(none) Default Value: 0x00000000

27.1.135 GFXSS_DC_DCNANO_GCREGDEBUGLSTCURSORREQ

Description: debug registers.. count cursor last frame number of requested burst. READ ONLY

Address: 0x448019D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTCURSORREQ_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTCURSORREQ_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTCURSORREQ_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTCURSORREQ_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGLSTCUR-SORREQ_NUM	(none) Default Value: 0x00000000

27.1.136 GFXSS_DC_DCNANO_GCREGDEBUGTOTCURSORRRB

Description: debug registers.. count cursor current frame number of returned burst. READ ONLY

Address: 0x448019DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTCURSORRRB_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTCURSORRRB_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTCURSORRRB_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTCURSORRRB_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGTOTCUR-SORRRB_NUM	(none) Default Value: 0x00000000

27.1.137 GFXSS_DC_DCNANO_GCREGDEBUGLSTCURSORRRB

Description: debug registers.. count cursor last frame number of returned burst. READ ONLY

Address: 0x448019E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTCURSORRRB_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTCURSORRRB_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTCURSORRRB_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTCURSORRRB_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGLSTCUR-SORRRB_NUM	(none) Default Value: 0x00000000

27.1.138 GFXSS_DC_DCNANO_GCREGDEBUGTOTDCREQ

Description: debug registers.. count DC current frame number of requested burst. READ ONLY

Address: 0x448019E4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTDCREQ_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTDCREQ_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTDCREQ_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTDCREQ_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGTOTD-CREQ_NUM	(none) Default Value: 0x00000000

27.1.139 GFXSS_DC_DCNANO_GCREGDEBUGLSTDCREQ

Description: debug registers.. count DC last frame number of requested burst. READ ONLY

Address: 0x448019E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTDCREQ_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTDCREQ_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTDCREQ_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTDCREQ_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGLSTD-CREQ_NUM	(none) Default Value: 0x00000000

27.1.140 GFXSS_DC_DCNANO_GCREGDEBUGTOTDCRRB

Description: debug registers.. count DC current frame number of returned burst. READ ONLY

Address: 0x448019EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTDCRRB_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTDCRRB_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTDCRRB_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGTOTDCRRB_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGTOTD-CRRB_NUM	(none) Default Value: 0x00000000

27.1.141 GFXSS_DC_DCNANO_GCREGDEBUGLSTDCRRB

Description: debug registers.. count DC last frame number of returned burst. READ ONLY

Address: 0x448019F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTDCRRB_NUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTDCRRB_NUM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTDCRRB_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGLSTDCRRB_NUM [31:24]							

Bits	Name	Description
31 : 0	GCREGDEBUGLSTD-CRRB_NUM	(none) Default Value: 0x00000000

27.1.142 GFXSS_DC_DCNANO_GCREGDEBUGFRAMEANDMISFLAG

Description: debug registers. READ ONLY

Address: 0x448019F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R			R				R
HW Access	W			W				W
Name	GCREGDEBUGFRAMEANDMIS-FLAG_CURRENT_FRAME_CNT [7:5]			GCREGDEBUGFRAMEANDMISFLAG_CUR-RENT_MISMATCH_FLAG [4:1]				GCREGDE-BUG-FRAMEAN DMIS-FLAG_CUR RENT_MIS-MATCH_-FLAG_TOT AL

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	GCREGDEBUGFRAMEANDMISFLAG_CURRENT_FRAME_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R			R				R
HW Access	W			W				W
Name	GCREGDEBUGFRAMEANDMIS-FLAG_LAST_FRAME_CNT [23:21]			GCREGDEBUGFRAMEANDMISFLAG_LAST_MIS-MATCH_FLAG [20:17]				GCREGDE-BUG-FRAMEAN DMIS-FLAG_LAS T_MIS-MATCH_-FLAG_TOT AL

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	GCREGDEBUGFRAMEANDMISFLAG_LAST_FRAME_CNT [31:24]							

Bits	Name	Description
31 : 21	GCREGDEBUGFRAME-ANDMISFLAG_LAST_-FRAME_CNT	debug registers: count DC last frame number Default Value: 0x000
20 : 17	GCREGDEBUGFRAME-ANDMIS-FLAG_LAST_MISMATCH _FLAG	debug registers: indicate each layer last frame mismatch of request and rerurn back number Default Value: 0x0
16	GCREGDEBUGFRAME-ANDMIS-FLAG_LAST_MISMATCH _FLAG_TOTAL	debug registers: indicate DC last frame mismatch of request and rerurn back number Default Value: 0x0

27.1.142 GFXSS_DC_DCNANO_GCREGDEBUGFRAMEANDMISFLAG (continued)

15 : 5	GCREGDEBUGFRAME-ANDMISFLAG_CUR-RENT_FRAME_CNT	debug registers: count DC current frame number Default Value: 0x000
4 : 1	GCREGDEBUGFRAME-ANDMISFLAG_CUR-RENT_MISMATCH_FLAG	debug registers: indicate each layer current frame mismatch of request and rerurn back number Default Value: 0x0
0	GCREGDEBUGFRAME-ANDMISFLAG_CUR-RENT_MISMATCH_FLAG_TOTAL	debug registers: indicate DC current frame mismatch of request and rerurn back number Default Value: 0x0

27.1.143 GFXSS_MIPIDSI_MXMIPIDSI_CTL

Description: IP control.

Address: 0x44802000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	IP enable bit. When disabled (value 0), the functional state of the core is reset. That includes the MMIO map of the core (access results in an AHB error response). Registers of this map are still accesible then. Default Value: 0

27.1.144 GFXSS_MIPIDSI_MXMIPIDSI_CLK_CTL

Description: Clock control.

Address: 0x44802004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							CLK_CFG

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	CLK_CFG	Setup for DPHY configuration clock. Typical value is DIV2. Must only be set to DIV1 if the system clock is not faster than 52 MHz and has a duty cycle of 50%. Change only while IP is disabled. Default Value: 1 **0x0: SYS_DIV1 :** System clock. **0x1: SYS_DIV2 :** System clock divided by 2. Enforces correct duty cycle for the configuration clock.

27.1.145 GFXSS_MIPIDSI_MXMIPIDSI_INTR

Description: Interrupt status bits.

Address: 0x44802010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1C
HW Access	Reserved							RW1SC
Name	Reserved [7:1]							CORE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1C
HW Access	Reserved							RW1SC
Name	Reserved [15:9]							DBI_TE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW1C
HW Access	Reserved							RW1SC
Name	Reserved [23:17]							DPI_HALT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	DPI_HALT	Command transmission error occurred in DPI mode. A command initiated by the generic slave interface was too large for transmission during the blanking period of the video timing. Writing a '1' to this field resets the bit. Default Value: 0
8	DBI_TE	Tearing Effect was signalled by a display in DBI mode. Writing a '1' to this field resets the bit. Default Value: 0
0	CORE	The DSI Host Controller core has signalled an interrupt. Writing a '1' to this field resets the bit. Interrupt status inside the core is not affected by this. Default Value: 0

27.1.146 GFXSS_MIPIDSI_MXMIPIDSI_INTR_SET

Description: Interrupt set bits.

Address: 0x44802014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [7:1]							CORE_SET

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [15:9]							DBI_TE_SET

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW1S
HW Access	Reserved							A
Name	Reserved [23:17]							DPI_HALT_SET

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	DPI_HALT_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
8	DBI_TE_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
0	CORE_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

27.1.147 GFXSS_MIPIDSI_MXMIPIDSI_INTR_MASK

Description: Interrupt mask bits.

Address: 0x44802018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							CORE_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							DBI_TE_MASK

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							DPI_HALT_MASK

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	DPI_HALT_MASK	Mask for corresponding field in INTR register. Default Value: 0
8	DBI_TE_MASK	Mask for corresponding field in INTR register. Default Value: 0
0	CORE_MASK	Mask for corresponding field in INTR register. Default Value: 0

27.1.148 GFXSS_MIPIDSI_MXMIPIDSI_INTR_MASKED

Description: Interrupt masked bits.

Address: 0x4480201C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							CORE_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							DBI_TE_MASKED

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [23:17]							DPI_HALT_MASKED

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	DPI_HALT_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
8	DBI_TE_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
0	CORE_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0

27.1.149 GFXSS_MIPIDSI_MXMIPIDSI_DPI_CMD

Description: DPI command control.

Address: 0x44802020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							DPI_SHUT-DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							DPI_-COLOR-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	DPI_COLORMODE	Turns on/off the color reduction mode of a MIPI-DSI display in DPI mode. The bit is sampled with the next vertical synchronization pulse, so the video timing of the Display Controller must be active for at least one more frame. Polarity depends on the Host Controller configuration. Default Value: 0
0	DPI_SHUTDOWN	Turns on/off the shutdown mode of a MIPI-DSI display in DPI mode. The bit is sampled with the next vertical synchronization pulse, so the video timing of the Display Controller must be active for at least one more frame. Polarity depends on the Host Controller configuration. Default Value: 0

27.1.150 GFXSS_MIPIDSI_MXMIPIDSI_DBI_CMD

Description: DBI command control.

Address: 0x44802024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							DBI_RESET

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	DBI_RESET	Turns on/off the reset signal for a MIPI-DSI display in DBI mode (low active). The value must only be changed while no DBI command transmission is on-going. Default Value: 1

27.1.151 GFXSS_MIPIDSI_MXMIPIDSI_PHY_FREQ_RANGE

Description: PHY frequency range selection.

Address: 0x44802030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CFG_CLK_FREQ_RANGE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	HS_FREQ_RANGE [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14 : 8	HS_FREQ_RANGE	High-speed Frequency Range Selection. This signal should be set with the D-PHY in power-down and must not change during operation. This signal can be overridden through D-PHY test control registers. Default Value: 0
7 : 0	CFG_CLK_FRE-Q_RANGE	System clock frequency configuration preset. Should be set according to the following equation: cfgclkfreqrange[7:0] = round[(Fcfg_clk(MHz)-17)*4]. Default Value: 0x4C

27.1.152 GFXSS_MIPIDSI_MXMIPIDSI_BIST

Description: BIST control.

Address: 0x44802034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					R	R	RW
HW Access	Reserved					W	W	R
Name	Reserved [7:3]					OK	DONE	ON

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2	OK	Indicates the result status. '1' indicates BIST is successful and '0' indicates failure. Default Value: 1
1	DONE	Indicates running status. Value '1' Indicates BIST operation is completed. Default Value: 0
0	ON	Start/stop for the BIST operation. Assert value '1' to start. Default Value: 0

27.1.153 GFXSS_MIPIDSI_MXMIPIDSI_IO_CONTINUITY_TEST

Description: IO continuity test control.

Address: 0x44802038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							RW
HW Access	W							R
Name	DATA [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 1	DATA	Data to observe Default Value: 0
0	EN	Start/stop for IO continuity test. Assert value '1' to start. Default Value: 0

27.1.154 GFXSS_MIPIDSI_MXMIPIDSI_PLL_TEST_CONFIG1

Description: PLL-SoC interface configuration for Test.

Address: 0x4480203C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	PROP_CNTRL [7:6]		VCO_CNTRL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INT_CNTRL [15:12]				PROP_CNTRL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW		RW	
HW Access	R				R		R	
Name	CPBIAS_CNTRL [23:20]				GMP_CNTRL [19:18]		INT_CNTRL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [31:27]					CPBIAS_CNTRL [26:24]		

Bits	Name	Description
26 : 20	CPBIAS_CNTRL	Charge pump bias control This signal can be overridden through D-PHY test control registers. Default Value: 0
19 : 18	GMP_CNTRL	Control of the effective loop-filter resistance This signal can be overridden through D-PHY test control registers. Default Value: 0
17 : 12	INT_CNTRL	Integral charge pump current control This signal can be overridden through D-PHY test control registers. Default Value: 0
11 : 6	PROP_CNTRL	Proportional Charge Pump control This signal can be overridden through D-PHY test control registers Default Value: 0
5 : 0	VCO_CNTRL	VCO Internal Capacitance Control This signal can be overridden through D-PHY test control registers. Default Value: 0

27.1.155 GFXSS_MIPIDSI_MXMIPIDSI_PLL_TEST_CONFIG2

Description: PLL-SoC interface configuration for Test.

Address: 0x44802040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW				R	RW
HW Access	R		R				W	R
Name	PLL_M [7:6]		PLL_N [5:2]				LOCK_PLL	GP_-CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PLL_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	
HW Access	R	R	R	R	R	R	R	
Name	WAKEUP-PLL	TEST_STOP_CLK_EN	SHADOW_-CLEAR	PLL_SHAD-OW_CON-TROL	FORCE_LOCK	UP-DATEPLL	CLKSEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23	WAKEUPPLL	Wakeuppll signal should be set to 1'b1 during entire operation except when used as part of a relock procedure. This signal has override capability over the PLL boot FSM and allows to trigger a new relock sequence in the system. It is set to 1'b1 during normal operation and pulsed low during at least 1uS during relock sequence (to trigger a new PLL relock). Default Value: 1
22	TEST_STOP_CLK_EN	Stop clock signal for scan dump support. Default Value: 0
21	SHADOW_CLEAR	Set to '1' to clear shadow registers. Default Value: 1
20	PLL_SHADOW_CON-TROL	Selection of PLL configuration mechanism. PLL can be configured through D-PHY or through SoC control and shadow control registers: 0: SoC control and shadow registers 1: D-PHY test control register Default Value: 1
19	FORCE_LOCK	Force lock bit: 0 - according to lock detector-default 1 - lock indication forced Default Value: 0

27.1.155 GFXSS_MIPIDSI_MXMIPIDSI_PLL_TEST_CONFIG2 (continued)

18	UPDATEPLL	Control for PLL operation frequency updated. When exercised, PLL SoC control signals are latched to PLL shadow_registers to set PLL operating frequency. Default Value: 0
17 : 16	CLKSEL	Control of PLL clock output selection. 00 - Clocks stopped 01 - Clock generation 10 - Buffered clkext 11 - Forbidden Default Value: 1
15 : 6	PLL_M	Control of the Feedback Multiplication Ratio M This signal can be overridden through D-PHY test control registers. Default Value: 0
5 : 2	PLL_N	Control of the Input Frequency Division Ratio N This signal can be overridden through D-PHY test control registers. Default Value: 0
1	LOCK_PLL	Lock State Signaling. 0: PLL is not locked 1: PLL is locked Default Value: 0
0	GP_CLK_EN	Enable signal for clkout_gp clock Default Value: 0

27.1.156 GFXSS_MIPIDSI_MXMIPIDSI_PLL_TEST_OBS1

Description: PLL Test Observation bits.

Address: 0x44802044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R					
HW Access	W		W					
Name	PROP_CNTRL_OBS [7:6]		VCO_CNTRL_OBS [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	W				W			
Name	INT_CNTRL_OBS [15:12]				PROP_CNTRL_OBS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R		R	
HW Access	W				W		W	
Name	CPBIAS_CNTRL_OBS [23:20]				GMP_CNTRL_OBS [19:18]		INT_CNTRL_OBS [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved					R		
HW Access	Reserved					W		
Name	Reserved [31:27]					CPBIAS_CNTRL_OBS [26:24]		

Bits	Name	Description
26 : 20	CPBIAS_CNTRL_OBS	Used for SOC observability of the cpbias_cntrl_obs that is controlling the PLL. Default Value: 0
19 : 18	GMP_CNTRL_OBS	Used for SOC observability of the gmp_cntrl_obs that is controlling the PLL. Default Value: 0
17 : 12	INT_CNTRL_OBS	Used for SOC observability of the int_cntrl_obs that is controlling the PLL. Default Value: 0
11 : 6	PROP_CNTRL_OBS	Used for SOC observability of the prop_cntrl_obs that is controlling the PLL. Default Value: 0
5 : 0	VCO_CNTRL_OBS	Output of multiplexer controlled by pll_shadow_control signal. This output signal represents the control signal provided by PHY test control registers or SoC control depending on pll_shadow_control selection. Used for SOC observability of the vco_cntrl_obs that is controlling the PLL Default Value: 0

27.1.157 GFXSS_MIPIDSI_MXMIPIDSI_PLL_TEST_OBS2

Description: PLL Test Observation bits.

Address: 0x44802048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PLL_M_OBS [7:4]				PLL_N_OBS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	R	R					
HW Access	Reserved	W	W					
Name	Reserved	PLL_SHAD-OW_CON-TROL_OBS	PLL_M_OBS [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14	PLL_SHADOW_CON-TROL_OBS	Used for SOC observability of the pll_shadow_control_obs that is controlling the PLL Default Value: 1
13 : 4	PLL_M_OBS	Used for SOC observability of the m_obs that is controlling the PLL. Default Value: 0
3 : 0	PLL_N_OBS	Output of multiplexer controlled by pll_shadow_control signal. This output signal represents the control signal provided by PHY test control registers or SoC control depending on pll_shadow_control selection. Used for SOC observability of the n_obs that is controlling the PLL. Default Value: 0

27.1.158 GFXSS_MIPIDSI_MXMIPIDSI_LP_INTERNAL_LOOPBACK_TEST

Description: Low Power internal Loopback Test

Address: 0x4480204C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							R
HW Access	W							W
Name	RXDATAESC [7:1]							RXDA-TAESC_VALID

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			R				R
HW Access	Reserved			W				W
Name	Reserved [15:13]			RXTRIGGERESC [12:9]				RXDA-TAESC

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12 : 9	RXTRIGGERESC	Received low power internal loopback data on rxtriggeresc. The TX data can be sent by writing to PHY_TX_TRIGGERS register (one hot encoded) Default Value: 0
8 : 1	RXDATAESC	Received low power internal loopback data on rxdataesc. The SW can configure the Generic interface to send short packet with payload size of 2 bytes and the first byte sent would appear on this field, if received successfully. Default Value: 0
0	RXDATAESC_VALID	Indicate that rxdatasec field is valid. SW can poll this bit before reading the rxdatasec field Default Value: 0

27.1.159 GFXSS_MIPIDSI_DWCMIPIDSI_VERSION

Description: Contains the version of the DSI host controller.

Address: 0x44803000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VERSION_VERSION [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VERSION_VERSION [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VERSION_VERSION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VERSION_VERSION [31:24]							

Bits	Name	Description
31 : 0	VERSION_VERSION	This field indicates the version of the DWC_mipi_dsi_host. Default Value: 0x30313531

27.1.160 GFXSS_MIPIDSI_DWCMIPIDSI_PWR_UP

Description: Controls the power up of the controller.

Address: 0x44803004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							RW
HW Access	R							R
Name	PWR_UP_RESERVED_31_1 [7:1]							PWR_UP_SHUT-DOWNZ

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PWR_UP_RESERVED_31_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PWR_UP_RESERVED_31_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PWR_UP_RESERVED_31_1 [31:24]							

Bits	Name	Description
31 : 1	PWR_UP_RE-SERVED_31_1	Reserved and read as zero. Default Value: 0x0
0	PWR_UP_SHUTDOWNZ	This bit configures the controller either to power up or to reset. Default Value: 0x0 **0x1: POWERUP :** (none) **0x0: RESET :** (none)

27.1.161 GFXSS_MIPIDSI_DWCMIPIDSI_CLKMGR_CFG

Description: Configures the factor for internal dividers to divide lanebyteclk for timeout purposes.

Address: 0x44803008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLKMGR_CFG_TX_ESC_CLK_DIVISION [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CLKMGR_CFG_TO_CLK_DIVISION [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	CLKMGR_CFG_RESERVED_31_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	CLKMGR_CFG_RESERVED_31_16 [31:24]							

Bits	Name	Description
31 : 16	CLKMGR_CFG_RESERVED_31_16	Reserved and read as zero. Default Value: 0x0
15 : 8	CLKMGR_CFG_TO_CLK_DIVISION	This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of high-speed to low-power and low-power to high-speed transition error. Default Value: 0x0
7 : 0	CLKMGR_CFG_TX_ESC_CLK_DIVISION	This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation. Default Value: 0x0

27.1.162 GFXSS_MIPIDSI_DWCMIPIDSI_DPI_VCID

Description: Configures the Virtual Channel ID for DPI traffic.

Address: 0x4480300C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						RW	
HW Access	R						R	
Name	DPI_VCID_RESERVED_31_2 [7:2]						DPI_VCID_DPI_VCID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	DPI_VCID_RESERVED_31_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	DPI_VCID_RESERVED_31_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DPI_VCID_RESERVED_31_2 [31:24]							

Bits	Name	Description
31 : 2	DPI_VCID_RESERVED_31_2	Reserved and read as zero. Default Value: 0x0
1 : 0	DPI_VCID_DPI_VCID	This field configures the DPI virtual channel id that is indexed to the Video mode packets. Default Value: 0x0

27.1.163 GFXSS_MIPIDSI_DWCMIPIDSI_DPI_COLOR_CODING

Description: Configures DPI color coding.

Address: 0x44803010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				RW			
HW Access	R				R			
Name	DPI_COLOR_CODING_RESERVED_7_4 [7:4]				DPI_COLOR_CODING_DPI_COLOR_CODING [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							RW
HW Access	R							R
Name	DPI_COLOR_CODING_RESERVED_31_9 [15:9]							DPI_COLOR_CODING_LOOSELY18_EN

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	DPI_COLOR_CODING_RESERVED_31_9 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DPI_COLOR_CODING_RESERVED_31_9 [31:24]							

Bits	Name	Description
31 : 9	DPI_COLOR_CODING_RESERVED_31_9	Reserved and read as zero. Default Value: 0x0
8	DPI_COLOR_CODING_LOOSELY18_EN	When set to 1, this bit activates loosely packed variant to 18-bit configurations. Default Value: 0x0
7 : 4	DPI_COLOR_CODING_RESERVED_7_4	Reserved and read as zero. Default Value: 0x0
3 : 0	DPI_COLOR_CODING_DPI_COLOR_CODING	This field configures the DPI color for Video Mode/eDPI Command Mode coding as follows: Default Value: 0x0 **0x0: CC00 :** (none) **0x1: CC01 :** (none) **0x2: CC02 :** (none)

27.1.163 GFXSS_MIPIDSI_DWCMIPIDSI_DPI_COLOR_CODING (continued)

0x3: CC03 :

(none)

0x4: CC04 :

(none)

0x5: CC05 :

(none)

0x6: CC06 :

(none)

0x7: CC07 :

(none)

0x8: CC08 :

(none)

0x9: CC09 :

(none)

0xa: CC10 :

(none)

0xb: CC11 :

(none)

0xc: CC12 :

(none)

0xd: CC13 :

(none)

0xe: CC14 :

(none)

0xf: CC15 :

(none)

27.1.164 GFXSS_MIPIDSI_DWCMIPIDSI_DPI_CFG_POL

Description: Configures the polarity of DPI signals.

Address: 0x44803014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R			RW	RW	RW	RW	RW
HW Access	R			R	R	R	R	R
Name	DPI_CFG_POL_RESERVED_31_5 [7:5]			DPI_CFG_POL_COLORM_ACTIVE_LOW	DPI_CFG_POL_SHUTD_ACTIVE_LOW	DPI_CFG_POL_HSYNC_ACTIVE_LOW	DPI_CFG_POL_VSYNC_ACTIVE_LOW	DPI_CFG_POL_DATAEN_ACTIVE_LOW

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	DPI_CFG_POL_RESERVED_31_5 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	DPI_CFG_POL_RESERVED_31_5 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DPI_CFG_POL_RESERVED_31_5 [31:24]							

Bits	Name	Description
31 : 5	DPI_CFG_POL_RESERVED_31_5	Reserved and read as zero. Default Value: 0x0
4	DPI_CFG_POL_COLORM_ACTIVE_LOW	When set to 1, this bit configures the color mode pin (dpicolorm) as active low. Default Value: 0x0
3	DPI_CFG_POL_SHUTD_ACTIVE_LOW	When set to 1, this bit configures the shutdown pin (dpishutdn) as active low. Default Value: 0x0
2	DPI_CFG_POL_HSYNC_ACTIVE_LOW	When set to 1, this bit configures the horizontal synchronism pin (dpihsync) as active low. Default Value: 0x0
1	DPI_CFG_POL_VSYNC_ACTIVE_LOW	When set to 1, this bit configures the vertical synchronism pin (dpivsync) as active low. Default Value: 0x0
0	DPI_CFG_POL_DATAEN_ACTIVE_LOW	When set to 1, this bit configures the data enable pin (dpidataen) as active low. Default Value: 0x0

27.1.165 GFXSS_MIPIDSI_DWCMIPIDSI_DPI_LP_CMD_TIM

Description: Configures the timing for low-power commands sent while in video mode.

Address: 0x44803018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DPI_LP_CMD_TIM_INVACT_LPCMD_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	DPI_LP_CMD_TIM_RESERVED_15_8 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DPI_LP_CMD_TIM_OUTVACT_LPCMD_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DPI_LP_CMD_TIM_RESERVED_31_24 [31:24]							

Bits	Name	Description
31 : 24	DPI_LP_CMD_TIM_RESERVED_31_24	Reserved and read as zero. Default Value: 0x0
23 : 16	DPI_LP_CMD_TIM_OUTVACT_LPCMD_TIME	This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions. Default Value: 0x0
15 : 8	DPI_LP_CMD_TIM_RESERVED_15_8	Reserved and read as zero. Default Value: 0x0
7 : 0	DPI_LP_CMD_TIM_INVACT_LPCMD_TIME	This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region. Default Value: 0x0

27.1.166 GFXSS_MIPIDSI_DWCMIPIDSI_DBI_VCID

Description: Configures Virtual Channel ID for DBI traffic.

Address: 0x4480301C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						RW	
HW Access	R						R	
Name	DBI_VCID_RESERVED_31_2 [7:2]						DBI_VCID_DBI_VCID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	DBI_VCID_RESERVED_31_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	DBI_VCID_RESERVED_31_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DBI_VCID_RESERVED_31_2 [31:24]							

Bits	Name	Description
31 : 2	DBI_VCID_RESERVED_31_2	Reserved and read as zero. Default Value: 0x0
1 : 0	DBI_VCID_DBI_VCID	This field configures the virtual channel id that is indexed to the DCS packets from DBI. Default Value: 0x0

27.1.167 GFXSS_MIPIDSI_DWCMIPIDSI_DBI_CFG

Description: Configures the bit width of pixels for DBI.

Address: 0x44803020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				RW			
HW Access	R				R			
Name	DBI_CFG_RESERVED_7_4 [7:4]				DBI_CFG_IN_DBI_CONF [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				RW			
HW Access	R				R			
Name	DBI_CFG_RESERVED_15_12 [15:12]				DBI_CFG_OUT_DBI_CONF [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R						RW	
HW Access	R						R	
Name	DBI_CFG_RESERVED_31_18 [23:18]						DBI_CFG_LUT_SIZE_-CONF [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DBI_CFG_RESERVED_31_18 [31:24]							

Bits	Name	Description
31 : 18	DBI_CFG_RE-SERVED_31_18	Reserved and read as zero. Default Value: 0x0
17 : 16	DBI_CFG_LUT_SIZE_-CONF	This field configures the size used to transport the Write Lut commands as follows: Default Value: 0x0 **0x0: LUTSIZE0 :** (none) **0x1: LUTSIZE1 :** (none) **0x2: LUTSIZE2 :** (none) **0x3: LUTSIZE3 :** (none)
15 : 12	DBI_CFG_RE-SERVED_15_12	Reserved and read as zero. Default Value: 0x0

27.1.167 GFXSS_MIPIDSI_DWCMIPIDSI_DBI_CFG (continued)

11 : 8	DBI_CFG_OUT_DBI_-CONF	This field configures the DBI output pixel data as follows: Default Value: 0x0 **0x0: PIXELDATA0 :** (none) **0x1: PIXELDATA1 :** (none) **0xa: PIXELDATA10 :** (none) **0xb: PIXELDATA11 :** (none) **0xc: PIXELDATA12 :** (none) **0x2: PIXELDATA2 :** (none) **0x3: PIXELDATA3 :** (none) **0x4: PIXELDATA4 :** (none) **0x5: PIXELDATA5 :** (none) **0x6: PIXELDATA6 :** (none) **0x7: PIXELDATA7 :** (none) **0x8: PIXELDATA8 :** (none) **0x9: PIXELDATA9 :** (none)
7 : 4	DBI_CFG_RE-SERVED_7_4	Reserved and read as zero. Default Value: 0x0

27.1.167 GFXSS_MIPIDSI_DWCMIPIDSI_DBI_CFG (continued)

3 : 0	DBI_CFG_IN_DBI_CONF	This field configures the DBI input pixel data as follows: Default Value: 0x0 **0x0: PIXELDATA0 :** (none) **0x1: PIXELDATA1 :** (none) **0xa: PIXELDATA10 :** (none) **0xb: PIXELDATA11 :** (none) **0xc: PIXELDATA12 :** (none) **0x2: PIXELDATA2 :** (none) **0x3: PIXELDATA3 :** (none) **0x4: PIXELDATA4 :** (none) **0x5: PIXELDATA5 :** (none) **0x6: PIXELDATA6 :** (none) **0x7: PIXELDATA7 :** (none) **0x8: PIXELDATA8 :** (none) **0x9: PIXELDATA9 :** (none)

27.1.168 GFXSS_MIPIDSI_DWCMIPIDSI_DBI_PARTITIONING_EN

Description: Configures whether DWC_mipi_dsi_host is to partition DBI traffic automatically.

Address: 0x44803024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							RW
HW Access	R							R
Name	DBI_PARTITIONING_EN_RESERVED_31_1 [7:1]							DBI_PARTITION-ING_EN_PARTITION-ING_EN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	DBI_PARTITIONING_EN_RESERVED_31_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	DBI_PARTITIONING_EN_RESERVED_31_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DBI_PARTITIONING_EN_RESERVED_31_1 [31:24]							

Bits	Name	Description
31 : 1	DBI_PARTITION-ING_EN_RE-SERVED_31_1	Reserved and read as zero. Default Value: 0x0
0	DBI_PARTITION-ING_EN_PARTITION-ING_EN	When set to 1, this bit enables the use of write_memory_continue input commands (system needs to ensure correct partitioning of Long Write commands). When not set, partitioning is automatically performed in the DWC_mipi_dsi_host. Default Value: 0x0

27.1.169 GFXSS_MIPIDSI_DWCMIPIDSI_DBI_CMDSIZE

Description: Configures the command size and the size for automatic partitioning of DBI packets.

Address: 0x44803028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DBI_CMDSIZE_WR_CMD_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DBI_CMDSIZE_WR_CMD_SIZE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DBI_CMDSIZE_ALLOWED_CMD_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DBI_CMDSIZE_ALLOWED_CMD_SIZE [31:24]							

Bits	Name	Description
31 : 16	DBI_CMDSIZE_ALLOWED_CMD_SIZE	This field configures the maximum allowed size for a DCS write memory command. This field is used to partition a write memory command into one write_memory_start and a variable number of write_memory_continue commands. It is only used if the partitioning_en bit of the DBI_CFG register is disabled. The size of the DSI packet payload is the actual payload size minus 1, because the DCS command is in the DSI packet payload. Default Value: 0x0
15 : 0	DBI_CMDSIZE_WR_CMD_SIZE	This field configures the size of the DCS write memory commands. The size of DSI packet payload is the actual payload size minus 1, because the DCS command is in the DSI packet payload. Default Value: 0x0

27.1.170 GFXSS_MIPIDSI_DWCMIPIDSI_PCKHDL_CFG

Description: Configures how EoTp, BTA, CRC and ECC are to be used, to meet peripherals characteristics

Address: 0x4480302C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		RW	RW	RW	RW	RW	RW
HW Access	R		R	R	R	R	R	R
Name	PCKHDL_CFG_RESERVED_31_6 [7:6]		PCKHDL_CFG_EOTP_TX_LP_EN	PCKHDL_CFG_CRC_RX_EN	PCKHDL_CFG_ECC_RX_EN	PCKHDL_CFG_BTA_EN	PCKHDL_CFG_EOTP_RX_EN	PCKHDL_CFG_EOTP_TX_EN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PCKHDL_CFG_RESERVED_31_6 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PCKHDL_CFG_RESERVED_31_6 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PCKHDL_CFG_RESERVED_31_6 [31:24]							

Bits	Name	Description
31 : 6	PCKHDL_CFG_RESERVED_31_6	Reserved and read as zero. Default Value: 0x0
5	PCKHDL_CFG_EOTP_TX_LP_EN	When set to 1, this bit enables the EoTp transmission in low-power. Default Value: 0x0
4	PCKHDL_CFG_CRC_RX_EN	When set to 1, this bit enables the CRC reception and error reporting. Default Value: 0x0
3	PCKHDL_CFG_ECC_RX_EN	When set to 1, this bit enables the ECC reception, error correction, and reporting. Default Value: 0x0
2	PCKHDL_CFG_BTA_EN	When set to 1, this bit enables the Bus Turn-Around (BTA) request. Default Value: 0x0
1	PCKHDL_CFG_EOTP_RX_EN	When set to 1, this bit enables the EoTp reception. Default Value: 0x0
0	PCKHDL_CFG_EOTP_TX_EN	When set to 1, this bit enables the EoTp transmission in high-speed. Default Value: 0x0

27.1.171 GFXSS_MIPIDSI_DWCMIPIDSI_GEN_VCID

Description: Configures the Virtual Channel ID of READ responses to store and return to Generic interface.

Address: 0x44803030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						RW	
HW Access	R						R	
Name	GEN_VCID_RESERVED_7_2 [7:2]						GEN_VCID_-GEN_VCID_RX [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R						RW	
HW Access	R						R	
Name	GEN_VCID_RESERVED_15_10 [15:10]						GEN_VCID_-GEN_VCID_TEAR_AUTO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R						RW	
HW Access	R						R	
Name	GEN_VCID_RESERVED_31_18 [23:18]						GEN_VCID_-GEN_VCID_TX_AUTO [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	GEN_VCID_RESERVED_31_18 [31:24]							

Bits	Name	Description
31 : 18	GEN_VCID_RE-SERVED_31_18	Reserved and read as zero. Default Value: 0x0
17 : 16	GEN_VCID_-GEN_VCID_TX_AUTO	This field indicates the Generic interface virtual channel identification where generic packet is automatically generated & transmitted. Default Value: 0x0
15 : 10	GEN_VCID_RE-SERVED_15_10	Reserved and read as zero. Default Value: 0x0
9 : 8	GEN_VCID_-GEN_VCID_TEAR_AUTO	This field indicates the virtual channel identification for tear effect by hardware Default Value: 0x0
7 : 2	GEN_VCID_RE-SERVED_7_2	Reserved and read as zero. Default Value: 0x0
1 : 0	GEN_VCID_-GEN_VCID_RX	This field indicates the Generic interface read-back virtual channel identification. Default Value: 0x0

27.1.172 GFXSS_MIPIDSI_DWCMIPIDSI_MODE_CFG

Description: Configures the mode of operation between Video or Command Mode. (Commands can still be sent while in video mode.)

Address: 0x44803034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							RW
HW Access	R							R
Name	MODE_CFG_RESERVED_31_1 [7:1]							MODE_CFG_CMD_VIDEO_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MODE_CFG_RESERVED_31_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	MODE_CFG_RESERVED_31_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	MODE_CFG_RESERVED_31_1 [31:24]							

Bits	Name	Description
31 : 1	MODE_CFG_RESERVED_31_1	Reserved and read as zero. Default Value: 0x0
0	MODE_CFG_CMD_VIDEO_MODE	This bit configures the operation mode: Default Value: 0x1 **0x1: CMDMODE :** (none) **0x0: VIDMODE :** (none)

27.1.173 GFXSS_MIPIDSI_DWCMIPIDSI_VID_MODE_CFG

Description: Configures several aspects of Video mode operation, the transmission mode, switching to low-power in the middle of a frame, enabling acknowledge and whether to send commands in low-power.

Address: 0x44803038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						RW	
HW Access	R						R	
Name	VID_MODE_CFG_RESERVED_7_2 [7:2]						VID_MODE_CFG_VID_-MODE_TYPE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VID_-MODE_CF-G_LP_CMD_EN	VID_-MODE_CF-G_FRAME_BTA_ACK_EN	VID_-MODE_CF-G_LP_HFP_EN	VID_-MODE_CF-G_LP_HBP_EN	VID_-MODE_CF-G_LP_VACT_EN	VID_-MODE_CF-G_LP_VFP_EN	VID_-MODE_CF-G_LP_VBP_EN	VID_-MODE_CF-G_LP_VSA_EN

Bits	23	22	21	20	19	18	17	16
SW Access	R			RW	R			RW
HW Access	R			R	R			R
Name	VID_MODE_CFG_RESERVED_23_21 [23:21]			VID_-MODE_CF-G_VPG_MODE	VID_MODE_CFG_RESERVED_19_17 [19:17]			VID_-MODE_CF-G_VPG_EN

Bits	31	30	29	28	27	26	25	24
SW Access	R							RW
HW Access	R							R
Name	VID_MODE_CFG_RESERVED_31_25 [31:25]							VID_-MODE_CF-G_VPG_ORIENTATION

Bits	Name	Description
31 : 25	VID_MODE_CFG_RE-SERVED_31_25	Reserved and read as zero. Default Value: 0x0
24	VID_MODE_CFG_VP-G_ORIENTATION	This field indicates the color bar orientation as follows: Default Value: 0x0 **0x0: VPGORENT0 :** (none) **0x1: VPGORENT1 :** (none)
23 : 21	VID_MODE_CFG_RE-SERVED_23_21	Reserved and read as zero. Default Value: 0x0

27.1.173 GFXSS_MIPIDSI_DWCMIPIDSI_VID_MODE_CFG (continued)

20	VID_MODE_CFG_VPG_-MODE	This field is to select the pattern: Default Value: 0x0 **0x1: BERPATTERN :** (none) **0x0: COLORBAR :** (none)
19 : 17	VID_MODE_CFG_RE-SERVED_19_17	Reserved and read as zero. Default Value: 0x0
16	VID_MODE_CFG_VP-G_EN	When set to 1, this bit enables the video mode pattern generator. Default Value: 0x0
15	VID_MODE_CFG_LP_C-MD_EN	When set to 1, this bit enables the command transmission only in low-power mode. Default Value: 0x0
14	VID_MODE_CFG_-FRAME_BTA_ACK_EN	When set to 1, this bit enables the request for an acknowledge response at the end of a frame. Default Value: 0x0
13	VID_MODE_CFG_LP_HF-P_EN	When set to 1, this bit enables the return to low-power inside the HFP period when timing allows. Default Value: 0x0
12	VID_MODE_CF-G_LP_HBP_EN	When set to 1, this bit enables the return to low-power inside the HBP period when timing allows. Default Value: 0x0
11	VID_MODE_CF-G_LP_VACT_EN	When set to 1, this bit enables the return to low-power inside the VACT period when timing allows. Default Value: 0x0
10	VID_MODE_CFG_LP_VF-P_EN	When set to 1, this bit enables the return to low-power inside the VFP period when timing allows. Default Value: 0x0
9	VID_MODE_CFG_LP_VB-P_EN	When set to 1, this bit enables the return to low-power inside the VBP period when timing allows. Default Value: 0x0
8	VID_MODE_CF-G_LP_VSA_EN	When set to 1, this bit enables the return to low-power inside the VSA period when timing allows. Default Value: 0x0
7 : 2	VID_MODE_CFG_RE-SERVED_7_2	Reserved and read as zero. Default Value: 0x0
1 : 0	VID_MODE_CFG_VID_-MODE_TYPE	This field indicates the video mode transmission type as follows: Default Value: 0x0 **0x0: VIDMODE0 :** (none) **0x1: VIDMODE1 :** (none) **0x2: VIDMODE2 :** (none) **0x3: VIDMODE3 :** (none)

27.1.174 GFXSS_MIPIDSI_DWCMIPIDSI_VID_PKT_SIZE

Description: Configures the video packet size.

Address: 0x4480303C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VID_PKT_SIZE_VID_PKT_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R		RW					
HW Access	R		R					
Name	VID_PKT_SIZE_RESERVED_31_14 [15:14]		VID_PKT_SIZE_VID_PKT_SIZE [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_PKT_SIZE_RESERVED_31_14 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_PKT_SIZE_RESERVED_31_14 [31:24]							

Bits	Name	Description
31 : 14	VID_PKT_SIZE_RESERVED_31_14	Reserved and read as zero. Default Value: 0x0
13 : 0	VID_PKT_SIZE_VID_PKT_SIZE	This field configures the number of pixels in a single video packet. - For 18-bit not loosely packed data types, this number must be a multiple of 4. - For YCbCr data types, it must be a multiple of 2, as described in the DSI specification. - For DSC24, this field configures the number of Bytes. Note that when using slices (i.e chunks) the minimum size packet size must be 3. Default Value: 0x0

27.1.175 GFXSS_MIPIDSI_DWCMIPIDSI_VID_NUM_CHUNKS

Description: Configures the number of chunks to use. The data in each chunk has the size provided by VID_PKT_SIZE.

Address: 0x44803040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VID_NUM_CHUNKS_VID_NUM_CHUNKS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R			RW				
HW Access	R			R				
Name	VID_NUM_CHUNKS_RESERVED_31_13 [15:13]			VID_NUM_CHUNKS_VID_NUM_CHUNKS [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_NUM_CHUNKS_RESERVED_31_13 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_NUM_CHUNKS_RESERVED_31_13 [31:24]							

Bits	Name	Description
31 : 13	VID_NUM_CHUNKS_RESERVED_31_13	Reserved and read as zero. Default Value: 0x0
12 : 0	VID_NUM_CHUNKS_VID_NUM_CHUNKS	This register configures the number of chunks to be transmitted during a Line period (a chunk is pair made of a video packet and a null packet). If set to 0 or 1, video line is still transmitted in a single packet. If set to 1 that packet is part of a chunk, meaning that a null packet follows it (if vid_null_size>0). Otherwise, multiple chunks are used to transmit each video line. Default Value: 0x0

27.1.176 GFXSS_MIPIDSI_DWCMIPIDSI_VID_NULL_SIZE

Description: Configures the size of null packets.

Address: 0x44803044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VID_NULL_SIZE_VID_NULL_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R			RW				
HW Access	R			R				
Name	VID_NULL_SIZE_RESERVED_31_13 [15:13]			VID_NULL_SIZE_VID_NULL_SIZE [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_NULL_SIZE_RESERVED_31_13 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_NULL_SIZE_RESERVED_31_13 [31:24]							

Bits	Name	Description
31 : 13	VID_NULL_SIZE_RESERVED_31_13	Reserved and read as zero. Default Value: 0x0
12 : 0	VID_NULL_SIZE_VID_NULL_SIZE	This register configures the number of bytes inside a null packet. Setting to 0 disables null packets. Default Value: 0x0

27.1.177 GFXSS_MIPIDSI_DWCMIPIDSI_VID_HSA_TIME

Description: Configures the video HSA time.

Address: 0x44803048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VID_HSA_TIME_VID_HSA_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				RW			
HW Access	R				R			
Name	VID_HSA_TIME_RESERVED_31_12 [15:12]				VID_HSA_TIME_VID_HSA_TIME [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_HSA_TIME_RESERVED_31_12 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_HSA_TIME_RESERVED_31_12 [31:24]							

Bits	Name	Description
31 : 12	VID_HSA_TIME_RESERVED_31_12	Reserved and read as zero. Default Value: 0x0
11 : 0	VID_HSA_TIME_VID_HSA_TIME	This field configures the Horizontal Synchronism Active period in lane byte clock cycles. Default Value: 0x0

27.1.178 GFXSS_MIPIDSI_DWCMIPIDSI_VID_HBP_TIME

Description: Configures the video HBP time.

Address: 0x4480304C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VID_HBP_TIME_VID_HBP_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				RW			
HW Access	R				R			
Name	VID_HBP_TIME_RESERVED_31_12 [15:12]				VID_HBP_TIME_VID_HBP_TIME [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_HBP_TIME_RESERVED_31_12 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_HBP_TIME_RESERVED_31_12 [31:24]							

Bits	Name	Description
31 : 12	VID_HBP_TIME_RESERVED_31_12	Reserved and read as zero. Default Value: 0x0
11 : 0	VID_HBP_TIME_VID_HBP_TIME	This field configures the Horizontal Back Porch period in lane byte clock cycles. Default Value: 0x0

27.1.179 GFXSS_MIPIDSI_DWCMIPIDSI_VID_HLINE_TIME

Description: Configures the overall time for each video line.

Address: 0x44803050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VID_HLINE_TIME_VID_HLINE_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	RW						
HW Access	R	R						
Name	VID_H-LINE_-TIME_RESERVED_31_15	VID_HLINE_TIME_VID_HLINE_TIME [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_HLINE_TIME_RESERVED_31_15 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_HLINE_TIME_RESERVED_31_15 [31:24]							

Bits	Name	Description
31 : 15	VID_HLINE_TIME_RE-SERVED_31_15	Reserved and read as zero. Default Value: 0x0
14 : 0	VID_HLINE_-TIME_VID_HLINE_TIME	This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles. Default Value: 0x0

27.1.180 GFXSS_MIPIDSI_DWCMIPIDSI_VID_VSA_LINES

Description: Configures the VSA period.

Address: 0x44803054

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VID_VSA_LINES_VSA_LINES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R						RW	
HW Access	R						R	
Name	VID_VSA_LINES_RESERVED_31_10 [15:10]						VID_VSA_LINES_VSA_LINES [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_VSA_LINES_RESERVED_31_10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_VSA_LINES_RESERVED_31_10 [31:24]							

Bits	Name	Description
31 : 10	VID_VSA_LINES_RESERVED_31_10	Reserved and read as zero. Default Value: 0x0
9 : 0	VID_VSA_LINES_VSA_LINES	This field configures the Vertical Synchronism Active period measured in number of horizontal lines. Default Value: 0x0

27.1.181 GFXSS_MIPIDSI_DWCMIPIDSI_VID_VBP_LINES

Description: Configures the VBP period.

Address: 0x44803058

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VID_VBP_LINES_VBP_LINES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R						RW	
HW Access	R						R	
Name	VID_VBP_LINES_RESERVED_31_10 [15:10]						VID_VBP_LINES_VB-P_LINES [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_VBP_LINES_RESERVED_31_10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_VBP_LINES_RESERVED_31_10 [31:24]							

Bits	Name	Description
31 : 10	VID_VBP_LINES_RE-SERVED_31_10	Reserved and read as zero. Default Value: 0x0
9 : 0	VID_VBP_LINES_VB-P_LINES	This field configures the Vertical Back Porch period measured in number of horizontal lines. Default Value: 0x0

27.1.182 GFXSS_MIPIDSI_DWCMIPIDSI_VID_VFP_LINES

Description: Configures the VFP period.

Address: 0x4480305C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VID_VFP_LINES_VFP_LINES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R						RW	
HW Access	R						R	
Name	VID_VFP_LINES_RESERVED_31_10 [15:10]						VID_VFP_LINES_VF-P_LINES [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_VFP_LINES_RESERVED_31_10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_VFP_LINES_RESERVED_31_10 [31:24]							

Bits	Name	Description
31 : 10	VID_VFP_LINES_RE-SERVED_31_10	Reserved and read as zero. Default Value: 0x0
9 : 0	VID_VFP_LINES_VF-P_LINES	This field configures the Vertical Front Porch period measured in number of horizontal lines. Default Value: 0x0

27.1.183 GFXSS_MIPIDSI_DWCMIPIDSI_VID_VACTIVE_LINES

Description: Configures the vertical resolution of video.

Address: 0x44803060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VID_VACTIVE_LINES_V_ACTIVE_LINES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R		RW					
HW Access	R		R					
Name	VID_VACTIVE_LINES_RESERVED_31_14 [15:14]		VID_VACTIVE_LINES_V_ACTIVE_LINES [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_VACTIVE_LINES_RESERVED_31_14 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_VACTIVE_LINES_RESERVED_31_14 [31:24]							

Bits	Name	Description
31 : 14	VID_VACTIVE_LINES_RESERVED_31_14	Reserved and read as zero. Default Value: 0x0
13 : 0	VID_VACTIVE_LINES_V_ACTIVE_LINES	This field configures the Vertical Active period measured in number of horizontal lines. Default Value: 0x0

27.1.184 GFXSS_MIPIDSI_DWCMIPIDSI_CMD_MODE_CFG

Description: Configures several aspect of command mode operation, tearing effect, acknowledge for each packet and the speed mode to transmit each Data Type related to commands.

Address: 0x44803068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						RW	RW
HW Access	R						R	R
Name	CMD_MODE_CFG_RESERVED_7_2 [7:2]						CMD_MODE_CFG_ACK_RQST_EN	CMD_MODE_CFG_TEAR_FX_EN

Bits	15	14	13	12	11	10	9	8
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CMD_MODE_CFG_RESERVED_15	CMD_MODE_CFG_GEN_LW_TX	CMD_MODE_CFG_GEN_SR_2P_TX	CMD_MODE_CFG_GEN_SR_1P_TX	CMD_MODE_CFG_GEN_SR_0P_TX	CMD_MODE_CFG_GEN_SW_2P_TX	CMD_MODE_CFG_GEN_SW_1P_TX	CMD_MODE_CFG_GEN_SW_0P_TX

Bits	23	22	21	20	19	18	17	16
SW Access	R				RW	RW	RW	RW
HW Access	R				R	R	R	R
Name	CMD_MODE_CFG_RESERVED_23_20 [23:20]				CMD_MODE_CFG_DCS_LW_TX	CMD_MODE_CFG_DCS_SR_0P_TX	CMD_MODE_CFG_DCS_SW_1P_TX	CMD_MODE_CFG_DCS_SW_0P_TX

Bits	31	30	29	28	27	26	25	24
SW Access	R							RW
HW Access	R							R
Name	CMD_MODE_CFG_RESERVED_31_25 [31:25]							CMD_MODE_CFG_MAX_RD_PKT_SIZE

Bits	Name	Description
31 : 25	CMD_MODE_CFG_RESERVED_31_25	Reserved and read as zero. Default Value: 0x0
24	CMD_MODE_CFG_MAX_RD_PKT_SIZE	This bit configures the maximum read packet size command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)

27.1.184 GFXSS_MIPIDSI_DWCMIPIDSI_CMD_MODE_CFG (continued)

23 : 20	CMD_MODE_CFG_RESERVED_23_20	Reserved and read as zero. Default Value: 0x0
19	CMD_MODE_CFG_DCS_LW_TX	This bit configures the DCS long write packet command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)
18	CMD_MODE_CFG_DCS_SR_0P_TX	This bit configures the DCS short read packet with zero parameter command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)
17	CMD_MODE_CFG_DCS_SW_1P_TX	This bit configures the DCS short write packet with one parameter command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)
16	CMD_MODE_CFG_DCS_SW_0P_TX	This bit configures the DCS short write packet with zero parameter command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)
15	CMD_MODE_CFG_RESERVED_15	Reserved and read as zero. Default Value: 0x0
14	CMD_MODE_CFG_GEN_LW_TX	This bit configures the Generic long write packet command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)

27.1.184 GFXSS_MIPIDSI_DWCMIPIDSI_CMD_MODE_CFG (continued)

13	CMD_MODE_CFG_-GEN_SR_2P_TX	This bit configures the Generic short read packet with two parameters command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)
12	CMD_MODE_CFG_-GEN_SR_1P_TX	This bit configures the Generic short read packet with one parameter command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)
11	CMD_MODE_CFG_-GEN_SR_0P_TX	This bit configures the Generic short read packet with zero parameter command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)
10	CMD_MODE_CFG_-GEN_SW_2P_TX	This bit configures the Generic short write packet with two parameters command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)
9	CMD_MODE_CFG_-GEN_SW_1P_TX	This bit configures the Generic short write packet with one parameter command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)

27.1.184 GFXSS_MIPIDSI_DWCMIPIDSI_CMD_MODE_CFG (continued)

8	CMD_MODE_CFG_-GEN_SW_0P_TX	This bit configures the Generic short write packet with zero parameter command transmission type: Default Value: 0x0 **0x0: HIGHSPEED :** (none) **0x1: LOWPOWER :** (none)
7 : 2	CMD_MODE_CFG_RE-SERVED_7_2	Reserved and read as zero. Default Value: 0x0
1	CMD_MODE_CF-G_ACK_RQST_EN	When set to 1, this bit enables the acknowledge request after each packet transmission. Default Value: 0x0
0	CMD_MODE_CF-G_TEAR_FX_EN	When set to 1, this bit enables the tearing effect acknowledge request. Default Value: 0x0

27.1.185 GFXSS_MIPIDSI_DWCMIPIDSI_GEN_HDR

Description: Sets the header for new packets sent using the Generic interface.

Address: 0x4480306C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	GEN_HDR_GEN_VC [7:6]		GEN_HDR_GEN_DT [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GEN_HDR_GEN_WC_LSBYTE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GEN_HDR_GEN_WC_MSBYTE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	GEN_HDR_RESERVED_31_24 [31:24]							

Bits	Name	Description
31 : 24	GEN_HDR_RESERVED_31_24	Reserved and read as zero. Default Value: 0x0
23 : 16	GEN_HDR_GEN_WC_MSBYTE	This field configures the most significant byte of the header packet's word count for long packets or data 1 for short packets. Default Value: 0x0
15 : 8	GEN_HDR_GEN_WC_LSBYTE	This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets. Default Value: 0x0
7 : 6	GEN_HDR_GEN_VC	This field configures the Virtual Channel ID of the header packet. Default Value: 0x0
5 : 0	GEN_HDR_GEN_DT	This field configures the packet Data Type of the header packet. Default Value: 0x0

27.1.186 GFXSS_MIPIDSI_DWCMIPIDSI_GEN_PLD_DATA

Description: Sets the payload for packets sent using the Generic interface and, when read returns the contents of READ responses from the peripheral.

Address: 0x44803070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GEN_PLD_DATA_GEN_PLD_B1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GEN_PLD_DATA_GEN_PLD_B2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GEN_PLD_DATA_GEN_PLD_B3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GEN_PLD_DATA_GEN_PLD_B4 [31:24]							

Bits	Name	Description
31 : 24	GEN_PLD_DATA_- GEN_PLD_B4	This field indicates byte 4 of the packet payload. Default Value: 0x0
23 : 16	GEN_PLD_DATA_- GEN_PLD_B3	This field indicates byte 3 of the packet payload. Default Value: 0x0
15 : 8	GEN_PLD_DATA_- GEN_PLD_B2	This field indicates byte 2 of the packet payload. Default Value: 0x0
7 : 0	GEN_PLD_DATA_- GEN_PLD_B1	This field indicates byte 1 of the packet payload. Default Value: 0x0

27.1.187 GFXSS_MIPIDSI_DWCMIPIDSI_CMD_PKT_STATUS

Description: Contains information about the status of FIFOs related to DBI and Generic interface.

Address: 0x44803074

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	R	W	W	W	W	W	W	W
Name	CMD_PKT_STATUS_RESERVED_7	CMD_PKT_STATUS_GEN_RD_CMD_BUSY	CMD_PKT_STATUS_GEN_PLD_R_FULL	CMD_PKT_STATUS_GEN_PLD_R_EMPTY	CMD_PKT_STATUS_GEN_PLD_W_FULL	CMD_PKT_STATUS_GEN_PLD_W_EMPTY	CMD_PKT_STATUS_GEN_CMD_FULL	CMD_PKT_STATUS_GEN_CMD_EMPTY

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	R	W	W	W	W	W	W	W
Name	CMD_PKT_STATUS_RESERVED_15	CMD_PKT_STATUS_DBI_RD_CMD_BUSY	CMD_PKT_STATUS_DBI_PLD_R_FULL	CMD_PKT_STATUS_DBI_PLD_R_EMPTY	CMD_PKT_STATUS_DBI_PLD_W_FULL	CMD_PKT_STATUS_DBI_PLD_W_EMPTY	CMD_PKT_STATUS_DBI_CMD_FULL	CMD_PKT_STATUS_DBI_CMD_EMPY

Bits	23	22	21	20	19	18	17	16
SW Access	R				R	R	R	R
HW Access	R				W	W	W	W
Name	CMD_PKT_STATUS_RESERVED_23_20 [23:20]				CMD_PKT_STATUS_GEN_BUFF_PLD_FULL	CMD_PKT_STATUS_GEN_BUFF_PLD_EMPTY	CMD_PKT_STATUS_GEN_BUFF_CMD_FULL	CMD_PKT_STATUS_GEN_BUFF_CMD_EMPTY

Bits	31	30	29	28	27	26	25	24
SW Access	R				R	R	R	R
HW Access	R				W	W	W	W
Name	CMD_PKT_STATUS_RESERVED_31_28 [31:28]				CMD_PKT_STATUS_DBI_BUFF_PLD_FULL	CMD_PKT_STATUS_DBI_BUFF_PLD_EMPTY	CMD_PKT_STATUS_DBI_BUFF_CMD_FULL	CMD_PKT_STATUS_DBI_BUFF_CMD_EMPTY

Bits	Name	Description
31 : 28	CMD_PKT_STATUS_RESERVED_31_28	Reserved and read as zero. Default Value: 0x0
27	CMD_PKT_STATUS_DBI_BUFF_PLD_FULL	This bit indicates the full status of the DBI payload internal buffer. Default Value: 0x0
26	CMD_PKT_STATUS_DBI_BUFF_PLD_EMPTY	This bit indicates the empty status of the DBI payload internal buffer. Default Value: 0x1
25	CMD_PKT_STATUS_DBI_BUFF_CMD_FULL	This bit indicates the full status of the DBI command internal buffer. Default Value: 0x0
24	CMD_PKT_STATUS_DBI_BUFF_CMD_EMPTY	This bit indicates the empty status of the DBI command internal buffer. Default Value: 0x1

27.1.187 GFXSS_MIPIDSI_DWCMIPIDSI_CMD_PKT_STATUS (continued)

23 : 20	CMD_PKT_STATUS_RESERVED_23_20	Reserved and read as zero. Default Value: 0x0
19	CMD_PKT_STATUS_GEN_BUFF_PLD_FULL	This bit indicates the full status of the generic payload internal buffer. Default Value: 0x0
18	CMD_PKT_STATUS_GEN_BUFF_PLD_EMPTY	This bit indicates the empty status of the generic payload internal buffer. Default Value: 0x1
17	CMD_PKT_STATUS_GEN_BUFF_CMD_FULL	This bit indicates the full status of the generic command internal buffer. Default Value: 0x0
16	CMD_PKT_STATUS_GEN_BUFF_CMD_EMPTY	This bit indicates the empty status of the generic command internal buffer. Default Value: 0x1
15	CMD_PKT_STATUS_RESERVED_15	Reserved and read as zero. Default Value: 0x0
14	CMD_PKT_STATUS_DBI_RD_CMD_BUSY	This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO for DBI interface. Default Value: 0x0
13	CMD_PKT_STATUS_DBI_PLD_R_FULL	This bit indicates the full status of the DBI read payload FIFO. Default Value: 0x0
12	CMD_PKT_STATUS_DBI_PLD_R_EMPTY	This bit indicates the empty status of the DBI read payload Default Value: 0x1
11	CMD_PKT_STATUS_DBI_PLD_W_FULL	This bit indicates the full status of the DBI write payload FIFO. Default Value: 0x0
10	CMD_PKT_STATUS_DBI_PLD_W_EMPTY	This bit indicates the empty status of the DBI write payload FIFO. Default Value: 0x1
9	CMD_PKT_STATUS_DBI_CMD_FULL	This bit indicates the full status of the DBI command FIFO. Default Value: 0x0
8	CMD_PKT_STATUS_DBI_CMD_EMPY	This bit indicates the empty status of the DBI command FIFO. Default Value: 0x1
7	CMD_PKT_STATUS_RESERVED_7	Reserved and read as zero. Default Value: 0x0
6	CMD_PKT_STATUS_GEN_RD_CMD_BUSY	This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO for GENERIC interface. Default Value: 0x0
5	CMD_PKT_STATUS_GEN_PLD_R_FULL	This bit indicates the full status of the generic read payload FIFO. Default Value: 0x0
4	CMD_PKT_STATUS_GEN_PLD_R_EMPTY	This bit indicates the empty status of the generic read payload FIFO. Default Value: 0x1
3	CMD_PKT_STATUS_GEN_PLD_W_FULL	This bit indicates the full status of the generic write payload FIFO. Default Value: 0x0
2	CMD_PKT_STATUS_GEN_PLD_W_EMPTY	This bit indicates the empty status of the generic write payload FIFO. Default Value: 0x1
1	CMD_PKT_STATUS_GEN_CMD_FULL	This bit indicates the full status of the generic command FIFO. Default Value: 0x0
0	CMD_PKT_STATUS_GEN_CMD_EMPTY	This bit indicates the empty status of the generic command FIFO. Default Value: 0x1

27.1.188 GFXSS_MIPIDSI_DWCMIPIDSI_TO_CNT_CFG

Description: Configures counters that trigger timeout errors. These are used to warn the system of a failure, through an interrupt, and restart the controller in case of unexpected situations that cause deadlock conditions.

Address: 0x44803078

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TO_CNT_CFG_LPRX_TO_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TO_CNT_CFG_LPRX_TO_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TO_CNT_CFG_HSTX_TO_CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TO_CNT_CFG_HSTX_TO_CNT [31:24]							

Bits	Name	Description
31 : 16	TO_CNT_CFG_HSTX-_TO_CNT	This field configures the timeout counter that triggers a high-speed transmission timeout contention detection (measured in TO_CLK_DIVISION cycles). If using non-burst mode and there is not sufficient time to switch from high-speed to low-power and back in the period which is from one line data finishing to the next line sync start, the DSI link returns low-power state once per frame, then you should configure the TO_CLK_DIVISION and hstx_to_cnt to satisfy the following formula: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one FRAME data transmission * (1 + 10%) In burst mode, RGB pixel packets are time-compressed, leaving more time during a scan line. So if in burst mode and there is sufficient time to switch from high-speed to low-power and back in the period of time from one line data finishing to the next line sync start, the DSI link can return low-power mode and back in this time interval to save power. If you choose so, you should configure the TO_CLK_DIVISION and hstx_to_cnt to satisfy the following formula: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one LINE data transmission * (1 + 10%) Default Value: 0x0
15 : 0	TO_CNT_CFG_LPRX-_TO_CNT	This field configures the timeout counter that triggers a low-power reception timeout contention detection (measured in TO_CLK_DIVISION cycles). Default Value: 0x0

27.1.189 GFXSS_MIPIDSI_DWCMIPIDSI_HS_RD_TO_CNT

Description: Configures the Peripheral Response timeout after high-speed Read operations.

Address: 0x4480307C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_RD_TO_CNT_HS_RD_TO_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	HS_RD_TO_CNT_HS_RD_TO_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	HS_RD_TO_CNT_RESERVED_31_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	HS_RD_TO_CNT_RESERVED_31_16 [31:24]							

Bits	Name	Description
31 : 16	HS_RD_TO_CNT_RESERVED_31_16	Reserved and read as zero. Default Value: 0x0
15 : 0	HS_RD_TO_CNT_HS_RD_TO_CNT	This field sets a period for which DWC_mipi_dsi_host keeps the link still, after sending a high-speed Read operation. This period is measured in cycles of lanebyteclk, starts to count when the D-PHY enters stop state and causes no interrupts. Default Value: 0x0

27.1.190 GFXSS_MIPIDSI_DWCMIPIDSI_LP_RD_TO_CNT

Description: Configures the Peripheral Response timeout after low-power Read operations.

Address: 0x44803080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LP_RD_TO_CNT_LP_RD_TO_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LP_RD_TO_CNT_LP_RD_TO_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	LP_RD_TO_CNT_RESERVED_31_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	LP_RD_TO_CNT_RESERVED_31_16 [31:24]							

Bits	Name	Description
31 : 16	LP_RD_TO_CNT_RESERVED_31_16	Reserved and read as zero. Default Value: 0x0
15 : 0	LP_RD_TO_CNT_LP_RD_TO_CNT	This field sets a period for which DWC_mipi_dsi_host keeps the link still, after sending a low-power Read operation. This period is measured in cycles of lanebyteclk, starts to count when the D-PHY enters stop state and causes no interrupts. Default Value: 0x0

27.1.191 GFXSS_MIPIDSI_DWCMIPIDSI_HS_WR_TO_CNT

Description: Configures the Peripheral Response timeout after high-speed Write operations.

Address: 0x44803084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_WR_TO_CNT_HS_WR_TO_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	HS_WR_TO_CNT_HS_WR_TO_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	HS_WR_TO_CNT_RESERVED_23_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							R
HW Access	R							R
Name	HS_WR_TO_CNT_RESERVED_31_25 [31:25]							HS_WR_TO_CNT_RESERVED_24

Bits	Name	Description
31 : 25	HS_WR_TO_CNT_RESERVED_31_25	Reserved and read as zero. Default Value: 0x0
24	HS_WR_TO_CNT_RESERVED_24	Reserved and read as zero Default Value: 0x0
23 : 16	HS_WR_TO_CNT_RESERVED_23_16	Reserved and read as zero. Default Value: 0x0
15 : 0	HS_WR_TO_CNT_HS_WR_TO_CNT	This field sets a period for which DWC_mipi_dsi_host keeps the link still, after sending a high-speed Write operation. This period is measured in cycles of lanebyteclk, starts to count when the D-PHY enters stop state and causes no interrupts. Default Value: 0x0

27.1.192 GFXSS_MIPIDSI_DWCMIPIDSI_LP_WR_TO_CNT

Description: Configures the Peripheral Response timeout after low-power Write operations.

Address: 0x44803088

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LP_WR_TO_CNT_LP_WR_TO_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LP_WR_TO_CNT_LP_WR_TO_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	LP_WR_TO_CNT_RESERVED_31_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	LP_WR_TO_CNT_RESERVED_31_16 [31:24]							

Bits	Name	Description
31 : 16	LP_WR_TO_CNT_RESERVED_31_16	Reserved and read as zero. Default Value: 0x0
15 : 0	LP_WR_TO_CNT_LP_WR_TO_CNT	This field sets a period for which DWC_mipi_dsi_host keeps the link still, after sending a low-power Write operation. This period is measured in cycles of lanebyteclk, starts to count when the D-PHY enters stop state and causes no interrupts. Default Value: 0x0

27.1.193 GFXSS_MIPIDSI_DWCMIPIDSI_BTA_TO_CNT

Description: Configures the Peripheral Response timeout after Bus Turnaround completion.

Address: 0x4480308C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BTA_TO_CNT_BTA_TO_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	BTA_TO_CNT_BTA_TO_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	BTA_TO_CNT_RESERVED_31_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	BTA_TO_CNT_RESERVED_31_16 [31:24]							

Bits	Name	Description
31 : 16	BTA_TO_CNT_RESERVED_31_16	Reserved and read as zero. Default Value: 0x0
15 : 0	BTA_TO_CNT_BTA_TO_CNT	This field sets a period for which DWC_mipi_dsi_host keeps the link still, after completing a Bus Turnaround. This period is measured in cycles of lanebyteclk, starts to count when the D-PHY enters stop state and causes no interrupts. Default Value: 0x0

27.1.194 GFXSS_MIPIDSI_DWCMIPIDSI_SDF_3D

Description: Stores 3D control information for VSS packets in video mode.

Address: 0x44803090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	SDF_3D_RESERVED_15_6 [7:6]		SDF_3D_RIGHT_FIRST	SDF_3D_SECOND_VSYNC	SDF_3D_FORMAT_3D [3:2]		SDF_3D_MODE_3D [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	SDF_3D_RESERVED_15_6 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							RW
HW Access	R							R
Name	SDF_3D_RESERVED_31_17 [23:17]							SDF_3D_SEND_3D_CFG

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	SDF_3D_RESERVED_31_17 [31:24]							

Bits	Name	Description
31 : 17	SDF_3D_RESERVED_31_17	Reserved and read as zero. Default Value: 0x0
16	SDF_3D_SEND_3D_CFG	When set, causes the next VSS packet to include 3D control payload in every VSS packet. Default Value: 0x0
15 : 6	SDF_3D_RESERVED_15_6	Reserved and read as zero. Default Value: 0x0
5	SDF_3D_RIGHT_FIRST	This bit defines the left/right order: Default Value: 0x0 **0x0: LFIRST :** (none) **0x1: RFIRST :** (none)
4	SDF_3D_SECOND_VSYNC	This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: Default Value: 0x0

27.1.194 GFXSS_MIPIDSI_DWCMIPIDSI_SDF_3D (continued)

		0x0: NOSYNC : (none) **0x1: SYNC :** (none)
3 : 2	SDF_3D_FORMAT_3D	This field defines 3D Image Format: Default Value: 0x0 **0x1: FRAME :** (none) **0x0: LINE :** (none) **0x2: PIXEL :** (none) **0x3: RESERVED :** (none)
1 : 0	SDF_3D_MODE_3D	This field defines 3D Mode On/Off and Display Orientation: Default Value: 0x0 **0x0: MODE0 :** (none) **0x1: MODE1 :** (none) **0x2: MODE2 :** (none) **0x3: MODE3 :** (none)

27.1.195 GFXSS_MIPIDSI_DWCMIPIDSI_LPCLK_CTRL

Description: Configures the possibility for using non continuous clock in the clock lane.

Address: 0x44803094

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						RW	RW
HW Access	R						R	R
Name	LPCLK_CTRL_RESERVED_31_2 [7:2]						LPCLK_CTRL_AUTO_CLKLANE_CTRL	LPCLK_CTRL_PHY_TXREQUESTCLKHS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	LPCLK_CTRL_RESERVED_31_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	LPCLK_CTRL_RESERVED_31_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	LPCLK_CTRL_RESERVED_31_2 [31:24]							

Bits	Name	Description
31 : 2	LPCLK_CTRL_RESERVED_31_2	Reserved and read as zero. Default Value: 0x0
1	LPCLK_CTRL_AUTO_CLKLANE_CTRL	This bit enables the automatic mechanism to stop providing clock in the clock lane when time allows. Default Value: 0x0
0	LPCLK_CTRL_PHY_TXREQUESTCLKHS	This bit controls the D-PHY PPI txrequestclkhs signal. Default Value: 0x0

27.1.196 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TMR_LPCLK_CFG

Description: Sets the time that DWC_mipi_dsi_host assumes in calculations for the clock lane to switch between high-speed and low-power.

Address: 0x44803098

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PHY_TMR_LPCLK_CFG_PHY_CLKLP2HS_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R						RW	
HW Access	R						R	
Name	PHY_TMR_LPCLK_CFG_RESERVED_15_10 [15:10]						PHY_TMR_LPCLK_CFG_-PHY_CLKLP2HS_TIME [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PHY_TMR_LPCLK_CFG_PHY_CLKHS2LP_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R						RW	
HW Access	R						R	
Name	PHY_TMR_LPCLK_CFG_RESERVED_31_26 [31:26]						PHY_TMR_LPCLK_CFG_-PHY_CLKHS2LP_TIME [25:24]	

Bits	Name	Description
31 : 26	PHY_TMR_LPCLK_CF-G_RESERVED_31_26	Reserved and read as zero. Default Value: 0x0
25 : 16	PHY_TMR_LPCLK_CF-G_PHY_CLKHS2LP_-TIME	This field configures the maximum time that the D-PHY clock lane takes to go from high-speed to low-power transmission measured in lane byte clock cycles. Default Value: 0x0
15 : 10	PHY_TMR_LPCLK_CF-G_RESERVED_15_10	Reserved and read as zero. Default Value: 0x0
9 : 0	PHY_TMR_LPCLK_CF-G_PHY_CLKLP2HS_-TIME	This field configures the maximum time that the D-PHY clock lane takes to go from low-power to high-speed transmission measured in lane byte clock cycles. Default Value: 0x0

27.1.197 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TMR_CFG

Description: Sets the time that DWC_mipi_dsi_host assumes in calculations for the data lanes to switch between high-speed and low-power.

Address: 0x4480309C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PHY_TMR_CFG_PHY_LP2HS_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R						RW	
HW Access	R						R	
Name	PHY_TMR_CFG_RESERVED_15_10 [15:10]						PHY_TMR_CFG_- PHY_LP2HS_TIME [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PHY_TMR_CFG_PHY_HS2LP_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R						RW	
HW Access	R						R	
Name	PHY_TMR_CFG_RESERVED_31_26 [31:26]						PHY_TMR_CFG_- PHY_HS2LP_TIME [25:24]	

Bits	Name	Description
31 : 26	PHY_TMR_CFG_RE-SERVED_31_26	Reserved and read as zero. Default Value: 0x0
25 : 16	PHY_TMR_CFG_-PHY_HS2LP_TIME	This field configures the maximum time that the D-PHY data lanes take to go from high-speed to low-power transmission measured in lane byte clock cycles. Default Value: 0x0
15 : 10	PHY_TMR_CFG_RE-SERVED_15_10	Reserved and read as zero. Default Value: 0x0
9 : 0	PHY_TMR_CFG_-PHY_LP2HS_TIME	This field configures the maximum time that the D-PHY data lanes take to go from low-power to high-speed transmission measured in lane byte clock cycles. Default Value: 0x0

27.1.198 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_RSTZ

Description: Controls resets and the PLL of the D-PHY.

Address: 0x448030A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				RW	RW	RW	RW
HW Access	R				R	R	R	R
Name	PHY_RSTZ_RESERVED_31_4 [7:4]				PHY_RSTZ_PHY_FORCEPLL	PHY_RSTZ_PHY_ENABLECLK	PHY_RSTZ_PHY_RSTZ	PHY_RSTZ_PHY_SHUTDOWNZ

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PHY_RSTZ_RESERVED_31_4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PHY_RSTZ_RESERVED_31_4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PHY_RSTZ_RESERVED_31_4 [31:24]							

Bits	Name	Description
31 : 4	PHY_RSTZ_RESERVED_31_4	Reserved and read as zero. Default Value: 0x0
3	PHY_RSTZ_PHY_FORCEPLL	When the D-PHY is in ULPS, this bit enables the D-PHY PLL. Default Value: 0x0
2	PHY_RSTZ_PHY_ENABLECLK	When set to 1, this bit enables the D-PHY Clock Lane Module. Default Value: 0x0
1	PHY_RSTZ_PHY_RSTZ	When set to 0, this bit places the digital section of the D-PHY in the reset state. Default Value: 0x0
0	PHY_RSTZ_PHY_SHUTDOWNZ	When set to 0, this bit places the complete D-PHY macro in power-down state. Default Value: 0x0

27.1.199 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_IF_CFG

Description: Configures the number of active lanes and the minimum time to remain in stop state.

Address: 0x448030A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						RW	
HW Access	R						R	
Name	PHY_IF_CFG_RESERVED_7_2 [7:2]						PHY_IF_CFG_N_LANES [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PHY_IF_CFG_PHY_STOP_WAIT_TIME [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PHY_IF_CFG_RESERVED_31_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PHY_IF_CFG_RESERVED_31_16 [31:24]							

Bits	Name	Description
31 : 16	PHY_IF_CFG_RE-SERVED_31_16	Reserved and read as zero. Default Value: 0x0
15 : 8	PHY_IF_CFG_-PHY_STOP_WAIT_TIME	This field configures the minimum time PHY needs to stay in StopState before requesting an high-speed transmission Default Value: 0x0
7 : 2	PHY_IF_CFG_RE-SERVED_7_2	Reserved and read as zero. Default Value: 0x0
1 : 0	PHY_IF_CFG_N_LANES	This field configures the number of active data lanes: Default Value: 0x1 **0x3: FOURLANES :** (none) **0x0: ONELANES :** (none) **0x2: THREELANES :** (none)

27.1.199 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_IF_CFG (continued)

0x1: TWOLANES :

(none)

27.1.200 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_ULPS_CTRL

Description: Configures entering and leaving ULPS in the D-PHY.

Address: 0x448030A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				RW	RW	RW	RW
HW Access	R				R	R	R	R
Name	PHY_ULPS_CTRL_RESERVED_31_4 [7:4]				PHY_ULPS_CTRL_-PHY_TX-EXITULPSLAN	PHY_ULPS_CTRL_-PHY_TX-REQULPSLAN	PHY_ULPS_CTRL_-PHY_TX-EXITULPSCLK	PHY_ULPS_CTRL_-PHY_TX-REQULPSCLK

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PHY_ULPS_CTRL_RESERVED_31_4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PHY_ULPS_CTRL_RESERVED_31_4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PHY_ULPS_CTRL_RESERVED_31_4 [31:24]							

Bits	Name	Description
31 : 4	PHY_ULPS_CTRL_RE-SERVED_31_4	Reserved and read as zero. Default Value: 0x0
3	PHY_ULPS_CTRL_-PHY_TXEXITULPSLAN	ULPS mode Exit on all active data lanes. Default Value: 0x0
2	PHY_ULPS_CTRL_-PHY_TXREQULPSLAN	ULPS mode Request on all active data lanes. Default Value: 0x0
1	PHY_ULPS_CTRL_-PHY_TXEXITULPSCLK	ULPS mode Exit on clock lane. Default Value: 0x0
0	PHY_ULPS_CTRL_-PHY_TXREQULPSCLK	ULPS mode Request on clock lane. Default Value: 0x0

27.1.201 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TX_TRIGGERS

Description: Configures the pins that activate triggers in the D-PHY.

Address: 0x448030AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				RW			
HW Access	R				R			
Name	PHY_TX_TRIGGERS_RESERVED_31_4 [7:4]				PHY_TX_TRIGGERS_PHY_TX_TRIGGERS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PHY_TX_TRIGGERS_RESERVED_31_4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PHY_TX_TRIGGERS_RESERVED_31_4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PHY_TX_TRIGGERS_RESERVED_31_4 [31:24]							

Bits	Name	Description
31 : 4	PHY_TX_TRIG-GERS_RESERVED_31_4	Reserved and read as zero. Default Value: 0x0
3 : 0	PHY_TX_TRIGGERS_-PHY_TX_TRIGGERS	This field controls the trigger transmissions. Default Value: 0x0

27.1.202 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_STATUS

Description: Contains information about the status of the D-PHY.

Address: 0x448030B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PHY_STATUS_-PHY_STOPSTATE1LANE	PHY_STATUS_-PHY_RXULPSESC0LANE	PHY_STATUS_-PHY_ULPSACTIVENOT0LANE	PHY_STATUS_-PHY_STOPSTATE0LANE	PHY_STATUS_-PHY_ULPSACTIVENOT-CLK	PHY_STATUS_-PHY_STOPSTATECLK-LANE	PHY_STATUS_PHY_-DIRECTION	PHY_STATUS_-PHY_LOCK

Bits	15	14	13	12	11	10	9	8
SW Access	R			R	R	R	R	R
HW Access	R			R	R	R	R	W
Name	PHY_STATUS_RESERVED_31_13 [15:13]			PHY_STATUS_RESERVED_12	PHY_STATUS_RESERVED_11	PHY_STATUS_RESERVED_10	PHY_STATUS_RESERVED_9	PHY_STATUS_-PHY_ULPSACTIVENOT1LANE

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PHY_STATUS_RESERVED_31_13 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PHY_STATUS_RESERVED_31_13 [31:24]							

Bits	Name	Description
31 : 13	PHY_STATUS_RESERVED_31_13	Reserved and read as zero. Default Value: 0x0
12	PHY_STATUS_RESERVED_12	Reserved and read as one. Default Value: Undefined
11	PHY_STATUS_RESERVED_11	Reserved and read as zero. Default Value: Undefined
10	PHY_STATUS_RESERVED_10	Reserved and read as one. Default Value: Undefined
9	PHY_STATUS_RESERVED_9	Reserved and read as zero. Default Value: Undefined
8	PHY_STATUS_-PHY_ULPSACTIVENOT1LANE	This bit indicates the status of ulpsactivenot1lane D-PHY signal. Default Value: Undefined
7	PHY_STATUS_-PHY_STOPSTATE1LANE	This bit indicates the status of phystopstate1lane D-PHY signal. Default Value: Undefined

27.1.202 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_STATUS (continued)

6	PHY_STATUS_PHY_RX-ULPSESC0LANE	This bit indicates the status of rxulpsesc0lane D-PHY signal. Default Value: Undefined
5	PHY_STATUS_-PHY_ULPSAC-TIVENOT0LANE	This bit indicates the status of ulpsactivenot0lane D-PHY signal. Default Value: Undefined
4	PHY_STATUS_-PHY_STOPSTATE0LANE	This bit indicates the status of phystopstate0lane D-PHY signal. Default Value: Undefined
3	PHY_STATUS_-PHY_ULPSACTIVENOT-CLK	This bit indicates the status of phyulpsactivenotclk D-PHY signal. Default Value: Undefined
2	PHY_STATUS_-PHY_STOPSTATECLK-LANE	This bit indicates the status of phystopstateclklane D-PHY signal. Default Value: Undefined
1	PHY_STATUS_PHY_DI-RECTION	This bit indicates the status of phydirection D-PHY signal. Default Value: Undefined
0	PHY_STATUS_-PHY_LOCK	This bit indicates the status of phylock D-PHY signal. Default Value: Undefined

27.1.203 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TST_CTRL0

Description: Controls clock and clear pins of the D-PHY vendor specific interface.

Address: 0x448030B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						RW	RW
HW Access	R						R	R
Name	PHY_TST_CTRL0_RESERVED_31_2 [7:2]						PHY_TST_CTRL0_PHY_TESTCLK	PHY_TST_CTRL0_PHY_TESTCLR

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PHY_TST_CTRL0_RESERVED_31_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PHY_TST_CTRL0_RESERVED_31_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PHY_TST_CTRL0_RESERVED_31_2 [31:24]							

Bits	Name	Description
31 : 2	PHY_TST_CTRL0_RESERVED_31_2	Reserved and read as zero. Default Value: 0x0
1	PHY_TST_CTRL0_PHY_TESTCLK	This bit is used to clock the TESTDIN bus into the D-PHY. Default Value: 0x0
0	PHY_TST_CTRL0_PHY_TESTCLR	PHY test interface clear (active high). Default Value: 0x1

27.1.204 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TST_CTRL1

Description: Controls data and enable pins of the D-PHY vendor specific interface.

Address: 0x448030B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PHY_TST_CTRL1_PHY_TESTDIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	PHY_TST_CTRL1_PHT_TESTDOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R						RW	RW
HW Access	R						R	R
Name	PHY_TST_CTRL1_RESERVED_31_18 [23:18]						PHY_TST_CTRL1_PHY_TESTSEL	PHY_TST_CTRL1_PHY_TESTEN

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PHY_TST_CTRL1_RESERVED_31_18 [31:24]							

Bits	Name	Description
31 : 18	PHY_TST_CTRL1_RESERVED_31_18	Reserved and read as zero. Default Value: 0x0
17	PHY_TST_CTRL1_PHY_TESTSEL	PHY BiDIR MUX selector Default Value: 0x0
16	PHY_TST_CTRL1_PHY_TESTEN	PHY test interface operation selector: Default Value: 0x0 **0x1: WRITEADDR :** (none) **0x0: WRITEDATA :** (none)
15 : 8	PHY_TST_CTRL1_PHT_TESTDOUT	PHY output 8-bit data bus for read-back and internal probing functionalities. Default Value: 0x0
7 : 0	PHY_TST_CTRL1_PHY_TESTDIN	PHY test interface input 8-bit data bus for internal register programming and test functionalities access. Default Value: 0x0

27.1.205 GFXSS_MIPIDSI_DWCMIPIDSI_INT_ST0

Description: Contains the status of interrupt sources from acknowledge reports and the D-PHY.

Address: 0x448030BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INT_ST0_ACK_WITH_ERR_7	INT_ST0_ACK_WITH_ERR_6	INT_ST0_ACK_WITH_ERR_5	INT_ST0_ACK_WITH_ERR_4	INT_ST0_ACK_WITH_ERR_3	INT_ST0_ACK_WITH_ERR_2	INT_ST0_ACK_WITH_ERR_1	INT_ST0_ACK_WITH_ERR_0

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INT_ST0_ACK_WITH_ERR_15	INT_ST0_ACK_WITH_ERR_14	INT_ST0_ACK_WITH_ERR_13	INT_ST0_ACK_WITH_ERR_12	INT_ST0_ACK_WITH_ERR_11	INT_ST0_ACK_WITH_ERR_10	INT_ST0_ACK_WITH_ERR_9	INT_ST0_ACK_WITH_ERR_8

Bits	23	22	21	20	19	18	17	16
SW Access	R			R	R	R	R	R
HW Access	R			W	W	W	W	W
Name	INT_ST0_RESERVED_31_21 [23:21]			INT_ST0_DPHY_ERRORS_4	INT_ST0_DPHY_ERRORS_3	INT_ST0_DPHY_ERRORS_2	INT_ST0_DPHY_ERRORS_1	INT_ST0_DPHY_ERRORS_0

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	INT_ST0_RESERVED_31_21 [31:24]							

Bits	Name	Description
31 : 21	INT_ST0_RESERVED_31_21	Reserved and read as zero. Default Value: 0x0
20	INT_ST0_DPHY_ERRORS_4	This bit indicates LP1 contention error ErrContentionLP1 from Lane 0. Default Value: 0x0
19	INT_ST0_DPHY_ERRORS_3	This bit indicates LP0 contention error ErrContentionLP0 from Lane 0. Default Value: 0x0
18	INT_ST0_DPHY_ERRORS_2	This bit indicates control error ErrControl from Lane 0. Default Value: 0x0
17	INT_ST0_DPHY_ERRORS_1	This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0. Default Value: 0x0
16	INT_ST0_DPHY_ERRORS_0	This bit indicates ErrEsc escape entry error from Lane 0. Default Value: 0x0
15	INT_ST0_ACK_WITH_ERR_15	This bit retrieves the DSI protocol violation from the Acknowledge error report. Default Value: 0x0

27.1.205 GFXSS_MIPIDSI_DWCMIPIDSI_INT_ST0 (continued)

14	INT_ST0_ACK_WITH_ERR_14	This bit retrieves the reserved (specific to device) from the Acknowledge error report. Default Value: 0x0
13	INT_ST0_ACK_WITH_ERR_13	This bit retrieves the invalid transmission length from the Acknowledge error report. Default Value: 0x0
12	INT_ST0_ACK_WITH_ERR_12	This bit retrieves the DSI VC ID Invalid from the Acknowledge error report. Default Value: 0x0
11	INT_ST0_ACK_WITH_ERR_11	This bit retrieves the not recognized DSI data type from the Acknowledge error report. Default Value: 0x0
10	INT_ST0_ACK_WITH_ERR_10	This bit retrieves the checksum error (long packet only) from the Acknowledge error report. Default Value: 0x0
9	INT_ST0_ACK_WITH_ERR_9	This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report. Default Value: 0x0
8	INT_ST0_ACK_WITH_ERR_8	This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report. Default Value: 0x0
7	INT_ST0_ACK_WITH_ERR_7	This bit retrieves the Contention Detected error from the Acknownledge error report. Default Value: 0x0
6	INT_ST0_ACK_WITH_ERR_6	This bit retrieves the False Control error from the Acknowledge error report. Default Value: 0x0
5	INT_ST0_ACK_WITH_ERR_5	This bit retrieves the Peripheral Timeout error from the Acknowledge error report. Default Value: 0x0
4	INT_ST0_ACK_WITH_ERR_4	This bit retrieves the low-power Transmit Sync error from the Acknowledge error report. Default Value: 0x0
3	INT_ST0_ACK_WITH_ERR_3	This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report. Default Value: 0x0
2	INT_ST0_ACK_WITH_ERR_2	This bit retrieves the EoT Sync error from the Acknowledge error report. Default Value: 0x0
1	INT_ST0_ACK_WITH_ERR_1	This bit retrieves the SoT Sync error from the Acknowledge error report. Default Value: 0x0
0	INT_ST0_ACK_WITH_ERR_0	This bit retrieves the SoT error from the Acknowledge error report. Default Value: 0x0

27.1.206 GFXSS_MIPIDSI_DWCMIPIDSI_INT_ST1

Description: Contains the status of interrupt sources related to timeouts, ECC, CRC, packet size, EoTp, Generic and DBI interfaces.

Address: 0x448030C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INT_ST1_DPI_PLD_WR_ERR	INT_ST1_EOPT_ERR	INT_ST1_PKT_SIZE_ERR	INT_ST1_CRC_ERR	INT_ST1_ECC_MULTPL_ERR	INT_ST1_ECC_SINGLE_ERR	INT_ST1_TO_LP_RX	INT_ST1_TO_HS_TX

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INT_ST1_DBI_PLD_RD_ERR	INT_ST1_DBI_PLD_WR_ERR	INT_ST1_DBI_CMD_WR_ERR	INT_ST1_GEN_PLD_RECEV_ERR	INT_ST1_GEN_PLD_RD_ERR	INT_ST1_GEN_PLD_SEND_ERR	INT_ST1_GEN_PLD_WR_ERR	INT_ST1_GEN_CMD_WR_ERR

Bits	23	22	21	20	19	18	17	16
SW Access	R			R	R	R	R	R
HW Access	R			R	W	R	W	W
Name	INT_ST1_RESERVED_31_21 [23:21]			INT_ST1_RESERVED_20	INT_ST1_DPI_BUFF_PLD_UNDER	INT_ST1_RESERVED_18	INT_ST1_DBI_ILEGAL_COMM_ERR	INT_ST1_DBI_PLD_RECV_ERR

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	INT_ST1_RESERVED_31_21 [31:24]							

Bits	Name	Description
31 : 21	INT_ST1_RESERVED_31_21	Reserved and read as zero. Default Value: 0x0
20	INT_ST1_RESERVED_20	Reserved and read as zero Default Value: 0x0
19	INT_ST1_DPI_BUFF_PLD_UNDER	This bit indicates that an underflow has occurred when reading payload to build DSI packet for video mode Default Value: 0x0
18	INT_ST1_RESERVED_18	Reserved and read as zero Default Value: 0x0
17	INT_ST1_DBI_ILEGAL_COMM_ERR	This bit indicates that an attempt to write an illegal command on the DBI interface is made and the controller is blocked by transmission. Default Value: 0x0
16	INT_ST1_DBI_PLD_RECV_ERR	This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted. Default Value: 0x0

27.1.206 GFXSS_MIPIDSI_DWCMIPIDSI_INT_ST1 (continued)

15	INT_ST1_DBI_PLD_RD_ERR	This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted. Default Value: 0x0
14	INT_ST1_DBI_PLD_WR_ERR	This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written. Default Value: 0x0
13	INT_ST1_DBI_CMD_WR_ERR	This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written. Default Value: 0x0
12	INT_ST1_GEN_PLD_RECEV_ERR	This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted. Default Value: 0x0
11	INT_ST1_GEN_PLD_RD_ERR	This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted. Default Value: 0x0
10	INT_ST1_GEN_PLD_SEND_ERR	This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent. Default Value: 0x0
9	INT_ST1_GEN_PLD_WR_ERR	This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written. Default Value: 0x0
8	INT_ST1_GEN_CMD_WR_ERR	This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written. Default Value: 0x0
7	INT_ST1_DPI_PLD_WR_ERR	This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted. Default Value: 0x0
6	INT_ST1_EOPT_ERR	This bit indicates that the EoTp packet has not been received at the end of the incoming peripheral transmission. Default Value: 0x0
5	INT_ST1_PKT_SIZE_ERR	This bit indicates that the packet size error has been detected during the packet reception. Default Value: 0x0
4	INT_ST1_CRC_ERR	This bit indicates that the CRC error has been detected in the received packet payload. Default Value: 0x0
3	INT_ST1_ECC_MULTPL_ERR	This bit indicates that the ECC multiple error has been detected in a received packet. Default Value: 0x0
2	INT_ST1_ECC_SINGLE_ERR	This bit indicates that the ECC single error has been detected and corrected in a received packet. Default Value: 0x0
1	INT_ST1_TO_LP_RX	This bit indicates that the low-power reception timeout counter reached the end and contention has been detected. Default Value: 0x0
0	INT_ST1_TO_HS_TX	This bit indicates that the high-speed transmission timeout counter reached the end and contention has been detected. Default Value: 0x0

27.1.207 GFXSS_MIPIDSI_DWCMIPIDSI_INT_MSK0

Description: Configures masks for the sources of interrupts that affect the INT_ST0 register. Write 1 to un-mask each error report.

Address: 0x448030C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INT_MSK0_MASK_ACK_WITH_ERR_7	INT_MSK0_MASK_ACK_WITH_ERR_6	INT_MSK0_MASK_ACK_WITH_ERR_5	INT_MSK0_MASK_ACK_WITH_ERR_4	INT_MSK0_MASK_ACK_WITH_ERR_3	INT_MSK0_MASK_ACK_WITH_ERR_2	INT_MSK0_MASK_ACK_WITH_ERR_1	INT_MSK0_MASK_ACK_WITH_ERR_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INT_MSK0_MASK_ACK_WITH_ERR_15	INT_MSK0_MASK_ACK_WITH_ERR_14	INT_MSK0_MASK_ACK_WITH_ERR_13	INT_MSK0_MASK_ACK_WITH_ERR_12	INT_MSK0_MASK_ACK_WITH_ERR_11	INT_MSK0_MASK_ACK_WITH_ERR_10	INT_MSK0_MASK_ACK_WITH_ERR_9	INT_MSK0_MASK_ACK_WITH_ERR_8

Bits	23	22	21	20	19	18	17	16
SW Access	R			RW	RW	RW	RW	RW
HW Access	R			R	R	R	R	R
Name	INT_MSK0_RESERVED_31_21 [23:21]			INT_MSK0_MASK_D-PHY_ERRORS_4	INT_MSK0_MASK_D-PHY_ERRORS_3	INT_MSK0_MASK_D-PHY_ERRORS_2	INT_MSK0_MASK_D-PHY_ERRORS_1	INT_MSK0_MASK_D-PHY_ERRORS_0

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	INT_MSK0_RESERVED_31_21 [31:24]							

Bits	Name	Description
31 : 21	INT_MSK0_RESERVED_31_21	Reserved and read as zero. Default Value: 0x0
20	INT_MSK0_MASK_D-PHY_ERRORS_4	Mask for dphy_errors_4 Default Value: 0x0
19	INT_MSK0_MASK_D-PHY_ERRORS_3	Mask for dphy_errors_3 Default Value: 0x0
18	INT_MSK0_MASK_D-PHY_ERRORS_2	Mask for dphy_errors_2 Default Value: 0x0
17	INT_MSK0_MASK_D-PHY_ERRORS_1	Mask for dphy_errors_1 Default Value: 0x0
16	INT_MSK0_MASK_D-PHY_ERRORS_0	Mask for dphy_errors_0 Default Value: 0x0

27.1.207 GFXSS_MIPIDSI_DWCMIPIDSI_INT_MSK0 (continued)

15	INT_MSK0_MASK_ACK_WITH_ERR_15	Mask for ack_with_err_15 Default Value: 0x0
14	INT_MSK0_MASK_ACK_WITH_ERR_14	Mask for ack_with_err_14 Default Value: 0x0
13	INT_MSK0_MASK_ACK_WITH_ERR_13	Mask for ack_with_err_13 Default Value: 0x0
12	INT_MSK0_MASK_ACK_WITH_ERR_12	Mask for ack_with_err_12 Default Value: 0x0
11	INT_MSK0_MASK_ACK_WITH_ERR_11	Mask for ack_with_err_11 Default Value: 0x0
10	INT_MSK0_MASK_ACK_WITH_ERR_10	Mask for ack_with_err_10 Default Value: 0x0
9	INT_MSK0_MASK_ACK_WITH_ERR_9	Mask for ack_with_err_9 Default Value: 0x0
8	INT_MSK0_MASK_ACK_WITH_ERR_8	Mask for ack_with_err_8 Default Value: 0x0
7	INT_MSK0_MASK_ACK_WITH_ERR_7	Mask for ack_with_err_7 Default Value: 0x0
6	INT_MSK0_MASK_ACK_WITH_ERR_6	Mask for ack_with_err_6 Default Value: 0x0
5	INT_MSK0_MASK_ACK_WITH_ERR_5	Mask for ack_with_err_5 Default Value: 0x0
4	INT_MSK0_MASK_ACK_WITH_ERR_4	Mask for ack_with_err_4 Default Value: 0x0
3	INT_MSK0_MASK_ACK_WITH_ERR_3	Mask for ack_with_err_3 Default Value: 0x0
2	INT_MSK0_MASK_ACK_WITH_ERR_2	Mask for ack_with_err_2 Default Value: 0x0
1	INT_MSK0_MASK_ACK_WITH_ERR_1	Mask for ack_with_err_1 Default Value: 0x0
0	INT_MSK0_MASK_ACK_WITH_ERR_0	Mask for ack_with_err_0 Default Value: 0x0

27.1.208 GFXSS_MIPIDSI_DWCMIPIDSI_INT_MSK1

Description: Configures masks for the sources of interrupts that affect the INT_ST1 register.

Address: 0x448030C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INT_MSK1_MASK_DPI_PLD_WR_ERR	INT_MSK1_MASK_EOPT_ERR	INT_MSK1_MASK_PKT_SIZE_ERR	INT_MSK1_MASK_CRC_ERR	INT_MSK1_MASK_ECC_MULTPL_ERR	INT_MSK1_MASK_ECC_SINGLE_ERR	INT_MSK1_MASK_TO_LP_RX	INT_MSK1_MASK_TO_HS_TX

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INT_MSK1_MASK_DBI_PLD_RD_ERR	INT_MSK1_MASK_DBI_PLD_WR_ERR	INT_MSK1_MASK_DBI_CMD_WR_ERR	INT_MSK1_MASK_GEN_PLD_RECEV_ERR	INT_MSK1_MASK_GEN_PLD_RD_ERR	INT_MSK1_MASK_GEN_PLD_SEND_ERR	INT_MSK1_MASK_GEN_PLD_WR_ERR	INT_MSK1_MASK_GEN_CMD_WR_ERR

Bits	23	22	21	20	19	18	17	16
SW Access	R			R	RW	R	RW	RW
HW Access	R			R	R	R	R	R
Name	INT_MSK1_RESERVED_31_21 [23:21]			INT_MSK1_RESERVED_20	INT_MSK1_MASK_DPI_BUFF_PLD_UNDER	INT_MSK1_RESERVED_18	INT_MSK1_MASK_DBI_ILEGAL_COMM_ERR	INT_MSK1_MASK_DBI_PLD_RECV_ERR

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	INT_MSK1_RESERVED_31_21 [31:24]							

Bits	Name	Description
31 : 21	INT_MSK1_RESERVED_31_21	Reserved and read as zero. Default Value: 0x0
20	INT_MSK1_RESERVED_20	Reserved and read as zero Default Value: 0x0
19	INT_MSK1_MASK_DPI_BUFF_PLD_UNDER	Mask for dpi_buff_pld_under Default Value: 0x0
18	INT_MSK1_RESERVED_18	Reserved and read as zero Default Value: 0x0
17	INT_MSK1_MASK_DBI_ILEGAL_COMM_ERR	Mask for dbi_ilegal_comm_err Default Value: 0x0

27.1.208 GFXSS_MIPIDSI_DWCMIPIDSI_INT_MSK1 (continued)

16	INT_MSK1_MASK_DBI_PLD_RECV_ERR	Mask for dbi_pld_recv_err Default Value: 0x0
15	INT_MSK1_MASK_DBI_PLD_RD_ERR	Mask for dbi_pld_rd_err Default Value: 0x0
14	INT_MSK1_MASK_DBI_PLD_WR_ERR	Mask for dbi_pld_wr_err Default Value: 0x0
13	INT_MSK1_MASK_DBI_CMD_WR_ERR	Mask for dbi_cmd_wr_err Default Value: 0x0
12	INT_MSK1_MASK_GEN_PLD_RECEV_ERR	Mask for gen_pld_recev_err Default Value: 0x0
11	INT_MSK1_MASK_GEN_PLD_RD_ERR	Mask for gen_pld_rd_err Default Value: 0x0
10	INT_MSK1_MASK_GEN_PLD_SEND_ERR	Mask for gen_pld_send_err Default Value: 0x0
9	INT_MSK1_MASK_GEN_PLD_WR_ERR	Mask for gen_pld_wr_err Default Value: 0x0
8	INT_MSK1_MASK_GEN_CMD_WR_ERR	Mask for gen_cmd_wr_err Default Value: 0x0
7	INT_MSK1_MASK_DPI_PLD_WR_ERR	Mask for dpi_pld_wr_err Default Value: 0x0
6	INT_MSK1_MASK_EOPT_ERR	Mask for eopt_err Default Value: 0x0
5	INT_MSK1_MASK_PKT_SIZE_ERR	Mask for pkt_size_err Default Value: 0x0
4	INT_MSK1_MASK_CRC_ERR	Mask for crc_err Default Value: 0x0
3	INT_MSK1_MASK_ECC_MULTPL_ERR	Mask for ecc_multpl_err Default Value: 0x0
2	INT_MSK1_MASK_ECC_SINGLE_ERR	Mask for ecc_single_err Default Value: 0x0
1	INT_MSK1_MASK_TO_LP_RX	Mask for to_lp_rx Default Value: 0x0
0	INT_MSK1_MASK_TO_HS_TX	Mask for to_hs_tx Default Value: 0x0

27.1.209 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_CAL

Description: Controls the skew calibration of D-PHY.

Address: 0x448030CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							RW
HW Access	R							R
Name	PHY_CAL_RESERVED_31_1 [7:1]							PHY_-CAL_TX-SKEWCALHS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	PHY_CAL_RESERVED_31_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PHY_CAL_RESERVED_31_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PHY_CAL_RESERVED_31_1 [31:24]							

Bits	Name	Description
31 : 1	PHY_CAL_RE-SERVED_31_1	Reserved and read as zero. Default Value: 0x0
0	PHY_CAL_TXSKEWCAL-HS	High-speed skew calibration is started when txskewcalhs is set high (assuming that PHY is in Stop state). Default Value: 0x0

27.1.210 GFXSS_MIPIDSI_DWCMIPIDSI_INT_FORCE0

Description: Forces interrupt that affect the INT_ST0 register.

Address: 0x448030D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INT_-FORCE0_-FORCE_ACK_WITH_ERR_7	INT_-FORCE0_-FORCE_ACK_WITH_ERR_6	INT_-FORCE0_-FORCE_ACK_WITH_ERR_5	INT_-FORCE0_-FORCE_ACK_WITH_ERR_4	INT_-FORCE0_-FORCE_ACK_WITH_ERR_3	INT_-FORCE0_-FORCE_ACK_WITH_ERR_2	INT_-FORCE0_-FORCE_ACK_WITH_ERR_1	INT_-FORCE0_-FORCE_ACK_WITH_ERR_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INT_-FORCE0_-FORCE_ACK_WITH_ERR_15	INT_-FORCE0_-FORCE_ACK_WITH_ERR_14	INT_-FORCE0_-FORCE_ACK_WITH_ERR_13	INT_-FORCE0_-FORCE_ACK_WITH_ERR_12	INT_-FORCE0_-FORCE_ACK_WITH_ERR_11	INT_-FORCE0_-FORCE_ACK_WITH_ERR_10	INT_-FORCE0_-FORCE_ACK_WITH_ERR_9	INT_-FORCE0_-FORCE_ACK_WITH_ERR_8

Bits	23	22	21	20	19	18	17	16
SW Access	R			RW	RW	RW	RW	RW
HW Access	R			R	R	R	R	R
Name	INT_FORCE0_RESERVED_31_21 [23:21]			INT_-FORCE0_-FORCE_DPHY_ER-RORS_4	INT_-FORCE0_-FORCE_DPHY_ER-RORS_3	INT_-FORCE0_-FORCE_DPHY_ER-RORS_2	INT_-FORCE0_-FORCE_DPHY_ER-RORS_1	INT_-FORCE0_-FORCE_DPHY_ER-RORS_0

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	INT_FORCE0_RESERVED_31_21 [31:24]							

Bits	Name	Description
31 : 21	INT_FORCE0_RE-SERVED_31_21	Reserved and read as zero. Default Value: 0x0
20	INT_FORCE0_FORCE_D-PHY_ERRORS_4	Force dphy_errors_4 Default Value: 0x0
19	INT_FORCE0_FORCE_D-PHY_ERRORS_3	Force dphy_errors_3 Default Value: 0x0
18	INT_FORCE0_FORCE_D-PHY_ERRORS_2	Force dphy_errors_2 Default Value: 0x0
17	INT_FORCE0_FORCE_D-PHY_ERRORS_1	Force dphy_errors_1 Default Value: 0x0
16	INT_FORCE0_FORCE_D-PHY_ERRORS_0	Force dphy_errors_0 Default Value: 0x0

27.1.210 GFXSS_MIPIDSI_DWCMIPIDSI_INT_FORCE0 (continued)

15	INT_FORCE0_-FORCE_ACK_WITH_ER-R_15	Force ack_with_err_15 Default Value: 0x0
14	INT_FORCE0_-FORCE_ACK_WITH_ER-R_14	Force ack_with_err_14 Default Value: 0x0
13	INT_FORCE0_-FORCE_ACK_WITH_ER-R_13	Force ack_with_err_13 Default Value: 0x0
12	INT_FORCE0_-FORCE_ACK_WITH_ER-R_12	Force ack_with_err_12 Default Value: 0x0
11	INT_FORCE0_-FORCE_ACK_WITH_ER-R_11	Force ack_with_err_11 Default Value: 0x0
10	INT_FORCE0_-FORCE_ACK_WITH_ER-R_10	Force ack_with_err_10 Default Value: 0x0
9	INT_FORCE0_-FORCE_ACK_WITH_ER-R_9	Force ack_with_err_9 Default Value: 0x0
8	INT_FORCE0_-FORCE_ACK_WITH_ER-R_8	Force ack_with_err_8 Default Value: 0x0
7	INT_FORCE0_-FORCE_ACK_WITH_ER-R_7	Force ack_with_err_7 Default Value: 0x0
6	INT_FORCE0_-FORCE_ACK_WITH_ER-R_6	Force ack_with_err_6 Default Value: 0x0
5	INT_FORCE0_-FORCE_ACK_WITH_ER-R_5	Force ack_with_err_5 Default Value: 0x0
4	INT_FORCE0_-FORCE_ACK_WITH_ER-R_4	Force ack_with_err_4 Default Value: 0x0
3	INT_FORCE0_-FORCE_ACK_WITH_ER-R_3	Force ack_with_err_3 Default Value: 0x0
2	INT_FORCE0_-FORCE_ACK_WITH_ER-R_2	Force ack_with_err_2 Default Value: 0x0
1	INT_FORCE0_-FORCE_ACK_WITH_ER-R_1	Force ack_with_err_1 Default Value: 0x0
0	INT_FORCE0_-FORCE_ACK_WITH_ER-R_0	Force ack_with_err_0 Default Value: 0x0

27.1.211 GFXSS_MIPIDSI_DWCMIPIDSI_INT_FORCE1

Description: Forces interrupts that affect the INT_ST1 register.

Address: 0x448030DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INT_-FORCE1_-FORCE_DPI_PLD_WR_ERR	INT_-FORCE1_-FORCE_EOPT_ERR	INT_-FORCE1_-FORCE_PKT_-SIZE_ERR	INT_-FORCE1_-FORCE_CRC_ERR	INT_-FORCE1_-FORCE_ECC_MULT-PL_ERR	INT_-FORCE1_-FORCE_ECC_SIN-GLE_ERR	INT_-FORCE1_-FORCE_TO_LP_RX	INT_-FORCE1_-FORCE_TO_HS_TX

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INT_-FORCE1_-FORCE_DBI_PLD_RD_ERR	INT_-FORCE1_-FORCE_DBI_PLD_WR_ERR	INT_-FORCE1_-FORCE_DBI_CM-D_WR_ERR	INT_-FORCE1_-FORCE_GEN_PLD_RE-CEV_ERR	INT_-FORCE1_-FORCE_GEN_PLD_RD_ERR	INT_-FORCE1_-FORCE_GEN_PLD_SEND_ERR	INT_-FORCE1_-FORCE_GEN_PLD_WR_ERR	INT_-FORCE1_-FORCE_GEN_CM-D_WR_ERR

Bits	23	22	21	20	19	18	17	16
SW Access	R			R	RW	R	RW	RW
HW Access	R			R	R	R	R	R
Name	INT_FORCE1_RESERVED_31_21 [23:21]			INT_-FORCE1_RES-ERVED_20	INT_-FORCE1_-FORCE_DPI_BUFF_PLD_UNDER	INT_-FORCE1_RES-ERVED_18	INT_-FORCE1_-FORCE_DBI_ILE-GAL_COM-M_ERR	INT_-FORCE1_-FORCE_DBI_PLD_RECV_ERR

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	INT_FORCE1_RESERVED_31_21 [31:24]							

Bits	Name	Description
31 : 21	INT_FORCE1_RE-SERVED_31_21	Reserved and read as zero. Default Value: 0x0
20	INT_FORCE1_RE-SERVED_20	Reserved and read as zero Default Value: 0x0
19	INT_FORCE1_FORCE_D-PI_BUFF_PLD_UNDER	Force for dpi_buff_pld_under. Default Value: 0x0
18	INT_FORCE1_RE-SERVED_18	Reserved and read as zero Default Value: 0x0
17	INT_FORCE1_FORCE_D-BI_ILEGAL_COMM_ERR	Force dbi_ilegal_comm_err. Default Value: 0x0

27.1.211 GFXSS_MIPIDSI_DWCMIPIDSI_INT_FORCE1 (continued)

16	INT_FORCE1_FORCE_DBI_PLD_RECV_ERR	Force dbi_pld_recv_err. Default Value: 0x0
15	INT_FORCE1_FORCE_DBI_PLD_RD_ERR	Force dbi_pld_rd_err. Default Value: 0x0
14	INT_FORCE1_FORCE_DBI_PLD_WR_ERR	Force dbi_pld_wr_err. Default Value: 0x0
13	INT_FORCE1_FORCE_DBI_CMD_WR_ERR	Force dbi_cmd_wr_err. Default Value: 0x0
12	INT_FORCE1_FORCE_GEN_PLD_RECEV_ERR	Force gen_pld_recev_err Default Value: 0x0
11	INT_FORCE1_FORCE_GEN_PLD_RD_ERR	Force gen_pld_rd_err Default Value: 0x0
10	INT_FORCE1_FORCE_GEN_PLD_SEND_ERR	Force gen_pld_send_err Default Value: 0x0
9	INT_FORCE1_FORCE_GEN_PLD_WR_ERR	Force gen_pld_wr_err Default Value: 0x0
8	INT_FORCE1_FORCE_GEN_CMD_WR_ERR	Force gen_cmd_wr_err Default Value: 0x0
7	INT_FORCE1_FORCE_DPI_PLD_WR_ERR	Force dpi_pld_wr_err Default Value: 0x0
6	INT_FORCE1_FORCE_EOPT_ERR	Force eopt_err Default Value: 0x0
5	INT_FORCE1_FORCE_PKT_SIZE_ERR	Force pkt_size_err Default Value: 0x0
4	INT_FORCE1_FORCE_CRC_ERR	Force crc_err Default Value: 0x0
3	INT_FORCE1_FORCE_ECC_MULTPL_ERR	Force ecc_multpl_err Default Value: 0x0
2	INT_FORCE1_FORCE_ECC_SINGLE_ERR	Force ecc_single_err Default Value: 0x0
1	INT_FORCE1_FORCE_TO_LP_RX	Force to_lp_rx Default Value: 0x0
0	INT_FORCE1_FORCE_TO_HS_TX	Force to_hs_tx Default Value: 0x0

27.1.212 GFXSS_MIPIDSI_DWCMIPIDSI_DSC_PARAMETER

Description: Configures Display Stream Compression.

Address: 0x448030F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							RW
HW Access	R							R
Name	DSC_PARAMETER_RESERVED_7_1 [7:1]							DSC_PARAMETER_COMPRESSION_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	R						RW	
HW Access	R						R	
Name	DSC_PARAMETER_RESERVED_15_10 [15:10]						DSC_PARAMETER_COMPRESS_ALGO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R						RW	
HW Access	R						R	
Name	DSC_PARAMETER_RESERVED_31_18 [23:18]						DSC_PARAMETER_PPS_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DSC_PARAMETER_RESERVED_31_18 [31:24]							

Bits	Name	Description
31 : 18	DSC_PARAMETER_RESERVED_31_18	Reserved and read as zero. Default Value: 0x0
17 : 16	DSC_PARAMETER_PPS_SEL	This field indicates the PPS selector: Default Value: 0x0 **0x0: PPSSEL0 :** (none) **0x1: PPSSEL1 :** (none) **0x2: PPSSEL2 :** (none)

27.1.212 GFXSS_MIPIDSI_DWCMIPIDSI_DSC_PARAMETER (continued)

		0x3: PPSSEL3 : (none)
15 : 10	DSC_PARAMETER_RESERVED_15_10	Reserved and read as zero. Default Value: 0x0
9 : 8	DSC_PARAMETER_COMPRESS_ALGO	This field indicates the algorithm identifier: Default Value: 0x0
		0x0: ALGO0 : (none)
		0x1: ALGO1 : (none)
		0x2: ALGO2 : (none)
		0x3: ALGO3 : (none)
7 : 1	DSC_PARAMETER_RESERVED_7_1	Reserved and read as zero. Default Value: 0x0
0	DSC_PARAMETER_COMPRESSION_MODE	When set to 1, this bit enables the compression mode. Default Value: 0x0

27.1.213 GFXSS_MIPIDSI_DWCMIPIDSI_PHY_TMR_RD_CFG

Description: Configures times related to PHY to perform some operations in lane byte clock cycles.

Address: 0x448030F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PHY_TMR_RD_CFG_MAX_RD_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	RW						
HW Access	R	R						
Name	PHY_TMR_RD_CFG_RESERVED_31_15	PHY_TMR_RD_CFG_MAX_RD_TIME [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	PHY_TMR_RD_CFG_RESERVED_31_15 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	PHY_TMR_RD_CFG_RESERVED_31_15 [31:24]							

Bits	Name	Description
31 : 15	PHY_TMR_RD_CFG_RESERVED_31_15	Reserved and read as zero. Default Value: 0x0
14 : 0	PHY_TMR_RD_CFG_MAX_RD_TIME	This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when no read command is in progress. Default Value: 0x0

27.1.214 GFXSS_MIPIDSI_DWCMIPIDSI_VID_SHADOW_CTRL

Description: Controls dpi shadow feature

Address: 0x44803100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							RW
HW Access	R							R
Name	VID_SHADOW_CTRL_RESERVED_7_1 [7:1]							VID_SHADOW_CTRL_VID_SHADOW_EN

Bits	15	14	13	12	11	10	9	8
SW Access	R							RW
HW Access	R							R
Name	VID_SHADOW_CTRL_RESERVED_15_9 [15:9]							VID_SHADOW_CTRL_VID_SHADOW_REQ

Bits	23	22	21	20	19	18	17	16
SW Access	R							RW
HW Access	R							R
Name	VID_SHADOW_CTRL_RESERVED_31_17 [23:17]							VID_SHADOW_CTRL_VID_SHADOW_PIN_REQ

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_SHADOW_CTRL_RESERVED_31_17 [31:24]							

Bits	Name	Description
31 : 17	VID_SHADOW_CTRL_RESERVED_31_17	Reserved and read as zero. Default Value: 0x0
16	VID_SHADOW_CTRL_VID_SHADOW_PIN_REQ	When set to 1, the video request is done by external pin. In this mode vid_shadow_req is ignored. Default Value: 0x0
15 : 9	VID_SHADOW_CTRL_RESERVED_15_9	Reserved and read as zero. Default Value: 0x0
8	VID_SHADOW_CTRL_VID_SHADOW_REQ	When set to 1, this bit request that the dpi registers from regbank are copied to the auxiliary registers. When the request is completed this bit is auto clear. Default Value: 0x0
7 : 1	VID_SHADOW_CTRL_RESERVED_7_1	Reserved and read as zero. Default Value: 0x0

27.1.214 GFXSS_MIPIDSI_DWCMIPIDSI_VID_SHADOW_CTRL (continued)

0	VID_SHADOW_CTRL_VID_SHADOW_EN	When set to 1, DPI receives the active configuration from the auxiliary registers. When the feature is set at the same time than vid_shadow_req the auxiliary registers are automatically updated. Default Value: 0x0

27.1.215 GFXSS_MIPIDSI_DWCMIPIDSI_DPI_VCID_ACT

Description: Holds the value that controller is using for DPI_VCID.

Address: 0x4480310C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						R	
HW Access	R						W	
Name	DPI_VCID_ACT_RESERVED_31_2 [7:2]						DPI_VCID_ACT_DPI_VCID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	DPI_VCID_ACT_RESERVED_31_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	DPI_VCID_ACT_RESERVED_31_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DPI_VCID_ACT_RESERVED_31_2 [31:24]							

Bits	Name	Description
31 : 2	DPI_VCID_ACT_RESERVED_31_2	Reserved and read as zero. Default Value: 0x0
1 : 0	DPI_VCID_ACT_DPI_VCID	This field specifies the DPI virtual channel id that is indexed to the Video mode packets. Default Value: 0x0

27.1.216 GFXSS_MIPIDSI_DWCMIPIDSI_DPI_COLOR_CODING_ACT

Description: Holds the value that controller is using for DPI_COLOR_CODING.

Address: 0x44803110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				W			
Name	DPI_COLOR_CODING_ACT_RESERVED_7_4 [7:4]				DPI_COLOR_CODING_ACT_DPI_COLOR_CODING [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							R
HW Access	R							W
Name	DPI_COLOR_CODING_ACT_RESERVED_31_9 [15:9]							DPI_COLOR_CODING_ACT_LOOSELY18_EN

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	DPI_COLOR_CODING_ACT_RESERVED_31_9 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DPI_COLOR_CODING_ACT_RESERVED_31_9 [31:24]							

Bits	Name	Description
31 : 9	DPI_COLOR_CODING_ACT_RESERVED_31_9	Reserved and read as zero. Default Value: 0x0
8	DPI_COLOR_CODING_ACT_LOOSELY18_EN	When 1, this bit activates loosely packed variant to 18-bit configurations. Default Value: 0x0
7 : 4	DPI_COLOR_CODING_ACT_RESERVED_7_4	Reserved and read as zero. Default Value: 0x0
3 : 0	DPI_COLOR_CODING_ACT_DPI_COLOR_CODING	This field configures the DPI color for Video Mode/eDPI Command Mode coding as follows: Default Value: 0x0 **0x0: CC00 :** (none) **0x1: CC01 :** (none)

27.1.216 GFXSS_MIPIDSI_DWCMIPIDSI_DPI_COLOR_CODING_ACT (continued)

0x2: CC02 :

(none)

0x3: CC03 :

(none)

0x4: CC04 :

(none)

0x5: CC05 :

(none)

0x6: CC06 :

(none)

0x7: CC07 :

(none)

0x8: CC08 :

(none)

0x9: CC09 :

(none)

0xa: CC10 :

(none)

0xb: CC11 :

(none)

0xc: CC12 :

(none)

0xd: CC13 :

(none)

0xe: CC14 :

(none)

0xf: CC15 :

(none)

27.1.217 GFXSS_MIPIDSI_DWCMIPIDSI_DPI_LP_CMD_TIM_ACT

Description: Holds the value that controller is using for DPI_LP_CMD_TIM.

Address: 0x44803118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DPI_LP_CMD_TIM_ACT_INVACT_LPCMD_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	DPI_LP_CMD_TIM_ACT_RESERVED_15_8 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DPI_LP_CMD_TIM_ACT_OUTVACT_LPCMD_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	DPI_LP_CMD_TIM_ACT_RESERVED_31_24 [31:24]							

Bits	Name	Description
31 : 24	DPI_LP_CMD_TIM_ACT_RESERVED_31_24	Reserved and read as zero. Default Value: 0x0
23 : 16	DPI_LP_CMD_TIM_ACT_OUTVACT_LPCMD_TIME	This field is used for the transmission of commands in low-power mode. It specifies the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions. Default Value: 0x0
15 : 8	DPI_LP_CMD_TIM_ACT_RESERVED_15_8	Reserved and read as zero. Default Value: 0x0
7 : 0	DPI_LP_CMD_TIM_ACT_INVACT_LPCMD_TIME	This field is used for the transmission of commands in low-power mode. It specifies the size, in bytes, of the largest packet that can fit in a line during the VACT region. Default Value: 0x0

27.1.218 GFXSS_MIPIDSI_DWCMIPIDSI_VID_MODE_CFG_ACT

Description: Holds the value that controller is using for VID_MODE_CFG.

Address: 0x44803138

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	
HW Access	W	W	W	W	W	W	W	
Name	VID_-MODE_CF-G_ACT_LP_HFP_EN	VID_-MODE_CF-G_ACT_LP_HBP_EN	VID_-MODE_CF-G_ACT_LP_VACT_EN	VID_-MODE_CF-G_ACT_LP_VFP_EN	VID_-MODE_CF-G_ACT_LP_VBP_EN	VID_-MODE_CF-G_ACT_LP_VSA_EN	VID_MODE_CF-G_ACT_VID_MODE_-TYPE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R						R	R
HW Access	R						W	W
Name	VID_MODE_CFG_ACT_RESERVED_31_10 [15:10]						VID_-MODE_CF-G_ACT_LP_CMD_EN	VID_-MODE_CF-G_ACT_FRAME_BTA_ACK_EN

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_MODE_CFG_ACT_RESERVED_31_10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_MODE_CFG_ACT_RESERVED_31_10 [31:24]							

Bits	Name	Description
31 : 10	VID_MODE_CF-G_ACT_RE-SERVED_31_10	Reserved and read as zero. Default Value: 0x0
9	VID_MODE_CF-G_ACT_LP_CMD_EN	When 1, this bit enables the command transmission only in low-power mode. Default Value: 0x0
8	VID_MODE_CFG_ACT_-FRAME_BTA_ACK_EN	When 1, this bit enables the request for an acknowledge response at the end of a frame. Default Value: 0x0
7	VID_MODE_CF-G_ACT_LP_HFP_EN	When 1, this bit enables the return to low-power inside the HFP period when timing allows. Default Value: 0x0
6	VID_MODE_CF-G_ACT_LP_HBP_EN	When 1, this bit enables the return to low-power inside the HBP period when timing allows. Default Value: 0x0
5	VID_MODE_CF-G_ACT_LP_VACT_EN	When 1, this bit enables the return to low-power inside the VACT period when timing allows. Default Value: 0x0
4	VID_MODE_CF-G_ACT_LP_VFP_EN	When 1, this bit enables the return to low-power inside the VFP period when timing allows. Default Value: 0x0
3	VID_MODE_CF-G_ACT_LP_VBP_EN	When 1, this bit enables the return to low-power inside the VBP period when timing allows. Default Value: 0x0

27.1.218 GFXSS_MIPIDSI_DWCMIPIDSI_VID_MODE_CFG_ACT (continued)

2	VID_MODE_CF-G_ACT_LP_VSA_EN	When 1, this bit enables the return to low-power inside the VSA period when timing allows. Default Value: 0x0
1 : 0	VID_MODE_CF-G_ACT_VID_MODE_-TYPE	This field specifies the video mode transmission type as follows: Default Value: 0x0 **0x0: VIDMODE0 :** (none) **0x1: VIDMODE1 :** (none) **0x2: VIDMODE2 :** (none) **0x3: VIDMODE3 :** (none)

27.1.219 GFXSS_MIPIDSI_DWCMIPIDSI_VID_PKT_SIZE_ACT

Description: Holds the value that controller is using for VID_PKT_SIZE.

Address: 0x4480313C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VID_PKT_SIZE_ACT_VID_PKT_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R		R					
HW Access	R		W					
Name	VID_PKT_SIZE_ACT_RESERVED_31_14 [15:14]		VID_PKT_SIZE_ACT_VID_PKT_SIZE [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_PKT_SIZE_ACT_RESERVED_31_14 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_PKT_SIZE_ACT_RESERVED_31_14 [31:24]							

Bits	Name	Description
31 : 14	VID_PKT_SIZE_ACT_RESERVED_31_14	Reserved and read as zero. Default Value: 0x0
13 : 0	VID_PKT_SIZE_ACT_VID_PKT_SIZE	This field specifies the number of pixels in a single video packet. For 18-bit not loosely packed this number must be a multiple of 4 and YCbCr Data Types, it must be a multiple of 2, as described in DSI specification. Default Value: 0x0

27.1.220 GFXSS_MIPIDSI_DWCMIPIDSI_VID_NUM_CHUNKS_ACT

Description: This register holds the value that controller is using for VID_NUM_CHUNKS.

Address: 0x44803140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VID_NUM_CHUNKS_ACT_VID_NUM_CHUNKS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R			R				
HW Access	R			W				
Name	VID_NUM_CHUNKS_ACT_RE-SERVED_31_13 [15:13]			VID_NUM_CHUNKS_ACT_VID_NUM_CHUNKS [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_NUM_CHUNKS_ACT_RESERVED_31_13 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_NUM_CHUNKS_ACT_RESERVED_31_13 [31:24]							

Bits	Name	Description
31 : 13	VID_NUM_CHUNKS_ACT_RESERVED_31_13	Reserved and read as zero. Default Value: 0x0
12 : 0	VID_NUM_CHUNKS_ACT_VID_NUM_CHUNKS	This register specifies the number of chunks to be transmitted during a Line period (a chunk is pair made of a video packet and a null packet). If set to 0 or 1, video line is still transmitted in a single packet. If set to 1 that packet is part of a chunk, meaning that a null packet follows it (if vid_null_size>0). Otherwise, multiple chunks are used to transmit each video line. Default Value: 0x0

27.1.221 GFXSS_MIPIDSI_DWCMIPIDSI_VID_NULL_SIZE_ACT

Description: Holds the value that controller is using for VID_NULL_SIZE.

Address: 0x44803144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VID_NULL_SIZE_ACT_VID_NULL_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R			R				
HW Access	R			W				
Name	VID_NULL_SIZE_ACT_RESERVED_31_13 [15:13]			VID_NULL_SIZE_ACT_VID_NULL_SIZE [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_NULL_SIZE_ACT_RESERVED_31_13 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_NULL_SIZE_ACT_RESERVED_31_13 [31:24]							

Bits	Name	Description
31 : 13	VID_NULL_- SIZE_ACT_RE- SERVED_31_13	Reserved and read as zero. Default Value: 0x0
12 : 0	VID_NULL_- SIZE_ACT_VID_NULL_- SIZE	This register specifies the number of bytes inside a null packet. Setting to 0 disables null packets. Default Value: 0x0

27.1.222 GFXSS_MIPIDSI_DWCMIPIDSI_VID_HSA_TIME_ACT

Description: Holds the value that controller is using for VID_HSA_TIME.

Address: 0x44803148

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VID_HSA_TIME_ACT_VID_HSA_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	R				W			
Name	VID_HSA_TIME_ACT_RESERVED_31_12 [15:12]				VID_HSA_TIME_ACT_VID_HSA_TIME [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_HSA_TIME_ACT_RESERVED_31_12 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_HSA_TIME_ACT_RESERVED_31_12 [31:24]							

Bits	Name	Description
31 : 12	VID_HSA_- TIME_ACT_RE- SERVED_31_12	Reserved and read as zero. Default Value: 0x0
11 : 0	VID_HSA_- TIME_ACT_VID_HSA_- TIME	This field specifies the Horizontal Synchronism Active period in lane byte clock cycles. Default Value: 0x0

27.1.223 GFXSS_MIPIDSI_DWCMIPIDSI_VID_HBP_TIME_ACT

Description: Holds the value that controller is using for VID_HBP_TIME.

Address: 0x4480314C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VID_HBP_TIME_ACT_VID_HBP_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	R				W			
Name	VID_HBP_TIME_ACT_RESERVED_31_12 [15:12]				VID_HBP_TIME_ACT_VID_HBP_TIME [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_HBP_TIME_ACT_RESERVED_31_12 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_HBP_TIME_ACT_RESERVED_31_12 [31:24]							

Bits	Name	Description
31 : 12	VID_HBP_- TIME_ACT_RE- SERVED_31_12	Reserved and read as zero. Default Value: 0x0
11 : 0	VID_HBP_- TIME_ACT_VID_HBP_- TIME	This field specifies the Horizontal Back Porch period in lane byte clock cycles. Default Value: 0x0

27.1.224 GFXSS_MIPIDSI_DWCMIPIDSI_VID_HLINE_TIME_ACT

Description: Holds the value that controller is using for VID_HLINE_TIME.

Address: 0x44803150

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VID_HLINE_TIME_ACT_VID_HLINE_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	R	W						
Name	VID_H-LINE_-TIME_ACT_RE-SERVED_31_15	VID_HLINE_TIME_ACT_VID_HLINE_TIME [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_HLINE_TIME_ACT_RESERVED_31_15 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_HLINE_TIME_ACT_RESERVED_31_15 [31:24]							

Bits	Name	Description
31 : 15	VID_HLINE_-TIME_ACT_RE-SERVED_31_15	Reserved and read as zero. Default Value: 0x0
14 : 0	VID_HLINE_-TIME_ACT_VID_HLINE_-TIME	This field specifies the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles. Default Value: 0x0

27.1.225 GFXSS_MIPIDSI_DWCMIPIDSI_VID_VSA_LINES_ACT

Description: Holds the value that controller is using for VID_VSA_LINES.

Address: 0x44803154

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VID_VSA_LINES_ACT_VSA_LINES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R						R	
HW Access	R						W	
Name	VID_VSA_LINES_ACT_RESERVED_31_10 [15:10]						VID_VSA_LINES_ACT_VSA_LINES [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_VSA_LINES_ACT_RESERVED_31_10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_VSA_LINES_ACT_RESERVED_31_10 [31:24]							

Bits	Name	Description
31 : 10	VID_VSA_LINES_ACT_RESERVED_31_10	Reserved and read as zero. Default Value: 0x0
9 : 0	VID_VSA_LINES_ACT_VSA_LINES	This field specifies the Vertical Synchronism Active period measured in number of horizontal lines. Default Value: 0x0

27.1.226 GFXSS_MIPIDSI_DWCMIPIDSI_VID_VBP_LINES_ACT

Description: Holds the value that controller is using for VID_VBP_LINES.

Address: 0x44803158

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VID_VBP_LINES_ACT_VBP_LINES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R						R	
HW Access	R						W	
Name	VID_VBP_LINES_ACT_RESERVED_31_10 [15:10]						VID_VB-P_LINES_ACT_VB-P_LINES [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_VBP_LINES_ACT_RESERVED_31_10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_VBP_LINES_ACT_RESERVED_31_10 [31:24]							

Bits	Name	Description
31 : 10	VID_VB-P_LINES_ACT_RE-SERVED_31_10	Reserved and read as zero. Default Value: 0x0
9 : 0	VID_VB-P_LINES_ACT_VB-P_LINES	This field specifies the Vertical Back Porch period measured in number of horizontal lines. Default Value: 0x0

27.1.227 GFXSS_MIPIDSI_DWCMIPIDSI_VID_VFP_LINES_ACT

Description: Holds the value that controller is using for VID_VFP_LINES.

Address: 0x4480315C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VID_VFP_LINES_ACT_VFP_LINES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R						R	
HW Access	R						W	
Name	VID_VFP_LINES_ACT_RESERVED_31_10 [15:10]						VID_VF-P_LINES_ACT_VF-P_LINES [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_VFP_LINES_ACT_RESERVED_31_10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_VFP_LINES_ACT_RESERVED_31_10 [31:24]							

Bits	Name	Description
31 : 10	VID_VF-P_LINES_ACT_RE-SERVED_31_10	Reserved and read as zero. Default Value: 0x0
9 : 0	VID_VF-P_LINES_ACT_VF-P_LINES	This field specifies the Vertical Front Porch period measured in number of horizontal lines. Default Value: 0x0

27.1.228 GFXSS_MIPIDSI_DWCMIPIDSI_VID_VACTIVE_LINES_ACT

Description: Holds the value that controller is using for VID_VACTIVE_LINES.

Address: 0x44803160

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VID_VACTIVE_LINES_ACT_V_ACTIVE_LINES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R		R					
HW Access	R		W					
Name	VID_VACTIVE_LINES_ACT_RESERVED_31_14 [15:14]		VID_VACTIVE_LINES_ACT_V_ACTIVE_LINES [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VID_VACTIVE_LINES_ACT_RESERVED_31_14 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_VACTIVE_LINES_ACT_RESERVED_31_14 [31:24]							

Bits	Name	Description
31 : 14	VID_VACTIVE_LINES_ACT_RESERVED_31_14	Reserved and read as zero. Default Value: 0x0
13 : 0	VID_VACTIVE_LINES_ACT_V_ACTIVE_LINES	This field specifies the Vertical Active period measured in number of horizontal lines. Default Value: 0x0

27.1.229 GFXSS_MIPIDSI_DWCMIPIDSI_VID_PKT_STATUS

Description: Contains information about the status of FIFOs related to DPI and eDPI interfaces.

Address: 0x44803168

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	R	R	R	R	W	W	W	W
Name	VID_PKT_STATUS_RESERVED_7	VID_PKT_STATUS_RESERVED_6	VID_PKT_STATUS_RESERVED_5	VID_PKT_STATUS_RESERVED_4	VID_PKT_STATUS_DPI_PLD_W_FULL	VID_PKT_STATUS_DPI_PLD_W_EMPTY	VID_PKT_STATUS_DPI_CMD_W_FULL	VID_PKT_STATUS_DPI_CMD_W_EMPTY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VID_PKT_STATUS_RESERVED_15_8 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R		R	R
HW Access	R	R	R	R	R		W	W
Name	VID_PKT_STATUS_RESERVED_23	VID_PKT_STATUS_RESERVED_22	VID_PKT_STATUS_RESERVED_21	VID_PKT_STATUS_RESERVED_20	VID_PKT_STATUS_RESERVED_19_18 [19:18]		VID_PKT_STATUS_DPI_BUFF_PLD_FULL	VID_PKT_STATUS_DPI_BUFF_PLD_EMPTY

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VID_PKT_STATUS_RESERVED_31_24 [31:24]							

Bits	Name	Description
31 : 24	VID_PKT_STATUS_RESERVED_31_24	Reserved and read as zero. Default Value: 0x0
23	VID_PKT_STATUS_RESERVED_23	Reserved and read as zero Default Value: 0x0
22	VID_PKT_STATUS_RESERVED_22	Reserved and read as zero Default Value: 0x0
21	VID_PKT_STATUS_RESERVED_21	Reserved and read as zero Default Value: 0x0
20	VID_PKT_STATUS_RESERVED_20	Reserved and read as zero Default Value: 0x0
19 : 18	VID_PKT_STATUS_RESERVED_19_18	Reserved and read as zero. Default Value: 0x0
17	VID_PKT_STATUS_DPI_BUFF_PLD_FULL	This bit indicates the full status of the payload internal buffer for video Mode. This bit is set to 0 for command Mode. Default Value: 0x0

27.1.229 GFXSS_MIPIDSI_DWCMIPIDSI_VID_PKT_STATUS (continued)

16	VID_PKT_STATUS_DPI_BUFF_PLD_EMPTY	This bit indicates the empty status of the payload internal buffer for video Mode. This bit is set to 0 for command Mode. Default Value: 0x1
15 : 8	VID_PKT_STATUS_RESERVED_15_8	Reserved and read as zero. Default Value: 0x0
7	VID_PKT_STATUS_RESERVED_7	Reserved and read as zero Default Value: 0x0
6	VID_PKT_STATUS_RESERVED_6	Reserved and read as zero Default Value: 0x0
5	VID_PKT_STATUS_RESERVED_5	Reserved and read as zero Default Value: 0x0
4	VID_PKT_STATUS_RESERVED_4	Reserved and read as zero Default Value: 0x0
3	VID_PKT_STATUS_DPI_PLD_W_FULL	This bit indicates the full status of write payload FIFO for video Mode. This bit is set to 0 for command Mode. Default Value: 0x0
2	VID_PKT_STATUS_DPI_PLD_W_EMPTY	This bit indicates the empty status of write payload FIFO for video Mode. This bit is set to 0 for command Mode. Default Value: 0x1
1	VID_PKT_STATUS_DPI_CMD_W_FULL	This bit indicates the full status of write command FIFO for video Mode. This bit is set to 0 for command Mode. Default Value: 0x0
0	VID_PKT_STATUS_DPI_CMD_W_EMPTY	This bit indicates the empty status of write command FIFO for video Mode. This bit is set to 0 for command Mode. Default Value: 0x1

27.1.230 GFXSS_MIPIDSI_DWCMIPIDSI_SDF_3D_ACT

Description: Holds the value that controller is using for SDF_3D.

Address: 0x44803190

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R	R	R		R	
HW Access	R		W	W	W		W	
Name	SDF_3D_ACT_RESERVED_15_6 [7:6]		SDF_3D_ACT_RIGHT_FIRST	SDF_3D_ACT_SECOND_VSYNC	SDF_3D_ACT_FORMAT_3D [3:2]		SDF_3D_ACT_MODE_3D [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	SDF_3D_ACT_RESERVED_15_6 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							R
HW Access	R							W
Name	SDF_3D_ACT_RESERVED_31_17 [23:17]							SDF_3D_ACT_SEND_3D_CFG

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	SDF_3D_ACT_RESERVED_31_17 [31:24]							

Bits	Name	Description
31 : 17	SDF_3D_ACT_RESERVED_31_17	Reserved and read as zero. Default Value: 0x0
16	SDF_3D_ACT_SEND_3D_CFG	When set, causes the next VSS packet to include 3D control payload in every VSS packet. Default Value: 0x0
15 : 6	SDF_3D_ACT_RESERVED_15_6	Reserved and read as zero. Default Value: 0x0
5	SDF_3D_ACT_RIGHT_FIRST	This bit specifies the left/right order: Default Value: 0x0 **0x0: LEFTFIRST :** (none) **0x1: RIGHTFIRST :** (none)

27.1.230 GFXSS_MIPIDSI_DWCMIPIDSI_SDF_3D_ACT (continued)

4	SDF_3D_ACT_SECOND_VSYNC	This field specifies whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: Default Value: 0x0 **0x0: NOSYNCPULSE :** (none) **0x1: SYNCPULSE :** (none)
3 : 2	SDF_3D_ACT_FORMAT_3D	This field specifies 3D Image Format: Default Value: 0x0 **0x1: FRAME :** (none) **0x0: LINE :** (none) **0x2: PIXEL :** (none) **0x3: RESERVED :** (none)
1 : 0	SDF_3D_ACT_MODE_3D	This field specifies 3D Mode On/Off and Display Orientation: Default Value: 0x0 **0x0: MODE0 :** (none) **0x1: MODE1 :** (none) **0x2: MODE2 :** (none) **0x3: MODE3 :** (none)

28 Autonomous Analog registers

This section discusses the Autonomous Analog registers. It lists all the registers in mapping tables, in address order.

28.1 Register details

Register name	Address	Description
CTBL0_STA_CFG	0x42E00400	Configuration (only accessible if ACTRLR.STATUS.MODE=0)
CTBL0_STA_COMP_STAT	0x42E00404	Comparator status
CTBL0_DYN0_OA_MUX_CFG	0x42E00600	Opamp Mux Configuration
CTBL0_DYN1_OA_MUX_CFG	0x42E00610	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL0_DYN2_OA_MUX_CFG	0x42E00620	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL0_DYN3_OA_MUX_CFG	0x42E00630	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL0_DYN4_OA_MUX_CFG	0x42E00640	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL0_DYN5_OA_MUX_CFG	0x42E00650	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL0_DYN6_OA_MUX_CFG	0x42E00660	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL0_DYN7_OA_MUX_CFG	0x42E00670	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL0_TRIM_OA0_OFFSET_TRIM	0x42E00F00	Opamp0 trim control
CTBL0_TRIM_OA0_SLOPE_OFFSET_TRIM	0x42E00F04	Opamp0 trim control
CTBL0_TRIM_OA0_COMP_TRIM	0x42E00F08	Opamp0 trim control
CTBL0_TRIM_OA1_OFFSET_TRIM	0x42E00F0C	Opamp1 trim control
CTBL0_TRIM_OA1_SLOPE_OFFSET_TRIM	0x42E00F10	Opamp1 trim control
CTBL0_TRIM_OA1_COMP_TRIM	0x42E00F14	Opamp1 trim control
CTBL0_TRIM_RMP_TRIM	0x42E00F18	Risk Mitigation bits

Autonomous Analog registers

Register name	Address	Description
CTBL1_STA_CFG	0x42E10400	Configuration (only accessible if ACTRLR.STATUS.MODE=0). See CTBL0_STA_CFG for the details of bit fields.
CTBL1_STA_COMP_STAT	0x42E10404	Comparator status. See CTBL0_STA_COMP_STAT for the details of bit fields.
CTBL1_DYN0_OA_MUX_CFG	0x42E10600	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL1_DYN1_OA_MUX_CFG	0x42E10610	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL1_DYN2_OA_MUX_CFG	0x42E10620	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL1_DYN3_OA_MUX_CFG	0x42E10630	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL1_DYN4_OA_MUX_CFG	0x42E10640	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL1_DYN5_OA_MUX_CFG	0x42E10650	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL1_DYN6_OA_MUX_CFG	0x42E10660	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL1_DYN7_OA_MUX_CFG	0x42E10670	Opamp Mux Configuration. See CTBL0_DYN0_OA_MUX_CFG for the details of bit fields.
CTBL1_TRIM_OA0_OFFSET_TRIM	0x42E10F00	Opamp0 trim control. See CTBL0_TRIM_OA0_OFFSET_TRIM for the details of bit fields.
CTBL1_TRIM_OA0_SLOPE_OFFSET_TRIM	0x42E10F04	Opamp0 trim control. See CTBL0_TRIM_OA0_SLOPE_OFFSET_TRIM for the details of bit fields.
CTBL1_TRIM_OA0_COMP_TRIM	0x42E10F08	Opamp0 trim control. See CTBL0_TRIM_OA0_COMP_TRIM for the details of bit fields.
CTBL1_TRIM_OA1_OFFSET_TRIM	0x42E10F0C	Opamp1 trim control. See CTBL0_TRIM_OA1_OFFSET_TRIM for the details of bit fields.
CTBL1_TRIM_OA1_SLOPE_OFFSET_TRIM	0x42E10F10	Opamp1 trim control. See CTBL0_TRIM_OA1_SLOPE_OFFSET_TRIM for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
CTBL1_TRIM_OA1_COMP_TRIM	0x42E10F14	Opamp1 trim control. See CTBL0_TRIM_OA1_COMP_TRIM for the details of bit fields.
CTBL1_TRIM_RMP_TRIM	0x42E10F18	Risk Mitigation bits. See CTBL0_TRIM_RMP_TRIM for the details of bit fields.
PTC_STA_CFG	0x42E40400	PTC Configuration Register (only accessible if ACTRLR.STATUS.MODE=0)
PTC_STA_COMP_STAT	0x42E40404	PTC Status Register
PTC_STA_PP_CFG0	0x42E40408	Post Process Configuration register (only accessible if ACTRLR.STATUS.MODE=0)
PTC_STA_PP_CFG1	0x42E4040C	Post Process Configuration register (only accessible if ACTRLR.STATUS.MODE=0). See PTC_STA_PP_CFG0 for the details of bit fields.
PTC_DYN0_MUX_CFG	0x42E40600	PTC Mux Configuration
PTC_DYN1_MUX_CFG	0x42E40610	PTC Mux Configuration. See PTC_DYN0_MUX_CFG for the details of bit fields.
PTC_DYN2_MUX_CFG	0x42E40620	PTC Mux Configuration. See PTC_DYN0_MUX_CFG for the details of bit fields.
PTC_DYN3_MUX_CFG	0x42E40630	PTC Mux Configuration. See PTC_DYN0_MUX_CFG for the details of bit fields.
PTC_DYN4_MUX_CFG	0x42E40640	PTC Mux Configuration. See PTC_DYN0_MUX_CFG for the details of bit fields.
PTC_DYN5_MUX_CFG	0x42E40650	PTC Mux Configuration. See PTC_DYN0_MUX_CFG for the details of bit fields.
PTC_DYN6_MUX_CFG	0x42E40660	PTC Mux Configuration. See PTC_DYN0_MUX_CFG for the details of bit fields.
PTC_DYN7_MUX_CFG	0x42E40670	PTC Mux Configuration. See PTC_DYN0_MUX_CFG for the details of bit fields.
PTC_PP0_CFG	0x42E40700	Post Processing configuration
PTC_PP0_FRAME	0x42E40704	Post Processing frame
PTC_PP0_THRESHOLD	0x42E40708	Post Processing threshold
PTC_PP0_WINDOW	0x42E4070C	Post Processing window
PTC_PP1_CFG	0x42E40710	Post Processing configuration. See PTC_PP0_CFG for the details of bit fields.
PTC_PP1_FRAME	0x42E40714	Post Processing frame. See PTC_PP0_FRAME for the details of bit fields.
PTC_PP1_THRESHOLD	0x42E40718	Post Processing threshold. See PTC_PP0_THRESHOLD for the details of bit fields.
PTC_PP1_WINDOW	0x42E4071C	Post Processing window. See PTC_PP0_WINDOW for the details of bit fields.
PTC_TRIM_CMP0_OFFSET_TRIM	0x42E40F00	Comparator 0 offset trim register
PTC_TRIM_CMP1_OFFSET_TRIM	0x42E40F04	Comparator 1 offset trim register

Autonomous Analog registers

Register name	Address	Description
DAC0_SRAM0	0x42E60000	SRAM Waveform Table (only accessible if ACTRLR.STATUS.MODE=0). This is the starting address of a register bank containing 512 registers (DAC0_SRAM0 to DAC0_SRAM511).
DAC0_STA_CTRL	0x42E60800	DAC control register (only accessible if ACTRLR.STATUS.MODE=0)
DAC0_STA_SAMPLE_TIME	0x42E60804	Sample control register (only accessible if ACTRLR.STATUS.MODE=0)
DAC0_STA_STEP_VAL0	0x42E60808	step val register (only accessible if ACTRLR.STATUS.MODE=0)
DAC0_STA_STEP_VAL1	0x42E6080C	step val register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_STEP_VAL0 for the details of bit fields.
DAC0_STA_STEP_VAL2	0x42E60810	step val register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_STEP_VAL0 for the details of bit fields.
DAC0_STA_DEGLITCH_TIME	0x42E60818	deglitch time register (only accessible if ACTRLR.STATUS.MODE=0)
DAC0_STA_CHAN_CFG0	0x42E60820	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0)
DAC0_STA_CHAN_CFG1	0x42E60824	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG2	0x42E60828	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG3	0x42E6082C	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG4	0x42E60830	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG5	0x42E60834	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG6	0x42E60838	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG7	0x42E6083C	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG8	0x42E60840	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.

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Register name	Address	Description
DAC0_STA_CHAN_CFG9	0x42E60844	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG10	0x42E60848	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG11	0x42E6084C	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG12	0x42E60850	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG13	0x42E60854	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_CHAN_CFG14	0x42E60858	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC0_STA_FW_DAC_VAL	0x42E60860	Firmare Channel DAC Value (only accessible if ACTRLR.STATUS.MODE=0)
DAC0_STA_FW_DAC_VAL_NXT	0x42E60864	Firmware Channel DAC Value Next
DAC0_STA_CHAN_STATUS_CFG0	0x42E60870	Channel status configuration register
DAC0_STA_CHAN_STATUS_CFG1	0x42E60874	Channel status configuration register. See DAC0_STA_CHAN_STATUS_CFG0 for the details of bit fields.
DAC0_STA_CHAN_STATUS_CFG2	0x42E60878	Channel status configuration register. See DAC0_STA_CHAN_STATUS_CFG0 for the details of bit fields.
DAC0_STA_RANGE_STATUS	0x42E60880	Range status register
DAC0_TRIM_REFBUF_OFFSET_TRIM	0x42E60F00	Reference buffer trim control
DAC0_TRIM_REFBUF_SLOPE_OFFSET_TRIM	0x42E60F04	Reference buffer trim control
DAC0_TRIM_REFBUF_COMP_TRIM	0x42E60F08	Reference buffer trim control
DAC0_TRIM_OUTBUF_OFFSET_TRIM0	0x42E60F0C	Output buffer trim control
DAC0_TRIM_OUTBUF_OFFSET_TRIM1	0x42E60F10	Output buffer trim control. See DAC0_TRIM_OUTBUF_OFFSET_TRIM0 for the details of bit fields.
DAC0_TRIM_OUTBUF_SLOPE_OFFSET_TRIM0	0x42E60F14	Output buffer trim control
DAC0_TRIM_OUTBUF_SLOPE_OFFSET_TRIM1	0x42E60F18	Output buffer trim control. See DAC0_TRIM_OUTBUF_SLOPE_OFFSET_TRIM0 for the details of bit fields.
DAC0_TRIM_OUTBUF_COMP_TRIM0	0x42E60F1C	Output buffer trim control

Autonomous Analog registers

Register name	Address	Description
DAC0_TRIM_OUTBUF_COMP_TRIM1	0x42E60F20	Output buffer trim control. See DAC0_TRIM_OUTBUF_COMP_TRIM0 for the details of bit fields.
DAC0_TRIM_RMP_TRIM	0x42E60F24	Risk Mitigation bits
DAC1_SRAM0	0x42E70000	SRAM Waveform Table (only accessible if ACTRLR.STATUS.MODE=0). This is the starting address of a register bank containing 512 registers (DAC1_SRAM0 to DAC1_SRAM511). See DAC0_SRAM0 for the details of bit fields.
DAC1_STA_CTRL	0x42E70800	DAC control register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CTRL for the details of bit fields.
DAC1_STA_SAMPLE_TIME	0x42E70804	Sample control register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_SAMPLE_TIME for the details of bit fields.
DAC1_STA_STEP_VAL0	0x42E70808	step val register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_STEP_VAL0 for the details of bit fields.
DAC1_STA_STEP_VAL1	0x42E7080C	step val register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_STEP_VAL0 for the details of bit fields.
DAC1_STA_STEP_VAL2	0x42E70810	step val register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_STEP_VAL0 for the details of bit fields.
DAC1_STA_DEGLITCH_TIME	0x42E70818	deglitch time register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_DEGLITCH_TIME for the details of bit fields.
DAC1_STA_CHAN_CFG0	0x42E70820	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG1	0x42E70824	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG2	0x42E70828	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG3	0x42E7082C	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG4	0x42E70830	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
DAC1_STA_CHAN_CFG5	0x42E70834	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG6	0x42E70838	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG7	0x42E7083C	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG8	0x42E70840	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG9	0x42E70844	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG10	0x42E70848	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG11	0x42E7084C	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG12	0x42E70850	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG13	0x42E70854	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_CHAN_CFG14	0x42E70858	Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_CHAN_CFG0 for the details of bit fields.
DAC1_STA_FW_DAC_VAL	0x42E70860	Firmare Channel DAC Value (only accessible if ACTRLR.STATUS.MODE=0). See DAC0_STA_FW_DAC_VAL for the details of bit fields.
DAC1_STA_FW_DAC_VAL_NXT	0x42E70864	Firmware Channel DAC Value Next. See DAC0_STA_FW_DAC_VAL_NXT for the details of bit fields.
DAC1_STA_CHAN_STATUS_CFG0	0x42E70870	Channel status configuration register. See DAC0_STA_CHAN_STATUS_CFG0 for the details of bit fields.
DAC1_STA_CHAN_STATUS_CFG1	0x42E70874	Channel status configuration register. See DAC0_STA_CHAN_STATUS_CFG0 for the details of bit fields.
DAC1_STA_CHAN_STATUS_CFG2	0x42E70878	Channel status configuration register. See DAC0_STA_CHAN_STATUS_CFG0 for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
DAC1_STA_RANGE_STATUS	0x42E70880	Range status register. See DAC0_STA_RANGE_STATUS for the details of bit fields.
DAC1_TRIM_REFBUF_OFFSET_TRIM	0x42E70F00	Reference buffer trim control. See DAC0_TRIM_REFBUF_OFFSET_TRIM for the details of bit fields.
DAC1_TRIM_REFBUF_SLOPE_OFFSET_TRIM	0x42E70F04	Reference buffer trim control. See DAC0_TRIM_REFBUF_SLOPE_OFFSET_TRIM for the details of bit fields.
DAC1_TRIM_REFBUF_COMP_TRIM	0x42E70F08	Reference buffer trim control. See DAC0_TRIM_REFBUF_COMP_TRIM for the details of bit fields.
DAC1_TRIM_OUTBUF_OFFSET_TRIM0	0x42E70F0C	Output buffer trim control. See DAC0_TRIM_OUTBUF_OFFSET_TRIM0 for the details of bit fields.
DAC1_TRIM_OUTBUF_OFFSET_TRIM1	0x42E70F10	Output buffer trim control. See DAC0_TRIM_OUTBUF_OFFSET_TRIM0 for the details of bit fields.
DAC1_TRIM_OUTBUF_SLOPE_OFFSET_TRIM0	0x42E70F14	Output buffer trim control. See DAC0_TRIM_OUTBUF_SLOPE_OFFSET_TRIM0 for the details of bit fields.
DAC1_TRIM_OUTBUF_SLOPE_OFFSET_TRIM1	0x42E70F18	Output buffer trim control. See DAC0_TRIM_OUTBUF_SLOPE_OFFSET_TRIM0 for the details of bit fields.
DAC1_TRIM_OUTBUF_COMP_TRIM0	0x42E70F1C	Output buffer trim control. See DAC0_TRIM_OUTBUF_COMP_TRIM0 for the details of bit fields.
DAC1_TRIM_OUTBUF_COMP_TRIM1	0x42E70F20	Output buffer trim control. See DAC0_TRIM_OUTBUF_COMP_TRIM0 for the details of bit fields.
DAC1_TRIM_RMP_TRIM	0x42E70F24	Risk Mitigation bits. See DAC0_TRIM_RMP_TRIM for the details of bit fields.
SAR_SEQ_HS_DATA0	0x42E80100	SAR Sequencer High Speed Data (only accessible if ACTRLR.STATUS.MODE=0). This is the starting address of a register bank containing 32 registers (SAR_SEQ_HS_DATA0 to SAR_SEQ_HS_DATA31).
SAR_SEQ_LP_DATA0	0x42E80180	SAR Sequencer Low Power Data (only accessible if ACTRLR.STATUS.MODE=0). This is the starting address of a register bank containing 32 registers (SAR_SEQ_LP_DATA0 to SAR_SEQ_LP_DATA31).
SAR_STA_CTRL	0x42E80400	SAR Control register (only accessible if ACTRLR.STATUS.MODE=0)
SAR_STA_FIR_CFG0	0x42E80408	FIR Configuration register (only accessible if ACTRLR.STATUS.MODE=0)

Autonomous Analog registers

Register name	Address	Description
SAR_STA_FIR_CFG1	0x42E8040C	FIR Configuration register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_FIR_CFG0 for the details of bit fields.
SAR_STA_TR_SAMPLE_TIME	0x42E80418	SAR Trigger Sample Time (Risk Mitigation Only)
SAR_STA_SAMPLE_TIME0	0x42E80420	Sample control register (only accessible if ACTRLR.STATUS.MODE=0)
SAR_STA_SAMPLE_TIME1	0x42E80424	Sample control register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_SAMPLE_TIME0 for the details of bit fields.
SAR_STA_SAMPLE_TIME2	0x42E80428	Sample control register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_SAMPLE_TIME0 for the details of bit fields.
SAR_STA_SAMPLE_TIME3	0x42E8042C	Sample control register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_SAMPLE_TIME0 for the details of bit fields.
SAR_STA_GPIO_CHAN_CFG0	0x42E80430	High Speed GPIO Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0)
SAR_STA_GPIO_CHAN_CFG1	0x42E80434	High Speed GPIO Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_GPIO_CHAN_CFG0 for the details of bit fields.
SAR_STA_GPIO_CHAN_CFG2	0x42E80438	High Speed GPIO Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_GPIO_CHAN_CFG0 for the details of bit fields.
SAR_STA_GPIO_CHAN_CFG3	0x42E8043C	High Speed GPIO Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_GPIO_CHAN_CFG0 for the details of bit fields.
SAR_STA_GPIO_CHAN_CFG4	0x42E80440	High Speed GPIO Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_GPIO_CHAN_CFG0 for the details of bit fields.
SAR_STA_GPIO_CHAN_CFG5	0x42E80444	High Speed GPIO Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_GPIO_CHAN_CFG0 for the details of bit fields.
SAR_STA_GPIO_CHAN_CFG6	0x42E80448	High Speed GPIO Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_GPIO_CHAN_CFG0 for the details of bit fields.
SAR_STA_GPIO_CHAN_CFG7	0x42E8044C	High Speed GPIO Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_GPIO_CHAN_CFG0 for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
SAR_STA_MUX_CHAN_CFG0	0x42E80450	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0)
SAR_STA_MUX_CHAN_CFG1	0x42E80454	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG2	0x42E80458	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG3	0x42E8045C	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG4	0x42E80460	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG5	0x42E80464	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG6	0x42E80468	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG7	0x42E8046C	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
SAR_STA_MUX_CHAN_CFG8	0x42E80470	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG9	0x42E80474	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG10	0x42E80478	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG11	0x42E8047C	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG12	0x42E80480	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG13	0x42E80484	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_MUX_CHAN_CFG14	0x42E80488	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
SAR_STA_MUX_CHAN_CFG15	0x42E8048C	High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_MUX_CHAN_CFG0 for the details of bit fields.
SAR_STA_STATUS_CFG0	0x42E80490	Global range detect mode register (only accessible if ACTRLR.STATUS.MODE=0)
SAR_STA_STATUS_CFG1	0x42E80494	Global range detect mode register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_STATUS_CFG0 for the details of bit fields.
SAR_STA_STATUS_CFG2	0x42E80498	Global range detect mode register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_STATUS_CFG0 for the details of bit fields.
SAR_STA_STATUS_CFG3	0x42E8049C	Global range detect mode register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_STATUS_CFG0 for the details of bit fields.
SAR_STA_STATUS_RANGE_LOW0	0x42E804A0	Global range detect low value register (only accessible if ACTRLR.STATUS.MODE=0)
SAR_STA_STATUS_RANGE_LOW1	0x42E804A4	Global range detect low value register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_STATUS_RANGE_LOW0 for the details of bit fields.
SAR_STA_STATUS_RANGE_LOW2	0x42E804A8	Global range detect low value register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_STATUS_RANGE_LOW0 for the details of bit fields.
SAR_STA_STATUS_RANGE_LOW3	0x42E804AC	Global range detect low value register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_STATUS_RANGE_LOW0 for the details of bit fields.
SAR_STA_STATUS_RANGE_HIGH0	0x42E804B0	Global range detect high value register (only accessible if ACTRLR.STATUS.MODE=0)
SAR_STA_STATUS_RANGE_HIGH1	0x42E804B4	Global range detect high value register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_STATUS_RANGE_HIGH0 for the details of bit fields.
SAR_STA_STATUS_RANGE_HIGH2	0x42E804B8	Global range detect high value register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_STATUS_RANGE_HIGH0 for the details of bit fields.
SAR_STA_STATUS_RANGE_HIGH3	0x42E804BC	Global range detect high value register (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_STATUS_RANGE_HIGH0 for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
SAR_STA_GPIO_CHAN_RESULT0	0x42E804C0	High Speed GPIO Channel result register
SAR_STA_GPIO_CHAN_RESULT1	0x42E804C4	High Speed GPIO Channel result register. See SAR_STA_GPIO_CHAN_RESULT0 for the details of bit fields.
SAR_STA_GPIO_CHAN_RESULT2	0x42E804C8	High Speed GPIO Channel result register. See SAR_STA_GPIO_CHAN_RESULT0 for the details of bit fields.
SAR_STA_GPIO_CHAN_RESULT3	0x42E804CC	High Speed GPIO Channel result register. See SAR_STA_GPIO_CHAN_RESULT0 for the details of bit fields.
SAR_STA_GPIO_CHAN_RESULT4	0x42E804D0	High Speed GPIO Channel result register. See SAR_STA_GPIO_CHAN_RESULT0 for the details of bit fields.
SAR_STA_GPIO_CHAN_RESULT5	0x42E804D4	High Speed GPIO Channel result register. See SAR_STA_GPIO_CHAN_RESULT0 for the details of bit fields.
SAR_STA_GPIO_CHAN_RESULT6	0x42E804D8	High Speed GPIO Channel result register. See SAR_STA_GPIO_CHAN_RESULT0 for the details of bit fields.
SAR_STA_GPIO_CHAN_RESULT7	0x42E804DC	High Speed GPIO Channel result register. See SAR_STA_GPIO_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT0	0x42E804E0	High Speed / Low Power Muxed Channel result register
SAR_STA_MUX_CHAN_RESULT1	0x42E804E4	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT2	0x42E804E8	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT3	0x42E804EC	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT4	0x42E804F0	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT5	0x42E804F4	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT6	0x42E804F8	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
SAR_STA_MUX_CHAN_RESULT7	0x42E804FC	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT8	0x42E80500	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT9	0x42E80504	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT10	0x42E80508	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT11	0x42E8050C	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT12	0x42E80510	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT13	0x42E80514	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT14	0x42E80518	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_MUX_CHAN_RESULT15	0x42E8051C	High Speed / Low Power Muxed Channel result register. See SAR_STA_MUX_CHAN_RESULT0 for the details of bit fields.
SAR_STA_FIR_RESULT0	0x42E80520	FIR result register
SAR_STA_FIR_RESULT1	0x42E80524	FIR result register. See SAR_STA_FIR_RESULT0 for the details of bit fields.
SAR_STA_CHAN_RESULT_MASK	0x42E80530	Channel result mask (only accessible if ACTRLR.STATUS.MODE=0)
SAR_STA_FIR_RESULT_MASK	0x42E80534	FIR result mask (only accessible if ACTRLR.STATUS.MODE=0)
SAR_STA_CHAN_RESULT_UPDATED	0x42E80538	Channel result register status
SAR_STA_FIR_RESULT_UPDATED	0x42E8053C	FIR result register status
SAR_STA_STATUS	0x42E80540	SAR status register
SAR_STA_RANGE_STATUS	0x42E80544	Range status register
SAR_STA_CHAN_COEFF0	0x42E80550	Channel correction coefficients (only accessible if ACTRLR.STATUS.MODE=0)
SAR_STA_CHAN_COEFF1	0x42E80554	Channel correction coefficients (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_CHAN_COEFF0 for the details of bit fields.

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Register name	Address	Description
SAR_STA_CHAN_COEFF2	0x42E80558	Channel correction coefficients (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_CHAN_COEFF0 for the details of bit fields.
SAR_STA_CHAN_COEFF3	0x42E8055C	Channel correction coefficients (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_CHAN_COEFF0 for the details of bit fields.
SAR_STA_CHAN_COEFF4	0x42E80560	Channel correction coefficients (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_CHAN_COEFF0 for the details of bit fields.
SAR_STA_CHAN_COEFF5	0x42E80564	Channel correction coefficients (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_CHAN_COEFF0 for the details of bit fields.
SAR_STA_CHAN_COEFF6	0x42E80568	Channel correction coefficients (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_CHAN_COEFF0 for the details of bit fields.
SAR_STA_CHAN_COEFF7	0x42E8056C	Channel correction coefficients (only accessible if ACTRLR.STATUS.MODE=0). See SAR_STA_CHAN_COEFF0 for the details of bit fields.
SAR_FIR00_COEF	0x42E80600	Coefficient Value
SAR_FIR00_TAP	0x42E80604	Tap Value
SAR_FIR01_COEF	0x42E80608	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR01_TAP	0x42E8060C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR02_COEF	0x42E80610	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR02_TAP	0x42E80614	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR03_COEF	0x42E80618	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR03_TAP	0x42E8061C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR04_COEF	0x42E80620	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR04_TAP	0x42E80624	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR05_COEF	0x42E80628	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR05_TAP	0x42E8062C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR06_COEF	0x42E80630	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.

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Register name	Address	Description
SAR_FIR06_TAP	0x42E80634	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR07_COEF	0x42E80638	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR07_TAP	0x42E8063C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR08_COEF	0x42E80640	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR08_TAP	0x42E80644	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR09_COEF	0x42E80648	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR09_TAP	0x42E8064C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR010_COEF	0x42E80650	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR010_TAP	0x42E80654	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR011_COEF	0x42E80658	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR011_TAP	0x42E8065C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR012_COEF	0x42E80660	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR012_TAP	0x42E80664	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR013_COEF	0x42E80668	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR013_TAP	0x42E8066C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR014_COEF	0x42E80670	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR014_TAP	0x42E80674	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR015_COEF	0x42E80678	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR015_TAP	0x42E8067C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR016_COEF	0x42E80680	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR016_TAP	0x42E80684	Tap Value. See SAR_FIR00_TAP for the details of bit fields.

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Register name	Address	Description
SAR_FIR017_COEF	0x42E80688	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR017_TAP	0x42E8068C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR018_COEF	0x42E80690	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR018_TAP	0x42E80694	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR019_COEF	0x42E80698	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR019_TAP	0x42E8069C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR020_COEF	0x42E806A0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR020_TAP	0x42E806A4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR021_COEF	0x42E806A8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR021_TAP	0x42E806AC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR022_COEF	0x42E806B0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR022_TAP	0x42E806B4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR023_COEF	0x42E806B8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR023_TAP	0x42E806BC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR024_COEF	0x42E806C0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR024_TAP	0x42E806C4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR025_COEF	0x42E806C8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR025_TAP	0x42E806CC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR026_COEF	0x42E806D0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR026_TAP	0x42E806D4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR027_COEF	0x42E806D8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.

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Register name	Address	Description
SAR_FIR027_TAP	0x42E806DC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR028_COEF	0x42E806E0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR028_TAP	0x42E806E4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR029_COEF	0x42E806E8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR029_TAP	0x42E806EC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR030_COEF	0x42E806F0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR030_TAP	0x42E806F4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR031_COEF	0x42E806F8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR031_TAP	0x42E806FC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR032_COEF	0x42E80700	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR032_TAP	0x42E80704	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR033_COEF	0x42E80708	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR033_TAP	0x42E8070C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR034_COEF	0x42E80710	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR034_TAP	0x42E80714	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR035_COEF	0x42E80718	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR035_TAP	0x42E8071C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR036_COEF	0x42E80720	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR036_TAP	0x42E80724	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR037_COEF	0x42E80728	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR037_TAP	0x42E8072C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
SAR_FIR038_COEF	0x42E80730	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR038_TAP	0x42E80734	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR039_COEF	0x42E80738	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR039_TAP	0x42E8073C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR040_COEF	0x42E80740	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR040_TAP	0x42E80744	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR041_COEF	0x42E80748	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR041_TAP	0x42E8074C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR042_COEF	0x42E80750	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR042_TAP	0x42E80754	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR043_COEF	0x42E80758	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR043_TAP	0x42E8075C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR044_COEF	0x42E80760	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR044_TAP	0x42E80764	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR045_COEF	0x42E80768	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR045_TAP	0x42E8076C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR046_COEF	0x42E80770	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR046_TAP	0x42E80774	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR047_COEF	0x42E80778	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR047_TAP	0x42E8077C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR048_COEF	0x42E80780	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
SAR_FIR048_TAP	0x42E80784	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR049_COEF	0x42E80788	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR049_TAP	0x42E8078C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR050_COEF	0x42E80790	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR050_TAP	0x42E80794	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR051_COEF	0x42E80798	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR051_TAP	0x42E8079C	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR052_COEF	0x42E807A0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR052_TAP	0x42E807A4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR053_COEF	0x42E807A8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR053_TAP	0x42E807AC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR054_COEF	0x42E807B0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR054_TAP	0x42E807B4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR055_COEF	0x42E807B8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR055_TAP	0x42E807BC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR056_COEF	0x42E807C0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR056_TAP	0x42E807C4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR057_COEF	0x42E807C8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR057_TAP	0x42E807CC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR058_COEF	0x42E807D0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR058_TAP	0x42E807D4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.

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Register name	Address	Description
SAR_FIR059_COEF	0x42E807D8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR059_TAP	0x42E807DC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR060_COEF	0x42E807E0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR060_TAP	0x42E807E4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR061_COEF	0x42E807E8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR061_TAP	0x42E807EC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR062_COEF	0x42E807F0	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR062_TAP	0x42E807F4	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR063_COEF	0x42E807F8	Coefficient Value. See SAR_FIR00_COEF for the details of bit fields.
SAR_FIR063_TAP	0x42E807FC	Tap Value. See SAR_FIR00_TAP for the details of bit fields.
SAR_FIR10_COEF	0x42E80800	Coefficient Value
SAR_FIR10_TAP	0x42E80804	Tap Value
SAR_FIR11_COEF	0x42E80808	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR11_TAP	0x42E8080C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR12_COEF	0x42E80810	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR12_TAP	0x42E80814	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR13_COEF	0x42E80818	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR13_TAP	0x42E8081C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR14_COEF	0x42E80820	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR14_TAP	0x42E80824	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR15_COEF	0x42E80828	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR15_TAP	0x42E8082C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.

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Register name	Address	Description
SAR_FIR16_COEF	0x42E80830	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR16_TAP	0x42E80834	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR17_COEF	0x42E80838	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR17_TAP	0x42E8083C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR18_COEF	0x42E80840	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR18_TAP	0x42E80844	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR19_COEF	0x42E80848	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR19_TAP	0x42E8084C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR110_COEF	0x42E80850	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR110_TAP	0x42E80854	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR111_COEF	0x42E80858	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR111_TAP	0x42E8085C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR112_COEF	0x42E80860	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR112_TAP	0x42E80864	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR113_COEF	0x42E80868	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR113_TAP	0x42E8086C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR114_COEF	0x42E80870	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR114_TAP	0x42E80874	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR115_COEF	0x42E80878	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR115_TAP	0x42E8087C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR116_COEF	0x42E80880	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.

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Register name	Address	Description
SAR_FIR116_TAP	0x42E80884	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR117_COEF	0x42E80888	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR117_TAP	0x42E8088C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR118_COEF	0x42E80890	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR118_TAP	0x42E80894	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR119_COEF	0x42E80898	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR119_TAP	0x42E8089C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR120_COEF	0x42E808A0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR120_TAP	0x42E808A4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR121_COEF	0x42E808A8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR121_TAP	0x42E808AC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR122_COEF	0x42E808B0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR122_TAP	0x42E808B4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR123_COEF	0x42E808B8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR123_TAP	0x42E808BC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR124_COEF	0x42E808C0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR124_TAP	0x42E808C4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR125_COEF	0x42E808C8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR125_TAP	0x42E808CC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR126_COEF	0x42E808D0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR126_TAP	0x42E808D4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.

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Register name	Address	Description
SAR_FIR127_COEF	0x42E808D8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR127_TAP	0x42E808DC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR128_COEF	0x42E808E0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR128_TAP	0x42E808E4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR129_COEF	0x42E808E8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR129_TAP	0x42E808EC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR130_COEF	0x42E808F0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR130_TAP	0x42E808F4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR131_COEF	0x42E808F8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR131_TAP	0x42E808FC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR132_COEF	0x42E80900	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR132_TAP	0x42E80904	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR133_COEF	0x42E80908	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR133_TAP	0x42E8090C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR134_COEF	0x42E80910	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR134_TAP	0x42E80914	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR135_COEF	0x42E80918	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR135_TAP	0x42E8091C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR136_COEF	0x42E80920	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR136_TAP	0x42E80924	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR137_COEF	0x42E80928	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.

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Register name	Address	Description
SAR_FIR137_TAP	0x42E8092C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR138_COEF	0x42E80930	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR138_TAP	0x42E80934	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR139_COEF	0x42E80938	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR139_TAP	0x42E8093C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR140_COEF	0x42E80940	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR140_TAP	0x42E80944	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR141_COEF	0x42E80948	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR141_TAP	0x42E8094C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR142_COEF	0x42E80950	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR142_TAP	0x42E80954	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR143_COEF	0x42E80958	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR143_TAP	0x42E8095C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR144_COEF	0x42E80960	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR144_TAP	0x42E80964	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR145_COEF	0x42E80968	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR145_TAP	0x42E8096C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR146_COEF	0x42E80970	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR146_TAP	0x42E80974	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR147_COEF	0x42E80978	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR147_TAP	0x42E8097C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.

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Register name	Address	Description
SAR_FIR148_COEF	0x42E80980	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR148_TAP	0x42E80984	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR149_COEF	0x42E80988	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR149_TAP	0x42E8098C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR150_COEF	0x42E80990	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR150_TAP	0x42E80994	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR151_COEF	0x42E80998	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR151_TAP	0x42E8099C	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR152_COEF	0x42E809A0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR152_TAP	0x42E809A4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR153_COEF	0x42E809A8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR153_TAP	0x42E809AC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR154_COEF	0x42E809B0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR154_TAP	0x42E809B4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR155_COEF	0x42E809B8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR155_TAP	0x42E809BC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR156_COEF	0x42E809C0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR156_TAP	0x42E809C4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR157_COEF	0x42E809C8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR157_TAP	0x42E809CC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR158_COEF	0x42E809D0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.

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Register name	Address	Description
SAR_FIR158_TAP	0x42E809D4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR159_COEF	0x42E809D8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR159_TAP	0x42E809DC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR160_COEF	0x42E809E0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR160_TAP	0x42E809E4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR161_COEF	0x42E809E8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR161_TAP	0x42E809EC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR162_COEF	0x42E809F0	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR162_TAP	0x42E809F4	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_FIR163_COEF	0x42E809F8	Coefficient Value. See SAR_FIR10_COEF for the details of bit fields.
SAR_FIR163_TAP	0x42E809FC	Tap Value. See SAR_FIR10_TAP for the details of bit fields.
SAR_HS_CAL_MEM_CALCTRL	0x42E80C14	SAR HS Core Calibration Control Register
SAR_HS_CAL_MEM_CONVCTRL	0x42E80C1C	SAR HS Core Conversion Control Register
SAR_HS_CAL_MEM_ADFTMUX	0x42E80C20	SAR HS Core Analog DFT Multiplexer Control Register
SAR_HS_CAL_MEM_CALMEM00	0x42E80C40	SAR HS Core Channel Calibration Values
SAR_HS_CAL_MEM_CALMEM01	0x42E80C44	SAR HS Core Channel Calibration Values. See SAR_HS_CAL_MEM_CALMEM00 for the details of bit fields.
SAR_HS_CAL_MEM_CALMEM02	0x42E80C48	SAR HS Core Channel Calibration Values. See SAR_HS_CAL_MEM_CALMEM00 for the details of bit fields.
SAR_HS_CAL_MEM_CALMEM03	0x42E80C4C	SAR HS Core Channel Calibration Values. See SAR_HS_CAL_MEM_CALMEM00 for the details of bit fields.
SAR_HS_CAL_MEM_CALMEM04	0x42E80C50	SAR HS Core Channel Calibration Values. See SAR_HS_CAL_MEM_CALMEM00 for the details of bit fields.
SAR_HS_CAL_MEM_CALMEM05	0x42E80C54	SAR HS Core Channel Calibration Values. See SAR_HS_CAL_MEM_CALMEM00 for the details of bit fields.

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Register name	Address	Description
SAR_HS_CAL_MEM_CALMEM06	0x42E80C58	SAR HS Core Channel Calibration Values. See SAR_HS_CAL_MEM_CALMEM00 for the details of bit fields.
SAR_HS_CAL_MEM_CALMEM07	0x42E80C5C	SAR HS Core Channel Calibration Values. See SAR_HS_CAL_MEM_CALMEM00 for the details of bit fields.
SAR_HS_CAL_MEM_CALMEM08	0x42E80C60	SAR HS Core Channel Calibration Values. See SAR_HS_CAL_MEM_CALMEM00 for the details of bit fields.
SAR_HS_CAL_MEM_CALMEM09	0x42E80C64	SAR HS Core Channel Calibration Values. See SAR_HS_CAL_MEM_CALMEM00 for the details of bit fields.
SAR_LP_CAL_MEM_CALCTRL	0x42E80C94	SAR LP Core Calibration Control Register
SAR_LP_CAL_MEM_CONVCTRL	0x42E80C9C	SAR LP Core Conversion Control Register
SAR_LP_CAL_MEM_ADFTMUX	0x42E80CA0	SAR LP Core Analog DFT Multiplexer Control Register
SAR_LP_CAL_MEM_CALMEM0	0x42E80CC0	SAR LP Core Channel Calibration Values
SAR_TRIM_BUF0_OFFSET_TRIM	0x42E80F00	Buffer zero trim control
SAR_TRIM_BUF0_SLOPE_OFFSET_TRIM	0x42E80F04	Buffer zero trim control
SAR_TRIM_BUF0_COMP_TRIM	0x42E80F08	Buffer zero trim control
SAR_TRIM_BUF1_OFFSET_TRIM	0x42E80F0C	Buffer one trim control
SAR_TRIM_BUF1_SLOPE_OFFSET_TRIM	0x42E80F10	Buffer one trim control
SAR_TRIM_BUF1_COMP_TRIM	0x42E80F14	Buffer one trim control
SAR_TRIM_RMP_TRIM	0x42E80F18	Risk Mitigation bits
ACTRLR_CTRL	0x42ED0000	control register
ACTRLR_CMD_RUN	0x42ED0004	run command register
ACTRLR_CMD_STATE	0x42ED0008	state override register
ACTRLR_FW_TR0	0x42ED0010	firmware trigger
ACTRLR_FW_TR1	0x42ED0014	firmware trigger. See ACTRLR_FW_TR0 for the details of bit fields.
ACTRLR_FW_TR2	0x42ED0018	firmware trigger. See ACTRLR_FW_TR0 for the details of bit fields.
ACTRLR_FW_TR3	0x42ED001C	firmware trigger. See ACTRLR_FW_TR0 for the details of bit fields.
ACTRLR_STATUS	0x42ED0020	status register
ACTRLR_CFG	0x42ED0024	config register (only accessible if CTRL.EN=0)
ACTRLR_DEBUG_PAUSE	0x42ED0030	pause debug register
ACTRLR_DEBUG_SINGLE_STEP	0x42ED0034	single step debug register
ACTRLR_PWR_STATUS	0x42ED0038	power status register
ACTRLR_CNTR_STATUS0	0x42ED0100	Loop/Interval counter status register

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Register name	Address	Description
ACTRLR_CNTR_STATUS1	0x42ED0104	Loop/Interval counter status register. See ACTRLR_CNTR_STATUS0 for the details of bit fields.
ACTRLR_CNTR_STATUS2	0x42ED0108	Loop/Interval counter status register. See ACTRLR_CNTR_STATUS0 for the details of bit fields.
ACTRLR_CNTR_STATUS3	0x42ED010C	Loop/Interval counter status register. See ACTRLR_CNTR_STATUS0 for the details of bit fields.
ACTRLR_TTCFG0_TT_CFG0	0x42ED0800	AC Table Configuration 0
ACTRLR_TTCFG0_TT_CFG1	0x42ED0804	AC Table Configuration 1
ACTRLR_TTCFG0_TT_CFG2	0x42ED0808	AC Table Configuration 2
ACTRLR_TTCFG0_TT_CFG3	0x42ED080C	AC Table Configuration 3
ACTRLR_TTCFG0_TT_CFG4	0x42ED0810	AC Table Configuration 4
ACTRLR_TTCFG1_TT_CFG0	0x42ED0820	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG1_TT_CFG1	0x42ED0824	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG1_TT_CFG2	0x42ED0828	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG1_TT_CFG3	0x42ED082C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG1_TT_CFG4	0x42ED0830	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG2_TT_CFG0	0x42ED0840	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG2_TT_CFG1	0x42ED0844	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG2_TT_CFG2	0x42ED0848	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG2_TT_CFG3	0x42ED084C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG2_TT_CFG4	0x42ED0850	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG3_TT_CFG0	0x42ED0860	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG3_TT_CFG1	0x42ED0864	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG3_TT_CFG2	0x42ED0868	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG3_TT_CFG3	0x42ED086C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG3_TT_CFG4	0x42ED0870	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG4_TT_CFG0	0x42ED0880	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG4_TT_CFG1	0x42ED0884	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG4_TT_CFG2	0x42ED0888	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG4_TT_CFG3	0x42ED088C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG4_TT_CFG4	0x42ED0890	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG5_TT_CFG0	0x42ED08A0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG5_TT_CFG1	0x42ED08A4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG5_TT_CFG2	0x42ED08A8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG5_TT_CFG3	0x42ED08AC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG5_TT_CFG4	0x42ED08B0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG6_TT_CFG0	0x42ED08C0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG6_TT_CFG1	0x42ED08C4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG6_TT_CFG2	0x42ED08C8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG6_TT_CFG3	0x42ED08CC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG6_TT_CFG4	0x42ED08D0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG7_TT_CFG0	0x42ED08E0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG7_TT_CFG1	0x42ED08E4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG7_TT_CFG2	0x42ED08E8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG7_TT_CFG3	0x42ED08EC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG7_TT_CFG4	0x42ED08F0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG8_TT_CFG0	0x42ED0900	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG8_TT_CFG1	0x42ED0904	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG8_TT_CFG2	0x42ED0908	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG8_TT_CFG3	0x42ED090C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG8_TT_CFG4	0x42ED0910	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG9_TT_CFG0	0x42ED0920	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG9_TT_CFG1	0x42ED0924	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG9_TT_CFG2	0x42ED0928	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG9_TT_CFG3	0x42ED092C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG9_TT_CFG4	0x42ED0930	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG10_TT_CFG0	0x42ED0940	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG10_TT_CFG1	0x42ED0944	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG10_TT_CFG2	0x42ED0948	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG10_TT_CFG3	0x42ED094C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG10_TT_CFG4	0x42ED0950	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG11_TT_CFG0	0x42ED0960	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG11_TT_CFG1	0x42ED0964	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG11_TT_CFG2	0x42ED0968	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG11_TT_CFG3	0x42ED096C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG11_TT_CFG4	0x42ED0970	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG12_TT_CFG0	0x42ED0980	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG12_TT_CFG1	0x42ED0984	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG12_TT_CFG2	0x42ED0988	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG12_TT_CFG3	0x42ED098C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG12_TT_CFG4	0x42ED0990	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG13_TT_CFG0	0x42ED09A0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG13_TT_CFG1	0x42ED09A4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG13_TT_CFG2	0x42ED09A8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG13_TT_CFG3	0x42ED09AC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG13_TT_CFG4	0x42ED09B0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG14_TT_CFG0	0x42ED09C0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG14_TT_CFG1	0x42ED09C4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG14_TT_CFG2	0x42ED09C8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG14_TT_CFG3	0x42ED09CC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG14_TT_CFG4	0x42ED09D0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG15_TT_CFG0	0x42ED09E0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG15_TT_CFG1	0x42ED09E4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG15_TT_CFG2	0x42ED09E8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG15_TT_CFG3	0x42ED09EC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG15_TT_CFG4	0x42ED09F0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG16_TT_CFG0	0x42ED0A00	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG16_TT_CFG1	0x42ED0A04	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG16_TT_CFG2	0x42ED0A08	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG16_TT_CFG3	0x42ED0A0C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG16_TT_CFG4	0x42ED0A10	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG17_TT_CFG0	0x42ED0A20	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG17_TT_CFG1	0x42ED0A24	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG17_TT_CFG2	0x42ED0A28	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG17_TT_CFG3	0x42ED0A2C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG17_TT_CFG4	0x42ED0A30	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG18_TT_CFG0	0x42ED0A40	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG18_TT_CFG1	0x42ED0A44	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG18_TT_CFG2	0x42ED0A48	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG18_TT_CFG3	0x42ED0A4C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG18_TT_CFG4	0x42ED0A50	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG19_TT_CFG0	0x42ED0A60	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG19_TT_CFG1	0x42ED0A64	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG19_TT_CFG2	0x42ED0A68	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG19_TT_CFG3	0x42ED0A6C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG19_TT_CFG4	0x42ED0A70	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG20_TT_CFG0	0x42ED0A80	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG20_TT_CFG1	0x42ED0A84	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG20_TT_CFG2	0x42ED0A88	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG20_TT_CFG3	0x42ED0A8C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG20_TT_CFG4	0x42ED0A90	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG21_TT_CFG0	0x42ED0AA0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG21_TT_CFG1	0x42ED0AA4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG21_TT_CFG2	0x42ED0AA8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG21_TT_CFG3	0x42ED0AAC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG21_TT_CFG4	0x42ED0AB0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG22_TT_CFG0	0x42ED0AC0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG22_TT_CFG1	0x42ED0AC4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG22_TT_CFG2	0x42ED0AC8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG22_TT_CFG3	0x42ED0ACC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG22_TT_CFG4	0x42ED0AD0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG23_TT_CFG0	0x42ED0AE0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG23_TT_CFG1	0x42ED0AE4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG23_TT_CFG2	0x42ED0AE8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG23_TT_CFG3	0x42ED0AEC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG23_TT_CFG4	0x42ED0AF0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG24_TT_CFG0	0x42ED0B00	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG24_TT_CFG1	0x42ED0B04	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG24_TT_CFG2	0x42ED0B08	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG24_TT_CFG3	0x42ED0B0C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG24_TT_CFG4	0x42ED0B10	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG25_TT_CFG0	0x42ED0B20	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG25_TT_CFG1	0x42ED0B24	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG25_TT_CFG2	0x42ED0B28	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG25_TT_CFG3	0x42ED0B2C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG25_TT_CFG4	0x42ED0B30	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG26_TT_CFG0	0x42ED0B40	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG26_TT_CFG1	0x42ED0B44	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG26_TT_CFG2	0x42ED0B48	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG26_TT_CFG3	0x42ED0B4C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG26_TT_CFG4	0x42ED0B50	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG27_TT_CFG0	0x42ED0B60	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG27_TT_CFG1	0x42ED0B64	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG27_TT_CFG2	0x42ED0B68	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG27_TT_CFG3	0x42ED0B6C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG27_TT_CFG4	0x42ED0B70	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG28_TT_CFG0	0x42ED0B80	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG28_TT_CFG1	0x42ED0B84	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG28_TT_CFG2	0x42ED0B88	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG28_TT_CFG3	0x42ED0B8C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG28_TT_CFG4	0x42ED0B90	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG29_TT_CFG0	0x42ED0BA0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG29_TT_CFG1	0x42ED0BA4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG29_TT_CFG2	0x42ED0BA8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG29_TT_CFG3	0x42ED0BAC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG29_TT_CFG4	0x42ED0BB0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG30_TT_CFG0	0x42ED0BC0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG30_TT_CFG1	0x42ED0BC4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG30_TT_CFG2	0x42ED0BC8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG30_TT_CFG3	0x42ED0BCC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG30_TT_CFG4	0x42ED0BD0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG31_TT_CFG0	0x42ED0BE0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG31_TT_CFG1	0x42ED0BE4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG31_TT_CFG2	0x42ED0BE8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG31_TT_CFG3	0x42ED0BEC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG31_TT_CFG4	0x42ED0BF0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG32_TT_CFG0	0x42ED0C00	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG32_TT_CFG1	0x42ED0C04	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG32_TT_CFG2	0x42ED0C08	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG32_TT_CFG3	0x42ED0C0C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG32_TT_CFG4	0x42ED0C10	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG33_TT_CFG0	0x42ED0C20	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG33_TT_CFG1	0x42ED0C24	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG33_TT_CFG2	0x42ED0C28	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG33_TT_CFG3	0x42ED0C2C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG33_TT_CFG4	0x42ED0C30	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG34_TT_CFG0	0x42ED0C40	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG34_TT_CFG1	0x42ED0C44	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG34_TT_CFG2	0x42ED0C48	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG34_TT_CFG3	0x42ED0C4C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG34_TT_CFG4	0x42ED0C50	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG35_TT_CFG0	0x42ED0C60	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG35_TT_CFG1	0x42ED0C64	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG35_TT_CFG2	0x42ED0C68	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG35_TT_CFG3	0x42ED0C6C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG35_TT_CFG4	0x42ED0C70	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG36_TT_CFG0	0x42ED0C80	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG36_TT_CFG1	0x42ED0C84	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG36_TT_CFG2	0x42ED0C88	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG36_TT_CFG3	0x42ED0C8C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG36_TT_CFG4	0x42ED0C90	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG37_TT_CFG0	0x42ED0CA0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG37_TT_CFG1	0x42ED0CA4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG37_TT_CFG2	0x42ED0CA8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG37_TT_CFG3	0x42ED0CAC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG37_TT_CFG4	0x42ED0CB0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG38_TT_CFG0	0x42ED0CC0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG38_TT_CFG1	0x42ED0CC4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG38_TT_CFG2	0x42ED0CC8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG38_TT_CFG3	0x42ED0CCC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG38_TT_CFG4	0x42ED0CD0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG39_TT_CFG0	0x42ED0CE0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG39_TT_CFG1	0x42ED0CE4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG39_TT_CFG2	0x42ED0CE8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG39_TT_CFG3	0x42ED0CEC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG39_TT_CFG4	0x42ED0CF0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG40_TT_CFG0	0x42ED0D00	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG40_TT_CFG1	0x42ED0D04	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG40_TT_CFG2	0x42ED0D08	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG40_TT_CFG3	0x42ED0D0C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG40_TT_CFG4	0x42ED0D10	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG41_TT_CFG0	0x42ED0D20	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG41_TT_CFG1	0x42ED0D24	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG41_TT_CFG2	0x42ED0D28	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG41_TT_CFG3	0x42ED0D2C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG41_TT_CFG4	0x42ED0D30	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG42_TT_CFG0	0x42ED0D40	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG42_TT_CFG1	0x42ED0D44	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG42_TT_CFG2	0x42ED0D48	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG42_TT_CFG3	0x42ED0D4C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG42_TT_CFG4	0x42ED0D50	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG43_TT_CFG0	0x42ED0D60	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG43_TT_CFG1	0x42ED0D64	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG43_TT_CFG2	0x42ED0D68	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG43_TT_CFG3	0x42ED0D6C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG43_TT_CFG4	0x42ED0D70	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG44_TT_CFG0	0x42ED0D80	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG44_TT_CFG1	0x42ED0D84	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG44_TT_CFG2	0x42ED0D88	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG44_TT_CFG3	0x42ED0D8C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG44_TT_CFG4	0x42ED0D90	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG45_TT_CFG0	0x42ED0DA0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG45_TT_CFG1	0x42ED0DA4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG45_TT_CFG2	0x42ED0DA8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG45_TT_CFG3	0x42ED0DAC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG45_TT_CFG4	0x42ED0DB0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG46_TT_CFG0	0x42ED0DC0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG46_TT_CFG1	0x42ED0DC4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG46_TT_CFG2	0x42ED0DC8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG46_TT_CFG3	0x42ED0DCC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG46_TT_CFG4	0x42ED0DD0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG47_TT_CFG0	0x42ED0DE0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG47_TT_CFG1	0x42ED0DE4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG47_TT_CFG2	0x42ED0DE8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG47_TT_CFG3	0x42ED0DEC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG47_TT_CFG4	0x42ED0DF0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG48_TT_CFG0	0x42ED0E00	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG48_TT_CFG1	0x42ED0E04	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG48_TT_CFG2	0x42ED0E08	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG48_TT_CFG3	0x42ED0E0C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG48_TT_CFG4	0x42ED0E10	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG49_TT_CFG0	0x42ED0E20	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG49_TT_CFG1	0x42ED0E24	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG49_TT_CFG2	0x42ED0E28	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG49_TT_CFG3	0x42ED0E2C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG49_TT_CFG4	0x42ED0E30	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG50_TT_CFG0	0x42ED0E40	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG50_TT_CFG1	0x42ED0E44	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG50_TT_CFG2	0x42ED0E48	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG50_TT_CFG3	0x42ED0E4C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG50_TT_CFG4	0x42ED0E50	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG51_TT_CFG0	0x42ED0E60	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG51_TT_CFG1	0x42ED0E64	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG51_TT_CFG2	0x42ED0E68	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG51_TT_CFG3	0x42ED0E6C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG51_TT_CFG4	0x42ED0E70	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG52_TT_CFG0	0x42ED0E80	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG52_TT_CFG1	0x42ED0E84	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG52_TT_CFG2	0x42ED0E88	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG52_TT_CFG3	0x42ED0E8C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG52_TT_CFG4	0x42ED0E90	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG53_TT_CFG0	0x42ED0EA0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG53_TT_CFG1	0x42ED0EA4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG53_TT_CFG2	0x42ED0EA8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG53_TT_CFG3	0x42ED0EAC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG53_TT_CFG4	0x42ED0EB0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG54_TT_CFG0	0x42ED0EC0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG54_TT_CFG1	0x42ED0EC4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG54_TT_CFG2	0x42ED0EC8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG54_TT_CFG3	0x42ED0ECC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG54_TT_CFG4	0x42ED0ED0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG55_TT_CFG0	0x42ED0EE0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG55_TT_CFG1	0x42ED0EE4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG55_TT_CFG2	0x42ED0EE8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG55_TT_CFG3	0x42ED0EEC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG55_TT_CFG4	0x42ED0EF0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG56_TT_CFG0	0x42ED0F00	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG56_TT_CFG1	0x42ED0F04	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG56_TT_CFG2	0x42ED0F08	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG56_TT_CFG3	0x42ED0F0C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG56_TT_CFG4	0x42ED0F10	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG57_TT_CFG0	0x42ED0F20	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG57_TT_CFG1	0x42ED0F24	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG57_TT_CFG2	0x42ED0F28	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG57_TT_CFG3	0x42ED0F2C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG57_TT_CFG4	0x42ED0F30	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG58_TT_CFG0	0x42ED0F40	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG58_TT_CFG1	0x42ED0F44	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG58_TT_CFG2	0x42ED0F48	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG58_TT_CFG3	0x42ED0F4C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG58_TT_CFG4	0x42ED0F50	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG59_TT_CFG0	0x42ED0F60	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG59_TT_CFG1	0x42ED0F64	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG59_TT_CFG2	0x42ED0F68	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG59_TT_CFG3	0x42ED0F6C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG59_TT_CFG4	0x42ED0F70	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG60_TT_CFG0	0x42ED0F80	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG60_TT_CFG1	0x42ED0F84	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG60_TT_CFG2	0x42ED0F88	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG60_TT_CFG3	0x42ED0F8C	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG60_TT_CFG4	0x42ED0F90	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG61_TT_CFG0	0x42ED0FA0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG61_TT_CFG1	0x42ED0FA4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG61_TT_CFG2	0x42ED0FA8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG61_TT_CFG3	0x42ED0FAC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG61_TT_CFG4	0x42ED0FB0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG62_TT_CFG0	0x42ED0FC0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG62_TT_CFG1	0x42ED0FC4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG62_TT_CFG2	0x42ED0FC8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG62_TT_CFG3	0x42ED0FCC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.

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Register name	Address	Description
ACTRLR_TTCFG62_TT_CFG4	0x42ED0FD0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
ACTRLR_TTCFG63_TT_CFG0	0x42ED0FE0	AC Table Configuration 0. See ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
ACTRLR_TTCFG63_TT_CFG1	0x42ED0FE4	AC Table Configuration 1. See ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
ACTRLR_TTCFG63_TT_CFG2	0x42ED0FE8	AC Table Configuration 2. See ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
ACTRLR_TTCFG63_TT_CFG3	0x42ED0FEC	AC Table Configuration 3. See ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
ACTRLR_TTCFG63_TT_CFG4	0x42ED0FF0	AC Table Configuration 4. See ACTRLR_TTCFG0_TT_CFG4 for the details of bit fields.
INFRA_CLOCK_PTC_LP_DIV	0x42EE0004	Low Power Clock divider for PTC (only accessible if ACTRLR.STATUS.MODE=0)
INFRA_CLOCK_DAC_LP_DIV0	0x42EE0008	Low Power Clock divider for DAC (only accessible if ACTRLR.STATUS.MODE=0)
INFRA_CLOCK_DAC_LP_DIV1	0x42EE000C	Low Power Clock divider for DAC (only accessible if ACTRLR.STATUS.MODE=0). See INFRA_CLOCK_DAC_LP_DIV0 for the details of bit fields.
INFRA_CLOCK_PRIO_HS_DIV	0x42EE0014	Clock enable for IP priority enabler (only accessible if ACTRLR.STATUS.MODE=0)
INFRA_PRIO_CFG0	0x42EE0020	Sub IP Block IP priority enabler configuration (only accessible if ACTRLR.STATUS.MODE=0)
INFRA_PRIO_CFG1	0x42EE0024	Sub IP Block IP priority enabler configuration (only accessible if ACTRLR.STATUS.MODE=0). See INFRA_PRIO_CFG0 for the details of bit fields.
INFRA_PRIO_CFG2	0x42EE0028	Sub IP Block IP priority enabler configuration (only accessible if ACTRLR.STATUS.MODE=0). See INFRA_PRIO_CFG0 for the details of bit fields.
INFRA_PRIO_CFG3	0x42EE002C	Sub IP Block IP priority enabler configuration (only accessible if ACTRLR.STATUS.MODE=0). See INFRA_PRIO_CFG0 for the details of bit fields.
INFRA_LPOSC_CFG	0x42EE0100	Low Power Oscillator configuration register
INFRA_LPOSC_TRIM	0x42EE01F0	LPOSC Trim Register
INFRA_AREF_CTRL	0x42EE0200	AREF control
INFRA_AREF_VREF_TRIM0	0x42EE02D0	VREF Trim bits
INFRA_AREF_VREF_TRIM1	0x42EE02D4	VREF Trim bits
INFRA_AREF_VREF_TRIM2	0x42EE02D8	VREF Trim bits
INFRA_AREF_VREF_TRIM3	0x42EE02DC	VREF Trim bits
INFRA_AREF_IZTAT_TRIM0	0x42EE02E0	IZTAT Trim bits
INFRA_AREF_IPTAT_TRIM0	0x42EE02E4	IPTAT Trim bits

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Register name	Address	Description
INFRA_AREF_IPTAT_TRIM1	0x42EE02E8	IPTAT Trim bits
INFRA_AREF_ICTAT_TRIM0	0x42EE02EC	ICTAT Trim bits
INFRA_AREF_ICTAT_TRIM1	0x42EE02F0	ICTAT Trim bits
INFRA_AREF_ICTAT_TRIM2	0x42EE02F4	ICTAT Trim bits
INFRA_PRB_VREF_CTRL0	0x42EE0300	PRB VREF Control
INFRA_PRB_VREF_CTRL1	0x42EE0304	PRB VREF Control. See INFRA_PRB_VREF_CTRL0 for the details of bit fields.
INFRA_TIMER_CTRL	0x42EE0400	Timer trigger control register
INFRA_TIMER_CFG	0x42EE0404	Timer trigger configuration register
INFRA_TIMER_PERIOD	0x42EE0408	Timer trigger period register
LPPASS_MMIO_INTR_CAUSE	0x42EF0000	Interrupt cause register
LPPASS_MMIO_FIFO_INTR_CAUSE	0x42EF0004	FIFO Interrupt cause register
LPPASS_MMIO_TR_OUT0	0x42EF0010	Trigger out select register
LPPASS_MMIO_TR_OUT1	0x42EF0014	Trigger out select register. See LPPASS_MMIO_TR_OUT0 for the details of bit fields.
LPPASS_MMIO_TR_OUT2	0x42EF0018	Trigger out select register. See LPPASS_MMIO_TR_OUT0 for the details of bit fields.
LPPASS_MMIO_TR_OUT3	0x42EF001C	Trigger out select register. See LPPASS_MMIO_TR_OUT0 for the details of bit fields.
LPPASS_MMIO_TR_OUT4	0x42EF0020	Trigger out select register. See LPPASS_MMIO_TR_OUT0 for the details of bit fields.
LPPASS_MMIO_TR_OUT5	0x42EF0024	Trigger out select register. See LPPASS_MMIO_TR_OUT0 for the details of bit fields.
LPPASS_MMIO_TR_OUT6	0x42EF0028	Trigger out select register. See LPPASS_MMIO_TR_OUT0 for the details of bit fields.
LPPASS_MMIO_TR_OUT7	0x42EF002C	Trigger out select register. See LPPASS_MMIO_TR_OUT0 for the details of bit fields.
LPPASS_MMIO_INTR	0x42EF0040	Interrupt request register
LPPASS_MMIO_INTR_SET	0x42EF0048	Interrupt request set register
LPPASS_MMIO_INTR_MASK	0x42EF0050	Interrupt request mask
LPPASS_MMIO_INTR_MASKED	0x42EF0058	Interrupt request masked
LPPASS_MMIO_FIFO_INTR	0x42EF0060	FIFO Interrupt request register
LPPASS_MMIO_FIFO_INTR_SET	0x42EF0068	FIFO Interrupt set request register
LPPASS_MMIO_FIFO_INTR_MASK	0x42EF0070	FIFO Interrupt mask register
LPPASS_MMIO_FIFO_INTR_MASKED	0x42EF0078	FIFO Interrupt masked request register
LPPASS_MMIO_STA_CFG	0x42EF0400	FIFO configuration register.
LPPASS_MMIO_STA_MODE	0x42EF0404	FIFO mode register.
LPPASS_MMIO_STA_MODE_STATUS	0x42EF0408	FIFO mode status register.
LPPASS_MMIO_STA_LEVEL0	0x42EF0410	FIFO level register.

Autonomous Analog registers

Register name	Address	Description
LPPASS_MMIO_STA_LEVEL1	0x42EF0414	FIFO level register.. See LPPASS_MMIO_STA_LEVEL0 for the details of bit fields.
LPPASS_MMIO_STA_LEVEL2	0x42EF0418	FIFO level register.. See LPPASS_MMIO_STA_LEVEL0 for the details of bit fields.
LPPASS_MMIO_STA_LEVEL3	0x42EF041C	FIFO level register.. See LPPASS_MMIO_STA_LEVEL0 for the details of bit fields.
LPPASS_MMIO_STA_LEVEL4	0x42EF0420	FIFO level register.. See LPPASS_MMIO_STA_LEVEL0 for the details of bit fields.
LPPASS_MMIO_STA_LEVEL5	0x42EF0424	FIFO level register.. See LPPASS_MMIO_STA_LEVEL0 for the details of bit fields.
LPPASS_MMIO_STA_LEVEL6	0x42EF0428	FIFO level register.. See LPPASS_MMIO_STA_LEVEL0 for the details of bit fields.
LPPASS_MMIO_STA_LEVEL7	0x42EF042C	FIFO level register.. See LPPASS_MMIO_STA_LEVEL0 for the details of bit fields.
LPPASS_MMIO_STA_RD_DATA0	0x42EF0430	FIFO 32-bit read data register
LPPASS_MMIO_STA_RD_DATA1	0x42EF0434	FIFO 32-bit read data register. See LPPASS_MMIO_STA_RD_DATA0 for the details of bit fields.
LPPASS_MMIO_STA_RD_DATA2	0x42EF0438	FIFO 32-bit read data register. See LPPASS_MMIO_STA_RD_DATA0 for the details of bit fields.
LPPASS_MMIO_STA_RD_DATA3	0x42EF043C	FIFO 32-bit read data register. See LPPASS_MMIO_STA_RD_DATA0 for the details of bit fields.
LPPASS_MMIO_STA_RD_DATA4	0x42EF0440	FIFO 32-bit read data register. See LPPASS_MMIO_STA_RD_DATA0 for the details of bit fields.
LPPASS_MMIO_STA_RD_DATA5	0x42EF0444	FIFO 32-bit read data register. See LPPASS_MMIO_STA_RD_DATA0 for the details of bit fields.
LPPASS_MMIO_STA_RD_DATA6	0x42EF0448	FIFO 32-bit read data register. See LPPASS_MMIO_STA_RD_DATA0 for the details of bit fields.
LPPASS_MMIO_STA_RD_DATA7	0x42EF044C	FIFO 32-bit read data register. See LPPASS_MMIO_STA_RD_DATA0 for the details of bit fields.
LPPASS_MMIO_STA_USED0	0x42EF0450	FIFO used register
LPPASS_MMIO_STA_USED1	0x42EF0454	FIFO used register. See LPPASS_MMIO_STA_USED0 for the details of bit fields.
LPPASS_MMIO_STA_USED2	0x42EF0458	FIFO used register. See LPPASS_MMIO_STA_USED0 for the details of bit fields.
LPPASS_MMIO_STA_USED3	0x42EF045C	FIFO used register. See LPPASS_MMIO_STA_USED0 for the details of bit fields.

Autonomous Analog registers

Register name	Address	Description
LPPASS_MMIO_STA_USED4	0x42EF0460	FIFO used register. See LPPASS_MMIO_STA_USED0 for the details of bit fields.
LPPASS_MMIO_STA_USED5	0x42EF0464	FIFO used register. See LPPASS_MMIO_STA_USED0 for the details of bit fields.
LPPASS_MMIO_STA_USED6	0x42EF0468	FIFO used register. See LPPASS_MMIO_STA_USED0 for the details of bit fields.
LPPASS_MMIO_STA_USED7	0x42EF046C	FIFO used register. See LPPASS_MMIO_STA_USED0 for the details of bit fields.
LPPASS_MMIO_STA_STATUS0	0x42EF0470	FIFO status register
LPPASS_MMIO_STA_STATUS1	0x42EF0474	FIFO status register. See LPPASS_MMIO_STA_STATUS0 for the details of bit fields.
LPPASS_MMIO_STA_STATUS2	0x42EF0478	FIFO status register. See LPPASS_MMIO_STA_STATUS0 for the details of bit fields.
LPPASS_MMIO_STA_STATUS3	0x42EF047C	FIFO status register. See LPPASS_MMIO_STA_STATUS0 for the details of bit fields.
LPPASS_MMIO_STA_STATUS4	0x42EF0480	FIFO status register. See LPPASS_MMIO_STA_STATUS0 for the details of bit fields.
LPPASS_MMIO_STA_STATUS5	0x42EF0484	FIFO status register. See LPPASS_MMIO_STA_STATUS0 for the details of bit fields.
LPPASS_MMIO_STA_STATUS6	0x42EF0488	FIFO status register. See LPPASS_MMIO_STA_STATUS0 for the details of bit fields.
LPPASS_MMIO_STA_STATUS7	0x42EF048C	FIFO status register. See LPPASS_MMIO_STA_STATUS0 for the details of bit fields.

28.1.1 CTBL0_STA_CFG

Description: Configuration (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E00400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OA0_TOPO [7:4]				OA0_PWR_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW	RW	RW	
HW Access	R				R	R	R	
Name	C0_FB [15:12]				OA0_C-C_ENABLE	RES0_SWAP	OA0_COMP_OUT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	OA1_TOPO [23:20]				OA1_PWR_MODE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW	RW	RW	
HW Access	R				R	R	R	
Name	C1_FB [31:28]				OA1_C-C_ENABLE	RES1_SWAP	OA1_COMP_OUT [25:24]	

Bits	Name	Description
31 : 28	C1_FB	Feed back Cap value (see C0_FB) Default Value: 0
27	OA1_CC_ENABLE	Opamp1 miller compensation capacitor enable Default Value: 0 **0x0: DISABLE :** Opamp1 contains no miller compensation capactior. **0x1: ENABLE :** The compensation capacitor value is determined by CTBL_TRIM_STRUCT.OA1_COM-P_TRIM.OA1_COMP_TRIM
26	RES1_SWAP	Swap Top and Bottom resistor value (see RES0_SWAP) Default Value: 0
25 : 24	OA1_COMP_OUT	Opamp1 comparator edge detect output (for interrupt and trigger generation) Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected

28.1.1 CTBL0_STA_CFG (continued)

		0x1: RISING : Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
23 : 20	OA1_TOPO	OA1 Opamp Configuration: see description of OA0_CFG Default Value: 0
19 : 16	OA1_PWR_MODE	Opamp1 power level: see description of OA0_PWR_MODE Default Value: 0
15 : 12	C0_FB	Feed back Cap value select This field is only used if OA0_TOPO is set to 1, 2, or 4 and the Opamp Gain (set by the AC) is set to a non-unity value. The feedback capacitor is used to compensate the resistive feedback network. Values range from 0pF to 10.5pF in 0.7pF increments. 0000: 0pF 0001: 0.7pF 0010: 1.4pF 0011: 2.1pF 0100: 2.8pF 0101: 3.5pF 0110: 4.2pF 0111: 4.9pF 1000: 5.6pF 1001: 6.3pF 1010: 7.0pF 1011: 7.7pF 1100: 8.4pF 1101: 9.1pF 1110: 9.8pF 1111: 10.5pF Default Value: 0
11	OA0_CC_ENABLE	Opamp0 miller compensation capacitor enable Default Value: 0 **0x0: DISABLE :** Opamp0 contains no miller compensation capactior. **0x1: ENABLE :** The compensation capacitor value is determined by CTBL_TRIM_STRUCT.OA0_COMP_TRIM.OA0_COMP_TRIM
10	RES0_SWAP	RESERVED: Do not change from default Swap Top and Bottom resistor value Default Value: 0
9 : 8	OA0_COMP_OUT	6= Buffer Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected

28.1.1 CTBL0_STA_CFG (continued)

		0x1: RISING : Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
7 : 4	OA0_TOPO	OA0 Opamp Configuration 0= Comparator 1= PGA 2= TIA 3= Open Loop Opamp (must enable OA_TO_PIN in dynamic configuration) 4= Differential Amplifier (requires the same config for both OAs) 5= Hysteretic Comparator 6= Buffer 7-15=RESERVED Default Value: 0
3 : 0	OA0_PWR_MODE	Opamp0 power level Default Value: 0 **0x0: OFF :** Off **0x1: ULTRA_LOW :** If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=0: opamp quiscent current of 15uA, input common mode of 0.2V to VDDA-1V, gain bandwidth of 30kHz. If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=1: opamp quiscent current of 15uA, input common mode of 0.2V to VDDA-1V, gain bandwidth of 100kHz, 10uA output drive capability. **0x2: ULTRA_LOW_RAIL :** If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=0: opamp quiscent current of 35uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 30kHz. If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=1: opamp quiscent current of 35uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 100kHz, 10uA output drive capability. **0x3: LOW :** Do Not Use **0x4: LOW_RAIL :** If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=0: opamp quiscent current of 150uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 350kHz. If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=1: opamp quiscent current of 150uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 1.2MHz, 100uA output drive capability. **0x5: MEDIUM :** Do Not Use

28.1.1 CTBL0_STA_CFG (continued)

0x6: MEDIUM_RAIL :

If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=0: opamp quiscent current of 200uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 700kHz.
If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=1: opamp quiscent current of 200uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 2.4MHz, 1mA output drive capability.

0x7: HIGH :

Do Not Use

0x8: HIGH_RAIL :

If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=0: opamp quiscent current of 600uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 1.75MHz.
If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=1: opamp quiscent current of 600uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 6MHz,1mA output drive capability.

0x9: ULTRA_HIGH :

Do Not Use

0xa: ULTRA_HIGH_RAIL :

If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=0: opamp quiscent current of 800uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 2.8MHz.
If CTBL_DYN_CFG_STRUCT.OA_MUX_CFG.OA_TO_PIN=1: opamp quiscent current of 800uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 7.5MHz, 10mA output drive capability.

0xb: RESERVED_0 :

0xc: RESERVED_1 :

0xd: RESERVED_2 :

0xe: RESERVED_3 :

0xf: RESERVED_4 :

28.1.2 CTBL0_STA_COMP_STAT

Description: Comparator status

Address: 0x42E00404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							OA0_-COMP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [23:17]							OA1_-COMP

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	OA1_COMP	Opamp1 current comparator status Default Value: 0
0	OA0_COMP	Opamp0 current comparator status Default Value: 0

28.1.3 CTBL0_DYN0_OA_MUX_CFG

Description: Opamp Mux Configuration

Address: 0x42E00600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW			Reserved		RW	
HW Access	Reserved	R			Reserved		R	
Name	Reserved	OA_INP_REF [6:4]			Reserved [3:2]		OA_INP_DIRECT [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW		Reserved		RW	
HW Access	Reserved		R		Reserved		R	
Name	Reserved [15:14]		OA_RES_DIRECT [13:12]		Reserved [11:10]		OA_INM_DIRECT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW				Reserved	RW		
HW Access	R				Reserved	R		
Name	CTBBUS_MUX_IN [23:20]				Reserved	OA_RES_REF [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW	Reserved		RW			
HW Access	Reserved	R	Reserved		R			
Name	Reserved	OA_TO_PIN	Reserved [29:28]		CTBBUS_MUX_OUT [27:24]			

Bits	Name	Description
30	OA_TO_PIN	OA Output connects to pin Default Value: 0
27 : 24	CTBBUS_MUX_OUT	CTBBUS (Shared Mux)Output mux 0 = Disconnected 1 = CTBBUS to Opamp positive input 2 = CTBBUS to Opamp negative input 3 = CTBBUS to Opamp resistor bottom 4-15 = RESERVED Default Value: 0
23 : 20	CTBBUS_MUX_IN	CTBBUS (Shared Mux) Input mux 0 = Disconnected 1 = P0 to CTBBUS 2 = P1 to CTBBUS 3 = P2 to CTBBUS 4 = P3 to CTBBUS 5 = P4 to CTBBUS 6 = P5 to CTBBUS 7 = P6 to CTBBUS 8 = P7 to CTBBUS 9-15 = RESERVED Default Value: 0

28.1.3 CTBL0_DYN0_OA_MUX_CFG (continued)

18 : 16	OA_RES_REF	Opamp inverting terminal reference connection 0 = Disconnected 1 = vref0 2 = vref1 3= Adjacent CTBL OA0 Output 4 = Adjacent CTBL OA1 Output 5 = VSSA 6-15 = RESERVED Default Value: 0
13 : 12	OA_RES_DIRECT	Opamp inverting terminal direct connection 0 = Disconnected 1 = OA0: P0 OA1: P5 2 = OA0: P1 OA1: P4 3 = RESERVED Default Value: 0
9 : 8	OA_INM_DIRECT	Opamp inverting terminal direct connection 0 = Disconnected 1 = OA0: P0 OA1: P5 2 = OA0: P1 OA1: P4 3 = RESERVED Default Value: 0
6 : 4	OA_INP_REF	Opamp non-inverting terminal reference connection 0 = Disconnected 1 = vref0 2 = vref1 3 = vref2 4 = vref3 5 = vbgr 6 = Adjacent CTBL OA0 Output 7 = Adjacent CTBL OA1 Output Default Value: 0
1 : 0	OA_INP_DIRECT	Opamp non-inverting terminal direct connection 0 = Disconnected 1 = OA0: P0 OA1: P5 2 = OA0: P1 OA1: P4 3 = RESERVED Default Value: 0

28.1.4 CTBL0_TRIM_OA0_OFFSET_TRIM

Description: Opamp0 trim control

Address: 0x42E00F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		OA0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	OA0_OFFSET_TRIM	Opamp0 offset trim Default Value: 0

28.1.5 CTBL0_TRIM_OA0_SLOPE_OFFSET_TRIM

Description: Opamp0 trim control

Address: 0x42E00F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		OA0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	OA0_SLOPE_OFF-SET_TRIM	Opamp0 slope offset drift trim Default Value: 0

28.1.6 CTBL0_TRIM_OA0_COMP_TRIM

Description: Opamp0 trim control

Address: 0x42E00F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				OA0_COMP_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	OA0_COMP_TRIM	Opamp0 Compensation Capacitor Trim Bit<3> is not used Bits<2:0> 000 = 0.1pF 001 = 1.1pF 010 = 2.1pF 011 = 3.1pF 100 = 4.1pF 101 = 5.1pF 110 = 6.1pF 111 = 7.1pF Default Value: 0

28.1.7 CTBL0_TRIM_OA1_OFFSET_TRIM

Description: Opamp1 trim control

Address: 0x42E00F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		OA1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	OA1_OFFSET_TRIM	Opamp1 offset trim Default Value: 0

28.1.8 CTBL0_TRIM_OA1_SLOPE_OFFSET_TRIM

Description: Opamp1 trim control

Address: 0x42E00F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		OA1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	OA1_SLOPE_OFF-SET_TRIM	Opamp1 slope offset drift trim Default Value: 0

28.1.9 CTBL0_TRIM_OA1_COMP_TRIM

Description: Opamp1 trim control

Address: 0x42E00F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				OA1_COMP_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	OA1_COMP_TRIM	Opamp1 Compensation Capacitor Trim (See OA0_COMP_TRIM) Default Value: 0

28.1.10 CTBL0_TRIM_RMP_TRIM

Description: Risk Mitigation bits

Address: 0x42E00F18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				RMP_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	RMP_TRIM	Bits <1:0> Risk mitigation for bias in reference block 0 = Bias +20% 1 = Normal Bias (Default) 2 = Normal BIas 3 = Bias -20% Bits <3:2> Risk mitigation for pump block in OA0 and OA1 0 = Normal Pump Operation for OA0 and OA1 (If pump is enabled). 1 = Reserved (Don't use!) 2 = Pumps are boosted for OA0 and OA1 (if PUMP is enabled). 3 = Reserved (Don't use!) Default Value: 1

28.1.11 PTC_STA_CFG

Description: PTC Configuration Register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E40400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW		Reserved	RW	RW	
HW Access	Reserved		R		Reserved	R	R	
Name	Reserved [7:6]		COMP0_OUT [5:4]		Reserved	COMP0_HYST	COMP0_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW		Reserved	RW	RW	
HW Access	Reserved		R		Reserved	R	R	
Name	Reserved [15:14]		COMP1_OUT [13:12]		Reserved	COMP1_HYST	COMP1_MODE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
13 : 12	COMP1_OUT	See COMP0_OUT Default Value: 0 **0x0: DISABLE :** **0x1: RISING :** **0x2: FALLING :** **0x3: BOTH :**
10	COMP1_HYST	See COMP0_HYST Default Value: 0
9 : 8	COMP1_MODE	See COMP0_MODE Default Value: 0 **0x0: OFF :** **0x1: ULP :** **0x2: LP :**

28.1.11 PTC_STA_CFG (continued)

		0x3: NORMAL :
5 : 4	COMP0_OUT	Comparator 0 output (for interrupt and trigger generation) Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
2	COMP0_HYST	Add 30mV hysteresis to the comparator 0 0= Disable Hysteresis 1= Enable Hysteresis Default Value: 0
1 : 0	COMP0_MODE	Operating mode for the comparator 0 Default Value: 0 **0x0: OFF :** Off **0x1: ULP :** Ultra lowpower operating mode (quiscent current < 300nA, 7us response time to 100mV overdrive). The comparator is biased using a local reference. **0x2: LP :** Low Power operating mode (quiscent current < 10uA, 1us response time to 100mV overdrive). **0x3: NORMAL :** Normal Power operating mode (quiscent current < 150uA, 0.1us response time to 100mV overdrive).

28.1.12 PTC_STA_COMP_STAT

Description: PTC Status Register

Address: 0x42E40404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [23:17]							OUT1

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	OUT1	Current output value of the comparator 1. Default Value: 0
0	OUT0	Current output value of the comparator 0. Default Value: 0

28.1.13 PTC_STA_PP_CFG0

Description: Post Process Configuration register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E40408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						INPUT_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	INPUT_SEL	Default Value: 0 **0x0: DISABLED :** **0x1: COMP0 :** Comparator 0 output **0x2: COMP1 :** Comparator 1 output **0x3: RESERVED :**

28.1.14 PTC_DYN0_MUX_CFG

Description: PTC Mux Configuration

Address: 0x42E40600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			INP_MUX_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [15:13]			INN_MUX_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
12 : 8	INN_MUX_SEL	Default Value: 0 **0x0: COREIO_0 :** CTBL0 GPIO Pin 1. See product datasheet for specific pin number. **0x1: COREIO_1 :** CTBL0 GPIO Pin 4. See product datasheet for specific pin number. **0x2: COREIO_2 :** CTBL0 GPIO Pin 6. See product datasheet for specific pin number. **0x3: COREIO_3 :** CTBL0 GPIO Pin 7. See product datasheet for specific pin number. **0x4: COREIO_4 :** CTBL1 GPIO Pin 1. See product datasheet for specific pin number. **0x5: COREIO_5 :** CTBL1 GPIO Pin 4. See product datasheet for specific pin number.

28.1.14 PTC_DYN0_MUX_CFG (continued)

0x6: COREIO_6 :

CTBL1 GPIO Pin 6. See product datasheet for specific pin number.

0x7: COREIO_7 :

CTBL1 GPIO Pin 7. See product datasheet for specific pin number.

0x8: CTBL0_OA0 :

CTBL0 Opamp0 Output

0x9: CTBL0_OA1 :

CTBL0 Opamp1 Output

0xa: CTBL1_OA0 :

CTBL1 Opamp0 Output

0xb: CTBL1_OA1 :

CTBL1 Opamp1 Output

0xc: VREF0 :

DAC0 output

0xd: VREF1 :

DAC1 output

0xe: VREF2 :

PRB VREF0 output

0xf: VREF3 :

PRB VREF1 output

0x10: GPIO_0 :

SAR/PTC GPIO Pin 0. See product datasheet for specific pin number.

0x11: GPIO_1 :

SAR/PTC GPIO Pin 1. See product datasheet for specific pin number.

0x12: GPIO_2 :

SAR/PTC GPIO Pin 2. See product datasheet for specific pin number.

0x13: GPIO_3 :

SAR/PTC GPIO Pin 3. See product datasheet for specific pin number.

28.1.14 PTC_DYN0_MUX_CFG (continued)

0x14: GPIO_4 :

SAR/PTC GPIO Pin 4. See product datasheet for specific pin number.

0x15: GPIO_5 :

SAR/PTC GPIO Pin 5. See product datasheet for specific pin number.

0x16: GPIO_6 :

SAR/PTC GPIO Pin 6. See product datasheet for specific pin number.

0x17: GPIO_7 :

SAR/PTC GPIO Pin 7. See product datasheet for specific pin number.

0x18: RESEREVED_0 :

0x19: RESEREVED_1 :

0x1a: RESEREVED_2 :

0x1b: RESEREVED_3 :

0x1c: RESEREVED_4 :

0x1d: RESEREVED_5 :

0x1e: RESEREVED_6 :

0x1f: RESEREVED_7 :

4 : 0 INP_MUX_SEL Default Value: 0

0x0: COREIO_0 :

CTBL0 GPIO Pin 1. See product datasheet for specific pin number.

0x1: COREIO_1 :

CTBL0 GPIO Pin 4. See product datasheet for specific pin number.

0x2: COREIO_2 :

CTBL0 GPIO Pin 6. See product datasheet for specific pin number.

0x3: COREIO_3 :

CTBL0 GPIO Pin 7. See product datasheet for specific pin number.

0x4: COREIO_4 :

CTBL1 GPIO Pin 1. See product datasheet for specific pin number.

28.1.14 PTC_DYN0_MUX_CFG (continued)

0x5: COREIO_5 :

CTBL1 GPIO Pin 4. See product datasheet for specific pin number.

0x6: COREIO_6 :

CTBL1 GPIO Pin 6. See product datasheet for specific pin number.

0x7: COREIO_7 :

CTBL1 GPIO Pin 7. See product datasheet for specific pin number.

0x8: CTBL0_OA0 :

CTBL0 Opamp0 Output

0x9: CTBL0_OA1 :

CTBL0 Opamp1 Output

0xa: CTBL1_OA0 :

CTBL1 Opamp0 Output

0xb: CTBL1_OA1 :

CTBL1 Opamp1 Output

0xc: VREF0 :

DAC0 output

0xd: VREF1 :

DAC1 output

0xe: VREF2 :

PRB VREF0 output

0xf: VREF3 :

PRB VREF1 output

0x10: GPIO_0 :

SAR/PTC GPIO Pin 0. See product datasheet for specific pin number.

0x11: GPIO_1 :

SAR/PTC GPIO Pin 1. See product datasheet for specific pin number.

0x12: GPIO_2 :

SAR/PTC GPIO Pin 2. See product datasheet for specific pin number.

28.1.14 PTC_DYN0_MUX_CFG (continued)

0x13: GPIO_3 :

SAR/PTC GPIO Pin 3. See product datasheet for specific pin number.

0x14: GPIO_4 :

SAR/PTC GPIO Pin 4. See product datasheet for specific pin number.

0x15: GPIO_5 :

SAR/PTC GPIO Pin 5. See product datasheet for specific pin number.

0x16: GPIO_6 :

SAR/PTC GPIO Pin 6. See product datasheet for specific pin number.

0x17: GPIO_7 :

SAR/PTC GPIO Pin 7. See product datasheet for specific pin number.

0x18: RESEREVED_0 :

0x19: RESEREVED_1 :

0x1a: RESEREVED_2 :

0x1b: RESEREVED_3 :

0x1c: RESEREVED_4 :

0x1d: RESEREVED_5 :

0x1e: RESEREVED_6 :

0x1f: RESEREVED_7 :

28.1.15 PTC_PP0_CFG

Description: Post Processing configuration

Address: 0x42E40700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW		RW	
HW Access	Reserved				R		R	
Name	Reserved [7:4]				MODE [3:2]		INPUT_TYPE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				LUT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11 : 8	LUT	LUT function A and B corresponds to the individual post processor range outputs (i.e. for PTC_PP_-STRUCT0_CFG.LUT, A is the Post Processor 0 range comparison, and B is the Post Processor 1 range comparison. For PTC_PP_STRUCT1_CFG.LUT, A is the Post Processor 1 range comparison, and B is the Post Processor 0 range comparison) Default Value: 0 **0x0: A :** **0x1: A_BAR_AND_B :** **0x2: B :** **0x3: A_AND_B :** **0x4: A_AND_B_BAR :** **0x5: A_XOR_B :** **0x6: A_OR_B :** **0x7: A_NOR_B :**

28.1.15 PTC_PP0_CFG (continued)

		0x8: A_XNOR_B :
		0x9: B_BAR :
		0xa: A_OR_B_BAR :
		0xb: A_BAR :
		0xc: A_BAR_OR_B :
		0xd: A_NAND_B :
		0xe: RESERVED0 :
		0xf: RESERVED1 :
3 : 2	MODE	Post Processor Counter Mode Default Value: 0
		0x0: DIRECT :
		Direct mode: in this mode, the counter is configured to count the number of INPUT_TYPES. The condition is evaluated (based on the THRESHOLD register) every rising edge of the post precessor clock. If the condition is met, the counter is reset.
		0x1: FRAME :
		Frame mode: in this mode, the counter is configured to count the number of INPUT_TYPES that occur during a given frame. The frame rate is determined by FRAME.PERIOD. At the end of the frame, the condition is evaluated (based on the THRESHOLD register) and the counter is reset to begin the next frame.
		0x2: WINDOW :
		Window mode: in this mode, the counter is configured to count the number of INPUT_TYPES that occur inside a given window. The window size is set by WINDOW.SIZE. After filling the window, the condition is evaluted (based on the THRESHOLD register) every rising edge of the post processor clock. The counter is not reset in this mode.
		0x3: RESERVED :
1 : 0	INPUT_TYPE	Input data type (selected by PTC_STA_CFG.PP_CFG0(1).INPUT_SEL.) Default Value: 0
		0x0: LEVEL :
		level sensitive
		0x1: EDGE_RISING :
		rising edge sensitive
		0x2: EDGE_FALLING :
		falling edge sensitive

28.1.15 PTC_PP0_CFG (continued)

0x3: EDGE_BOTH :

both rising and falling edge sensitive

28.1.16 PTC_PP0_FRAME

Description: Post Processing frame

Address: 0x42E40704

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				PERIOD [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11 : 0	PERIOD	Period Value. This field is only applicable if CFG.MODE=FRAM. The frame rate is PERIOD+1 PTC Clock cycles. Default Value: 0

28.1.17 PTC_PP0_THRESHOLD

Description: Post Processing threshold

Address: 0x42E40708

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				LOW [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved		RW		RW			
HW Access	Reserved		R		R			
Name	Reserved [31:30]		COND [29:28]		HIGH [27:24]			

Bits	Name	Description
29 : 28	COND	Range condition select. Default Value: 0 **0x0: BELOW :** counter output < LOW **0x1: INSIDE :** LOW <= counter output < HIGH **0x2: ABOVE :** counter output > HIGH **0x3: OUTSIDE :** counter output < LOW || counter output >= HIGH
27 : 16	HIGH	High threshold Default Value: 0
11 : 0	LOW	Low threshold Default Value: 0

28.1.18 PTC_PP0_WINDOW

Description: Post Processing window

Address: 0x42E4070C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	SIZE	Window size. This field is only applicable if CFG.MODE=WINDOW Default Value: 4 **0x0: WINDOW_TWO :** Window size of 2 **0x1: WINDOW_FOUR :** Window size of 4 **0x2: WINDOW_EIGHT :** Window size of 8 **0x3: WINDOW_SIXTEEN :** Window size of 16 **0x4: WINDOW_THIRTY_TWO :** Window size of 32

28.1.18 PTC_PP0_WINDOW (continued)

0x5: WINDOW_SIXTY_FOUR :

Window size of 64

0x6: WINDOW_ONE_TWENTY_EIGHT :

Window size of 128

0x7: RESERVED :

28.1.19 PTC_TRIM_CMP0_OFFSET_TRIM

Description: Comparator 0 offset trim register

Address: 0x42E40F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [7:6]		CMP0_EN	CMP0_POLARITY	CMP0_MAGNITUDE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	CMP0_EN	enables CMP0 offset trim 0 = disabled 1 = enabled Default Value: 0
4	CMP0_POLARITY	polarity of CMP0 offset trim. 0 = negative 1 = positive Default Value: 0
3 : 0	CMP0_MAGNITUDE	magnitude of CMP0 offset trim. 1mV offset shift per bit. Default Value: 0

28.1.20 PTC_TRIM_CMP1_OFFSET_TRIM

Description: Comparator 1 offset trim register

Address: 0x42E40F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [7:6]		CMP1_EN	CMP1_POLARITY	CMP1_MAGNITUDE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	CMP1_EN	enables CMP1 offset trim 0 = disabled 1 = enabled Default Value: 0
4	CMP1_POLARITY	polarity of CMP1 offset trim. 0 = negative 1 = positive Default Value: 0
3 : 0	CMP1_MAGNITUDE	magnitude of CMP1 offset trim. 1mV offset shift per bit. Default Value: 0

28.1.21 DAC0_SRAM0

Description: SRAM Waveform Table (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E60000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAVEFORM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW			
HW Access	R		R		R			
Name	OUT_DM [15:14]		RESERVED [13:12]		WAVEFORM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	OUT_DM	DAC Output Drive Mode Default Value: Undefined **0x0: OUT_EN :** DAC output enabled (outputs WAVEFORM) **0x1: OUT_HIZ :** DAC output disabled (output is Tri-state) **0x2: OUT_REF :** DAC output disabled (output Vssa or Vref when disabled (see CTRL.BOT_SEL)) **0x3: RESERVED :**
13 : 12	RESERVED	Default Value: Undefined
11 : 0	WAVEFORM	DAC waveform Default Value: Undefined

28.1.22 DAC0_STA_CTRL

Description: DAC control register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E60800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	RW	RW	RW		
HW Access	Reserved	R	R	R	R	R		
Name	Reserved	DIS-ABLED_-MODE	BOT_SEL	DEG-LITCH_EN	VREF_SEL	TOPO [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	OUTBUF_PWR_MODE [15:12]				REFBUF_PWR_MODE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							FORMAT

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved	RW			Reserved			
HW Access	Reserved	R			Reserved			
Name	Reserved	REF_MUX_SEL [30:28]			Reserved [27:24]			

Bits	Name	Description
30 : 28	REF_MUX_SEL	DAC reference mux output select Default Value: 0 **0x0: VBGR :** DAC reference mux is driven by the AREF bandgap output (source selected by AREF.CTRL.VREF_SEL) **0x1: CTBL0_OA0 :** CTBL0 Opamp0 Output **0x2: CTBL0_OA1 :** CTBL0 Opamp1 Output **0x3: CTBL1_OA0 :** CTBL1 Opamp0 Output **0x4: CTBL1_OA1 :** CTBL1 Opamp1 Output

28.1.22 DAC0_STA_CTRL (continued)

		0x5: VDDA : Do Not Use **0x6: PRB_VREF0 :** PRB VREF0 output **0x7: PRB_VREF1 :** PRB VREF1 output
16	FORMAT	DAC output format select Default Value: 0 **0x0: UNSIGNED12 :** Unsigned 12-bit number, i.e. no value decoding **0x1: VIRT_SIGNED12 :** Virtual signed 12-bits' VDAC. Value decoding: add 0x800 to the 12-bit Value (=invert MSB), to convert the lowest signed number 0x800 to the lowest unsigned number 0x000. This is the same as the SAR handles 12-bit 'virtual' signed numbers.
15 : 12	OUTBUF_PWR_MODE	Output buffer power level Default Value: 0 **0x0: OFF :** Off **0x1: ULTRA_LOW :** If TOPO=BUFFERED_INTERNAL: quiscent current of 15uA, input common mode of 0.2V to VDDA-1V, gain bandwidth of 30kHz. If TOPO=BUFFERED_EXTERNAL: quiscent current of 15uA, input common mode of 0.2V to VDDA-1V, gain bandwidth of 100kHz, 10uA output drive capability. **0x2: ULTRA_LOW_RAIL :** If TOPO=BUFFERED_INTERNAL: quiscent current of 35uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 30kHz. If TOPO=BUFFERED_EXTERNAL: quiscent current of 35uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 100kHz, 10uA output drive capability. **0x3: LOW :** Do Not Use **0x4: LOW_RAIL :** If TOPO=BUFFERED_INTERNAL: quiscent current of 150uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 350kHz. If TOPO=BUFFERED_EXTERNAL: quiscent current of 150uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 1.2MHz, 100uA output drive capability.

28.1.22 DAC0_STA_CTRL (continued)

0x5: MEDIUM :

Do Not Use

0x6: MEDIUM_RAIL :

If TOPO=BUFFERED_INTERNAL: quiscent current of 200uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 700kHz.
If TOPO=BUFFERED_EXTERNAL: quiscent current of 200uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 2.4MHz, 1mA output drive capability.

0x7: HIGH :

Do Not Use

0x8: HIGH_RAIL :

If TOPO=BUFFERED_INTERNAL: quiscent current of 600uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 1.75MHz.
If TOPO=BUFFERED_EXTERNAL: quiscent current of 600uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 6MHz,1mA output drive capability.

0x9: ULTRA_HIGH :

Do Not Use

0xa: ULTRA_HIGH_RAIL :

If TOPO=BUFFERED_INTERNAL: quiscent current of 800uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 2.8MHz.
If TOPO=BUFFERED_EXTERNAL: quiscent current of 800uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 7.5MHz, 10mA output drive capability.

0xb: RESERVED_0 :

0xc: RESERVED_1 :

0xd: RESERVED_2 :

0xe: RESERVED_3 :

0xf: RESERVED_4 :

11 : 8	REFBUF_PWR_MODE	Reference buffer power level Default Value: 0

0x0: OFF :

Off

0x1: ULTRA_LOW :

reference buffer quiscent current of 15uA, input common mode of 0.2V to VDDA-1V, gain bandwidth of 30kHz.

28.1.22 DAC0_STA_CTRL (continued)

0x2: ULTRA_LOW_RAIL :

reference buffer quiscent current of 35uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 30kHz.

0x3: LOW :

Do Not Use

0x4: LOW_RAIL :

reference buffer quiscent current of 150uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 350kHz.

0x5: MEDIUM :

Do Not Use

0x6: MEDIUM_RAIL :

reference buffer quiscent current of 200uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 700kHz.

0x7: HIGH :

Do Not Use

0x8: HIGH_RAIL :

reference buffer quiscent current of 600uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 1.75MHz.

0x9: ULTRA_HIGH :

Do Not Use

0xa: ULTRA_HIGH_RAIL :

reference buffer quiscent current of 800uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth of 2.8MHz.

0xb: RESERVED_0 :

0xc: RESERVED_1 :

0xd: RESERVED_2 :

0xe: RESERVED_3 :

0xf: RESERVED_4 :

6	DISABLED_MODE	Select the output value when the output is disabled 0: Tri-state CTDAC output when disabled 1: output Vssa or Vref when disabled (see BOT_SEL description) Default Value: 0

28.1.22 DAC0_STA_CTRL (continued)

5	BOT_SEL	Bottom connection select to R2R network. 0: Connect to VSSA: DAC enabled: when DM_OUT=OUT_EN, the DAC range is [0, 4095] * Vref / 4096, when DM_OUT=OUT_REF, the DAC outputs VSSA. DAC disabled and DISABLED_MODE=1, the DAC outputs VSSA. 1: Connect to VREF: DAC enabled: when DM_OUT=OUT_EN, the DAC range is [1, 4096] * Vref / 4096, when DM_OUT=OUT_REF, the DAC outputs VREF. DAC disabled and DISABLED_MODE=1, the DAC outputs VREF. Default Value: 0
4	DEGLITCH_EN	Deglitch enable This field is used to prevent glitches after the DAC output changes by opening the output switch for (open time set by DEGLITCH_TIME). If TOPO is set to 0-2, CHO switch is opened during deglitch time, if TOPO is set to 3,4, COS switch is opened during deglitch time. Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**
3	VREF_SEL	DAC reference select Default Value: 0 **0x0: VREF_MUX_OUT :** DAC reference is driven by the reference mux (see REF_MUX_SEL). This selection requires that REFBUF_PWR_MODE be set to a value other than OFF. **0x1: VDDA :** DAC reference is driven directly from VDDA. Since this path does not use the DAC reference buffer, REFBUF_PWR_MODE should be set to OFF.
2 : 0	TOPO	DAC Topology Default Value: 0 **0x0: DIRECT :** DAC drives output directly **0x1: DIRECT_WITH_TRACK_CAP :** DAC drives output directly with Track Cap on output **0x2: DIRECT_WITH_TRACK_HOLD_CAP :** DAC drives output directly with Track and Hold Cap on output **0x3: BUFFERED_INTERNAL :** DAC output is buffered (internal connections only) **0x4: BUFFERED_EXTERNAL :** DAC output is buffered for internal or external connections **0x5: RESERVED_0 :** **0x6: RESERVED_1 :**

28.1.22 DAC0_STA_CTRL (continued)

0x7: RESERVED_2 :

28.1.23 DAC0_STA_SAMPLE_TIME

Description: Sample control register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E60804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	SAMPLE_TIME	Sample Time selection for Sample and Hold Modes This field is only used if enabled DAC channel is configured for sample and hold operation (i.e. CHAN_CFG.SAMPLE_AND_HOLD_EN=1) The sample time is measured in terms of CLK_HF (nominally 80MHz) cycles (if ACTRLR.STATUS.MODE=HS) or CLK_LPOSC (nominally 4.096MHz) cycles (if ACTRLR.STATUS.MODE=LP). Sample time = SAMPLE_TIME+1, range 1..256 Default Value: 0

28.1.24 DAC0_STA_STEP_VAL0

Description: step val register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E60808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	VAL	DAC step value. Actual step value is VAL+1. Step Type (address or data) is set by CHAN_CFG.MODE. The maximim allowable step value is set by the operational mode as follows: If CHAN_CFG.MODE= LUT_OS_ONE_QUAD, LUT_CONT_ONE_QUAD or ADDR: Max step size = (CHAN_CFG.END_ADDR - CHAN_CFG.START_ADDR + 1) If CHAN_CFG.MODE= LUT_OS_TWO_QUAD, LUT_OS_FOUR_QUAD, LUT_CONT_TWO_QUAD, LUT_CONT_FOUR_QUAD: Max step size = (CHAN_CFG.END_ADDR - CHAN_CFG.START_ADDR) If CHAN_CFG.MODE = DATA, there is no max step size. If the programmed step size exceeds the Max step size, the hardware not not advance the address pointer, and an EPOCH will be produced every DAC_CLOCK_EN. Default Value: 0

28.1.25 DAC0_STA_DEGLITCH_TIME

Description: deglitch time register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E60818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEGLITCH_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 0	DEGLITCH_TIME	Geglitch Time selection for DAC value updates This field is only used if CTRL.DEGLITCH_EN=1. The deglitch time is measured in terms of CLK_HF (nominally 80MHz) cycles (if ACTRLR.STATUS.MODE=HS) or CLK_LPOSC (nominally 4.096MHz) cycles (if ACTRLR.STATUS.MODE=LP). Deglitch time = GEGLITCH_TIME+1, range 1..256 Default Value: 1

28.1.26 DAC0_STA_CHAN_CFG0

Description: Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E60820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	START_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				Reserved	RW		
HW Access	R				Reserved	R		
Name	END_ADDR [15:12]				Reserved	START_ADDR [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved	RW						
HW Access	Reserved	R						
Name	Reserved	END_ADDR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW	RW		
HW Access	R		R		R	R		
Name	STATUS_SEL [31:30]		STEP_VAL_SEL [29:28]		SAM-PLE_AND_HOLD_EN	MODE [26:24]		

Bits	Name	Description
31 : 30	STATUS_SEL	Status selections. Default Value: 0 **0x0: DISABLED :** **0x1: STATUS_0 :** **0x2: STATUS_1 :** **0x3: STATUS_2 :**
29 : 28	STEP_VAL_SEL	DAC Step Value Selection Default Value: 0 **0x0: DISABLED :** STEP_VAL is 1. **0x1: STEP_0 :** STEP_VAL is set by STEP_VAL0.VAL.

28.1.26 DAC0_STA_CHAN_CFG0 (continued)

		0x2: STEP_1 : STEP_VAL is set by STEP_VAL1.VAL. **0x3: STEP_2 :** STEP_VAL is set by STEP_VAL2.VAL.
27	SAMPLE_AND_HOLD_EN	DAC Sample and Hold Enable SAMPLE_AND_HOLD_EN can only be selected if CTRL.TOPO=BUFFERED_INTERNAL or BUFFERED_EXTERNAL. The DAC is updated every positive edge of the DAC clock with the following sequence: 1. The DAC is configured for SAMPLE: DAC array is enabled and outputs the updated value (based on MODE) onto a capacitor for SAMPLE_TIME duration. 2. The DAC is configured for HOLD: DAC array is disabled and last output value is held on capacitor until next positive edge of the DAC clock (HOLD duration is DAC clock period - SAMPLE_TIME) *NOTE: For MODE=ADDRESS or DATA, the AC must wait for (ACT=WAIT_FOR) the DAC strobe (COND=DAC_STROBE) before re-triggering the DAC_INC/DAC_DEC fields. Default Value: 0
26 : 24	MODE	DAC operating mode Default Value: 0 **0x0: LUT_OS_ONE_QUAD :** DAC configured for One Shot One Quadrant LUT mode. LUT address increments every positive edge of the DAC clock until END_ADDR is reached or exceeded. Update Step size set by STEP_VAL_SEL. The One Shot is completed by the END_ADDR is reached. The DAC outputs an EPOCH trigger after reaching (or exceeding) the END_ADDR and outputing the corresponding value. **0x1: LUT_OS_TWO_QUAD :** DAC configured for One Shot Two Quadrant LUT mode. LUT address increments every positive edge of the DAC clock until END_ADDR is reached*, then the LUT address decrements back to the START_ADDR. DAC outputs an EPOCH trigger after returning to (or exceeding) the START_ADDR and outputing the START_ADDR value. *NOTE: If the END_ADDR is not reached but instead exceeded (can occur for STEP_VAL_SEL=1,2) then the LUT address is decremented from END_ADDR by the exceeded amount). After outputing the END ADDR in one direction, While wrapping around in reverse direction STEP_VAL is decremented from that last address value. (i.e. we output the last value only once and while going back in opposite direction, we ouput the address which is last address minus the step_val).

28.1.26 DAC0_STA_CHAN_CFG0 (continued)

0x2: LUT_OS_FOUR_QUAD :

DAC configured for One Shot Four Quadrant LUT mode.
LUT address is updated every positive edge of the DAC clock according to the following algorithm:
1. LUT address increments until END_ADDR is reached*.
2. LUT address decrements until START_ADDR is reached*.
3. Invert polarity and repeat 1 and 2.
DAC outputs an EPOCH trigger after returning to (or exceeding) the START_ADDR with an Inverted polarity and outputting the corresponding value.
(This mode assumes that the DAC waveform table (stored in SRAM) constitutes 1/4 of the desired generated waveform)
*NOTE: If the START/END_ADDR is not reached but instead exceeded (can occur for STEP_VAL_SEL=1,2) then the LUT address is adjusted (i.e. decremented from END_ADDR or incremented from the STAR_ADDR by the amount exceeded).
After outputing the START/END ADDR in one direction, While wrapping around in opposite direction STEP_VAL is incremented/decremented from that last address value. (i.e. we output the last value only once and while going back in opposite direction, we ouput the address which is last address plus/minus the step_val).

0x3: LUT_CONT_ONE_QUAD :

DAC configured for Continuous One Quadrant LUT mode.
LUT address increments every positive edge of the DAC clock until END_ADDR is reached*. The address then wraps back to the START_ADDR and repeats indefinitiely. Update Step size set by STEP_VAL_SEL.
The DAC outputs an EPOCH trigger after reaching (or exceeding) the END_ADDR and outputing the corresponding value.
*NOTE: If the END_ADDR is not reached but instead exceeded (can occur for STEP_VAL_-SEL=1,2) then the LUT address wraps back to the STAR_ADDR and is further incremented by the amount exceeded).

0x4: LUT_CONT_TWO_QUAD :

DAC configured for Continuous Two Quadrant LUT mode.
LUT address increments every positive edge of the DAC clock until END_ADDR is reached*, then the LUT address decrements back to the START_ADDR and repeats indefinitely.
DAC outputs an EPOCH trigger after returning to the START_ADDR and outputing the START_ADDR value.
*NOTE: If the START/END_ADDR is not reached but instead exceeded (can occur for STEP_VAL_SEL=1,2) then the LUT address is adjusted (i.e. decremented from END_ADDR or incremented from the STAR_ADDR by the amount exceeded).
After outputing the START/END ADDR in one direction, While wrapping around in opposite direction STEP_VAL is incremented/decremented from that last address value. (i.e. we output the last value only once and while going back in opposite direction, we ouput the address which is last address plus/minus the step_val).

28.1.26 DAC0_STA_CHAN_CFG0 (continued)

0x5: LUT_CONT_FOUR_QUAD :

DAC configured for Continuous Four Quadrant LUT mode.
LUT address is updated every positive edge of the DAC clock according to the following algorithm:
1. LUT address increments until END_ADDR is reached*.
2. LUT address decrements until START_ADDR is reached*.
3. Invert polarity and repeat 1 and 2 and repeat indefinitely.
DAC outputs an EPOCH trigger after returning to (or exceeding) the START_ADDR with an Inverted polarity and outputting the corresponding value.
(This mode assumes that the DAC waveform table (stored in SRAM) constitutes 1/4 of the desired generated waveform)
*NOTE: If the START/END_ADDR is not reached but instead exceeded (can occur for STEP_VAL_SEL=1,2) then the LUT address is adjusted (i.e. decremented from END_ADDR or incremented from the STAR_ADDR by the amount exceeded).
After outputing the START/END ADDR in one direction, While wrapping around in opposite direction STEP_VAL is incremented/decremented from that last address value. (i.e. we output the last value only once and while going back in opposite direction, we ouput the address which is last address plus/minus the step_val).

0x6: ADDR :

DAC configured for ADDRESS mode
Address is updated every positive edge of the DAC_INC or DAC_DEC from AC (unless SAMPLE_AND_HOLD_EN is set). Step size set by STEP_SIZE_EN and STEP_VAL.

If on the START_ADDR and DAC_DEC is triggered, the ADDR wraps forward to the END_ADDR.
If on the END_ADDR and DAC_INC is triggered, the address wraps back to the START_ADDR.
In this mode, the DAC does not output an EPOCH trigger.

0x7: DATA :

DAC configured for DATA mode
DAC outputs the data stored at the start address. The DAC output value is incremented or decremented based on AC.DAC_INC and AC.DAC_DEC The data is updated every positive edge of the DAC_INC or DAC_DEC (unless SAMPLE_AND_HOLD_EN is set). The increment/decrement amount is set by STEP_VAL_SEL.
In this mode, the DAC does not output an EPOCH trigger.
The DAC value is clamped if requested to go under the minimum code (0x000 for unsigned or 0x800 for signed) or above the maximum code (0xFFF for unsigned or 0x7FF for signed).

22 : 12	END_ADDR	End of Waveform Address pointer The end address must be greater than or equal to the start address (START_ADDR) END_ADDR is word(16bits) aligned and value ranges from 0-511 Default Value: 0
10 : 0	START_ADDR	Start of Waveform Address pointer When triggered (AC_DAC_TR), the DAC outputs the value at START_ADDR START_ADDR is word(16bits) aligned and value ranges from 0-511 Default Value: 0

28.1.27 DAC0_STA_FW_DAC_VAL

Description: Firmare Channel DAC Value (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E60860

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW		Reserved		RW			
HW Access	RW		Reserved		RW			
Name	OUT_DM [15:14]		Reserved [13:12]		VALUE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	OUT_DM	DAC Output Drive Mode Default Value: 0 **0x0: OUT_EN :** DAC output enabled (outputs VALUE) **0x1: OUT_HIZ :** DAC output disabled (output is Tri-state) **0x2: OUT_REF :** DAC output disabled (output Vssa or Vref when disabled (see CTRL.BOT_SEL)) **0x3: RESERVED :**
11 : 0	VALUE	DAC Value Writes to this register are ignored unless ACTRLR.TIMER_TABLE_- STRUCT.TT_CFG3.DAC[X]_CHANNEL=FW_CHANNEL Default Value: 0

28.1.28 DAC0_STA_FW_DAC_VAL_NXT

Description: Firmware Channel DAC Value Next

Address: 0x42E60864

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW		Reserved		RW			
HW Access	R		Reserved		R			
Name	OUT_DM [15:14]		Reserved [13:12]		VALUE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 14	OUT_DM	DAC Output Drive Mode Default Value: 0 **0x0: OUT_EN :** DAC output enabled (outputs VALUE) **0x1: OUT_HIZ :** DAC output disabled (output is Tri-state) **0x2: OUT_REF :** DAC output disabled (output Vssa or Vref when disabled (see CTRL.BOT_SEL)) **0x3: RESERVED :**
11 : 0	VALUE	Next value for FW_DAC_VAL.VALUE Writes to this register are ignored unless ACTRLR.TIMER_TABLE_STRUCT.TT_CFG3.DAC[X]_CHANNEL=FW_CHANNEL Default Value: 0

28.1.29 DAC0_STA_CHAN_STATUS_CFG0

Description: Channel status configuration register

Address: 0x42E60870

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						RANGE_COND [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	RANGE_HIGH [23:20]				RANGE_LOW [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [31:24]							

Bits	Name	Description
31 : 20	RANGE_HIGH	High threshold for range detect Default Value: 0
19 : 8	RANGE_LOW	Low threshold for range detect Default Value: 0
1 : 0	RANGE_COND	Range condition select. Default Value: 0 **0x0: BELOW :** DAC Value < RANGE_LOW **0x1: INSIDE :** RANGE_LOW <= DAC Value/Address < RANGE_HIGH **0x2: ABOVE :** DAC Value > RANGE_HIGH **0x3: OUTSIDE :** Dac Value < RANGE_LOW || DAC Value/Address >= RANGE_HIGH

28.1.30 DAC0_STA_RANGE_STATUS

Description: Range status register

Address: 0x42E60880

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	CHAN_RANGE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW1C						
HW Access	Reserved	RW1S						
Name	Reserved	CHAN_RANGE_STATUS [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
14 : 0	CHAN_RANGE_STATUS	Channel Range detect status: hardware sets this bit for each channel if the condition specified by the CHAN_CFG.STATUS_SEL register is met. Write with '1' to clear bit. This register does not apply to the FW Channel (Channel 15). Default Value: 0

28.1.31 DAC0_TRIM_REFBUF_OFFSET_TRIM

Description: Reference buffer trim control

Address: 0x42E60F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		REFBUF_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	REFBUF_OFFSET_TRIM	Refbuf offset trim Default Value: 0

28.1.32 DAC0_TRIM_REFBUF_SLOPE_OFFSET_TRIM

Description: Reference buffer trim control

Address: 0x42E60F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		REFBUF_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	REFBUF_SLOPE_OFF-SET_TRIM	Refbuf slope offset drift trim Default Value: 0

28.1.33 DAC0_TRIM_REFBUF_COMP_TRIM

Description: Reference buffer trim control

Address: 0x42E60F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				REFBUF_COMP_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	REFBUF_COMP_TRIM	Buffer 0 Compensation Capacitor Trim Bit<3> is not used Bits<2:0> 000 = 0.1pF 001 = 1.1pF 010 = 2.1pF 011 = 3.1pF 100 = 4.1pF 101 = 5.1pF 110 = 6.1pF 111 = 7.1pF Default Value: 0

28.1.34 DAC0_TRIM_OUTBUF_OFFSET_TRIM0

Description: Output buffer trim control

Address: 0x42E60F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		OUTBUF_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	OUTBUF_OFFSET_TRIM	Outbuf offset trim Default Value: 0

28.1.35 DAC0_TRIM_OUTBUF_SLOPE_OFFSET_TRIM0

Description: Output buffer trim control

Address: 0x42E60F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		OUTBUF_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	OUTBUF_SLOPE_OFF-SET_TRIM	Outbuf slope offset drift trim Default Value: 0

28.1.36 DAC0_TRIM_OUTBUF_COMP_TRIM0

Description: Output buffer trim control

Address: 0x42E60F1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				OUTBUF_COMP_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	OUTBUF_COMP_TRIM	see REFBUF_COMP_TRIM.REFBUF_COMP_TRIM Default Value: 0

28.1.37 DAC0_TRIM_RMP_TRIM

Description: Risk Mitigation bits

Address: 0x42E60F24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				RMP_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	RMP_TRIM	Bits <1:0> Risk mitigation for bias in reference block 0 = Bias +20% 1 = Normal Bias (Default) 2 = Normal BIas 3 = Bias -20% Bits <3:2> Risk mitigation for pump block in OA0 and OA1 0 = Normal Pump Operation for OA0 and OA1 (If pump is enabled). 1 = Reserved (Don't use!) 2 = Pumps are boosted for OA0 and OA1 (if PUMP is enabled). 3 = Reserved (Don't use!) Default Value: 1

28.1.38 SAR_SEQ_HS_DATA0

Description: SAR Sequencer High Speed Data (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_GPIO_CHAN_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW	RW		
HW Access	R				R	R		
Name	MUX0_CHAN_SEL [15:12]				RE-SERVED_0	HS_MUX_CHAN_EN_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW		RW			
HW Access	R	R	R		R			
Name	TR_SAM-PLE_-TIME_EN	SAMPLE_-TIME_EN	SAMPLE_TIME_SEL [21:20]		MUX1_CHAN_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW	RW		
HW Access	R		R		R	R		
Name	NEXT_ACTION [31:30]		CALIBRATE [29:28]		AVG_EN	AVG_CNT [26:24]		

Bits	Name	Description
31 : 30	NEXT_ACTION	Next Addr Field Default Value: Undefined **0x0: STOP :** assert SAR_DONE and SAR_EOS condition and go to idle. This action is used to indicate the end of a scan. **0x1: GO_TO_ENTRY_ADDR :** assert SAR_EOS condition and jump to Entry Addr. This action is used for continuous operation. In continuous operation, disabling the SAR (AC.SAR_EN=0) is the only mechanism available to cease SAR operation (without disabling the entire AC). **0x2: GO_TO_NEXT :** Go to next addr. This action is used to continue to a next state in a given scan. **0x3: RESERVED :**
29 : 28	CALIBRATE	Real Time Calibration Request. This signals the ADC to initiate a real-time calibration process during an ADC scan. Default Value: Undefined

28.1.38 SAR_SEQ_HS_DATA0 (continued)

		0x0: DISABLED : Calibration Disabled **0x1: OFFSET_AND_LINEARITY :** Calibrate both Offset and Linearity **0x2: OFFSET :** Callibrate Offset only **0x3: LINEARITY :** Callibrate Linearity only
27	AVG_EN	Average Enable This field is ignored if SAR_STA_CFG.CTRL.AVG_MODE=DISABLED. This field applies to all enabled channels (HS_GPIO_CHAN_EN and HS_MUX_CHAN_EN_SEL). 0 = averaging disabled 1 = averaging enabled If SAR_STA_CFG.CTRL.AVG_MODE=ACCUNDUMP, the enabled channels will be sampled, converted, and accumulated back to back (amount set by AVG_CNT). After AVG_CNT times, the accumulated results for each enabled channels are optionally shifted (set by SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.AVG_SHIFT and SAR_STA_CFG.CTRL.SHIFT_MODE). If SAR_STA_CFG.CTRL.AVG_MODE=INTERLEAVED, the enabled channels will be sampled, converted, and accumulated once per scan (amount set by AVG_CNT). After AVG_CNT scans, the accumulated results for each enabled channels are optionally shifted (set by SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.AVG_SHIFT and SAR_STA_CFG.CTRL.SHIFT_MODE). Requirements for using interleaved averaging: 1. The Entry Address state must have AVG_EN set. 2. The same value for AVG_CNT must be used across all states with AVG_EN set. 3. The AC cannot trigger the ADC with different multiple Entry Addresses (scans). 4. The SAR generates a SAR_DONE status at the end of every scan (unless confgured for continuous operation at which point only a SAR_EOS is generated), regardless of the value of AVG_CNT. If all channels in the scan are averaged, the AC can poll the SAR_RESULT or any of the SAR_(FIR)_FIFO_DONE triggers to determine when the averaged results are available. If only a subset of channels are averaged in a scan, it is up to the AC to count the number of scans to determine when the averaged results are available. Default Value: Undefined
26 : 24	AVG_CNT	Averaging Count for channels that have averaging enabled (AVG_EN). A channel will be sampled and accumulated (1<<(AVG_CNT+1)) = [2..256] times. If SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.AVG_SHIFT for an enabled channel is set, the accumulated samples are right shifted based on the value of SAR_STA_CFG.CTRL.SHIFT_MODE: SAR_STA_CFG.CTRL.SHIFT_MODE=TWELVE: After the last accumulation, the result is shifted back to 12 bits SAR_STA_CFG.CTRL.SHIFT_MODE=SIXTEEN: After the last accumulation, if avg_cnt >=32 the result will be shifted back to 16-bits, if avg_cnt < 32, no shift will be done as the result already is guaranteed to fit in 16 bits. Default Value: Undefined

28.1.38 SAR_SEQ_HS_DATA0 (continued)

23	TR_SAMPLE_TIME_EN	Trigger Sample Time Enable. This field must always remain 0. For risk mitigation purposes only: this bit only applies to the first SAR table entry pointed to by the Autonomous Controller on a trigger if additional sample time is required. When this bit is set, the sample time on this first triggered table entry is SAR_STA_CFG.TR_SAMPLE_-TIME.HS_SAMPLE_TIME. This only applies to when the table entry is first triggered. In continuous mode, when this table entry is executed again, the SAMPLE_TIME_EN/ SAMPLE_TIME_SEL will be used. Default Value: Undefined
22	SAMPLE_TIME_EN	Sample Time Enable. If this bit is set, then the start of conversion for this SAR table entry will be delayed by the sample time pointed to in SAMPLE_TIME_SEL Default Value: Undefined
21 : 20	SAMPLE_TIME_SEL	Sample Time Select. Choose from 1 of 4 available Sample Times in SAR_STA_CFG.SAMPLE_-TIME registers Default Value: Undefined
19 : 16	MUX1_CHAN_SEL	MUX1 Channel Sel (See MUX0_CHAN_SEL) (This field is not used if HS_MUX_CHAN_EN_SEL = DISABLED or MUX0_SINGLE_ENDED or MUX0_PSEUDO_DIFF) Default Value: Undefined
15 : 12	MUX0_CHAN_SEL	MUX0 Channel Sel (This field is not used if HS_MUX_CHAN_EN_SEL = DISABLED or MUX1_SINGLE_ENDED) Default Value: Undefined **0x0: MUX_CHANNEL_0 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG0 **0x1: MUX_CHANNEL_1 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG1 **0x2: MUX_CHANNEL_2 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG2 **0x3: MUX_CHANNEL_3 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG3 **0x4: MUX_CHANNEL_4 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG4 **0x5: MUX_CHANNEL_5 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG5 **0x6: MUX_CHANNEL_6 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG6 **0x7: MUX_CHANNEL_7 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG7

28.1.38 SAR_SEQ_HS_DATA0 (continued)

0x8: MUX_CHANNEL_8 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG8

0x9: MUX_CHANNEL_9 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG9

0xa: MUX_CHANNEL_10 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG10

0xb: MUX_CHANNEL_11 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG11

0xc: MUX_CHANNEL_12 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG12

0xd: MUX_CHANNEL_13 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG13

0xe: MUX_CHANNEL_14 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG14

0xf: MUX_CHANNEL_15 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG15

11	RESERVED_0	Default Value: Undefined
10 : 8	HS_MUX_CHAN_EN_-SEL	Enable and Selection for HS Muxed SAR Channels Default Value: Undefined

0x0: DISABLED :

Disabled

0x1: MUX0_SINGLE_ENDED :

One Single Ended Conversion (configured by MUX0_CHAN_SEL)

0x2: MUX1_SINGLE_ENDED :

One Single Ended Conversion (configured by MUX1_CHAN_SEL)

0x3: MUX0_AND_MUX1_SINGLE_ENDED :

Two Simultaneously Sampled Single Ended Conversions (configured by MUX0_CHAN_SEL and MUX1_CHAN_SEL)

0x4: MUX0_PSEUDO_DIFF :

One Pseudo differential conversion (configured by MUX0_CHAN_SEL)

28.1.38 SAR_SEQ_HS_DATA0 (continued)

0x5: RESERVED_0 :

0x6: RESERVED_1 :

0x7: RESERVED_2 :

7 : 0	HS_GPIO_CHAN_EN	Enables for HS GPIO SAR Channels For each bit in this field: 0- HS GPIO SAR Channel is disabled 1- HS GPIO SAR Channel is enabled [0]: Channel 0, configured by SAR_STA_CFG.GPIO_CHAN_CFG0 [1]: Channel 1, configured by SAR_STA_CFG.GPIO_CHAN_CFG1 [2]: Channel 2, configured by SAR_STA_CFG.GPIO_CHAN_CFG2 [3]: Channel 3, configured by SAR_STA_CFG.GPIO_CHAN_CFG3 [4]: Channel 4, configured by SAR_STA_CFG.GPIO_CHAN_CFG4 [5]: Channel 5, configured by SAR_STA_CFG.GPIO_CHAN_CFG5 [6]: Channel 6, configured by SAR_STA_CFG.GPIO_CHAN_CFG6 [7]: Channel 7, configured by SAR_STA_CFG.GPIO_CHAN_CFG7 Default Value: Undefined

28.1.39 SAR_SEQ_LP_DATA0

Description: SAR Sequencer Low Power Data (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							RW
HW Access	R							R
Name	RESERVED_1 [7:1]							LP_CHAN_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	CHAN_SEL [15:12]				RESERVED_1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW		RW			
HW Access	R	R	R		R			
Name	TR_SAM-PLE_-TIME_EN	SAMPLE_-TIME_EN	SAMPLE_TIME_SEL [21:20]		RESERVED_2 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW	RW		
HW Access	R		R		R	R		
Name	NEXT_ACTION [31:30]		CALIBRATE [29:28]		AVG_EN	AVG_CNT [26:24]		

Bits	Name	Description
31 : 30	NEXT_ACTION	Next Addr Field Default Value: Undefined **0x0: STOP :** assert SAR_DONE and SAR_EOS condition and go to idle. This action is used to indicate the end of a scan. **0x1: GO_TO_ENTRY_ADDR :** assert SAR_EOS condition and jump to Entry Addr. This action is used for continuous operation. In continuous operation, disabling the SAR (AC.SAR_EN=0) is the only mechanism available to cease SAR operation (without disabling the entire AC). **0x2: GO_TO_NEXT :** Go to next addr. This action is used to continue to a next state in a given scan. **0x3: RESERVED :**
29 : 28	CALIBRATE	Real Time Calibration Request. This signals the ADC to initiate a real-time calibration process during an ADC scan. Default Value: Undefined

28.1.39 SAR_SEQ_LP_DATA0 (continued)

		0x0: DISABLED : Calibration Disabled **0x1: OFFSET_AND_LINEARITY :** Calibrate both Offset and Linearity **0x2: OFFSET :** Callibrate Offset only **0x3: LINEARITY :** Callibrate Linearity only
27	AVG_EN	Average Enable This field is ignored if SAR_STA_CFG.CTRL.AVG_MODE=DISABLED. This field applies to all enabled channels (HS_GPIO_CHAN_EN and HS_MUX_CHAN_EN_SEL). 0 = averaging disabled 1 = averaging enabled If SAR_STA_CFG.CTRL.AVG_MODE=ACCUNDUMP, the enabled channels will be sampled, converted, and accumulated back to back (amount set by AVG_CNT). After AVG_CNT times, the accumulated results for each enabled channels are optionally shifted (set by SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.AVG_SHIFT and SAR_STA_CFG.CTRL.SHIFT_MODE). If SAR_STA_CFG.CTRL.AVG_MODE=INTERLEAVED, the enabled channels will be sampled, converted, and accumulated once per scan (amount set by AVG_CNT). After AVG_CNT scans, the accumulated results for each enabled channels are optionally shifted (set by SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.AVG_SHIFT and SAR_STA_CFG.CTRL.SHIFT_MODE). Requirements for using interleaved averaging: 1. The Entry Address state must have AVG_EN set. 2. The same value for AVG_CNT must be used across all states with AVG_EN set. 3. The AC cannot trigger the ADC with different multiple Entry Addresses (scans). 4. The SAR generates a SAR_DONE status at the end of every scan (unless confgured for continuous operation at which point only a SAR_EOS is generated), regardless of the value of AVG_CNT. If all channels in the scan are averaged, the AC can poll the SAR_RESULT or any of the SAR_(FIR)_FIFO_DONE triggers to determine when the averaged results are available. If only a subset of channels are averaged in a scan, it is up to the AC to count the number of scans to determine when the averaged results are available. Default Value: Undefined
26 : 24	AVG_CNT	Averaging Count for channels that have averaging enabled (AVG_EN). A channel will be sampled and accumulated (1<<(AVG_CNT+1)) = [2..256] times. If SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.AVG_SHIFT for an enabled channel is set, the accumulated samples are right shifted based on the value of SAR_STA_CFG.CTRL.SHIFT_MODE: SAR_STA_CFG.CTRL.SHIFT_MODE=TWELVE: After the last accumulation, the result is shifted back to 12 bits SAR_STA_CFG.CTRL.SHIFT_MODE=SIXTEEN: After the last accumulation, if avg_cnt >=32 the result will be shifted back to 16-bits, if avg_cnt < 32, no shift will be done as the result already is guaranteed to fit in 16 bits. Default Value: Undefined

28.1.39 SAR_SEQ_LP_DATA0 (continued)

23	TR_SAMPLE_TIME_EN	Trigger Sample Time Enable. This field must always remain 0. For risk mitigation purposes only: this bit only applies to the first SAR table entry pointed to by the Autonomous Controller on a trigger if additional sample time is required. When this bit is set, the sample time on this first triggered table entry is SAR_STA_CFG.TR_SAMPLE_-TIME.LP_SAMPLE_TIME. This only applies to when the table entry is first triggered. In continuous mode, when this table entry is executed again, the SAMPLE_TIME_EN/ SAMPLE_TIME_SEL will be used. Default Value: Undefined
22	SAMPLE_TIME_EN	Sample Time Enable. If this bit is set, then the start of conversion for this SAR table entry will be delayed by the sample time pointed to in SAMPLE_TIME_SEL Default Value: Undefined
21 : 20	SAMPLE_TIME_SEL	Sample Time Select. Choose from 1 of 4 available Sample Times for the static config Default Value: Undefined
19 : 16	RESERVED_2	Default Value: Undefined
15 : 12	CHAN_SEL	LP Channel Select Default Value: Undefined **0x0: MUX_CHANNEL_0 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG0 **0x1: MUX_CHANNEL_1 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG1 **0x2: MUX_CHANNEL_2 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG2 **0x3: MUX_CHANNEL_3 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG3 **0x4: MUX_CHANNEL_4 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG4 **0x5: MUX_CHANNEL_5 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG5 **0x6: MUX_CHANNEL_6 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG6 **0x7: MUX_CHANNEL_7 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG7 **0x8: MUX_CHANNEL_8 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG8 **0x9: MUX_CHANNEL_9 :** mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG9

28.1.39 SAR_SEQ_LP_DATA0 (continued)

0xa: MUX_CHANNEL_10 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG10

0xb: MUX_CHANNEL_11 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG11

0xc: MUX_CHANNEL_12 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG12

0xd: MUX_CHANNEL_13 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG13

0xe: MUX_CHANNEL_14 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG14

0xf: MUX_CHANNEL_15 :

mux configured by settings in SAR_STA_CFG.MUX_CHAN_CFG15

11 : 1	RESERVED_1	Default Value: Undefined
0	LP_CHAN_EN	LP Channel Enable Default Value: Undefined

28.1.40 SAR_STA_CTRL

Description: SAR Control register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			Reserved	RW		
HW Access	R	R			Reserved	R		
Name	LP_DIFFERENTIAL_EN	LP_VREF_SEL [6:4]			Reserved	HS_VREF_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	BUF1_PWR_MODE [15:12]				BUF0_PWR_MODE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	LP_SAR_PWR_MODE [23:22]		SHIFT_MODE	CHAN_ID_EN	STARTUP_CAL_EN [19:18]		AVG_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
23 : 22	LP_SAR_PWR_MODE	Request to disable Channel Buffer after sampling is done and SAR Macro after conversion is done. (Valid only in LP mode). Default Value: 0 **0x0: DISABLED :** Buffer and Core are not disabled **0x1: BUFFER_AND_CORE :** Disable both Buffer and Core **0x2: BUFFER :** Disable Buffer only **0x3: CORE :** Disable Core only
21	SHIFT_MODE	If GPIO(MUX)_CHAN_CFG.AVG_SHIFT is enabled for a given channel, shift the result to support 12 or 16-bit resolutions. This field does not impact FIR outputs. Default Value: 0

28.1.40 SAR_STA_CTRL (continued)

0x0: TWELVE :

TWELVE: After the last accumulation, the result is shifted back to 12 bits

0x1: SIXTEEN :

SIXTEEN: After the last accumulation, if SEQ_HS(LP)_DATA.AVG_CNT >=32 the result will be shifted back to 16-bits, if SEQ_HS(LP)_DATA.AVG_CNT < 32, no shift will be done as the result already is guaranteed to fit in 16 bits.

20	CHAN_ID_EN	Channel Number Identifier Enable Default Value: 0

0x0: DISABLED :

Data stored in FIFO (selected by GPIO_CHAN_CFG.FIFO_SEL or MUX_CHAN_CFG.FIFO_-SEL) does not include Channel Number Identifier. FIFO data is SAR result sign extended to 32-bits.

0x1: ENABLED :

Data stored in FIFO (selected by GPIO_CHAN_CFG.FIFO_SEL ot MUX_CHAN_CFG.FIFO_-SEL) does include Channel Number Identifier. MSB of FIFO data ([31:24]) is defined as follows:
[27:24]: GPIO Channel Number (Valid numbers are 0-7)
[31:28]: Mux Channel Number (Valid numbers are 0-15)
SAR result sign extended to 24-bits.
NOTE: FIR data that is written to a FIFO does not have an associated channel ID as the data can be up to 32-bits. FIR data should always be written to dedicated FIFOs.

19 : 18	STARTUP_CAL_EN	Startup calibration request This field is used to request a calibration process whenever the SAR is powered up (i.e. when AC.SAR.EN toggles from 0 to 1). Default Value: 0

0x0: DISABLED :

Startup calibration Disabled

0x1: OFFSET_AND_LINEARITY :

calibrate both Offset and Linearity

0x2: OFFSET :

callibrate Offset only

0x3: LINEARITY :

callibrate Linearity only

17 : 16	AVG_MODE	Averaging mode applied to all channels in a scan where averaging is enabled Default Value: 0

0x0: DISABLED :

Disabled

28.1.40 SAR_STA_CTRL (continued)

0x1: ACCUNDUMP :

Accumulate and Dump (1st order accumulate and dump filter): enabled channels for a given SEQ_HS(LP)_DATA state with AVG_EN set will be accumulated back to back and optionally shifted (if GPIO(MUX)_CHAN_CFG.SHIFT_EN is set). The number of accumulations is set by SEQ_HS(LP)_DATA.AVG_CNT.

0x2: RESERVED_0 :

0x3: RESERVED_1 :

15 : 12	BUF1_PWR_MODE	Output buffer power level: see description of BUF0_PWR_MODE Default Value: 0
11 : 8	BUF0_PWR_MODE	Buffer zero power level Default Value: 0

0x0: OFF :

Off

0x1: ULTRA_LOW :

Buffer quiscent current of 15uA, input common mode of 0.2V to VDDA-1V, gain bandwidth 30kHz

0x2: ULTRA_LOW_RAIL :

Buffer quiscent current of 35uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth 30kHz

0x3: LOW :

Do Not Use

0x4: LOW_RAIL :

Buffer quiscent current of 150uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth 350kHz

0x5: MEDIUM :

Do Not Use

0x6: MEDIUM_RAIL :

Buffer quiscent current of 200uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth 700kHz

0x7: HIGH :

Do Not Use

0x8: HIGH_RAIL :

Buffer quiscent current of 600uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth 1.75MHz

28.1.40 SAR_STA_CTRL (continued)

		0x9: ULTRA_HIGH : Do Not Use **0xa: ULTRA_HIGH_RAIL :** Buffer quiscent current of 800uA, input common mode of 0.2V to VDDA-0.2V, gain bandwidth 2.8MHz **0xb: RESERVED_0 :** **0xc: RESERVED_1 :** **0xd: RESERVED_2 :** **0xe: RESERVED_3 :** **0xf: RESERVED_4 :**
7	LP_DIFFERENTIAL_EN	Low Power Differential Enable This field is only used for LP mode and is applied to all Mux Channels. Default Value: 1 **0x0: DISABLED :** Single ended operation (MUX_CHAN_CFG[X].NEG_PIN_SEL and MUX-_CHAN_CFG[X].NEG_COEFF_SEL are ignored) **0x1: ENABLED :** Differential operation MUX_CHAN_CFG[X].NEG_PIN_SEL and MUX-_CHAN_CFG[X].NEG_COEFF_SEL are used.
6 : 4	LP_VREF_SEL	See HS_VREF_SEL Default Value: 0
2 : 0	HS_VREF_SEL	ADC Core VREF selection Default Value: 0 **0x0: VDDA :** VREF set to VDDA. The internal reference buffer is off, and an external capacitor is not used. **0x1: VREF_EXT :** VREF set to external reference (provided through GPIO). The internal reference buffer is off, and an external capacitor is optional. **0x2: VBGR :** VREF set to internal bandgap reference. The internal reference buffer is on, and an external capacitor is mandatory for HS mode and optional for LP mode. **0x3: VDDA_BY_2 :** VREF set to internal VDDA divider (VDDA/2). The internal reference buffer is on, and an external capacitor is not mandatory for HS mode and optional for LP mode.

28.1.40 SAR_STA_CTRL (continued)

0x4: PRB_VREF0 :

VREF set to internal PRB Reference 0. The internal reference buffer is on, and an external capacitor is mandatory for both HS and LP modes.

0x5: PRB_VREF1 :

VREF set to internal PRB Reference 0. The internal reference buffer is on, and an external capacitor is mandatory for both HS and LP modes.

0x6: RESERVED_0 :

0x7: RESERVED_1 :

28.1.41 SAR_STA_FIR_CFG0

Description: FIR Configuration register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			CHANNEL_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [15:14]		TAP_SEL [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW	RW			
HW Access	Reserved			R	R			
Name	Reserved [23:21]			WAIT_TAP_INIT	SHIFT_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				Reserved	RW		
HW Access	R				Reserved	R		
Name	FIFO_SEL [31:28]				Reserved	STATUS_SEL [26:24]		

Bits	Name	Description
31 : 28	FIFO_SEL	FIFO selections. Select 1 of the 8 for FIFO data storage The FIFO must be configured to support the number of desired FIFOs (LPPASS_MMIO.FIFO_STA_CFG.CFG.SEL) Default Value: 0 **0x0: DISABLED :** **0x1: FIFO_0 :** **0x2: FIFO_1 :** **0x3: FIFO_2 :** **0x4: FIFO_3 :** **0x5: FIFO_4 :** **0x6: FIFO_5 :** **0x7: FIFO_6 :** **0x8: FIFO_7 :**

28.1.41 SAR_STA_FIR_CFG0 (continued)

		0x9: RESERVED_0 :
		0xa: RESERVED_1 :
		0xb: RESERVED_2 :
		0xc: RESERVED_3 :
		0xd: RESERVED_4 :
		0xe: RESERVED_5 :
		0xf: RESERVED_6 :
26 : 24	STATUS_SEL	Status selections. Default Value: 0
		0x0: DISABLED :
		0x1: STATUS_STRUCT_0 :
		0x2: STATUS_STRUCT_1 :
		0x3: STATUS_STRUCT_2 :
		0x4: STATUS_STRUCT_3 :
		0x5: RESERVED_0 :
		0x6: RESERVED_1 :
		0x7: RESERVED_2 :
20	WAIT_TAP_INIT	Wait for TAP_SEL number before outputing the first valid data Default Value: 1
		0x0: DISABLED :
		The FIR will produce a SAR_FIR0(1)_DONE trigger after every update (regardless of the number of filled taps)
		0x1: ENABLED :
		The FIR will wait for TAP_SEL+1 locations to be filled prior to producing a SAR_FIR0(1)_DONE trigger.
19 : 16	SHIFT_SEL	FIR Shift Select Shift the FIR output right by the number in this field Default Value: 0
13 : 8	TAP_SEL	FIR Tap Select FIR Tap Select = TAP_SEL+1, range 1..64 Default Value: 0

28.1.41 SAR_STA_FIR_CFG0 (continued)

4 : 0	CHANNEL_SEL	Channel selection for FIR input The FIR input data is the final output of the selected channel (i.e. if a channel is configured for averaging, the FIR will only receive the final averaged value (no intermediate accumulated values are sent to the FIR)). Default Value: 0 **0x0: DISABLED :** **0x1: GPIO_CHANNEL_0 :** **0x2: GPIO_CHANNEL_1 :** **0x3: GPIO_CHANNEL_2 :** **0x4: GPIO_CHANNEL_3 :** **0x5: GPIO_CHANNEL_4 :** **0x6: GPIO_CHANNEL_5 :** **0x7: GPIO_CHANNEL_6 :** **0x8: GPIO_CHANNEL_7 :** **0x9: MUX_CHANNEL_0 :** **0xa: MUX_CHANNEL_1 :** **0xb: MUX_CHANNEL_2 :** **0xc: MUX_CHANNEL_3 :** **0xd: MUX_CHANNEL_4 :** **0xe: MUX_CHANNEL_5 :** **0xf: MUX_CHANNEL_6 :** **0x10: MUX_CHANNEL_7 :** **0x11: MUX_CHANNEL_8 :** **0x12: MUX_CHANNEL_9 :** **0x13: MUX_CHANNEL_10 :** **0x14: MUX_CHANNEL_11 :** **0x15: MUX_CHANNEL_12 :** **0x16: MUX_CHANNEL_13 :**

28.1.41 SAR_STA_FIR_CFG0 (continued)

0x17: MUX_CHANNEL_14 :

0x18: MUX_CHANNEL_15 :

0x19: RESERVED_0 :

0x1a: RESERVED_1 :

0x1b: RESERVED_2 :

0x1c: RESERVED_3 :

0x1d: RESERVED_4 :

0x1e: RESERVED_5 :

0x1f: RESERVED_6 :

28.1.42 SAR_STA_TR_SAMPLE_TIME

Description: SAR Trigger Sample Time (Risk Mitigation Only)

Address: 0x42E80418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_TR_SAMPLE_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						HS_TR_SAMPLE_TIME [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LP_TR_SAMPLE_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [31:26]						LP_TR_SAMPLE_TIME [25:24]	

Bits	Name	Description
25 : 16	LP_TR_SAMPLE_TIME	Low Power (LP) Trigger Sample Time This field is for risk mitigation purposes only. This field is only applicable if TR_SAMPLE_TIME_EN is set by the Entry Address pointed to by the Autonomous Controller. LP_TR_SAMPLE_TIME sets the number of LP clock cycles to allow for sampling. Entry Address Sample Time = LP_TR_SAMPLE_TIME+1, range 1..1024 Default Value: 5
9 : 0	HS_TR_SAMPLE_TIME	High Speed (HS) Trigger Sample Time This field is for risk mitigation purposes only. This field is only applicable if TR_SAMPLE_TIME_EN is set by the Entry Address pointed to by the Autonomous Controller. HS_TR_SAMPLE_TIME sets the number of HS clock cycles to allow for sampling of the first address (Entry Address) of a scan. Entry Address Sample Time = HS_TR_SAMPLE_TIME+1, range 1..1024 Default Value: 31

28.1.43 SAR_STA_SAMPLE_TIME0

Description: Sample control register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_SAMPLE_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						HS_SAMPLE_TIME [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LP_SAMPLE_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [31:26]						LP_SAMPLE_TIME [25:24]	

Bits	Name	Description
25 : 16	LP_SAMPLE_TIME	Sample time (aperture) in LP clock cycles (4MHz). Sample time = SAMPLE_TIME+1, range 1..1024 Default Value: 5
9 : 0	HS_SAMPLE_TIME	Sample time (aperture) in HS clock cycles (nominally 80MHz). Sample time = SAMPLE_TIME+1, range 1..1024 Default Value: 31

28.1.44 SAR_STA_GPIO_CHAN_CFG0

Description: High Speed GPIO Channel configuration register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	RW	Reserved		RW		
HW Access	Reserved	R	R	Reserved		R		
Name	Reserved	SIGNED	HS_DIF-FEREN-TIAL_EN	Reserved [4:3]		POS_PIN [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved	RW			RW			
HW Access	Reserved	R			R			
Name	Reserved	NEG_PIN [14:12]			POS_COEFF_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	Reserved		
HW Access	R				R	Reserved		
Name	NEG_COEFF_SEL [23:20]				AVG_SHIFT	Reserved [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW				Reserved	RW		
HW Access	R				Reserved	R		
Name	FIFO_SEL [31:28]				Reserved	STATUS_SEL [26:24]		

Bits	Name	Description
31 : 28	FIFO_SEL	FIFO selections. Select 1 of the 8 for FIFO data storage The FIFO must be configured to support the number of desired FIFOs (LPPASS_MMIO.FI-FO_STA_CFG.CFG.SEL) Default Value: 0 **0x0: DISABLED :** **0x1: FIFO_0 :** **0x2: FIFO_1 :** **0x3: FIFO_2 :** **0x4: FIFO_3 :** **0x5: FIFO_4 :** **0x6: FIFO_5 :** **0x7: FIFO_6 :**

28.1.44 SAR_STA_GPIO_CHAN_CFG0 (continued)

		0x8: FIFO_7 :
		0x9: RESERVED_0 :
		0xa: RESERVED_1 :
		0xb: RESERVED_2 :
		0xc: RESERVED_3 :
		0xd: RESERVED_4 :
		0xe: RESERVED_5 :
		0xf: RESERVED_6 :
26 : 24	STATUS_SEL	Status selections. Default Value: 0
		0x0: DISABLED :
		0x1: STATUS_STRUCT_0 :
		0x2: STATUS_STRUCT_1 :
		0x3: STATUS_STRUCT_2 :
		0x4: STATUS_STRUCT_3 :
		0x5: RESERVED_0 :
		0x6: RESERVED_1 :
		0x7: RESERVED_2 :
23 : 20	NEG_COEFF_SEL	See POS_COEFF_SEL Valid only in HS mode & HS_DIFFERENTIAL_EN enabled Default Value: 0
19	AVG_SHIFT	Average Shift Enable This field is only valid if the following conditions are met: Averaging is configured for accumulate and dump or interleaved: CTRL.AVG_MODE=1,2 Averaging is enabled for particular state in the sequence table: SEQ_HS_DATA.AVG_EN=1 The amount of shifting is set by CTRL.SHIFT_MODE. Default Value: 0
14 : 12	NEG_PIN	Negative Input Assignment see POS_PIN Valid only in HS mode & HS_DIFFERENTIAL_EN enabled Default Value: 0
11 : 8	POS_COEFF_SEL	Positive Input Coefficient Select Default Value: 0
		0x0: DISABLED :
		0x1: CHAN_COEFF0 :

28.1.44 SAR_STA_GPIO_CHAN_CFG0 (continued)

		0x2: CHAN_COEFF1 : **0x3: CHAN_COEFF2 :** **0x4: CHAN_COEFF3 :** **0x5: CHAN_COEFF4 :** **0x6: CHAN_COEFF5 :** **0x7: CHAN_COEFF6 :** **0x8: CHAN_COEFF7 :** **0x9: RESERVED_0 :** **0xa: RESERVED_1 :** **0xb: RESERVED_2 :** **0xc: RESERVED_3 :** **0xd: RESERVED_4 :** **0xe: RESERVED_5 :** **0xf: RESERVED_6 :**
6	SIGNED	Output data as a signed value Default Value: 0 **0x0: UNSIGNED :** Default: result data is unsigned (zero extended if needed) **0x1: SIGNED :** result data is signed (sign extended if needed)
5	HS_DIFFERENTIAL_EN	High Speed Differential Enable Default Value: 0 **0x0: DISABLED :** Channel configured for single ended operation (NEG_PIN_SEL and NEG_COEFF_SEL are ignored) **0x1: ENABLED :** Channel configured for pseudo differential operation (NEG_PIN_SEL and NEG_COEFF_SEL are used)
2 : 0	POS_PIN	Positive Input Assignment Default Value: 0

28.1.44 SAR_STA_GPIO_CHAN_CFG0 (continued)

0x0: P0 :

SAR/PTC GPIO Pin 0. See product datasheet for specific pin number.

0x1: P1 :

SAR/PTC GPIO Pin 1. See product datasheet for specific pin number.

0x2: P2 :

SAR/PTC GPIO Pin 2. See product datasheet for specific pin number.

0x3: P3 :

SAR/PTC GPIO Pin 3. See product datasheet for specific pin number.

0x4: P4 :

SAR/PTC GPIO Pin 4. See product datasheet for specific pin number.

0x5: P5 :

SAR/PTC GPIO Pin 5. See product datasheet for specific pin number.

0x6: P6 :

SAR/PTC GPIO Pin 6. See product datasheet for specific pin number.

0x7: P7 :

SAR/PTC GPIO Pin 7. See product datasheet for specific pin number.

28.1.45 SAR_STA_MUX_CHAN_CFG0

Description: High Speed / Low Power Muxed Channel configuration register (Channel 0 routing is used for default routing (i.e. when the SAR gets enabled) (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved	RW	Reserved	RW				
HW Access	Reserved	R	Reserved	R				
Name	Reserved	SIGNED	Reserved	POS_MUX_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	NEG_MUX_SEL [15:12]				POS_COEFF_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	RW	Reserved	RW
HW Access	R				R	R	Reserved	R
Name	NEG_COEFF_SEL [23:20]				AVG_SHIFT	BUF_BY-PASS	Reserved	NEG_MUX-_SEL

Bits	31	30	29	28	27	26	25	24
SW Access	RW				Reserved	RW		
HW Access	R				Reserved	R		
Name	FIFO_SEL [31:28]				Reserved	STATUS_SEL [26:24]		

Bits	Name	Description
31 : 28	FIFO_SEL	FIFO selections. Select 1 of the 8 for FIFO data storage The FIFO must be configured to support the number of desired FIFOs (LPPASS_MMIO.FI-FO_STA_CFG.CFG.SEL) Default Value: 0 **0x0: DISABLED :** **0x1: FIFO_0 :** **0x2: FIFO_1 :** **0x3: FIFO_2 :** **0x4: FIFO_3 :** **0x5: FIFO_4 :** **0x6: FIFO_5 :** **0x7: FIFO_6 :**

28.1.45 SAR_STA_MUX_CHAN_CFG0 (continued)

		0x8: FIFO_7 :
		0x9: RESERVED_0 :
		0xa: RESERVED_1 :
		0xb: RESERVED_2 :
		0xc: RESERVED_3 :
		0xd: RESERVED_4 :
		0xe: RESERVED_5 :
		0xf: RESERVED_6 :
26 : 24	STATUS_SEL	Status selections Default Value: 0
		0x0: DISABLED :
		0x1: STATUS_STRUCT_0 :
		0x2: STATUS_STRUCT_1 :
		0x3: STATUS_STRUCT_2 :
		0x4: STATUS_STRUCT_3 :
		0x5: RESERVED_0 :
		0x6: RESERVED_1 :
		0x7: RESERVED_2 :
23 : 20	NEG_COEFF_SEL	See POS_COEFF_SEL. Valid only when SEQ_HS_DATA.MUX0_PSEUDO_DIFF enabled in HS mode Default Value: 0
19	AVG_SHIFT	Average Shift Enable This field is only valid if the following conditions are met: Averaging is configured for accumulate and dump or interleaved: CTRL.AVG_MODE=1,2 Averaging is enabled for particular state in the sequence table: SEQ_HS(LP)_DATA.AVG_EN=1 The amount of shifting is set by CTRL.SHIFT_MODE. Default Value: 0
18	BUF_BYPASS	Channel Buffer bypass Default Value: 0
		0x0: DISABLED :
		Buffered bypass disabled
		0x1: ENABLED :
		Buffered bypass enabled

28.1.45 SAR_STA_MUX_CHAN_CFG0 (continued)

16 : 12	NEG_MUX_SEL	Negative Mux Select See POS_MUX_SEL. Valid only in LP mode and when SEQ_HS_DATA.MUX0_PSEUDO_DIFF enabled in HS mode Default Value: 0
11 : 8	POS_COEFF_SEL	Positive Input Coefficient Select Default Value: 0 **0x0: DISABLED :** **0x1: CHAN_COEFF0 :** **0x2: CHAN_COEFF1 :** **0x3: CHAN_COEFF2 :** **0x4: CHAN_COEFF3 :** **0x5: CHAN_COEFF4 :** **0x6: CHAN_COEFF5 :** **0x7: CHAN_COEFF6 :** **0x8: CHAN_COEFF7 :** **0x9: RESERVED_0 :** **0xa: RESERVED_1 :** **0xb: RESERVED_2 :** **0xc: RESERVED_3 :** **0xd: RESERVED_4 :** **0xe: RESERVED_5 :** **0xf: RESERVED_6 :**
6	SIGNED	Output data as a signed value Default Value: 0 **0x0: UNSIGNED :** Default: result data is unsigned (zero extended if needed) **0x1: SIGNED :** result data is signed (sign extended if needed)
4 : 0	POS_MUX_SEL	Positive Mux Select Default Value: 0

28.1.45 SAR_STA_MUX_CHAN_CFG0 (continued)

0x0: COREIO_0 :

CTBL0 GPIO Pin 1. See product datasheet for specific pin number.

0x1: COREIO_1 :

CTBL0 GPIO Pin 4. See product datasheet for specific pin number.

0x2: COREIO_2 :

CTBL0 GPIO Pin 6. See product datasheet for specific pin number.

0x3: COREIO_3 :

CTBL0 GPIO Pin 7. See product datasheet for specific pin number.

0x4: COREIO_4 :

CTBL1 GPIO Pin 1. See product datasheet for specific pin number.

0x5: COREIO_5 :

CTBL1 GPIO Pin 4. See product datasheet for specific pin number.

0x6: COREIO_6 :

CTBL1 GPIO Pin 6. See product datasheet for specific pin number.

0x7: COREIO_7 :

CTBL1 GPIO Pin 7. See product datasheet for specific pin number.

0x8: CTBL0_OA0 :

CTBL0 Opamp0 Output

0x9: CTBL0_OA1 :

CTBL0 Opamp1 Output

0xa: CTBL1_OA0 :

CTBL1 Opamp0 Output

0xb: CTBL1_OA1 :

CTBL1 Opamp1 Output

0xc: VREF0 :

DAC0 output

0xd: VREF1 :

DAC1 output

28.1.45 SAR_STA_MUX_CHAN_CFG0 (continued)

0xe: TEMP_SENSOR :

Temperature Sensor

0xf: GPIO_0 :

SAR/PTC GPIO Pin 0. See product datasheet for specific pin number.

0x10: GPIO_1 :

SAR/PTC GPIO Pin 1. See product datasheet for specific pin number.

0x11: GPIO_2 :

SAR/PTC GPIO Pin 2. See product datasheet for specific pin number.

0x12: GPIO_3 :

SAR/PTC GPIO Pin 3. See product datasheet for specific pin number.

0x13: GPIO_4 :

SAR/PTC GPIO Pin 4. See product datasheet for specific pin number.

0x14: GPIO_5 :

SAR/PTC GPIO Pin 5. See product datasheet for specific pin number.

0x15: GPIO_6 :

SAR/PTC GPIO Pin 6. See product datasheet for specific pin number.

0x16: GPIO_7 :

SAR/PTC GPIO Pin 7. See product datasheet for specific pin number.

0x17: AMUXBUS_A :

Do Not Use

0x18: AMUXBUS_B :

Do Not Use

0x19: VSSA_KELVIN :

SAR Ground

0x1a: RESEREVED_0 :

0x1b: RESEREVED_1 :

0x1c: RESEREVED_2 :

0x1d: RESEREVED_3 :

28.1.45 SAR_STA_MUX_CHAN_CFG0 (continued)

0x1e: RESEREVED_4 :

0x1f: RESEREVED_5 :

28.1.46 SAR_STA_STATUS_CFG0

Description: Global range detect mode register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80490

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						RANGE_COND [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	RANGE_COND	Range condition select. Default Value: 0 **0x0: BELOW :** result < RANGE_LOW **0x1: INSIDE :** RANGE_LOW <= result < RANGE_HIGH **0x2: ABOVE :** result > RANGE_HIGH **0x3: OUTSIDE :** result < RANGE_LOW || result >= RANGE_HIGH

28.1.47 SAR_STA_STATUS_RANGE_LOW0

Description: Global range detect low value register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E804A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [31:24]							

Bits	Name	Description
31 : 0	RANGE_LOW	Low threshold for range detect Default Value: 0

28.1.48 SAR_STA_STATUS_RANGE_HIGH0

Description: Global range detect high value register (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E804B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [31:24]							

Bits	Name	Description
31 : 0	RANGE_HIGH	High threshold for range detect Default Value: 0

28.1.49 SAR_STA_GPIO_CHAN_RESULT0

Description: High Speed GPIO Channel result register

Address: 0x42E804C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	RESULT [31:24]							

Bits	Name	Description
31 : 0	RESULT	SAR conversion channel result data of the channel. The data is written here if the corresponding bit in CHAN_RESULT_MASK.GPIO_CHAN_RESULT_MASK is set. Default Value: Undefined

28.1.50 SAR_STA_MUX_CHAN_RESULT0

Description: High Speed / Low Power Muxed Channel result register

Address: 0x42E804E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	RESULT [31:24]							

Bits	Name	Description
31 : 0	RESULT	SAR conversion channel result data of the channel. The data is written here if the corresponding bit in CHAN_RESULT_MASK.MUX_CHAN_RESULT_MASK is set. Default Value: Undefined

28.1.51 SAR_STA_FIR_RESULT0

Description: FIR result register

Address: 0x42E80520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	RESULT [31:24]							

Bits	Name	Description
31 : 0	RESULT	FIR output data. The data is written here if the corresponding bit in FIR_RESULT_MASK.FIR_RESULT_MASK is set. Default Value: Undefined

28.1.52 SAR_STA_CHAN_RESULT_MASK

Description: Channel result mask (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80530

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	GPIO_CHAN_RESULT_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MUX_CHAN_RESULT_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MUX_CHAN_RESULT_MASK [31:24]							

Bits	Name	Description
31 : 16	MUX_CHAN_RESULT_MASK	If set the MUX_CHAN_RESULT.RESULT register will be used to store SAR conversion data and an EOS will be generated at the end of a scan that includes the MUX channel. If this bit isn't set, the channel must be configured to store the result in a FIFO. (Default is for all result registers to be used). Default Value: 0xFFFF
7 : 0	GPIO_CHAN_RESULT_MASK	If set, the GPIO_CHAN_RESULT.RESULT register will be used to store SAR conversion data and an EOS will be generated at the end of a scan that includes the MUX channel. If this bit isn't set, the channel must be configured to store the result in a FIFO. (Default is for all result registers to be used). Default Value: 0xFF

28.1.53 SAR_STA_FIR_RESULT_MASK

Description: FIR result mask (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80534

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						FIR_RESULT_MASK [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	FIR_RESULT_MASK	If set, the FIR_RESULT.RESULT register will be used to store FIR outputs. If this bit isn't set, the FIR must be configured to store the result in a FIFO. (Default is for the FIR result registers to be used). Default Value: 3

28.1.54 SAR_STA_CHAN_RESULT_UPDATED

Description: Channel result register status

Address: 0x42E80538

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	GPIO_CHAN_RESULT_UPDATED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW1S							
Name	MUX_CHAN_RESULT_UPDATED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW1S							
Name	MUX_CHAN_RESULT_UPDATED [31:24]							

Bits	Name	Description
31 : 16	MUX_CHAN_RESULT_UPDATED	If set the corresponding MUX_CHAN_RESULT.RESULT register was updated, i.e. was sampled during the previous scan and, in case of Interleaved averaging, reached the averaging count. If this bit is low then either the channel is not enabled or the averaging count is not yet reached for Interleaved averaging. Write 1 to clear. Default Value: 0
7 : 0	GPIO_CHAN_RESULT_UPDATED	If set the corresponding GPIO_CHAN_RESULT.RESULT register was updated, i.e. was sampled during the previous scan and, in case of Interleaved averaging, reached the averaging count. If this bit is low then either the channel is not enabled or the averaging count is not yet reached for Interleaved averaging. Write 1 to clear. Default Value: 0

28.1.55 SAR_STA_FIR_RESULT_UPDATED

Description: FIR result register status

Address: 0x42E8053C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1C	
HW Access	Reserved						RW1S	
Name	Reserved [7:2]						FIR_RESULT_UPDATED [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	FIR_RESULT_UPDATED	If set the corresponding FIR_RESULT.RESULT register was updated. If this bit is low then either the FIR is not enabled or the FIR output is not yet available. Write 1 to clear. Default Value: 0

28.1.56 SAR_STA_STATUS

Description: SAR status register

Address: 0x42E80540

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	BUSY	Reserved [30:24]						

Bits	Name	Description
31	BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS (i.e. the last state of a scan has SEQ_HS(LP)_DATA.NEXT_ACTION=GO_TO_ENTRY_ADDR). Except for CONINUOUS mode, firmware should wait for this bit to be low before powering down the SAR (AC.SAR_EN=0). Default Value: 0

28.1.57 SAR_STA_RANGE_STATUS

Description: Range status register

Address: 0x42E80544

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	GPIO_CHAN_RANGE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW1C	
HW Access	Reserved						RW1S	
Name	Reserved [15:10]						FIR_RANGE_STATUS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW1S							
Name	MUX_CHAN_RANGE_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW1S							
Name	MUX_CHAN_RANGE_STATUS [31:24]							

Bits	Name	Description
31 : 16	MUX-_CHAN_RANGE_STA-TUS	MUX Channel Range detect status: hardware sets this bit for each channel if the conversion result (after averaging) of that channel met the condition specified by the MUX_CHAN_CFG.STATUS_SEL registers. Write with '1' to clear bit. Default Value: 0
9 : 8	FIR_RANGE_STATUS	FIR Range detect status: hardware sets this bit for each FIR if the FIR output met the condition specified by the FIR_CFG.STATUS_SEL registers. Write with '1' to clear bit. Default Value: 0
7 : 0	GPI-O_CHAN_RANGE_STA-TUS	GPIO Channel Range detect status: hardware sets this bit for each channel if the conversion result (after averaging) of that channel met the condition specified by the GPIO_CHAN_CFG.STATUS_SEL registers. Write with '1' to clear bit. Default Value: 0

28.1.58 SAR_STA_CHAN_COEFF0

Description: Channel correction coefficients (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42E80550

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [15:12]				OFFSET [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	GAIN [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	GAIN [31:24]							

Bits	Name	Description
31 : 16	GAIN	Gain Correction Coefficient (Default value is gain of 1). This field is intended to correct sources of gain error in the SAR channel (from the GPIO to the SAR ADC input). It is expected that both the channel offset correction coefficient and SAR ADC offset have already been calibrated (i.e. HS(LP)_CAL_MEM values are valid). Multiplies the 12-bit SAR conversion by X.XXXXXXXXXXXXXXX Range is: 1/2^15=(0.000030517578125) to 2-(1/2^15)=(1.999969482421875) Default Value: 0x8000
11 : 0	OFFSET	Channel Offset Correction Coefficient (Default value is offset of 0). This field is intended to correct sources of offset error in the SAR channel (from the GPIO to the SAR ADC input). It is expected that the SAR ADC offset has already been calibrated (i.e. HS(LP)_CAL_MEM values are valid). Signed offset values range from -2048 (0x800) to +2047 (0x7FF) is added to 12-bit SAR conversion. Default Value: 0

28.1.59 SAR_FIR00_COEF

Description: Coefficient Value

Address: 0x42E80600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COEF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COEF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COEF	FIR Coefficient Value The coefficient values can range from -1+1/215 to 1-1/215 with a resolution of 1/215. The coefficient uses twos-complement notation and the decimal point is fixed to the right of the most significant bit. Examples: -0.25 = 0xE000 and 0.25 = 0x2000 Default Value: Undefined

28.1.60 SAR_FIR00_TAP

Description: Tap Value

Address: 0x42E80604

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TAP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TAP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	TAP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	TAP [31:24]							

Bits	Name	Description
31 : 0	TAP	Tap value, in typical operation, software only reads the tap. For debug purposes only, sofware can write to the tap. Default Value: Undefined

28.1.61 SAR_FIR10_COEF

Description: Coefficient Value

Address: 0x42E80800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COEF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COEF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	COEF	FIR Coefficient Value The coefficient values can range from -1+1/215 to 1-1/215 with a resolution of 1/215. The coefficient uses twos-complement notation and the decimal point is fixed to the right of the most significant bit. Examples: -0.25 = 0xE000 and 0.25 = 0x2000 Default Value: Undefined

28.1.62 SAR_FIR10_TAP

Description: Tap Value

Address: 0x42E80804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TAP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TAP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	TAP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	TAP [31:24]							

Bits	Name	Description
31 : 0	TAP	Tap value, in typical operation, software only reads the tap. For debug purposes only, sofware can write to the tap. Default Value: Undefined

28.1.63 SAR_HS_CAL_MEM_CALCTRL

Description: SAR HS Core Calibration Control Register

Address: 0x42E80C14

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							RW
HW Access	R							R
Name	R1 [7:1]							OFFDEP

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW		RW	
HW Access	R				R		R	
Name	R12 [15:12]				STC [11:10]		AVG [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	R12 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	R12 [31:24]							

Bits	Name	Description
31 : 12	R12	Reserved Read as 0, should be written with 0 Default Value: 0
11 : 10	STC	Calibration sample time control Default Value: 0 **0x0: STC_512 :** use sample time of 512 clk_lppass cycles **0x1: STC_1024 :** use sample time of 1024 clk_lppass cycles **0x2: STC_2048 :** use sample time of 2048 clk_lppass cycles **0x3: STC_32 :** use sample time of 32 clk_lppass cycles
9 : 8	AVG	Determines averaging repetitions for calibration Default Value: 0

28.1.63 SAR_HS_CAL_MEM_CALCTRL (continued)

		0x0: AVG_16 : use 16 averaging repititions per calibration value **0x1: AVG_32 :** use 32 averaging repititions per calibration value **0x2: AVG_64 :** use 64 averaging repititions per calibration value **0x3: AVG_2 :** use 2 averaging repititions per calibration value
7 : 1	R1	Reserved Read as 0, should be written with 0 Default Value: 0
0	OFFDEP	Use the old offset-dependent calibration scheme when this bit is set. Default Value: 0

28.1.64 SAR_HS_CAL_MEM_CONVCTRL

Description: SAR HS Core Conversion Control Register

Address: 0x42E80C1C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	R6 [7:6]		RES_RAW	MSB_CTRL	R2 [3:2]		INIT_TC [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	R6 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	R6 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	R6 [31:24]							

Bits	Name	Description
31 : 6	R6	Reserved Read as 0, should be written with 0 Default Value: 0
5	RES_RAW	DO NOT change from Default for *A0 PSOC™ Edge. Output the raw result (13-bit, redundant coding) instead of the processed one (12-bit, binary coding). Default Value: 0
4	MSB_CTRL	When set, the redistribution time for the MSB decision is extended to two sync periods. Default Value: 0
3 : 2	R2	Reserved Read as 0, should be written with 0 Default Value: 0
1 : 0	INIT_TC	Choose for how many sync-periods the core-side capacitors are initialized to the common mode voltage, via the OCS switch, after conversion start is received. Default Value: 0 **0x0: CONV_INIT_1 :** Initialize for 1 sync-period to the core's common mode voltage before redistribution starts **0x1: CONV_INIT_2 :** Initialize for 2 sync-period to the core's common mode voltage before redistribution starts

28.1.64 SAR_HS_CAL_MEM_CONVCTRL (continued)

0x2: CONV_INIT_4 :

Initialize for 4 sync-period to the core's common mode voltage before redistribution starts

0x3: CONV_INIT_16 :

Initialize for 16 sync-period to the core's common mode voltage before redistribution starts

28.1.65 SAR_HS_CAL_MEM_ADFTMUX

Description: SAR HS Core Analog DFT Multiplexer Control Register

Address: 0x42E80C20

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				RW
HW Access	R			R				R
Name	R5 [7:5]			SEL [4:1]				EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	R5 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	R5 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	R5 [31:24]							

Bits	Name	Description
31 : 5	R5	Reserved Read as 0, should be written with 0 Default Value: 0
4 : 1	SEL	Select the voltage to be output on the Analog DFT port when ADFTMUX.EN=1 Default Value: 0 **0x0: SEL_VCM_CH0 :** Select common mode voltage of channel 0 when ADFTMUX.EN=1 **0x1: SEL_VCM_CH1 :** Select common mode voltage of channel 1 when ADFTMUX.EN=1 **0x2: SEL_VCM_CH2 :** Select common mode voltage of channel 2 when ADFTMUX.EN=1 **0x3: SEL_VCM_CH3 :** Select common mode voltage of channel 3 when ADFTMUX.EN=1 **0x4: SEL_VCM_CH4 :** Select common mode voltage of channel 4 when ADFTMUX.EN=1

28.1.65 SAR_HS_CAL_MEM_ADFTMUX (continued)

0x5: SEL_VCM_CH5 :

Select common mode voltage of channel 5 when ADFTMUX.EN=1

0x6: SEL_VCM_CH6 :

Select common mode voltage of channel 6 when ADFTMUX.EN=1

0x7: SEL_VCM_CH7 :

Select common mode voltage of channel 7 when ADFTMUX.EN=1

0x8: SEL_VCM_CH8 :

Select common mode voltage of channel 8 when ADFTMUX.EN=1

0x9: SEL_VCM_CH9 :

Select common mode voltage of channel 9 when ADFTMUX.EN=1

0xa: SEL_VCM_CORE :

Select common mode voltage of core when ADFTMUX.EN=1

0xb: SEL_VAREF :

Select positive reference voltage when ADFTMUX.EN=1

0xc: SEL_VSSA :

Select analog ground when ADFTMUX.EN=1

0xd: RESERVED_0 :

0xe: RESERVED_1 :

0xf: RESERVED_2 :

0	EN	Enable the ADT Mux selection according to ADFTMUX.SEL when set. If unset, the ADFT Mux output port will not be driven from the ADC. Default Value: 0

28.1.66 SAR_HS_CAL_MEM_CALMEM00

Description: SAR HS Core Channel Calibration Values

Address: 0x42E80C40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	LINBIT10 [7:6]		LINBIT9 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LINBIT11 [15:12]				LINBIT10 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW						RW	
HW Access	R						R	
Name	LINBIT12 [23:18]						LINBIT11 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW							RW
HW Access	R							R
Name	OFFSET [31:25]							LINBIT12

Bits	Name	Description
31 : 25	OFFSET	Offset calibration value Default Value: 0
24 : 18	LINBIT12	Linearity calibration value for bit 12 (MSB) of the capacitor array Default Value: 0
17 : 12	LINBIT11	Linearity calibration value for bit 11 (MSB-1) of the capacitor array Default Value: 0
11 : 6	LINBIT10	Linearity calibration value for bit 10 (MSB-2) of the capacitor array Default Value: 0
5 : 0	LINBIT9	Linearity calibration value for bit 9 (MSB-3) of the capacitor array Default Value: 0

28.1.67 SAR_LP_CAL_MEM_CALCTRL

Description: SAR LP Core Calibration Control Register

Address: 0x42E80C94

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							RW
HW Access	R							R
Name	R1 [7:1]							OFFDEP

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW		RW	
HW Access	R				R		R	
Name	R12 [15:12]				STC [11:10]		AVG [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	R12 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	R12 [31:24]							

Bits	Name	Description
31 : 12	R12	Reserved Read as 0, should be written with 0 Default Value: 0
11 : 10	STC	Calibration sample time control Default Value: 0 **0x0: STC_512 :** use sample time of 512 clk_lppass cycles **0x1: STC_1024 :** use sample time of 1024 clk_lppass cycles **0x2: STC_2048 :** use sample time of 2048 clk_lppass cycles **0x3: STC_32 :** use sample time of 32 clk_lppass cycles
9 : 8	AVG	Determines averaging repetitions for calibration Default Value: 0

28.1.67 SAR_LP_CAL_MEM_CALCTRL (continued)

		0x0: AVG_16 : use 16 averaging repititions per calibration value **0x1: AVG_32 :** use 32 averaging repititions per calibration value **0x2: AVG_64 :** use 64 averaging repititions per calibration value **0x3: AVG_2 :** use 2 averaging repititions per calibration value
7 : 1	R1	Reserved Read as 0, should be written with 0 Default Value: 0
0	OFFDEP	Use the old offset-dependent calibration scheme when this bit is set. Default Value: 0

28.1.68 SAR_LP_CAL_MEM_CONVCTRL

Description: SAR LP Core Conversion Control Register

Address: 0x42E80C9C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW				
HW Access	R		R	R				
Name	R6 [7:6]		RES_RAW	R0 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	R6 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	R6 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	R6 [31:24]							

Bits	Name	Description
31 : 6	R6	Reserved Read as 0, should be written with 0 Default Value: 0
5	RES_RAW	DO NOT change from Default for *A0 PSOC™. Output the raw result (13-bit, redundant coding) instead of the processed on (12-bit, binary coding) Default Value: 0
4 : 0	R0	Reserved Read as 0, should be written with 0 Default Value: 0

28.1.69 SAR_LP_CAL_MEM_ADFTMUX

Description: SAR LP Core Analog DFT Multiplexer Control Register

Address: 0x42E80CA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW		RW
HW Access	R					R		R
Name	R5 [7:3]					SEL [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	R5 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	R5 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	R5 [31:24]							

Bits	Name	Description
31 : 3	R5	Reserved Read as 0, should be written with 0 Default Value: 0
2 : 1	SEL	Select the voltage to be output on the Analog DFT port when ADFTMUX.EN=1 Default Value: 0 **0x0: SEL_VCM_CORE :** Select common mode voltage of core when ADFTMUX.EN=1 **0x1: SEL_VAREF :** Select positive reference voltage when ADFTMUX.EN=1 **0x2: SEL_VSSA :** Select analog ground when ADFTMUX.EN=1 **0x3: RESERVED_0 :**
0	EN	Enable the ADT Mux selection according to ADFTMUX.SEL when set. If unset, the ADFT Mux output port will not be driven from the ADC. Default Value: 0

28.1.70 SAR_LP_CAL_MEM_CALMEM0

Description: SAR LP Core Channel Calibration Values

Address: 0x42E80CC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	LINBIT10 [7:6]		LINBIT9 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LINBIT11 [15:12]				LINBIT10 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW						RW	
HW Access	R						R	
Name	LINBIT12 [23:18]						LINBIT11 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW							RW
HW Access	R							R
Name	OFFSET [31:25]							LINBIT12

Bits	Name	Description
31 : 25	OFFSET	Offset calibration value Default Value: Undefined
24 : 18	LINBIT12	Linearity calibration value for bit 12 (MSB) of the capacitor array Default Value: Undefined
17 : 12	LINBIT11	Linearity calibration value for bit 11 (MSB-1) of the capacitor array Default Value: Undefined
11 : 6	LINBIT10	Linearity calibration value for bit 10 (MSB-2) of the capacitor array Default Value: Undefined
5 : 0	LINBIT9	Linearity calibration value for bit 9 (MSB-3) of the capacitor array Default Value: Undefined

28.1.71 SAR_TRIM_BUF0_OFFSET_TRIM

Description: Buffer zero trim control

Address: 0x42E80F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		BUF0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	BUF0_OFFSET_TRIM	buffer 0 offset trim Default Value: 0

28.1.72 SAR_TRIM_BUF0_SLOPE_OFFSET_TRIM

Description: Buffer zero trim control

Address: 0x42E80F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		BUF0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	BUF0_SLOPE_OFF-SET_TRIM	buffer 0 slope offset drift trim Default Value: 0

28.1.73 SAR_TRIM_BUF0_COMP_TRIM

Description: Buffer zero trim control

Address: 0x42E80F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				BUF0_COMP_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	BUF0_COMP_TRIM	Buffer 0 Compensation Capacitor Trim Bit<3> is not used Bits<2:0> 000 = 0.1pF 001 = 1.1pF 010 = 2.1pF 011 = 3.1pF 100 = 4.1pF 101 = 5.1pF 110 = 6.1pF 111 = 7.1pF Default Value: 0

28.1.74 SAR_TRIM_BUF1_OFFSET_TRIM

Description: Buffer one trim control

Address: 0x42E80F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		BUF1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	BUF1_OFFSET_TRIM	buffer 1 offset trim Default Value: 0

28.1.75 SAR_TRIM_BUF1_SLOPE_OFFSET_TRIM

Description: Buffer one trim control

Address: 0x42E80F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		BUF1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	BUF1_SLOPE_OFF-SET_TRIM	buffer 1 slope offset drift trim Default Value: 0

28.1.76 SAR_TRIM_BUF1_COMP_TRIM

Description: Buffer one trim control

Address: 0x42E80F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				BUF1_COMP_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	BUF1_COMP_TRIM	see BUF0_COMP_TRIM Default Value: 0

28.1.77 SAR_TRIM_RMP_TRIM

Description: Risk Mitigation bits

Address: 0x42E80F18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW			
HW Access	Reserved			R	R			
Name	Reserved [7:5]			TEMP_-SEN-SOR_TRIM	RMP_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4	TEMP_SENSOR_TRIM	Risk Mitigation Trim bits for SAR Temperature sensor Default Value: 1
3 : 0	RMP_TRIM	Bits <1:0> Risk mitigation for bias in reference block 0 = Bias +20% 1 = Normal Bias (Default) 2 = Normal BIas 3 = Bias -20% Bits <3:2> Risk mitigation for pump block in OA0 and OA1 0 = Normal Pump Operation for OA0 and OA1 (If pump is enabled). 1 = Reserved (Don't use!) 2 = Pumps are boosted for OA0 and OA1 (if PUMP is enabled). 3 = Reserved (Don't use!) Default Value: 1

28.1.78 ACTRLR_CTRL

Description: control register

Address: 0x42ED0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	- 0: LPPASS IP disabled - 1: LPPASS IP enabled This field functions as the Global Enable for the LPPASS IP. This field must be set to gain read/write access to any other register in the LPPASS memory map. During initial IP release from reset (i.e. during POR), the LPPASS IP (along with its switched internal power domain) is disabled. After setting this bit, the LPPASS internal switched domain is powered up. The user must then wait for PWR_STATUS.SW_OK to assert. At this point, the user has read/write access to all LPPASS memory map registers. Clearing this field (i.e. disabling the LPPASS) can lead to status only clearing, or status and configuration clearing (see CFG.DISABLE_MODE). Default Value: 0

28.1.79 ACTRLR_CMD_RUN

Description: run command register

Address: 0x42ED0004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							RW1C
Name	Reserved [7:1]							RUN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	RUN	Autonomous Controller Run Command Firmware should only write to this field when STATUS=STOPPED or PAUSED. When firmware sets this field, the Autonomous Controller starts running at the State pointed to by CMD_STATE. Hardware clears this field when the Autonomous Controller acknowledges the run command. If this field is set while STATUS=RUNNING, the Autonomous Controller will not respond to the command (beyond clearing the field). This register is reset whenever the following occurs: 1. The Autonomous Controller is disabled (clearing CTRL.ENABLED) 2. The LPPASS is configured for HS mode (STATUS.MODE=0) and the chip leaves an Active Mode. Default Value: 0

28.1.80 ACTRLR_CMD_STATE

Description: state override register

Address: 0x42ED0008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		RW					
Name	Reserved [7:6]		STATE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	STATE	Autonomous Controller Command State This field indicates where which AC State (0-63) the AC will execute instructions from when it receives a RUN or SINGLE_STEP command. Hardware updates this field whenever the AC transitions from RUNNING to STOPPED or PAUSED. When STOPPED or PAUSED, firmware can overrwrite this field to force the AC to execute from a specific STATE when triggered by a subsequent RUN or SINGLE_STEP command. This field must never be written to if STATUS=RUNNING. This register is reset whenever the following occurs: 1. The Autonomous Controller is disabled (clearing CTRL.ENABLED) 2. The LPPASS is configured for HS mode (STATUS.MODE=0) and the chip leaves an Active Mode. Default Value: 0

28.1.81 ACTRLR_FW_TR0

Description: firmware trigger

Address: 0x42ED0010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							RW1C
Name	Reserved [7:1]							FW_TR

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	FW_TR	Firmware Trigger This field is used as a firmware trigger for the Autonomous Controller. The Autonomous Controller can be programmed to respond to the firmware trigger by programming a state with a condtion (COND) TR_LPPASS_IN*. Additionally, writing to this field will force the Autonomus Controller to wake from sleep. Hardware clears this bit when the Autonomous Controller acknowledges the trigger. This register is reset whenever the following occurs: 1. The Autonomous Controller is disabled (clearing CTRL.ENABLED) 2. The LPPASS is configured for HS mode (STATUS.MODE=0) and the chip leaves an Active Mode. Default Value: 0

28.1.82 ACTRLR_STATUS

Description: status register

Address: 0x42ED0020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [7:6]		CUR_STATE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved					R	R	
HW Access	Reserved					W	W	
Name	Reserved [15:11]					MODE	STATUS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
10	MODE	This field indicates the mode of the Autonomous Controller. The Autonmous Controller always resets to HS mode. This field is reset whenever the following occurs: 1. The Autonomous Controller is disabled (clearing CTRL.ENABLED) 2. The LPPASS is configured for HS mode (STATUS.MODE=0) and the chip leaves an Active Mode. Default Value: 0 **0x0: HS :** Autonomous Controller is in High Speed (HS) mode In this mode, the LPPASS IP is functional only in chip Active modes. The LPPASS IP is clocked from a peripheral source derived from clk_hf. **0x1: LP :** Autonomous Controller is Low Power (LP) mode In this mode, the LPPASS IP is functional in both chip Active and Deepsleep modes. The LP-PASS IP is clocked from the internal LPOSC.
9 : 8	STATUS	Autonomous Controller status Default Value: 0 **0x0: STOPPED :** Autonomous Controller is stopped

28.1.82 ACTRLR_STATUS (continued)

		0x1: RUNNING : Autonomous Controller is running **0x2: PAUSED :** Autonomous Controller is paused **0x3: RESERVED :**
5 : 0	CUR_STATE	This register indicates the current state of the Autonomous Controller (valid values are 0-63). Default Value: 0

28.1.83 ACTRLR_CFG

Description: config register (only accessible if CTRL.EN=0)

Address: 0x42ED0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				DOUT_EN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [23:18]						DISABLE_-MODE	SLEEP_-MODE

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
17	DISABLE_MODE	Autonomous Controller Disable Mode -0 : Keep the LPPASS switched digital supply powered when the AC is disabled (i.e. CTRL.EN-ABLED=0). - 1: Power Down the LPPASS digital supply when AC is disabled. This has the following conse-quences to the LPPASS: 1. Digital leakage is reduced (i.e. all logic on the LPPASS switched supply is powered off). 2. All LPPASS configuration is lost (all registers are reset and SRAMs lose data). Default Value: 0
16	SLEEP_MODE	Autonomous Controller Sleep Mode -0 : Keep the LPPASS switched digital supply powered when the AC is sleeping (i.e. AC state programmed to action (ACT)=WAIT_FOR, and condition (COND)=wakeup source). - 1: Power Down the LPPASS digital supply when AC is asleep (i.e. AC ACT=WAIT_FOR, AC_COND= wakeup source). This has the following consequences to the LPPASS: 1. Digital leakage is reduced (i.e. all logic on the LPPASS switched supply is powered off). 2. CTBLs, SAR FIRs, and the DACs loose all configuration (i.e. they must be re-programmed to be functional again). 3. The wakeup time is increased by 3us (to account for the switched power domain coming up). Default Value: 0
3 : 0	DOUT_EN	DOUT output enable. Bits in this field must be set prior to writing to TIMER_TABLE_STRUCT.TT_CF0_DOUT. -0 : DOUT[X] output disabled - 1: DOUT[X] output enabled Default Value: 0

28.1.84 ACTRLR_DEBUG_PAUSE

Description: pause debug register

Address: 0x42ED0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							RW1C
Name	Reserved [7:1]							PAUSE

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	PAUSE	Pause Command Setting this field requests the Autonomous Controller (AC) to pause. This field is used for debug purposes only. The AC waits for the present state to complete before pausing. If the present state cannot complete (i.e. the ACT and COND are programmed improperly), the AC will not pause. This command must not be used when executing an AC sleep state (ACT=WAIT_FOR and COND=WAKE_*). When the AC is paused, all AC registerd conditions are cleared. Hardware clears this bit when the Autonomous Controller is paused. This command is ignored if STATUS.STATUS is PAUSED or STOP. Default Value: 0

28.1.85 ACTRLR_DEBUG_SINGLE_STEP

Description: single step debug register

Address: 0x42ED0034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW1S
HW Access	Reserved							RW1C
Name	Reserved [7:1]							SINGLE_-STEP

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	SINGLE_STEP	Single Step Command Setting this field requests the Autonomous Controller (AC) to execute the next AC state (pointed to by CMD_STATE.STATE) and pause after completing that state. This field is used for debug purposes only. If the state (pointed to by CMD_STATE.STATE) cannot complete (i.e. the ACT and COND are programmed improperly), the AC will not pause at the end of the single step command. This command must not be used when executing an AC sleep state (ACT=WAIT_FOR and COND=*_WAKE). When the AC is paused, all AC registerd conditions are cleared. Hardware clears this bit when the Autonomous Controller pauses after executing the single step command. This command is ignored if STATUS.STATUS is RUNNING. Default Value: 0

28.1.86 ACTRLR_PWR_STATUS

Description: power status register

Address: 0x42ED0038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							SW_OK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	SW_OK	This field indicates the status of the LPPASS switched power domain. This status should be polled whenever CTRL.EN toggles from a 0 to 1. 0: switched domain is powered off. 1: switched domain is powered on. Default Value: 0

28.1.87 ACTRLR_CNTR_STATUS0

Description: Loop/Interval counter status register

Address: 0x42ED0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		R					
HW Access	Reserved		W					
Name	Reserved [7:6]		CUR_STATE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CUR_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved				R			
HW Access	Reserved				W			
Name	Reserved [23:20]				CUR_CNT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R	Reserved						
HW Access	W	Reserved						
Name	BUSY	Reserved [30:24]						

Bits	Name	Description
31	BUSY	This field indicates if the counter is busy (i.e. count value is non-zero). Default Value: 0
19 : 8	CUR_CNT	This field indicates the count value for the given counter. Default Value: 0
5 : 0	CUR_STATE	This field indicates the assigned Autonomous Controller (AC) State of a counter. Valid numbers are 0-63. Default Value: 0

28.1.88 ACTRLR_TTCFG0_TT_CFG0

Description: AC Table Configuration 0

Address: 0x42ED0800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW	RW			
HW Access	Reserved			R	R			
Name	Reserved [7:5]			MODE	DOUT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CTBL1_UNLOCK	CTBL0_UNLOCK	PTC_UNLOCK	DAC1_UNLOCK	DAC0_UNLOCK	SAR_UNLOCK	PRB_UNLOCK	MODE_UNLOCK

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							DOUT_UNLOCK

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	DOUT_UNLOCK	DOUT Unlock 0: Lock: DOUT does NOT get updated 1: Unlock: DOUT does get updated Default Value: 0
15	CTBL1_UNLOCK	See CTBL0_UNLOCK Default Value: 0
14	CTBL0_UNLOCK	CTBL0 Unlock 0: Lock: CTBL0 fields: OPA1(0)_EN, OPA1(0)_GAIN, OPA1(0)_CFG do NOT get updated 1: Unlock: CTBL0 fields: OPA1(0)_EN, OPA1(0)_GAIN, OPA1(0)_CFG do get updated Default Value: 0
13	PTC_UNLOCK	PTC Unlock 0: Lock: PTC fields: CMP1(0)_EN, CMP1(0)_CFG do NOT get updated 1: Unlock: PTC fields: CMP1(0)_EN, CMP1(0)_CFG do get updated Default Value: 0
12	DAC1_UNLOCK	See DAC0_UNLOCK Default Value: 0
11	DAC0_UNLOCK	DAC0 Unlock 0: Lock: DAC0 fields: EN does NOT get updated 1: Unlock: DAC0 fields: EN does get updated Default Value: 0

28.1.88 ACTRLR_TTCFG0_TT_CFG0 (continued)

10	SAR_UNLOCK	SAR Unlock 0: Lock: SAR fields: EN does NOT get updated 1: Unlock: SAR fields: EN does get updated Default Value: 0
9	PRB_UNLOCK	PRB Unlock 0: Lock: PRB fields: VREF1(0)_VAL, VREF1(0)_FW_MODE do NOT get updated 1: Unlock: PRB fields: VREF1(0)_VAL, VREF1(0)_FW_MODE do get updated Default Value: 0
8	MODE_UNLOCK	Mode Unlock 0: Lock: MODE does NOT get updated 1: Unlock: MODE does get updated Default Value: 0
4	MODE	LPPASS Operating Mode 0: High Speed (HS) Operation - The PASS is clocked from CLK_HF directly (nominally 80MHz) and is only functional in chip Active mode (i.e. the IP is reset in chip Deepsleep and Hibernate) 1: Low Power (LP) Operation - The PASS is clocked from CLK_LPOSC (4MHz) and is functional in chip Active and Deepsleep mode (i.e. the IP is only reset in Hibernate) Default Value: 0
3 : 0	DOUT	LPPASS data out generation (the corresponding bit in CFG.DOUT_EN must be set when using this field) The data out bus is driven directly to the GPIO HSIO interface. The HSIO interface must be programmed properly for the DOUT bus to be observed on the GPIO pins. Default Value: 0

28.1.89 ACTRLR_TTCFG0_TT_CFG1

Description: AC Table Configuration 1

Address: 0x42ED0804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	RESERVED_0 [7:6]		BR_ADDR [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	RESERVED_1 [15:14]		COND [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	RW		
HW Access	R				R	R		
Name	CNT [23:20]				INTR_SET	ACTION [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CNT [31:24]							

Bits	Name	Description
31 : 20	CNT	This field is used to set the timer/counter values for either interval and loop counts. The actual count is CNT+1. Therefore, the range is 1 to 4096. The value of 1 is degenerate. This field is only valid if the action (ACT) is set to WAIT_FOR, or BRANCH_IF_* and the condition (COND) is set to CNT_DONE. If ACT is set to WAIT_FOR, the counter is first loaded with CNT+1 and is subsequently decremented every clock cycle (clock set by MODE). On terminal count, the CNT_DONE trigger is asserted. If ACT is set to BRANCH_IF_*, the counter is first checked if it is busy (count value is nonzero). If busy, the counter is decremented. If not busy, the counter is loaded with CNT+1. On terminal count, the CNT_DONE trigger is asserted. Default Value: Undefined
19	INTR_SET	AC Interrupt Set This field is used for setting the Autonomous Controller Interrupt and/or trigger. When set in a particular state, the AC generates a single cycle pulse to the interrupt logic. The AC interrupt or AC trigger must be unmasked for this field to generate an interrupt/trigger. If ACTION=WAIT_FOR, the signle cycle pulse is generated after the COND occurs, otherwise the single cycle pulse is sent immediately upon entering the state where the field is set. Default Value: Undefined
18 : 16	ACTION	Autonomous Controller Action Default Value: Undefined **0x0: STOP :** Stop the autonomous controller

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x1: NEXT :

Proceed to the next state

0x2: WAIT_FOR :

Wait for the associated COND to occur before moving to the next state
If COND=FALSE, stay in the present state indefinitely. If COND=TRUE, move to the next state.

0x3: BRANCH_IF_TRUE :

Check if COND has occurred, If it has, take the indicated branch (BR ADDR), if not, proceed to the next state.
If COND=FALSE, proceed to the next state. If COND=TRUE, take the indicated branch (BR_ADDR).

0x4: BRANCH_IF_FALSE :

Check if COND has occurred, If it has proceed to the next state, if not, take the indicated branch (BR ADDR)
If COND=FALSE, take the indicated branch (BR_ADDR). If COND=TRUE, proceed to the next state.

0x5: BRANCH_IF_TRUE_CLR :

Check if COND has occurred, If it has, take the indicated branch (BR ADDR), if not, proceed to the next state.
If COND=FALSE, proceed to the next state. If COND=TRUE, take the indicated branch (BR_ADDR).
If the indicated branch is taken, all loop counters are cleared (reset). If the AC_CONDITION is set to CNT_DONE, then the loop counters are not cleared (reset).

0x6: BRANCH_IF_FALSE_CLR :

Check if COND has occurred, If it has proceed to the next state, if not, take the indicated branch (BR ADDR)
If COND=FALSE, take the indicated branch (BR_ADDR). If COND=TRUE, proceed to the next state.
If the indicated branch is taken, all loop counters are cleared (reset). If the AC CONDITION is set to CNT_DONE, then the loop counters are not cleared (reset).

0x7: RESERVED0 :

15 : 14	RESERVED_1	Default Value: Undefined
13 : 8	COND	Autonomous Controller Condition Default Value: Undefined

0x0: False :

Hardcoded FALSE value

0x1: True :

Hardcoded TRUE value

0x2: BLOCK_READY :

Enabled block(s) are ready for use.

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x3: CNT_DONE :

if the ACTION is WAIT_FOR - this is an interval timer.
If the ACTION is BRANCH IF - this is a loop counter.

0x4: SAR_DONE :

SAR Sequencer Done
This status is sticky. It is set by the SAR when finishing a state in the SAR sequencer table (HS or LP) where SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to STOP. This field should NOT be used if the SAR is configured for CONTINUOUS operation (i.e. SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to GO_TO_ENTRY_ADDRESS).
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_DONE.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_DONEs).
This status does NOT indicate that the SAR data has been written to the FIFO (indicated by SAR_FIFO_DONE).

0x5: SAR_EOS :

SAR Sequencer EOS
This status is sticky. It is set by the SAR when finishing the state in the SAR sequencer table (HS or LP) where SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to GO_TO_ENTRY_ADDRESS or STOP. The status is cleared by the AC when executing an AC state with the COND programmed to SAR_EOS. No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_EOSs).
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_EOS.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_EOSs).

0x6: SAR_RANGE0 :

SAR Range 0 detection
This status is sticky. It is set by the SAR if the RANGE0 condition is met for a given channel with range 0 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_0).

The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_RANGE0.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_RANGE0s).

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x7: SAR_RANGE1 :

SAR Range 1 detection
This status is sticky. It is set by the SAR if the RANGE0 condition is met for a given channel with range 1 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_1).

The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_RANGE1.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_RANGE0s).

0x8: SAR_RANGE2 :

SAR Range 2 detection
This status is sticky. It is set by the SAR if the RANGE2 condition is met for a given channel with range 0 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_2).

The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_RANGE2.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_RANGE2s).

0x9: SAR_RANGE3 :

SAR Range 3 detection
This status is sticky. It is set by the SAR if the RANGE0 condition is met for a given channel with range 3 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_3).

The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_RANGE3.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_RANGE3s).

0xa: SAR_BUSY :

SAR BUSY detection
This status is set whenever the SAR is running a scan. This status is transparent from the SAR sequencer (i.e. the status is not sticky).

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0xb: SAR_FIR0_DONE :

SAR FIR0 Done detection
This status is sticky. It is set by the SAR FIR0 block whenever FIR0 produces a valid output. The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_RANGE3.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
The status is cleared by the AC when executing an AC state with the COND programmed to SAR_FIR0_DONE. No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_FIR0_DONEs). This status does NOT indicate that the FIR0 data has been written to the FIFO (indicated by SAR_FIR0_FIFO_DONE).

0xc: SAR_FIR1_DONE :

SAR FIR1 Done detection
This status is sticky. It is set by the SAR FIR1 block whenever FIR0 produces a valid output. The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_RANGE3.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
The status is cleared by the AC when executing an AC state with the COND programmed to SAR_FIR1_DONE. No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_FIR1_DONEs). This status does NOT indicate that the FIR1 data has been written to the FIFO (indicated by SAR_FIR1_FIFO_DONE).

0xd: SAR_FIFO_DONE :

SAR FIFO Done
This status is sticky. This status is SAR_DONE ANDED with FIFO writing complete. This field should NOT be used if the SAR is configured for CONTINUOUS operation (i.e. SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to GO_TO_ENTRY_ADDRESS) since SAR_DONE is never asserted. In that case, the user should use the appropriate FIFO_LEVEL triggers.
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_FIFO_DONE.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_FIFO_DONEs).
This status does NOT indicate that the SAR data has been written to the FIFO (indicated by SAR_FIFO_DONE).

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0xe: SAR_FIR0_FIFO_DONE :

SAR FIR0 FIFO Done detection
This status is sticky. It is set by the SAR FIR0 block whenever FIR0 data has been written into the FIFO. When using this bit, it is expected that FIR0 writes to the FIFO only once in a given SAR scan.
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_FIR0_FIFO_DONE.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_FIR0_FIFO_DONEs).

0xf: SAR_FIR1_FIFO_DONE :

SAR FIR1 FIFO Done detection
This status is sticky. It is set by the SAR FIR1 block whenever FIR1 data has been written into the FIFO. When using this bit, it is expected that FIR1 writes to the FIFO only once in a given SAR scan.
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_FIR1_FIFO_DONE.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.SAR_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple SAR_FIR1_FIFO_DONEs).

0x10: PTC_STROBE0 :

PTC Post Processor 0 Strobe
This status is set whenever the PTC Post Processor 0 has valid data. This status is transparent from the PTC post processor (i.e. the status is not sticky).
The AC needs to poll this status (i.e. ACTION is WAIT_FOR and COND is PTC_STROBE0) prior to checking PTC_RANGE0.

0x11: PTC_STROBE1 :

PTC Post Processor 1 Strobe
This status is set whenever the PTC Post Processor 1 has valid data. This status is transparent from the PTC post processor (i.e. the status is not sticky).
The AC needs to poll this status (i.e. ACTION is WAIT_FOR and COND is PTC_STROBE1) prior to checking PTC_RANGE1.

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x12: PTC_CMP0 :

PTC COMP0 output
This status is sticky. It is set by the PTC Comparator 0 if the condition is met (i.e. PTC_STA_CFG.CFG.COMP0_OUT field).
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to PTC_CMP0.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling PTC comparator 1 (by clearing TT_CFG3.PTC_CMP0_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple PTC_CMP0s).

0x13: PTC_CMP1 :

PTC COMP1 output
This status is sticky. It is set by the PTC Comparator 1 if the condition is met (i.e. PTC_STA_CFG.CFG.COMP1_OUT field).
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to PTC_CMP1.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling PTC comparator 1 (by clearing TT_CFG3.PTC_CMP1_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple PTC_CMP1s).

0x14: PTC_RANGE0 :

PTC Post Processor 0 Range output
This status is sticky. It is set by the PTC Post Processor if the RANGE0 condition is met (i.e. PTC_PP_STRUCT0.*).
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_FIR1_FIFO_DONE.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling both PTC comparators (by clearing TT_CFG3.PTC_CMP0_EN AND TT_CFG3_PTC_COMP1_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple PTC_RANGE0s).

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x15: PTC_RANGE1 :

PTC Post Processor 1 Range output
This status is sticky. It is set by the PTC Post Processor if the RANGE1 condition is met (i.e. PTC_PP_STRUCT1.*).
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to SAR_FIR1_FIFO_DONE.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling both PTC comparators (by clearing TT_CFG3.PTC_CMP0_EN AND TT_CFG3_PTC_COMP1_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple PTC_RANGE1s).

0x16: CTBL0_CMP0 :

CTBL0 COMP0 output
This status is sticky. It is set by the CTBL0 Opamp0 Comparator if the condition is met (i.e. CTBL_STA_CFG.CFG.COMP0_OUT field).
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to CTBL0_CMP0.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling CTBL0 opamp0 (by clearing TT_CFG2.CTBL0_OA0_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple CTBL0_CMP0s).

0x17: CTBL0_CMP1 :

CTBL0 COMP1 output
This status is sticky. It is set by the CTBL0 Opamp1 Comparator if the condition is met (i.e. CTBL_STA_CFG.CFG.COMP1_OUT field).
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to CTBL0_CMP1.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling CTBL0 opamp1 (by clearing TT_CFG2.CTBL0_OA1_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple CTBL0_CMP1s).

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x18: CTBL1_CMP0 :

CTBL1 COMP0 output
This status is sticky. It is set by the CTBL1 Opamp0 Comparator if the condition is met (i.e. CTBL_STA_CFG.CFG.COMP0_OUT field).
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to CTBL1_CMP0.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling CTBL1 opamp0 (by clearing TT_CFG2.CTBL0_OA0_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple CTBL1_CMP0s).

0x19: CTBL1_CMP1 :

CTBL1 COMP1 output
This status is sticky. It is set by the CTBL1 Opamp1 Comparator if the condition is met (i.e. CTBL_STA_CFG.CFG.COMP1_OUT field).
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to CTBL1_CMP1.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling CTBL1 opamp1 (by clearing TT_CFG2.CTBL0_OA1_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple CTBL1_CMP1s).

0x1a: RESERVED0 :

0x1b: RESERVED1 :

0x1c: RESERVED2 :

0x1d: RESERVED3 :

0x1e: RESERVED4 :

0x1f: RESERVED5 :

0x20: CHIP_ACTIVE_MODE :

Chip Active Mode Status
This status is set whenever the system is operating in Active Mode (this includes all Low Power active modes)

0x21: CHIP_DEEPSLEEP_MODE :

Chip Deepsleep Mode Status
This status is set whenever the system is operating in Deepsleep Mode (this includes all RAM power modes in Deepsleep)

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x22: TR_LPPASS_IN0 :

External trigger 0 (or the FW trigger 0)
This status is sticky. It is set by the either the external hardware trigger 0 or FW trigger 0 asserting.
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to TR_LPPASS_IN0.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple TR_LPPASS_IN0s).

0x23: TR_LPPASS_IN1 :

External trigger 0 (or the FW trigger 1)
This status is sticky. It is set by the either the external hardware trigger 0 or FW trigger 1 asserting.
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to TR_LPPASS_IN1.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple TR_LPPASS_IN1s).

0x24: TR_LPPASS_IN2 :

External trigger 0 (or the FW trigger 2)
This status is sticky. It is set by the either the external hardware trigger 0 or FW trigger 2 asserting.
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to TR_LPPASS_IN2.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple TR_LPPASS_IN2s).

0x25: TR_LPPASS_IN3 :

External trigger 0 (or the FW trigger 3)
This status is sticky. It is set by the either the external hardware trigger 0 or FW trigger 3 asserting.
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to TR_LPPASS_IN3.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple TR_LPPASS_IN3s).

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x26: TR_LPPASS_IN_WAKE :

External Trigger Wakeup Source
When using this condition, the action (ACT) must be set to WAIT_FOR.
This condition is used to put the AC to sleep. The AC will wake from sleep when any external trigger [0-3] is asserted.
When the AC is sleeping, all registered AC conditions are cleared.

0x27: TIMER_DONE_WAKE :

Timer Wakeup Source
When using this condition, the action (ACT) must be set to WAIT_FOR. The Wakeup Timer must also be configured (INFRA.TIMER registers).
This condition is used to put the AC to sleep. The AC will wake from sleep when the Wakeup Timer reaches terminal count (TC).
When the AC is sleeping, all registered AC conditions are cleared.

0x28: CTBL0_CMP0_WAKE :

CTBL0 comparator 0 wakeup
When using this condition, the action (ACT) must be set to WAIT_FOR. The comparator wakeup condition is configured per CTBL0_STA_CFG_Regs.CFG.OA0_COMP_OUT. The CTBL0 comparator 0 be enabled during sleep (TT_CFG2.CTBL0_OA0_EN=1).
This condition is used to put the AC to sleep. The AC will wake from sleep when CTBL0 Comparator 0 meets the configured wakeup condition.
When the AC is sleeping, all registered AC conditions are cleared.

0x29: CTBL0_CMP1_WAKE :

CTBL0 comparator 1 wakeup
When using this condition, the action (ACT) must be set to WAIT_FOR. The comparator wakeup condition is configured per CTBL0_STA_CFG_Regs.CFG.OA0_COMP_OUT. The CTBL0 comparator 1 be enabled during sleep (TT_CFG2.CTBL0_OA1_EN=1).
This condition is used to put the AC to sleep. The AC will wake from sleep when CTBL0 Comparator 1 meets the configured wakeup condition.
When the AC is sleeping, all registered AC conditions are cleared.

0x2a: CTBL1_CMP0_WAKE :

CTBL1 comparator 0 wakeup
When using this condition, the action (ACT) must be set to WAIT_FOR. The comparator wakeup condition is configured per CTBL1_STA_CFG_Regs.CFG.OA0_COMP_OUT. The CTBL1 comparator 0 be enabled during sleep (TT_CFG2.CTBL1_OA0_EN=1).
This condition is used to put the AC to sleep. The AC will wake from sleep due when CTBL1 Comparator 0 meets the configured wkaeup condition.
When the AC is sleeping, all registered AC conditions are cleared.

0x2b: CTBL1_CMP1_WAKE :

CTBL1 comparator 1 wakeup
When using this condition, the action (ACT) must be set to WAIT_FOR. The comparator wakeup condition is configured per CTBL1_STA_CFG_Regs.CFG.OA0_COMP_OUT. The CTBL1 comparator 1 be enabled during sleep (TT_CFG2.CTBL1_OA1_EN=1).
This condition is used to put the AC to sleep. The AC will wake from sleep when CTBL1 Comparator 1 meets the configured wakeup condition.
When the AC is sleeping, all registered AC conditions are cleared.

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x2c: PTC_CMP0_WAKE :

PTC comparator 0 wakeup
When using this condition, the action (ACT) must be set to WAIT_FOR. The comparator wakeup condition is configured per PTC_STA_CFG_Regs.CFG.COMP0_OUT. The PTC comparator 0 be enabled during sleep (TT_CFG3.PTC_CMP0_EN=1).
This condition is used to put the AC to sleep. The AC will wake from sleep when PTC Comparator 0 meets the configured wakeup condition.
When the AC is sleeping, all registered AC conditions are cleared.

0x2d: PTC_CMP1_WAKE :

PTC comparator 1 wakeup
When using this condition, the action (ACT) must be set to WAIT_FOR. The comparator wakeup condition is configured per PTC_STA_CFG_Regs.CFG.COMP1_OUT. The PTC comparator 0 be enabled during sleep (TT_CFG3.PTC_CMP1_EN=1).
This condition is used to put the AC to sleep. The AC will wake from sleep when PTC Comparator 1 meets the configured wakeup condition.
When the AC is sleeping, all registered AC conditions are cleared.

0x2e: FIFO_LEVEL0 :

FIFO Level 0 trigger
This status is set whenever FIFO0 level condition has been met (FIFO_LEVEL0.LEVEL). This status is transparent from the FIFO (i.e. the status is not sticky).

0x2f: FIFO_LEVEL1 :

FIFO Level 1 trigger
This status requires that FIFO_STA_CFG_Regs.CFG.SEL=1,2,3.
This status is set whenever FIFO1 level condition has been met (FIFO_LEVEL1.LEVEL). This status is transparent from the FIFO (i.e. the status is not sticky).

0x30: FIFO_LEVEL2 :

FIFO Level 2 trigger
This status requires that FIFO_STA_CFG_Regs.CFG.SEL=2,3.
This status is set whenever FIFO2 level condition has been met (FIFO_LEVEL2.LEVEL). This status is transparent from the FIFO (i.e. the status is not sticky).

0x31: FIFO_LEVEL3 :

FIFO Level 3 trigger
This status requires that FIFO_STA_CFG_Regs.CFG.SEL=2,3.
This status is set whenever FIFO3 level condition has been met (FIFO_LEVEL3.LEVEL). This status is transparent from the FIFO (i.e. the status is not sticky).

0x32: FIFO_LEVEL4 :

FIFO Level 4 trigger
This status requires that FIFO_STA_CFG_Regs.CFG.SEL=3.
This status is set whenever FIFO4 level condition has been met (FIFO_LEVEL4.LEVEL). This status is transparent from the FIFO (i.e. the status is not sticky).

0x33: FIFO_LEVEL5 :

FIFO Level 5 trigger
This status requires that FIFO_STA_CFG_Regs.CFG.SEL=3.
This status is set whenever FIFO5 level condition has been met (FIFO_LEVEL5.LEVEL). This status is transparent from the FIFO (i.e. the status is not sticky).

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x34: FIFO_LEVEL6 :

FIFO Level 6 trigger
This status requires that FIFO_STA_CFG_Regs.CFG.SEL=3.
This status is set whenever FIFO6 level condition has been met (FIFO_LEVEL6.LEVEL). This status is transparent from the FIFO (i.e. the status is not sticky).

0x35: FIFO_LEVEL7 :

FIFO Level 7 trigger
This status requires that FIFO_STA_CFG_Regs.CFG.SEL=3.
This status is set whenever FIFO7 level condition has been met (FIFO_LEVEL7.LEVEL). This status is transparent from the FIFO (i.e. the status is not sticky).

0x36: DAC0_RANGE0 :

DAC0 Range 0 detection
This status is sticky. It is set by the DAC0 if the RANGE0 condition is met for a given channel with range 0 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_0). This status is not used when DAC0 is configured for FW mode.

The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to DAC0_RANGE0.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the DAC0 (by clearing TT_CFG3.DAC0_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple DAC0_RANGE0s).

0x37: DAC0_RANGE1 :

DAC0 Range 1 detection
This status is sticky. It is set by the DAC0 if the RANGE1 condition is met for a given channel with range 1 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_1). This status is not used when DAC0 is configured for FW mode.

The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to DAC0_RANGE1.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the DAC0 (by clearing TT_CFG3.DAC0_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple DAC0_RANGE1s).

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x38: DAC0_RANGE2 :

DAC0 Range 2 detection
This status is sticky. It is set by the DAC0 if the RANGE2 condition is met for a given channel with range 2 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_2). This status is not used when DAC0 is configured for FW mode.

The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to DAC0_RANGE2.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the DAC0 (by clearing TT_CFG3.DAC0_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple DAC0_RANGE2s).

0x39: DAC0_EPOCH :

DAC0 End of Waveform event
This status is sticky. It is set by the DAC when finishing a waveform. This condition is only used if the DAC channel (pointed to by the AC when triggered) is configured for LUT mode.
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to DAC0_EPOCH.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.DAC0_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple DAC0_EPOCHs).

0x3a: DAC0_STROBE :

DAC0 Strobe
This status is set whenever the DAC output has been updated. This status is typically used by the AC to poll when the DAC has responded to the DAC_INC/DAC_DEC fields.This status is transparent from the DAC (i.e. the status is not sticky).
The AC needs to poll this status (i.e. ACTION is WAIT_FOR and COND is DAC0_STROBE) prior to checking DAC_RANGE0-2 or setting DAC_INC/DAC_DEC fields.

0x3b: DAC1_RANGE0 :

DAC1 Range 0 detection
This status is sticky. It is set by the DAC1 if the RANGE0 condition is met for a given channel with range 0 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_0).

The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to DAC1_RANGE0.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the DAC1 (by clearing TT_CFG3.DAC1_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple DAC1_RANGE0s).

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

0x3c: DAC1_RANGE1 :

DAC1 Range 1 detection
This status is sticky. It is set by the DAC0 if the RANGE1 condition is met for a given channel with range 1 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_1).

The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to DAC1_RANGE1.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the DAC1 (by clearing TT_CFG3.DAC1_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple DAC1_RANGE1s).

0x3d: DAC1_RANGE2 :

DAC1 Range 2 detection
This status is sticky. It is set by the DAC1 if the RANGE2 condition is met for a given channel with range 2 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_2).

The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to DAC1_RANGE2.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the DAC1 (by clearing TT_CFG3.DAC1_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple DAC1_RANGE2s).

0x3e: DAC1_EPOCH :

DAC1 End of Waveform event
This status is sticky. It is set by the DAC when finishing a waveform. This condition is only used if the DAC channel (pointed to by the AC when triggered) is configured for LUT mode.
The status is cleared by the AC when any of the following occur:
1. Executing an AC state where ACT is set to WAIT_FOR or BRANCH_IF_* and COND is set to DAC1_EPOCH.
2. Executing an AC state where ACT is set to WAIT_FOR and COND is set to any of the *_WAKE.
3. Pausing the AC (using the DEBUG_PAUSE or DEBUG_SINGLE_STEP commands)
4. Disabling the AC (through CTRL.ENABLED)
5. Disabling the SAR (by clearing TT_CFG3.DAC1_EN)
No overflow indication is provided for this bit. Therefore, it is up to the user to program the AC such that this status is read prior to an overflow (multiple DAC1_EPOCHs).

0x3f: DAC1_STROBE :

DAC1 Strobe
This status is set whenever the DAC output has been updated. This status is typically used by the AC to poll when the DAC has responded to the DAC_INC/DAC_DEC fields.This status is transparent from the DAC (i.e. the status is not sticky).
The AC needs to poll this status (i.e. ACTION is WAIT_FOR and COND is DAC1_STROBE) prior to checking DAC1_RANGE0-2 or setting DAC_INC/DAC_DEC fields.

7 : 6	RESERVED_0	Default Value: Undefined

28.1.89 ACTRLR_TTCFG0_TT_CFG1 (continued)

5 : 0	BR_ADDR	absolute address of the branch if taken (0-63 possible). This field in only used if the AC action (ACT) is set to BRANCH_IF_* and the condtion (COND) is met. Default Value: Undefined

28.1.90 ACTRLR_TTCFG0_TT_CFG2

Description: AC Table Configuration 2

Address: 0x42ED0808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	CTBL0_OA0_EN	CTBL0_OA0_CFG [6:4]			CTBL0_OA0_GAIN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	CTBL0_OA1_EN	CTBL0_OA1_CFG [14:12]			CTBL0_OA1_GAIN [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	CTBL1_OA0_EN	CTBL1_OA0_CFG [22:20]			CTBL1_OA0_GAIN [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	CTBL1_OA1_EN	CTBL1_OA1_CFG [30:28]			CTBL1_OA1_GAIN [27:24]			

Bits	Name	Description
31	CTBL1_OA1_EN	CTBL1 Opamp1 enable This field is only used by the Autonomous Controller if CTBL1_UNLOCK is set. Otherwise, the field is ignored. Default Value: Undefined **0x0: DISABLED :** Disabled CTBL1 Opamp1 is powered down, comparator logic is reset and all CTBL1 OA1 AC conditions are cleared. CTBL1 configuration is retained. **0x1: ENABLED :** Enabled CTBL1 Opamp1 is powered and all logic is enabled and clocked.
30 : 28	CTBL1_OA1_CFG	See CTBL0_OA0_CFG Default Value: Undefined

28.1.90 ACTRLR_TTCFG0_TT_CFG2 (continued)

27 : 24	CTBL1_OA1_GAIN	See CTBL0_OA0_GAIN Default Value: Undefined
23	CTBL1_OA0_EN	See CTBL0_OA0_EN Default Value: Undefined
22 : 20	CTBL1_OA0_CFG	See CTBL0_OA0_CFG Default Value: Undefined
19 : 16	CTBL1_OA0_GAIN	See CTBL0_OA0_GAIN Default Value: Undefined
15	CTBL0_OA1_EN	See CTBL0_OA0_EN Default Value: Undefined
14 : 12	CTBL0_OA1_CFG	CTBL0 Opamp1 Mux Configuration This field determines the state of all input and reference muxes to the Opamp along with the output driver (i.e. if the oamp drives internal loads only or internal/external loads). This field is only used by the Autonomous Controller if CTBL0_UNLOCK is set. Otherwise, the field is ignored. Default Value: Undefined **0x0: CFG_0 :** Configuration 0 Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs0 **0x1: CFG_1 :** Configuration 1 Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs1 **0x2: CFG_2 :** Configuration 2 Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs2 **0x3: CFG_3 :** Configuration 3 Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs3 **0x4: CFG_4 :** Configuration 4 Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs4 **0x5: CFG_5 :** Configuration 5 Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs5 **0x6: CFG_6 :** Configuration 6 Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs6 **0x7: CFG_7 :** Configuration 7 Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs7

28.1.90 ACTRLR_TTCFG0_TT_CFG2 (continued)

11 : 8	CTBL0_OA1_GAIN	CTBL0 Opamp1 gain control. This field affects the value of the input (Rin) and feedback (Rfb) resistors. This field is only used by the Autonomous Controller if CTBL0_UNLOCK is set. Otherwise, the field is ignored. This field is only valid if CTBL0_STA_CFG_Regs.CFG.OA1_TOPO= 1 (PGA), 2 (TIA), 4 (Differential Amplifier) For PGA and Differential Amplifier configuration, both input and feedback resistors are used. For TIA configuration, only the feedback resistor is used. For Differential Amplifier configurations, CTBL0_OA0_GAIN must equal CTBL0_OA1_GAIN Default Value: Undefined **0x0: 1_00 :** Rin = 192k, Rfb = 0 Gain of 1.00 **0x1: 1_42 :** Rin = 135k, Rfb = 57k Non-Inverting PGA: Gain of 1.42 Inverting PGA: Gain of 0.42 TIA: Rfb = 57k Differential Amplifier: Gain of 0.21 **0x2: 2_00 :** Rin = 96k, Rfb = 96k Non-Inverting PGA: Gain of 2.00 Inverting PGA: Gain of 1.00 TIA: Rfb = 96k Differential Amplifier: Gain of 0.50 **0x3: 2_78 :** Rin = 69k, Rfb = 123k Non-Inverting PGA: Gain of 2.78 Inverting PGA: Gain of 1.78 TIA: Rfb = 123k Differential Amplifier: Gain of 0.89 **0x4: 4_00 :** Rin = 48k, Rfb = 144k Non-Inverting PGA: Gain of 4.00 Inverting PGA: Gain of 3.00 TIA: Rfb = 144k Differential Amplifier: Gain of 1.50 **0x5: 5_82 :** Rin = 33k, Rfb = 159k Non-Inverting PGA: Gain of 5.82 Inverting PGA: Gain of 4.82 TIA: Rfb = 159k Differential Amplifier: Gain of 2.41

28.1.90 ACTRLR_TTCFG0_TT_CFG2 (continued)

0x6: 8_00 :

Rin = 24k, Rfb = 168k
Non-Inverting PGA: Gain of 8.00
Inverting PGA: Gain of 7.00
TIA: Rfb = 168k
Differential Amplifier: Gain of 3.50

0x7: 10_67 :

Rin = 18k, Rfb = 174k
Non-Inverting PGA: Gain of 10.67
Inverting PGA: Gain of 9.67
TIA: Rfb = 174k
Differential Amplifier: Gain of 4.83

0x8: 16_00 :

Rin = 12k, Rfb = 180k
Non-Inverting PGA: Gain of 16.00
Inverting PGA: Gain of 15.00
TIA: Rfb = 180k
Differential Amplifier: Gain of 7.50

0x9: 21_33 :

Rin = 9k, Rfb = 183k
Non-Inverting PGA: Gain of 21.33
Inverting PGA: Gain of 20.33
TIA: Rfb = 183k
Differential Amplifier: Gain of 10.17

0xa: 32_00 :

Rin = 6k, Rfb = 186k
Non-Inverting PGA: Gain of 32.00
Inverting PGA: Gain of 31.00
TIA: Rfb = 186k
Differential Amplifier: Gain of 15.50

0xb: RESERVED_0 :

0xc: RESERVED_1 :

0xd: RESERVED_2 :

0xe: RESERVED_3 :

0xf: RESERVED_4 :

7	CTBL0_OA0_EN	CTBL0 Opamp0 enable This field is only used by the Autonomous Controller if CTBL0_UNLOCK is set. Otherwise, the field is ignored. Default Value: Undefined

28.1.90 ACTRLR_TTCFG0_TT_CFG2 (continued)

0x0: DISABLED :

Disabled
CTBL0 Opamp0 is powered down, comparator logic is reset and all CTBL0 OA0 AC conditions are cleared. CTBL0 configuration is retained.

0x1: ENABLED :

Enabled
CTBL0 Opamp0 is powered and all logic is enabled and clocked.

6 : 4	CTBL0_OA0_CFG	CTBL0 Opamp0 Mux Configuration This field determines the state of all input and reference muxes to the Opamp along with the output driver (i.e. if the oamp drives internal loads only or internal/external loads). This field is only used by the Autonomous Controller if CTBL0_UNLOCK is set. Otherwise, the field is ignored. Default Value: Undefined

0x0: CFG_0 :

Configuration 0
Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs0

0x1: CFG_1 :

Configuration 1
Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs1

0x2: CFG_2 :

Configuration 2
Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs2

0x3: CFG_3 :

Configuration 3
Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs3

0x4: CFG_4 :

Configuration 4
Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs4

0x5: CFG_5 :

Configuration 5
Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs5

0x6: CFG_6 :

Configuration 6
Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs6

0x7: CFG_7 :

Configuration 7
Mux settings determined by CTBL0_DYN_CFG_STRUCT_Regs7

28.1.90 ACTRLR_TTCFG0_TT_CFG2 (continued)

3 : 0	CTBL0_OA0_GAIN	CTBL0 Opamp0 gain control. This field affects the value of the input (Rin) and feedback (Rfb) resistors. This field is only used by the Autonomous Controller if CTBL0_UNLOCK is set. Otherwise, the field is ignored. This field is only valid if CTBL0_STA_CFG_Regs.CFG.OA0_TOPO= 1 (PGA), 2 (TIA), 4 (Differential Amplifier) For PGA and Differential Amplifier configuration, both input and feedback resistors are used. For TIA configuration, only the feedback resistor is used. For Differential Amplifier configurations, CTBL0_OA0_GAIN must equal CTBL0_OA1_GAIN Default Value: Undefined **0x0: 1_00 :** Rin = 192k, Rfb = 0 Gain of 1.00 **0x1: 1_42 :** Rin = 135k, Rfb = 57k Non-Inverting PGA: Gain of 1.42 Inverting PGA: Gain of 0.42 TIA: Rfb = 57k Differential Amplifier: Gain of 0.42 **0x2: 2_00 :** Rin = 96k, Rfb = 96k Non-Inverting PGA: Gain of 2.00 Inverting PGA: Gain of 1.00 TIA: Rfb = 96k Differential Amplifier: Gain of 1.00 **0x3: 2_78 :** Rin = 69k, Rfb = 123k Non-Inverting PGA: Gain of 2.78 Inverting PGA: Gain of 1.78 TIA: Rfb = 123k Differential Amplifier: Gain of 1.78 **0x4: 4_00 :** Rin = 48k, Rfb = 144k Non-Inverting PGA: Gain of 4.00 Inverting PGA: Gain of 3.00 TIA: Rfb = 144k Differential Amplifier: Gain of 3.00 **0x5: 5_82 :** Rin = 33k, Rfb = 159k Non-Inverting PGA: Gain of 5.82 Inverting PGA: Gain of 4.82 TIA: Rfb = 159k Differential Amplifier: Gain of 4.82

28.1.90 ACTRLR_TTCFG0_TT_CFG2 (continued)

0x6: 8_00 :

Rin = 24k, Rfb = 168k
Non-Inverting PGA: Gain of 8.00
Inverting PGA: Gain of 7.00
TIA: Rfb = 168k
Differential Amplifier: Gain of 7.00

0x7: 10_67 :

Rin = 18k, Rfb = 174k
Non-Inverting PGA: Gain of 10.67
Inverting PGA: Gain of 9.67
TIA: Rfb = 174k
Differential Amplifier: Gain of 9.67

0x8: 16_00 :

Rin = 12k, Rfb = 180k
Non-Inverting PGA: Gain of 16.00
Inverting PGA: Gain of 15.00
TIA: Rfb = 180k
Differential Amplifier: Gain of 15.00

0x9: 21_33 :

Rin = 9k, Rfb = 183k
Non-Inverting PGA: Gain of 21.33
Inverting PGA: Gain of 20.33
TIA: Rfb = 183k
Differential Amplifier: Gain of 20.33

0xa: 32_00 :

Rin = 6k, Rfb = 186k
Non-Inverting PGA: Gain of 32.00
Inverting PGA: Gain of 31.00
TIA: Rfb = 186k
Differential Amplifier: Gain of 31.00

0xb: RESERVED_0 :

0xc: RESERVED_1 :

0xd: RESERVED_2 :

0xe: RESERVED_3 :

0xf: RESERVED_4 :

28.1.91 ACTRLR_TTCFG0_TT_CFG3

Description: AC Table Configuration 3

Address: 0x42ED080C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW				
HW Access	R	R	R	R				
Name	SAR_EN	SAR_TR	RE-SERVED_2	SAR_ENTRY_ADDR [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW			
HW Access	R	R	R	R	R			
Name	DAC0_EN	DAC0_DEC	DAC0_INC	DAC0_TR	DAC0_CHANNEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW			
HW Access	R	R	R	R	R			
Name	DAC1_EN	DAC1_DEC	DAC1_INC	DAC1_TR	DAC1_CHANNEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	PTC_C-MP1_EN	PTC_CMP1_CFG [30:28]			PTC_C-MP0_EN	PTC_CMP0_CFG [26:24]		

Bits	Name	Description
31	PTC_CMP1_EN	See PTC_CMP0_EN Default Value: Undefined
30 : 28	PTC_CMP1_CFG	See PTC_CMP0_CFG Default Value: Undefined
27	PTC_CMP0_EN	PTC Comparator0 enable This field is only used by the Autonomous Controller if PTC_UNLOCK is set. Otherwise, the field is ignored. Default Value: Undefined **0x0: DISABLED :** Disabled PTC Comparator 0 is powered down, Comparator 0 logic is reset, and Comparator 0 clock is gated. PTC_COMP0 AC condition is cleared. PTC_STROBE0 and PTC_RANGE0 are functional if PTC_COMP1_EN is set. Otherwise those conditions are cleared/disabled. PTC Comparator 0 configuration is retained. **0x1: ENABLED :** Enabled PTC Comparator 0 is powered and all logic is enabled and clocked.

28.1.91 ACTRLR_TTCFG0_TT_CFG3 (continued)

26 : 24	PTC_CMP0_CFG	PTC Comp0 Mux Configuration This field determines the state of all input muxes to the Comparator 0. This field is only used by the Autonomous Controller if PTC_UNLOCK is set. Otherwise, the field is ignored. Default Value: Undefined **0x0: CFG_0 :** Configuration 0 Mux settings determined by PTC_DYN_CFG_STRUCT_Regs0 **0x1: CFG_1 :** Configuration 1 Mux settings determined by PTC_DYN_CFG_STRUCT_Regs1 **0x2: CFG_2 :** Configuration 2 Mux settings determined by PTC_DYN_CFG_STRUCT_Regs2 **0x3: CFG_3 :** Configuration 3 Mux settings determined by PTC_DYN_CFG_STRUCT_Regs3 **0x4: CFG_4 :** Configuration 4 Mux settings determined by PTC_DYN_CFG_STRUCT_Regs4 **0x5: CFG_5 :** Configuration 5 Mux settings determined by PTC_DYN_CFG_STRUCT_Regs5 **0x6: CFG_6 :** Configuration 6 Mux settings determined by PTC_DYN_CFG_STRUCT_Regs6 **0x7: CFG_7 :** Configuration 7 Mux settings determined by PTC_DYN_CFG_STRUCT_Regs7
23	DAC1_EN	See DAC0_EN Default Value: Undefined
22	DAC1_DEC	See DAC0_DEC Default Value: Undefined
21	DAC1_INC	See DAC0_INC Default Value: Undefined
20	DAC1_TR	See DAC0_TR Default Value: Undefined
19 : 16	DAC1_CHANNEL	See DAC0_CHANNEL Default Value: Undefined

28.1.91 ACTRLR_TTCFG0_TT_CFG3 (continued)

15	DAC0_EN	DAC0 enable This field is only used by the Autonomous Controller if DAC0_UNLOCK is set. Otherwise, the field is ignored. Default Value: Undefined **0x0: DISABLED :** Disabled DAC0 is powered down, DAC0 logic is reset, DAC0 clocks are gated, and all DAC0 AC conditions are cleared. DAC0 configuration and waveform tables are retained. **0x1: ENABLED :** Enabled DAC0 is powered and all logic is enabled and clocked.
14	DAC0_DEC	DAC0 Decrement When entering a state where this field is set, the AC generates a single cycle pulse (decrement) to the DAC0 logic. DAC_INC and DAC_DEC CANNOT be simultaneously set in a given state (doing so will cause DAC_DEC to be ignored by the DAC0 logic). This field is only used by the DAC0 logic if the DAC0_CHANNEL field is set to 0-14 (Hardware channels) and DAC0.DAC_STA_CFG.CHAN_CFG.MODE = ADDR or DATA. If DAC0.DAC_STA_CFG.CHAN_CFG.MODE=ADDR, the DAC0 logic decrements the DAC address (Amount set by DAC0.DAC_STA_CFG.CHAN_CFG.STEP_SIZE_EN and STEP_SIZE_SEL) If DAC0.DAC_STA_CFG.CHAN_CFG.MODE=DATA, the DAC0 logic decrements the DAC Value (Amount set by CHAN_CFG.STEP_SIZE_EN and STEP_SIZE_SEL) Default Value: Undefined
13	DAC0_INC	DAC0 Increment When entering a state where this field is set, the AC generates a single cycle pulse (increment) to the DAC0 logic. DAC_INC and DAC_DEC CANNOT be simultaneously set in a given state (doing so will cause DAC_DEC to be ignored by the DAC0 logic). This field is only used by the DAC0 logic if the DAC0_CHANNEL field is set to 0-14 (Hardware channels) and DAC0.DAC_STA_CFG.CHAN_CFG.MODE = ADDR or DATA. If DAC0.DAC_STA_CFG.CHAN_CFG.MODE=ADDR, the DAC0 logic increments the DAC address (Amount set by DAC0.DAC_STA_CFG.CHAN_CFG.STEP_SIZE_EN and STEP_SIZE_SEL) If DAC0.DAC_STA_CFG.CHAN_CFG.MODE=DATA, the DAC0 logic increments the DAC Value (Amount set by CHAN_CFG.STEP_SIZE_EN and STEP_SIZE_SEL) Default Value: Undefined
12	DAC0_TR	DAC0 Trigger This field initiates DAC operation per the DAC0_CHANNEL selection. When entering a state where this field is set, the AC generates a single cycle pulse (trigger) to the DAC0 logic. This field is ignored unless: the DAC has been enabled in a prior state (DAC0_EN=1) and is ready (i.e. the AC has waited for BLOCK_READY in the same state where DAC0 was enabled). The DAC does NOT need to be disabled when switching channels. Default Value: Undefined
11 : 8	DAC0_CHANNEL	DAC0 Channel select This field is pointer to the active DAC channel. Valid values are 0-15. This field is ignored unless the following conditions are guaranteed: 1. The DAC is triggered (DAC0_TR=1). 2. The DAC has been enabled in a prior state (DAC0_EN=1) and is ready (i.e. the AC has waited for BLOCK_READY in the same state where DAC0 was enabled). Default Value: Undefined **0x0: CHANNEL_0 :** Channel 0 Hardware Channel 0: configured per DAC0.DAC_STA_CFG.CHAN_CFG0 Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

28.1.91 ACTRLR_TTCFG0_TT_CFG3 (continued)

0x1: CHANNEL_1 :

Channel 1
Hardware Channel 1: configured per DAC0.DAC_STA_CFG.CHAN_CFG1
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0x2: CHANNEL_2 :

Channel 2
Hardware Channel 2: configured per DAC0.DAC_STA_CFG.CHAN_CFG2
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0x3: CHANNEL_3 :

Channel 3
Hardware Channel 3: configured per DAC0.DAC_STA_CFG.CHAN_CFG3
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0x4: CHANNEL_4 :

Channel 4
Hardware Channel 4: configured per DAC0.DAC_STA_CFG.CHAN_CFG4
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0x5: CHANNEL_5 :

Channel 5
Hardware Channel 5: configured per DAC0.DAC_STA_CFG.CHAN_CFG5
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0x6: CHANNEL_6 :

Channel 6
Hardware Channel 6: configured per DAC0.DAC_STA_CFG.CHAN_CFG6
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0x7: CHANNEL_7 :

Channel 7
Hardware Channel 7: configured per DAC0.DAC_STA_CFG.CHAN_CFG7
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0x8: CHANNEL_8 :

Channel 8
Hardware Channel 8: configured per DAC0.DAC_STA_CFG.CHAN_CFG8
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0x9: CHANNEL_9 :

Channel 9
Hardware Channel 9: configured per DAC0.DAC_STA_CFG.CHAN_CFG9
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0xa: CHANNEL_10 :

Channel 10
Hardware Channel 10: configured per DAC0.DAC_STA_CFG.CHAN_CFG10
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

28.1.91 ACTRLR_TTCFG0_TT_CFG3 (continued)

0xb: CHANNEL_11 :

Channel 11
Hardware Channel 11: configured per DAC0.DAC_STA_CFG.CHAN_CFG11
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0xc: CHANNEL_12 :

Channel 12
Hardware Channel 12: configured per DAC0.DAC_STA_CFG.CHAN_CFG12
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0xd: CHANNEL_13 :

Channel 13
Hardware Channel 13: configured per DAC0.DAC_STA_CFG.CHAN_CFG13
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0xe: CHANNEL_14 :

Channel 14
Hardware Channel 14: configured per DAC0.DAC_STA_CFG.CHAN_CFG14
Writes to FW_DAC_VAL and FW_DAC_VAL_NXT are ignored.

0xf: FW_CHANNEL :

FW Channel
When selected, the DAC is configured for Firmware mode.
If ACTRLR.STATUS.MODE=0, firmware can write to FW_DAC_VAL and FW_DAC_VAL_NXT.
If ACTRLR.STATUS.MODE=1, firmware can only write to FW_DAC_VAL_NXT.
Autonomus Controller DAC conditions, DAC0_INC, DAC0_DEC are not used in this mode.

7	SAR_EN	SAR enable This field is only used by the Autonomous Controller if SAR_UNLOCK is set. Otherwise, the field is ignored. Default Value: Undefined **0x0: DISABLED :** Disabled SAR is powered down, SAR logic (and FIRs) are reset, SAR/FIR clocks are gated, and all SAR AC conditions are cleared. SAR configuration and sequencer tables are retained. FIFO status and content is not cleared (i.e. the FIFO contents can still be read if the SAR is disabled). **0x1: ENABLED :** Enabled SAR is powered and all SAR (FIR) logic is enabled and clocked.
6	SAR_TR	SAR Trigger (initiate SAR operation at sequencer address pointed to by SAR_ENTRY_ADDR) When entering a state where this field is set, the AC generates a single cycle pulse (trigger) to the SAR sequencer. This trigger is ignored by the SAR sequencer unless ALL of the following conditions are guaranteed: 1. The SAR has been enabled in a prior state (SAR_EN=1) and is ready (i.e. the AC has waited for BLOCK_READY in the same state where the SAR was enabled). 2. The SAR is idle (SAR.SAR_STA_CFG.STATUS.BUSY=0). Default Value: Undefined
5	RESERVED_2	Default Value: Undefined

28.1.91 ACTRLR_TTCFG0_TT_CFG3 (continued)

4 : 0	SAR_ENTRY_ADDR	SAR Timer Table Entry State This field is a pointer to the entry address of the SAR sequencer state table. If ACTRLR.STATUS.MODE=0, this field points to the High Speed state table (SEQ.HS.DATA) If ACTRLR.STATUS.MODE=1, this field points to the Low Power state table (SEQ.LP.DATA) Valid values are 0-31. This field is ignored unless the following conditions are guaranteed: 1. The SAR is triggered (SAR_TR=1). 2. The SAR has been enabled in a prior state (SAR_EN=1) and is ready (i.e. the AC has waited for BLOCK_READY in the same state where the SAR was enabled). 3. The SAR is idle (SAR.SAR_STA_CFG.STATUS.BUSY=0). This field is pointer to the entry address of the SAR sequencer state table. If ACTRLR.STATUS.MODE=0, this field points to the High Speed state table (SEQ.HS.DATA) If ACTRLR.STATUS.MODE=1, this field points to the Low Power state table (SEQ.LP.DATA) Default Value: Undefined

28.1.92 ACTRLR_TTCFG0_TT_CFG4

Description: AC Table Configuration 4

Address: 0x42ED0810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	Reserved			RW			
HW Access	R	Reserved			R			
Name	PRB_VREF0_FW_MODE	Reserved [22:20]			PRB_VREF0_VAL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved			RW			
HW Access	R	Reserved			R			
Name	PRB_VREF1_FW_MODE	Reserved [30:28]			PRB_VREF1_VAL [27:24]			

Bits	Name	Description
31	PRB_VREF1_FW_MODE	See PRB_VREF0_FW_MODE Default Value: 0
27 : 24	PRB_VREF1_VAL	See PRB_VREF0_VAL Default Value: 0
23	PRB_VREF0_FW_MODE	PRB VREF0 Firmware Mode This field is only used by the Autonomous Controller if PRB_UNLOCK is set. Otherwise, the field is ignored. Prior to writing to this field, VREF0 must be enabled (PRB.VREF_CTRL0.EN=1). Default Value: 0 **0x0: DISABLED :** Disabled (PRB output determined by TT.CFG4.PRB_VREF0_VAL) **0x1: ENABLED :** Enabled (PRB output determined by PRB.PRB_VREF_CTRL0.VAL)

28.1.92 ACTRLR_TTCFG0_TT_CFG4 (continued)

19 : 16	PRB_VREF0_VAL	TAP location for PRB VREF0. This field is only used by the Autonomous Controller if PRB_UNLOCK is set. Otherwise, the field is ignored. Prior the writing to this field, the following must be met: 1. PRB.VREF_CTRL0.EN=1 (VREF0 is enabled) 2. PRB_VREF0_FW_MODE = 0 (VREF0 is configured for Autonomous Controller control) The field is reset only when disabling the AC. Default Value: 0 **0x0: TAP_0 :** VREF0 = 0.06*PRB.VREF_CTRL.CFG **0x1: TAP_1 :** VREF0 = 0.13*PRB.VREF_CTRL.CFG **0x2: TAP_2 :** VREF0 = 0.19*PRB.VREF_CTRL.CFG **0x3: TAP_3 :** VREF0 = 0.25*PRB.VREF_CTRL.CFG **0x4: TAP_4 :** VREF0 = 0.31*PRB.VREF_CTRL.CFG **0x5: TAP_5 :** VREF0 = 0.38*PRB.VREF_CTRL.CFG **0x6: TAP_6 :** VREF0 = 0.44*PRB.VREF_CTRL.CFG **0x7: TAP_7 :** VREF0 = 0.50*PRB.VREF_CTRL.CFG **0x8: TAP_8 :** VREF0 = 0.56*PRB.VREF_CTRL.CFG **0x9: TAP_9 :** VREF0 = 0.63*PRB.VREF_CTRL.CFG **0xa: TAP_10 :** VREF0 = 0.69*PRB.VREF_CTRL.CFG **0xb: TAP_11 :** VREF0 = 0.75*PRB.VREF_CTRL.CFG

28.1.92 ACTRLR_TTCFG0_TT_CFG4 (continued)

0xc: TAP_12 :

VREF0 = 0.81*PRB.VREF_CTRL.CFG

0xd: TAP_13 :

VREF0 = 0.88*PRB.VREF_CTRL.CFG

0xe: TAP_14 :

VREF0 = 0.94*PRB.VREF_CTRL.CFG

0xf: TAP_15 :

VREF0 = 1.00*PRB.VREF_CTRL.CFG

28.1.93 INFRA_CLOCK_PTC_LP_DIV

Description: Low Power Clock divider for PTC (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42EE0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DIV_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						DIV_VAL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	DIV_VAL	Actual divide value is DIV_VAL+1. The root clock for this divider is the LPPASS LPOSC (4.096MHz nominal). This field is only used if the PTC is enabled (AC.PTC_CMP0(1)_EN=1) and the Autonomous Controller is configured for LP mode (ACTRLR.STATUS.MODE=LP). Default Value: 0

28.1.94 INFRA_CLOCK_DAC_LP_DIV0

Description: Low Power Clock divider for DAC (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42EE0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DIV_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						DIV_VAL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	DIV_VAL	Actual divide value is DIV_VAL+1. The root clock for this divider is the LPPASS LPOSC (4.096MHz nominal). This field is only used if the DAC is enabled (AC.DAC0(1)_EN=1) and the Autonomous Controller is configured for LP mode (ACTRLR.STATUS.MODE=LP). Default Value: 3

28.1.95 INFRA_CLOCK_PRIO_HS_DIV

Description: Clock enable for IP priority enabler (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42EE0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DIV_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [15:10]						DIV_VAL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	DIV_VAL	Actual divide value is DIV_VAL+1. The DIV value must be set to ensure that the corresponding clock rate is set to 4MHz. (The high speed system clock frequency is expected to be set to 80MHz, therby a defult DIV_VAL of 19 yields a 4MHz PRIO_HS clock). Default Value: 19

28.1.96 INFRA_PRIO_CFG0

Description: Sub IP Block IP priority enabler configuration (only accessible if ACTRLR.STATUS.MODE=0)

Address: 0x42EE0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		COUNT_VAL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CT-BL1_OA0_READY	CT-BL0_OA1_READY	CT-BL0_OA0_READY	PTC_C-MP1_READY	PTC_C-MP0_READY	DAC1_READY	DAC0_READY	SAR_READY

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [23:17]							CT-BL1_OA1_READY

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	CTBL1_OA1_READY	CTBL1 opamp1 ready Default Value: 0
15	CTBL1_OA0_READY	CTBL1 opamp0 ready Default Value: 0
14	CTBL0_OA1_READY	CTBL0 opamp1 ready Default Value: 0
13	CTBL0_OA0_READY	CTBL0 opamp0 ready Default Value: 0
12	PTC_CMP1_READY	PTC comparator 1 ready Default Value: 0
11	PTC_CMP0_READY	PTC comparator 0 ready Default Value: 0
10	DAC1_READY	DAC1 ready Default Value: 0
9	DAC0_READY	DAC0 ready Default Value: 0
8	SAR_READY	SAR ready Default Value: 0

28.1.96 INFRA_PRIO_CFG0 (continued)

5 : 0	COUNT_VAL	Actual count value is COUNT_VAL+1. This field determines the time delay between the Autonomous Controller (AC) setting the particular block enable bit and the corresponding assertion of the ready status bit. The delay time is based on a 4MHz clock (the corresponding delay time is 250ns*COUNT_VAL+1 (Delay time ranges from 250ns to 16us)). If delay times greater than 16us are required, then multiple PRIO_CFG states must be programmed to generate a cascade of delays (4 PRIO_CFG state*16us=64us maximum possible delay). Default Value: 0

28.1.97 INFRA_LPOSC_CFG

Description: Low Power Oscillator configuration register

Address: 0x42EE0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved					
HW Access	R	R	Reserved					
Name	ENABLE	MODE	Reserved [29:24]					

Bits	Name	Description
31	ENABLE	Master enable for LPOSC oscillator. This bit must be high at all times for all functions to work properly. Hardware will automatically disable the LPOSC during HIBERNATE and XRES. Default Value: 1
30	MODE	LPOSC functionality Default Value: 0 **0x0: ALWAYS_ON :** LPOSC always ON **0x1: DUTY_CYCLED :** LPOSC duty cycled based on AC Wakeup Signal

28.1.98 INFRA_LPOSC_TRIM

Description: LPOSC Trim Register

Address: 0x42EE01F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LPOSC_CTRL_FTRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							LPOSC_C-TRL_FTRIM

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [23:21]			LPOSC_CTRL_TCTRIM [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	LPOSC_CTRL_REFTRIM [31:24]							

Bits	Name	Description
31 : 24	LPOSC_CTRL_REFTRIM	LPOSC reference trims Default Value: 0x0
20 : 16	LPOSC_CTRL_TCTRIM	LPOSC temperature compensation trim Default Value: 0x10
8 : 0	LPOSC_CTRL_FTRIM	LPOSC frequency trim Default Value: 0x12B

28.1.99 INFRA_AREF_CTRL

Description: AREF control

Address: 0x42EE0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							VREF_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8	VREF_SEL	bandgap voltage select control Default Value: 0 **0x0: LOCAL :** Use locally generated Vref **0x1: EXTERNAL :** Use externally supplied Vref (aref_ext_vref)

28.1.100 INFRA_AREF_VREF_TRIM0

Description: VREF Trim bits

Address: 0x42EE02D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			VREF_ABS_TRIM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	VREF_ABS_TRIM	bandgap absolute voltage output trim (in signed magnitude format) MSB is not in use, selection from 0x00 - 0x0F 0x00 : No Voltage Trim Adjustment 0x0F : Maximum Positive Trim Adjustment (+20mV) Default Value: 0

28.1.101 INFRA_AREF_VREF_TRIM1

Description: VREF Trim bits

Address: 0x42EE02D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW					
HW Access	Reserved		R					
Name	Reserved [7:6]		VREF_TEMPCO_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5 : 0	VREF_TEMPCO_TRIM	bandgap voltage temperature correction trim 0x00 : Minimum temperature correction (smallest PTAT voltage) 0x3F : Maximum temperature correction (largest PTAT voltage) Default Value: 0

28.1.102 INFRA_AREF_VREF_TRIM2

Description: VREF Trim bits

Address: 0x42EE02D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				VREF_IPTAT2_ICTAT_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	VREF_IPTAT2_IC-TAT_TRIM	Default Value: 0

28.1.103 INFRA_AREF_VREF_TRIM3

Description: VREF Trim bits

Address: 0x42EE02DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			VREF_IPTAT2_DAC_TRIM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	VREF_IPTAT2_-DAC_TRIM	Default Value: 0

28.1.104 INFRA_AREF_IZTAT_TRIM0

Description: IZTAT Trim bits

Address: 0x42EE02E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	IZTAT_FINE_TRIM [7:4]				IZTAT_COARSE_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	IZTAT_FINE_TRIM	IZTAT temperature correction trim (RMB) 0x00 : No IZTAT temperature correction 0xFF : Maximum IZTAT temperature correction As this is a Risk Mitigation Register, it should be loaded with 0x08. Default Value: 0
3 : 0	IZTAT_COARSE_TRIM	IZTAT absolute current output trim 0x00 : Minimum IZTAT output current (~500nA) 0x3F : Maximum IZTAT output current (~1.5uA) Bits [7:6] are reserved. Default Value: 0

28.1.105 INFRA_AREF_IPTAT_TRIM0

Description: IPTAT Trim bits

Address: 0x42EE02E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	IPTAT_FINE_TRIM [7:4]				IPTAT_COARSE_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7 : 4	IPTAT_FINE_TRIM	IPTAT fine trim 0x0 : Minimum CTMB IPTAT Current (~875nA) 0xF : Maximum CTMB IPTAT Current (~1.1uA) Default Value: 0
3 : 0	IPTAT_COARSE_TRIM	IPTAT coarse trim 0x0 : Minimum IPTAT current (~150nA at room) 0xF : Maximum IPTAT current (~350nA at room) Default Value: 0

28.1.106 INFRA_AREF_IPTAT_TRIM1

Description: IPTAT Trim bits

Address: 0x42EE02E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			IPTAT_DAC_TRIM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	IPTAT_DAC_TRIM	IPTAT DAC trim 0x0 : Minimum IPTAT current (~150nA at room) 0xF : Maximum IPTAT current (~350nA at room) Default Value: 0

28.1.107 INFRA_AREF_ICTAT_TRIM0

Description: ICTAT Trim bits

Address: 0x42EE02EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved				RW			
HW Access	Reserved				R			
Name	Reserved [7:4]				RESERVED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
3 : 0	RESERVED	Default Value: 0

28.1.108 INFRA_AREF_ICTAT_TRIM1

Description: ICTAT Trim bits

Address: 0x42EE02F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved			RW				
HW Access	Reserved			R				
Name	Reserved [7:5]			ICTAT_COARSE_TRIM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
4 : 0	ICTAT_COARSE_TRIM	ICTAT coarse trim 0x0 : Minimum IPTAT current (~150nA at room) 0xF : Maximum IPTAT current (~350nA at room) Default Value: 0

28.1.109 INFRA_AREF_ICTAT_TRIM2

Description: ICTAT Trim bits

Address: 0x42EE02F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved					RW		
HW Access	Reserved					R		
Name	Reserved [7:3]					ICTAT_FINE_TRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
2 : 0	ICTAT_FINE_TRIM	ICTAT fine trim 0x0 : Minimum CTMB IPTAT Current (~875nA) 0xF : Maximum CTMB IPTAT Current (~1.1uA) Default Value: 0

28.1.110 INFRA_PRB_VREF_CTRL0

Description: PRB VREF Control

Address: 0x42EE0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				Reserved			RW
HW Access	R				Reserved			R
Name	VAL [7:4]				Reserved [3:1]			CFG

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	EN	Reserved [30:24]						

Bits	Name	Description
31	EN	PRB VREF enable control Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**
7 : 4	VAL	TAP location for PRB VREF Default Value: 0 **0x0: TAP_0 :** **0x1: TAP_1 :** **0x2: TAP_2 :** **0x3: TAP_3 :** **0x4: TAP_4 :** **0x5: TAP_5 :** **0x6: TAP_6 :**

28.1.110 INFRA_PRB_VREF_CTRL0 (continued)

0x7: TAP_7 :

0x8: TAP_8 :

0x9: TAP_9 :

0xa: TAP_10 :

0xb: TAP_11 :

0xc: TAP_12 :

0xd: TAP_13 :

0xe: TAP_14 :

0xf: TAP_15 :

0	CFG	PRB VREF reference configuration Default Value: 0 **0x0: VBG :** reference derived from VBG **0x1: VDDA :** reference derived from VDDA

28.1.111 INFRA_TIMER_CTRL

Description: Timer trigger control register

Address: 0x42EE0400

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	Reserved						
HW Access	R	Reserved						
Name	ENABLED	Reserved [30:24]						

Bits	Name	Description
31	ENABLED	0=disabled, 1=enabled This timer (downcounter) is used by the Autonomous Controller (AC) as a wakeup source (Autonomous Controller Action (ACT) = WAIT_FOR and Condition (COND) = TIMER_-DONE_WAKE). Even if CTRL.ENABLED is set, the Timer is held in Reset until the Autonomous Controller is running (ACTRLR.STATUS.STATUS= RUNNING). The Timer automatically resets whenenever the Autonomous Controller transitions between HS and LP modes, is paused, or disabled. The timer will generate a wakeup signal to the AC whenever it reaches Terminal Count (0). Default Value: 0

28.1.112 INFRA_TIMER_CFG

Description: Timer trigger configuration register

Address: 0x42EE0404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						CLOCK_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	CLOCK_SEL	Select Clock source of the Timer Default Value: 0 **0x0: CLK_LPOSC :** Timer clocked from CLK_LPOSC (nominally 4.096MHz) **0x1: CLK_LF :** Timer clocked from CLK_LF (nominally 32kHz) **0x2: TBD_0 :** **0x3: TBD_1 :**

28.1.113 INFRA_TIMER_PERIOD

Description: Timer trigger period register

Address: 0x42EE0408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PER_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PER_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
15 : 0	PER_VAL	Actual timer period is PER_VAL+1 (1 to 65536). Default Value: 0

28.1.114 LPPASS_MMIO_INTR_CAUSE

Description: Interrupt cause register

Address: 0x42EF0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PTC_RANGE1_INT	PTC_RANGE0_INT	PTC_-COMP1_INT	PTC_-COMP0_INT	CTBL1_-COMP1_INT	CTBL1_-COMP0_INT	CTBL0_-COMP1_INT	CTBL0_-COMP0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DAC1_RANGE2_INT	DAC1_RANGE1_INT	DAC1_RANGE0_INT	DAC0_EMPTY_INT	DAC0_EP-OCH_INT	DAC0_RANGE2_INT	DAC0_RANGE1_INT	DAC0_RANGE0_INT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	SAR_RANGE2_INT	SAR_RANGE1_INT	SAR_RANGE0_INT	SAR_RE-SULT_INT	SAR_EOS_INT	SAR_-DONE_INT	DAC1_EMPTY_INT	DAC1_EP-OCH_INT

Bits	31	30	29	28	27	26	25	24
SW Access	R	R				R	R	R
HW Access	W	W				W	W	W
Name	AC_INT	RESERVED [30:27]				SAR_-FIR1_RE-SULT_INT	SAR_-FIR0_RE-SULT_INT	SAR_RANGE3_INT

Bits	Name	Description
31	AC_INT	Autonomus Controller Interrupt Pending This interrupt is set by the Autonomus Controller whenever executing a state with ACTRLR.TIM-ER_TABLE_STRUCT.TT_CFG1.INTR_SET=1. Default Value: 0
30 : 27	RESERVED	Default Value: 0
26	SAR_FIR1_RESULT_INT	FIR1 Result Interrupt Pending This interrupt is set by SAR FIR1 whenever it generates a new result. The corresponding bit in SAR_STA_CFG.FIR_RESULT_MASK must be set in order for the FIR to generate the interrupt source. Default Value: 0
25	SAR_FIR0_RESULT_INT	FIR0 Result Interrupt Pending This interrupt is set by SAR FIR0 whenever it generates a new result. The corresponding bit in SAR_STA_CFG.FIR_RESULT_MASK must be set in order for the FIR to generate the interrupt source. Default Value: 0

28.1.114 LPPASS_MMIO_INTR_CAUSE (continued)

24	SAR_RANGE3_INT	SAR Range 3 detection Interrupt Pending This interrupt is set by the SAR if the RANGE3 condition is met for a given channel with range 3 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_-STRUCT_3). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the interrupt. Default Value: 0
23	SAR_RANGE2_INT	SAR Range 2 detection Interrupt Pending This interrupt is set by the SAR if the RANGE2 condition is met for a given channel with range 2 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_-STRUCT_2). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the interrupt. Default Value: 0
22	SAR_RANGE1_INT	SAR Range 1 detection Interrupt Pending This interrupt is set by the SAR if the RANGE1 condition is met for a given channel with range 1 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_-STRUCT_1). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the interrupt. Default Value: 0
21	SAR_RANGE0_INT	SAR Range 0 detection Interrupt Pending This interrupt is set by the SAR if the RANGE0 condition is met for a given channel with range 0 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_-STRUCT_0). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the interrupt. Default Value: 0
20	SAR_RESULT_INT	SAR Result Interrupt Pending This interrupt is set by the SAR when a channel writes data into its associated result register. Firmware must read SAR_STA_CFG.CHAN_RESULT_UPDATED to determine which channel generated the interrupt. The corresponding bit in SAR_STA_CFG.CHAN_RESULT_MASK must be set in order for the SAR to generate the interrupt source. Default Value: 0
19	SAR_EOS_INT	SAR Sequencer EOS Interrupt Pending This interrupt is set by the SAR when finishing the state in the SAR sequencer table (HS or LP) where SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to GO_TO_ENTRY_ADDRESS or STOP. This interrupt does NOT indicate that the SAR data has been written to the FIFO (the FIFO level interrupts should be used instead). Default Value: 0
18	SAR_DONE_INT	SAR Sequencer Done Interrupt Pending This interrupt is set by the SAR when finishing a state in the SAR sequencer table (HS or LP) where SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to STOP. The interrupt is not generated if the SAR is configured for CONTINUOUS operation (i.e. SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to GO_TO_ENTRY_ADDRESS). This interrupt does NOT indicate that the SAR data has been written to the FIFO (the FIFO level interrupts should be used instead). Default Value: 0
17	DAC1_EMPTY_INT	DAC1 Empty Interrupt Pending It is set by DAC1 when it empties the contents of its FW_DAC_VAL register. This interrupt is only generated if DAC1 is configured for FW operation (ACTRLR.TIMER_TABLE_-STRUCT.TT_CFG3.DAC1_CHANNEL=FW_CHANNEL. Default Value: 0
16	DAC1_EPOCH_INT	DAC1 End of Waveform Interrupt Pending It is set by DAC1 when finishing a waveform. This condition is only used if the DAC0 channel (pointed to by the AC when triggered) is configured for LUT mode. Default Value: 0
15	DAC1_RANGE2_INT	DAC1 Range 2 Interrupt Pending It is set by the DAC1 if the RANGE2 condition is met for a given channel with range 2 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_2). The interrupt is disabled when DAC1 is configured for FW mode. Default Value: 0

28.1.114 LPPASS_MMIO_INTR_CAUSE (continued)

14	DAC1_RANGE1_INT	DAC1 Range 1 Interrupt Pending It is set by the DAC1 if the RANGE1 condition is met for a given channel with range 1 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_1). The interrupt is disabled when DAC1 is configured for FW mode. Default Value: 0
13	DAC1_RANGE0_INT	DAC1 Range 0 Interrupt Pending It is set by the DAC1 if the RANGE0 condition is met for a given channel with range 0 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_0). The interrupt is disabled when DAC1 is configured for FW mode. Default Value: 0
12	DAC0_EMPTY_INT	DAC0 Empty Interrupt Pending It is set by DAC0 when it empties the contents of its FW_DAC_VAL register. This interrupt is only generated if DAC0 is configured for FW operation (ACTRLR.TIMER_TABLE_-STRUCT.TT_CFG3.DAC0_CHANNEL=FW_CHANNEL. Default Value: 0
11	DAC0_EPOCH_INT	DAC0 End of Waveform Interrupt Pending It is set by DAC0 when finishing a waveform. This condition is only used if the DAC0 channel (pointed to by the AC when triggered) is configured for LUT mode. Default Value: 0
10	DAC0_RANGE2_INT	DAC0 Range 2 Interrupt Pending It is set by the DAC0 if the RANGE2 condition is met for a given channel with range 2 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_2). The interrupt is disabled when DAC0 is configured for FW mode. Default Value: 0
9	DAC0_RANGE1_INT	DAC0 Range 1 Interrupt Pending It is set by the DAC0 if the RANGE1 condition is met for a given channel with range 1 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_1). The interrupt is disabled when DAC0 is configured for FW mode. Default Value: 0
8	DAC0_RANGE0_INT	DAC0 Range 0 Interrupt Pending It is set by the DAC0 if the RANGE0 condition is met for a given channel with range 0 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_0). The interrupt is disabled when DAC0 is configured for FW mode. Default Value: 0
7	PTC_RANGE1_INT	PTC Post Processor 1 Range Interrupt Pending It is set by the PTC Post Processor if the RANGE0 condition is met (i.e. PTC_PP_STRUCT1.*). Default Value: 0
6	PTC_RANGE0_INT	PTC Post Processor 0 Range Interrupt Pending It is set by the PTC Post Processor if the RANGE0 condition is met (i.e. PTC_PP_STRUCT0.*). Default Value: 0
5	PTC_COMP1_INT	PTC Comparator 1 Interrupt Pending It is set by the PTC Comparator 1 if the condition is met (i.e. PTC_STA_CFG.CFG.COMP1_OUT field). Default Value: 0
4	PTC_COMP0_INT	PTC Comparator 0 Interrupt Pending It is set by the PTC Comparator 0 if the condition is met (i.e. PTC_STA_CFG.CFG.COMP0_OUT field). Default Value: 0
3	CTBL1_COMP1_INT	CTBL1 Comparator 1 Interrupt Pending It is set by the CTBL1 Opamp1 Comparator if the condition is met (i.e. CT-BL_STA_CFG.CFG.COMP1_OUT field). Default Value: 0
2	CTBL1_COMP0_INT	CTBL1 Comparator 0 Interrupt Pending It is set by the CTBL1 Opamp0 Comparator if the condition is met (i.e. CT-BL_STA_CFG.CFG.COMP0_OUT field). Default Value: 0

28.1.114 LPPASS_MMIO_INTR_CAUSE (continued)

1	CTBL0_COMP1_INT	CTBL0 Comparator 1 Interrupt Pending It is set by the CTBL0 Opamp1 Comparator if the condition is met (i.e. CTBL_STA_CFG.CFG.COMP1_OUT field). Default Value: 0
0	CTBL0_COMP0_INT	CTBL0 Comparator 0 Interrupt Pending It is set by the CTBL0 Opamp0 Comparator if the condition is met (i.e. CTBL_STA_CFG.CFG.COMP0_OUT field). Default Value: 0

28.1.115 LPPASS_MMIO_FIFO_INTR_CAUSE

Description: FIFO Interrupt cause register

Address: 0x42EF0004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	FIFO_OVERFLOW7_INT	FIFO_OVERFLOW6_INT	FIFO_OVERFLOW5_INT	FIFO_OVERFLOW4_INT	FIFO_OVERFLOW3_INT	FIFO_OVERFLOW2_INT	FIFO_OVERFLOW1_INT	FIFO_OVERFLOW0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	FIFO_UNDERFLOW7_INT	FIFO_UNDERFLOW6_INT	FIFO_UNDERFLOW5_INT	FIFO_UNDERFLOW4_INT	FIFO_UNDERFLOW3_INT	FIFO_UNDERFLOW2_INT	FIFO_UNDERFLOW1_INT	FIFO_UNDERFLOW0_INT

Bits	23	22	21	20	19	18	17	16
SW Access	R			R	R		R	R
HW Access	W			W	W		W	W
Name	RESERVED_2 [23:21]			FIFO_LEVEL1_INT	RESERVED_1 [19:18]		FIFO_LEVEL0_INT	RESERVED_0

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	RESERVED_3	FIFO_LEVEL7_INT	FIFO_LEVEL6_INT	FIFO_LEVEL5_INT	FIFO_LEVEL4_INT	FIFO_LEVEL3_INT	FIFO_LEVEL2_INT	RESERVED_2

Bits	Name	Description
31	RESERVED_3	Default Value: 0
30	FIFO_LEVEL7_INT	FIFO Level 7 Interrupt Pending This level sensitive interrupt is set by the FIFO whenever FIFO 7 meets the FIFO_STA_CFG.LEVEL7.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
29	FIFO_LEVEL6_INT	FIFO Level 6 Interrupt Pending This level sensitive interrupt is set by the FIFO whenever FIFO 6 meets the FIFO_STA_CFG.LEVEL6.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0

28.1.115 LPPASS_MMIO_FIFO_INTR_CAUSE (continued)

28	FIFO_LEVEL5_INT	FIFO Level 5 Interrupt Pending This level sensitive interrupt is set by the FIFO whenever FIFO 5 meets the FIFO_STA_CFG.LEVEL5.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
27	FIFO_LEVEL4_INT	FIFO Level 4 Interrupt Pending This level sensitive interrupt is set by the FIFO whenever FIFO 4 meets the FIFO_STA_CFG.LEVEL4.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
26	FIFO_LEVEL3_INT	FIFO Level 3 Interrupt Pending This level sensitive interrupt is set by the FIFO whenever FIFO 3 meets the FIFO_STA_CFG.LEVEL3.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Default Value: 0
25	FIFO_LEVEL2_INT	FIFO Level 2 Interrupt Pending This level sensitive interrupt is set by the FIFO whenever FIFO 2 meets the FIFO_STA_CFG.LEVEL2.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Default Value: 0
24 : 21	RESERVED_2	Default Value: 0
20	FIFO_LEVEL1_INT	FIFO Level 1 Interrupt Pending This level sensitive interrupt is set by the FIFO whenever FIFO 1 meets the FIFO_STA_CFG.LEVEL1.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=1,2, or 3) Default Value: 0
19 : 18	RESERVED_1	Default Value: 0
17	FIFO_LEVEL0_INT	FIFO Level 0 Interrupt Pending This level sensitive interrupt is set by the FIFO whenever FIFO 0 meets the FIFO_STA_CFG.LEVEL0.LEVEL condition. Default Value: 0
16	RESERVED_0	Default Value: 0
15	FIFO_UNDERFLOW7_INT	FIFO Underflow 7 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 7 underflows (i.e. a read from FIFO 7 fails because FIFO 7 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
14	FIFO_UNDERFLOW6_INT	FIFO Underflow 6 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 6 underflows (i.e. a read from FIFO 6 fails because FIFO 6 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
13	FIFO_UNDERFLOW5_INT	FIFO Underflow 5 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 5 underflows (i.e. a read from FIFO 5 fails because FIFO 5 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0

28.1.115 LPPASS_MMIO_FIFO_INTR_CAUSE (continued)

12	FIFO_UNDER-FLOW4_INT	FIFO Underflow 4 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 4 underflows (i.e. a read from FIFO 4 fails because FIFO 4 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
11	FIFO_UNDER-FLOW3_INT	FIFO Overflow 3 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 3 underflows (i.e. a read from FIFO 3 fails because FIFO 3 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Default Value: 0
10	FIFO_UNDER-FLOW2_INT	FIFO Overflow 2 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 2 underflows (i.e. a read from FIFO 2 fails because FIFO 2 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Default Value: 0
9	FIFO_UNDER-FLOW1_INT	FIFO Overflow 1 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 1 underflows (i.e. a read from FIFO 1 fails because FIFO 1 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=1,2, or 3) Default Value: 0
8	FIFO_UNDER-FLOW0_INT	FIFO Underflow 0 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 0 underflows (i.e. a read from FIFO 0 fails because FIFO 0 is empty. Default Value: 0
7	FIFO_OVERFLOW7_INT	FIFO Overflow 7 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 7 overflows (i.e. a write to FIFO 7 fails because FIFO 7 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
6	FIFO_OVERFLOW6_INT	FIFO Overflow 6 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 6 overflows (i.e. a write to FIFO 6 fails because FIFO 6 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
5	FIFO_OVERFLOW5_INT	FIFO Overflow 5 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 5 overflows (i.e. a write to FIFO 5 fails because FIFO 5 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
4	FIFO_OVERFLOW4_INT	FIFO Overflow 4 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 4 overflows (i.e. a write to FIFO 4 fails because FIFO 4 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
3	FIFO_OVERFLOW3_INT	FIFO Overflow 3 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 3 overflows (i.e. a write to FIFO 3 fails because FIFO 3 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Default Value: 0

28.1.115 LPPASS_MMIO_FIFO_INTR_CAUSE (continued)

2	FIFO_OVERFLOW2_INT	FIFO Overflow 2 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 2 overflows (i.e. a write to FIFO 2 fails because FIFO 2 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Default Value: 0
1	FIFO_OVERFLOW1_INT	FIFO Overflow 1 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 1 overflows (i.e. a write to FIFO 1 fails because FIFO 1 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=1,2, or 3) Default Value: 0
0	FIFO_OVERFLOW0_INT	FIFO Overflow 0 Interrupt Pending This interrupt is set by the FIFO whenever FIFO 0 overflows (i.e. a write to FIFO 0 fails because FIFO 0 is full). Default Value: 0

28.1.116 LPPASS_MMIO_TR_OUT0

Description: Trigger out select register

Address: 0x42EF0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PTC_RANGE1	PTC_RANGE0	PTC_-COMP1	PTC_-COMP0	CTBL1_-COMP1	CTBL1_-COMP0	CTBL0_-COMP1	CTBL0_-COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	DAC1_RANGE2	DAC1_RANGE1	DAC1_RANGE0	RE-SERVED_4	DAC0_EP-OCH	DAC0_RANGE2	DAC0_RANGE1	DAC0_RANGE0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SAR_RANGE2	SAR_RANGE1	SAR_RANGE0	FIFO_LEV-EL1	SAR_EOS	SAR_DONE	FIFO_LEV-EL0	DAC1_EP-OCH

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	AC	FIFO_LEV-EL7	FIFO_LEV-EL6	FIFO_LEV-EL5	FIFO_LEV-EL4	FIFO_LEV-EL3	FIFO_LEV-EL2	SAR_RANGE3

Bits	Name	Description
31	AC	Autonomus Controller Trigger This trigger is set by the Autonomus Controller whenever executing a state with ACTRLR.TIM-ER_TABLE_STRUCT.TT_CFG1.INTR_SET=1. Default Value: 0
30	FIFO_LEVEL7	FIFO Level 7 Trigger This level sensitive trigger is set by the FIFO whenever FIFO 7 meets the FIFO_STA_CFG.LEV-EL7.LEVEL condition. This trigger is only generated if the FIFO is configured for multiple FIFOs (i.e. FI-FO_STA_CFG.CFG.SEL=3) Default Value: 0
29	FIFO_LEVEL6	FIFO Level 6 Trigger This level sensitive trigger is set by the FIFO whenever FIFO 6 meets the FIFO_STA_CFG.LEV-EL6.LEVEL condition. This trigger is only generated if the FIFO is configured for multiple FIFOs (i.e. FI-FO_STA_CFG.CFG.SEL=3) Default Value: 0
28	FIFO_LEVEL5	FIFO Level 5 Trigger This level sensitive trigger is set by the FIFO whenever FIFO 5 meets the FIFO_STA_CFG.LEV-EL5.LEVEL condition. This trigger is only generated if the FIFO is configured for multiple FIFOs (i.e. FI-FO_STA_CFG.CFG.SEL=3) Default Value: 0

28.1.116 LPPASS_MMIO_TR_OUT0 (continued)

27	FIFO_LEVEL4	FIFO Level 4 Trigger This level sensitive trigger is set by the FIFO whenever FIFO 4 meets the FIFO_STA_CFG.LEVEL4.LEVEL condition. This trigger is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Default Value: 0
26	FIFO_LEVEL3	FIFO Level 3 Trigger This level sensitive trigger is set by the FIFO whenever FIFO 3 meets the FIFO_STA_CFG.LEVEL3.LEVEL condition. This trigger is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Default Value: 0
25	FIFO_LEVEL2	FIFO Level 2 Trigger This level sensitive trigger is set by the FIFO whenever FIFO 2 meets the FIFO_STA_CFG.LEVEL2.LEVEL condition. This trigger is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Default Value: 0
24	SAR_RANGE3	SAR Range 3 Trigger This trigger is set by the SAR if the RANGE3 condition is met for a given channel with range 3 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_3). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the trigger. Default Value: 0
23	SAR_RANGE2	SAR Range 2 Trigger This trigger is set by the SAR if the RANGE2 condition is met for a given channel with range 2 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_2). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the trigger. Default Value: 0
22	SAR_RANGE1	SAR Range 1 Trigger This trigger is set by the SAR if the RANGE1 condition is met for a given channel with range 1 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_1). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the trigger. Default Value: 0
21	SAR_RANGE0	SAR Range 0 Trigger This trigger is set by the SAR if the RANGE0 condition is met for a given channel with range 0 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_0). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the trigger. Default Value: 0
20	FIFO_LEVEL1	FIFO Level 1 Trigger This level sensitive trigger is generated by the FIFO whenever FIFO 1 meets the FIFO_STA_CFG.LEVEL1.LEVEL condition. This trigger is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=1,2, or 3) Default Value: 0
19	SAR_EOS	SAR Sequencer EOS Trigger This itrigger is set by the SAR when finishing the state in the SAR sequencer table (HS or LP) where SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to GO_TO_ENTRY_ADDRESS or STOP. This trigger does NOT indicate that the SAR data has been written to the FIFO (the FIFO level triggers should be used instead). Default Value: 0

28.1.116 LPPASS_MMIO_TR_OUT0 (continued)

18	SAR_DONE	SAR Sequencer Done Trigger This trigger is set by the SAR when finishing a state in the SAR sequencer table (HS or LP) where SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to STOP. The interrupt is not generated if the SAR is configured for CONTINUOUS operation (i.e. SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to GO_TO_ENTRY_ADDRESS). This trigger does NOT indicate that the SAR data has been written to the FIFO (the FIFO level triggers should be used instead). Default Value: 0
17	FIFO_LEVEL0	FIFO Level 0 Trigger This is a level sensitive trigger that is generated by the FIFO whenever FIFO 0 meets the FIFO_STA_CFG.LEVEL0.LEVEL condition. Default Value: 0
16	DAC1_EPOCH	DAC1 End of Waveform Trigger It is generated by DAC1 when finishing a waveform. This condition is only used if the DAC1 channel (pointed to by the AC when triggered) is configured for LUT mode. Default Value: 0
15	DAC1_RANGE2	DAC1 Range 2 Trigger It is generated by the DAC1 if the RANGE2 condition is met for a given channel with range 2 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_2). The interrupt is disabled when DAC1 is configured for FW mode. Default Value: 0
14	DAC1_RANGE1	DAC1 Range 1 Trigger It is generated by the DAC1 if the RANGE1 condition is met for a given channel with range 1 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_1). The interrupt is disabled when DAC1 is configured for FW mode. Default Value: 0
13	DAC1_RANGE0	DAC1 Range 0 Trigger It is generated by the DAC1 if the RANGE0 condition is met for a given channel with range 0 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_0). The interrupt is disabled when DAC1 is configured for FW mode. Default Value: 0
12	RESERVED_4	Default Value: 0
11	DAC0_EPOCH	DAC0 End of Waveform Trigger It is generated by DAC0 when finishing a waveform. This condition is only used if the DAC0 channel (pointed to by the AC when triggered) is configured for LUT mode. Default Value: 0
10	DAC0_RANGE2	DAC0 Range 2 Trigger It is generated by the DAC0 if the RANGE2 condition is met for a given channel with range 2 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_2). The interrupt is disabled when DAC0 is configured for FW mode. Default Value: 0
9	DAC0_RANGE1	DAC0 Range 1 Trigger It is generated by the DAC0 if the RANGE1 condition is met for a given channel with range 1 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_1). The interrupt is disabled when DAC0 is configured for FW mode. Default Value: 0
8	DAC0_RANGE0	DAC0 Range 0 Trigger It is generated by the DAC0 if the RANGE0 condition is met for a given channel with range 0 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_SEL=STATUS_0). The interrupt is disabled when DAC0 is configured for FW mode. Default Value: 0
7	PTC_RANGE1	PTC Post Processor 1 Range Trigger It is generated by the PTC Post Processor if the RANGE0 condition is met (i.e. PTC_PP_STRUCT1.*). Default Value: 0

28.1.116 LPPASS_MMIO_TR_OUT0 (continued)

6	PTC_RANGE0	PTC Post Processor 0 Range Trigger It is generated by the PTC Post Processor if the RANGE0 condition is met (i.e. PTC_PP_-STRUCT0.*). Default Value: 0
5	PTC_COMP1	PTC Comparator 1 Interrupt Pending It is set by the PTC Comparator 1 if the condition is met (i.e. PTC_STA_CFG.CFG.COMP1_OUT field). Default Value: 0
4	PTC_COMP0	PTC Comparator 0 Trigger It is set by the PTC Comparator 0 if the condition is met (i.e. PTC_STA_CFG.CFG.COMP0_OUT field). Default Value: 0
3	CTBL1_COMP1	CTBL1 Comparator 1 Trigger It is generated by the CTBL1 Opamp1 Comparator if the condition is met (i.e. CT-BL_STA_CFG.CFG.COMP1_OUT field). Default Value: 0
2	CTBL1_COMP0	CTBL1 Comparator 0 Trigger It is generated by the CTBL1 Opamp0 Comparator if the condition is met (i.e. CT-BL_STA_CFG.CFG.COMP0_OUT field). Default Value: 0
1	CTBL0_COMP1	CTBL0 Comparator 1 Trigger It is generated by the CTBL0 Opamp1 Comparator if the condition is met (i.e. CT-BL_STA_CFG.CFG.COMP1_OUT field). Default Value: 0
0	CTBL0_COMP0	CTBL0 Comparator 0 Trigger It is generated by the CTBL0 Opamp0 Comparator if the condition is met (i.e. CT-BL_STA_CFG.CFG.COMP0_OUT field). Default Value: 0

28.1.117 LPPASS_MMIO_INTR

Description: Interrupt request register

Address: 0x42EF0040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	PTC_RANGE1	PTC_RANGE0	PTC_-COMP1	PTC_-COMP0	CTBL1_-COMP1	CTBL1_-COMP0	CTBL0_-COMP1	CTBL0_-COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	DAC1_RANGE2	DAC1_RANGE1	DAC1_RANGE0	DAC0_EMPTY	DAC0_EP-OCH	DAC0_RANGE2	DAC0_RANGE1	DAC0_RANGE0

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	SAR_RANGE2	SAR_RANGE1	SAR_RANGE0	SAR_RE-SULT	SAR_EOS	SAR_DONE	DAC1_EMPTY	DAC1_EP-OCH

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	RW1C				RW1C	RW1C	RW1C
HW Access	RW1S	RW1S				RW1S	RW1S	RW1S
Name	AC	RESERVED [30:27]				SAR_-FIR1_RE-SULT	SAR_-FIR0_RE-SULT	SAR_RANGE3

Bits	Name	Description
31	AC	Autonomus Controller Interrupt Request AC Interrupt: hardware sets this interrupt when the Autonomus Controller executes a state with ACTRLR.TIMER_TABLE_STRUCT.TT_CFG1.INTR_SET=1. Default Value: 0
30 : 27	RESERVED	Default Value: 0
26	SAR_FIR1_RESULT	FIR1 Result Interrupt Request SAR FIR1 Result Interrupt: hardware sets this interrupt when SAR FIR1 generates a new result. The corresponding bit in SAR_STA_CFG.FIR_RESULT_MASK must be set in order for the FIR to generate the interrupt source. Write a '1' to clear bit. Default Value: 0
25	SAR_FIR0_RESULT	FIR0 Result Interrupt Request SAR FIR0 Result Interrupt: hardware sets this interrupt when SAR FIR0 generates a new result. The corresponding bit in SAR_STA_CFG.FIR_RESULT_MASK must be set in order for the FIR to generate the interrupt source. Write a '1' to clear bit. Default Value: 0

28.1.117 LPPASS_MMIO_INTR (continued)

24	SAR_RANGE3	SAR Range 3 detection Interrupt Request SAR Range 3 Interrupt: hardware sets this interrupt when the SAR RANGE3 condition is met for a given channel with range 3 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_3). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the interrupt. Write a '1' to clear bit. Default Value: 0
23	SAR_RANGE2	SAR Range2 detection Interrupt Request SAR Range 2 Interrupt: hardware sets this interrupt when the SAR RANGE2 condition is met for a given channel with range 2 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_2). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the interrupt. Write a '1' to clear bit. Default Value: 0
22	SAR_RANGE1	SAR Range 1 detection Interrupt Request SAR Range 1 Interrupt: hardware sets this interrupt when the SAR RANGE1 condition is met for a given channel with range 1 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_1). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the interrupt. Write a '1' to clear bit. Default Value: 0
21	SAR_RANGE0	SAR Range 0 detection Interrupt Request SAR Range 0 Interrupt: hardware sets this interrupt when the SAR RANGE0 condition is met for a given channel with range 0 status enabled (i.e. SAR_STA_CFG.GPIO(MUX)_CHAN_CFG.STATUS_SEL=STATUS_STRUCT_0). Firmware must read SAR_STA_CFG.RANGE_STATUS to determine which channel generated the interrupt. Write a '1' to clear bit. Default Value: 0
20	SAR_RESULT	SAR Result Interrupt Request SAR Result Interrupt: hardware sets this interrupt when the SAR channel writes data into its associated result register. Firmware must read SAR_STA_CFG.CHAN_RESULT_UPDATED to determine which channel generated the interrupt. The corresponding bit in SAR_STA_CFG.CHAN_RESULT_MASK must be set in order for the SAR to generate the interrupt source. Write a '1' to clear bit. Default Value: 0
19	SAR_EOS	SAR Sequencer EOS Interrupt Request SAR Sequencer EOS Interrupt: hardware sets this interrupt when the SAR finishes the state in the SAR sequencer table (HS or LP) where SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to GO_TO_ENTRY_ADDRESS or STOP. This interrupt does NOT indicate that the SAR data has been written to the FIFO (the FIFO level interrupts should be used instead). Write a '1' to clear bit. Default Value: 0
18	SAR_DONE	SAR Sequencer Done Interrupt Request SAR Done Interrupt: hardware sets this interrupt when the SAR finishes a state in the SAR sequencer table (HS or LP) where SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to STOP. The interrupt is not generated if the SAR is configured for CONTINUOUS operation (i.e. SAR.SEQ_HS(LP)_DATA.NEXT_STATE is set to GO_TO_ENTRY_ADDRESS). This interrupt does NOT indicate that the SAR data has been written to the FIFO (the FIFO level interrupts should be used instead). Write a '1' to clear bit. Default Value: 0

28.1.117 LPPASS_MMIO_INTR (continued)

17	DAC1_EMPTY	DAC1 Empty Interrupt Request DAC1 Empty Interrupt: hardware sets this interrupt when DAC1 empties the contents of its FW_-DAC_VAL register. This interrupt is only generated if DAC1 is configured for FW operation (AC-TRLR.TIMER_TABLE_STRUCT.TT_CFG3.DAC1_CHANNEL=FW_CHANNEL. Write a '1' to clear bit. Default Value: 0
16	DAC1_EPOCH	DAC1 End of Waveform Interrupt Request DAC1 EPOCH Interrupt: hardware sets this interrupt when DAC1 finishes a waveform. This condition is only used if the DAC1 channel (pointed to by the AC when triggered) is configured for LUT mode. Write a '1' to clear bit. Default Value: 0
15	DAC1_RANGE2	DAC1 Range 2 Interrupt Request DAC1 RANGE2 Interrupt: hardware sets this interrupt if the DAC1 RANGE2 condition is met for a given channel with range 2 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_-SEL=STATUS_2). The interrupt is disabled when DAC1 is configured for FW mode. Write with '1' to clear bit. Default Value: 0
14	DAC1_RANGE1	DAC1 Range 1 Interrupt Request DAC1 RANGE1 Interrupt: hardware sets this interrupt if the DAC0 RANGE1 condition is met for a given channel with range 1 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_-SEL=STATUS_1). The interrupt is disabled when DAC1 is configured for FW mode. Write with '1' to clear bit. Default Value: 0
13	DAC1_RANGE0	DAC1 Range 0 Interrupt Request DAC1 RANGE0 Interrupt: hardware sets this interrupt if the DAC1 RANGE0 condition is met for a given channel with range 0 status enabled (i.e. DAC1_STA_CFG.CHAN_CFG.STATUS_-SEL=STATUS_0). The interrupt is disabled when DAC1 is configured for FW mode. Write with '1' to clear bit. Default Value: 0
12	DAC0_EMPTY	DAC0 Empty Interrupt Request DAC0 Empty Interrupt: hardware sets this interrupt when DAC0 empties the contents of its FW_-DAC_VAL register. This interrupt is only generated if DAC0 is configured for FW operation (AC-TRLR.TIMER_TABLE_STRUCT.TT_CFG3.DAC0_CHANNEL=FW_CHANNEL. Write a '1' to clear bit. Default Value: 0
11	DAC0_EPOCH	DAC0 End of Waveform Interrupt Request DAC0 EPOCH Interrupt: hardware sets this interrupt when DAC0 finishes a waveform. This condition is only used if the DAC0 channel (pointed to by the AC when triggered) is configured for LUT mode. Write a '1' to clear bit. Default Value: 0
10	DAC0_RANGE2	DAC0 Range 2 Interrupt Request DAC0 RANGE2 Interrupt: hardware sets this interrupt if the DAC0 RANGE2 condition is met for a given channel with range 2 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_-SEL=STATUS_2). The interrupt is disabled when DAC0 is configured for FW mode. Write with '1' to clear bit. Default Value: 0
9	DAC0_RANGE1	DAC0 Range 1 Interrupt Request DAC0 RANGE1 Interrupt: hardware sets this interrupt if the DAC0 RANGE1 condition is met for a given channel with range 1 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_-SEL=STATUS_1). The interrupt is disabled when DAC0 is configured for FW mode. Write with '1' to clear bit. Default Value: 0
8	DAC0_RANGE0	DAC0 Range 0 Interrupt Request DAC0 RANGE0 Interrupt: hardware sets this interrupt if the DAC0 RANGE0 condition is met for a given channel with range 0 status enabled (i.e. DAC0_STA_CFG.CHAN_CFG.STATUS_-SEL=STATUS_0). The interrupt is disabled when DAC0 is configured for FW mode. Write with '1' to clear bit. Default Value: 0

28.1.117 LPPASS_MMIO_INTR (continued)

7	PTC_RANGE1	PTC Post Processor 1 Range Interrupt Request PTC RANGE1 Interrupt: hardware sets this interrupt if the PTC Post Processor RANGE1 condition is met (i.e. PTC_PP_STRUCT1.*). Write with '1' to clear bit. Default Value: 0
6	PTC_RANGE0	PTC Post Processor 0 Range Interrupt Request PTC RANGE0 Interrupt: hardware sets this interrupt if the PTC Post Processor RANGE0 condition is met (i.e. PTC_PP_STRUCT0.*). Write with '1' to clear bit. Default Value: 0
5	PTC_COMP1	PTC Comparator 1 Interrupt Request PTC COMP1 Interrupt: hardware sets this interrupt if the condition is met (i.e. PTC_STA_CFG.CFG.COMP1_OUT field). Write with '1' to clear bit. Default Value: 0
4	PTC_COMP0	PTC Comparator 0 Interrupt Request PTC COMP0 Interrupt: hardware sets this interrupt if the condition is met (i.e. PTC_STA_CFG.CFG.COMP0_OUT field). Write with '1' to clear bit. Default Value: 0
3	CTBL1_COMP1	CTBL1 Comparator 1 Interrupt Request CTBL1 COMP1 Interrupt: hardware sets this interrupt if the condition is met (i.e. CTBL_STA_CFG.CFG.COMP1_OUT field). Write with '1' to clear bit. Default Value: 0
2	CTBL1_COMP0	CTBL1 Comparator 0 Interrupt Request CTBL1 COMP0 Interrupt: hardware sets this interrupt if the condition is met (i.e. CTBL_STA_CFG.CFG.COMP0_OUT field). Write with '1' to clear bit. Default Value: 0
1	CTBL0_COMP1	CTBL0 Comparator 1 Interrupt Request CTBL0 COMP1 Interrupt: hardware sets this interrupt if the condition is met (i.e. CTBL_STA_CFG.CFG.COMP1_OUT field). Write with '1' to clear bit. Default Value: 0
0	CTBL0_COMP0	CTBL0 Comparator 0 Interrupt Request CTBL0 COMP0 Interrupt: hardware sets this interrupt if the condition is met (i.e. CTBL_STA_CFG.CFG.COMP0_OUT field). Write with '1' to clear bit. Default Value: 0

28.1.118 LPPASS_MMIO_INTR_SET

Description: Interrupt request set register

Address: 0x42EF0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	PTC_RANGE1_SET	PTC_RANGE0_SET	PTC_-COMP1_SET	PTC_-COMP0_SET	CTBL1_-COMP1_SET	CTBL1_-COMP0_SET	CTBL0_-COMP1_SET	CTBL0_-COMP0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	DAC1_RANGE2_SET	DAC1_RANGE1_SET	DAC1_RANGE0_SET	DAC0_EMPTY_SET	DAC0_EP-OCH_SET	DAC0_RANGE2_SET	DAC0_RANGE1_SET	DAC0_RANGE0_SET

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	SAR_RANGE2_SET	SAR_RANGE1_SET	SAR_RANGE0_SET	SAR_RE-SULT_SET	SAR_EOS_SET	SAR_-DONE_SET	DAC1_EMPTY_SET	DAC1_EP-OCH_SET

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW1S				RW1S	RW1S	RW1S
HW Access	A	A				A	A	A
Name	AC_SET	RESERVED [30:27]				SAR_-FIR1_RE-SULT_SET	SAR_-FIR0_RE-SULT_SET	SAR_RANGE3_SET

Bits	Name	Description
31	AC_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
30 : 27	RESERVED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
26	SAR_FIR1_RESULT_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
25	SAR_FIR0_RESULT_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
24	SAR_RANGE3_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
23	SAR_RANGE2_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
22	SAR_RANGE1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
21	SAR_RANGE0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.118 LPPASS_MMIO_INTR_SET (continued)

20	SAR_RESULT_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
19	SAR_EOS_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
18	SAR_DONE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
17	DAC1_EMPTY_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
16	DAC1_EPOCH_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
15	DAC1_RANGE2_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
14	DAC1_RANGE1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
13	DAC1_RANGE0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
12	DAC0_EMPTY_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
11	DAC0_EPOCH_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	DAC0_RANGE2_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	DAC0_RANGE1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	DAC0_RANGE0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	PTC_RANGE1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	PTC_RANGE0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	PTC_COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	PTC_COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	CTBL1_COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	CTBL1_COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	CTBL0_COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	CTBL0_COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.119 LPPASS_MMIO_INTR_MASK

Description: Interrupt request mask

Address: 0x42EF0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PTC_RANGE1_MASK	PTC_RANGE0_MASK	PTC_-COMP1_MASK	PTC_-COMP0_MASK	CTBL1_-COMP1_MASK	CTBL1_-COMP0_MASK	CTBL0_-COMP1_MASK	CTBL0_-COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	DAC1_RANGE2_MASK	DAC1_RANGE1_MASK	DAC1_RANGE0_MASK	DAC0_EMPTY_MASK	DAC0_EP-OCH_MASK	DAC0_RANGE2_MASK	DAC0_RANGE1_MASK	DAC0_RANGE0_MASK

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SAR_RANGE2_MASK	SAR_RANGE1_MASK	SAR_RANGE0_MASK	SAR_RE-SULT_MASK	SAR_EOS_MASK	SAR_-DO-NE_MASK	DAC1_EMPTY_MASK	DAC1_EP-OCH_MASK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW				RW	RW	RW
HW Access	R	R				R	R	R
Name	AC_MASK	RESERVED [30:27]				SAR_-FIR1_RE-SULT_MASK	SAR_-FIR0_RE-SULT_MASK	SAR_RANGE3_MASK

Bits	Name	Description
31	AC_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
30 : 27	RESERVED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
26	SAR_FIR1_RE-SULT_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
25	SAR_FIR0_RE-SULT_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
24	SAR_RANGE3_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
23	SAR_RANGE2_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
22	SAR_RANGE1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.119 LPPASS_MMIO_INTR_MASK (continued)

21	SAR_RANGE0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
20	SAR_RESULT_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
19	SAR_EOS_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
18	SAR_DONE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
17	DAC1_EMPTY_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
16	DAC1_EPOCH_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
15	DAC1_RANGE2_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
14	DAC1_RANGE1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
13	DAC1_RANGE0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
12	DAC0_EMPTY_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
11	DAC0_EPOCH_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	DAC0_RANGE2_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	DAC0_RANGE1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	DAC0_RANGE0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	PTC_RANGE1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	PTC_RANGE0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	PTC_COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	PTC_COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	CTBL1_COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	CTBL1_COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	CTBL0_COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	CTBL0_COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.120 LPPASS_MMIO_INTR_MASKED

Description: Interrupt request masked

Address: 0x42EF0058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PTC_RANGE1_MASKED	PTC_RANGE0_MASKED	PTC_-COMP1_MASKED	PTC_-COMP0_MASKED	CTBL1_-COMP1_MASKED	CTBL1_-COMP0_MASKED	CTBL0_-COMP1_MASKED	CTBL0_-COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DAC1_RANGE2_MASKED	DAC1_RANGE1_MASKED	DAC1_RANGE0_MASKED	DAC0_EMPTY_MASKED	DAC0_EP-OCH_MASKED	DAC0_RANGE2_MASKED	DAC0_RANGE1_MASKED	DAC0_RANGE0_MASKED

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	SAR_RANGE2_MASKED	SAR_RANGE1_MASKED	SAR_RANGE0_MASKED	SAR_RE-SULT_MASKED	SAR_EOS_MASKED	SAR_-DO-NE_MASKED	DAC1_EMPTY_MASKED	DAC1_EP-OCH_MASKED

Bits	31	30	29	28	27	26	25	24
SW Access	R	R				R	R	R
HW Access	W	W				W	W	W
Name	AC_MASKED	RESERVED [30:27]				SAR_-FIR1_RE-SULT_MASKED	SAR_-FIR0_RE-SULT_MASKED	SAR_RANGE3_MASKED

Bits	Name	Description
31	AC_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
30 : 27	RESERVED	Logical and of corresponding request and mask bits. Default Value: 0
26	SAR_FIR1_RE-SULT_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
25	SAR_FIR0_RE-SULT_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
24	SAR_RANGE3_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
23	SAR_RANGE2_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
22	SAR_RANGE1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

28.1.120 LPPASS_MMIO_INTR_MASKED (continued)

21	SAR_RANGE0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
20	SAR_RESULT_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
19	SAR_EOS_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
18	SAR_DONE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
17	DAC1_EMPTY_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
16	DAC1_EPOCH_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
15	DAC1_RANGE2_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
14	DAC1_RANGE1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
13	DAC1_RANGE0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
12	DAC0_EMPTY_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
11	DAC0_EPOCH_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
10	DAC0_RANGE2_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
9	DAC0_RANGE1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
8	DAC0_RANGE0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
7	PTC_RANGE1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
6	PTC_RANGE0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
5	PTC_COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
4	PTC_COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3	CTBL1_-COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	CTBL1_-COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	CTBL0_-COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	CTBL0_-COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

28.1.121 LPPASS_MMIO_FIFO_INTR

Description: FIFO Interrupt request register

Address: 0x42EF0060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	FIFO_OVERFLOW7	FIFO_OVERFLOW6	FIFO_OVERFLOW5	FIFO_OVERFLOW4	FIFO_OVERFLOW3	FIFO_OVERFLOW2	FIFO_OVERFLOW1	FIFO_OVERFLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	FIFO_UNDERFLOW7	FIFO_UNDERFLOW6	FIFO_UNDERFLOW5	FIFO_UNDERFLOW4	FIFO_UNDERFLOW3	FIFO_UNDERFLOW2	FIFO_UNDERFLOW1	FIFO_UNDERFLOW0

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C			R	RW1C		R	RW1C
HW Access	RW1S			W	RW1S		W	RW1S
Name	RESERVED_2 [23:21]			FIFO_LEVEL1	RESERVED_1 [19:18]		FIFO_LEVEL0	RESERVED_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	R	R	R	R	R	R	RW1C
HW Access	RW1S	W	W	W	W	W	W	RW1S
Name	RESERVED_3	FIFO_LEVEL7	FIFO_LEVEL6	FIFO_LEVEL5	FIFO_LEVEL4	FIFO_LEVEL3	FIFO_LEVEL2	RESERVED_2

Bits	Name	Description
31	RESERVED_3	Default Value: 0
30	FIFO_LEVEL7	FIFO Level 7 Interrupt Request FIFO Level 7 Interrupt: hardware sets this level sensitive interrupt whenever FIFO 7 meets the FIFO_STA_CFG.LEVEL7.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) This interrupt is only cleared when the contents of FIFO drop below the FIFO_STA_CFG.LEVEL7.LEVEL condition. Default Value: 0
29	FIFO_LEVEL6	FIFO Level 6 Interrupt Request FIFO Level 6 Interrupt: hardware sets this level sensitive interrupt whenever FIFO 6 meets the FIFO_STA_CFG.LEVEL6.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) This interrupt is only cleared when the contents of FIFO drop below the FIFO_STA_CFG.LEVEL6.LEVEL condition. Default Value: 0

28.1.121 LPPASS_MMIO_FIFO_INTR (continued)

28	FIFO_LEVEL5	FIFO Level 5 Interrupt Request FIFO Level 5 Interrupt: hardware sets this level sensitive interrupt whenever FIFO 5 meets the FIFO_STA_CFG.LEVEL5.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) This interrupt is only cleared when the contents of FIFO drop below the FIFO_STA_CFG.LEVEL5.LEVEL condition. Default Value: 0
27	FIFO_LEVEL4	FIFO Level 4 Interrupt Request FIFO Level 4 Interrupt: hardware sets this level sensitive interrupt whenever FIFO 4 meets the FIFO_STA_CFG.LEVEL4.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) This interrupt is only cleared when the contents of FIFO drop below the FIFO_STA_CFG.LEVEL4.LEVEL condition. Default Value: 0
26	FIFO_LEVEL3	FIFO Level 3 Interrupt Request FIFO Level 3 Interrupt: hardware sets this level sensitive interrupt whenever FIFO 3 meets the FIFO_STA_CFG.LEVEL3.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) This interrupt is only cleared when the contents of FIFO drop below the FIFO_STA_CFG.LEVEL3.LEVEL condition. Default Value: 0
25	FIFO_LEVEL2	FIFO Level 2 Interrupt Request FIFO Level 2 Interrupt: hardware sets this level sensitive interrupt whenever FIFO 2 meets the FIFO_STA_CFG.LEVEL2.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) This interrupt is only cleared when the contents of FIFO drop below the FIFO_STA_CFG.LEVEL2.LEVEL condition. Default Value: 0
24 : 21	RESERVED_2	Default Value: 0
20	FIFO_LEVEL1	FIFO Level 1 Interrupt Request FIFO Level 1 Interrupt: hardware sets this level sensitive interrupt whenever FIFO 1 meets the FIFO_STA_CFG.LEVEL1.LEVEL condition. This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=1,2, or 3) This interrupt is only cleared when the contents of FIFO drop below the FIFO_STA_CFG.LEVEL1.LEVEL condition. Default Value: 0
19 : 18	RESERVED_1	Default Value: 0
17	FIFO_LEVEL0	FIFO Level 0 Interrupt Request FIFO Level 0 Interrupt: hardware sets this level sensitive interrupt whenever FIFO 0 meets the FIFO_STA_CFG.LEVEL0.LEVEL condition. This interrupt is only cleared when the contents of FIFO drop below the FIFO_STA_CFG.LEVEL0.LEVEL condition. Default Value: 0
16	RESERVED_0	Default Value: 0
15	FIFO_UNDERFLOW7	FIFO Overflow 7 Interrupt Request FIFO Overflow 7 Interrupt: hardware sets this interrupt whenever FIFO 7 underflows (i.e. a read from FIFO 7 fails because FIFO 7 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Write a '1' to clear bit. Default Value: 0

28.1.121 LPPASS_MMIO_FIFO_INTR (continued)

14	FIFO_UNDERFLOW6	FIFO Overflow 6 Interrupt Request FIFO Overflow 6 Interrupt: hardware sets this interrupt whenever FIFO 6 underflows (i.e. a read from FIFO 6 fails because FIFO 6 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Write a '1' to clear bit. Default Value: 0
13	FIFO_UNDERFLOW5	FIFO Overflow 5 Interrupt Request FIFO Overflow 5 Interrupt: hardware sets this interrupt whenever FIFO 5 underflows (i.e. a read from FIFO 5 fails because FIFO 5 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Write a '1' to clear bit. Default Value: 0
12	FIFO_UNDERFLOW4	FIFO Overflow 4 Interrupt Request FIFO Overflow 4 Interrupt: hardware sets this interrupt whenever FIFO 4 underflows (i.e. a read from FIFO 4 fails because FIFO 4 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Write a '1' to clear bit. Default Value: 0
11	FIFO_UNDERFLOW3	FIFO Overflow 3 Interrupt Request FIFO Overflow 3 Interrupt: hardware sets this interrupt whenever FIFO 3 underflows (i.e. a read from FIFO 3 fails because FIFO 3 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Write a '1' to clear bit. Default Value: 0
10	FIFO_UNDERFLOW2	FIFO Overflow 2 Interrupt Request FIFO Overflow 2 Interrupt: hardware sets this interrupt whenever FIFO 2 underflows (i.e. a read from FIFO 2 fails because FIFO 2 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Write a '1' to clear bit. Default Value: 0
9	FIFO_UNDERFLOW1	FIFO Overflow 1 Interrupt Request FIFO Underflow 1 Interrupt: hardware sets this interrupt whenever FIFO 1 underflows (i.e. a read from FIFO 1 fails because FIFO 1 is empty). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=1,2, or 3) Write a '1' to clear bit. Default Value: 0
8	FIFO_UNDERFLOW0	FIFO Underflow 0 Interrupt Request FIFO Underflow 0 Interrupt: hardware sets this interrupt whenever FIFO 0 underflows (i.e. a read from FIFO 0 fails because FIFO 0 is empty. Write a '1' to clear bit. Default Value: 0
7	FIFO_OVERFLOW7	FIFO Overflow 7 Interrupt Request FIFO Overflow 7 Interrupt: hardware sets this interrupt whenever FIFO 7 overflows (i.e. a write to FIFO 7 fails because FIFO 7 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Write a '1' to clear bit. Default Value: 0
6	FIFO_OVERFLOW6	FIFO Overflow 6 Interrupt Request FIFO Overflow 6 Interrupt: hardware sets this interrupt whenever FIFO 6 overflows (i.e. a write to FIFO 6 fails because FIFO 6 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Write a '1' to clear bit. Default Value: 0

28.1.121 LPPASS_MMIO_FIFO_INTR (continued)

5	FIFO_OVERFLOW5	FIFO Overflow 5 Interrupt Request FIFO Overflow 5 Interrupt: hardware sets this interrupt whenever FIFO 5 overflows (i.e. a write to FIFO 5 fails because FIFO 5 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Write a '1' to clear bit. Default Value: 0
4	FIFO_OVERFLOW4	FIFO Overflow 4 Interrupt Request FIFO Overflow 4 Interrupt: hardware sets this interrupt whenever FIFO 4 overflows (i.e. a write to FIFO 4 fails because FIFO 4 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=3) Write a '1' to clear bit. Default Value: 0
3	FIFO_OVERFLOW3	FIFO Overflow 3 Interrupt Request FIFO Overflow 3 Interrupt: hardware sets this interrupt whenever FIFO 3 overflows (i.e. a write to FIFO 3 fails because FIFO 3 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Write a '1' to clear bit. Default Value: 0
2	FIFO_OVERFLOW2	FIFO Overflow 2 Interrupt Request FIFO Overflow 2 Interrupt: hardware sets this interrupt whenever FIFO 2 overflows (i.e. a write to FIFO 2 fails because FIFO 2 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=2, or 3) Write a '1' to clear bit. Default Value: 0
1	FIFO_OVERFLOW1	FIFO Overflow 1 Interrupt Request FIFO Overflow 1 Interrupt: hardware sets this interrupt whenever FIFO 1 overflows (i.e. a write to FIFO 1 fails because FIFO 1 is full). This interrupt is only generated if the FIFO is configured for multiple FIFOs (i.e. FIFO_STA_CFG.CFG.SEL=1,2, or 3) Write a '1' to clear bit. Default Value: 0
0	FIFO_OVERFLOW0	FIFO Overflow 0 Interrupt Request FIFO Overflow 0 Interrupt: hardware sets this interrupt whenever FIFO 0 overflows (i.e. a write to FIFO 0 fails because FIFO 0 is full). Write a '1' to clear bit. Default Value: 0

28.1.122 LPPASS_MMIO_FIFO_INTR_SET

Description: FIFO Interrupt set request register

Address: 0x42EF0068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	FIFO_OVERFLOW7_SET	FIFO_OVERFLOW6_SET	FIFO_OVERFLOW5_SET	FIFO_OVERFLOW4_SET	FIFO_OVERFLOW3_SET	FIFO_OVERFLOW2_SET	FIFO_OVERFLOW1_SET	FIFO_OVERFLOW0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	FIFO_UNDERFLOW7_SET	FIFO_UNDERFLOW6_SET	FIFO_UNDERFLOW5_SET	FIFO_UNDERFLOW4_SET	FIFO_UNDERFLOW3_SET	FIFO_UNDERFLOW2_SET	FIFO_UNDERFLOW1_SET	FIFO_UNDERFLOW0_SET

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S			RW	RW1S		RW	RW1S
HW Access	A			R	A		R	A
Name	RESERVED_2 [23:21]			FIFO_LEVEL1_SET	RESERVED_1 [19:18]		FIFO_LEVEL0_SET	RESERVED_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW	RW	RW	RW	RW	RW	RW1S
HW Access	A	R	R	R	R	R	R	A
Name	RESERVED_3	FIFO_LEVEL7_SET	FIFO_LEVEL6_SET	FIFO_LEVEL5_SET	FIFO_LEVEL4_SET	FIFO_LEVEL3_SET	FIFO_LEVEL2_SET	RESERVED_2

Bits	Name	Description
31	RESERVED_3	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
30	FIFO_LEVEL7_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
29	FIFO_LEVEL6_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
28	FIFO_LEVEL5_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
27	FIFO_LEVEL4_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
26	FIFO_LEVEL3_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
25	FIFO_LEVEL2_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
24 : 21	RESERVED_2	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

28.1.122 LPPASS_MMIO_FIFO_INTR_SET (continued)

20	FIFO_LEVEL1_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
19 : 18	RESERVED_1	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
17	FIFO_LEVEL0_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
16	RESERVED_0	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
15	FIFO_UNDER-FLOW7_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
14	FIFO_UNDER-FLOW6_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
13	FIFO_UNDER-FLOW5_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
12	FIFO_UNDER-FLOW4_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
11	FIFO_UNDER-FLOW3_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
10	FIFO_UNDER-FLOW2_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
9	FIFO_UNDER-FLOW1_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
8	FIFO_UNDER-FLOW0_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
7	FIFO_OVERFLOW7_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
6	FIFO_OVERFLOW6_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
5	FIFO_OVERFLOW5_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
4	FIFO_OVERFLOW4_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
3	FIFO_OVERFLOW3_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
2	FIFO_OVERFLOW2_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
1	FIFO_OVERFLOW1_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
0	FIFO_OVERFLOW0_SET	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

28.1.123 LPPASS_MMIO_FIFO_INTR_MASK

Description: FIFO Interrupt mask register

Address: 0x42EF0070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	FIFO_OVERFLOW7_MASK	FIFO_OVERFLOW6_MASK	FIFO_OVERFLOW5_MASK	FIFO_OVERFLOW4_MASK	FIFO_OVERFLOW3_MASK	FIFO_OVERFLOW2_MASK	FIFO_OVERFLOW1_MASK	FIFO_OVERFLOW0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	FIFO_UNDERFLOW7_MASK	FIFO_UNDERFLOW6_MASK	FIFO_UNDERFLOW5_MASK	FIFO_UNDERFLOW4_MASK	FIFO_UNDERFLOW3_MASK	FIFO_UNDERFLOW2_MASK	FIFO_UNDERFLOW1_MASK	FIFO_UNDERFLOW0_MASK

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW	RW		RW	RW
HW Access	R			R	R		R	R
Name	RESERVED_2 [23:21]			FIFO_LEVEL1_MASK	RESERVED_1 [19:18]		FIFO_LEVEL0_MASK	RESERVED_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RESERVED_3	FIFO_LEVEL7_MASK	FIFO_LEVEL6_MASK	FIFO_LEVEL5_MASK	FIFO_LEVEL4_MASK	FIFO_LEVEL3_MASK	FIFO_LEVEL2_MASK	RESERVED_2

Bits	Name	Description
31	RESERVED_3	Mask for corresponding field in INTR register. Default Value: 0
30	FIFO_LEVEL7_MASK	Mask for corresponding field in INTR register. Default Value: 0
29	FIFO_LEVEL6_MASK	Mask for corresponding field in INTR register. Default Value: 0
28	FIFO_LEVEL5_MASK	Mask for corresponding field in INTR register. Default Value: 0
27	FIFO_LEVEL4_MASK	Mask for corresponding field in INTR register. Default Value: 0
26	FIFO_LEVEL3_MASK	Mask for corresponding field in INTR register. Default Value: 0
25	FIFO_LEVEL2_MASK	Mask for corresponding field in INTR register. Default Value: 0
24 : 21	RESERVED_2	Mask for corresponding field in INTR register. Default Value: 0

28.1.123 LPPASS_MMIO_FIFO_INTR_MASK (continued)

20	FIFO_LEVEL1_MASK	Mask for corresponding field in INTR register. Default Value: 0
19 : 18	RESERVED_1	Mask for corresponding field in INTR register. Default Value: 0
17	FIFO_LEVEL0_MASK	Mask for corresponding field in INTR register. Default Value: 0
16	RESERVED_0	Mask for corresponding field in INTR register. Default Value: 0
15	FIFO_UNDER-FLOW7_MASK	Mask for corresponding field in INTR register. Default Value: 0
14	FIFO_UNDER-FLOW6_MASK	Mask for corresponding field in INTR register. Default Value: 0
13	FIFO_UNDER-FLOW5_MASK	Mask for corresponding field in INTR register. Default Value: 0
12	FIFO_UNDER-FLOW4_MASK	Mask for corresponding field in INTR register. Default Value: 0
11	FIFO_UNDER-FLOW3_MASK	Mask for corresponding field in INTR register. Default Value: 0
10	FIFO_UNDER-FLOW2_MASK	Mask for corresponding field in INTR register. Default Value: 0
9	FIFO_UNDER-FLOW1_MASK	Mask for corresponding field in INTR register. Default Value: 0
8	FIFO_UNDER-FLOW0_MASK	Mask for corresponding field in INTR register. Default Value: 0
7	FIFO_OVER-FLOW7_MASK	Mask for corresponding field in INTR register. Default Value: 0
6	FIFO_OVER-FLOW6_MASK	Mask for corresponding field in INTR register. Default Value: 0
5	FIFO_OVER-FLOW5_MASK	Mask for corresponding field in INTR register. Default Value: 0
4	FIFO_OVER-FLOW4_MASK	Mask for corresponding field in INTR register. Default Value: 0
3	FIFO_OVER-FLOW3_MASK	Mask for corresponding field in INTR register. Default Value: 0
2	FIFO_OVER-FLOW2_MASK	Mask for corresponding field in INTR register. Default Value: 0
1	FIFO_OVER-FLOW1_MASK	Mask for corresponding field in INTR register. Default Value: 0
0	FIFO_OVER-FLOW0_MASK	Mask for corresponding field in INTR register. Default Value: 0

28.1.124 LPPASS_MMIO_FIFO_INTR_MASKED

Description: FIFO Interrupt masked request register

Address: 0x42EF0078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	FIFO_OVERFLOW7_MASKED	FIFO_OVERFLOW6_MASKED	FIFO_OVERFLOW5_MASKED	FIFO_OVERFLOW4_MASKED	FIFO_OVERFLOW3_MASKED	FIFO_OVERFLOW2_MASKED	FIFO_OVERFLOW1_MASKED	FIFO_OVERFLOW0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	FIFO_UNDERFLOW7_MASKED	FIFO_UNDERFLOW6_MASKED	FIFO_UNDERFLOW5_MASKED	FIFO_UNDERFLOW4_MASKED	FIFO_UNDERFLOW3_MASKED	FIFO_UNDERFLOW2_MASKED	FIFO_UNDERFLOW1_MASKED	FIFO_UNDERFLOW0_MASKED

Bits	23	22	21	20	19	18	17	16
SW Access	R			R	R		R	R
HW Access	W			W	W		W	W
Name	RESERVED_2 [23:21]			FIFO_LEVEL1_MASKED	RESERVED_1 [19:18]		FIFO_LEVEL0_MASKED	RESERVED_0

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	RESERVED_3	FIFO_LEVEL7_MASKED	FIFO_LEVEL6_MASKED	FIFO_LEVEL5_MASKED	FIFO_LEVEL4_MASKED	FIFO_LEVEL3_MASKED	FIFO_LEVEL2_MASKED	RESERVED_2

Bits	Name	Description
31	RESERVED_3	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
30	FIFO_LEVEL7_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
29	FIFO_LEVEL6_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
28	FIFO_LEVEL5_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
27	FIFO_LEVEL4_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
26	FIFO_LEVEL3_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
25	FIFO_LEVEL2_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0

28.1.124 LPPASS_MMIO_FIFO_INTR_MASKED (continued)

24 : 21	RESERVED_2	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
20	FIFO_LEVEL1_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
19 : 18	RESERVED_1	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
17	FIFO_LEVEL0_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
16	RESERVED_0	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
15	FIFO_UNDER-FLOW7_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
14	FIFO_UNDER-FLOW6_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
13	FIFO_UNDER-FLOW5_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
12	FIFO_UNDER-FLOW4_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
11	FIFO_UNDER-FLOW3_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
10	FIFO_UNDER-FLOW2_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
9	FIFO_UNDER-FLOW1_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
8	FIFO_UNDER-FLOW0_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
7	FIFO_OVER-FLOW7_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
6	FIFO_OVER-FLOW6_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
5	FIFO_OVER-FLOW5_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
4	FIFO_OVER-FLOW4_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
3	FIFO_OVER-FLOW3_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
2	FIFO_OVER-FLOW2_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
1	FIFO_OVER-FLOW1_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
0	FIFO_OVER-FLOW0_MASKED	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0

28.1.125 LPPASS_MMIO_STA_CFG

Description: FIFO configuration register.

Address: 0x42EF0400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	
HW Access	Reserved						R	
Name	Reserved [7:2]						SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1 : 0	SEL	FIFO Configuration Selection 0: FIFO configured for one 512 Entry FIFO (FIFO 0) 1: FIFO configured for two 256 Entry FIFOs: (FIFO 0-1) 2: FIFO configured for four 128 Entry FIFOs: (FIFO 0-3) 3: FIFO configured for eight 64 Entry FIFOs: (FIFO 0-7) Default Value: 0

28.1.126 LPPASS_MMIO_STA_MODE

Description: FIFO mode register.

Address: 0x42EF0404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [7:1]							RD_LOCK-OUT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	RD_LOCKOUT_EN	FIFO Read Lockout enable. This bit must be set before the chip mode transitions from active to deepsleep. This bit must be cleared before the system reads the FIFO. After changing the state of this bit, FW must poll MODE_STATUS.READ_LOCKOUT to determine when Lockout change takes effect. 0: Read Lockout disabled, FIFO contents can be read. 1: Read Lockout enabled, FIFO contents cannot be read. Default Value: 0

28.1.127 LPPASS_MMIO_STA_MODE_STATUS

Description: FIFO mode status register.

Address: 0x42EF0408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [7:1]							RD_LOCK-OUT

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
0	RD_LOCKOUT	FIFO Read Lockout status. 0: FIFO is not in Read Lockout mode. The system can read the contents of the FIFO. 1: FIFO is in Read Lockout mode. The chip can enter deepsleep mode. Default Value: 0

28.1.128 LPPASS_MMIO_STA_LEVEL0

Description: FIFO level register.

Address: 0x42EF0410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LEVEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							RW
HW Access	Reserved							R
Name	Reserved [15:9]							LEVEL

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
8 : 0	LEVEL	FIFO level set. A trigger (and optional interrupt) event occurs when USED.USED = LEVEL+1. Default Value: 0

28.1.129 LPPASS_MMIO_STA_RD_DATA0

Description: FIFO 32-bit read data register

Address: 0x42EF0430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	RESULT [31:24]							

Bits	Name	Description
31 : 0	RESULT	SAR 32-bit result. Default Value: Undefined

28.1.130 LPPASS_MMIO_STA_USED0

Description: FIFO used register

Address: 0x42EF0450

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved						R	
HW Access	Reserved						W	
Name	Reserved [15:10]						USED [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
9 : 0	USED	Number of used/occupied entries in the FIFO. Default Value: 0

28.1.131 LPPASS_MMIO_STA_STATUS0

Description: FIFO status register

Address: 0x42EF0470

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RD_PTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [15:9]							RD_PTR

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	WR_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							R
HW Access	Reserved							W
Name	Reserved [31:25]							WR_PTR

Bits	Name	Description
24 : 16	WR_PTR	FIFO write pointer: FIFO location at which a new data is written by the hardware. Note: This functionality is intended for debugging purposes. Default Value: 0
8 : 0	RD_PTR	FIFO read pointer: FIFO location from which a data is read. Note: This functionality is intended for debugging purposes. Default Value: 0

29 Low-power Comparator (LPCOMP) registers

This section discusses the LPCOMP registers. It lists all the registers in mapping tables, in address order.

29.1 Register details

Register name	Address	Description
LPCOMP_CONFIG	0x42880000	LPCOMP Configuration Register
LPCOMP_STATUS	0x42880004	LPCOMP Status Register
LPCOMP_INTR	0x42880010	LPCOMP Interrupt request register
LPCOMP_INTR_SET	0x42880014	LPCOMP Interrupt set register
LPCOMP_INTR_MASK	0x42880018	LPCOMP Interrupt request mask
LPCOMP_INTR_MASKED	0x4288001C	LPCOMP Interrupt request masked
LPCOMP_CMP0_CTRL	0x42880040	Comparator 0 control Register
LPCOMP_CMP0_SW	0x42880050	Comparator 0 switch control
LPCOMP_CMP0_SW_CLEAR	0x42880054	Comparator 0 switch control clear
LPCOMP_CMP1_CTRL	0x42880080	Comparator 1 control Register
LPCOMP_CMP1_SW	0x42880090	Comparator 1 switch control
LPCOMP_CMP1_SW_CLEAR	0x42880094	Comparator 1 switch control clear
LPCOMP_CMP0_OFFSET_TRIM	0x42880098	Comparator 0 offset trim register
LPCOMP_CMP1_OFFSET_TRIM	0x4288009C	Comparator 1 offset trim register

29.1.1 LPCOMP_CONFIG

Description: LPCOMP Configuration Register

Address: 0x42880000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	Reserved					
HW Access	R	R	Reserved					
Name	ENABLED	LPREF_EN	Reserved [29:24]					

Bits	Name	Description
31	ENABLED	- 0: LPCOMP disabled (puts analog in power down, opens all switches, all clocks turned off) - 1: LPCOMP enabled Default Value: 0
30	LPREF_EN	Enable the local reference generator circuit to generate the local Vref and Ibias. Ibias current is an alternative to the reference current IREF generated by SRSS. This bit must be set for System Deep Sleep and System Hibernate operation. Default Value: 0

29.1.2 LPCOMP_STATUS

Description: LPCOMP Status Register

Address: 0x42880004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [7:1]							OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							R
HW Access	Reserved							RW
Name	Reserved [23:17]							OUT1

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
16	OUT1	Current output value of the comparator 1. Default Value: 0
0	OUT0	Current output value of the comparator 0. Default Value: 0

29.1.3 LPCOMP_INTR

Description: LPCOMP Interrupt request register

Address: 0x42880010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1C	RW1C
HW Access	Reserved						A	A
Name	Reserved [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

29.1.4 LPCOMP_INTR_SET

Description: LPCOMP Interrupt set register

Address: 0x42880014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW1S	RW1S
HW Access	Reserved						A	A
Name	Reserved [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	COMP1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

29.1.5 LPCOMP_INTR_MASK

Description: LPCOMP Interrupt request mask

Address: 0x42880018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						RW	RW
HW Access	Reserved						R	R
Name	Reserved [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

29.1.6 LPCOMP_INTR_MASKED

Description: LPCOMP Interrupt request masked

Address: 0x4288001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved						R	R
HW Access	Reserved						W	W
Name	Reserved [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

29.1.7 LPCOMP_CMP0_CTRL

Description: Comparator 0 control Register

Address: 0x42880040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	Reserved			RW	
HW Access	R		R	Reserved			R	
Name	INTTYPE0 [7:6]		HYST0	Reserved [4:2]			MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW	RW	Reserved	
HW Access	Reserved				R	R	Reserved	
Name	Reserved [15:12]				DSI_LEV-EL0	DSI_BY-PASS0	Reserved [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	DSI_LEVEL0	Synchronous comparator output (trigger): 0=pulse 1=level Default Value: 0
10	DSI_BYPASS0	Asynchronous: bypass comparator output synchronization: 0=synchronize to system clock clk_sys (level or pulse) 1=bypass (output async) Note that in System Deep Sleep mode, this bit needs to be set to observe the output on the dedicated pin. Default Value: 0
7 : 6	INTTYPE0	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

29.1.7 LPCOMP_CMP0_CTRL (continued)

		0x3: BOTH : Both rising and falling edges
5	HYST0	Add hysteresis to the comparator. See the device datasheet for the value of comparator hysterisis voltage. 0= Disable Hysteresis 1= Enable Hysteresis Default Value: 0
1 : 0	MODE0	Power mode of the comparator. See the device datasheet for the current consumption and response time of each mode Default Value: 0 **0x0: OFF :** Off **0x1: ULP :** Ultra low power operating mode. This mode must be used for System Deep Sleep and System Hibernate operation. In this mode, local Ibias is used. **0x2: LP :** Low Power operating mode. In this mode, IREF from SRSS is used. **0x3: NORMAL :** Normal power, full speed operating mode. In this mode, IREF from SRSS is used.

29.1.8 LPCOMP_CMP0_SW

Description: Comparator 0 switch control

Address: 0x42880050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	Reserved	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	Reserved	RW1C	RW1C	RW1C
Name	CMP0_VN0	CMP0_BN0	CMP0_AN0	CMP0_IN0	Reserved	CMP0_BP0	CMP0_AP0	CMP0_IP0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	CMP0_VN0	Comparator 0 inverting terminal switch to local Vref (LPREF_EN must be set) Default Value: 0
6	CMP0_BN0	Reserved Default Value: 0
5	CMP0_AN0	Reserved Default Value: 0
4	CMP0_IN0	Comparator 0 inverting terminal isolation switch to GPIO. See the device datasheet for the location of this GPIO. Default Value: 0
2	CMP0_BP0	Reserved Default Value: 0
1	CMP0_AP0	Reserved Default Value: 0
0	CMP0_IP0	Comparator 0 non-inverting terminal isolation switch to GPIO. See the device datasheet for the location of this GPIO. Default Value: 0

29.1.9 LPCOMP_CMP0_SW_CLEAR

Description: Comparator 0 switch control clear

Address: 0x42880054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	Reserved	RW1C	RW1C	RW1C
HW Access	A	A	A	A	Reserved	A	A	A
Name	CMP0_VN0	CMP0_BN0	CMP0_AN0	CMP0_IN0	Reserved	CMP0_BP0	CMP0_AP0	CMP0_IP0

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	CMP0_VN0	see corresponding bit in CMP0_SW Default Value: 0
6	CMP0_BN0	see corresponding bit in CMP0_SW Default Value: 0
5	CMP0_AN0	see corresponding bit in CMP0_SW Default Value: 0
4	CMP0_IN0	see corresponding bit in CMP0_SW Default Value: 0
2	CMP0_BP0	see corresponding bit in CMP0_SW Default Value: 0
1	CMP0_AP0	see corresponding bit in CMP0_SW Default Value: 0
0	CMP0_IP0	see corresponding bit in CMP0_SW Default Value: 0

29.1.10 LPCOMP_CMP1_CTRL

Description: Comparator 1 control Register

Address: 0x42880080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	Reserved			RW	
HW Access	R		R	Reserved			R	
Name	INTTYPE1 [7:6]		HYST1	Reserved [4:2]			MODE1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved				RW	RW	Reserved	
HW Access	Reserved				R	R	Reserved	
Name	Reserved [15:12]				DSI_LEV-EL1	DSI_BY-PASS1	Reserved [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
11	DSI_LEVEL1	Synchronous comparator output (trigger): 0=pulse 1=level Default Value: 0
10	DSI_BYPASS1	Asynchronous: bypass comparator output synchronization: 0=synchronize to system clock clk_sys (level or pulse) 1=bypass (output async) Note that in System Deep Sleep mode, this bit needs to be set to observe the output on the dedicated pin. Default Value: 0
7 : 6	INTTYPE1	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

29.1.10 LPCOMP_CMP1_CTRL (continued)

		0x3: BOTH : Both rising and falling edges
5	HYST1	Add hysteresis to the comparator. See the device datasheet for the value of comparator hysterisis voltage. 0= Disable Hysteresis 1= Enable Hysteresis Default Value: 0
1 : 0	MODE1	Power mode of the comparator. See the device datasheet for the current consumption and response time of each mode Default Value: 0 **0x0: OFF :** Off **0x1: ULP :** Ultra low power operating mode. This mode must be used for System Deep Sleep and System Hibernate operation. In this mode, local Ibias is used. **0x2: LP :** Low Power operating mode. In this mode, IREF from SRSS is used. **0x3: NORMAL :** Normal power, full speed operating mode. In this mode, IREF from SRSS is used.

29.1.11 LPCOMP_CMP1_SW

Description: Comparator 1 switch control

Address: 0x42880090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	Reserved	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	Reserved	RW1C	RW1C	RW1C
Name	CMP1_VN1	CMP1_BN1	CMP1_AN1	CMP1_IN1	Reserved	CMP1_BP1	CMP1_AP1	CMP1_IP1

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	CMP1_VN1	Comparator 0 inverting terminal switch to local Vref (LPREF_EN must be set) Default Value: 0
6	CMP1_BN1	Reserved Default Value: 0
5	CMP1_AN1	Reserved Default Value: 0
4	CMP1_IN1	Comparator 0 inverting terminal isolation switch to GPIO. See the device datasheet for the location of this GPIO. Default Value: 0
2	CMP1_BP1	Reserved Default Value: 0
1	CMP1_AP1	Reserved Default Value: 0
0	CMP1_IP1	Comparator 0 non-inverting terminal isolation switch to GPIO. See the device datasheet for the location of this GPIO. Default Value: 0

29.1.12 LPCOMP_CMP1_SW_CLEAR

Description: Comparator 1 switch control clear

Address: 0x42880094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	Reserved	RW1C	RW1C	RW1C
HW Access	A	A	A	A	Reserved	A	A	A
Name	CMP1_VN1	CMP1_BN1	CMP1_AN1	CMP1_IN1	Reserved	CMP1_BP1	CMP1_AP1	CMP1_IP1

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
7	CMP1_VN1	see corresponding bit in CMP1_SW Default Value: 0
6	CMP1_BN1	see corresponding bit in CMP1_SW Default Value: 0
5	CMP1_AN1	see corresponding bit in CMP1_SW Default Value: 0
4	CMP1_IN1	see corresponding bit in CMP1_SW Default Value: 0
2	CMP1_BP1	see corresponding bit in CMP1_SW Default Value: 0
1	CMP1_AP1	see corresponding bit in CMP1_SW Default Value: 0
0	CMP1_IP1	see corresponding bit in CMP1_SW Default Value: 0

29.1.13 LPCOMP_CMP0_OFFSET_TRIM

Description: Comparator 0 offset trim register

Address: 0x42880098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [7:6]		CMP0_EN	CMP0_POLARITY	CMP0_MAGNITUDE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	CMP0_EN	enables CMP0 offset trim 0 = disabled 1 = enabled Default Value: 0
4	CMP0_POLARITY	polarity of CMP0 offset trim. 0 = negative 1 = positive Default Value: 0
3 : 0	CMP0_MAGNITUDE	magnitude of CMP0 offset trim. 1mV offset shift per bit. Default Value: 0

29.1.14 LPCOMP_CMP1_OFFSET_TRIM

Description: Comparator 1 offset trim register

Address: 0x4288009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	Reserved		RW	RW	RW			
HW Access	Reserved		R	R	R			
Name	Reserved [7:6]		CMP1_EN	CMP1_POLARITY	CMP1_MAGNITUDE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	Reserved							
HW Access	Reserved							
Name	Reserved [31:24]							

Bits	Name	Description
5	CMP1_EN	enables CMP1 offset trim 0 = disabled 1 = enabled Default Value: 0
4	CMP1_POLARITY	polarity of CMP1 offset trim. 0 = negative 1 = positive Default Value: 0
3 : 0	CMP1_MAGNITUDE	magnitude of CMP1 offset trim. 1mV offset shift per bit. Default Value: 0

Revision history

Document revision	Date	Description of changes
**	2025-09-05	Initial release.

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Edition 2025-09-05
Published by

Infineon Technologies AG
81726 Munich, Germany

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Document reference
002-38897 Rev. **

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